Calypso/Iota/Clara System Application Note

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NOTES :

1. Creation
2. RF and BCI application part rework
3. Minor wording change, sleep timing update, LDO voltage update,SIM schematic correction

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Reference documents:

[1] TWL3014	IOTA Data Manual SWRS010	
[2] TRF6150	CLARA Specification	ver 2.5
[3] HERCROM400G2	CALYPSO Specification CAL000	ver 0.5
[4] ULYS015	Ultra Low Power Down Controller	ver 1.1
[5] ULYS002	Activity control management	ver 1.1
[6] MB84VD2108/9X-85	Stacked MCP Flash memory and SRAM specifications	

Glossary:

ABB	Analog Base Band
DBB	Digital Base Band
LMM	Lead Mega Module
SM	State Machine
MB	Main Battery
BB	Back-up Battery
BG	Band Gap
ACTIVMCLK	This bit at logical 1 indicates to the ABB that a stable 13Mhz is available to the system

1 Introduction

Scope of this specification is to give a system point of view of TI GSM chipset solution . This specification will cover application aspect of a GSM system based on the three TI chips Calypso, Iota, Clara that build up the TI GSM chipset solution.

1.1 Calypso

HERCROM 400G2 [3] is a chip implementing the digital base-band processes of a GSM/GPRS mobile phone. This chip combines a DSP sub-chip (LEAD2 CPU) with its program and data memories, a Micro-Controller core with emulation facilities (ARM7TDMIE), internal 8Kb of Boot ROM memory, 4M bit SRAM memory, a clock squarer cell, several compiled single-port or 2-ports RAM and CMOS gates.
The application of this circuit is the management of the GSM/GPRS base-band processes through the GSM layer 1, 2 and 3 protocols as described in the ETSI standard with a specific attention to the power consumption in both GSM dedicated and idle modes, and GPRS (class 12) capability.

1.2 Iota

TWL3014 chip [1] includes a complete set of baseband functions to perform the interface and processing of voice signals, interface and processing of baseband in-phase (I) and quadrature (Q) signals which support single-slot and multi-slot mode, associated auxiliary RF control features, supply voltage regulation, battery charging control and switch ON/OFF system analysis.

1.3 Clara

The TRF6150 [2] is a triple band transceiver IC suitable for GSM, DCS and PCS GPRS class 12 applications.
The chip integrates:

- the receiver based on direct conversion architecture,
- the transmitter based on the modulation loop architecture,
- the frequency synthesis including an auxiliary N-integer synthesizer,
- a main N-fractional synthesizer,
- an IF VCO and RF VCO,
- the voltage regulators to supply on chip and off chip RF functions
- a power amplifier controller.

Few external components are required for a dual band application as a power amplifier, a switchplexer, only one dual band VCO and two front end filters.

2 System connections

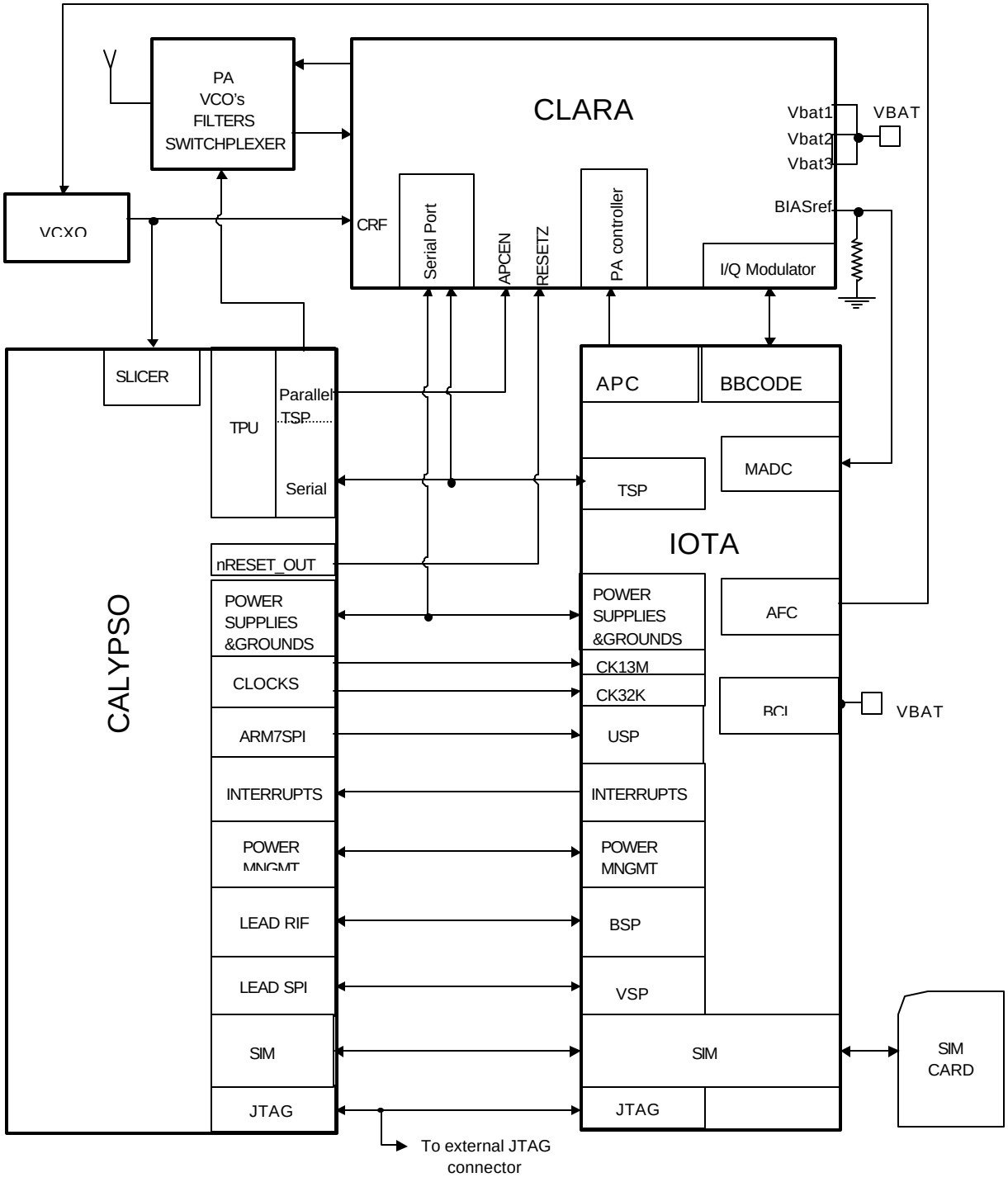


Figure 2-1 System connections

2.1 Calypso to Clara

Table 2-1 Calypso to Clara connections

CALYPSO			CLARA			Comments
Pin Name	Pin nb	Ball	Pin Name	Pin nb	Ball	
nRESET_OUT	45	N2	RESETZ	17	-	Serial port register reset
TSPDO	109	H11	DAT	12	-	TSP serial interface to Clara
TSPEN(1) [1]	111	H12	EN	13	-	TSP serial interface to Clara
TSPCLKX	107	J14	CLK	11		TSP serial interface to Clara
TSPACT(11)[2]	106	J13	APCEN	9	-	APC Enable signal

WARNING: Pin number and ball reference may not be updated. Please refer to latest spec version of Calypso and Clara

Calypso to Clara connections consist in few signals mainly dedicated to serial programmation of the Clara chip through the TSP. The TSP port is controlled by the TPU hence Clara register programmation is executed synchronously to the GSM time-base with a resolution of a GSM quarter of bit. For Clara register, data format and serial interface programming refer to CLA000 specification [2].
Also Clara serial interface reset is controlled by the Calypso reset signal for external peripheral and a TSPACT signal, generated by the parallel part of the TSP, provides an APC enable signal required by Clara with a GSM quarter bit resolution.

2.2 Iota to Clara

Table 2-2 Iota to Clara connections

IOTA			CLARA			Comments
Pin Name	Pin nb	Ball	Pin Name	Pin nb	Ball	
BULQM	73	C9	QN	18	-	I/Q UL&DL signals[3] [4]
BULQP	72	C10	QP	19	-	I/Q UL&DL signals
BULIM	69	D10	IN	20	-	I/Q UL&DL signals
BULIP	70	D9	IP	21	-	I/Q UL&DL signals
APC	32	K4	APC	8	-	PA envelope signal
VRIO2	2	B1	VR4in	10	-	Serial interface supply voltage
ADIN3	83	C7	BIASref	31	-	External current setting resistor
VBAT	94	A4	Vbat1	50	-	Reg1 battery supply voltage
			Vbat2	6	-	Reg2 battery supply voltage
			Vbat3	61	-	Reg3 battery supply voltage

WARNING: Pin number and ball reference may not be updated. Please refer to latest spec version of Iota and Clara

Iota to Clara connections include the I/Q Uplink and Downlink signals, the Automatic Power Control signal, the temperature sensor signal, serial interface supply connection and battery supply voltage connection.
The APC signal of Iota APC module is used by the CLARA PA controller to generate a smooth PA control signal. Shapes, delays and levels for this signal are managed by DBB through the programmation of APC module.

[1] Choice of TSPEN(x) can be done in order to ease PCB connections
[2] Choice of TSPACT(x) can be done in order to ease PCB connections
[3] Direct connection is done between the four wires Iota UL path and Clara UL/DL path.
[4] UL to DL path switch must be implemented in SW

The VRIO signal is the Iota power supply regulator output for IO's. It supplies the CLARA serial interface IO's as the CALYPSO TSP IO's in order to have serial connection on the same supply domain.
The ADIN3 to BIASref connection allows RF chip temperature measurements.
The VBAT connections is not an effective Iota to Clara connection as the battery pack is external, it has been added to this table to highlight the fact that Clara regulators are directly linked to the Main Battery.

2.3 Calypso to Iota

Table 2-3 Calypso to Iota connections

CALYPSO			IOTA			Comments
Pin Name	Pin nb	Ball	Pin Name	Pin nb	Ball	
TSP Serial interface						
TSPDO	109	H11	TDR	21	G3	
TSPEN(0)	110	H13	TEN	22	H1	
RIF/BSP Serial interface						
BFSR	86	L11	BFSX	27	K2	
BDR	82	K10	BDX	26	J1	
BFSX	87	P12	BFSR	29	H3	
BDX	85	M11	BDR	28	J3	
ARM SPI/USP Serial Interface						
MCUDI	66	N7	UDX	35	J5	Tristate when not enabled[5]
MCUDO	67	M7	UDR	34	K5	
MCUEN(0)	68	M8	UEN	39	K6	
LEAD SPI/VSP						
VCLKRX	88	N12	VCK	30	K3	
VDX	91	P14	VDR	41	H5	
VDR	90	N13	VDX	37	F5	
VFSRX	92	M13	VFS	36	G5	
SIM Interface						
SIM_CLK	119	F13	DBBSCK	17	F4	
SIM_IO	115	G13	DBBSIO	13	E5	
SIM_RST	117	G10	DBBSRST	18	G4	
JTAG Interface						
TDO	147	C10	TDI	68	D7	
TMS	148	E9	TMS	66	E8	Ext connection to JTAG controller
TCK	145	B10	TCK	71	D8	Ext connection to JTAG controller
TDI	144	D10				Ext connection to JTAG controller
			TDO	67	E7	Ext connection to JTAG controller
CLOCKS						
CLK32K_OUT	132	C12	CK32K	10	E2	
CLK13M_OUT	120	F12	CK13M	12	E4	
INTERRUPTS						
EXT_IRQ	42	M3	INT2	88	E6	
EXT_FIQ	44	P1	INT1	41	H6	
POWER MGMT						
ITWAKEUP	131	B14	ITWAKEUP	6	D2	
ON_OFF	126	F10	ONNOFF	11	E3	
RESPWRONZ	129	D12	RESPWONZ	8	D3	

WARNING: Pin number and ball reference may not be updated. Please refer to latest spec version of Calypso and Iota

[5] To avoid current consumption a pull down must be added on this line.

CALYPSO			IOTA			Comments
Pin Name	Pin nb	Ball	Pin Name	Pin nb	Ball	
POWER SUPPLIES						
VDD	13	E1	VRDBB Sense on VSDBB	24	J1	
	40	M1				
	65	P7				
	94	N14		23	H2	
	137	B12				
	169	A5				
VDD-RTC	127	D14	VRRTC	7	D1	
VDDS-RTC	128	D13	VRRTC	7	D1	
VDDS-MIF	8	D1	VRMEM	19	G1	
	22	G1				
	164	B6				
	173	A4				
VDDS1	55 98	N5 L14	VRIO2 Sense on VRIO1	2	B1	
VDDS2	142	A11		1	B2	
VDDPLL	121	F11	VRDBB	24	J1	
VDDANG	125	E11	VRIO2	2	B1	

WARNING: Pin number and ball reference may not be updated. Please refer to latest spec version of Calypso and Iota

2.3.1 TSP serial interface

The TSP serial interface allows the serial transmission of baseband control windows for the Iota BBCODEC. It is managed through a TPU scenario hence it allows GSM quarter bit resolution and a precise positioning of CODEC commands among the GSM TDMA frame.
Data format for this transmission is seven bits including UL/DL commands (On, Calibrate, Enable) and a start bit for ADC conversion. This command bit allows to place at precise moments in the TDMA frame the start of the ADC conversion.
Iota register are not accessible through this serial link, sense of transmission is from Calypso to Iota only.
Clara serial interface is also connected to Calypso TSP. Through this link the Calypso device programs Clara register in order to control regulators, synthesizers, the receiver, the offset PLL and the P.A. controller.
TSP serial clock runs at 6.5MHz.

2.3.2 RIF/BSP se rial interface

This interface is dedicated to the UL and DL transmission of I/Q samples between the DSP and the BBCODEC and to Iota register access.
On the UL path the DSP sends to the CODEC the burst bits to be modulated while on the DL path it receives non demodulated I/Q samples.
Write access to Iota register is done using the same data format as the UL. Main functions executed are:

- APC parameters programmation (levels, delays, ramp coefficients)
- AFC
- Voice CODEC control

No Iota read accesses are performed in current SW implementation through this interface.
Register accesses could be considered synchronized to the TDMA frame as the DSP receives commands on TDMA frame start boundary.

Clock frequency of RIF/BSP serial link is 13 MHz.
BSP access are not allowed when ACTIVMCLK='0'.

2.3.3 ARM SPI/USP serial interface

This interface is dedicated to Iota read and write register accesses from Calypso. Through this link is possible to access all Iota register, hence this port is used to configure and to manage the status of each block of Iota device. Also ADC result of conversion can be read through this interface. This access is asynchronous to the TDMA frame and has a higher priority than the BSP access. Possible conflicts due to simultaneous access from ARM SPI and LEAD RIF are managed by the Iota IBIC. This serial link runs at 13 MHz.

2.3.4 LEAD SPI/VSP serial interface

This interface allows voice samples exchanges in DL and UL direction between the DSP and the Iota Voice Band CODEC. Iota VSP is the master port in the transmission, serial link runs at 500 kHz.

2.3.5 SIM interface

The Sim Card digital interface in ABB insures the translation of logic levels between DBB and Sim Card, for the transmission of 3 different signals:

- A clock derived from a clock elaborated in DBB, to the Sim-Card (DBBSCK ⇨ SIM_CK)
- A reset signal from DBB to the Sim Card (DBBSRST ⇨ SIM_RST),
- A serial data from DBB to the Sim Card (DBBSIO ⇔ SIM_IO) and vice-versa.

The SIM card interface can be programmed to drive a 1.8V or 3V Sim Card.

2.3.6 JTAG interface

The test access port (TAP) meets JTAG testability standard (IEEE Std1131.1-1990). TAP allows public instructions set of JTAG standard and also private instructions to configure the device in special modes for test or debug purpose.

2.3.7 CLOCKS

Iota device receives two clocks from Calypso:

- A slow clock CLK32K_OUT used by the DBB as reference clock for low power modes (back-up, deep-sleep).
  The ABB adopt this clock as the VRPC synchronous state machine clock and as reference clock when fast clock is not present.

- A fast clock CLK13M_OUT used by the DBB and ABB as reference clock for all modules including serial transmission[6].

[6] This means that a single fast clock signal only goes from DBB to ABB. All serial interfaces adopt this clock as reference clock, no need to include a clock signal in each port connection.

2.3.8 INTERRUPTS

Iota device is able to generate two kinds of interrupts:

- An emergency interrupt connected to Calypso EXT_FIQ signaling the detection of a low battery voltage.

- An event detection interrupt connected to Calypso EXT_IRQ signaling :
  - Falling or rising edge at RPWON pin.
  - Falling edge at PWON pin.
  - Termination of an analog to digital conversion.
  - Charger plug.

2.3.9 POWER MGMNT

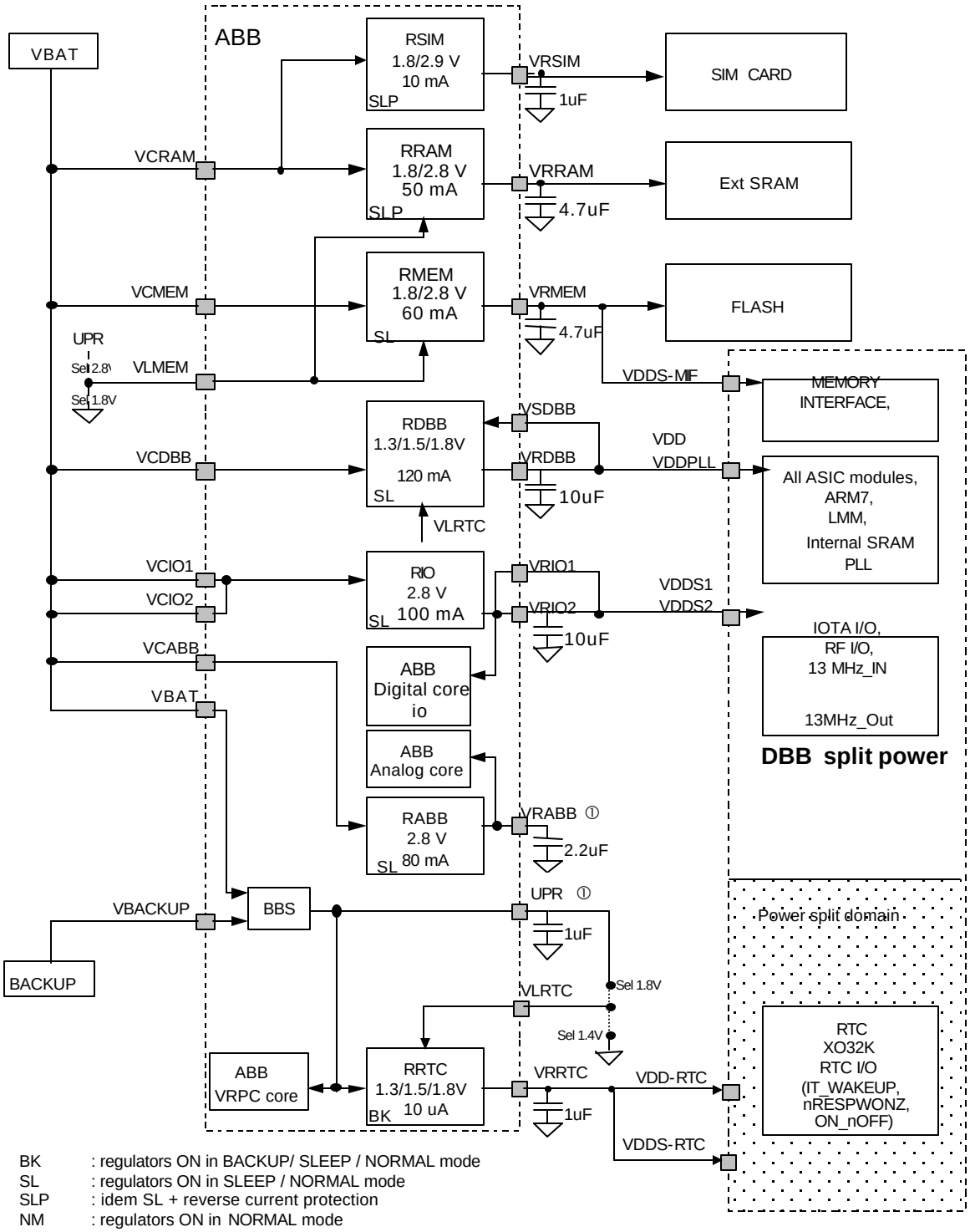
Those three signals controls system status and system status transitions, they are supplied on the VRRTC power domain.

The nRESPWONZ signal is generated by the ABB, it is the reset of the power split part of the DBB chip. It is active only one time (as long any kind of supply, BB or MB is present) at the first start of the mobile. Split power logic will provide to propagate this signal as global reset as soon as power supply will be present on the rest of the chip.

The ON_nOFF signal is generated by the ABB, it is the ASIC modules, ARM, LMM, reset.
It is at logical low level each time the system is switched off. Also this signal is managed by the split power logic and propagated to the rest of the circuit.
High logical level is asserted on this signal when the Iota power management has completed the enabling sequence of all LDO's meaning that the system is correctly supplied and that SW can be correctly executed.
At this time the MCU SW starts from its reset state.

The ITWAKEUP signal is generated by the DBB and it is used to wake up the system from low power modes (backup, deep sleep). It is built as a combination of all the interrupt request that are allowed to awake the Calypso ULPD module and the RTC alarm.

2.3.10 POWER supplies



BK : regulators ON in BACKUP/ SLEEP / NORMAL mode
SL : regulators ON in SLEEP / NORMAL mode
SLP : idem SL + reverse current protection
NM : regulators ON in NORMAL mode
① :

reserved for ABB private use only

Figure 2-2 Iota to Calypso supply connections

The schematic above shows Iota to Calypso power supply connections. Items to be highlighted on that schematic are the following:

- All main regulators have as non-regulated input the VBAT pin. Hence while MB is not connected no supply will be provided at the output of those LDO's.
- The back up regulator RRTC has as non-regulated input either the MB or BB, it is always enabled and provides supply to the Calypso "power split" domain on every functional mode of the system.
- Default voltage value for both RRTC and RDBB can be selected between 1.5V and 1.8V through the VLRTC input pin.
- Default voltage value of RMEM can be selected between 2.8V and 1.8V through the VLMEM input pin.
- RDBB regulator allows external voltage sensing for sharper regulation on the VSDBB input pin. This allows to eliminate of the pad and wire connection drop to the Calypso power supply input. To make this feature effective, return sense point must be chosen as next as possible to Calypso input.
- In Iota to Calypso application RTC I/O's level shifters are used with same voltage value at both sides => VDD-RTC = VDDS-RTC = 1.8V.

2.3.11 Calypso Supplies voltages rules

The Calypso device has five different Power domains corresponding to the following IOTA supplies:

A : RTC core domain	=> RRTC	1.5V – 1.8V depending on VLRTC connection
B: ASIC core domain	=> RDBB	1.5V – 1.8V depending on VLMEM connection
C: RTC I/O domain	=> RRTC	1.5V – 1.8V depending on VLRTC connection
D: ASIC I/O domain	=> RIO 2.8V	
E: Memory interface	=> RMEM	1.8V – 2.8V depending on VLMEM connection

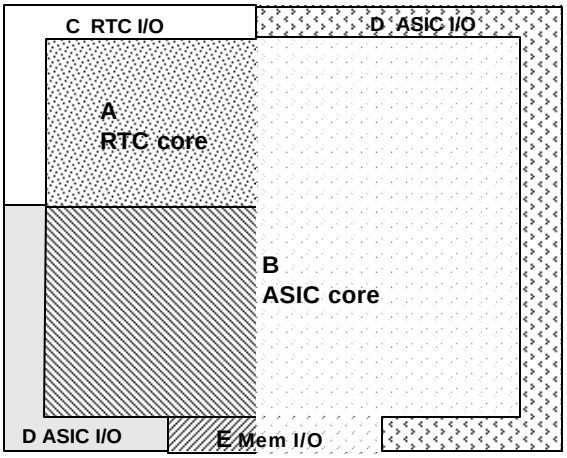


Figure 2-3 Calypso Power domains

To avoid current leakage at the interface A B the supply voltage of A domain must always be higher or equal to the B domain one.

For that reason the VLRTC input pin of IOTA is used to select the default-regulated voltage of both RRTC and RDBB regulators.
Also user SW must take care of never break the above rule, as the RRTC and RDBB output voltage values could be independently selected by SW.

3 Power split concept in Calypso-Iota systems

To have a minimum of consumption during OFF state in mobile equipment, only the active logic elements have to be supplied. Those blocks in a mobile application are the RTC (Real Time Clock) module, the XO32K (32 kHz oscillator) module and the INTH (Interrupt Handler) for the DBB part and the POR (Power On Reset) logic and a dedicated LDO in the ABB part .
This approach is possible by using Calypso Split Power feature together with the Iota dedicated regulator VRRTC.

In Calypso the core power domain is split in two sub domains powered with different voltage supplies. Those two domains can be selectively powered allowing the shut down of all those blocks not involved in OFF state logic functions.
Tactical cells realize the separation between the un-supplied part of the core and the active domain in order to avoid any current leakage between supply domains.
A POWERDOWN signal generated by the split control logic allows the isolation of the RTC and split domain from the rest of the circuit. This signal is active when the ON_nOFF signal coming from Iota is at low level indicating that main regulators are disabled.
The RESPWONZ signal is used to reset the RTC, the Split power logic and the XO32K module.
The external interface of split domains adopts level shifter I/O's this to allow compatibility with Nausica device. Note that in Iota/Calypso systems this feature is not used because split core is supplied at the same voltage of external I/O's

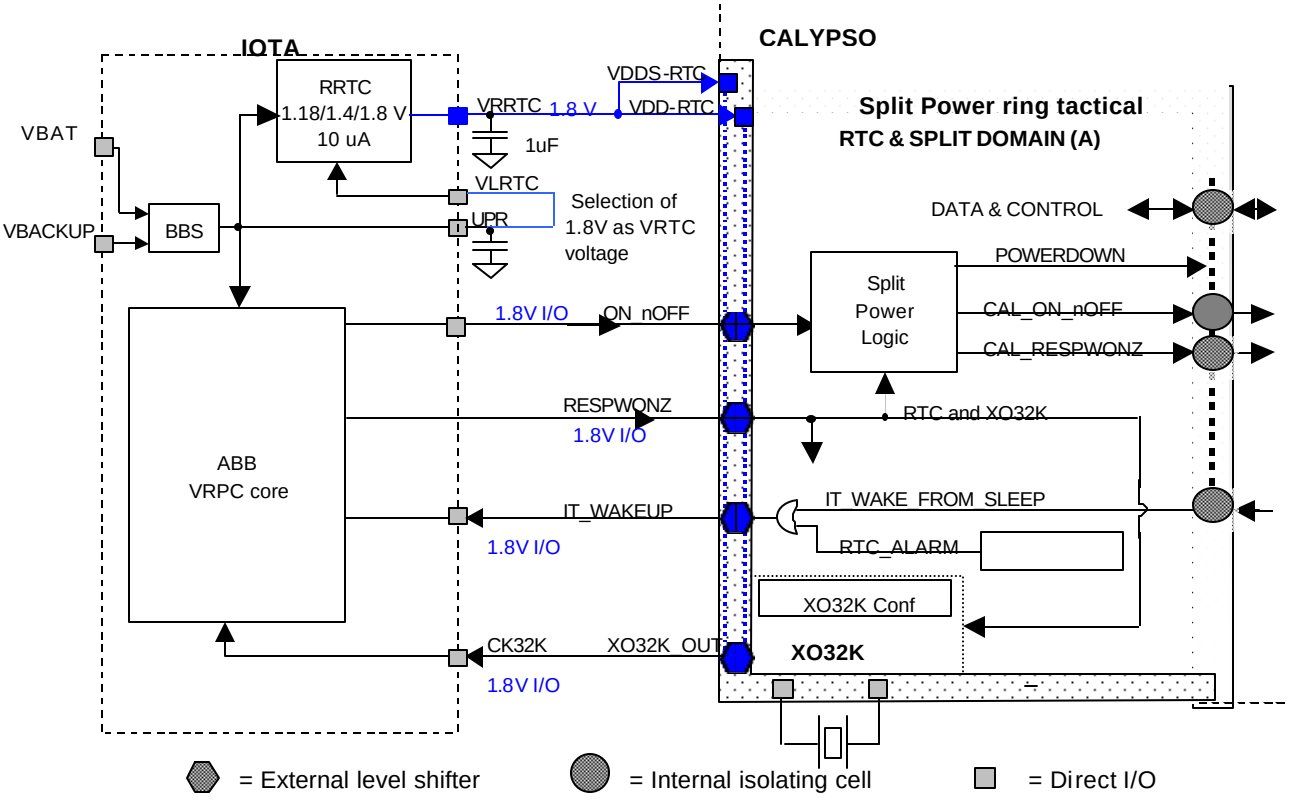


Figure 3-1 Power Split supply connections

Iota device dedicates a special low consumption LDO RRTC for split domain only. This LDO supplies:

- The VRPC digital core
- The power management I/O of Iota and Calypso split domain
- The split supply core (RTC and XO32K)

This regulator is always enabled and has a limited current drive capability(30uA).
Hence as soon as a MB or a BB battery are connected to Iota the VRRTC regulator will provide supply to the 32K oscillator and to the RTC.

3.1 System Power On Reset generation

The RESPWONZ signal is used as reset for the Iota VRPC SM and for Calypso RTC, Split power logic and the XO32K module.

The nRESPWONZ signal is held in a low state until both conditions below are not matched:

- The VRRTC regulator is at the nominal regulated voltage.
- The UPR voltage is higher than 2.6V

This to allow internal digital VRPC logic reset and external RTC and XO32K modules reset.
Once this signal has been released the XO32K modules starts providing the OSC32K_OUT signal to Iota. This clock is used by the VRPC synchronous state machine.

Simulation diagram below illustrate the nRESPWONZ signal logic behavior (POR_PAD in the plot) related to the VRRTC output voltage (VREG in the plot).

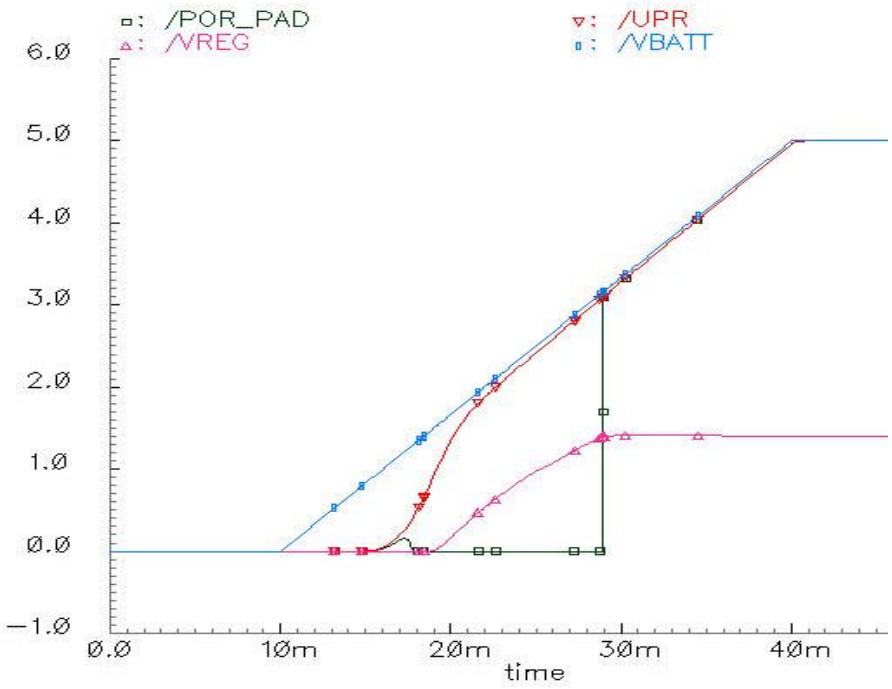


Figure 3-2 RESPWONZ signal behavior at first power up

Simulation conditions are :

- 1uF on VRRTC_OUT
- 10 uF on UPR
- rise time of the battery from 0V to 5V 30 ms.

In this example the nRESPWONZ signal is released only when the VRRTC regulator has reached its nominal voltage. Correct reset of the split part of Calypso is effective when split core is supplied with 80% of the nominal voltage and nRESPWONZ signal is held low for at least 5 ns. This is the case in the diagram above.

For what concern decreasing value of UPR the nRESPWONZ signal is forced to logic zero when the UPR voltage goes below 2.1V. This will reset the whole system.

4 System modes

In the following paragraphs are illustrated the different operating modes of the mobile. First objective of this analysis is to define the modes and to state which are the working blocks on each of them. Next chapters then, will consider system transitions between operating modes and current consumption evaluation of the system in most of them.

4.1 No Supply

This mode is characterized by the lack of supply sources neither from MB nor from BB. It can be the case of missing batteries or flat batteries. All ABB register are in reset state, DBB is forced to reset.

4.2 Active

Activity of the system is tightly linked to the state of the voltage regulators that provide current. Two chips, in the proposed chipset solution, have embedded regulators: Iota and Clara
While in Clara device LDO's are exclusively dedicated to the RF part of the system and their enable is related to RF periods of activity, Iota ones are used to supply both the DBB and the ABB part of the chipset. Thus any SW control activity on the system could be possible only when those regulators are active.
First definition of the active mode hence could be the following: System is in active mode when both Iota and Clara LDO's are enabled and SW is able to manage GSM activity.
Once Iota regulators are enabled and the Switch ON procedure terminated, SW becomes the system master ant it is its own choice to select operating modules depending on the application.
MB values allowing the system to stay in active mode are MB > 2.8V

4.3 Off

This mode is characterized by the presence of a charged MB (MB > 3.2V) and by the disabled state of Iota LDO's[7]. In this condition system is ready to accept a switch on command to pass in active mode. The ON_nOFF signal is at low level indicating to the DBB that LDO's are not able to deliver nominal current and isolating the split domain from the rest of the Calypso chip.
The system active blocks in this mode are:

Iota:
- VRRTC regulator
- POR logic
- BBSWITCH logic
- Power management I/O's (RESPWONZ, ON_nOFF, IT_WAKEUP)
- LDO's programmed to stay in SLEEP mode

Calypso:
- RTC
- XO32K
- Power split Logic
- Split I/O

Clara:
- None

[7] In OFF state RDBB,RMEM,RRAM,RIO,RSIM and RABB could stay in Sleep mode if selected through the MSKOFF register. In this mode LDO's max deliverable current is 1 mA.

4.4 Backup

This mode is characterized by the fact that the supply source of the system is the BB or a MB below 3.2V. In this state only the minimal mobile functionality's are still alive, the real time clock RTC, the POR logic and on some architectures the SRAM backup supply. Any switch on command in this state will be ignored.
The ON_nOFF signal is low, and the Calypso split domain isolated.

4.5 Sleep

System sleep mode is characterized by a low consumption state of Iota regulators. Although still enabled Iota LDO's are no longer able to provide the full active rated current. They keep the regulated voltage with a reduced maximum rated output current of 1mA.
This allows the system to freeze its configuration during inactivity periods.
In this mode in fact the ON_nOFF signals stays at high logical level (no register reset is asserted) but application SW is no longer enabled to run. This mode has been expressly conceived for system current consumption reduction during inactive periods of mobile paging mode and to support the L1 Deep Sleep SW mode.
Also in Sleep mode Iota main band gap is off, reference for regulators is provided by a local band gap.

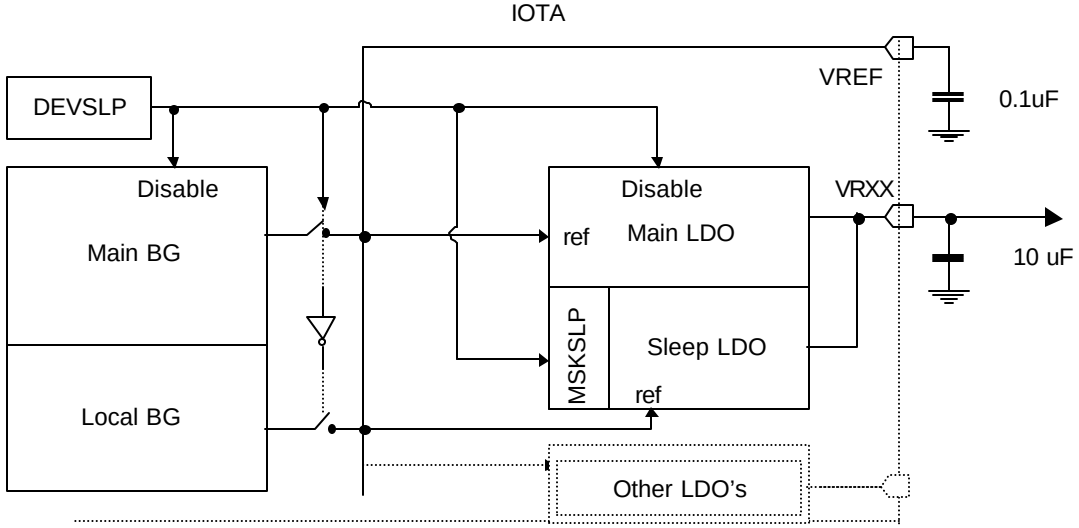


Figure 4-1 LDO BG reference during SLEEP mode

In Sleep mode current consumption is limited to the consumption of the local bangap and of the sleep regulator. Advantage of this architecture is that the external capacitors on regulator outputs and on VREF pins keep the charge during sleep mode allowing a quick re-start of LDO and main bangap entering the active mode.
Iota LDO's supporting the sleep feature are: RSIM, RRAM, RMEM, RDBB, RIO and RABB.
By default the RABB LDO is set in off mode when the system enters the SLEEP mode, while all the others stay active in the low current consumption mode. Different behavior of LDO's could be configured through VRPCMSK register. Selected regulators (MSKSLP = 1) will be disabled entering in sleep mode.

Active blocks in this mode are:

Iota:
- VRRTC regulator
- POR logic
- Power management I/O's (RESPWONZ, ON_nOFF, IT_WAKEUP)
- MB vs BB comparator
- Sleep LDO's
- Local bandgap
- BB charge (if enabled)

Calypso:
- RTC
- XO32K
- Power split Logic
- ULPD
- INTH
- All supply domains are powered but no current sink is allowed

Clara:
- Serial Port

5 System transitions between operating modes

The flow chart below describes system states transitions and their driving events. Following paragraphs will detail driving events.

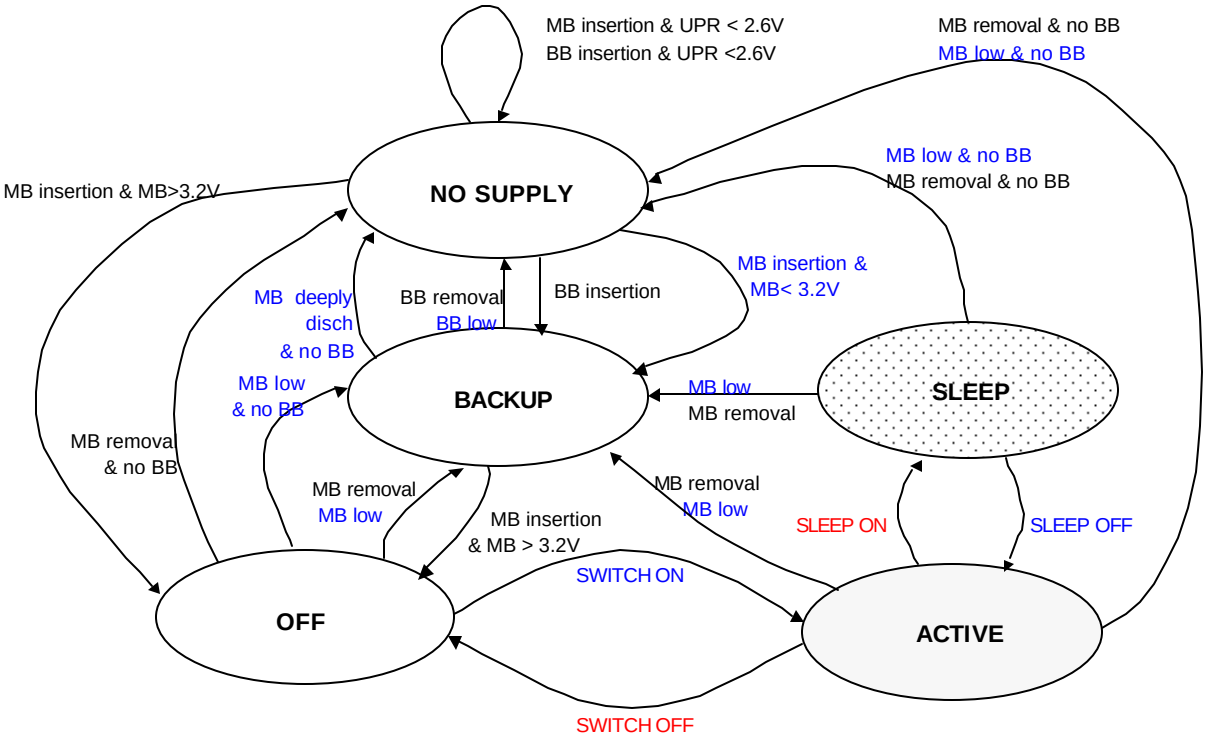


Figure 5-1 System operating modes transitions

NO SUPPLY	UPR<2.6V, ON_nOFF = 0, nRESPWONZ = 0
BACKUP	UPR<3.2V, start conditions not accepted, ON_nOFF = 0, Calypso split isolated
OFF	UPR>3.2V, start condition accepted, ON_nOFF = 0
ACTIVE	UPR>2.8V[8], SW control of the system, ON_nOFF = 1

SLE

In RED characters : SW driven transitions
In BLUE characters : HW detection driven transitions
In BLACK characters : Supply insertion/removal driven transitions

A high logic level of the ON_nOFF signal characterizes shaded states

[8]The system is designed to work correctly down to 3V battery value. In GSM application battery voltage is highly noised by the voltage drop induced by the PA (300-400 mV of battery drop during busrt emission).Hence GSM application SW decides to pass in OFF state long time before the battery voltage reaches 3V.

5.1 Supply insertion/removal driven transitions

The Iota device has a dedicated logic to manage system states depending on the presence of main and back up batteries. The VRPC state machine is able to detect MB and BB presence and their voltage level and to condition system behavior through the RESPWONZ and ON_nOFF outputs.
For design constraints when the system is conceived to work without BB the Iota VBKUP pin must be connected to VBAT.
Description of the following transitions consider this connection present when no BB is used.

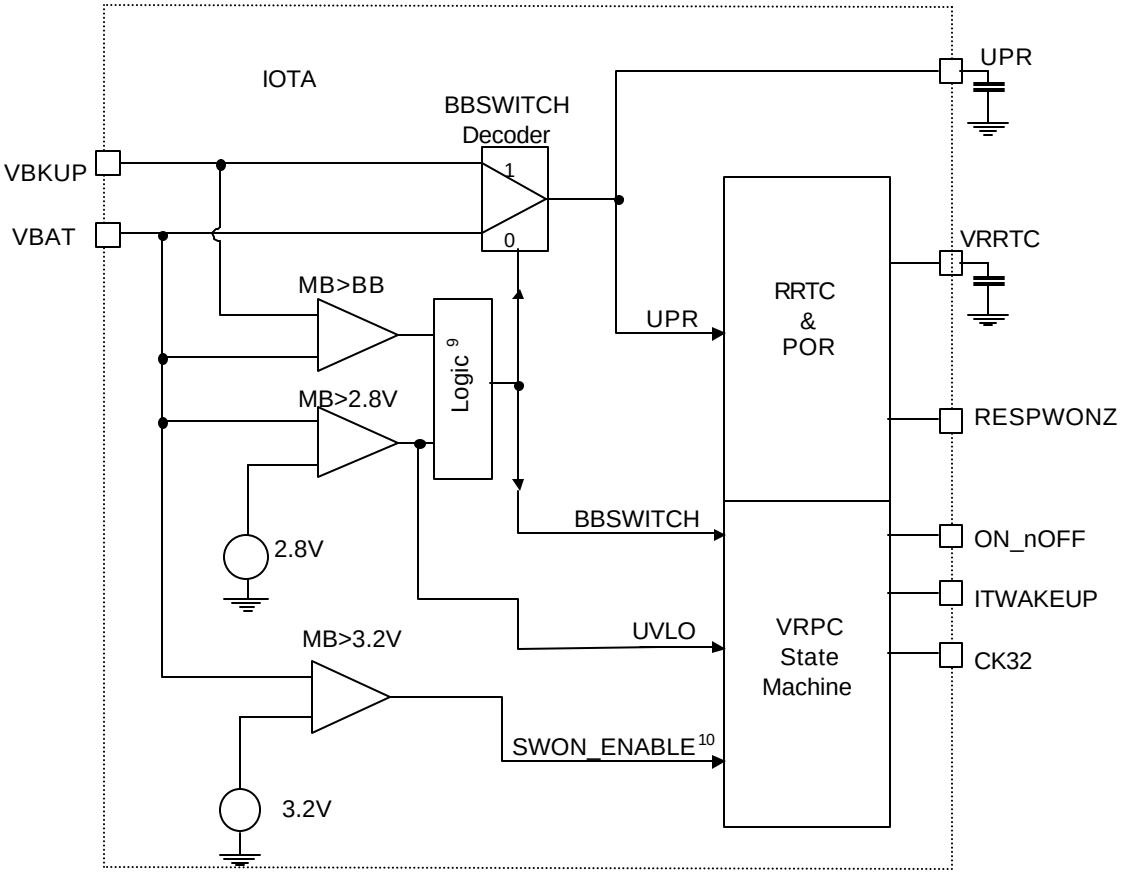


Figure 5-2 Iota BBSWITCH and VRPC State Machine

9 BBSWITCH = 1 if MB<BB & MB<2.8V
10 SWON_ENABLE conditions VRPC SM switch on sequence to the voltage of MB. Only if MB>3.2V switch on is allowed.

5.1.1 MB insertion

Three cases are possible:

1) System is not using BB (VBAT is connected to VBKUP) inserted battery is charged (MB> 3.2V).
   MB insertion from a NO SUPPLY state produces a first start of mobile, a so-called POWER ON, and the mobile passes in OFF state.
   The POR(Power On Reset) logic generates the RESPWON signal to reset internal VRPC logic and to Calypso split domain once the RRTC LDO has reached its nominal voltage. The VRPC state machine receives the 32K clock from Calypso XO32K supplied by the RRTC regulator and it is ready to accept a switch on conditions as MB value is higher than 3.2V(SWON_ENABLE). The ON_nOFF signal stays at low logical level indicating that no switch on condition has been detected.
   The BBSWITCH signal assumes the low logical level allowing the UPR to be supplied by the MB

2) System is using BB but it is not present at a fully charged MB insertion.

   This is an abnormal working configuration because VBKP pin must not be left floating. Nevertheless this configuration will not create problems as long as the MB is above 2.8V. For MB values below this threshold the BBSWITCH logic may become sensible to the VBCKUP floating input and generate some undesired switch of the MB/BB decoder. This will impact the UPR voltage compromising the whole behavior of the system.

3) BB present at MB>3.2V insertion.

   The insertion of a charged MB will make the system pass from the BACKUP state to the OFF state. The BBSWITCH signal will keep the low logic level signaling to the BBSWITCH decoder to switch on MB and to the VRPC SM that is possible to accept switch on events. The signal ON_nOFF stays at low level.

At the insertion of a MB the system will pass in OFF state if MB>3.2V as described for the three cases above or in BACKUP state if 2.6V<MB<3.2V. If MB<2.6V system stays in NO SUPPLY state.

5.1.2 BB insertion

Assuming that the system is in a NO SUPPLY mode and that BB is fully charged, the BB insertion generates the transition to the BACKUP mode.
As in the case of MB insertion from a NO SUPPLY condition this will generate a POWER ON of the system (first start). The POR (Power On Reset) logic generates the RESPWON signal to reset internal VRPC logic and to Calypso split domain once the RRTC LDO has reached its nominal voltage. The VRPC state machine receives the 32K clock from Calypso XO32K supplied by the RRTC regulator but it is not sensible to switch on events because SM inputs indicate that there is not MB. The signal ON_nOFF stays at low level.
System stays in NO SUPPLY state if BB voltage is not enough to bring the UPR voltage above 2.6V.

5.1.3 MB removal

The MB removal will bring the system in one of the two states NO SUPPLY or BACKUP depending by the presence of a BB battery. Removing MB while the system is in SLEEP or ACTIVE state will make Iota generate an INT1 to the DBB signaling that an EMERGENCY condition has occurred. The DBB is not able to treat this interrupt while in SLEEP mode.
This is possible only during active periods. From the interrupt generation the Iota VRPC SM gives the system a 150 us[11] timeout after which all regulators (except RRTC) are disabled.

5.1.4 BB removal

Assuming the system in BACKUP mode BB removal bring the system in NO SUPPLY state.

5.2 HW driven transitions

HW driven transitions includes state changes due to detection of HW events, as BB or MB discharge below a given threshold, and switch on events. While the first are to be considered as a safety feature of the system preventing faulty SW execution due to sudden lack of supply and the over-discharge of the batteries latter are to be considered as state changes due to external stimulus (SWITCH ON) or system power management stimulus (SLEEP OFF)

5.2.1 MB low

The Iota power management reacts to MB low condition depending on the system state in which this condition has been detected and on the presence/lack of a charged BB.
Also the condition “MB low” could be associated to different threshold values of the battery depending again on the system state.
MB low condition detected in:

- **OFF state**

  For this state the MB low condition consists in the detection of MB voltage under the 3.2V threshold (SWON_ENABLE threshold).
  The VRPC SM blocks switch on condition sensitivity and the system passes into BACKUP mode. Main regulators programmed to stay in sleep mode during OFF state remain enabled and still supplied on the MB.

- **ACTIVE state**

  For this state the MB low condition consists in the detection of MB voltage under the 2.8V threshold (UVLO threshold).

  Charged BB present:
  The UVLO comparator detects that MB voltage has undergone the 2.8V threshold. BBSWITCH signal is set to logic one because both conditions MB<2.8V & MB<BB are valid.

  The VRPC SM :
  - clears the MSKOFF register
  - generates an INT1 signaling the EMERGENCY condition
  - starts the 150 us watchdog timer.

  At the end of the WD count
  - sets the ON_nOFF signal to logic zero

[11] This value is strongly dependent on the amount of charge stored in LDO’s external capacitors and on system consumption.

- disables LDO's using MSKOFF register (previously cleared => cuts all

- disables Iota Band Gap.

In this configuration Iota UPR line is powered on BB. System passes to BACKUP state.
During the Watchdog interval application SW has 150 us[11] corresponding to 1950 13MHz clock cycles to treat the INT1 and execute possible configuration accesses in order to enter the BACKUP state.

No BB: Same as above, the only differentiating factor is that BBSWITCH never passes to logic one thus UPR line is always supplied by the MB

- **SLEEP state**

  Same as ACTIVE state. The SW does not take INT1 generation in account.

- **BAKUP state**

  For this state the MB low condition consists in the detection of MB voltage under the 2.8V threshold (UVLO threshold). Main regulators previously programmed to stay in sleep mode during OFF and BACKUP state remain enabled but they are no longer able to provide a regulated output. They will still sink current from MB following its decreasing value.

  Charged BB present: BBSWITCH signal is set to logic one because both conditions MB<2.8V & MB<BB are valid. System stays in BACKUP state but UPR is now provided by the BB.

  No BB: No action on BBSWITCH UPR is still supplied by MB, system stays in BACKUP.

5.2.2 BB low

This event generate a system state transition to NO SUPPLY in the case system is in BACKUP state and MB is missing or deeply discharged.
Threshold BB low is fixed by the Iota POR logic that assert a reset (nRESPWONZ to logic zero) when the UPR voltage goes below 2.1V. The system enters the NO SUPPLY state.
In the case of a present MB and some enabled main LDO this reset will also disable still active regulators.

5.2.3 MB deeply discharged & no BB

Same as above, when the MB discharge makes the UPR voltage going below 2.1V system passes from BACKUP state to NO SUPPLY state.

5.2.4 SWITCH ON

Switch on is possible only when a charged MB powers the system. Battery voltage values allowing switch on transition are above 3.2V(SWON_ENABLE input to the SM). There are four SWITCH ON events that allow the mobile to exit the OFF state and enter into ACTIVE state:

- Falling edge on the Iota PWRON pin
  PWRON pin is connected externally to the ON/OFF keypad button and internally pulled up to the VBAT voltage domain through a resistor whose value may vary between 300 KΩ and 500 KΩ. Hence as soon VBAT goes high PWRON pin follows VBAT and assuming its inactive logical level.
  Button push generates the falling edge on PWRON pin. This input is de-bounced for $1034*T_{32K}$ time interval. If PWRON pin level is still low after the de-bouncing period the VRPC SM starts the SWITCH ON sequence. Note that at this stage no interrupt request is generated toward the DBB.

- Falling edge on the Iota RPWRONZ pin.
  RPWRON pin has exactly the same characteristics than the PWRON pin.
  It is adopted to switch on the mobile through other events than a keypad ON/OFF This could be the case for an external accessory plug.

- Rising edge on ITWAKEUP pin
  This is the case of a wake-up event generated by the RTC (Real Time Clock) module of DBB. If a wake-up time has been programmed into the RTC registers this module asserts a switch on event at the specified time wakening-up the system. This can be the case of auto switch on application or alarm application.

- Voltage on CHG pin higher than the voltage on VBAT pin (charger insertion).
  This is the case of a charger insertion whose voltage is higher than the MB voltage allowing charging process.
  If the system is fitted with a flat MB plug of the charger will generate a switch on condition only when the MB, thanks to the precharge current, reaches the 3.2V threshold.

Once one of those condition has been accepted as valid the VRPC SM starts the SWITCH ON sequence disregarding any other valid SWITCH ON event. Check VRPC SM flow diagram in Iota specification [1].

Sequence consists in:

Iota:

- Enabling the main band gap
- Waiting for the Reference Band Gap to reach its nominal value (1.2 V)
- Checking for BG delivering the nominal reference.
- Checking for MB higher than 3.2V
- Enabling RDBB, RABB, RMEM
- Waiting for the LDO's to reach their nominal value.
- Enabling RIO
- Waiting for the LDO to reach its nominal value.
- Release ABB reset and setting the ON_nOFF signal to logic 1.

If one of the check included in the sequence fails the SM brings system back to OFF state.

Calypso:

- Waits default RF setup time(0 at reset).
- Set to logic one the RFEN pin
- Wait default VTCXO setup time (4096 at reset)
- Set to logic one the TCXOEN pin
- Wait SLICER setup time (4096 at reset)
- Enable SLICER module
- Wait 13MHz clock setup time (64 at reset)

- Release the FDP (Flash Deep Power) signal and chip internal reset.
- MCU receives 13 MHz clock after 3 T_{VTCXO} (VTCXO periods) and MCU activity starts after 20 $T_{VTCXO.}$

- Program starts:
  - SPI access to IOTA :
    - Configure Iota device
  - TSP accesses to RF part :
    - Enable Clara LDO's in fast mode
    - Configure Clara device
    - Configure TSPACT signal.
- Wait for a stable AFC output and nominal regulated output at CLARA LDO's. During this period system enter SW BIG SLEEP mode to avoid power consumption.
- Exit the BIG SLEEP mode.
- Program normal mode in CLARA bandgap.

System is now in ACTIVE state and able to perform GSM activity.

5.2.5 SLEEP OFF

Iota SLEEP mode has been conceived to support L1 Deep Sleep mode. Deep Sleep mode is a system low power consumption mode configured by L1 SW in which only a small part of the DBB modules keeps their activity on. Those modules are:

- RTC supplied on the VRRTC domain
- XO32K supplied on the VRRTC domain
- ULPD supplied on the VRDBB domain
- INTH[12] supplied on the VRDBB domain.

This mode allows reduction of power consumption during terminal idle mode, or PAGING, in which short periods of GSM activity are alternated with long idle periods.

Application SW puts the system in Deep Sleep once it has evaluated the length in terms of GSM frames in which the terminal is supposed to be inactive. This number of frames is stored in a so called GSM TIMER that starts to be decreased on a frame base once the system enter the Deep Sleep. GSM TIMER activity relies on the 32KHz clock.
There are several ways to exit the Deep Sleep mode:

- **Synchronous Wake-Up**

  The GSM TIMER reaches the zero value and wakes up DBB and ABB through an internal interrupt (DBB GSM TIMER IT) and the generation of an ITW AKEUP signal (ABB)

- **Asynchronous Wake-Up**

  DBB is wake-up from an asynchronous event before GSM TIMER interval has been elapsed. Those events generating an internal interrupt to DBB and an external ITWAKEUP signal may be (if non masked interrupts):

  - Keypad I/O transition — push keypad buttons.
  - RTC alarm — user pre-programmed alarm
  - UART — out-coming data.
  - EXT_FIQ — INT1 generation due to an EMERGENCY condition
  - EXT_IRQ — External accessory plug, Charger Plug, ON/OFF button push.

  SLEEP OFF transition to ACTIVE is generated either by an ITWAKEUP signal going from the DBB to the ABB or by one of the switch on conditions described for the SWITCH ON transition.
  This may lead to a double SLEEP OFF request arriving to the ABB.
  Let us assume that the system is in SLEEP state and that an external accessory is plugged. The edge on RPWRON pin is a valid condition to exit SLEEP mode hence Iota starts the SLEEP OFF sequence. This condition will also generate an INT2 to DBB signaling the detection of an edge on the pin.

[12] Interrupt Handler

If the EXT IRQ is enabled as source of wake-up events in the DBB the ABB will be requested to exit the SLEEP through an ITWAKEUP generation.
This new condition does not affect the already started SLEEP OFF sequence.
Once again all SLEEP OFF transition are considered valid only if MB voltage value is higher than 3.2V. In the case of a MB lower than 3.2V the system exit the SLEEP mode on a sleep off event but passes directly to BACKUP state.
Once a SLEEP OFF condition has been detected:

Iota:

- Enables the main band gap
- Waits for the BG to reach its nominal value (1.2 V)
- Checks for BG delivering the nominal reference.
- Checks for MB higher than 3.2V
- Enables RDBB, RABB, RMEM
- Waits for the LDO's reach their nominal value.
- Enables RIO
- Waits for the LDO to reach its nominal value.

If one of the check included in the sequence fails the SM brings system back to OFF state. Iota is then ready to support the system ACTIVE mode.

Calypso:

- Waits RF setup time(previously programmed in SETUP_RF_REG register).
- Set to logic one the RFEN pin
- Wait VTCXO setup time (previously programmed in SETUP_VCTXO_REG register)
- Set to logic one the TCXOEN pin
- Wait SLICER setup time (previously programmed in SETUP_SLICER_REG register)
- Enable SLICER module
- Wait 13MHz clock setup time (previously programmed in SETUP_CLOCK_13MHZ_REG register)
- Release the FDP (Flash Deep Power) signal and chip internal functional restart
- MCU receives 13 MHz clock after 3 T_{VTCXO} (VTCXO periods) and MCU activity starts after 20 $T_{VTCXO.}$
- Program starts:
    - SPI access to IOTA :
        - Restore Iota ACTIVMCLK
        - Restore AFC value
    - TSP accesses to RF part :
        - Enable Clara LDO's in fast mode
        - Restore TSPACT configuration.
- Wait for a stable AFC output and nominal regulated output at CLARA LDO's. During this period system enter SW BIG SLEEP mode to avoid power consumption.
- Exit the BIG SLEEP mode.
- Program normal mode in CLARA bandgap.
-

System is now ready to perform GSM activity.

Time diagram in next page summarizes system behavior exiting the SLEEP mode.

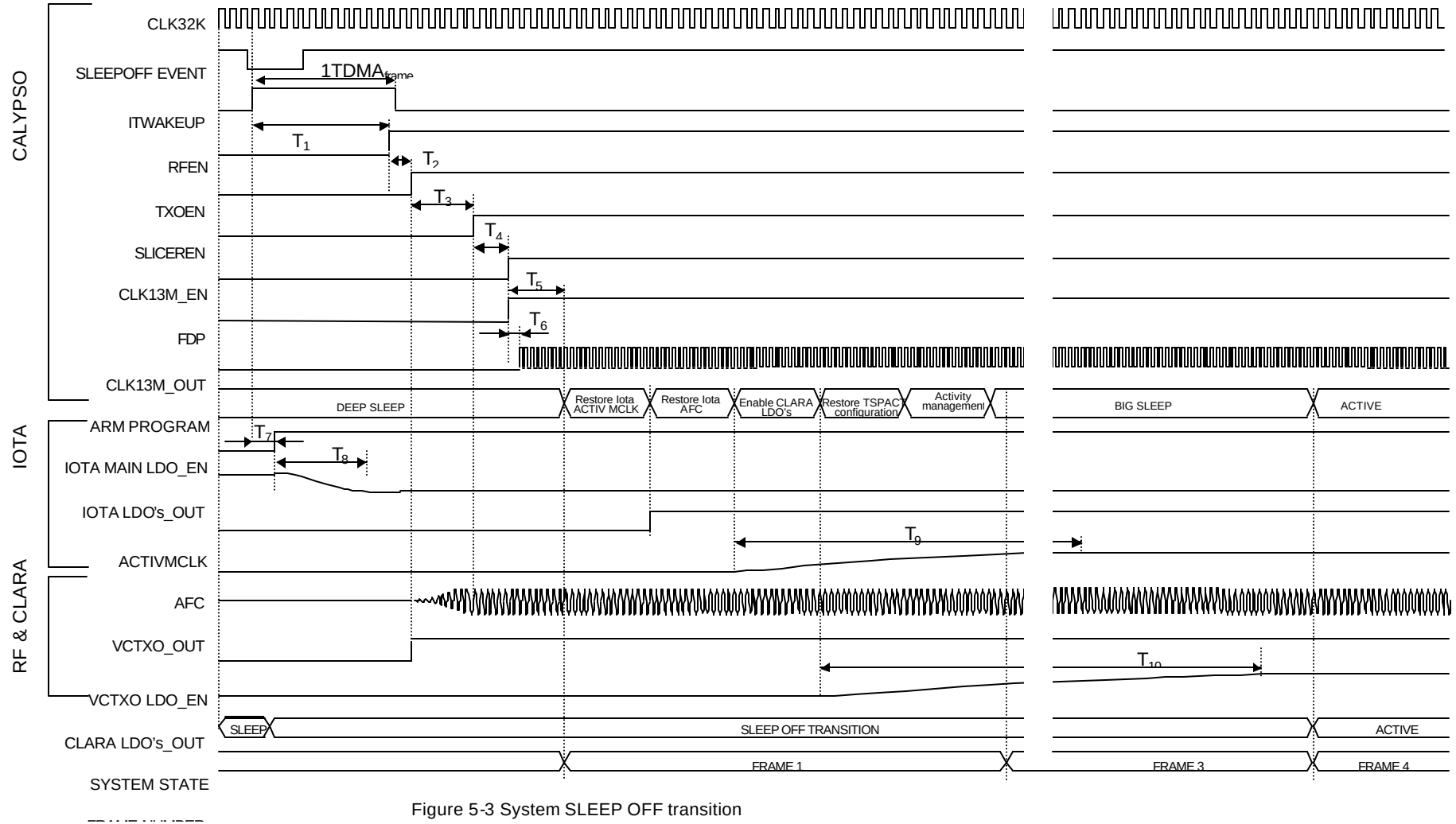


Figure 5-3 System SLEEP OFF transition

Table 5-1SLEEP OFF Timing descriptions

	Min	Typ	Max	Units	Description
T_1	1	1000	4096	T_{32k}	Setup RF time
T_2	1	31	4096	T_{32k}	Setup VCTXO time
T_3	1	490	4096	T_{32k}	Setup SLICER time
T_4	1	31	64	T_{32k}	Setup CLOCK_13 MHz time
T_5		20		T_{TCXO}	Time from FDP high to MCU code execution
T_6		3		T_{TCXO}	Time from FDP high to 13MHz available to MCU
T_7 T_8		2 151		T_{32k} T_{32k}	Time from ITWAKEUP detection and Iota LDO enable Iota main LDO turn on time from SLEEP mode
T_9	5 ms		15	ms	AFC setup time
T_{10}		10 [13]	55[14]	ms	CLARA LDO turn on time

The only timing constraint from system point of view is that T_8 Iota LDO's turn on time from SLEEP mode needs to be shorter than T_1+T_2. Is after that time interval, at VCTXO enable, that the system starts to sink more than the SLEEP current from Iota LDO's. Thus, at that time, they have to be already able to support ACTIVE mode current.

In current application the RFEN signal is not used. An external LDO enabled by the TXOEN signal provide power supply to the VCTXO

Application SW exiting the Deep Sleep (system SLEEP state) does not need to re-configure Clara device. The Clara serial port is supplied on a Iota sleep LDO (RIO) and register contents is maintained even in SLEEP mode.

[13] Typical value with speed-up enable
[14] Max value with speed-up disabled

5.3 SW driven transitions

SW driven transition includes SWITCH OFF and SLEEP ON transitions. Whether the first one has a HW origin, user decision to switch off the mobile through an ON/OFF button push, both transitions are initiated by a SW access to a Iota register. Before entering OFF or SLEEP state, application SW adequately configures the system then initiates the transition accessing to the ABB.

5.3.1 SWITCH OFF

This transition is initiated by a specific user action consisting in ON/OFF button push. This action generates a falling edge on the Iota PWRON pin. Signal on pin PWRON is de-bounced for TBD T_{32K} time interval (HW de-bouncing). If the PWRON pin level is still low after de-bouncing period Iota asserts an INT2 request to Calypso. Start of the SWITCH OFF sequence is under application SW control. Behavior may vary depending on application. A common mode of managing this input is the following:

- DBB receives the INT2 request from ABB
- DBB acknowledges the request reading ABB IT_STS_REG receiving back the information that INT source is an event on the ON/OFF pin.
- DBB starts polling the state of PWRON pin in VRPC_STS register, ONREFLT bit, to check whether the switch off condition is still valid (SW de-bouncing).
- Once passed the valid switch off time length (2-3 sec) DBB start system configuration to enter OFF mode and waits for the rising edge of PWRON pin polling its state.
- At rising edge[15] Calypso executes last system configurations and sends to Iota the DEV OFF command writing into VRPC_DEV register.

System configuration to enter OFF mode consists in:

- Halt application activity.
- Disable Clara LDO's and any other possible current sinking device controlled through TSPACT interface.
- Disable al Iota modules programming TOGBR1 and TOGBR2 registers.
- Select through the VRPCMSK register LDO's that have to stay in SLEEP mode. even during system OFF state[16] (depends on backup scheme adopted)
- Start the ACTIVE to OFF transition programming the bit DEVOFF in Iota VRPCDEV register.

At this stage the Iota VRPC SM takes HW control of the SWITCH OFF transition executing the following sequence:

- Wait 5 T_{32K} periods.
- Force the ON_nOFF signal to logic 0
- Forcing the internal ABB reset to logic 0
- Disable LDO's using the MSKOFF content

[15] Wait for rising edge of PWRON pin is necessary to avoid the presence of a new switch on condition in the case the ON/OFF pin stay pushed for a long time.

[16] Programming a 0 (default value) in the MSKOFF[4:0] register will select the associated LDO to be disabled during OFF mode. Programming a 1 the associated LDO will be still enabled but in a low consumption mode.

When the ON_nOFF signal goes to low state Calypso asserts the internal functional reset (DSP & MCU) and the external reset nRESET_OUT, split power part is isolated. The system is in OFF mode.

5.3.2 SLEEP ON

This transition is initiated on application SW decision. While in paging mode the mobile alternates shorts periods of GSM activities with relatively long (up to around 2 seconds in DRX9) period of inactivity that correspond to system SLEEP state.
Valid conditions to enter into SLEEP mode are evaluated by the activity management part of the application SW in terms of number of frames in which no system activity is required.
If number of inactivity frames is greater than given threshold[17] SW initiates system configuration to enter in Deep Sleep (SLEEP) mode.

System configuration consists in:

- De-mask all wake up sources (Keypad, external interrupts, GSM timer interrupt, RTC alarm).
- Program the GSM TIMER with the number of SLEEP frames and all the setup times for RF, VCTXO, SLICER and CLK13.
- Disable all Iota modules (TOGBR1 and TOGBR2 registers) AFC block is treated separately.
- Configure Clara Bandgap to speed-up mode and disable Clara LDO's.
- Configure the TSP parallel interface in order to have low logical value on the TSPACT signal going to RF.
- Select the delay SLPDLY between the MCU access that states SLEEP mode and the instant at which Iota LDO's will switch to SLEEP mode (VRPCCFG register in Iota).
- Configure Iota test mode to access directly the AFC_OUT register and force an AFC value of zero.
- Start the ACTIVE to SLEEP transition programming the bit DEVSLP in Iota VRPCDEV register.
- Set Iota ACTIVMCLK to zero indicating that the 13MHz clock will be no longer available to Iota.
- Halt Calypso peripheral modules.
- Program Big Sleep and Deep Sleep bits in Calypso CNTL_ARM_CLK register.

At this stage

Calypso :

ULPD switches on the 32 KHz clock to maintain the GSM time then it cuts in this order :

- The 13 MHz clock
- The SLICER
- The VCTXO and the external RF device (RFEN to logic 0).

Until a wake up event occurs ULPD state machines keeps this state.

Iota:

VRPC SM :

- Waits for the DLYSLP timer to be elapsed [SLPDLY(4..0)*16+12]*TCk32K

[17] The threshold value depends on the network-imposed conditions and on the number of frames required to enter and exit the SLEEP state. A good optimization of number of frames needed for transitions will make the SLEEP threshold lower, enhancing the standby consumption of the mobile.

- Disables LDO's using the MSKSLP configuration mask register[18]
- Switches to local Band Gap.

System is in SLEEP mode.

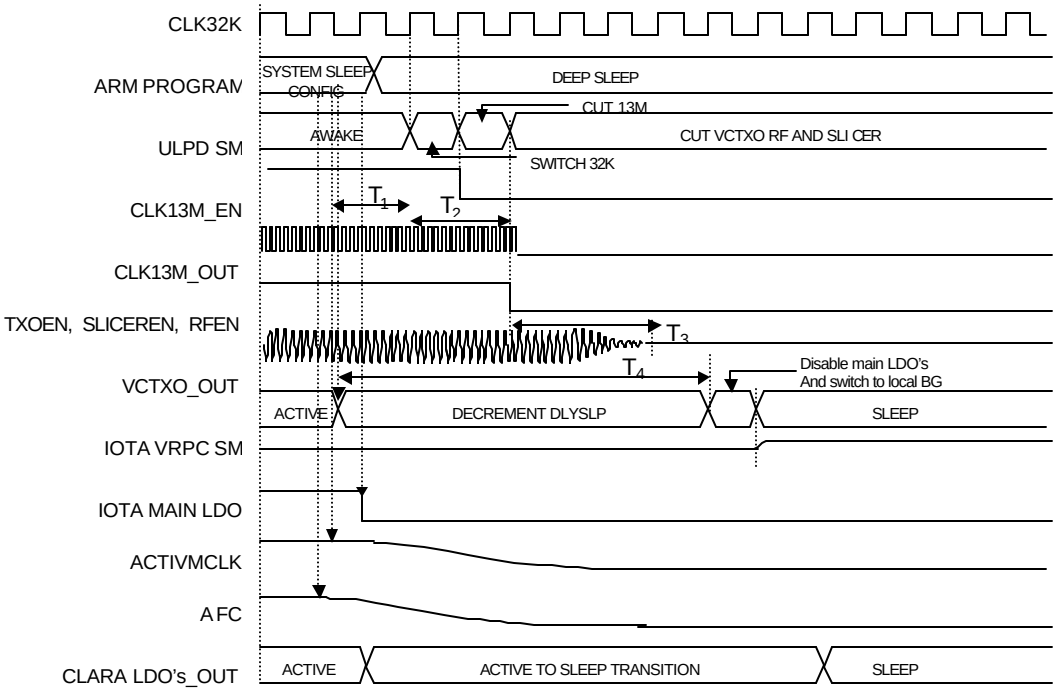


Figure 5-4 SLEEP ON transition

Table 5-2 SLEEP ON timing description

	Min	Typ	Max	Units	Description
T_1		SW +1		T_{32k}	Time from AFC disable to ULPD switch on 32KHz (1)
T_2		3		T_{32k}	ULPD SM execution time (switch32k,cut 13M, cut RF..)
T_3		TBD		T_{32k}	VCTXO disable time (2)
T_4	12		508	T_{32k}	DLYSLP counter delay (3)

(1) This time interval is SW dependent. Application SW must take care of shortening as much as possible this timing in order to minimize GSM time synchronization error. AFC control of 13MHz is no longer present but the 13 MHz clock is still used as reference for the GSM time.
(2) This time interval depends on VCTXO type.
(3) This delay must be greater than the sum $T_1+T_2+T_3$. This to ensure proper power supply during transition phase. Iota LDO's switch to SLEEP mode has to be executed only when

[18] Programming a 1 in the MSKSLP[4:0] register will select the associated LDO to be disabled during SLEEP mode. Programming a 0 (default value) the associated LDO will be still enabled but in a low consumption mode.

the whole system is in a low current consumption state. This delay is variable, given by the formula [SLPDLY(4..0)*16+12]*TCk32K.

6 Current consumption in BACKUP, OFF and SLEEP modes

Current consumption in low power modes has two main contributors: modules that are supposed to keep their activity even during those modes and leakage current of all that modules that whether in idle mode absorb some IDDQ current. Iota/Calypso/Clara system architecture has been conceived to optimize current consumption due to active modules and to reduce the part due to leakage IDDQ current.

6.1 BACKUP mode

This mode allows the lowest system current consumption. Value of this current mainly depends on the presence of the MB and on the previous programmation on LDO's enable.

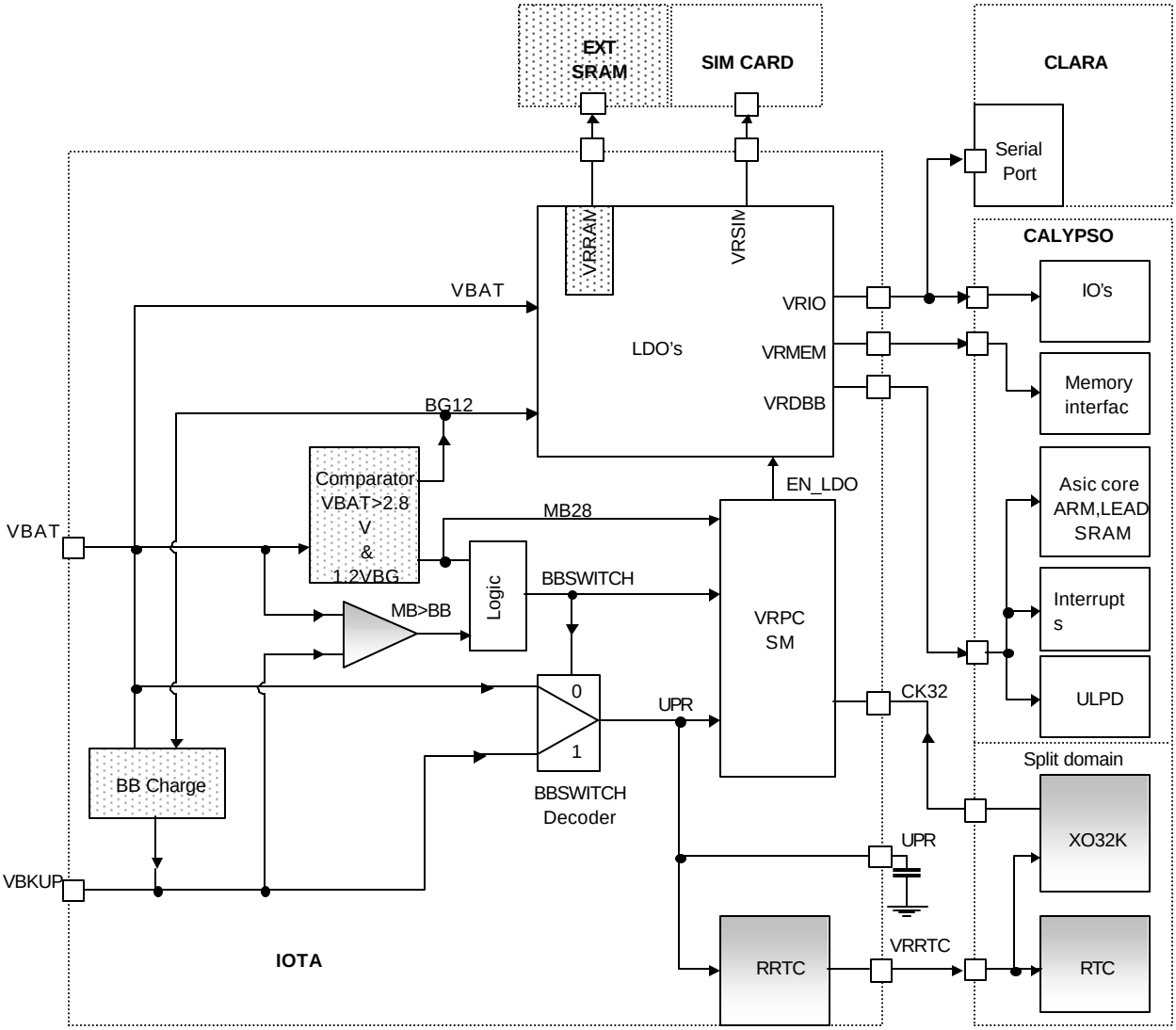


Figure 6-1 Active blocks in backup mode

Grey shaded blocks in Figure 6-1 Active blocks in backup mode correspond to active bloks during BACKUP either supplied by MB or BB.
Grey dotted blocks, with the exclusion of the band gap one that is always active as a MB is present, correspond to block that could be programmed to stay active during BACKUP state. Hence with MB fitted, current consumption computation may vary depending on system configuration.

6.1.1 System without MB

Active blocks in this configuration are included in the following table:

Table 6-1 Estimated System BACKUP current consumption on BB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6[19]
Clara	
None	-
Total	**8.6**

The indicated values have to be considered as typical ones, calculated at room temperature.

6.1.2 System with MB

This computation is done assuming that none of the LDO's has been left in sleep mode before entering the OFF state. Analysis of system current consumption with so-called back-up capability will be discussed in the next chapter. Scope of this calculation is to give a system current consumption floor reference. Active blocks in this configuration are included in the following table:

Table 6-2 Estimated System BACKUP current consumption on MB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
BB charge (if enabled)	10
Band Gap	5
Calypso	
RTC & Power Split Logic	1

[19] The CLK32K I/O current consumption has been evaluated applying the following formula: I_{avg} = V x f x C assuming V= 1.8V, C = 10pF, f = 32K.

XO32K	3.5
XO32K IO	0.6
Clara	
None	-
Total	**23.6**

The indicated values have to be considered typical value calculated at room temperature. In this mode all main regulator are disabled preventing any possible current leak.

6.2 OFF mode

This is the more common system mode after user switch off command. Charged MB is still fitted and provides supply to active modules.
Current computation in this mode will be done considering the need of data backup.
The proposed solution to achieve data backup during OFF and BACKUP modes adopts an external SRAM supplied by the Iota dedicated regulator RRAM.
Back-up data will be lost at MB removal as RRAM LDO is powered on MB

Table 6-3 Estimated System OFF current consumption on MB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic MB vs BB comparator	2.5 1
BB charge (if enabled)	10
Band Gap	5
RMEM LDO in sleep mode	13
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6
Clara	
None	-
External SRAM [6]	
SRAM Vcc Standby Current	1
Total	**37.6**

The indicated values have to be considered typical value calculated at room temperature.

6.3 SLEEP mode

Current consumption in this mode has a high impact on the standby time of the mobile.
Computation in this case will be done considering that all LDO's that could be programmed to stay in SLEEP mode will be in this state. This to evaluate the system maximal consumption in this mode.
For what concern Iota LDO's maximum current consumption is 20 uA in SLEEP mode. In this state maximum regulator drive current is 1mA

Note also that once the Calypso core is supplied (RDBB in SLEEP mode) to support DEEP SLEEP mode, all other Calypso supplies (RMEM and RIO) must be powered as well. This to avoid current leakage from the DBB core through I/O's and memory interface.

Table 6-4 Estimated System SLEEP current consumption on MB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
BB charge (if enabled)	10
Band Gap	5
RMEM LDO in sleep mode	13
RDBB LDO in sleep mode RRAM LDO in sleep mode	13 13
RIO LDO in sleep mode	13
RSIM LDO in sleep mode	13
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6
ASIC Core	100
Memory Interface	TBD
I/O's	TBD
Clara	
Serial Port	1
External SRAM [6]	
SRAM Vcc Stand-by Current	1
SIM Card	
SIM Vcc Stand-by Current (*) **Total**	TBD **190.6+TBD's**

(*) Depends on the adopted SIM card.

7 Applications

7.1 Analog

7.1.1 Sim interface

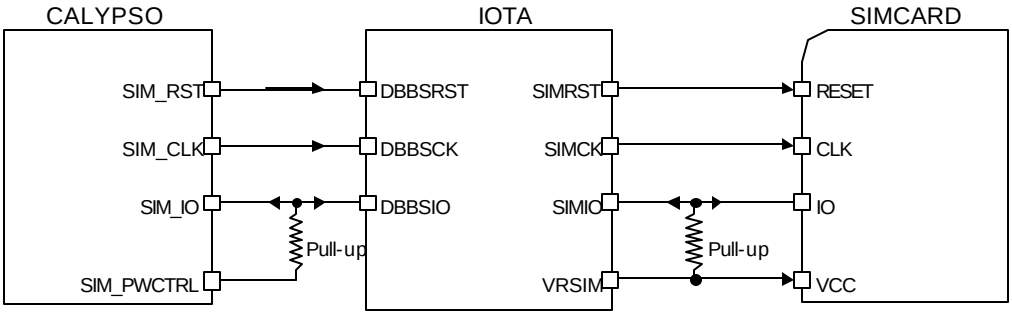


Figure 7-1 Sim Card connection schematic

The system is able to accept 3V and 1.8V SIM card following tables summarize required Iota SIM interface pin characteristics at 1.8V and 3V.

7.1.1.1 1.8V SIM interface

IO - electrical specifications

SIMLEN = 1, RIO and RSIM are enabled

Table 7-1 Electrical characteristics under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH} (note 1)	I_{OHmax} = + 20 µA	0,7 x Vcc	Vcc (note 3)	V
V_{OL}	I_{OLmax} = - 1mA	0 (note 3)	0,3	V
t_{RtF}	C_{in} = C_{out} = 30 pF		1	µs

NOTE1: It is assumed that a pull-up resistor is used on the interface device.
NOTE 2: During static conditions (idle state) only the positive value can apply. Under Dynamic operating conditions (transmissions) short term voltage spikes on the I/O line may cause a current reversal.
NOTE 3: To allow for overshoot the voltage on I/O shall remain between -0,3V and Vcc+0,3V during dynamic operation.

CLK – electrical specifications

Table 7-2 Electrical characteristics under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH}	SIMLEN = 1, VRIO and VRSIM set, I_{Ohmax} = + 20 µA	0,7 x Vcc	Vcc (note)	V
V_{OL}	SIMLEN = 1, VRIO and VRSIM set, I_{OLmax} = - 20 µA	0 (note)	0,2*VCC	V
V_{OL}	SIMLEN = 0, VRIO and VRSIM not set, I_{OLmax} = -1mA	0 (note)	0,2*VCC	V
t_{RtF}	C_{in} = C_{out} = 30 pF		50	Ns

NOTE : To allow for overshoot the voltage on CLK should remain between -0,3V and Vcc +0,3V during dynamic operations.

RESET – electrical specifications

Table 7-3 Electrical characteristics under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH}	SIMLEN = 1, VRIO and VRSIM set, I_{Ohmax} = +200 µA	0,8 x Vcc	Vcc (note)	V
V_{OL}	SIMLEN = 1, VRIO and VRSIM set, I_{OLmax} = -200 µA	0 (note)	0,2*VCC	V
V_{OL}	SIMLEN = 0, VRIO and VRSIM not set, I_{OLmax} = -1mA	0 (note)	0,2*VCC	V
t_{RtF}	C_{in} = C_{out} = 30 pF		400	µs

NOTE : To allow for overshoot the voltage on RST should remain between -0,3V and Vcc +0,3V during dynamic operations. For the VOH condition, the SIM shall not draw more than 20 µA from the RESET (RST) contact.

VCC – electrical specifications

Table 7-4 Electrical characteristics under normal operating conditions

Symbol	Minimum	Maximum	Unit
Vcc	1.62	1.98	V
Icc		4 (note)	mA

NOTE: The supply current at 1.8V refers to a clock frequency of 4 MHz.

7.1.1.2 SIM card 3V specification

IO - electrical specifications

(SIMLEN = 1, VRIO and VRSIM are set)

Table 7-5 Electrical characteristics under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH} (note 1)	I_{OHmax} = + 20 µA	0,7 x Vcc	Vcc (note 3)	V
V_{OL}	I_{OLmax} = - 1mA	0 (note 3)	0,4	V
t_{RtF}	$C_{in} = C_{out}$ = 30 pF		1	µs

NOTE 1: It is assumed that a pull-up resistor is used on the interface device.
NOTE 2: During static conditions (idle state) only the positive value can apply. Under Dynamic operating conditions (transmissions) short term voltage spikes on the I/O line may cause a current reversal.
NOTE 3: To allow for overshoot the voltage on I/O shall remain between -0,3V and Vcc+0,3V during dynamic operation.

CLK – electrical specifications

Table 7-6 Electrical characteristics under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH}	SIMLEN = 1, VRIO and VRSIM set, I_{Ohmax} = + 20 µA	0,7 x Vcc	Vcc (note)	V
V_{OL}	SIMLEN = 1, VRIO and VRSIM set, I_{OLmax} = - 20 µA	0 (note)	0,2*VCC	V
V_{OL}	SIMLEN = 0, VRIO and VRSIM not set, I_{OLmax} = -1mA	0 (note)	0,2*VCC	V
t_{RtF}	$C_{in} = C_{out}$ = 30 pF		50	ns

NOTE : To allow for overshoot the voltage on CLK should remain between -0,3V and Vcc +0,3V during dynamic operations.

RESET – electrical specifications

Table 7-7 Electrical characteristics under normal operating conditions

Symbol	Conditions	Minimum	Maximum	Unit
V_{OH}	SIMLEN = 1, VRIO and VRSIM set, I_{Ohmax} = +200 µA	0,8 x Vcc	Vcc (note)	V
V_{OL}	SIMLEN = 1, VRIO and VRSIM set, I_{OLmax} = -200 µA	0 (note)	0,2*VCC	V
V_{OL}	SIMLEN = 0, VRIO and VRSIM not set, I_{OLmax} = -1mA	0 (note)	0,2*VCC	V
t_{RtF}	$C_{in} = C_{out}$ = 30 pF		400	µs

NOTE : To allow for overshoot the voltage on RST should remain between -0,3V and Vcc +0,3V during dynamic operations. For the VOH condition, the SIM shall not draw more than 20 µA from the RESET (RST) contact.

VCC – electrical specifications

Table 7-8 Electrical characteristics under normal operating conditions

Symbol	Minimum	Maximum	Unit
Vcc	2.7	3.3	V
Icc		6 (note)	mA

NOTE: The supply current at 3,3V refers to a clock frequency of 4 MHz.

7.1.2 Optimized Backup scheme

Goal of this optimized back up scheme is to reduce mobile power consumption down to the floor backup consumption. In this configuration the external SRAM is still able to keep valid backed up data.

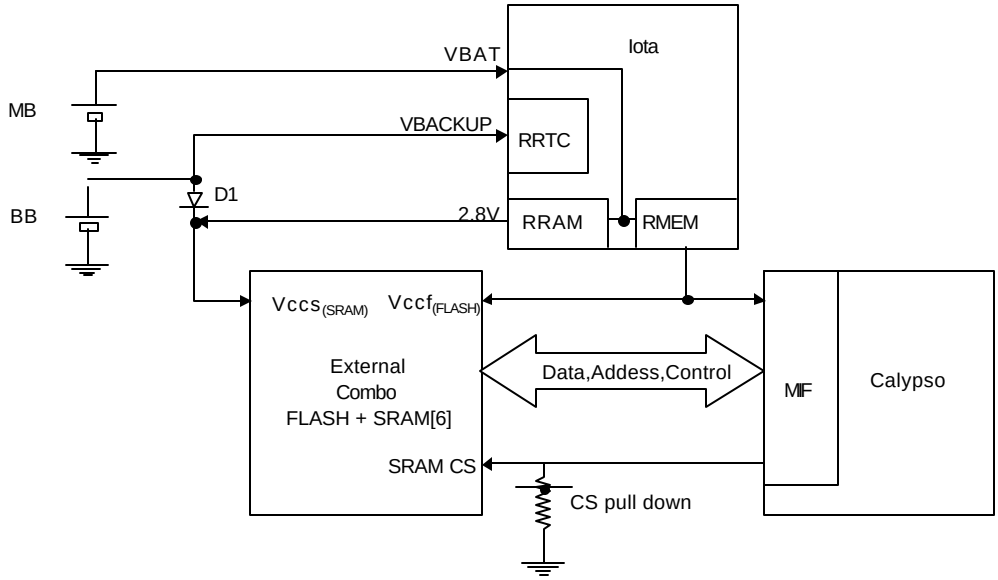


Figure 7-2 Optimized Back-Up scheme connections

The backup feature relies on a diode connection between the BB and SRAM supply line Vccs. This connection allows SRAM supply through the BB when the VRRAM regulator is off.
The pull down on SRAM CS pin (active high) grants HiZ state on Data, Address, Control bus when the MIF part of Calypso device is not supplied. This to avoid current leakage through this bus.
Choices of external diode and of the maximum value of the BB have to be done considering that:

- The adopted SRAM allow data retention down to a minimum of 1.5V for Vccs (SRAM supply line).
- System is halted as soon as UPR voltage goes below 2.1V.
- RRAM regulator reverse current protection is implemented as depicted in the schematic below, forcing at UPR voltage values the indicated terminals of the LDO pass transistor when the LDO is off.

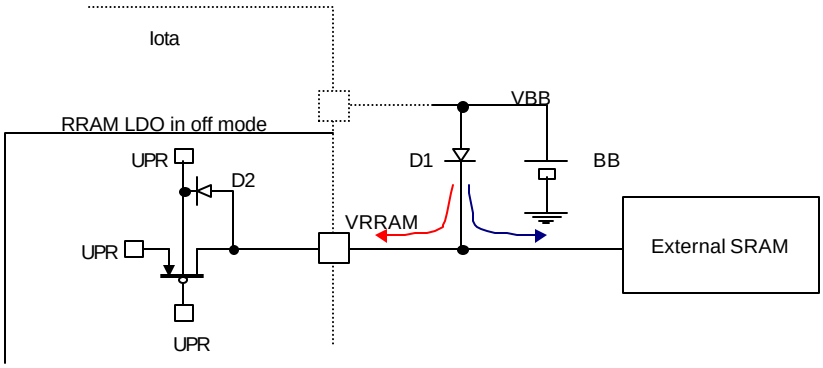


Figure 7-3 RRAM inverse current protection in OFF mode

Maximum voltage value of the BB and D1 diode drop voltage must suit the following relation in order to to avoid current leakage from the BB into the VRRAM pin when the regulator is in off

$$V_{BB\max} - V_{dropD1} \leq V_{UPR}$$

mode.

Possible values of UPR voltage depending on the MB and BB voltage values are illustrated in the diagram below.

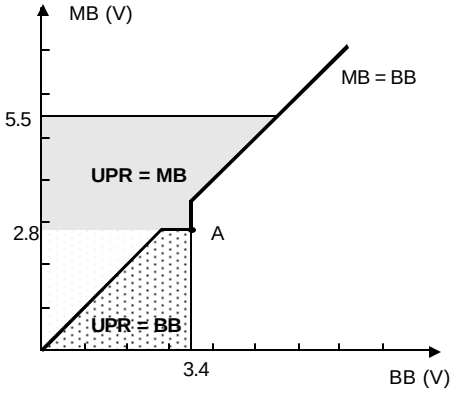


Figure 7-4 UPR supply dependency on MB and BB

Critical point for this application schematic is indicated with A in Figure 7-4. In this case the MB supplies UPR at 2.8V while BB could be fully charged.
Assuming that the maximum voltage value of the BB battery is 3.2V the diode D1 has to provide a voltage drop at least of 0.4V. In this case the parasitic diode D2 of the LDO pass transistor will not be forward biased hence no current will flow into VRRAM pin.
Choice of D1 diode voltage drop will impact also application schematic behavior during active mode of RRAM LDO. This regulator impose at VRRAM pin a regulated voltage that may vary from a minimum of 2.7V to a maximum of 2.9V. To avoid that during active mode a fully charged BB could supply the SRAM the diode voltage drop has also to satisfy the following condition:

$$V_{BB\max} - V_{dropD1} \leq V_{RRAM\ \min}$$

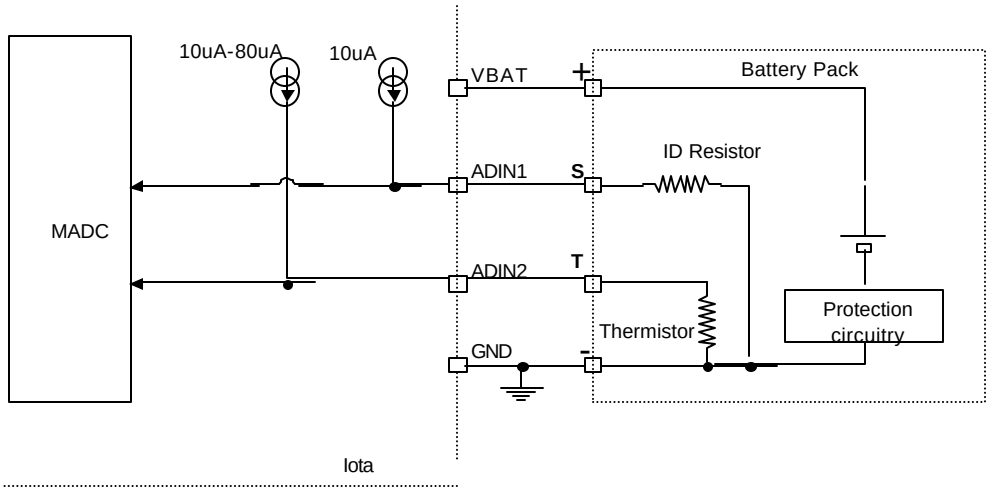
This relation imposes a minimum diode voltage drop of 0.5V.
Thus having a voltage drop of 0.5V and a SRAM minimum voltage for data retention equal to 1.5V this application schematic can exploit BB battery down to 2V.
This limit agrees with the system shut down limit fixed by Iota device to BB value of 2.1V.
System power consumption adopting this application schematic is the following:

Table 7-9 System BACKUP current consumption on BB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6
Clara	
None	-
External SRAM[6]	
SRAM Vcc Stand-by Current	1
Total	**9.6**

7.1.3 Madc

Following application schematic will illustrate type and temperature measurements for battery packs through the MADC interface.



SW set up for a temperature measurement:

- Enable the MADC module writing to logic 1 the MADCS bit in TOGBR1 register.
- Configure the ADIN2 source current to deliver the appropriate current value programming the THSENS[2..0] bits in the BCICTL1 register.
- Configure the MADC to convert the ADIN2input.
- Enable the ADIN2 bias current writing a logic 1 into THEN bit BCICTL1 register
- Start the MADC conversion executing a dummy write in one of the result registers (VBATREG as example).
- Wait for the end of conversion polling the ADCBUSY flag in ADC_STATUS register.
- Read conversion result in ADIN2 register.

7.1.4 Bci

Block diagram below illustrate the Iota BCI with its external components.

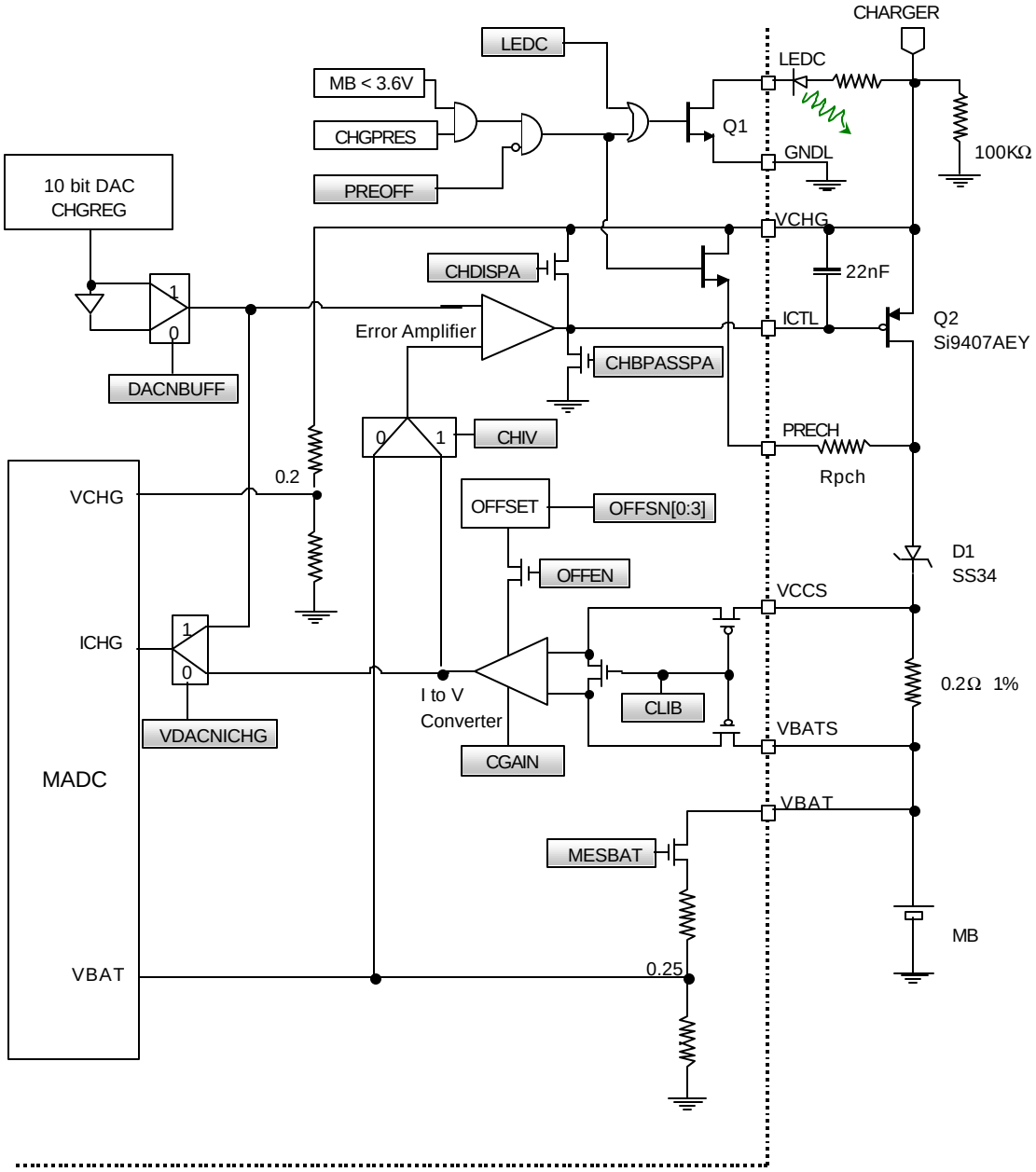


Figure 7-5 BCI block schematic and external component.

Shaded blocks in the picture represents physical register bit locations included in the three register controlling the BCI activity:

Name : BCICTL1					Description :					Address : 28 Page : 0					R/W
-	VDAC NICHG	TYPEN	THEN	THSENS2	THSENS1	THSENS0	MESBB	DACNBUF	MESBAT	1	1	1	0	0	1/0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

MESBAT — Connects resistive divider to Main battery, it also enable the voltage loop-back in the constant voltage charging mode. This bit has to be set to logic 1 in order to impose constant voltage on the battery.

DACNBUF — Bypass DAC buffer. Buffered output of the DAC is adopted for high constant current charges. Non buffered DAC ouput is more indicated for low constant current charges as it shows better linearity for low DAC code values.

MESBB — Connects resistive divider to Back-up Battery

THSENS [2..0] — Set eight possible values for thermal sensor bias current

THEN — Enables bias current for main battery temperature sensing

TYPEN — Enables bias current for main battery type reading

VDACNICHG — Allows selection of the MADC ICHG input:
0: ICHG input is connected with the ouptut of the I to V converter
1: ICHG input is connected with the output of the 10 bit DAC controlling the charge.
In this second configuration the output of the DAC could be measured only if the charge process is enabled.
To avoid uncontrolled current flow through the external pass transistor while executing this measurement ICTL output must be tight to VCHG level through CHGDISPA bit programmation to logic 1.

Name BCICTL2					Description :					Address : 29 Page : 0					R/W
RSV	RSV	PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHPASSPA	CHIV	CHEN	1	1	1	0	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET (CHG PRESENT)					
1	1	1	1	1	1	1	1	1	1	<--- VALUE AT RESET (CHG NOT PRESENT)					

CHEN — Enables the charger

CHIV — Selects constant current or constant voltage charging
0: Constant Voltage
1: Constant current

CHPASSPA — Controls fully charge of Main Battery
0: No effect
1: ICTL output pin is tight to GND forcing in active state the external pass transistor

CLIB — Enable the calibration routine of the I to V converter.
Calibration routine could be executed only is the charge is enabled. Thus to avoid uncontrolled current flow through the external pass transistor while executing this measurement ICTL output must be tight to VCHG level through CHGDISPA bit programmation to logic 1.

CHDISPA — Disable the charge pass transistor
0: No effect
1: ICTL output pin is tight to VCHG thus disabling the chare pass transistor

LEDC	SW control for LEDC. This LED indicates the presence of the precharge current flowing into the main battery. If the precharge is active (Vbat < 3.6V and PRECHOFF bit to logic0) programming logic 0 into this bit has no effect.
CGAIN4	Allow selection of current to voltage convertergain 0: I to V gain is 10 1: I to V gain is 4
PREOFF	Allow precharge disable: 0: Precharge is enabled 1: Precharge is disabled
RSV	: reserved bit (write only '0')
RSV	: reserved bit (write only '0')

This register is supplied by VCHG.
When charger is not present register content is read back as 0X3FF. This does not represent the real register content value. Each time the charger is inserted this register is reset to its initial state.

Name : BCICONF				Description :						Address : 13 Page : 1					R/W
-	-	BBSEL1	BBSEL0	BBCHGEN	OFFEN	OFFSN3	OFFSN2	OFFSN1	OFFSN0	1	1	1	0	0	1/0
R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	KEEP VALUE	<--- VALUE AT RESET (AFTER EACH SWITCH ON)					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET (AFTER FIRST RESET)					

OFFSN [3..0]	Allow the selection of 16 possible values for current to voltage conversion offset. 0: +0mv N: +N*12.5mV 15 : +187.5 mV (typical values). This features allows together with the I to V calibration routine to have a minimum impact of the I to V offset in current measurements, making possible small current acquisitions. It may happen that result of a calibration routine is zero. This means that the I to V offset is negative
OFFEN	: Enable offset settings for current to voltage conversion.
BBCHGEN	: Enable Back Up Battery Charger
BBSEL[1:0]	: This Iota feature allows the selection of Back up battery end of charge voltage through the BBSEL bits programmation. From characterization results end of charge values for the BB are:

Code	Min	Max
00	3.04	3.22V
01	3.14	3.34V
10	3.22	3.44V
11	3.22	3.44V

Name : CHGREG					Description :					Address : 25 Page : 0					R/W
CHG9	CHG8	CHG7	CHG6	CHG5	CHG4	CHG3	CHG2	CHG1	CHG0	1	1	0	0	1	1/0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

CHG [9..0] : 10 Bit DAC register for setting a voltage or a current for Main Battery charging.

This 10 bit DAC adopts the same reference voltage of the monitoring ADC. This feature allows an easier calculation of the value to be programmed in this register during a charging process.

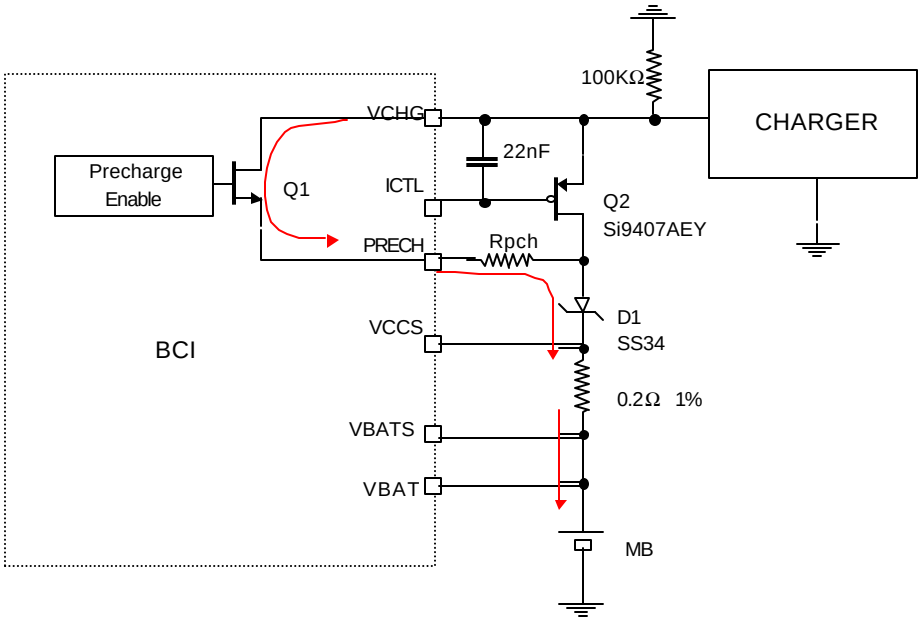


Figure 7-6 BCI connections schematic and precharge current path

7.1.4.1 Precharge

The precharge current is used to bring the MB to the minimum charged status allowing a safe system start. The fixed limit by the Iota VRPC is 3.2V. This means that for MB voltage values below this threshold the system is unable to accept any start condition. Nevertheless the BCI precharge part is active and providing precharge current to the MB to rise up its voltage.
Value of the precharge current can be selectable up to a maximum of 100 mV through the external resistor connected at the Iota PREC pin. This limit is imposed maximum current that can be flow through the Iota internal transistor (transistor Q1 in Figure 7-6) .
External resistor value must be evaluated calculating the precharge branch electrical equilibrium in the worst conditions:

- Vbat = 0V
- Q Rdson = min
- Vchg = max
- Vdrop diode = min.

Assuming Vchg max = 7V , Vdrop diode min = 0.5V and Rdson min =2Ω, from the electrical equilibrium of the precharge branch we have:

$$Vchg = Rdson * Ipchg + Rpch_{\min} * Ipchg + Vdrop_{D1} + 0.2 * Ipchg$$

And

$$Rpchg_{\min} = \frac{Vchg - Vdrop_{D1}}{Ipchg} - Rdson - 0.2\Omega = 62.8\Omega$$

Adopting such value for the external resistor we can extrapolate the precharge current value for different Vbat voltages:

$$Ipchg = \frac{Vchg - Vdrop_{D1} - Vbat}{Rpchg_{\min} + Rdson + 0.2\Omega}$$

Table 7-10 Precharge current vs VBAT

Vbat (Volts)	Ipchg (mA)
2.7	58.4
3.2	50.7
3.6	44.6

7.1.4.2 Algorithm basis for Li-Ion battery charging.

Following part describes Iota BCI registers configuration and algorithm basis for Li-Ion battery charging.

a) Calibration of the charging current I/V converter.

The sequence described below is the recommended one to calibrate the current I/V converter offset of the current controlled loop.

It is assumed that the Iota device is in switch-on condition and that the MADC module is already initialized and ready to monitor ICHG input.

Calibration sequence:

Plug in the charging device

Set the CHDISPA bit to logic 1 in BCICTL2 register. This setting is necessary to avoid strong current flow in the power transistor at the enable of the calibration. This must be done in the register access preceding the register access that enables the calibration.

Set the CLIB bit to logic 1 in order to enable I/V converter calibration.
This programmation configures the calibration switches connecting together the inputs of the current to voltage converter. Set the CHEN bit

Measure through the MADC the ICHARGER value.

Result of measurement could be zero, the current to voltage converter amplifier could have a negative input offset. This offset could be made positive and minimized programming the OFFEN and OFFSN[3..0] in the BCICONF register. Than a new measurement of the ICHARGER value is required to evaluate the effects on the offset of the above programmation.

Disable calibration writing logic 0 into CLIB and CHEN bit.

Result of this measure is the current to voltage converter offset, and it must be kept in account by the charging control algorithm to fix correctly the value of the charging current and to detect the end of charge condition.

In the first case, correct value of charging current is obtained adding the calculated offset value to the theoretical DAC value.

The calibration process is mandatory to achieve the necessary precision in the detection of the end of charge condition.
Current values to be measured in this case are of the same magnitude order than the I/V converter offset.

b) Battery charge control

The charging process is under control of the MCU; register accesses to Iota are done through the usp port.
It is assumed in the following sequence that a charger has been plugged, that the CHGREG value corresponding to 4.2V is already known and that Iota is in switch on condition (precharge phase already passed). In that case the application SW has to execute the following actions:

Enable the MADC module writing a logic one to MADCS bit into TOGBR1 register(Address 4 Page 0)

Perform the calibration routine described above and memorize the current to voltage offset value.

Connect the resistive divider to Main battery programming MESBAT bit to logic 1 into BCICTL1 register (Address 28 Page 0).

b1) Constant Current charging phase:

Set the constant charging current value in CHGREG register keeping in account the previously calculated offset value.(Address 25 Page 0).

Configure the Monitoring ADC to monitor the VBAT voltage. Select the conversion of the battery voltage writing a logic one to the VBATCV bit in ADCCTRL(Address 13 Page 0)

Disable the charger and select the constant current charge mode programming the CHEN bit to logic 0 and the CHIV bit to logic 1 in BCICTL2 register (Address 29 Page 0).

Enable the constant current charge programming the CHEN bit to logic one, keep CHIV bit at logic 1.
Start MADC conversion of the VBAT value to monitor battery voltage value.

Keep on monitoring the battery voltage.

NOTE:
The register CHGREG contains charging current value when BCI is in constant current mode and charging voltage value when BCI is in constant voltage mode.

b2) Constant Voltage charging phase.

At Peak voltage detection (normally 4.2 V for Li-ion battery type) the charging control algorithm:

Disables the charger. This is done programming the CHEN bit to logic 0 in BCICTL2 register (Address 29 Page 1).
Selects the constant voltage charge mode. This is done programming the CHIV bit to logic 0 in BCICTL2 register (Address 29 Page 1).

Sets the constant charging voltage value in CHGREG register.

Configures the Monitoring ADC to monitor the ICHG current writing a logic one to the IBATCV bit in ADCCTRL(Address 13 Page 0).

Enables the constant voltage charge programming the CHEN bit to logic one, keep CHIV to logic 0.

Monitors the battery current reading the ICHGREG register (Address 17 Page 0).
In current value calculation must be taken in account the I/V converter offset value.
Effective ICHG value is ICHGREG value minus I/V offset.

Stops the charging process at the detection of the minimum charging current (typ C/20 for Li-ion battery type) .

Reset all registers.

7.1.5 Led drivers

The diagram below illustrates the application schematic for led driver inputs LEDA, LEDB, LEDC. Schematic is the same for all LEDx input. In each case the current limiter resistor R has to be selected in order to be compliant with maximum current drive capability of each input. The input LEDC has to be pulled up to VCHG.
The table below summarizes LEDx inputs charcteristics:

Table 7-11 LEDx Input characteristics

Pin name	Max Driven current	High level V	Low level V	Supply	Led function
LED A	10 mA	VBAT	0.4V	VBAT	Paging led
LED B	150 mA	VBAT	0.7V	VBAT	Back-light leds
LED C	10 mA	VCHG	0.4V	VCHG	Precharge indicator led

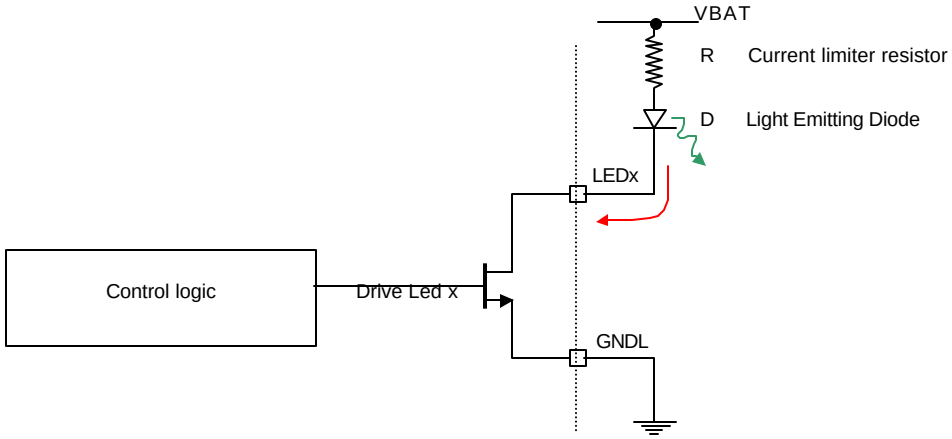


Figure 7-7 Led drivers application schematic

LEDA, LEDB are controlled through SW programmation of dedicated bit locations in ACDLED register.
LEDC control logic is different from the two above. The driver enable signal Drive Led C is generated as logic OR of two conditions: the presence of the precharge current and the logic value of LEDC bit in BCICTL2 register.
This means that as long the precharge current is enabled the driver will be enabled and led in on state, SW control of led state will be possible only when the precharge is disabled.

7.1.6 Audio application schematics

This section illustrate some audio application schematic examples. Most of them have been already adopted in previous GSM1.5 chipset based on Omega/Nausica ABB.

7.1.6.1 Microphone

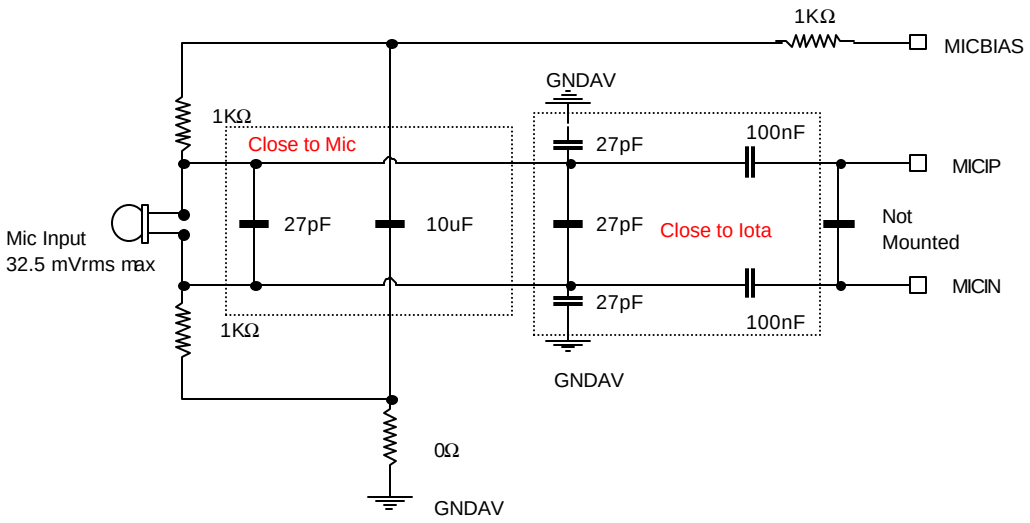


Figure 7-8 Microphone schematic connections

7.1.6.2 Headset Microphone

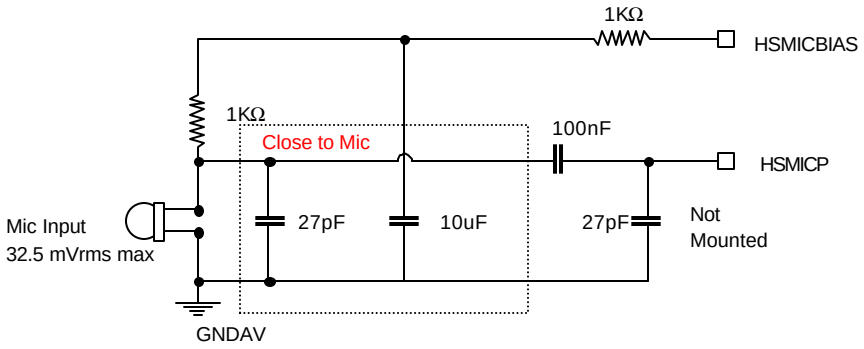


Figure 7-9 Headset Microphone schematic connections

7.1.6.3 Auxiliary Input

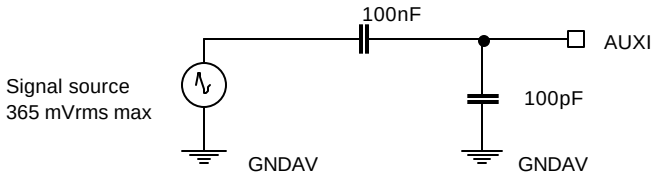


Figure 7-10 Auxiliary input connections schematic

7.1.6.4 Ear output

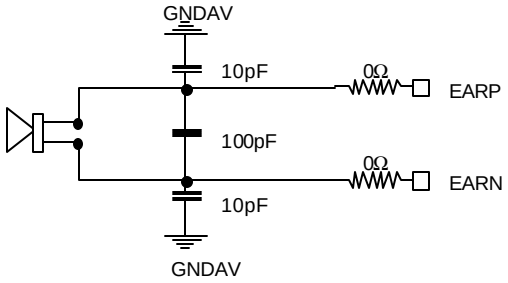


Figure 7-11 Ear Output connections schematic

7.1.6.5 Headset Output

Figure 7-12 Headset Output connection schematic

7.1.6.6 Auxiliary Output

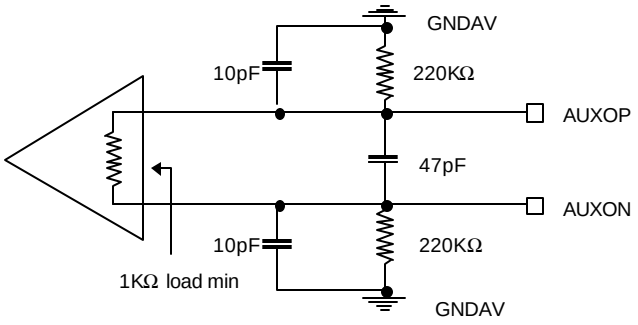


Figure 7-13 Auxiliary Output schematic connections

7.2 Digital

7.2.1 32KHz Oscillator

7.2.1.1 Internal equivalent schematic

The 32KHz oscillator delivers the reference clock for all the system during the first power battery connection and during sleep periods. The most important characteristics of this oscillator are the short frequency stability and the noise rejection ability. To improve as much as possible noise immunity, on CaLypso device, the oscillator is powered separately from the other internal modules. Specifically the ground connection VSSO has been isolated from the other ground connections
Simplified schematic of the internal circuitry is shown Figure 7-14 Internal equivalent schematic

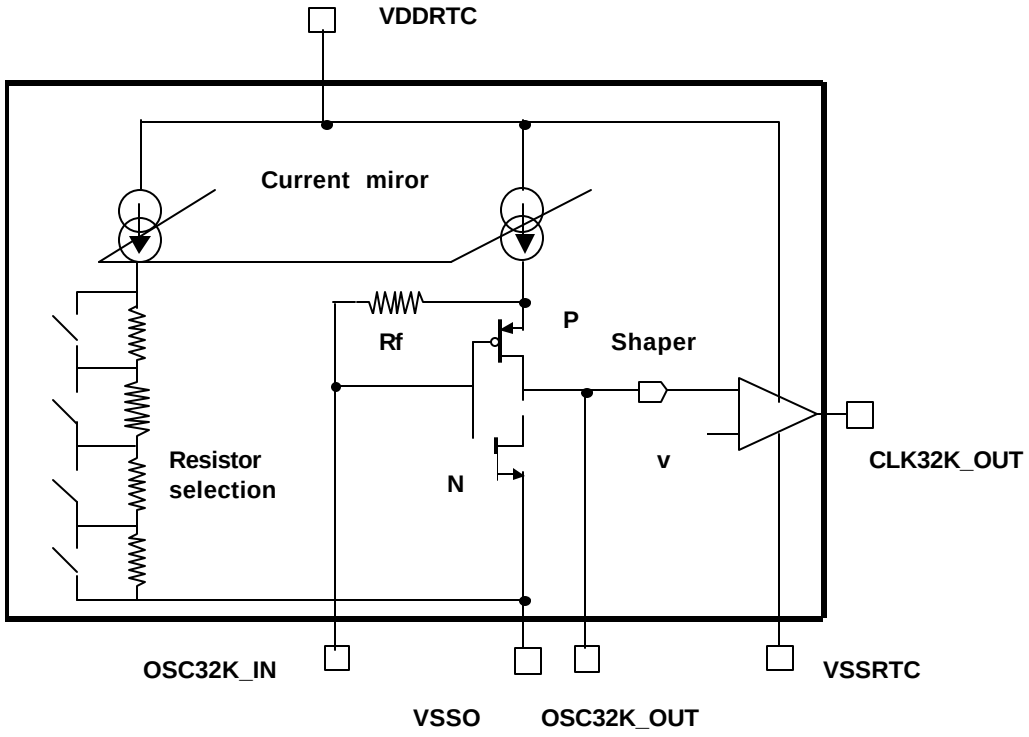


Figure 7-14 Internal equivalent schematic

Oscillator cell is based on a CMOS inverter coupled with the feedback resistor (implemented as a transmission gate). The inverter is powered by a current mirror circuit. The value of the current which is supplied to the oscillator can be adjusted. The change of the resistor value which determine the value of the current mirror is done by modifying the oscillator register contain. Correspondence between the resistor value and register contain is shown in Table 7-12

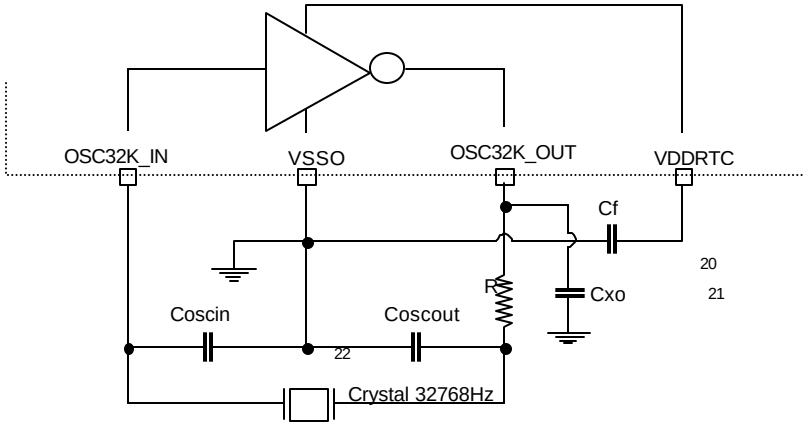
Table 7-12 Current resistance value versus register contents(Calypso C05).

Crystal resistor value	Programmed resistor value	Oscillator current
0 x 2 F	0K	
0 x 2 7	57 K	
0 X 2 E	80 K	
0 X 2 6	137 K	
0 X 2 C	160 K	
0 X 2 4	217 K	
0 X 2 A 0 X 2 2	240 K 297 K	
0 X 2 8	320 K	
0 X 2 0	377 K	

To secure the oscillations start time and to reduce the starting time, the default value at power on corresponds to the lower resistor value, and the maximum current drive in the oscillator.

7.2.1.2 Application

The 32KHz Crystal is connected between input and output of the oscillator (OS32K_IN and OSC32K_out pins), connections being shortest as possible. The two load capacitors are connected on the crystal and common point (ground return current) has to be connected to the dedicated oscillator ground VSSO. Filtering capacitor of the oscillator power supply must be connected to VSSO pin (same point as crystal load capacitor return point) and directly to the nearest VDDRTC pin using connection length as short as possible.
This to prevent frequency jitter performances to be affected by the power supply noise induced by fast internal logic transitions.



[20] Filtering capacitor Cf connections as short as possible.
[21] Filtering capacitor Cxo connections as short as possible.
[22] Capacitors and ground plan connections to VSSO pin as short as possible.

Figure 7-15 External Components

Capacitor Cxo (10Pf) has to be connected between OSC32K_OUT pin and ground. It prevents high frequency noise at shaper input stage thus avoiding degradation of jitter performances of the 32K logic signal.

7.2.1.3 External Components value and crystal specifications

External components value depends on the specification of the crystal which is used in the application. General informations are given on the Table 7-13

Table 7-13 External components general informations

Parameter	Description	Note	Min	Typic	Max	Unit
Frequency	Crystal spec		-20ppm	32.768	+20ppm	Hz
R	Crystal drive resistor	[1]		100		KOhm
CL	Crystal load capacitor	[2]	6		12.5	pF
C32Kin/out	Crystal to VSS capacitor	[3]	12		25	pF
R1	Crystal series resistor	[4]			100	KOhm

[1] Oscillator output resistor

Tuning fork crystal model may oscillate in a spurious tort ional mode, around 200KHz, instead of fundamental frequency at 32KHz when oscillator has enough gain at this frequency.
This resistor provides a cut frequency on the oscillator gain characteristic. The cut frequency value is determined according to the value of the capacitor which is connected to oscillator output. Cut frequency value must be between the two resonance, fundamental and spurious frequencies.

[2] Crystal load capacitor.

This parameter is the value of the capacitor to be connected across the crystal to have it oscillating at the frequency of 32.768HZ specified in the crystal datasheet.
Depending of the crystal model and of the crystal manufacturer this value can be different. Usual value is between 6pF min and 12.5pF Max.

[3] Phase load capacitors

The value of the capcitor to be put from crystal to ground (VSSO) depends on the crystal load specified by the crystal manufacturer. The two capacitors may have different values but the equivalent impidance of the two in series has to be equal to CL specified in the crystal data sheet.

CL= (Coscin * Coscout) /(Coscin + Coscout)

Other wise the frequency of the oscillation will be slightly different than the one specified in the crystal data sheet.

[4]Crystal series resistor.

This crystal parameter must be considered as the most important. R1 in the crystal data sheet represents the power lost in the crystal that must be compensated by the oscillator for the oscillation start. A too important value can prevent the oscillations starts.

7.2.1.4 Equivalent crystal schematic

Close to the crystal frequency resonance, the equivalent electrical circuit t of the crystal is the one of figure( ) .On this schematic, the capacitor C0 is the stray capacitance between the electrodes and the crystal holder. R,L,C represent the mechanical behavior of the crystal. L1, C1 represent the elasticity of vibrating system at the fundamental frequency and R1 the energy lost at the same frequency. This energy that must be compensated by the oscillator for the oscillation start. L2, C2,R2 have been added to take into account the potential spurious resonance around 200KHz.

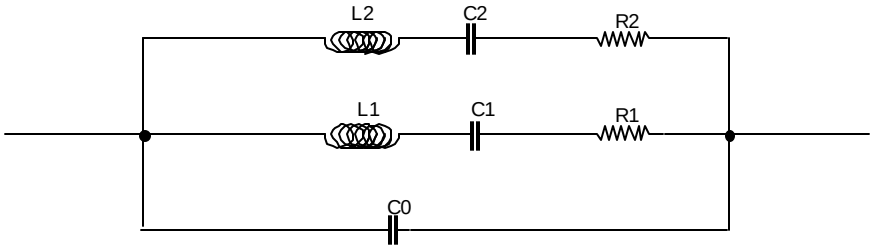


Figure 7-16 Equivalent resonant circuit

7.2.1.5 Typical parameters value measured on market available crystals.

Table here under, gives a quick overview of the data sheet for different crystals available on the market. Values of the table can be used for simulation program.

Table 7-14 Typical parameters value measured on market available crystals

Parameter/crystal	Microcrystal MS2	Epson MC146	Sunny CH-206
C0	1pF	0.8pF	0.9pF
C1	2.2fF	1.9fF	2fF
FL	32.768Hz +/-20ppm	32.768Hz +/- 20ppm	32.768 Hz +/- ppm
CL	12.5pF	7pF to 12.5pf	6pF min
Rs(Fundamental)	90Kmax	65K max	50K max
Rs (Harmonic 6th)	20K typ	400K typ	none
Power drive	1uW	1uW	1uW

Parameter/crystal	Microcrystal MX1 -T	Seiko SSP-T	Microcrystal CC5
C0	1.5pF	0.95pF	1.4 pF
C1	1.7fF	Not specified	2.25fF
FL	32.768 Hz +/- 20ppm	32.768 Hz +/- 20ppm	32.768 Hz +/- 20ppm
CL	10pF	7pF to 12.5pF	9pF to 12.5pf
Rs (Fundamental)	100K max	55 K max	100 K max
Rs (Harmonic 6th)	40K typ	none	30 K typ
Powe drive	1 uW	1 uW	1uW

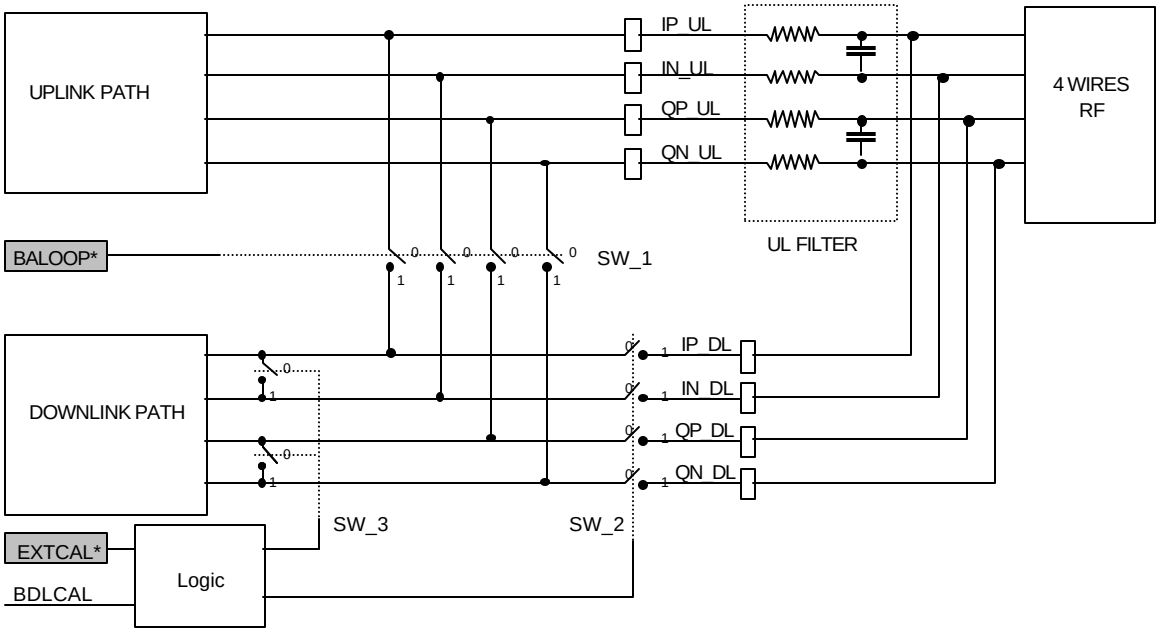
Parameter/crystal	Microcrystal CC4V-T	SM-14J KDS	Sunny CS-406
C0	1pF	1.05 pF	0.85pF
C1	2.25fF	1.9 fF	2.0 fF
FL	32.768 Hz +/- 20ppm	32.768 Hz +/- 20ppm	32.768Hz +/- 20ppm
CL	12.5pF	12.5pF	6pF min
Rs (Fundamental)	90K max	70 Kmax	50 K max
Rs (Harmonic 6th)	50K typ	none	none
Power drive	1 uW	1 uW	1uW

Generally, the value of CL can be modified on request when ordering. Value is comprised for all the models available between 6pF min and 12.5pF max. Nominal frequency of 32.768Hz corresponds to the frequency of the oscillations, when the crystal is loaded by the capacitor CL specified in the data sheet

Series resistor at the spurious resonance (around the harmonic 6) is not specified in the data sheet. The value is the table is a typical value measured on samples. The resistor value cannot be measured on all crystal models. For some of them, the resonance phenomena is not detectable.

7.3 RF

Iota device is able to support eight wires and four wires RF. In the case of a four wires RF I/Q signals should be connected as described in the schematics
SOLUTION 1: Hardware connection of UL and DL paths. BALOOP bit to logic 0 (SW_1 open)

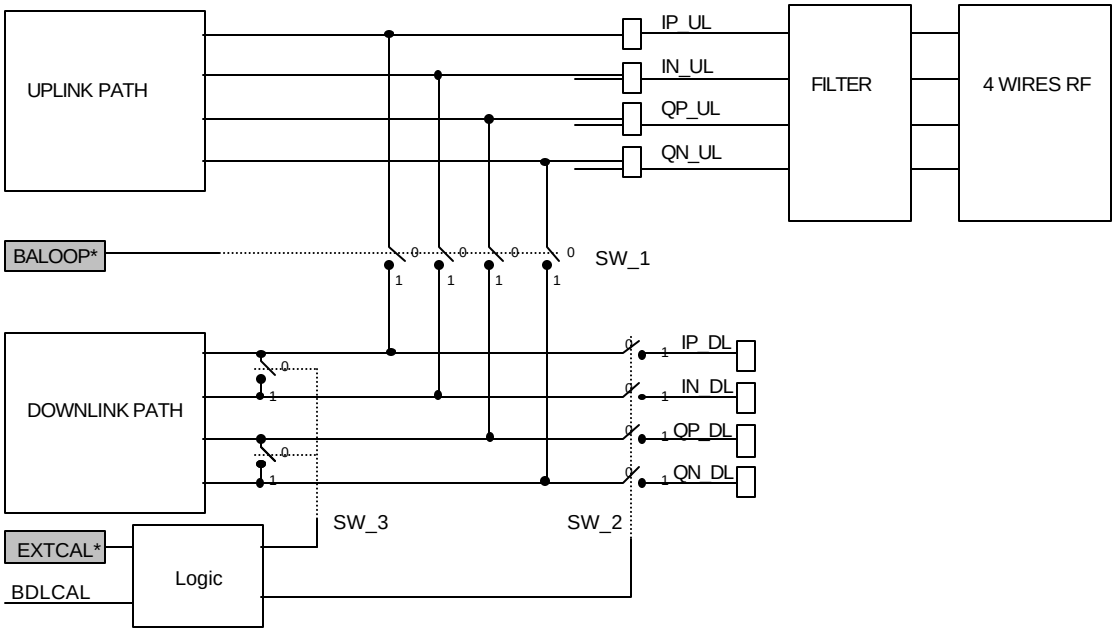


* Shaded blocks correspond to register bit locations.

Figure 7-17 Four wires RF connections to Iota, Solution1

This solution does not require SW modification respect to the 8 wire RF connection. The uplink path is in high Z when the signal BULON is low hence allowing the downlink path to be enabled. Same type of switches (SW1 has the same characteristic as SW_2) have been used on the DL path to avoid impedance differences between this solution and an 8 wire solution.
SW_2 is used to separate the DL path from the external during an internal DL calibration.
In this case SW_1 must stay open thus BALOOP = 0.

SOLUTION 2: Multiplex implemented through Iota internal BALOOP register bit (SW_1 closed under DSP control)



* Shaded blocks correspond to register bit locations.

Figure 7-18 Four wires RF connections to Iota, Solution2

Switch between UL and DL path is implemented in SW programming the Iota BALOOP bit at logic one in BBCTL register. This bit controls HW connection between UL and DL paths through SW_1.

Programmation of the BALOOP could be executed under MCU or DSP control.

If the control is executed through MCU, BALOOP bit has to be programmed to logic one at the initialization and then left to this value (minor MCU SW modification).

Through DSP could be possible to manage in a sharper manner the switch SW_1, selecting it to be closed just before executing a downlink operation than opening it at the end of the DL window (huge SW modifications are required).

This solution has two penalizing drawback consisting in:

- The elimination of the internal downlink calibration. This because SW_2 is no longer able to separate the DL path from the external world (see position of SW_2 in the schematic) hence result of DL calibration will always include all the DL path (ABB and RF).
- Required UL filter is also on the DL path.

8 System hints

8.1 Calypso power balls assignment

Due to uBGA packaging structure, it is not easy to implement on PCB a good electrical ground plan. To facilitate the PCB lay out and to improve signal integrity and EMC performances on Calypso device all the ground pins are placed on the balls raws closest to the package sides. So, ground connections to Ground plan reference are very short. This Reduce ground connection to a minimum possible length.
To make easy PCB design and to improve filtering efficiency Calypso power pins are also placed close to package sides and close to the corresponding ground pin for the different internal concerned module.
To take advantage of this pin assignment all ground connectons have to be done directly to the PCB ground plan close to package and capacitor for filtering has to be put on the nearest Vdd pin.

Table 8-1 Ground connections

CALYPSO			IOTA			Comments
Pin Name	Pin nb	Ball	Pin Name	Pin nb	Ball	
GROUND CONNECTIONS						
VSS	4	B1				
	17	F1				
	32	K1				
	46	P2				
	52	P4				
	69	N8				
	79 89	P10 P13				
	113	G14				
	146	A10				
VSSPLL	122	E14				
VSSRTC	130	C14				
VSSANG	123	E12				
VSSO	134	A14				
			GNDD	97	A3	
			GNDA	57	G10	
			GNDL	76	B9	Ground for Led driver
				77	A9	Ground for Led driver
			REFGND	82	A7	Real REFGND
				38	F5	GNDAV
				86	C6	AUXGND

8.1.1 Recommended chips placement and filtering rules .

On IOTA device , the soldering balls dedicated to power supply intended to power Calypso are located on the same package side. Particular care has been taken to avoid aver crossing of the different power supply lines on the PCB between Calypso and Iota. (This to minimize the

number of via.) The best placement strategy for the two components to optimize PCB layout is represented on Figure 8-1

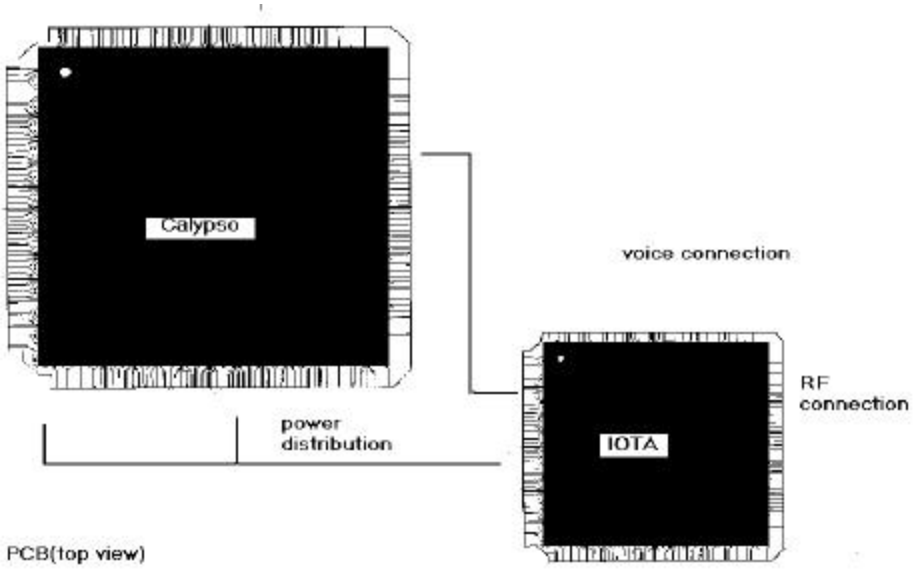


Figure 8-1 Recommended Chip placement

Each IOTA regulator output needs for stability performance and time response a tank capacitor. This capacitor must be connected as close as possible from the regulator output and the ground return current lead connected to general power ground. Reference ground has to be connected not too fare from the common ground point. To cancel high frequency noise generated by calypso fast transitions, a ceramic capacitor is required as close as possible to Calypso power pin as it is shown on
Figure 8-2

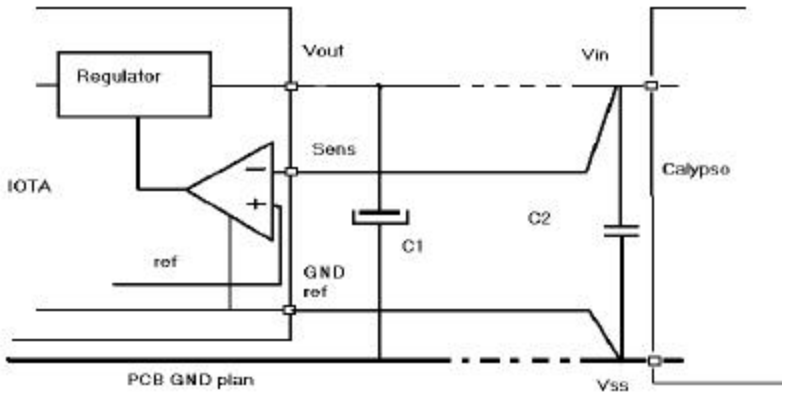


Figure 8-2 Capacitor placing

8.1.2 Capacitors Value recommendation

8.1.2.1 Iota Power Supplies

Table 8-2 Iota capacitors values

Iota LDO	Capacitor value	Recommended ESR	Ground pin	Comments
VRDBB	10uF	0,01Ω <Rs< 0.6 Ω	General ground	Sense input connected to terminal voltage to be regulated
VRRTC	1 uF	0,01Ω <Rs< 0.6 Ω	General ground	
VRMEM VRIO1/VRIO2	4.7 uF 10 uF	0,01Ω <Rs< 0.6 Ω 0,01Ω <Rs< 0.6 Ω	General ground General ground	
VRSIM	1 uF	0,01Ω <Rs< 0.6 Ω	General ground	
VRRAM	4.7uF	0,01Ω <Rs< 0.6 Ω	General ground	

8.1.2.2 Calypso Power Supply

Table 8-3 Calypso capacitors values

Calypso supply	Capacitor value	Calypso pins	Comments
VDD	100nF	P7, E1, G1, A5, B12, F11	HF noise suppression
VDD-RTC/VDDS-RTC	100nF	D14	HF noise suppression
VDDS-MIF	100nF	G1, A4	HF noise suppression

9 APPENDIX

9.1 Connection schematic Nausica Calypso

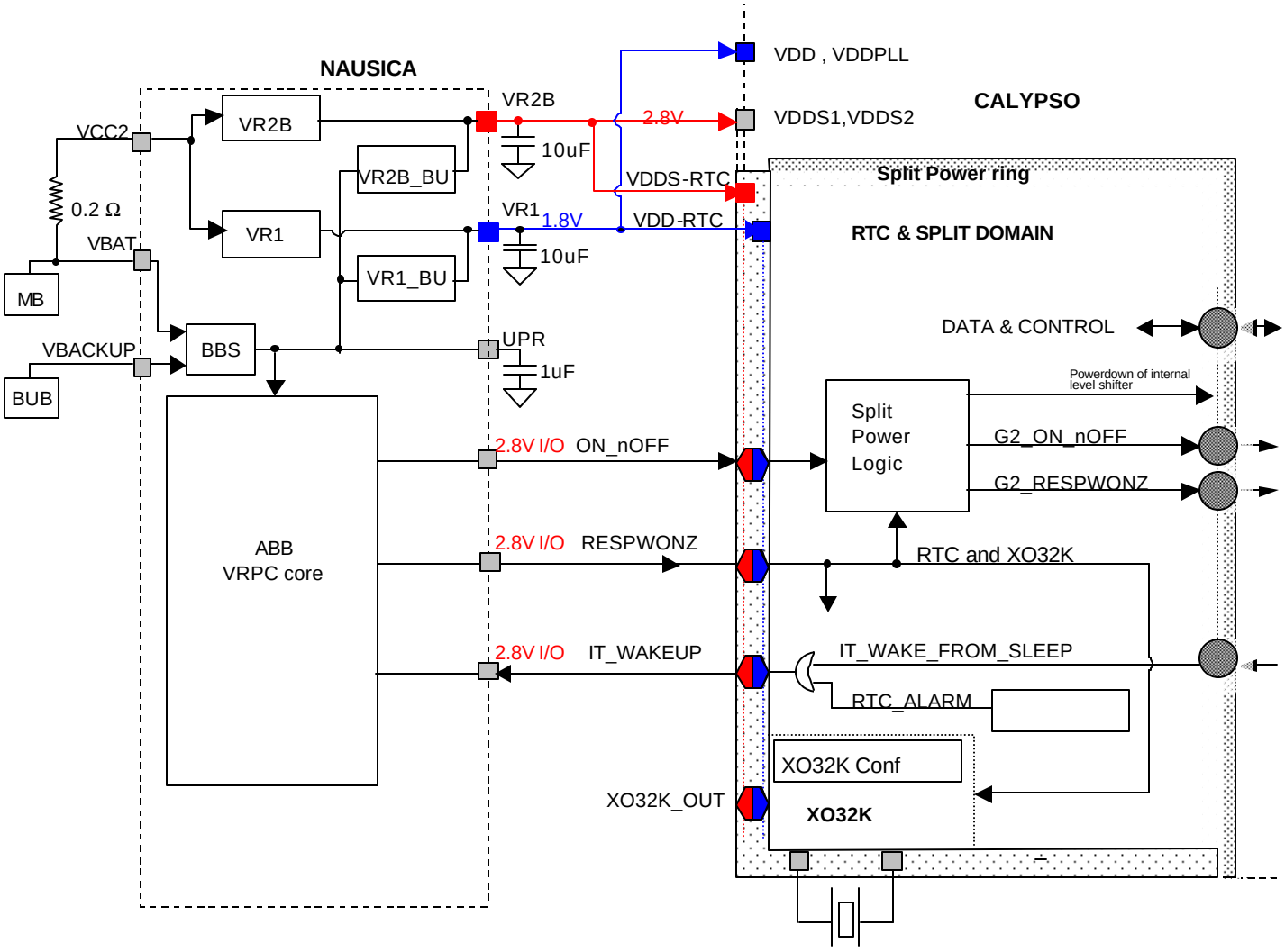


Figure 9-1 Calypso to Nausica connection schematic for split power

9.2 Power supply connections between Nausica/Iota and Ulysse/Calypso

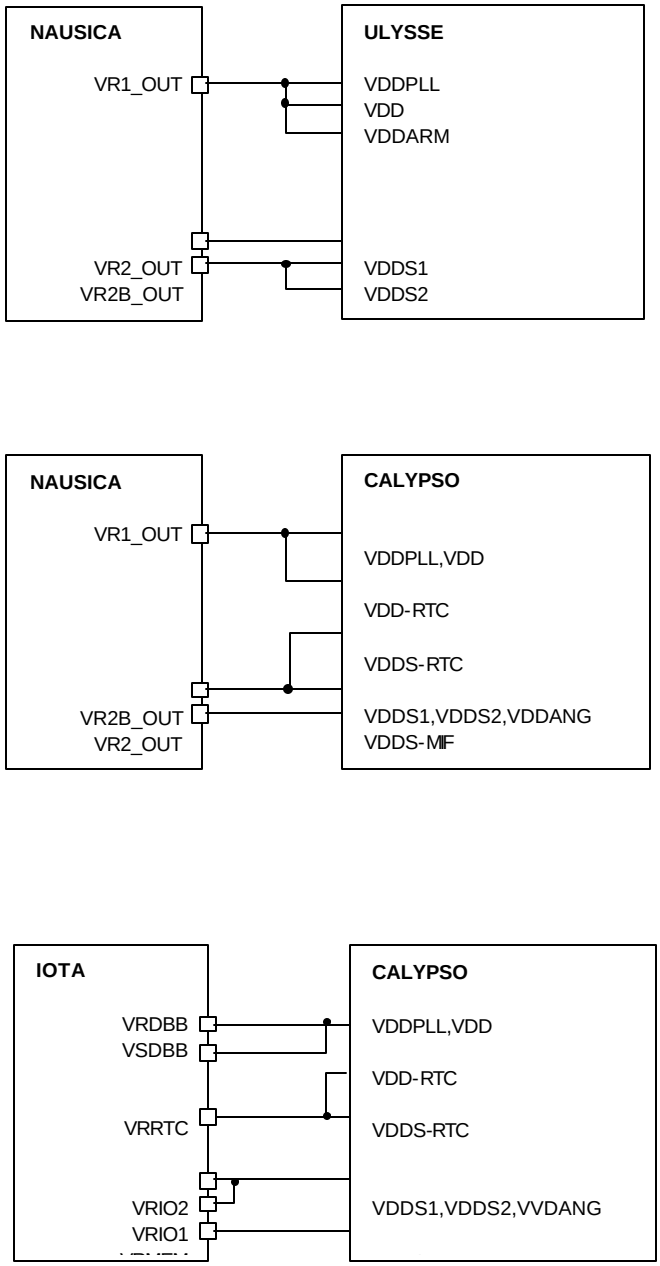


Figure 9-2 ABB to DBB supply connections