Pop noise cancellation

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	Originator	Approval	Quality
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HISTORY

Version	Date	Author	Notes
Ver: 1.0	6/26/01	L.Indiani	1
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Ver: 4.0			4

NOTES :

1. Creation
2. POP cancellation lab validation.
3. ……..
4.

GLOSSARY

VDL	Voice Down Link
HSO	HeadSet Output

REFERENCE DOCUMENTS

TWL3014	rev 2.0 (not yet approved)

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1. Pop cancellation architecture and functional description

Assumption:
Pop noise is due to the audio output amplifier being switched on.
Although the speaker is AC coupled through an external capacitor, the sharp rise time given by the activation of the bias causes a large 'spike' to propagate to the 32Ω earpiece which is uncomfortable to the user.

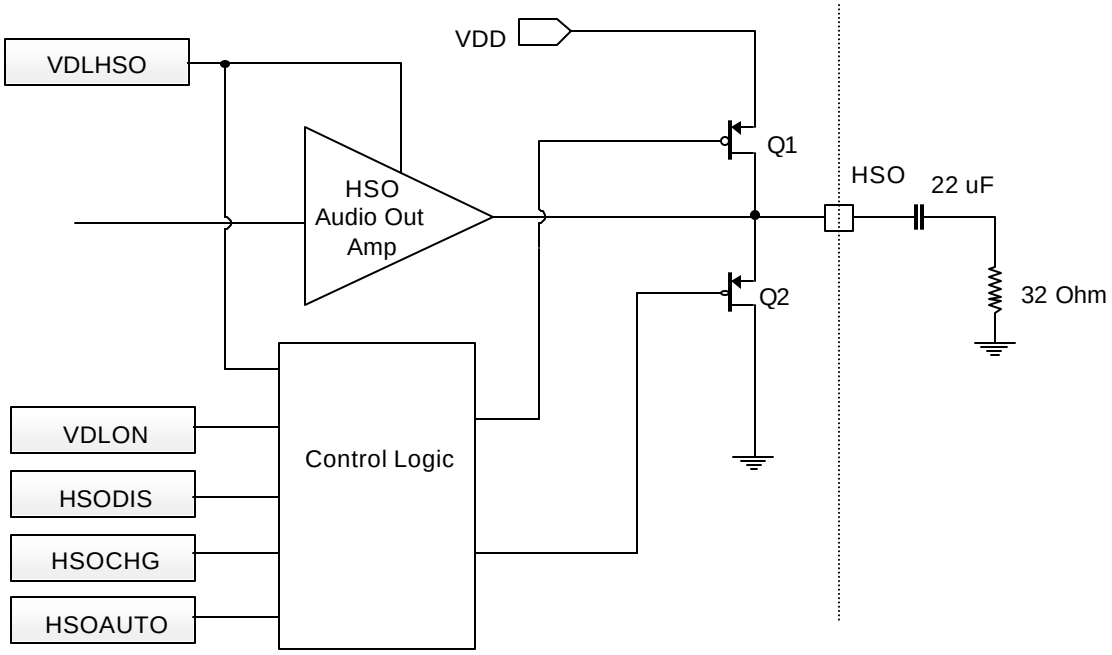

Figure 1-1 Pop cancellation architecture

Shaded blocks in the picture correspond to physical register bit locations. Pop cancellation is achieved through a pre-charge of the 22 uF output capacitor. The two transistors Q1 and Q2 impose the pre-charge voltage to be VDD/2 when both are enabled by the control logic. Discharge of the output capacitor is possible as well through the Q2 transistors with Q1 disabled.
Size of the two transistors has been chosen to have a typical precharge voltage rise time of 13 ms. Possible range for this timing considering process, temperature and supply variations is between 7 ms and 20 ms. Estimation of current consumption during precharge is 3mA average.
This evaluation and correct transistor sizing is possible once the external load to drive and charge status of the external capacitor before precharge are known.
Thus same architecture could be implemented on other VDL output amplifiers if those data are available.

The control logic receives as inputs the following signals:

VDLON: This signal is the powerdown of the DL audio path.
At logical zero all voice downlink is disabled.
At logical one all voice DL is enabled (digital and analog) except the output amplifiers.

VDLHSO: This signal is the enable of the headset amplifier.
At logical zero the HSO is disabled.
At logical one the HSO is enabled.

HSODIS: This signal enables the discharge of the external capacitor
At logical zero the discharge is disabled.
At logical one the discharge is enabled.
This bit has NO effect when:

- HSOCHG is set to logical 1, precharge is prioritized
- VDLON is set to logical 0, VDL path is disabled
- VDLHSO is set to logical 1, HSO out amp is enabled

HSOCHG: This signal enables the precharge of the external capacitor.
At logical zero the charge is disabled.
At logical one the charge is enabled.
This bit has NO effect when:

- VDLON is set to logical 0, VDL path is disabled

The HSOCHG could be configured to run in AUTOMATIC mode, in this case:

- This bit is set automatically to logic 1 on a rising edge of VDLON.
- This bit is cleared automatically to logic 0 when the VDLHSO is enabled.
- Write accesses have no effect on the analog part while the AUTO bit is set to logic 1.

Running in NORMAL mode :

- This bit has NO effect when VDLHSO is set to logical 1

HSOAUTO: This signal configures the functional mode of the precharge bit.
At logical zero HSOCHG runs in NORMAL mode.
At logical one HSOCHG runs in AUTO mode.

2. Voice timings with precharge in normal mode:

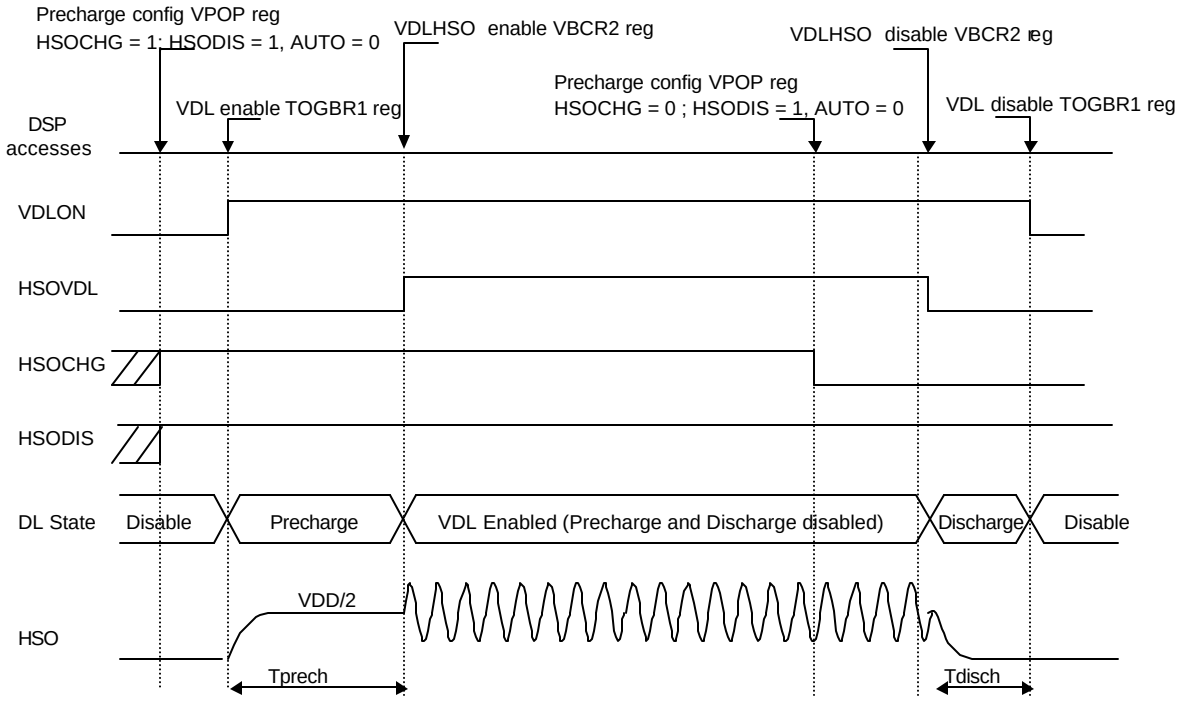

Figure 2-1 HSOCHG in normal mode

Each time the voice path is enabled the described register access sequence has to be performed in order to allow correct precharge and discharge of the HSO node
The precharge time interval Tprech and the discharge time interval Tdisch are under SW control.

3. Voice timings with precharge in auto mode:

First Voice path enable:

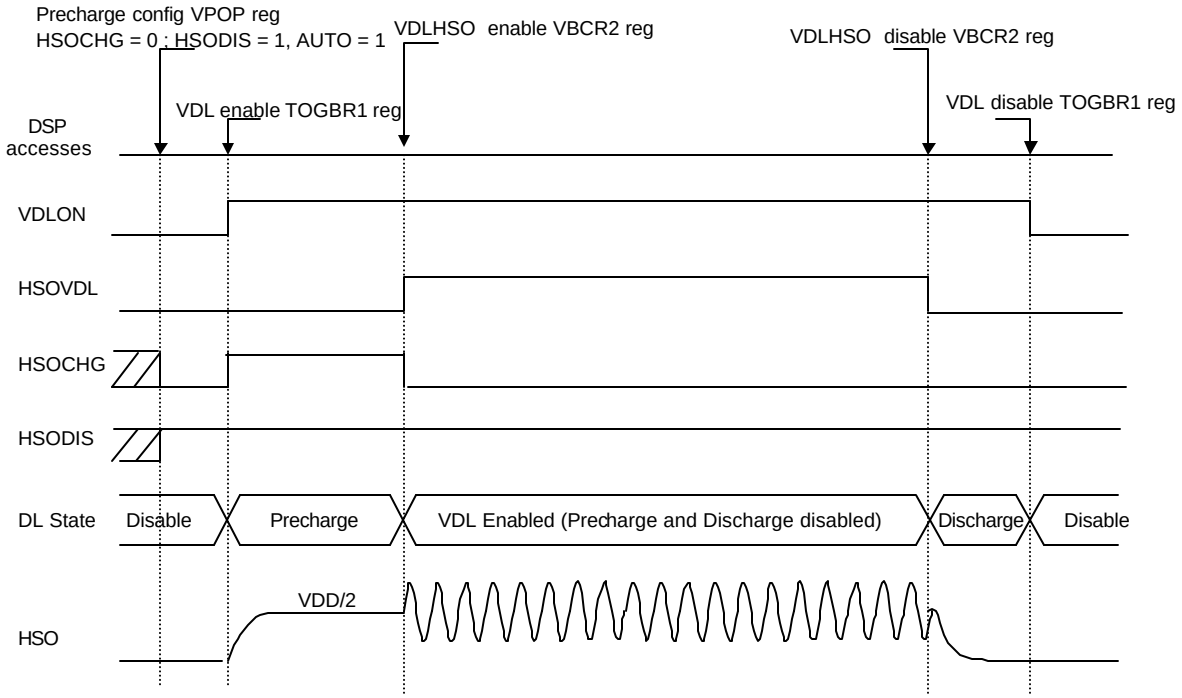

Figure 3-1 First enable of VDL in HSOCHG in auto mode

Successive VDL voice path enable (After Auto mode configuration)

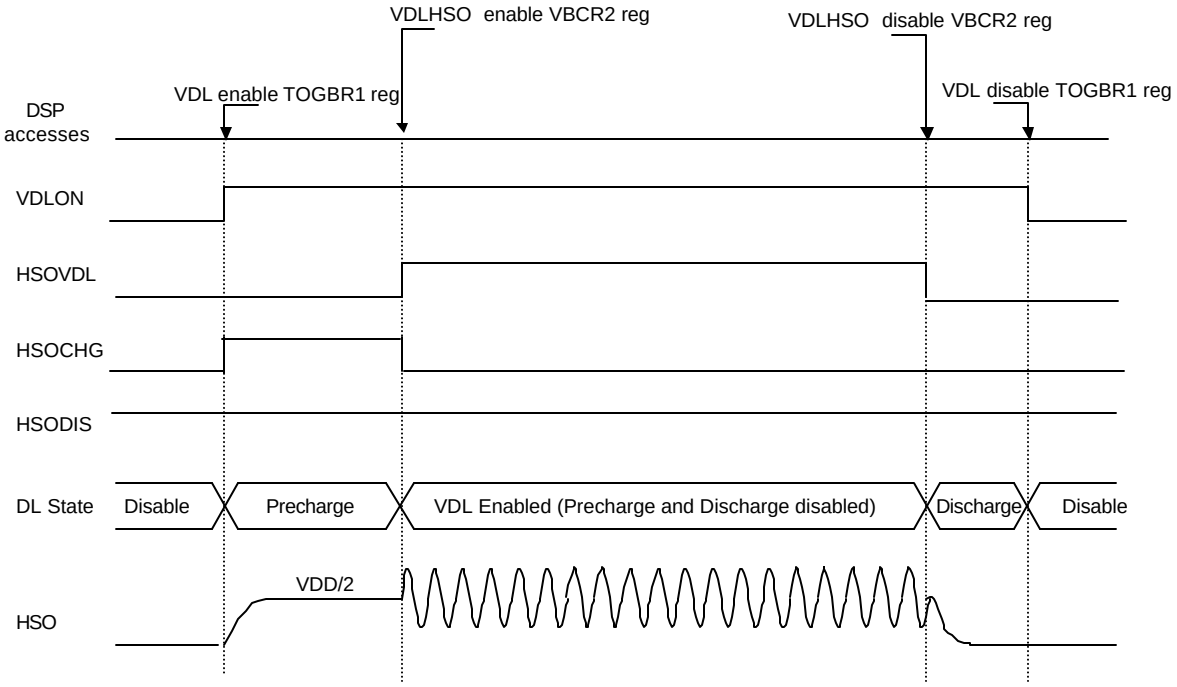

Figure 3-2 Successive enable of VDL in HSOCHG in auto mode

4. Validation on the HSO output

These tests are done with a real head set as HSO load.

4.1 POP noise cancellation system is not used.

First of all, you have to notice that in the application, the output amplifier is turned ON before the VDL module, or after it but in a time below 20ms.

To not use the anti-pop system, you have to set the VPOP register in such a way that the output amplifier is in NORMAL mode and the external capacitor charge and discharge are disabled as described in the previous chapters. It means VPOP = ”0x000”.

A correct scenario is:

1. VPOP register sets.
2. HSO amplifier ON (bit in VBCR2 register)
3. VDL ON (bit in TOGBR1 register) => the loud POP is heard, caused by a voltage drop from 0V to the reference voltage, the external capacitor is not first charged.
4. HSO OFF
5. VDL OFF =>slow discharge #25s

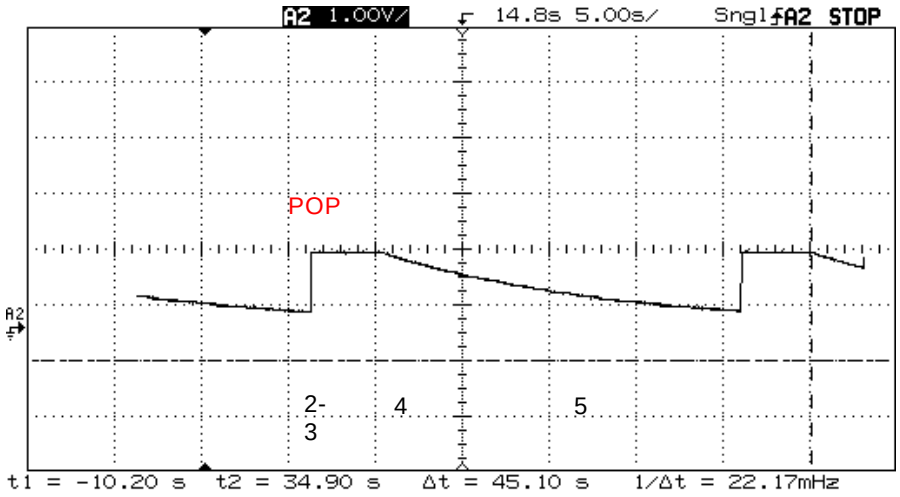

Figure 4-1 Enable of VDL and HSO in normal mode, with disabled capacitor charge. No input signal is applied on the Voice

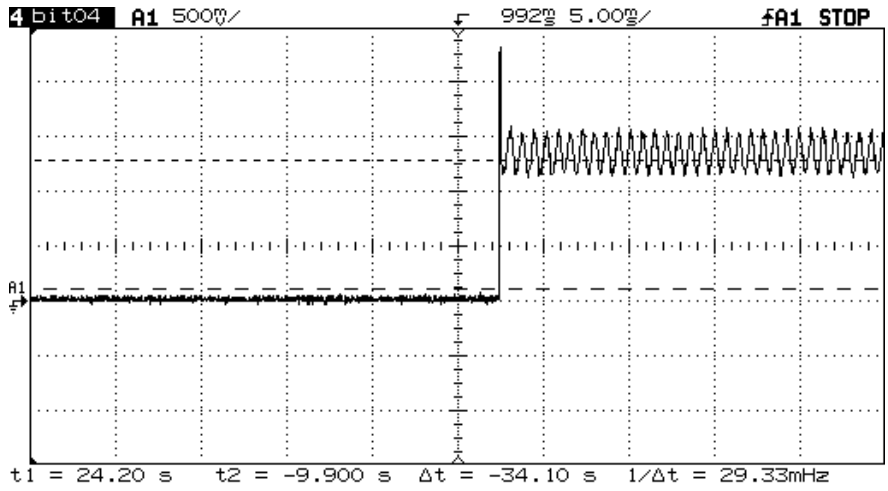

Figure 4-2 Zoom In: VDL and HSO are switching ON, in normal mode, with disabled capacitor charge. Input signal is applied on the Voice

4.2 POP noise cancellation system is used.

To use the anti-pop system, you have to set the VPOP register in such a way that the output amplifier is in AUTO or NORMAL mode and the capacitor discharge is enabled.
According to the selected mode, the external capacitor charge will be enabled automatically or by your own as described in the previous chapters.
This test is realized in an automatic way, and then the VPOP register value is “0x005”.

After loading the configuration of pop cancellation, you can follow the same scenario:
1. VDL ON => quick charge < 20ms; a quiet pop is heard relative to the 200mV voltage drop.
2. HSO ON => second quiet pop is heard (voltage drop of 75mV).
3. HSO OFF
4. VDL OFF

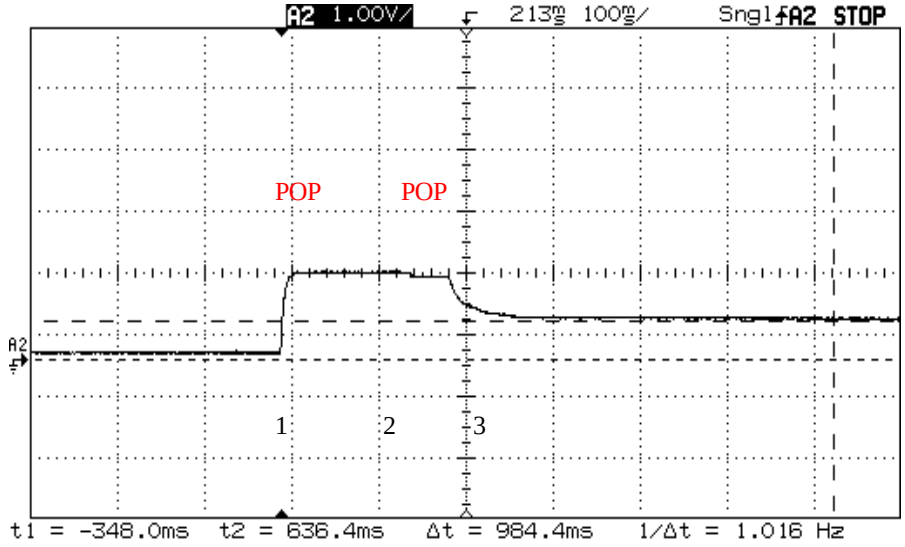

Figure 4-3 Enable of VDL and HSO in auto mode. No input signal applied on the Voice.

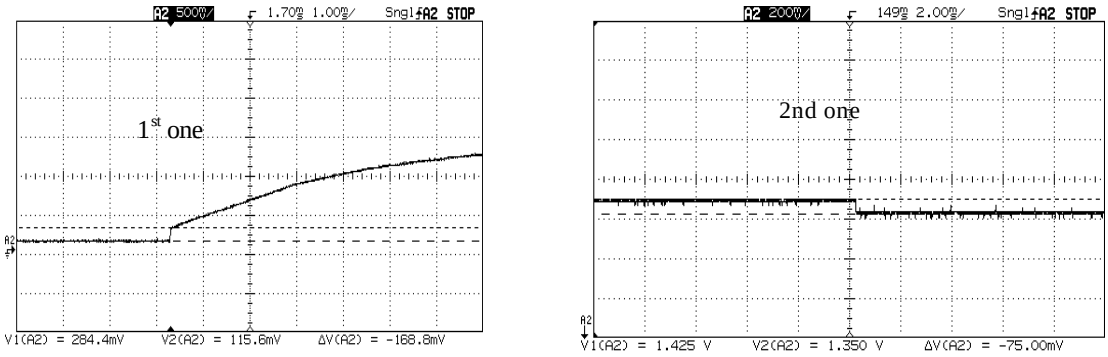

Figure 4-4 Zoom In: the VDL and HSO are switching ON, in auto mode. No input signal applied on the Voice.

If a signal is present on the voice input, only the first quiet pop is heard when the VDL is switched ON; the second pop, due to HSO switching on, will be not audible.

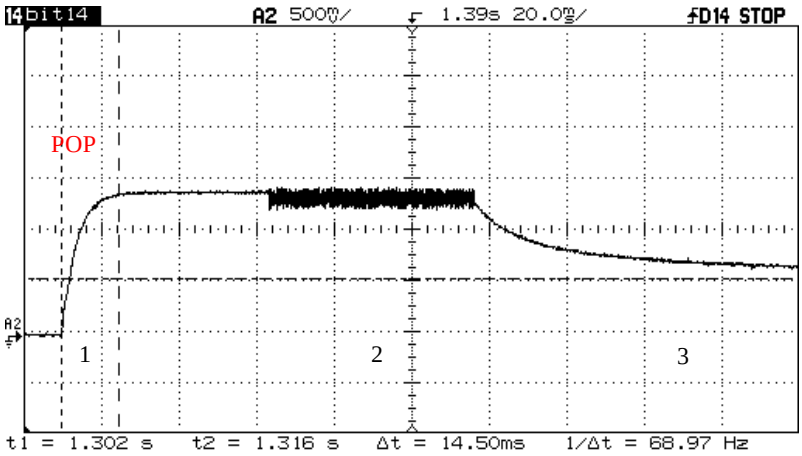

Figure 4-5 Enable of VDL and HSO in auto mode. Input signal applied on the Voice.

4.3 Conclusion

The implemented system allows the noise reduction but not a complete cancellation of it.