Application Notes

System transitions in IOTA
Rev 1.0

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Department: EWTBU

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HISTORY

Version	Date	Author	Notes
Ver: 1.0	4/2/02	Cardi.D	1
Ver: 2.0			2
Ver: 3.0			3
Ver: 4.0			4

NOTES :

1. Creation
2. ……..
3. ……..
4.

GLOSSARY

REFERENCE DOCUMENTS

TWL3104 Specification Ver1.0
Calypso/Iota/Clara System application note APN0 Ver1.1

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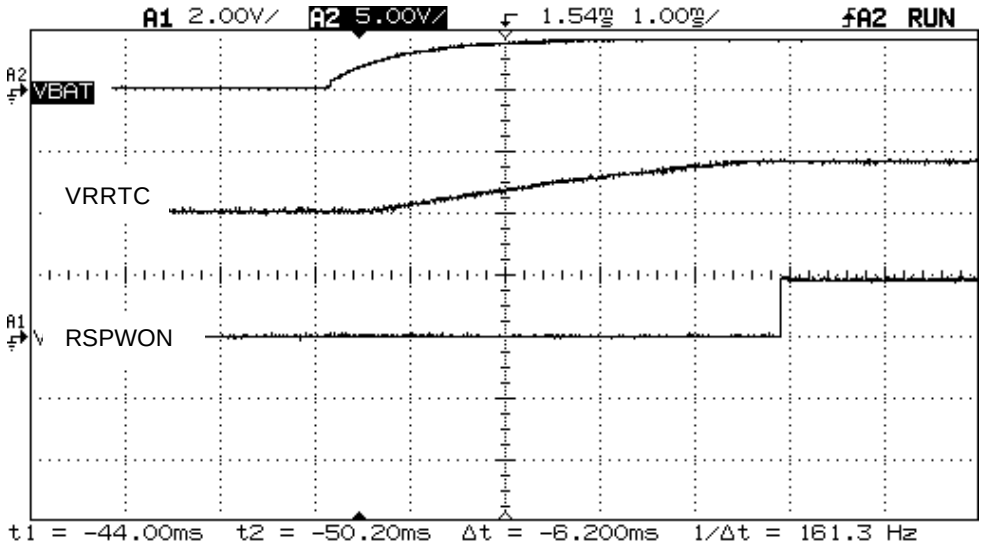
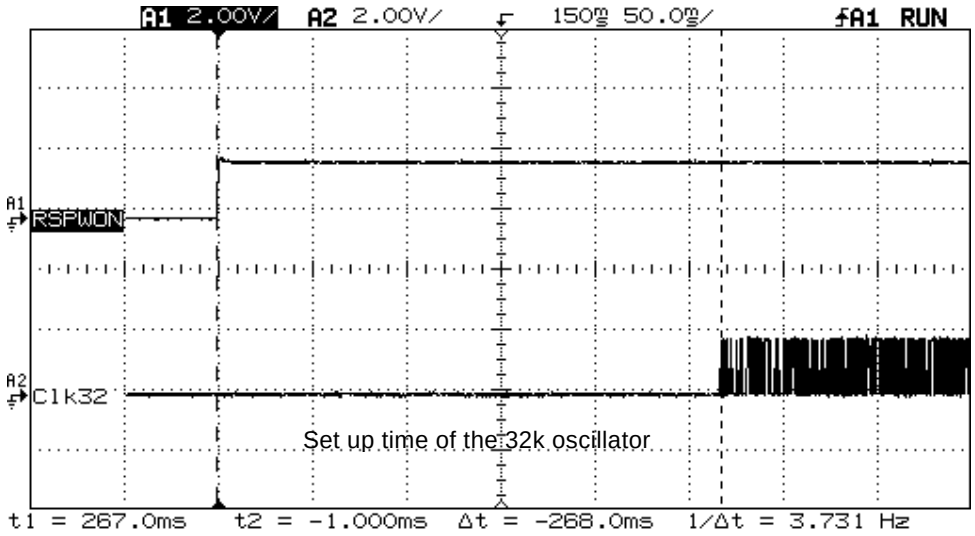
This document describes the different IOTA system transitions and their associated timing charts. It has been done with an EMI_CONSO board including IOTA and CALYPSO devices.

1 POWER ON

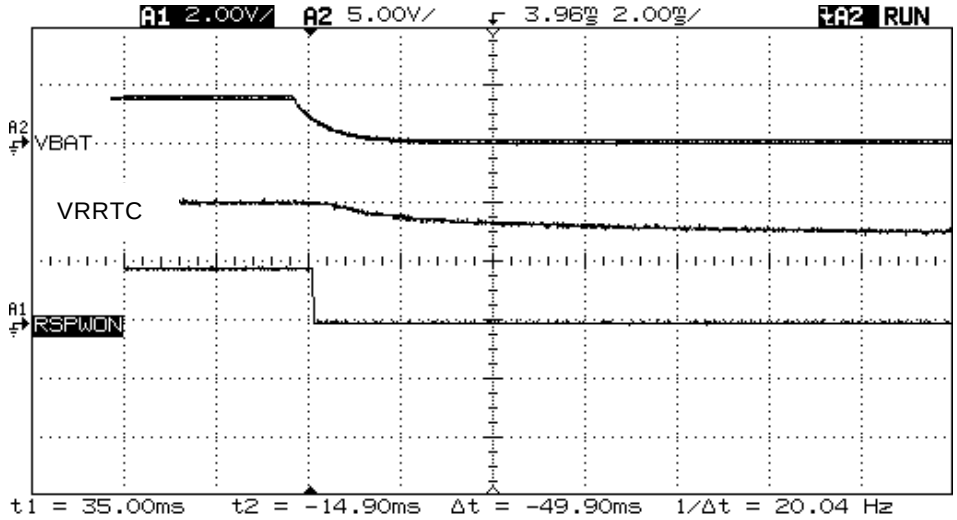
This transition characterizes the insertion and the presence of the Main Battery higher than 3.2V. The mobile passes from the NO SUPPLY state tothe OFF state.
The RSPWON signal goes high when the RTC regulator reaches his nominal regulated voltage. This is to allow the RTC, 32k oscillator and VRPC state machine resets.
The ON_nOFF signal stays at low logical level cause there is no SWITCH ON con dition.

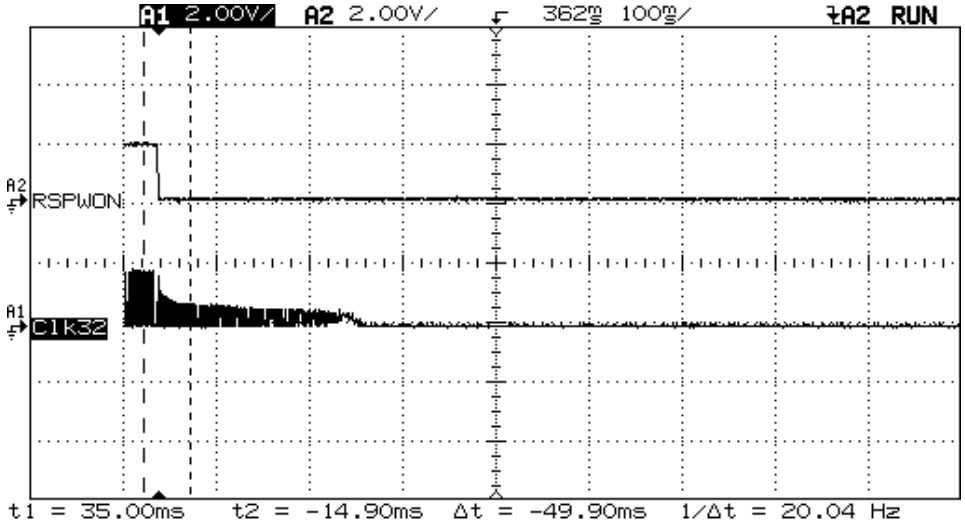




2 POWER OFF

It is characterized by the removal of the battery. The mobile passes in the NO SUPPLY state.





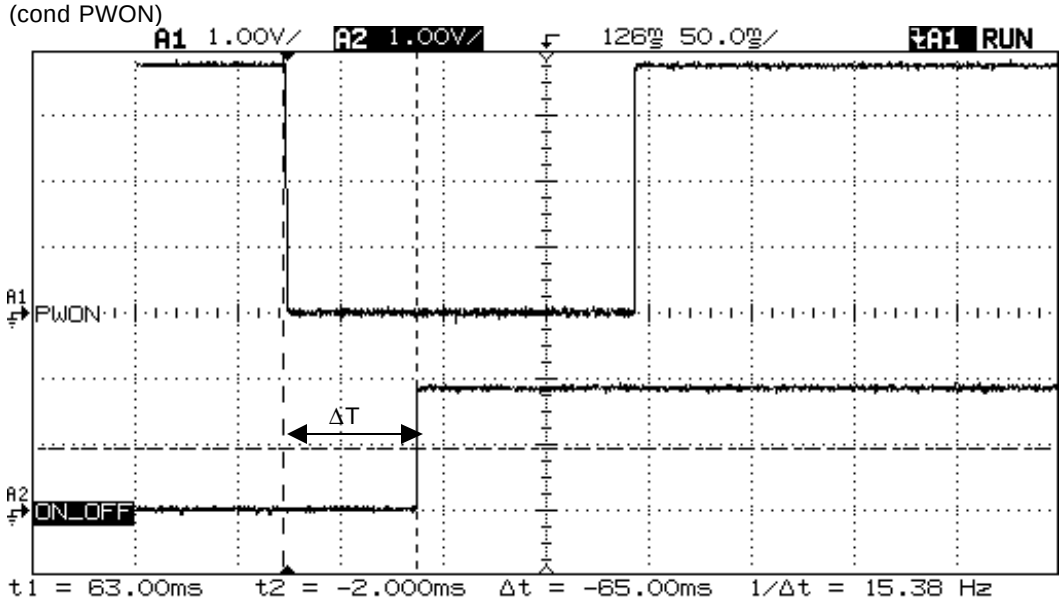
3 SWITCH ON

Switch on is possible when a charged MB higher than 3.2V powers the system.
There are four SWITCH ON events that allow the mobile to exit the OFF state and enter into ACTIVE state:

- Falling edge on the Iota PWRON pin
- Falling edge on the Iota RPWRONZ pin.
- Rising edge on ITWAKEUP pin
- Voltage on CHG pin higher than the voltage on VBAT pin (charger insertion).

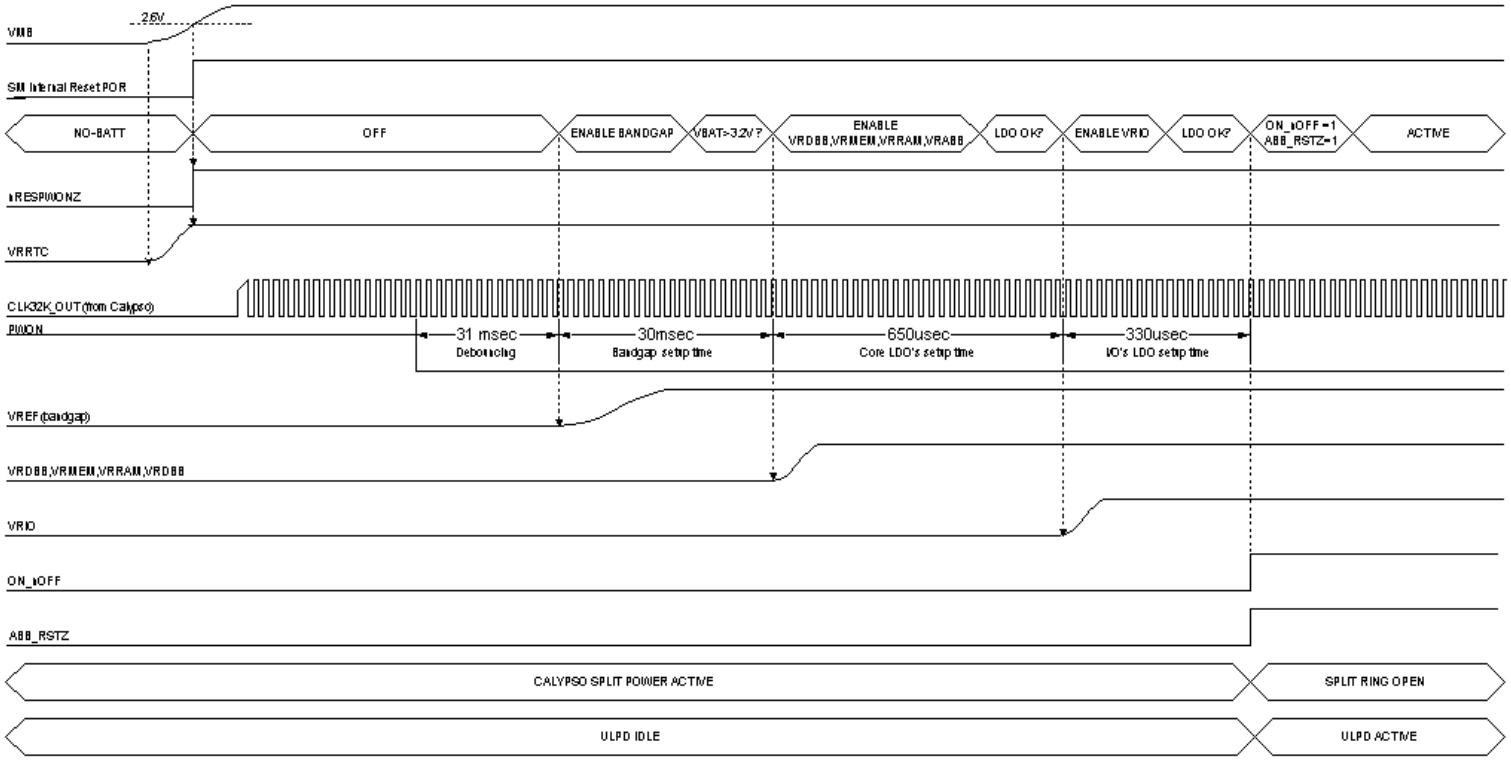
The ON_nOFF signal becomes high after the Iota power management sequence is completed. (All LDOs are enabled, and deliver requested supply) (See on the next page, the chronogram of the SWITCH ON sequence)

(cond PWON)



ΔT= 65ms =T_debouncing + T_band-gap-set-up-time + T_core&IO-LDOs-set-up-time

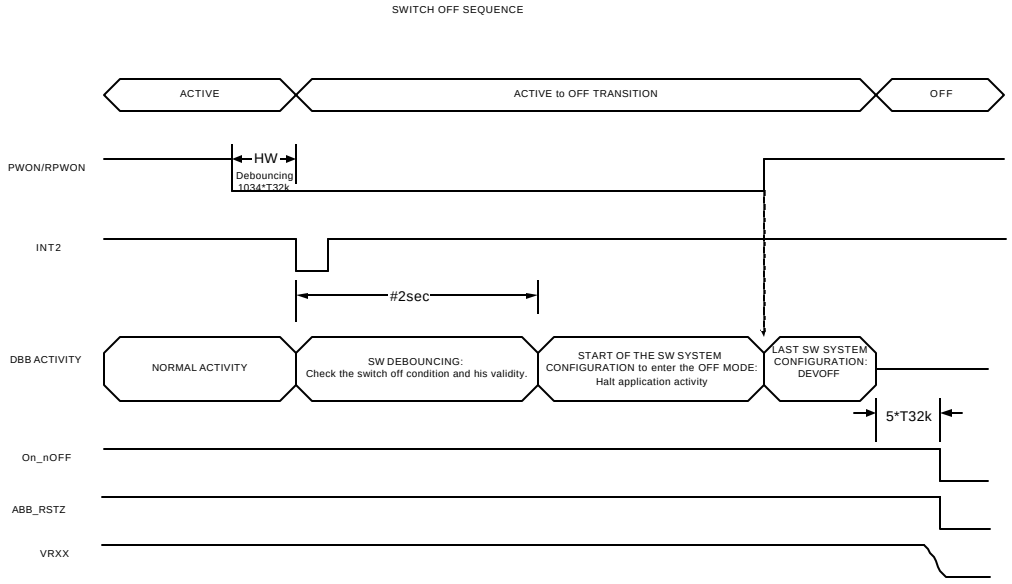
Iota first start upon a pwon button press



Chronogram of the switch ON sequence

4 SWITCH OFF

This transition is initiated by a specific user action consisting in ON/OFF button push. This action generates a falling edge on the Iota PWRON pin. If the PWRON pin level is still low after a HW de-bouncing period, Iota asserts an INT2 request to Calypso. This interrupt is acknowledged by the DBB which starts the SW switch off sequence, disabling Iota modules, terminating it by the write in the VRPCDEV register of the DEVOFF bit. The ON_nOFF signal is forced at low level. The mobile passes in the OFF state.
The system goes also in OFF mode in case of a low main battery (<2.8V). In that case, the ABB sends an INT1 (remaining low) to the DBB, instead of the INT2 signal, signaling an emergency is occurring. From the ACTIVE mode, the mobile passes in the BACKUP mode or the NO-SUPPLY mode, depending on the presence of a charged back-up battery.
The SWITCH OFF sequence remains the same, after sending the INT1, the DBB has 5*Tck32k to treat the interrupt, to start the SW system configuration to enter the new mode. After this delay, the ON_nOFF signal is set to logic zero, LDOs are disabled.



5 SLEEP ON

This transition is initiated on application SW decision. Valid conditions to enter into the SLEEP state are evaluated by the activity management part of theapplication SW in terms of number of frames in which no system activity is required.

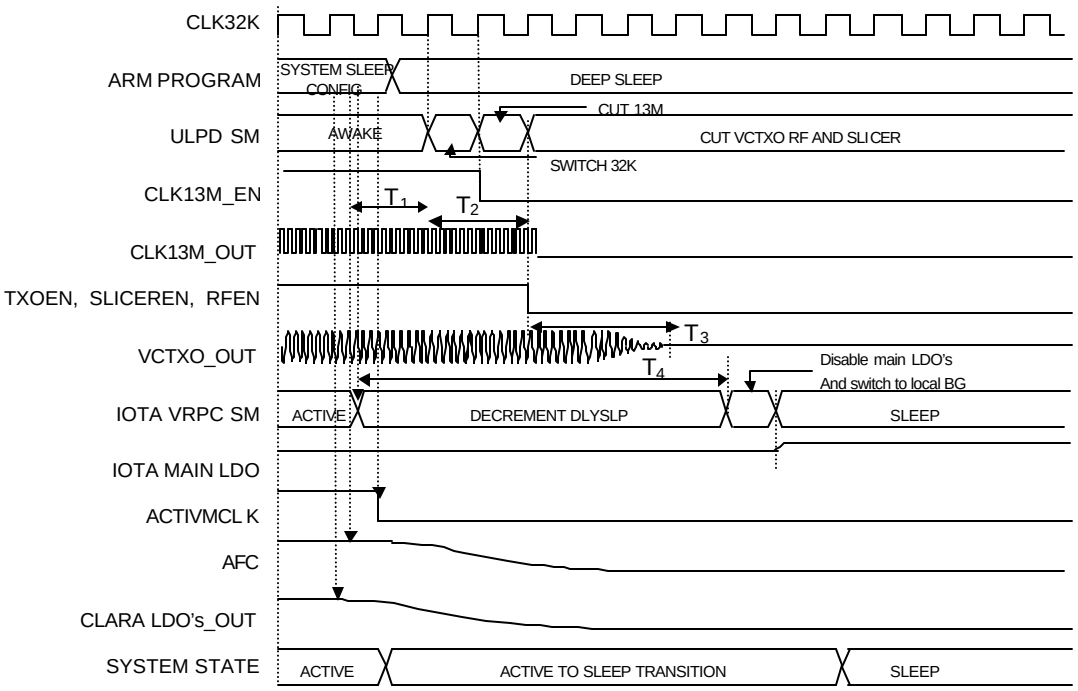


Fig 5.1 SLEEP ON transition

Table 5-1 SLEEP ON timing description

	Min	Typ	Max	Units	Description
T_1		SW +1		T_{32k}	Time from AFC disable to ULPD switch on 32KHz (1)
T_2		3		T_{32k}	ULPD SM execution time (switch32k,cut 13M, cut RF..)
T_3		TBD		T_{32k}	VCTXO disable time (2)
T_4	12		508	T_{32k}	DLYSLP counter delay (3)

(1) This time interval is SW dependent. Application SW must take care of shortening as much as possible this timing in order to minimize GSM time synchronization error. AFC control of 13MHz is no longer present but the 13 MHz clock is still used as reference for the GSM time.
(2) This time interval depends on VCTXO type.
(3) This delay must be greater than the sum $T_1+T_2+T_3$. This to ensure proper power supply during transition phase. Iota LDO's switch to SLEEP mode has to be executed only when the whole system is in a low current consumption state. This delay is variable, given by the formula [SLPDLY(4..0)*16+12]*TCk32K.

6 SLEEP OFF

SLEEP OFF transition leading to the ACTIVE state is generated either by an ITWAKEUP signal going from the DBB to the ABB or by one of the switch on conditions described for the SWITCH ON transition.

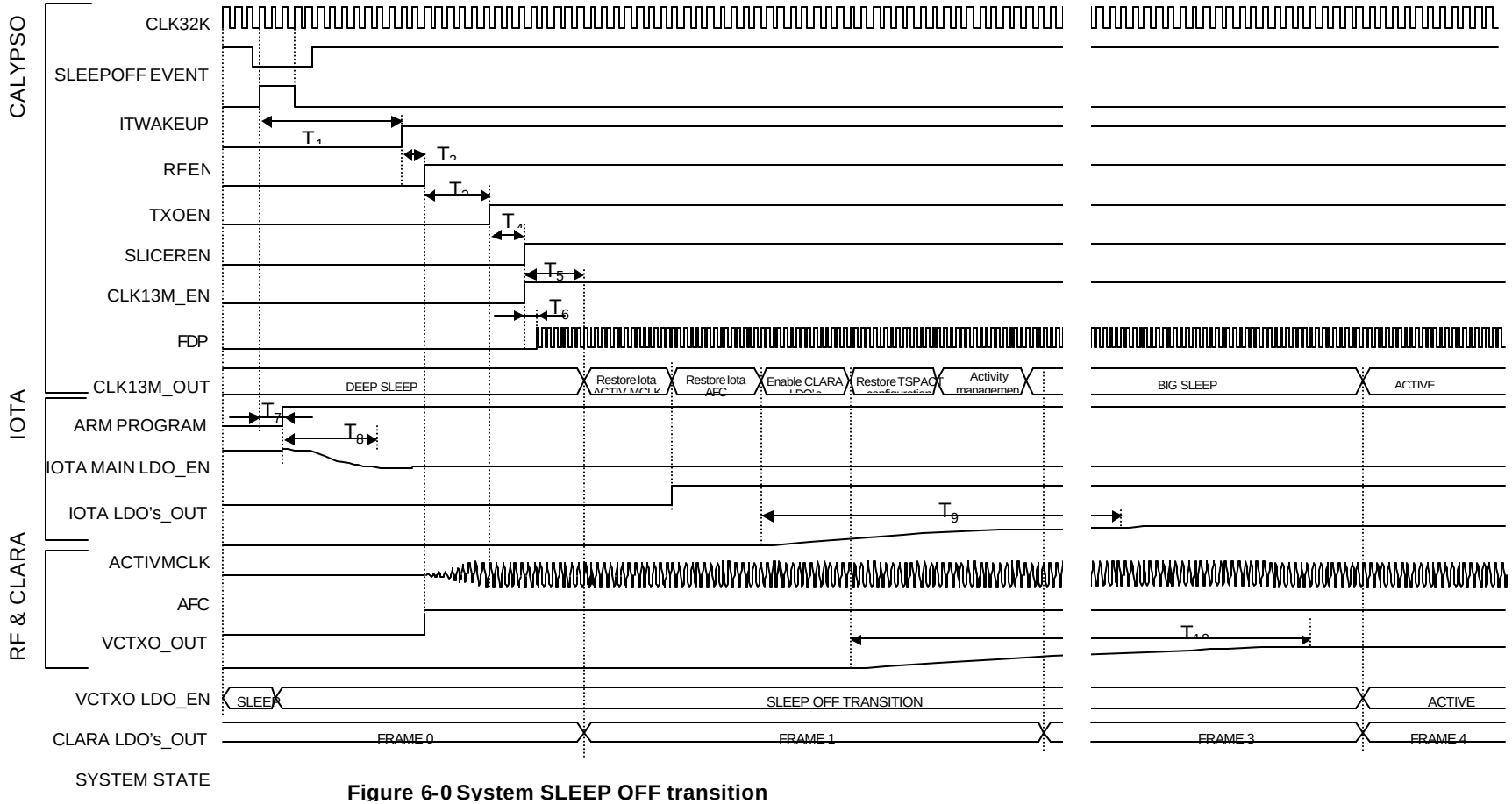


Figure 6-0 System SLEEP OFF transition

Table 6-1SLEEP OFF Timing descriptions

	Min	Typ	Max	Units	Description
T_1	1	1000	4096	T_{32k}	Setup RF time
T_2	1	31	4096	T_{32k}	Setup VCTXO time
T_3	1	490	4096	T_{32k}	Setup SLICER time
T_4	1	31	64	T_{32k}	Setup CLOCK_13 MHz time
T_5		20		T_{TCXO}	Time from FDP high to MCU code execution
T_6		3		T_{TCXO}	Time from FDP high to 13MHz available to MCU
T_7		2		T_{32k}	Time from ITWAKEUP detection and Iota LDO enable
T_8		151		T_{32k}	Iota main LDO turn on time from SLEEP mode
T_9	5 ms		15	ms	AFC setup time
T_{10}		10 [1]	55[2]	ms	CLARA LDO turn on time

The only timing constraint from system point of view is that T_8 Iota LDO's turn on time from SLEEP mode needs to be shorter than T_1+T_2. Is after that time interval, at VCTXO enable, that the system starts to sink more than the SLEEP current from Iota LDO's. Thus, at that time, they have to be already able to support ACTIVE mode current.

[1] Typical value with speed-up enable
[2] Max value with speed-up disabled