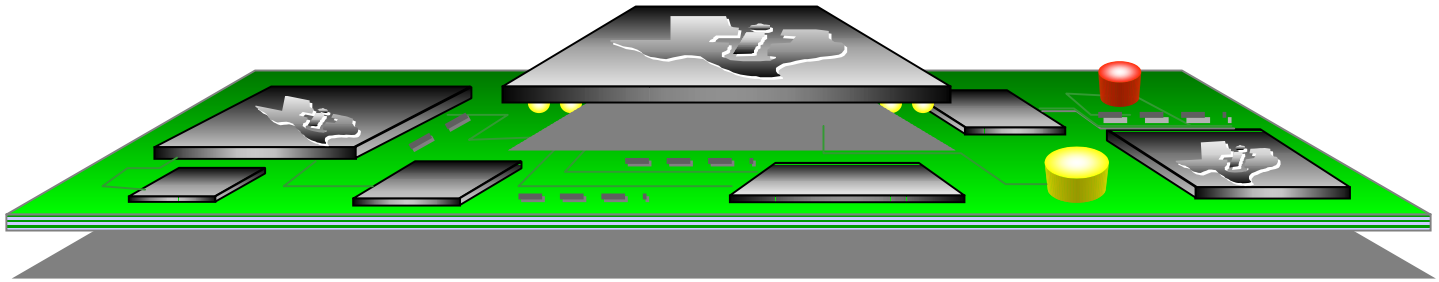
GSM/GPRS Chipset

Iota – Analog Baseband

Seminar



2002/04/04

Eric Song, Texas Instruments China

TI ABB Roadmap Summary

Baseband CODEC
Voiceband CODEC
RF Control
Voltage regulation
Battery charger interface
Power Management
Auxiliary ADC
Serial interfaces
SIM Card interface

In production

NEW FEATURES:

DBB split power compatibility
Consumption reduction in sleep and Back-up mode Direct Conversion compatibility
Headset audio interface
LED drivers

A12 In production

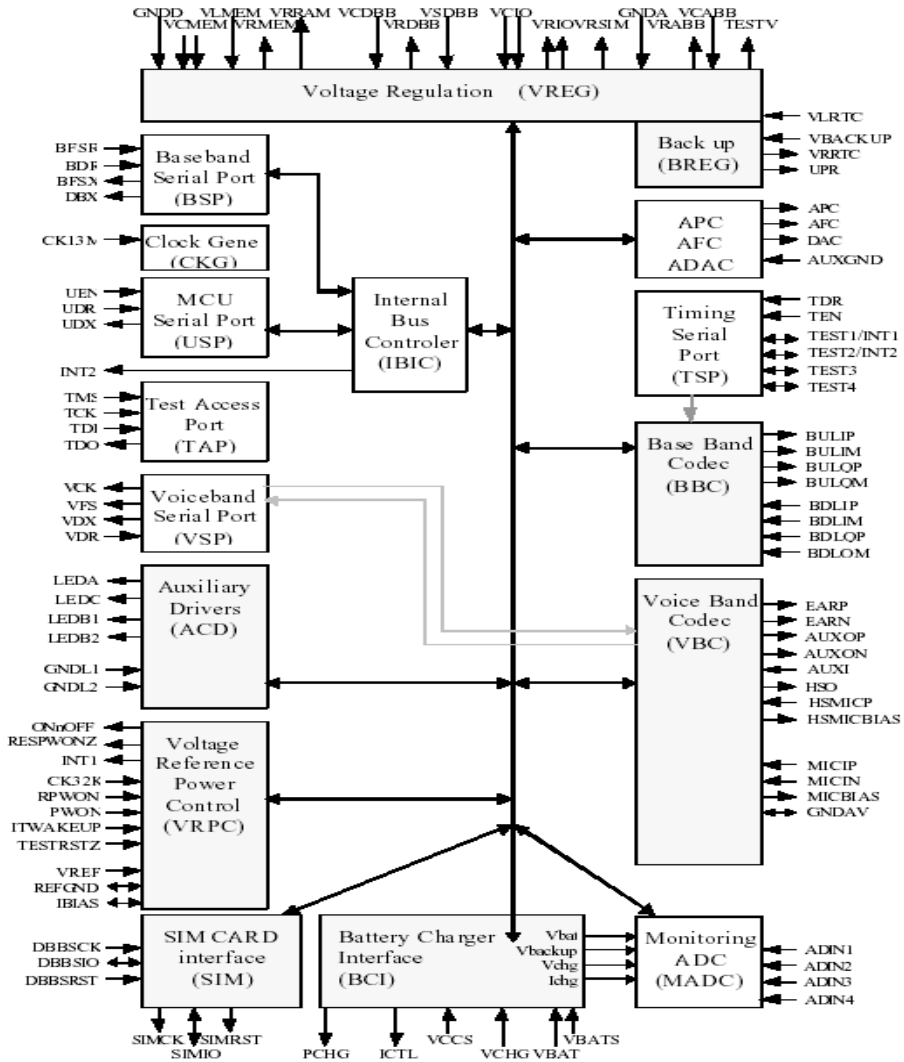
NEW FEATURES:

EDGE modulator and PWM
HIFI Stereo Audio DAC
Handsfree amplifier 8 Ohm
Charger interface 20V capability

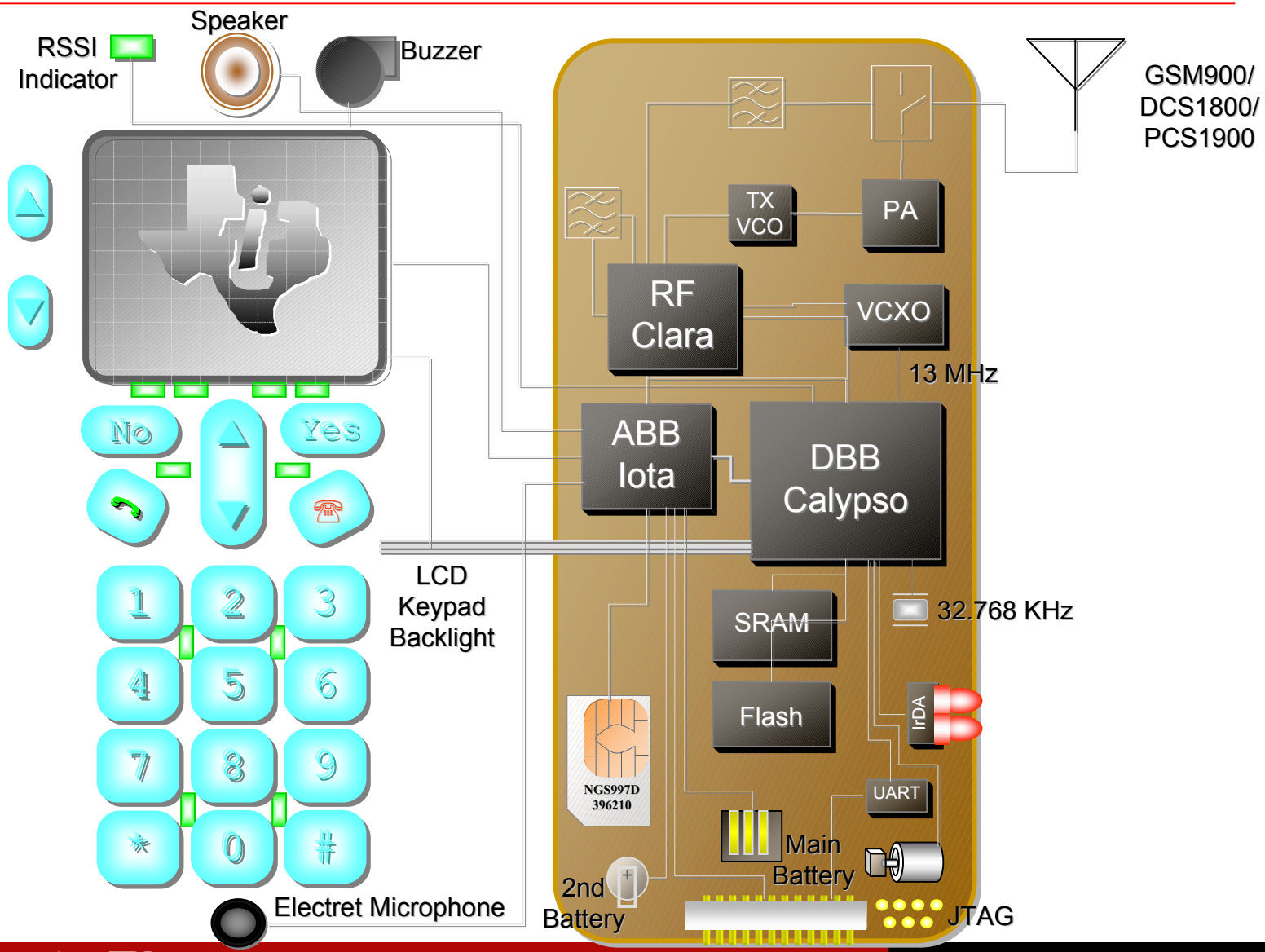
Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Ports
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

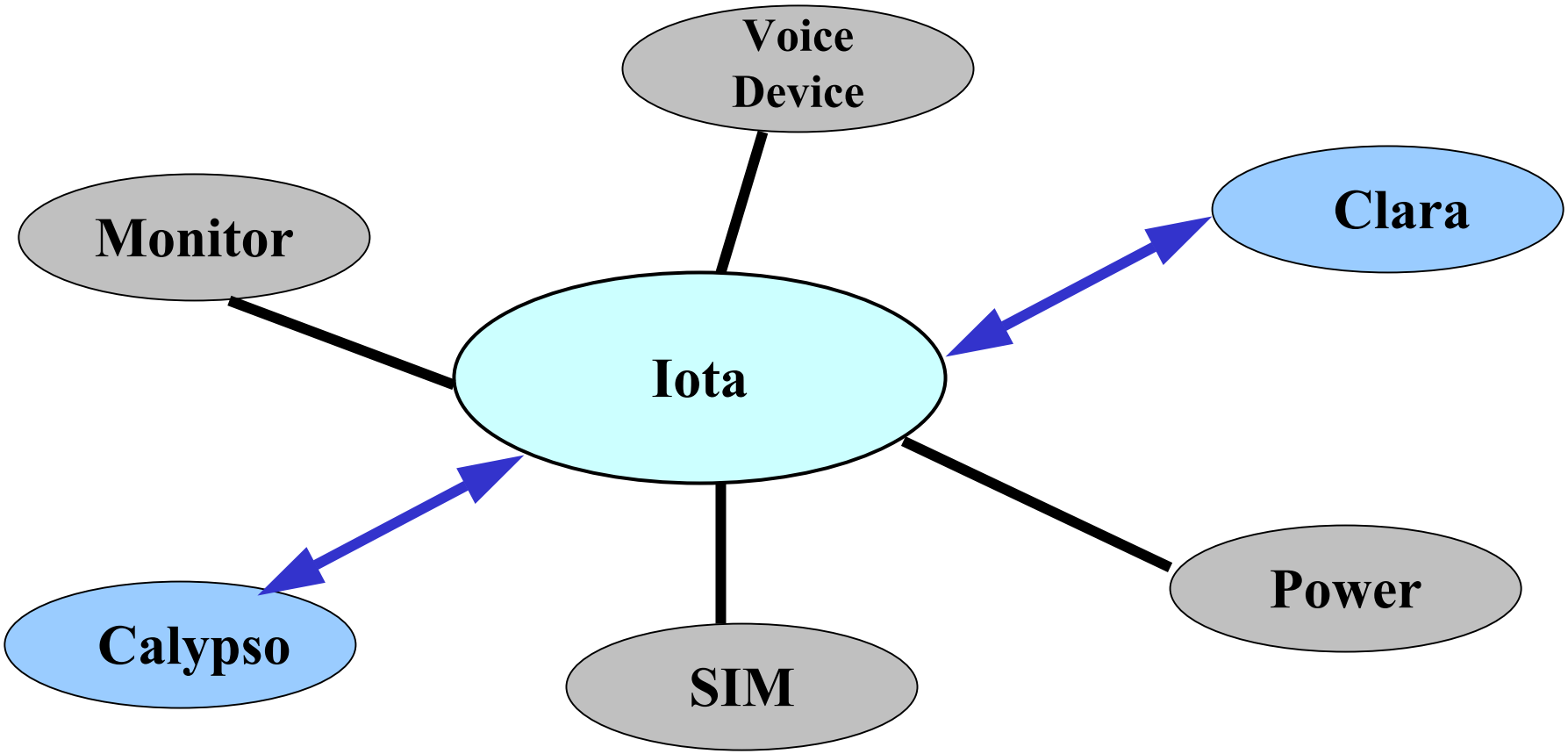
Iota Blocks diagram



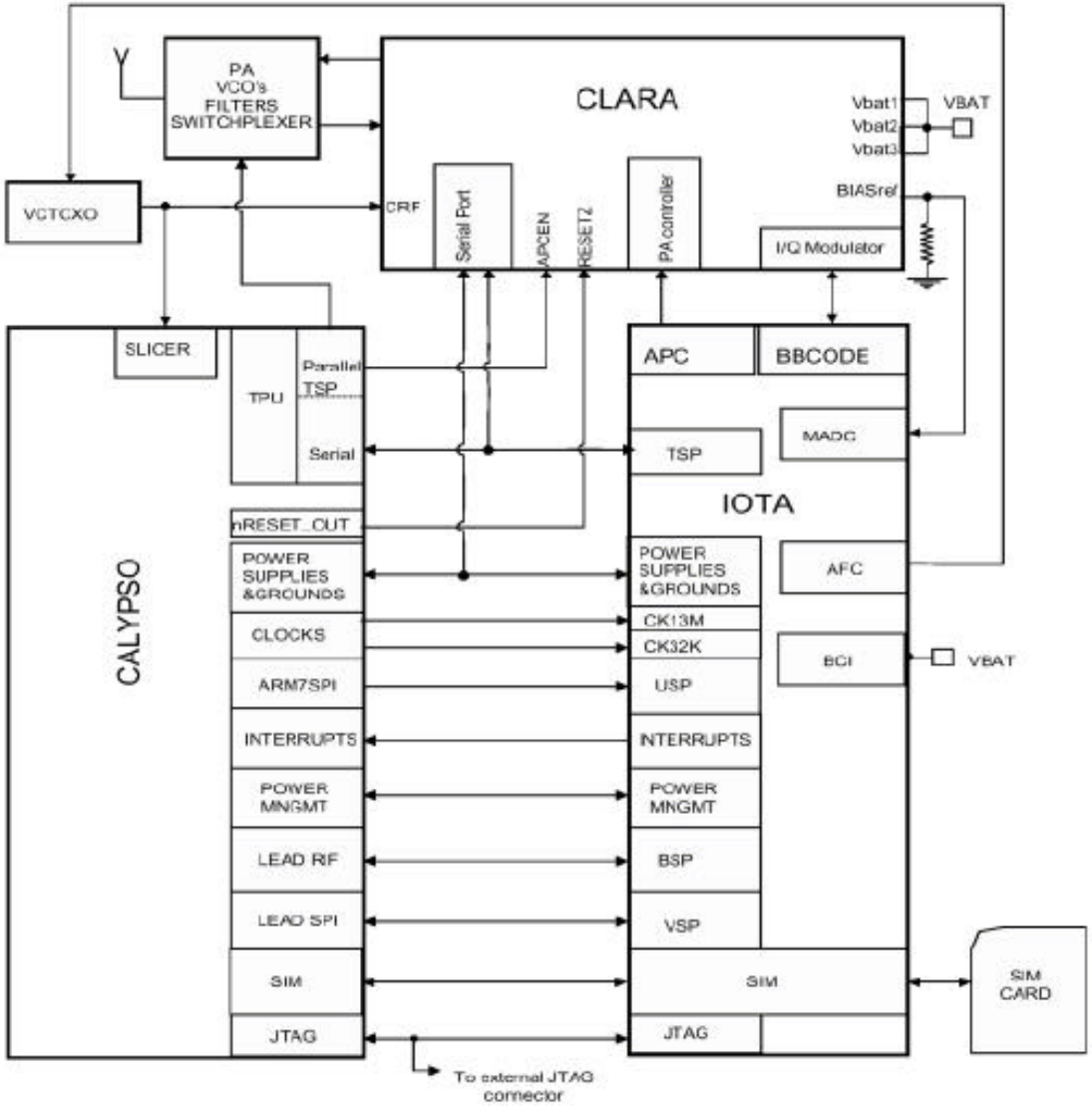
GSM/GPRS Application Diagram



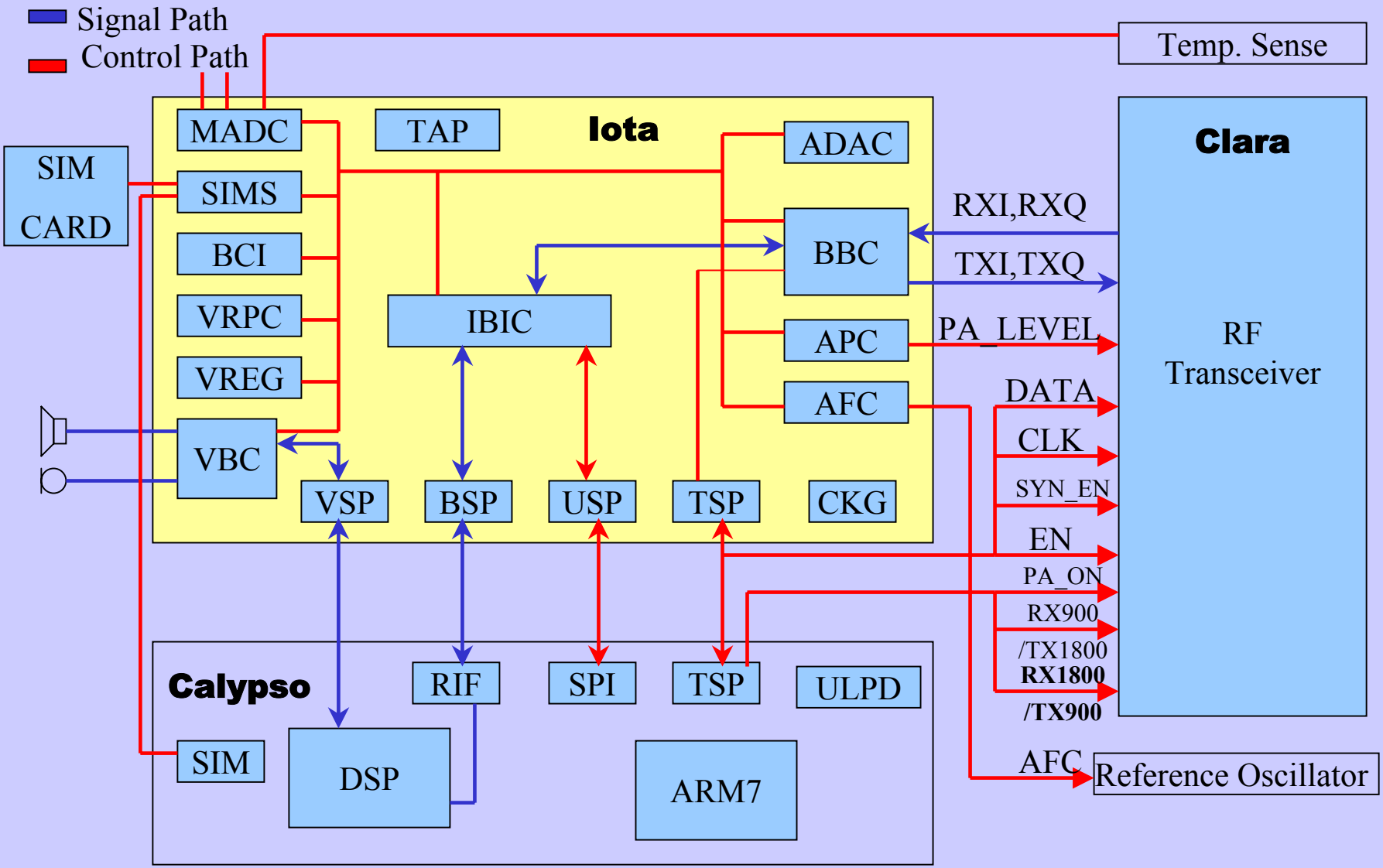
Iota's Function Block



System connections



Signal/Control Flow of Iota



Internal Registers Operations

Each word is split in three fields.

Data										Address					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	1 / 0

Writing to internal registers :

Bit 0 : At 0 (zero) it indicates a write operation.
Bit 1 to 5 : This field shall contain the address of the register to be accessed.
Bit 6 to 15 : This field shall contain the data to be written into the internal register.

Reading from internal registers :

Bit 0 : At 1 (one) it indicates a read operation.
Bit 1 to 5 : This field shall contain the address of the register to be accessed.
Bit 6 to 15 : This filed don't care in a read request operation.

Baseband Burst Operations

Transfer of radio data via BSP in 16 bit word format:

Data															I /Q
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Address format:

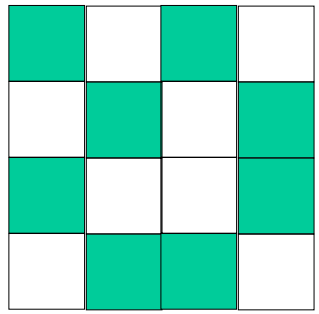
Address : 7 Page 0				
0	0	1	1	1

Address : 7 Page : 1				
0	0	1	1	1

Register Page Setup

Name : PAGEREG					Description : Page Select Register					Address : 1	Pages : 0 & 1				R/W
RESERV	RESERV	RESERV	RESERV	RESERV	RESERV	BSPP1	BSPP0	UCP1	UCP0	0	0	0	0	1	0
						W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

- UCP0: Set Address Page 0 for USP Access
- UCP1: Set Address Page 1 for USP Access
- BSPP0: Set Address Page 0 for BSP Access
- BSPP1: Set Address Page 1 for BSP Access



Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Port
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

Iota RF Control

- Automatic Power Control

- Automatic Frequency Control

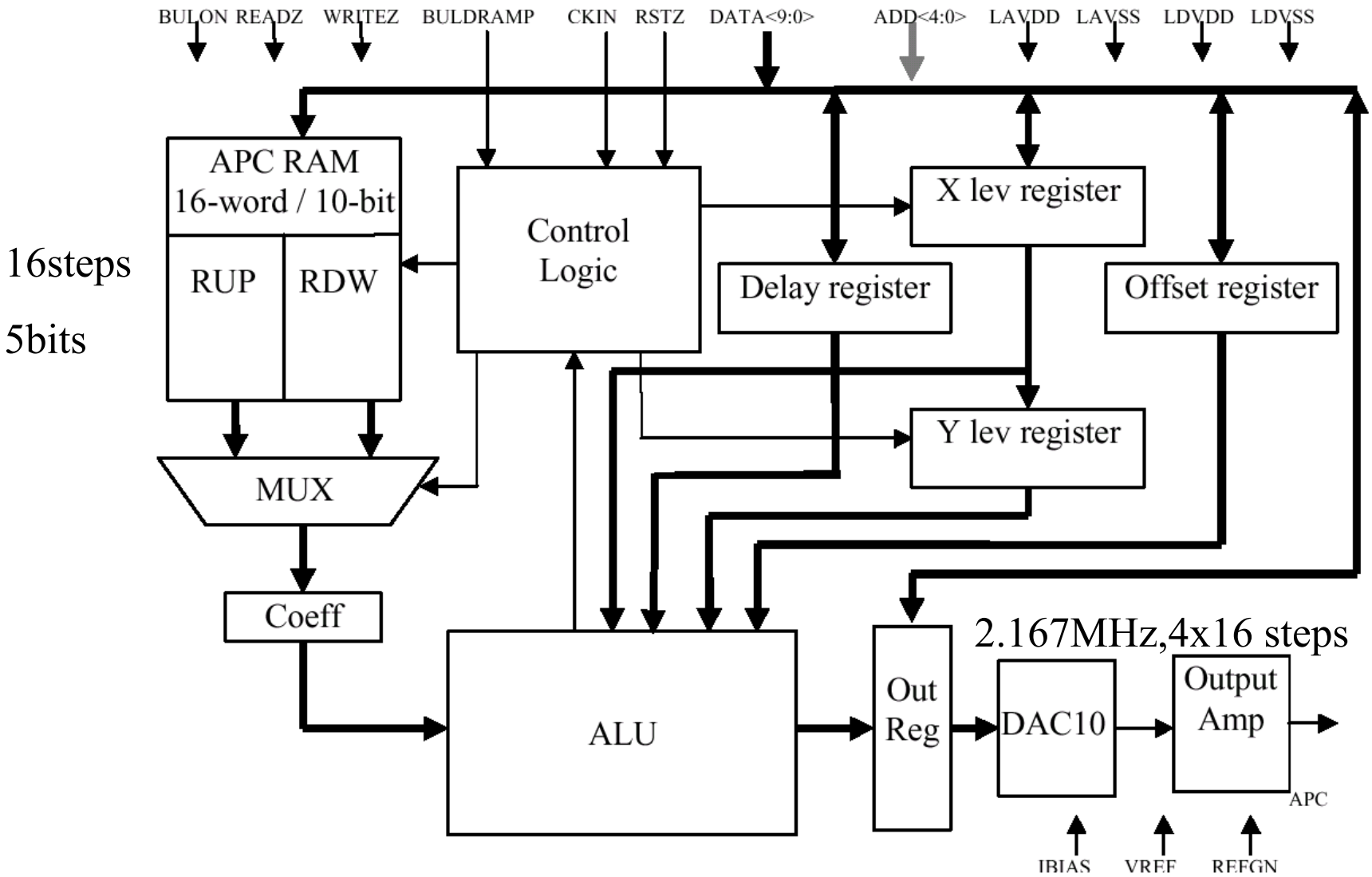
APC Functions

- Control the power ramping up
- Control the power ramping down
- Control the power level of the radio burst

Supporting:

single slot and mutislots transmission

APC Block Diagram



Sequence of Input to the DAC10

$$level = level_{init} + \sum_{i=0}^{15} \left(\frac{step_{lev}}{256} \times (up[i] \times (1 - sign_{step}) + dw[i] \times sign_{step}) \right)$$

$$= level_{init} + step_{lev} \times \sum_{i=0}^{15} \left(\frac{up[i]}{256} - \frac{dw[i]}{256} \right)$$

Where,

level is the new power level.

$level_{init}$ is the current power level.

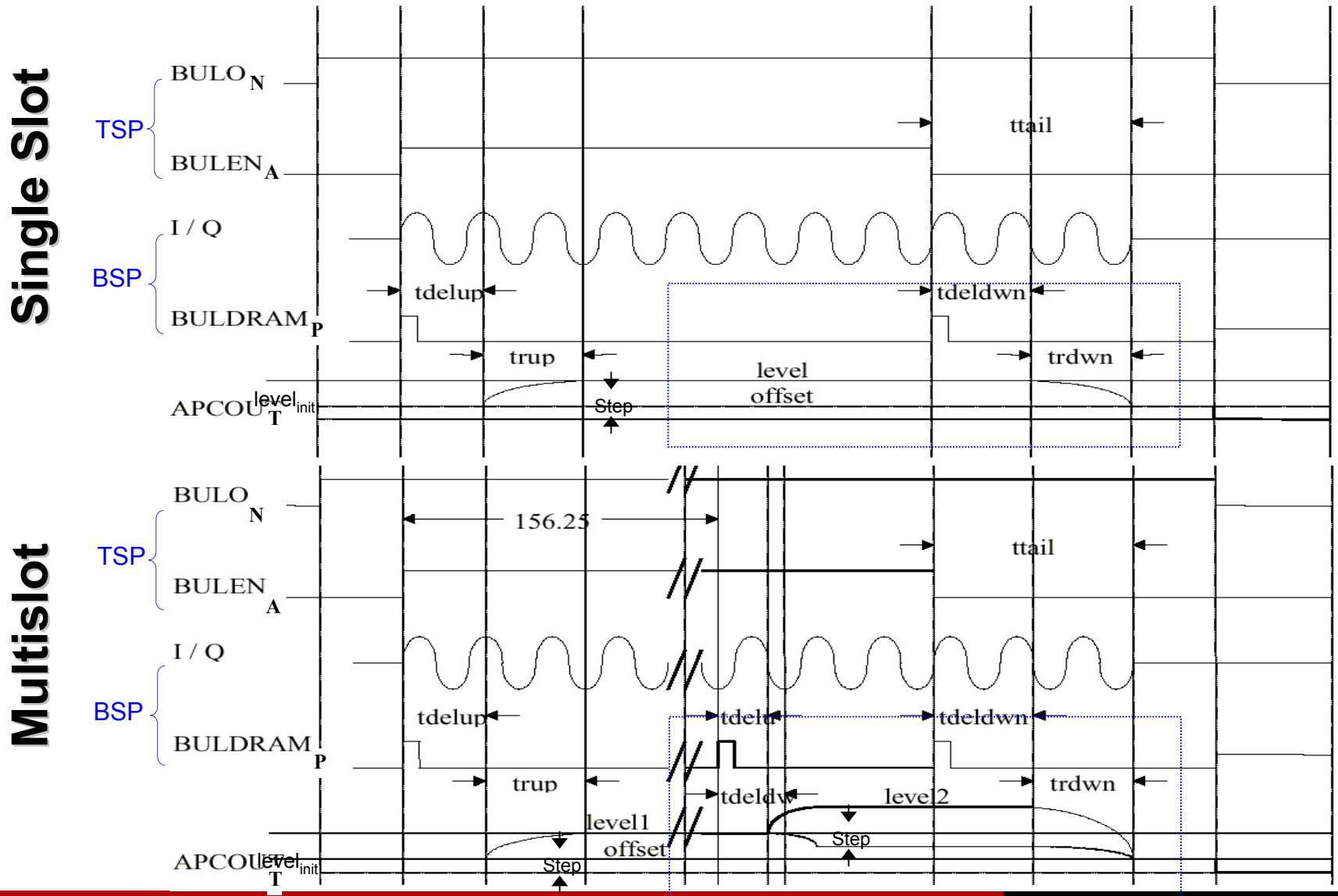
$step_{lev}$ is the power level step to be done.

up[i] are the coefficients of the ramp-up shaping filter.

dw[i] are the coefficients of the ramp-down shaping filter.

$sign_{ste}$ is the sign of $step_{lev}$
(0 for plus, 1 for minus).

APC Timing


Single Slot
TSP
BULON
BULENA
BSP
I / Q
BULDRAMP
APCOUT
tdelup
trup
level
offset
Step
levelinit
ttail
tdeldwn
trdwn
Multislot
156.25
tdelup
trup
tdeldw
level1
level2
offset
Step
ttail
tdeldwn
trdwn

Iota RF Control

- Automatic Power Control
- Automatic Frequency Control

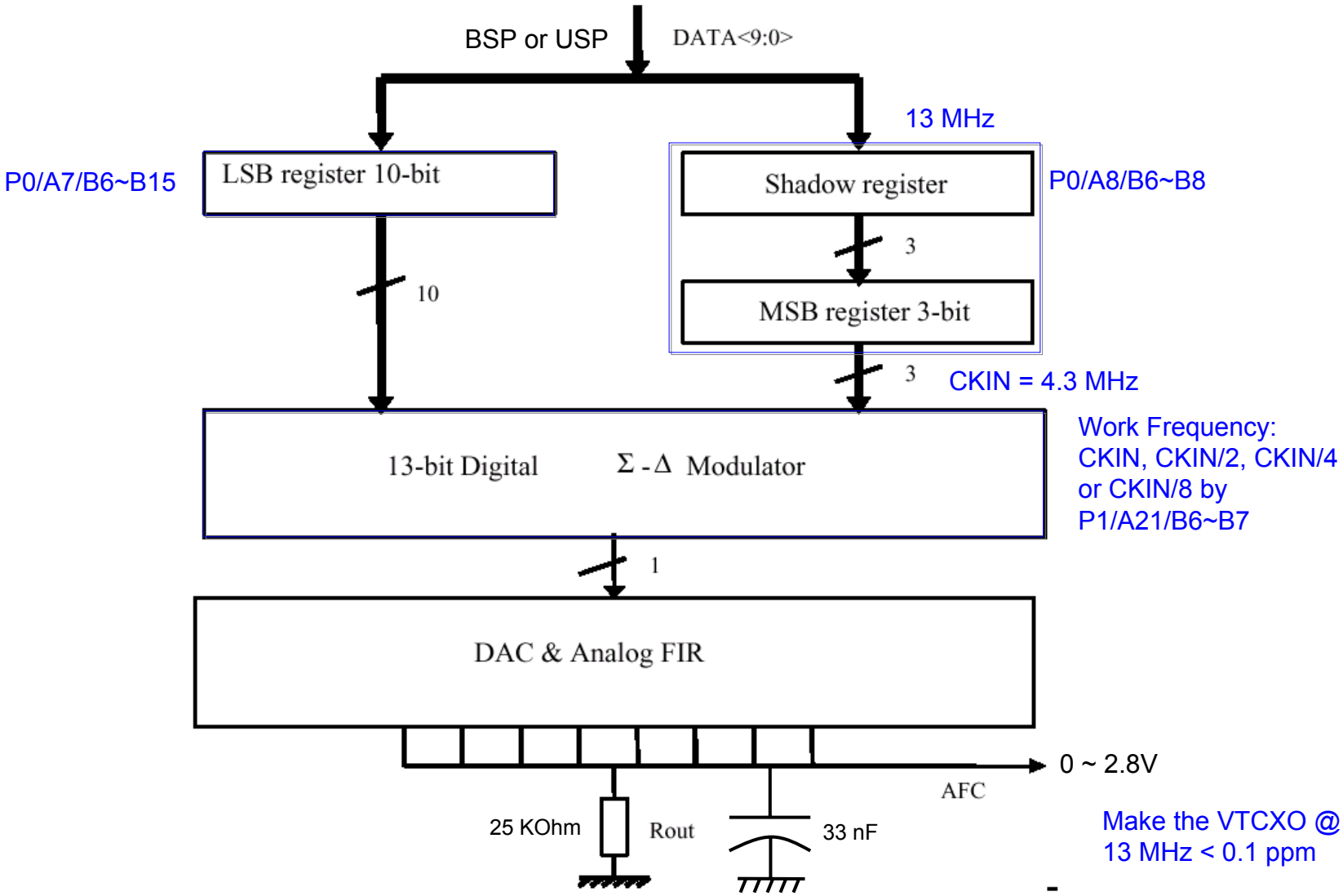
AFC Purpose

Correct frequency shifts of the voltage controlled oscillator to maintain the GSM 13 MHz master clock frequency in a 0.1ppm range.

The AFC signal is fed through a 13-bit AFC DAC for a Resulting range of:

$$-4096 < \text{AFC DAC value} < 4095$$

AFC Block Diagram



Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Port
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

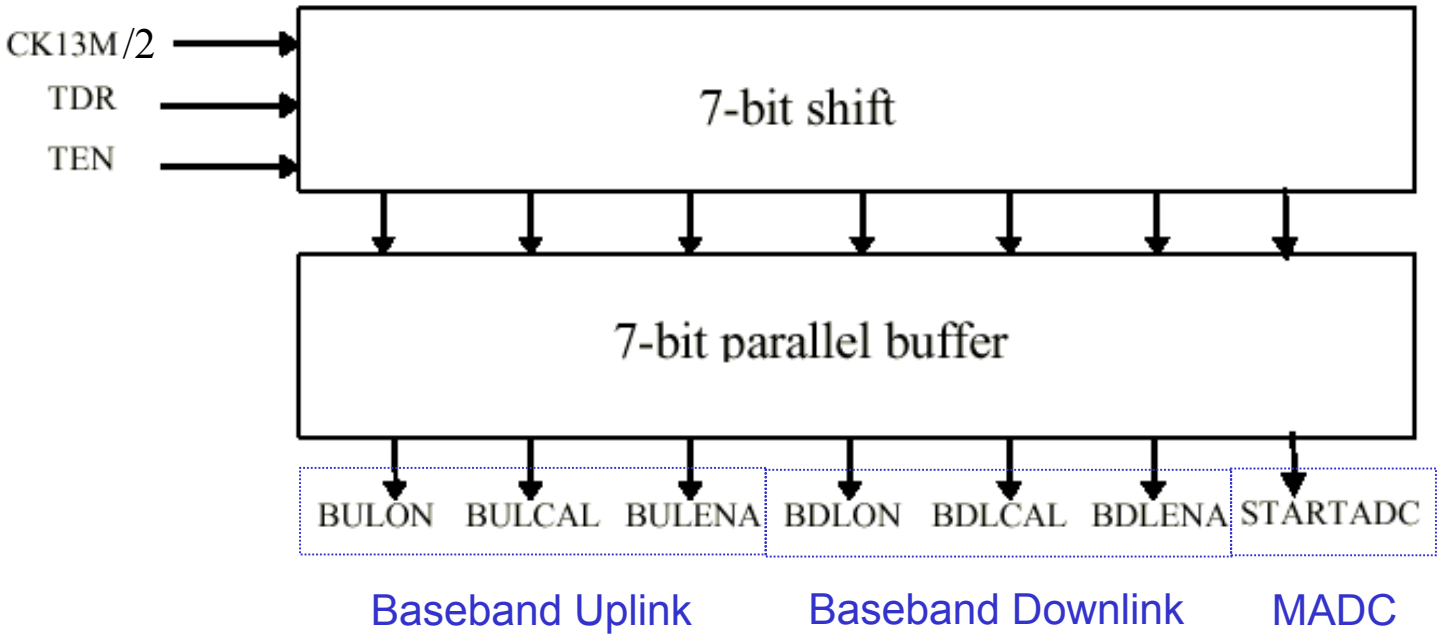
Iota Serial Port

- Timing Serial Port
- Micro-control Serial Port
- Voiceband Serial Port
- Baseband Serial Port

TSP Purpose

Control the real time GSM windows for the baseband codec and the window for ADC conversion.

Iota TSP Block Diagram

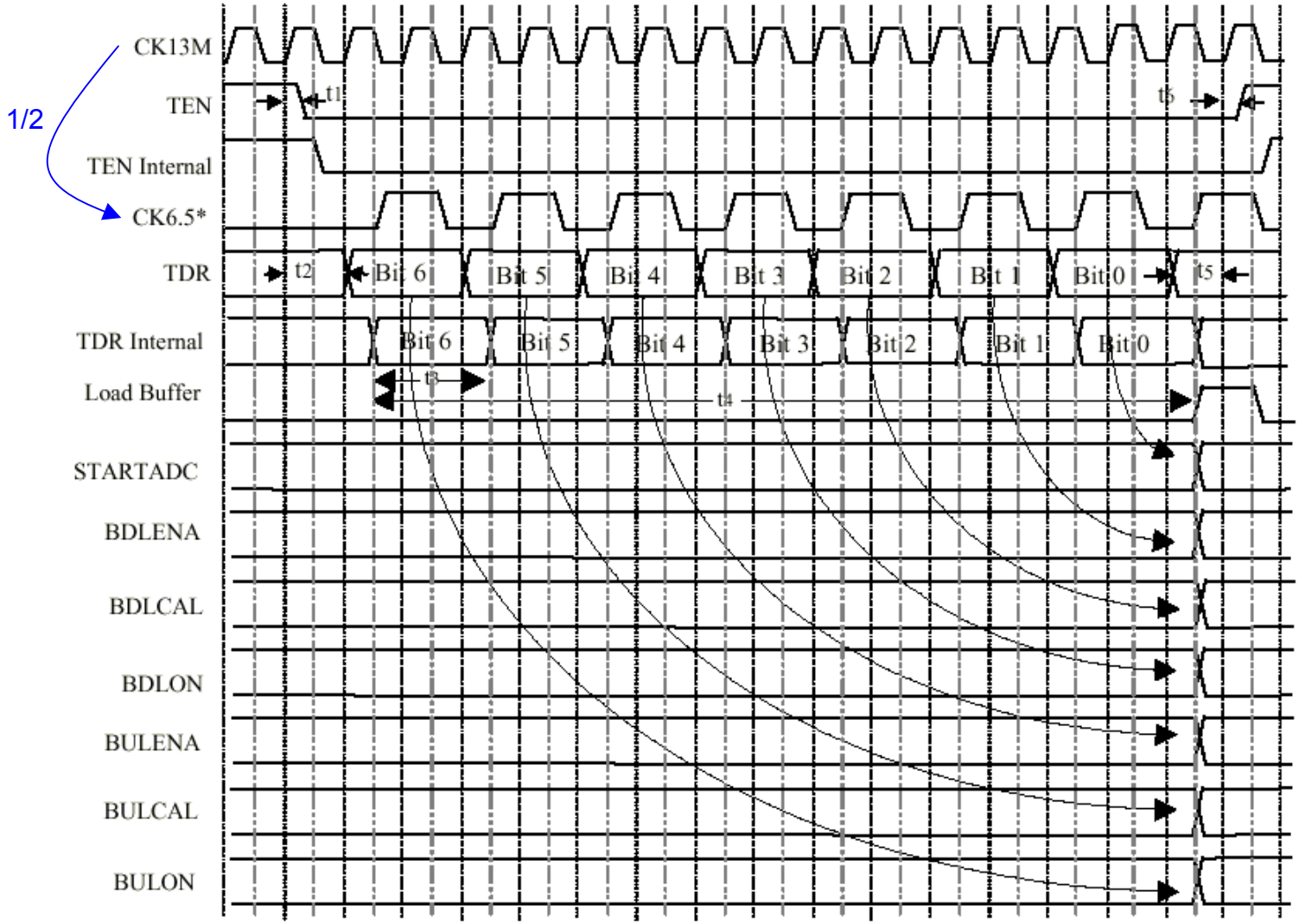


Register Definition

The bits are defined as follow ;

Bit 6 : BULON : Power-on window of the baseband uplink
Bit 5 : BULCAL : Offset calibration window of the baseband uplink.
Bit 4 : BULENA : Transmission window of the basband uplink
Bit 3 : BDLON : Power-on window of the baseband downlink
Bit 2 : BDLCAL : Offset calibration window of the baseband downlink
Bit 1 : BDLENA : Transmission window of the basband downlink
Bit 0 : STARTADC : Window for ADC conversion control

Iota TSP Timing Diagram



Iota Serial Port

- Timing Serial Port
- Baseband Serial Port
- Micro-control Serial Port

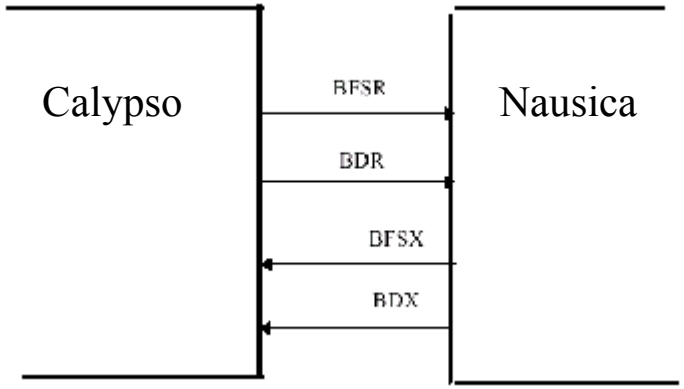
BSP Functions

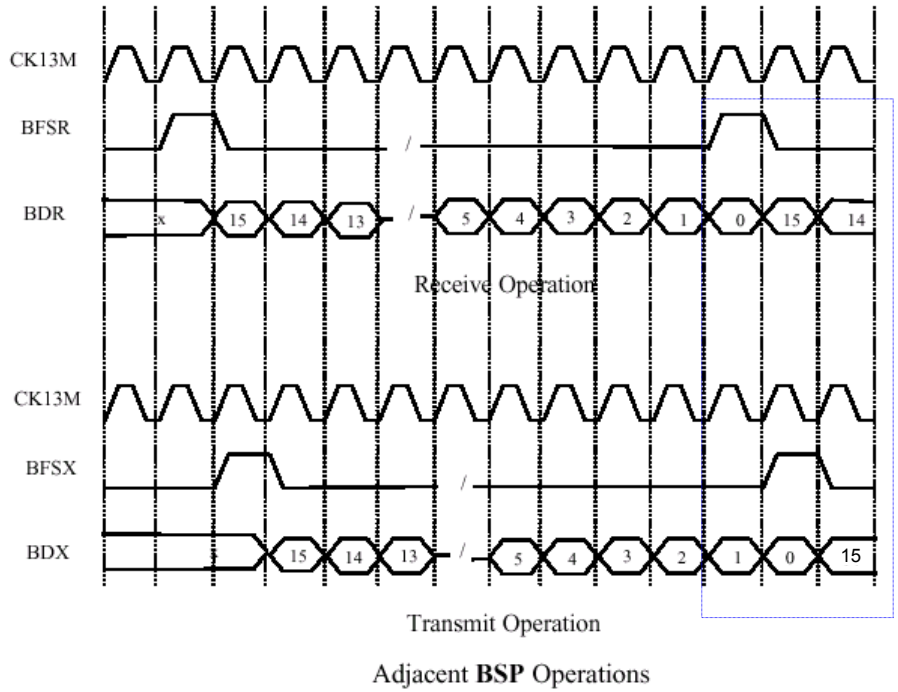
1.Transfer of baseband transmit and receive data

2.Access all internal programmation registers of the device.

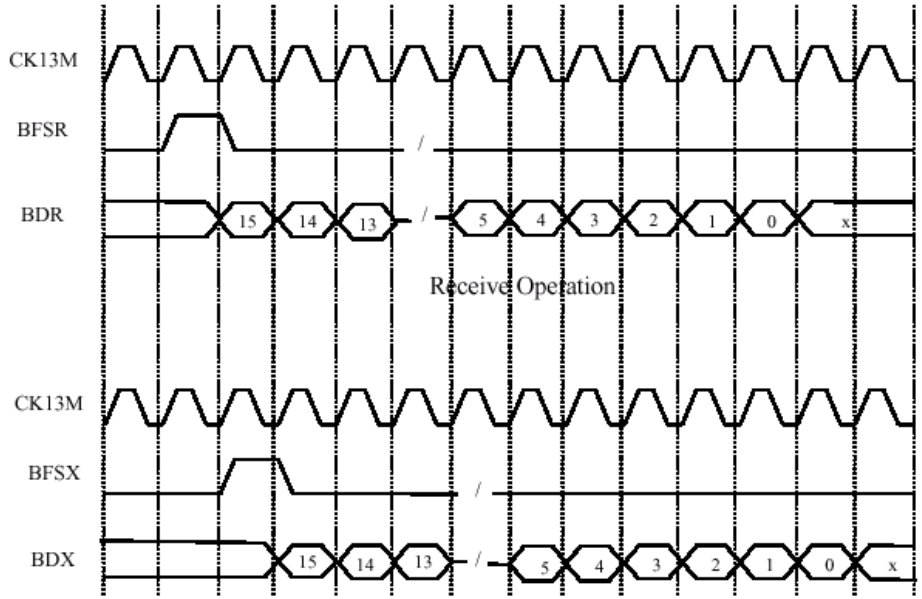
The word format of the serial interface is 16 bits.

Baseband Serial Port





Adjacent **BSP** Operations



Single **BSP** Operations

In the adjacent operations mode the first transmission is same as in the single operation mode. But for the following words the synchronization pulse is synchronized with the last bit (the LSB or bit0) from the previous word.

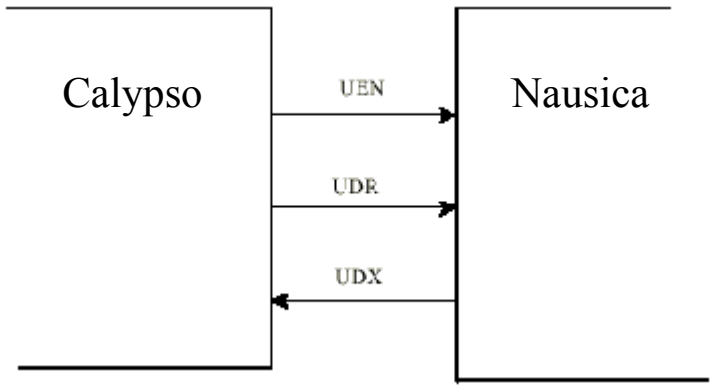
Iota Serial Port

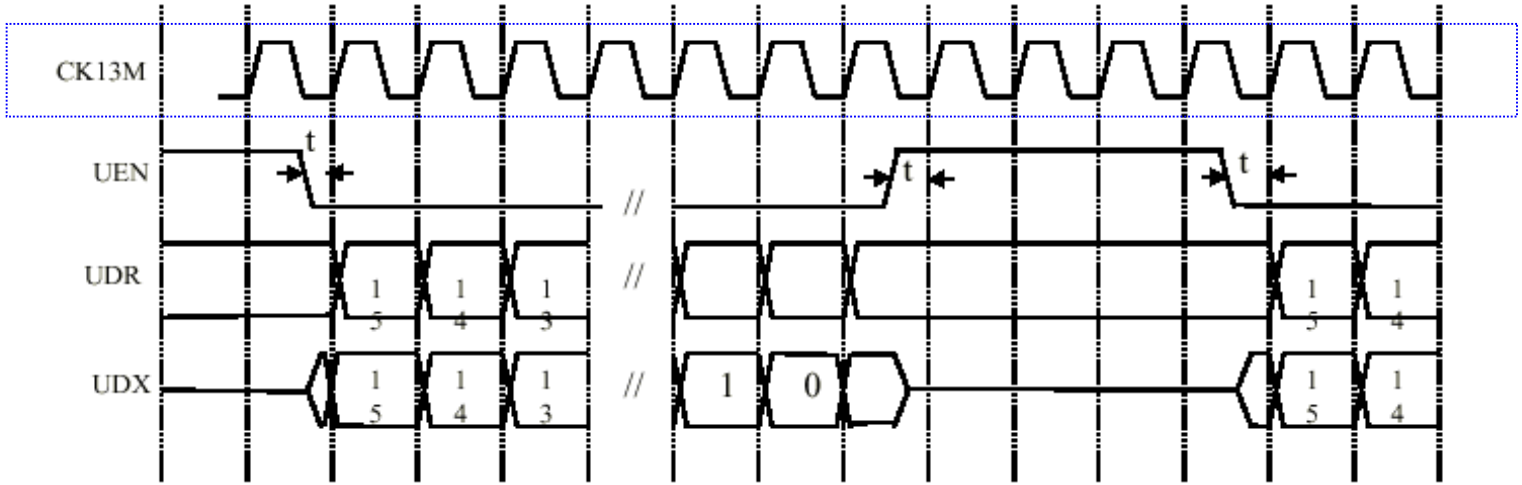
- Timing Serial Port
- Baseband Serial Port
- Micro-control Serial Port

USP Function

Allows a micro-controller to access to all the internal registers.

USP Operations





Receive and Transmit **USP** Operations

USP Data Format

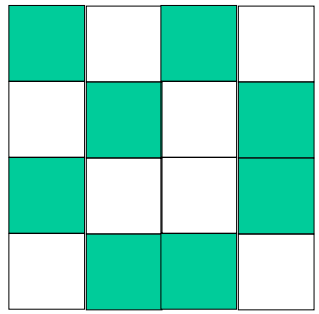
Data										Address					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	1 / 0

- Writing to Internal Registers :
  - Bit 0: At zero it indicates a write operation.
  - Bit 1 to 5: This field shall contain the address of the register to be accessed.
  - Bit 6 to 15: This field shall contain the data to be written into the internal register.
- Reading from Internal Registers :
  - Bit 0: At one it indicates a read operation.
  - Bit 1 to 5: This field shall contain the address of the register to be accessed.
  - Bit 6 to 15: This filed don' t care in a read request operation.

Register Page Setup

Name : PAGEREG						Description : Page Select Register				Address : 1					R/W
RESERV	RESERV	RESERV	RESERV	RESERV	RESERV	BSPP1	BSPP0	UCP1	UCP0	0	0	0	0	1	0
						W	W	W	W	<--- ACCESS TYPE					
0	0	0	0	0	0	0	0	0	0	<--- VALUE AT RESET					

- UCP0: Set Address Page 0 for USP Access
- UCP1: Set Address Page 1 for USP Access
- BSPP0: Set Address Page 0 for BSP Access
- BSPP1: Set Address Page 1 for BSP Access



Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Port
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

Iota Power Management

- Voltage Regulation
- Battery Charger Interface
- Voltage Reference Power-on Control
- SIM Card Regulator&Shifters

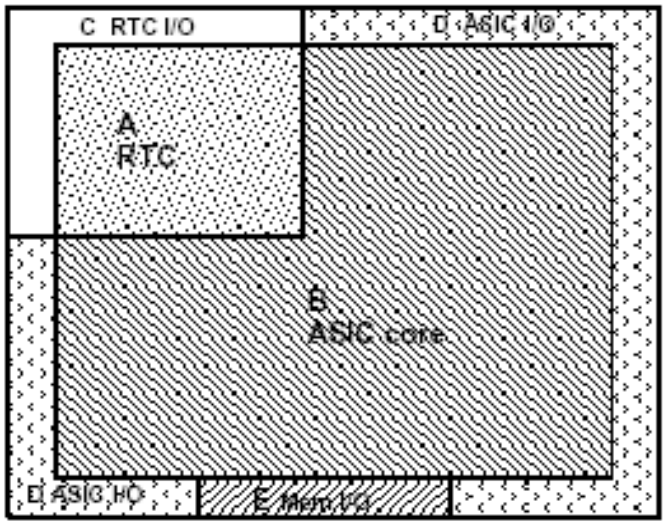
ABB to DBB Power Connections 1/2

- IOTA is not compatible with non split DBB
- LDO's are supplied directly on the main Battery
- RRTC is dedicated to the DBB split domain and it is always active
- DBB core and split part supply voltage are selectable through external pin
- RDBB supply has an external sense pin for sharper regulation
- RMEM is protected against reverse current when off.
- RABB LDO is not supporting SLEEP mode

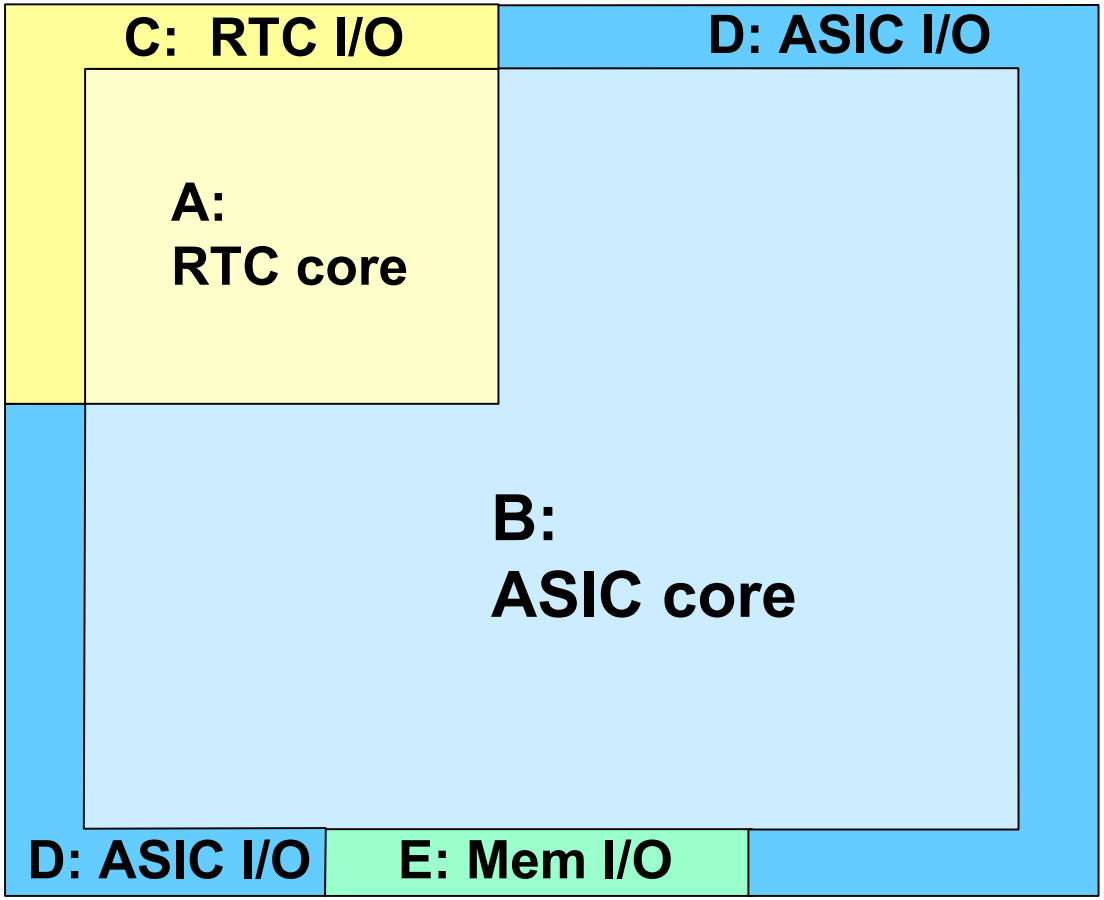
Calypso Supplies Voltage Rules

The Calypso device has five different Power domains corresponding to the following IOTA supplies:

A : RTC core domain	=> RRTC	1.4V – 1.8V depending on VLRTC connection
B: ASIC core domain	=> RDBB	1.4V – 1.8V depending on VLMEM connection
C: RTC I/O domain	=> RRTC	1.4V – 1.8V depending on VLRTC connection
D: ASIC I/O domain	=> RIO 2.8V	
E: Memory interface	=> RMEM	1.8V – 2.8V depending on VLMEM connection



Power Domains - HercROM400G2 (Calypso)



Five Power Domains

A: RTC Core - 1.8 V
32 KHz Clock,
IT_Wakeup,
Power on Reset,
On_Off.

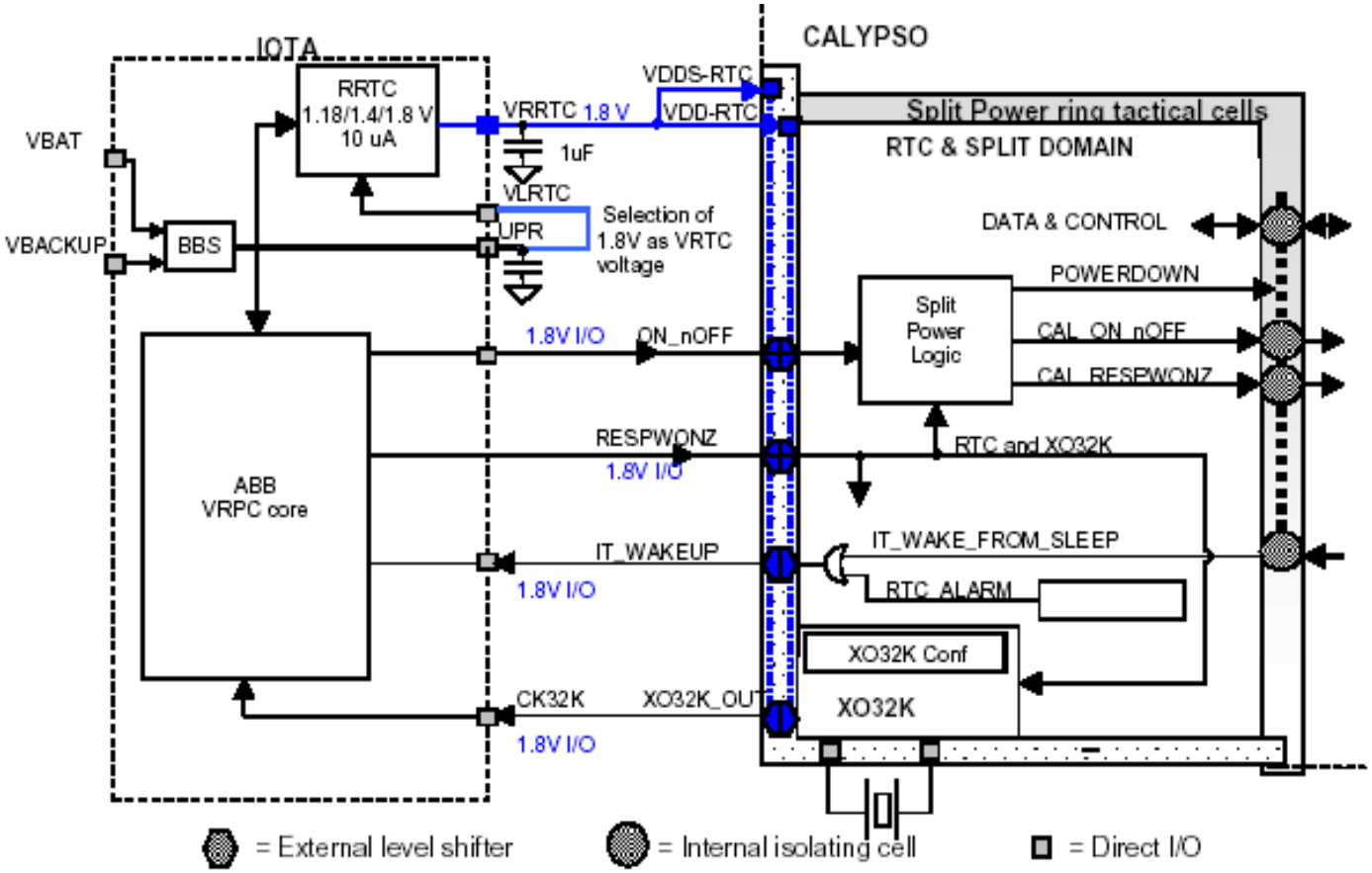
B: ASIC Core - 1.8 V
ARM, LEAD,
PLL, SRAM.

C: RTC I/O - 1.8 V

D: ASIC I/O - 2.8 V

E: Mem I/O -
1.8 or 2.8 V

Power Splite Concept



Split Power concept 2/2

- Suppression of current consumption due to internal SRAM and ASIC core.
- Isolation of split ring implemented through tactical cells driven by the ON_nOFF ABB signal.
- OR of wake up sources from SW Deep Sleep mode and RTC allows system wake up from Sleep and Off modes.
- IOTA device adopts as low frequency clock the 32Khz generated by the XO32K module.
- CALYPSO device maintains NAUSICA compatibility thanks to level shifter on power management I/O's.

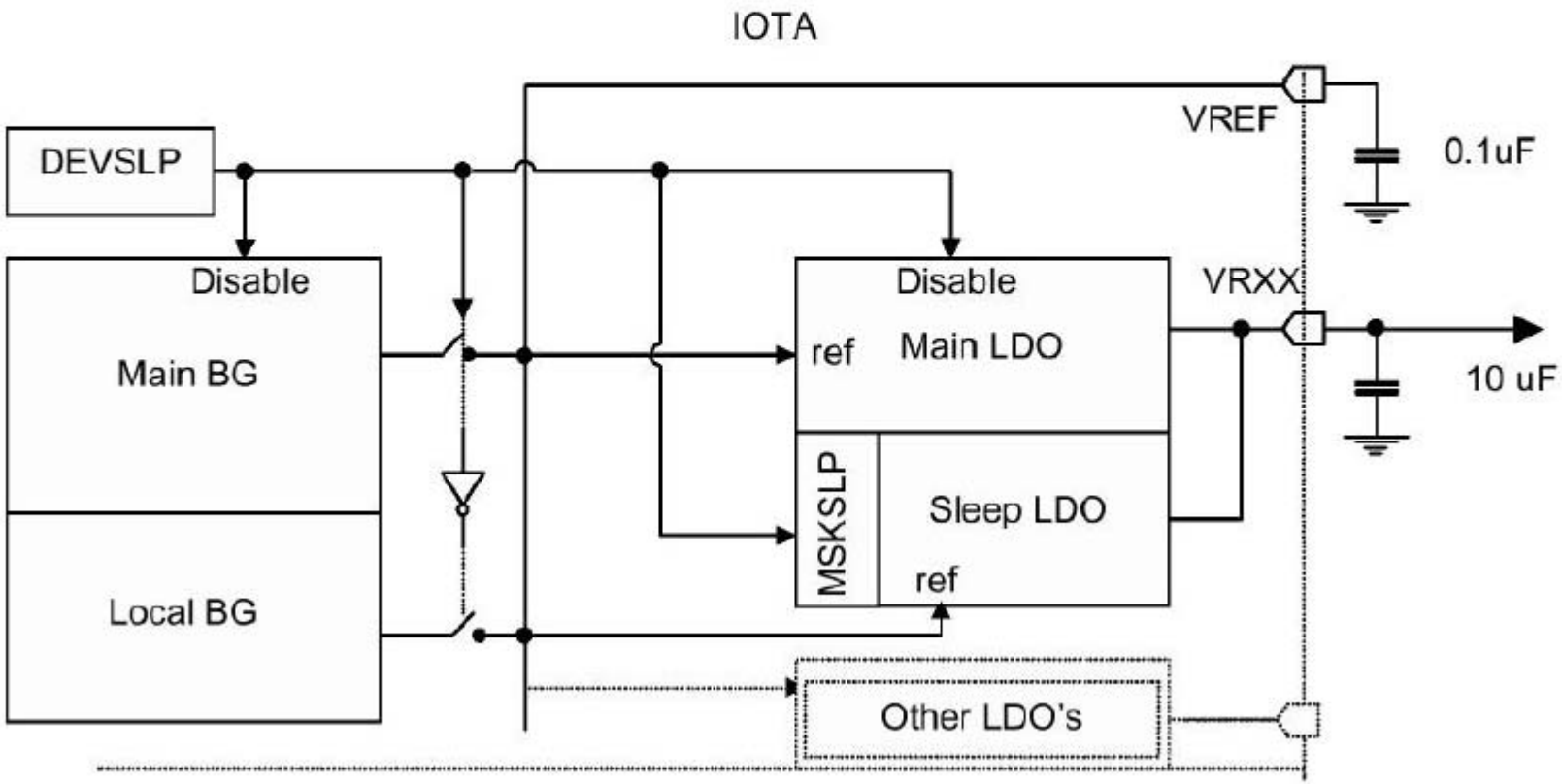
Sleep Concept 1/2

- Reduction of current consumption during mobile paging mode:
  - ✓ Charge pump removed.
  - ✓ Special low current consumption mode for LDO programmable by SW (maximum current limited to 1mA).
  - ✓ Main Band Gap current consumption reduced thanks to a local BG
  - ✓ IOTA HW Sleep mode expressly conceived to support L1 Deep Sleep SW mode

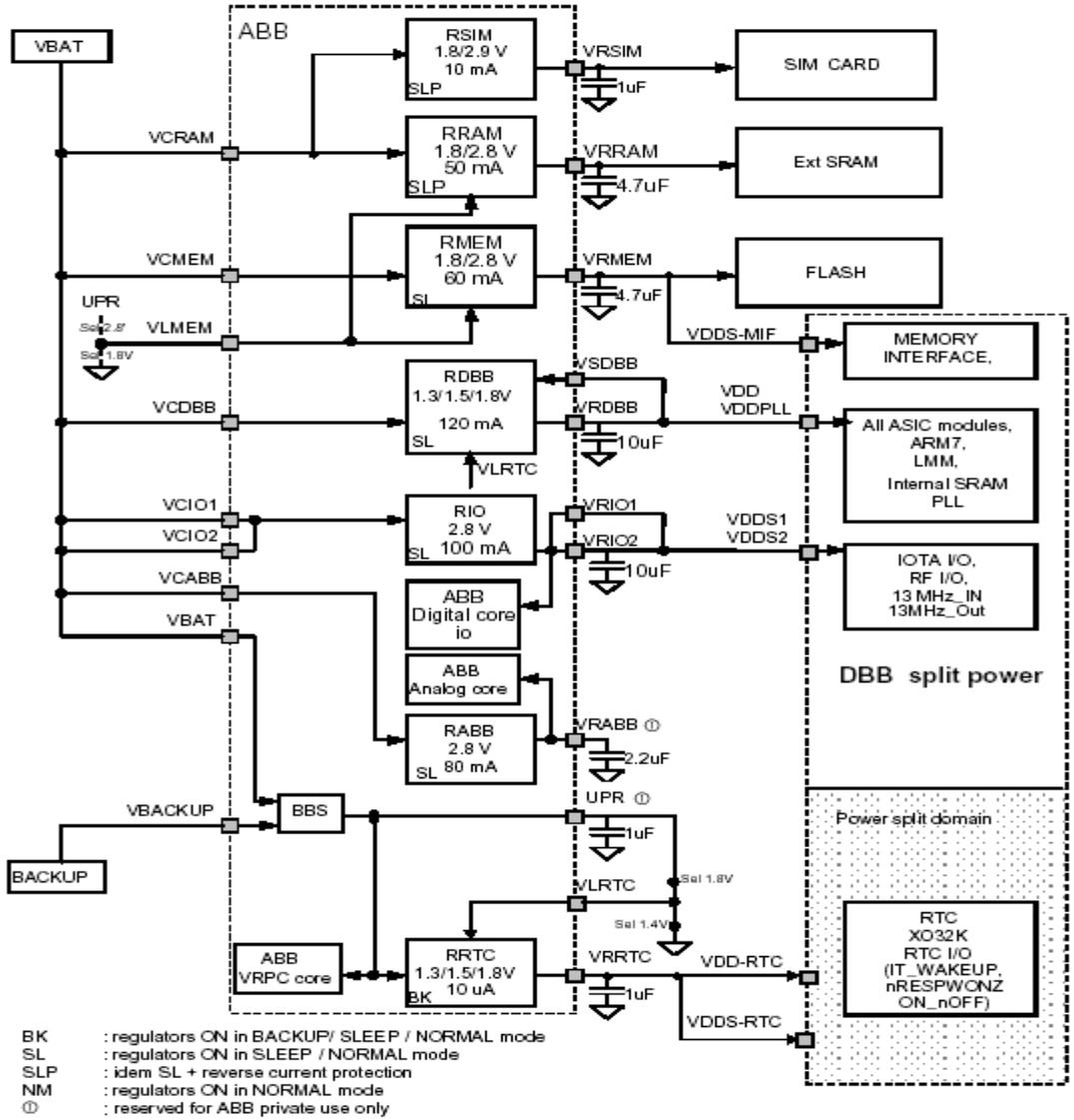
Power Saving - Principe

1) Measure exact frequency of 32 kHz oscillator by comparing with 13 MHz reference clock.
2) Calculate number of 32 kHz cycles before next frame to be received.
3) Program number of 32 kHz cycles to RTC counter.
4) Stop all CPU, DSP and other activities.
5) ……zzzzzzzzzzzzzz
6) Wake-up due to interrupt from RTC counter.
7) Receive paging.
8) GOTO 1)

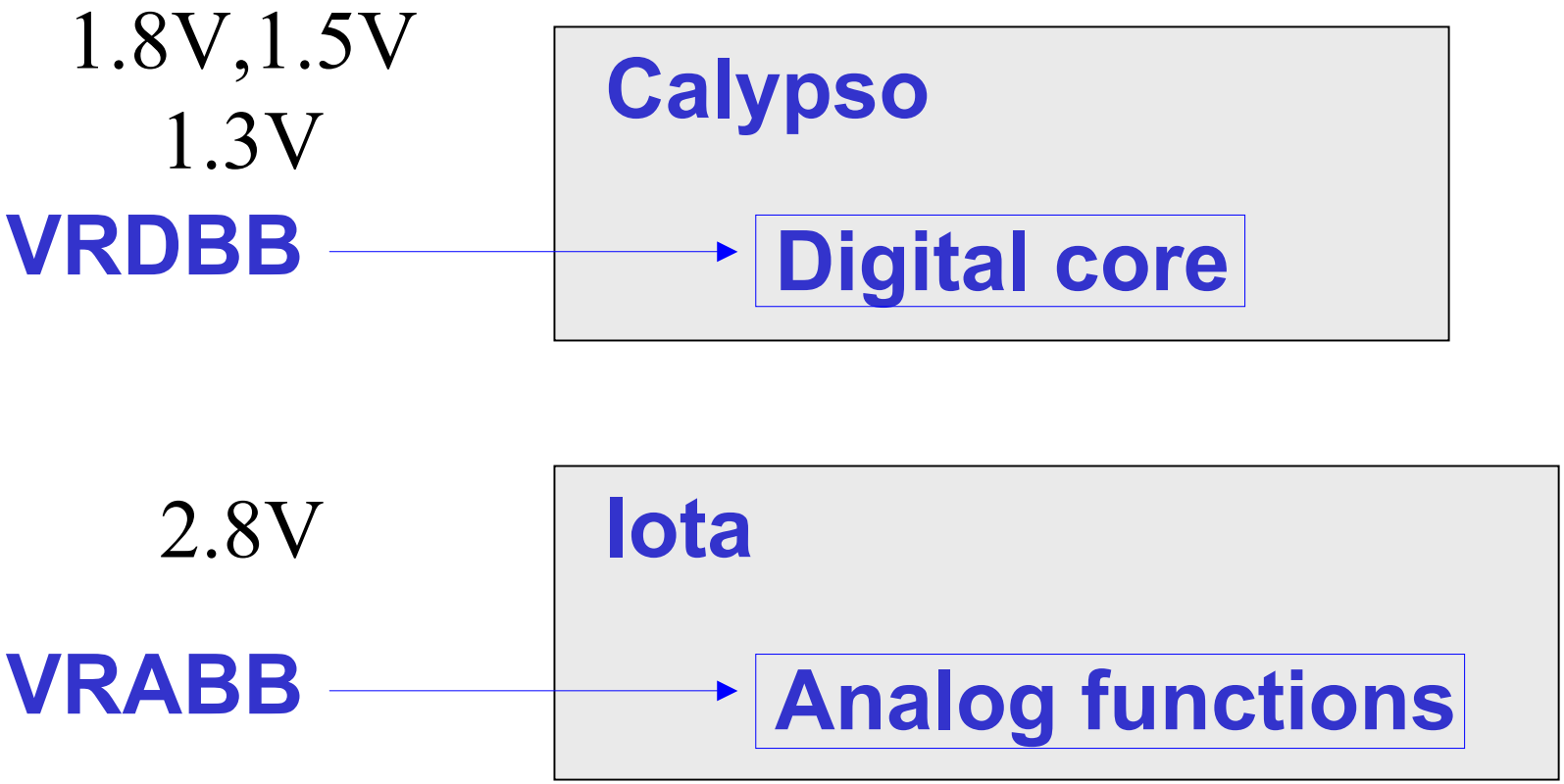
Sleep concept 2/2



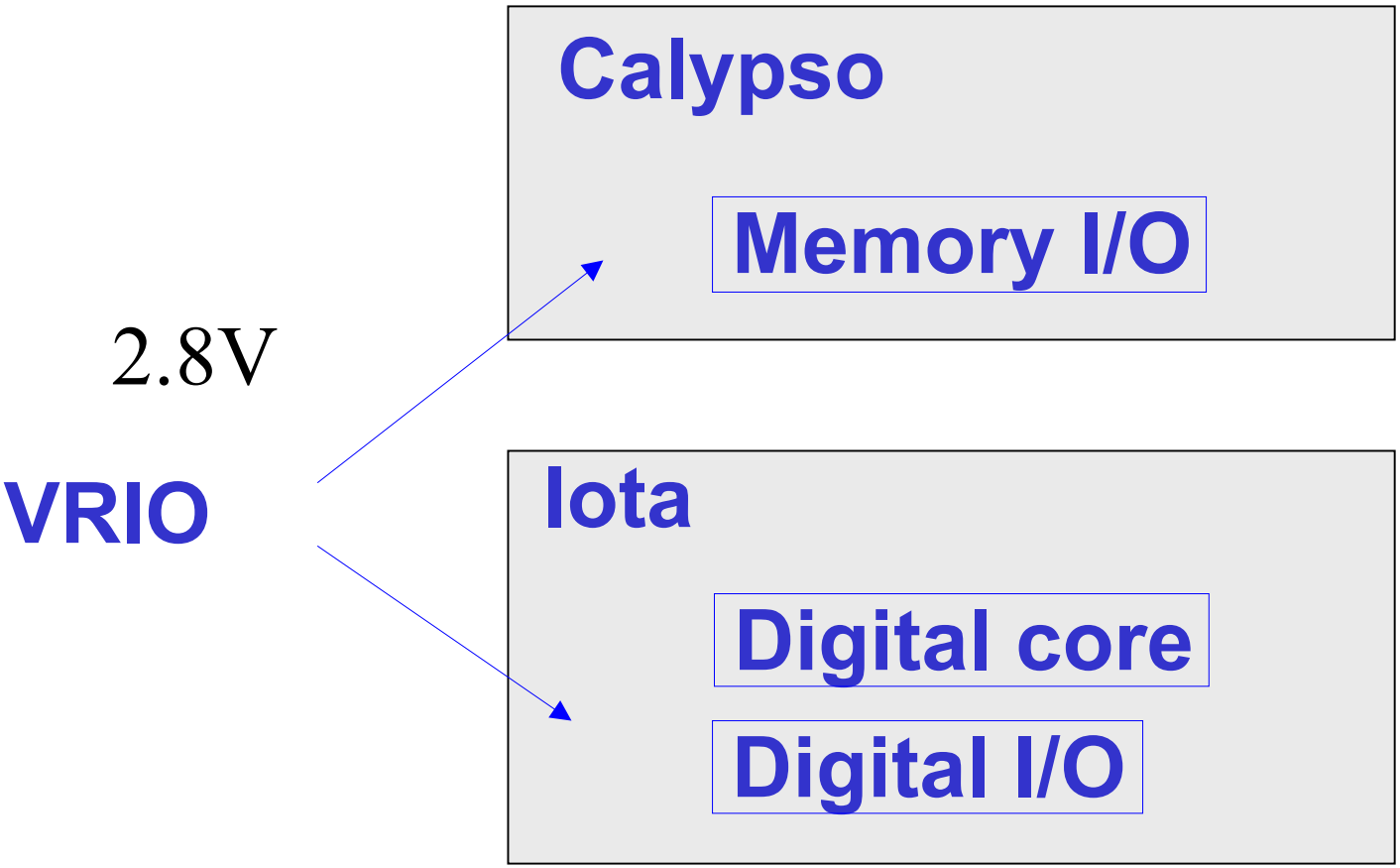
VREG - Blocks Description



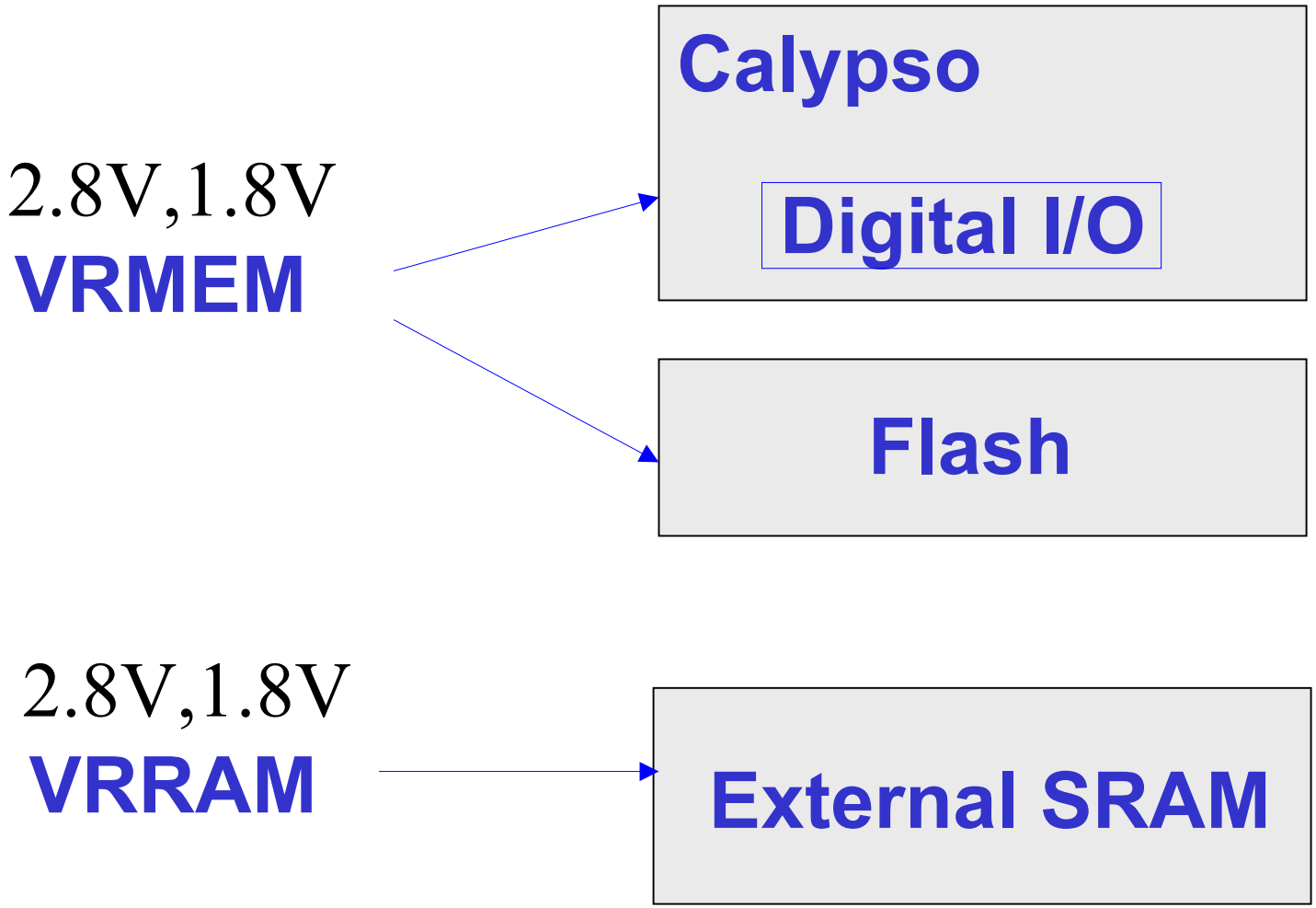
Voltage Regulation



Voltage Regulation



Voltage Regulation



Voltage Regulation

1.8V,1.5V,
1.3V

VRRTC →

Calypso

- **RTC**
- **32KHz oscillator**

Iota

- **VRPC**

Back up system maintains VRRTC insure a RTC Alarm can be send to Iota.

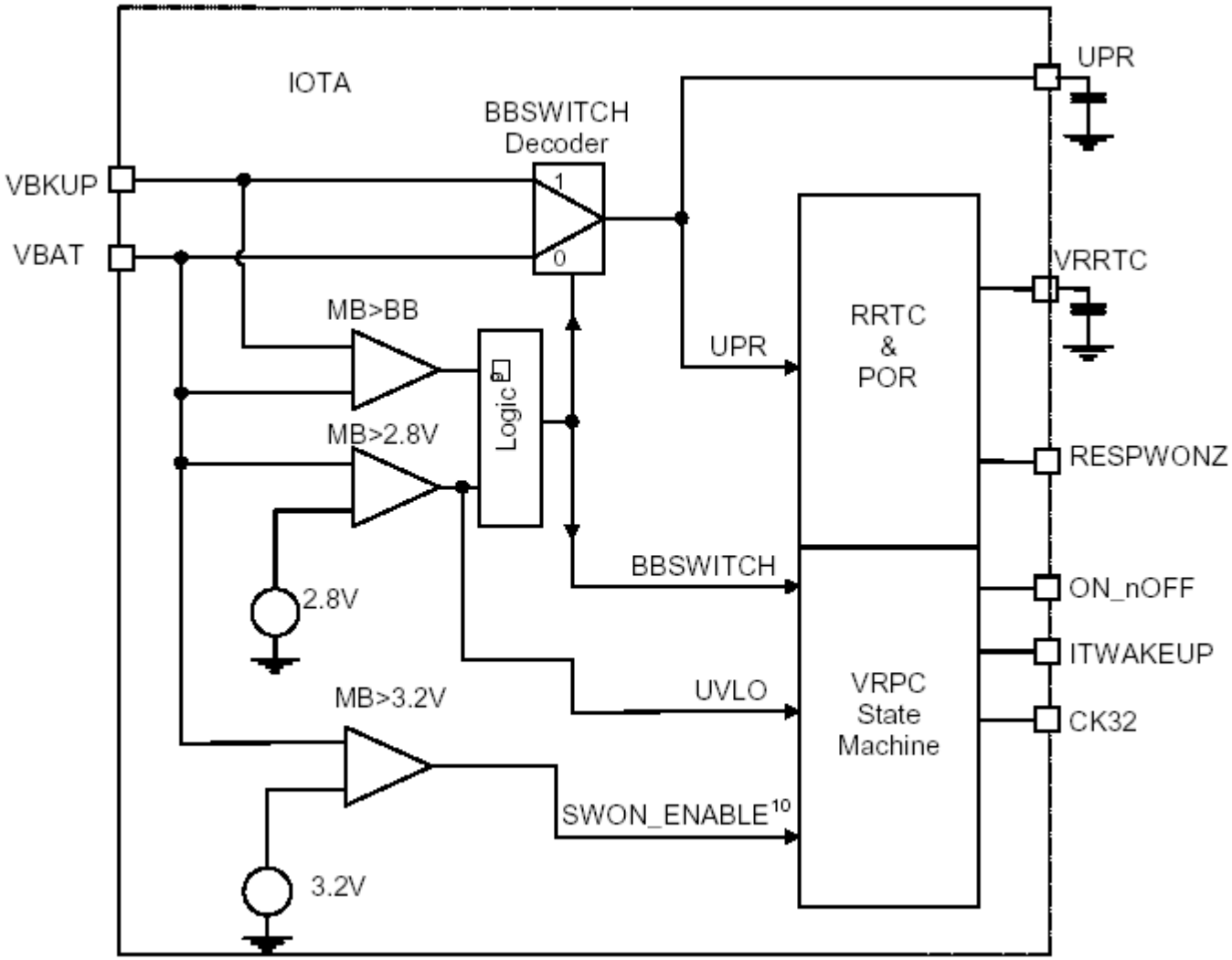
Topic

2.9V,1.8V

VRSIM →

SIM interface I/Os

VREG - Backup System



VREG - Backup System

RESPWONZ signal use to reset:

1. VRPC SM
2. Calypso RTC,Split power logic and XO32K Module.

RESPWONZ signal is held low level until below conditions matched:

1. The VRRTC is at the nominal regulated voltage
2. The UPR voltage is higher than 2.6V

Once this signal has been released:

OSC32K_OUT ⟶ Iota(VRPC SM)

VREG - Backup System

The decision to use **Main battery** or **Back-up battery :**

1. When **Vmain > Vbackup** or **2.8V < Vmain < Vbackup**
   → **use Main battery**

2. **When Vmain < Vbackup < 2.8V**
   → **use Back battery**

Iota Power Management

- Voltage Regulation
- Battery Charger Interface
- Voltage Reference Power-on Control
- SIM Card Regulator&Shifters

Battery Charger Interface

Function:

1. BCI is the charging control of both 1-cell Li-ion Battery or 3-serie Ni-MH/Ni-Cd cell battery with the support of the uC .

2. In case of a rechargeable Back-Up battery it also delivers a trickle charge current to the back-up battery from the main battery .

BCI

- Precharge and Trickle charge control
- Main battery charging control
- Back-up battery charge
- Battery temperature and Battery type measurements
  (Thermistor and battery identification resistor supplies)
- Battery monitoring

The charging scheme for the Li-ion battery

Precharge phase:

Low current charging(typ current is C/10)

That brings the battery at a voltage level allowing minimal system SW functionality(3.2V).

Fast charge phase(under SW control)**:**

1. constant current charging(typ current is 1xC)
2. constant voltage charging once a certain voltage threshold is reached(4.2V TBD).

Fast charge termination criterion:

Charging is stopped when the charging current (at constant voltage) has decreased down to C/20 (TBD) or by a selected Charge period timeout.

The charging scheme for the Ni-MH/Ni-Cd battery

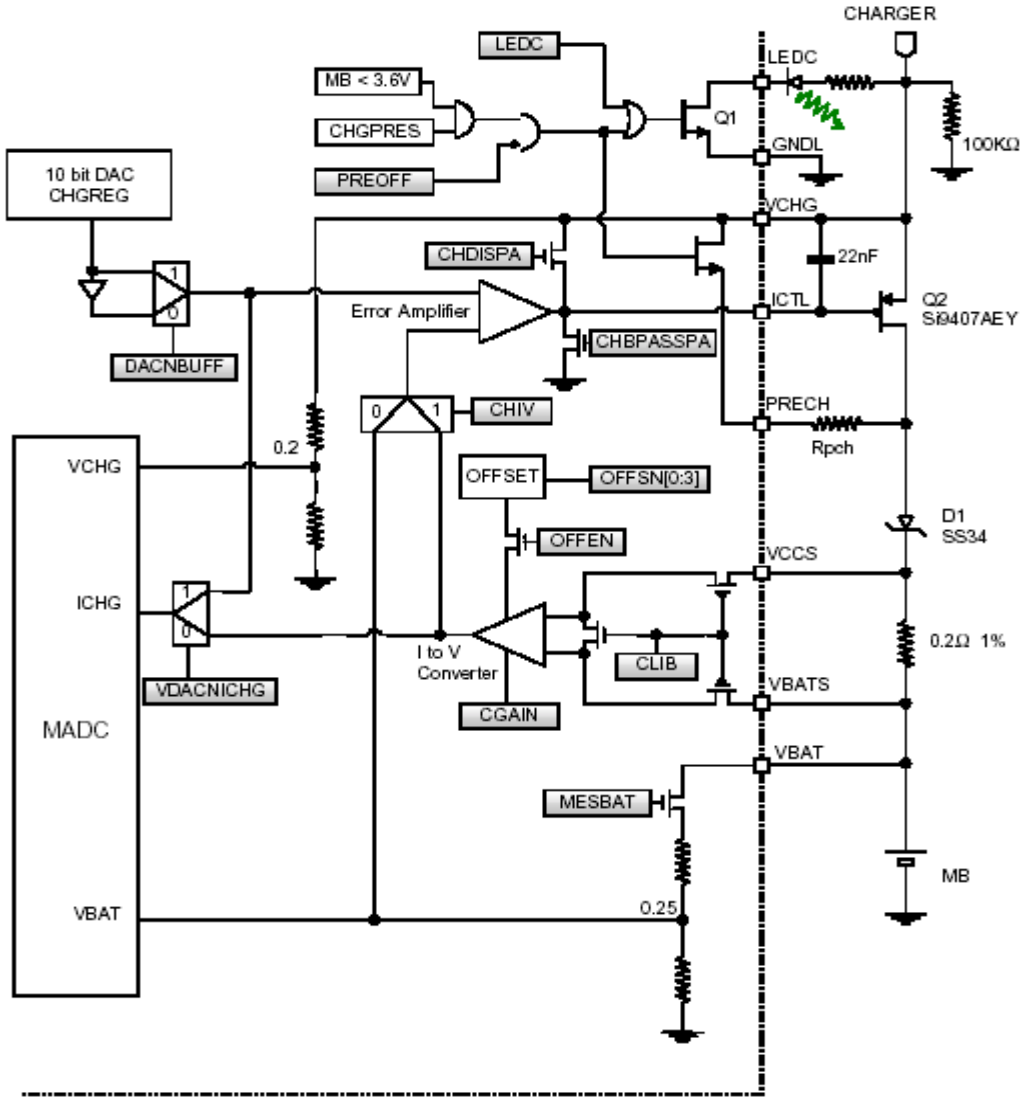
1. constant current charging

2. Charging is stopped when Delta-V versus time inverts from positive to slightly negative (typ. a few mV per cell) or by any other criteria involving battery voltage or battery temperature.

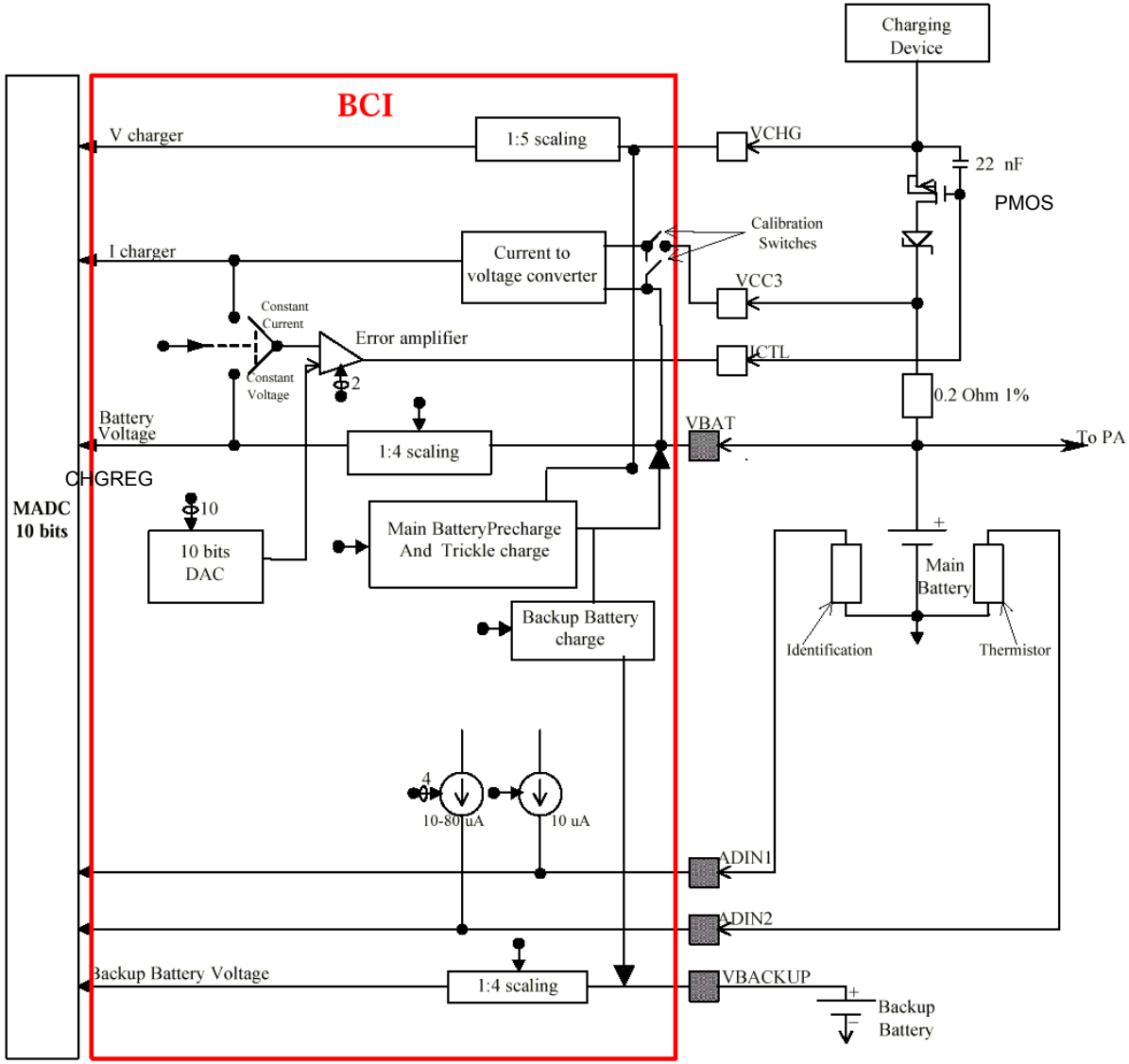
Battery monitoring

1. the battery voltage
2. battery temperature
3. battery type
4. battery charge current
5. battery charger input voltage
6. the back-up battery voltage

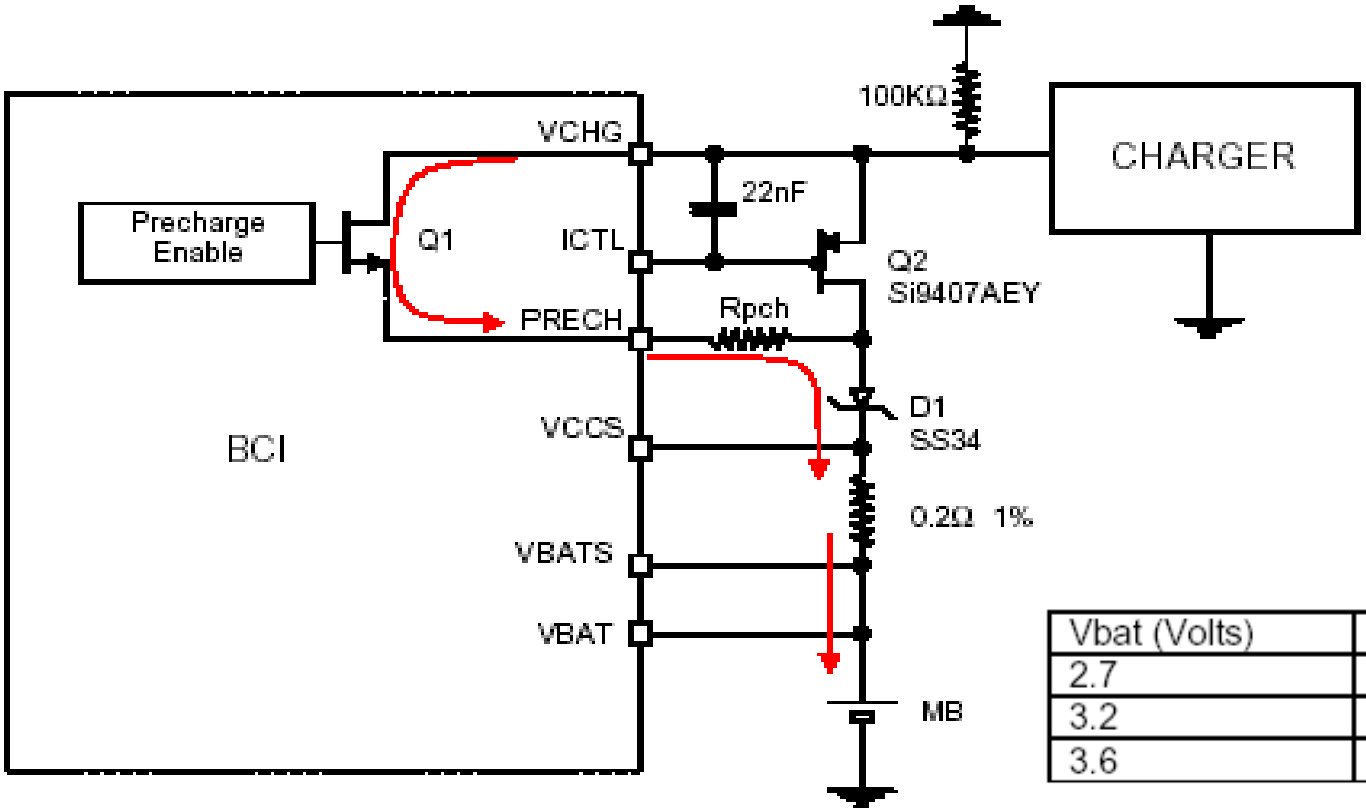
BCI - Block Diagram



BCI - Block Diagram



Precharge Circuit



Vbat (Volts)	Ipchg (mA)
2.7	58.4
3.2	50.7
3.6	44.6

When Vbat=0,Ipchg=100mA:

Rpch=(Vchg-VdropD1)/Ipchg-Rdson-0.2=62.8

Ipchg=(Vchg-VdropD1-Vbat)/(Rpch+Rdson+0.2)

Iota Power Management

- Voltage Regulation
- Battery Charger Interface
- Voltage Reference Power-on Control
- SIM Card Regulator&Shifters

Voltage Reference / Power Control

System Mode Definition

Mode Definition

NOBAT : Batteries (MAIN or BACK UP) are not efficient to supply ABB or DBB. PORZ is maintained low, All ABB registers are reseted, DBB is reseted.

BACKUP : BACKUP battery is used to supply UPR, only VRRTC is enable supplied by UPR, 32KHZ is available, all switch on conditions are masked. Part of ABB is reseted (see register bits definition) , DBB is reseted.

OFF : MAIN battery is used to supply UPR, VRRTC is available supplied by UPR, 32KHZ is available. VRDBB, VRMEM, VRRAM, VRIO, VRSIM supplied by MAIN battery can be in sleep mode (using MSKOFF register) or are disable. VRABB is disable. Part of ABB is reseted (see register bits definition), DBB is reseted.

SLEEP : MAIN battery is used to supply UPR, VRRTC is available supplied by UPR, 32KHZ is available. VRDBB, VRMEM, VRRAM, VRIO, VRSIM supplied by MAIN battery can be in sleep mode (using MSKSLP register) or are disable. VRABB is disable. All ABB blocks are forced in power down mode, but power on block configuration is kept when ABB return in ACTIV mode.

ACTIV : MAIN battery is used to supply UPR, VRRTC is available supplied by UPR, 32KHZ is available. VRDBB, VRMEM, VRRAM, VRIO, VRABB are enable and under DBB control, VRSIM is under DBB control.

System Mode

- ***No Supply***

  This mode is characterized by the lack of supply sources neither from MB nor from BB. It can be the case of missing batteries or flat batteries. All ABB register are in reset state, DBB is forced to reset.

System Mode

- ***Active***
- Activity of the system is tightly linked to the state of the voltage regulators that provide current. Two chips, in the proposed chipset solution, have embedded regulators: Iota and Clara
- While in Clara device LDO's are exclusively dedicated to the RF part of the system and their enable is related to RF periods of activity, Iota ones are used to supply both the DBB and the ABB part of the chipset. Thus any SW control activity on the system could be possible only when those regulators are active.
- First definition of the active mode hence could be the following: System is in active mode when both Iota and Clara LDO's are enabled and SW is able to manage GSM activity.
- Once Iota regulators are enabled and the Switch ON procedure terminated, SW becomes the system master ant it is its own choice to select operating modules depending on the application.
- MB values allowing the system to stay in active mode are MB > 2.8V

System Mode

- ***Off***
- This mode is characterized by the presence of a charged MB (MB > 3.2V) and by the disabled state of Iota LDO's7. In this condition system is ready to accept a switch on command to pass in active mode. The ON_nOFF signal is at low level indicating to the DBB that LDO's are not able to deliver nominal current and isolating the split domain from the rest of the Calypso chip.
- The system active blocks in this mode are:
- **Iota:**

  VRRTC regulator
  POR logic
  BBSWITCH logic
  Power management I/O's (RESPWONZ, ON_nOFF, IT_WAKEUP)
  LDO's programmed to stay in SLEEP mode
- **Calypso:**

  RTC
  XO32K
  Power split Logic
  Split I/O
- **Clara:**

  None

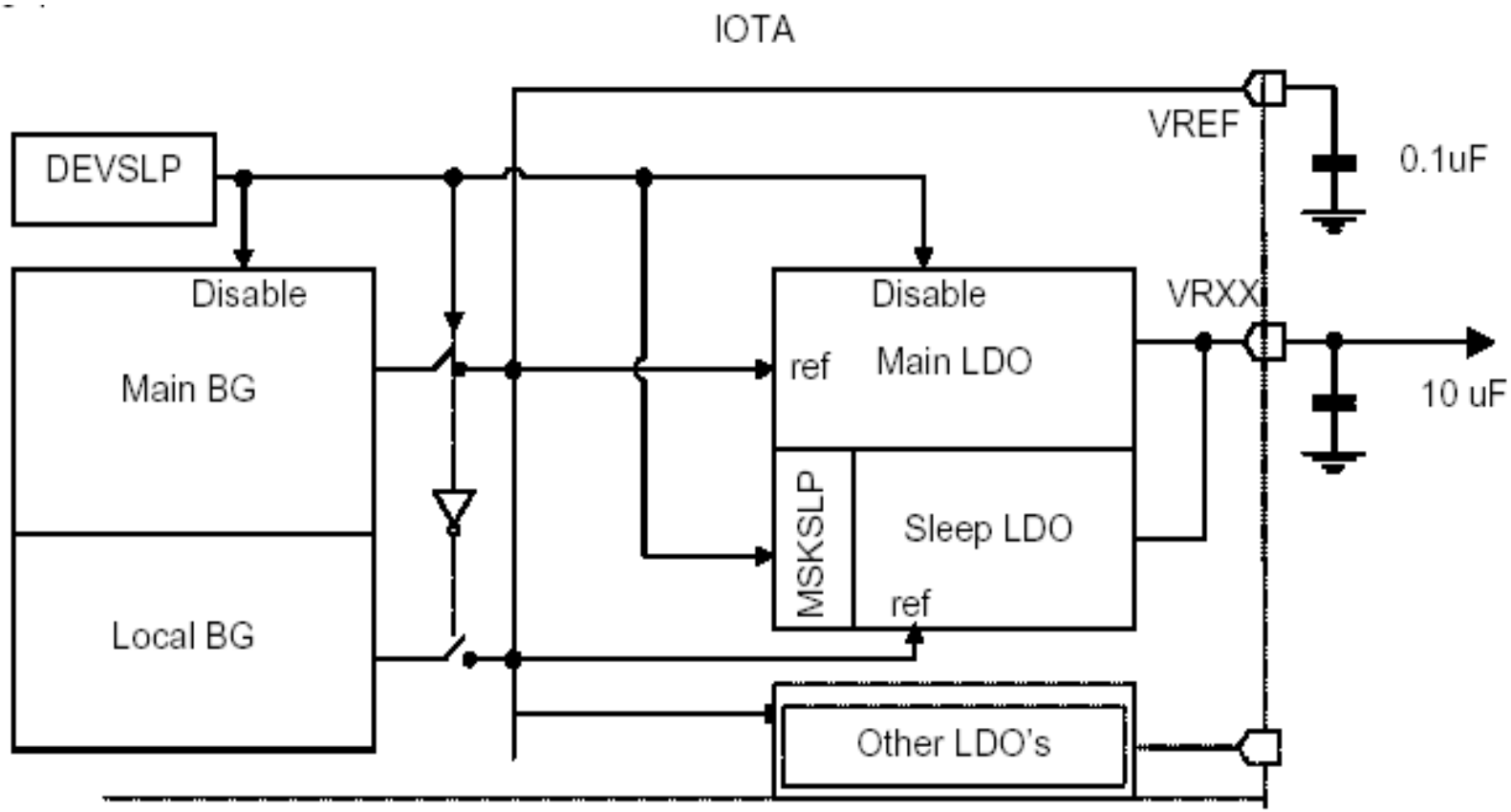
System Mode

- ***Backup***
- This mode is characterized by the fact that the supply source of the system is the BB or a MB below 3.2V. In this state only the minimal mobile functionality's are still alive, the real time clock RTC, the POR logic and on some architectures the SRAM backup supply. Any switch on command in this state will be ignored.
- The ON_nOFF signal is low, and the Calypso split domain isolated.

System Mode

- ***Sleep***
- System sleep mode is characterized by a low consumption state of Iota regulators. Although still enabled Iota LDO's are no longer able to provide the full active rated current. They keep the regulated voltage with a reduced maximum rated output current of 1mA.
- This allows the system to freeze its configuration during inactivity periods.
- In this mode in fact the ON_nOFF signals stays at high logical level (no register reset is asserted)
- But application SW is no longer enabled to run. This mode has been expressly conceived for system current consumption reduction during inactive periods of mobile paging mode and to support the L1 Deep Sleep SW mode.
- Also in Sleep mode Iota main band gap is off, reference for regulators is provided by a local band gap.

Sleep Mode


IOTA
DEVSLP
Disable
Main BG
Local BG
Disable
ref
Main LDO
MSKSLP
Sleep LDO
ref
Other LDO's
VREF
0.1uF
VRXX
10 uF

Sleep mode

Active blocks in this mode are:

Iota:
- VRRTC regulator
- POR logic
- Power management I/O's (RESPWONZ, ON_nOFF, IT_WAKEUP)
- MB vs BB comparator
- Sleep LDO's
- Local bandgap
- BB charge (if enabled)

Calypso:
- RTC
- XO32K
- Power split Logic
- ULPD
- INTH
- All supply domains are powered but no current sink is allowed

Clara:
- Serial Port

System mode transitions

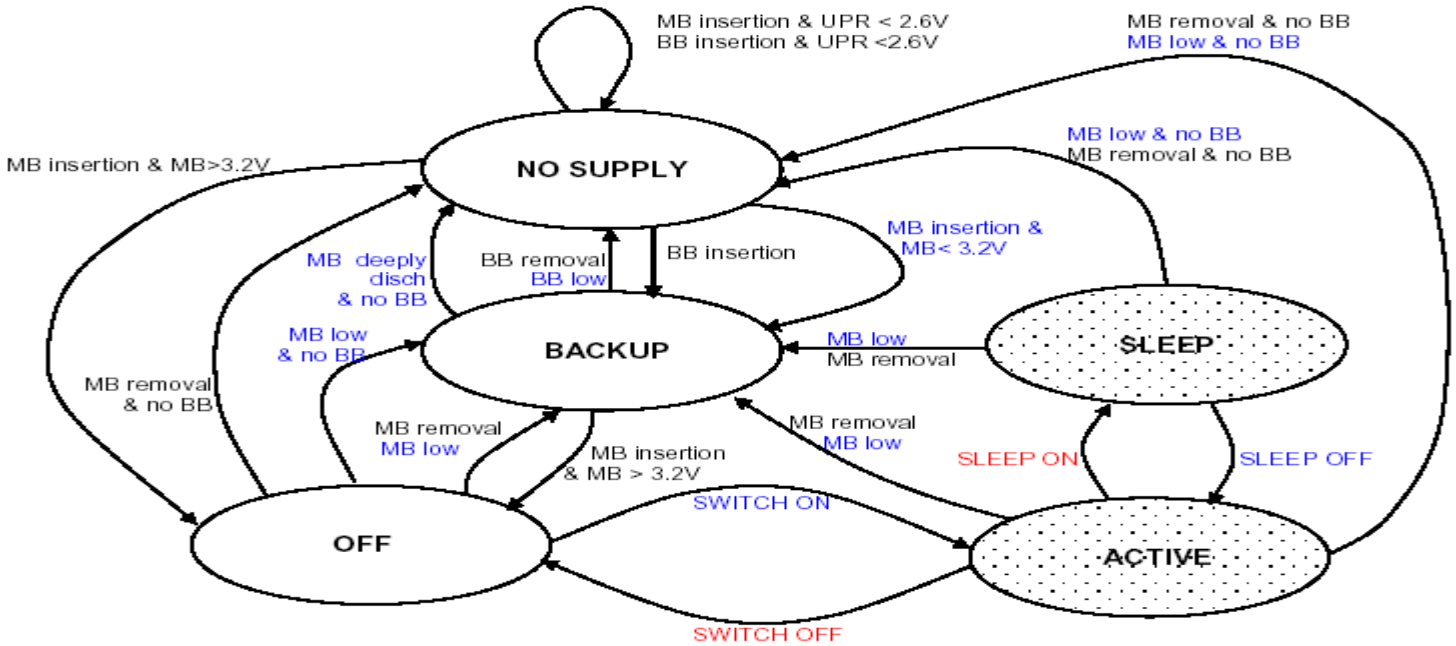


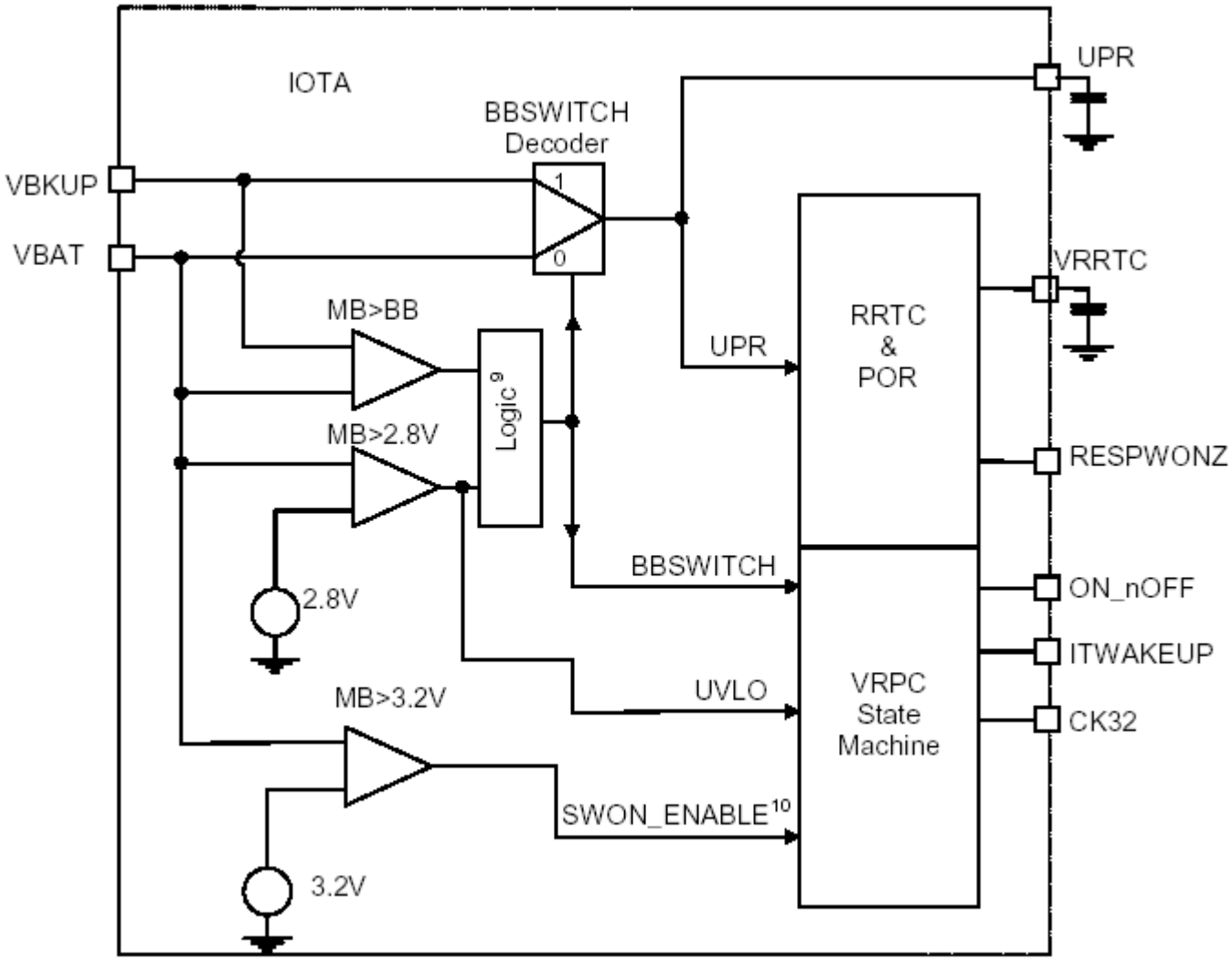
Figure 5-1 System operating modes transitions

NO SUPPLY	UPR<2.6V, ON_nOFF = 0, nRESPWONZ = 0
BACKUP	UPR<3.2V, start conditions not accepted, ON_nOFF = 0, Calypso split isolated
OFF	UPR>3.2V, start condition accepted, ON_nOFF = 0
ACTIVE	UPR>2.8V[8], SW control of the system, ON_nOFF = 1
SLEEP	UPR>2.8V, no SW running, ON_nOFF = 1, LDO's low consumption state

In RED characters : SW driven transitions
In BLUE characters : HW detection driven transitions
In BLACK characters : Supply insertion/removal driven transitions

A high logic level of the ON_nOFF signal characterizes shaded states

VRPC state machine



VRPC main functions

. Checking of power supplies levels : batteries and LDO output voltages,
. Detection of Switch ON condition,
. Controlling step by step Switch OFF to Switch ON logic sequence and Switch ON to Switch OFF logic sequence,

. Generation of interrupts,
. Generation of emergency Switch OFF request,
. Providing internal references currents and voltages, internal clock.

VRPC - Power on Condition

Power on Condition:

- On the plug of valid main battery or backup battery

3.1 System Power On Reset generation

The RESPWONZ signal is used as reset for the Iota VRPC SM and for Calypso RTC, Split power logic and the XO32K module.

The nRESPWONZ signal is held in a low state until both conditions below are not matched:

- The VRRTC regulator is at the nominal regulated voltage.
- The UPR voltage is higher than 2.6V

This to allow internal digital VRPC logic reset and external RTC and XO32K modules reset. Once this signal has been released the XO32K modules starts providing the OSC32K_OUT signal to Iota. This clock is used by the VRPC synchronous state machine.

VRPC - Switch on Condition

Switch On Condition:

1. Falling edge (after debounce) is detected at pin PWON
   Action : push ON button (debouncing time of 30ms)
2. Falling edge (after debounce) is detected at pin RPWON
   Action : ON REMOTE
3. Rising edge is detected on pin RTC_ALARM
   Action : IT_WAKE_UP
4. Signal CHGB='1'
   Action :CHARGER_IC plugged

Switch on sequence

Sequence consists in:

Iota:

- Enabling the main band gap
- Waiting **1010** 32KHz-clock cycles to let the BG reach its nominal value (1.2 V)
- Checking for BG delivering the nominal reference.
- Checking for MB higher than 3.2V
- Enabling RDBB, RABB, RMEM
- Waiting **10** 32KHz-clock cycles to let the LDO's reach their nominal value.
- Checking for LDO's delivering the nominal voltage.
- Enabling RIO
- Waiting **10** 32KHz-clock cycles to let the LDO reach its nominal value.
- Checking for LDO delivering the nominal voltage.
- Release ABB reset and setting the ON_nOFF signal to logic 1.

If one of the check included in the sequence fails the SM brings system back to OFF state.

Calypso:

- Waits default RF setup time(0 at reset).
- Set to logic one the RFEN pin
- Wait default VTCXO setup time (4096 at reset)
- Set to logic one the TCXOEN pin
- Wait SLICER setup time (4096 at reset)
- Enable SLICER module
- Wait 13MHz clock setup time (64 at reset)
- Release the FDP (Flash Deep Power) signal and chip internal reset.
- MCU receives 13 MHz clock after 3 T_{VTCXO} (VTCXO periods) and MCU activity starts after 20 T_{VTCXO}.

Switch on sequence

- Program starts:
  - SPI access to IOTA :
    - Configure Iota device
  - TSP accesses to RF part :
    - Enable Clara LDO's in fast mode
    - Configure Clara device
    - Configure TSPACT signal.
- Wait for a stable AFC output and nominal regulated output at CLARA LDO's. During this period system enter SW BIG SLEEP mode to avoid power consumption.
- Exit the BIG SLEEP mode.
- Program normal mode in CLARA bandgap.

System is now in ACTIVE state and able to perform GSM activity.

Sleep off conditions

- **Synchronous Wake-Up**

  The GSM TIMER reaches the zero value and wakes up DBB and ABB through an internal interrupt (DBB GSM TIMER IT) and the generation of an ITWAKEUP signal (ABB)

- **Asynchronous Wake-Up**

  DBB is wake-up from an asynchronous event before GSM TIMER interval has been elapsed. Those events generating an internal interrupt to DBB and an external ITWAKEUP signal may be (if non masked interrupts):

▪ Keypad I/O transition	push keypad buttons.
▪ RTC alarm	user pre-programmed alarm
▪ UART	out-coming data.
▪ EXT_FIQ	INT1 generation due to an EMERGENCY condition
▪ EXT_IRQ	External accessory plug, Charger Plug, ON/OFF button push.

Sleep off sequence

Iota:

- Enables the main band gap
- Waits **130** 32KHz-clock cycles to let the BG reach its nominal value (1.2 V)
- Checks for BG delivering the nominal reference.
- Checks for MB higher than 3.2V
- Enables RDBB, RABB, RMEM
- Waits **7** 32KHz-clock cycles to let the LDO's reach their nominal value.
- Checks for LDO's delivering the nominal voltage.
- Enables RIO
- Waits **7** 32KHz-clock cycles to let the LDO reach its nominal value.
- Checks for LDO delivering the nominal voltage.

If one of the check included in the sequence fails the SM brings system back to OFF state. Iota is then ready to support the system ACTIVE mode.

Calypso:

- Waits RF setup time(previously programmed in SETUP_RF_REG register).
- Set to logic one the RFEN pin
- Wait VTCXO setup time (previously programmed in SETUP_VCTXO_REG register)
- Set to logic one the TCXOEN pin
- Wait SLICER setup time (previously programmed in SETUP_SLICER_REG register)
- Enable SLICER module
- Wait 13MHz clock setup time (previously programmed in SETUP_CLOCK_13MHZ_REG register)
- Release the FDP (Flash Deep Power) signal and chip internal functional restart
- MCU receives 13 MHz clock after 3 T_{VTCXO} (VTCXO periods) and MCU activity starts after 20 T_{VTCXO}.
- Program starts:
  - SPI access to IOTA :
    - Restore Iota ACTIVMCLK
    - Restore AFC value
  - TSP accesses to RF part :
    - Enable Clara LDO's in fast mode
    - Restore TSPACT configuration.
- Wait for a stable AFC output and nominal regulated output at CLARA LDO's. During this period system enter SW BIG SLEEP mode to avoid power consumption.
- Exit the BIG SLEEP mode.
- Program normal mode in CLARA bandgap.

VRPC - Switch off Condition

Switch Off Condition:

1. Bit DEVICE_OFF = '1'
   Action: push ON button
2. Removal of Main battery
3. VBAT < 2.8V (emergency condition)
4. VBAT < VBACKUP (emergency condition)

• Note: When a switch off sequence is started, the sequence is completed even if a switch on condition occurs.

VRPC - Switch off Logic Sequence

System configuration to enter OFF mode consists in:

- Halt application activity.
- Disable Clara LDO's and any other possible current sinking device controlled through TSPACT interface.
- Disable al Iota modules programming TOGBR1 and TOGBR2 registers.
- Select through the VRPCMSK register LDO's that have to stay in SLEEP mode. even during system OFF state[16] (depends on backup scheme adopted)
- Start the ACTIVE to OFF transition programming the bit DEVOFF in Iota VRPCDEV register.

At this stage the Iota VRPC SM takes HW control of the SWITCH OFF transition executing the following sequence:

- Wait 5 T_{32K} periods.
- Force the ON_nOFF signal to logic 0
- Forcing the internal ABB reset to logic 0
- Disable LDO's using the MSKOFF content

When the ON_nOFF signal goes to low state Calypso asserts the internal functional reset (DSP & MCU) and the external reset nRESET_OUT, split power part is isolated. The system is in OFF mode.

Sleep on conditions

5.3.2 SLEEP ON

This transition is initiated on application SW decision. While in paging mode the mobile alternates shorts periods of GSM activities with relatively long (up to around 2 seconds in DRX9) period of inactivity that correspond to system SLEEP state.
Valid conditions to enter into SLEEP mode are evaluated by the activity management part of the application SW in terms of number of frames in which no system activity is required.
If number of inactivity frames is greater than given threshold[17] SW initiates system configuration to enter in Deep Sleep (SLEEP) mode.

Sleep on sequence

System configuration consists in:

- De-mask all wake up sources (Keypad, external interrupts, GSM timer interrupt, RTC alarm).
- Program the GSM TIMER with the number of SLEEP frames and all the setup times for RF, VCTXO, SLICER and CLK13.
- Disable all Iota modules (TOGBR1 and TOGBR2 registers) AFC block is treated separately.
- Configure Clara Bandgap to speed-up mode and disable Clara LDO's.
- Configure the TSP parallel interface in order to have low logical value on the TSPACT signal going to RF.
- Select the delay SLPDLY between the MCU access that states SLEEP mode and the instant at which Iota LDO's will switch to SLEEP mode (VRPCCFG register in Iota).
- Configure Iota test mode to access directly the AFC_OUT register and force an AFC value of zero.
- Start the ACTIVE to SLEEP transition programming the bit DEVSLP in Iota VRPCDEV register.
- Set Iota ACTIVMCLK to zero indicating that the 13MHz clock will be no longer available to Iota.
- Halt Calypso peripheral modules.
- Program Big Sleep and Deep Sleep bits in Calypso CNTL_ARM_CLK register.

At this stage

Calypso :

ULPD switches on the 32 KHz clock to maintain the GSM time then it cuts in this order :

- The 13 MHz clock
- The SLICER
- The VCTXO and the external RF device (RFEN to logic 0).

Until a wake up event occurs ULPD state machines keeps this state.

Iota:

VRPC SM :

- Waits for the DLYSLP timer to be elapsed (DLYSLP value x 20 T_{32K})
- Disables LDO's using the MSKSLP configuration mask register[18]
- Switches to local Band Gap.

System is in SLEEP mode.

Current consumption

Backup mode

6.1.1 System without MB

Active blocks in this configuration are included in the following table:

Table 6-1 Estimated System BACKUP current consumption on BB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6[19]
Clara	
None	-
Total	**8.6**

The indicated values have to be considered as typical ones, calculated at room temperature.

Current consumption

Backup mode

Table 6-2 Estimated System BACKUP current consumption on MB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
BB charge (if enabled)	10
Band Gap	5
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6
Clara	
None	-
Total	**23.6**

Current consumption (off mode)

OFF mode

Table 6-3 Estimated System OFF current consumption on MB

	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
BB charge (if enabled)	10
Band Gap	5
RMEM LDO in sleep mode	13
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6
Clara	
None	-
External SRAM [6]	
SRAM Vcc Standby Current	1
Total	**37.6**

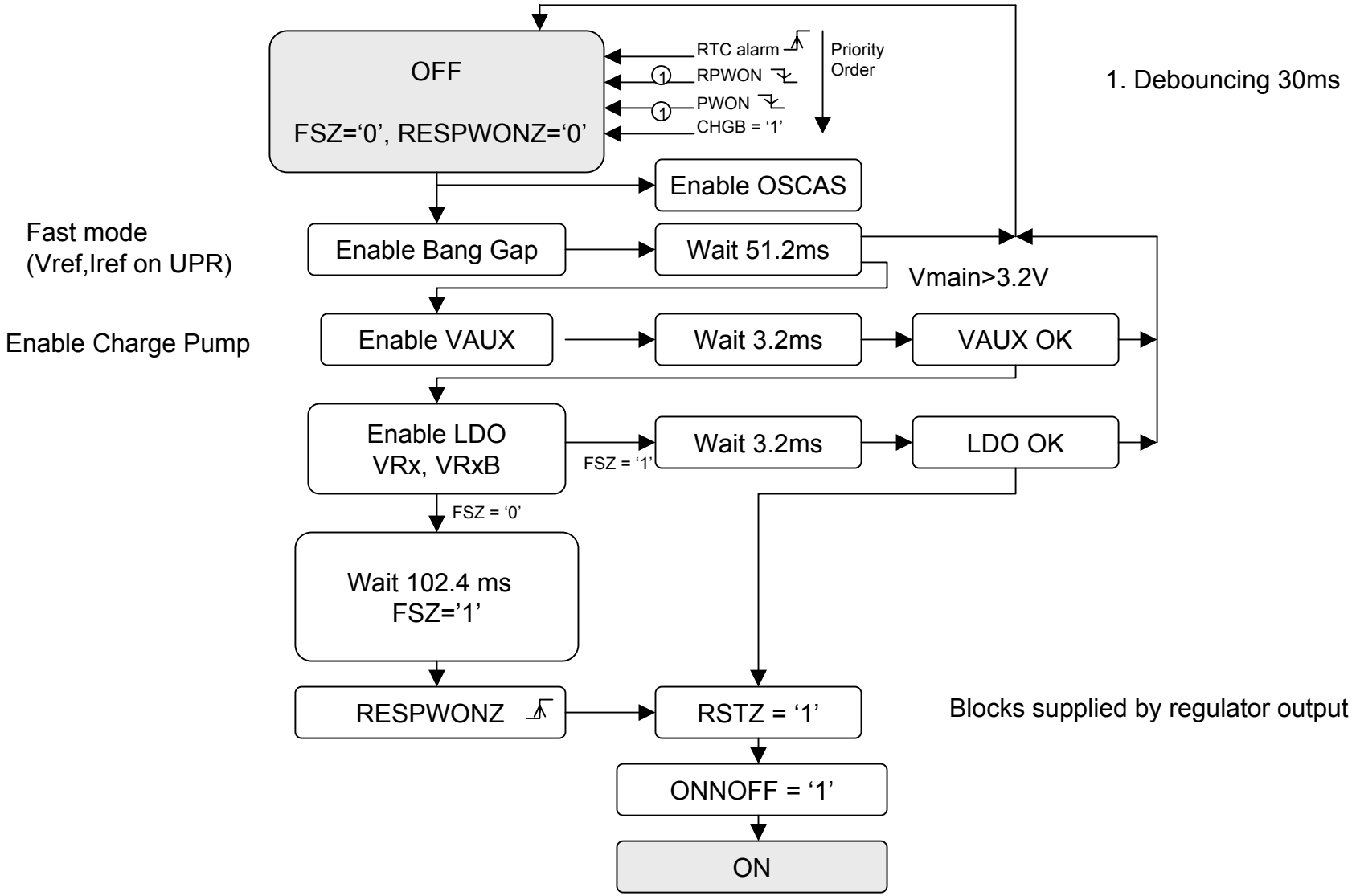
Current consumption (sleep mode)

Sleep mode

Table 6-4 Estimated System SLEEP current consumption on MB

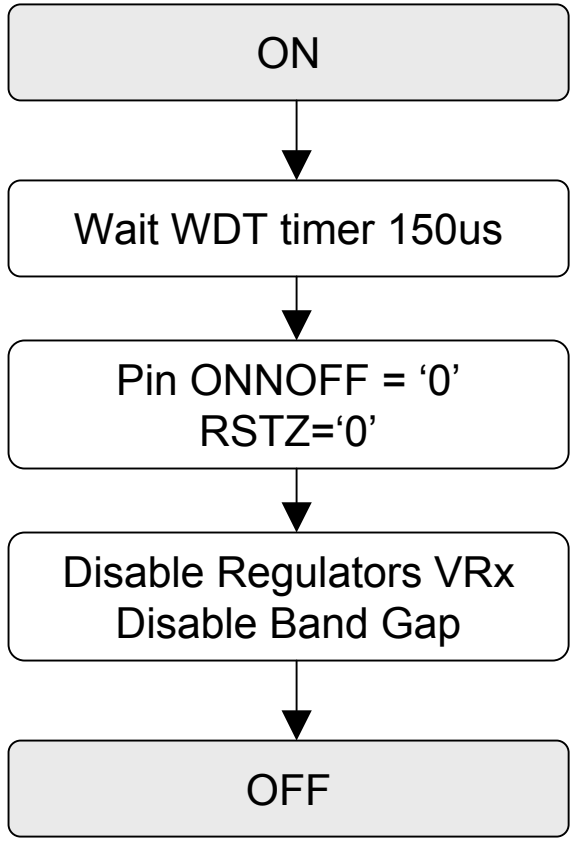
	Current Consumption (µ A)
Iota	
VRRTC regulator & POR logic	2.5
MB vs BB comparator	1
BB charge (if enabled)	10
Band Gap	5
RMEM LDO in sleep mode	13
RDBB LDO in sleep mode	13
RRAM LDO in sleep mode	13
RIO LDO in sleep mode	13
RSIM LDO in sleep mode	13
Calypso	
RTC & Power Split Logic	1
XO32K	3.5
XO32K IO	0.6
ASIC Core	100
Memory Interface	TBD
I/O's	TBD
Clara	
Serial Port	1
External SRAM [6]	
SRAM Vcc Stand-by Current	1
SIM Card	
SIM Vcc Stand-by Current (*)	TBD
Total	**190.6+TBD's**

VRPC - Switch On Logic Sequence



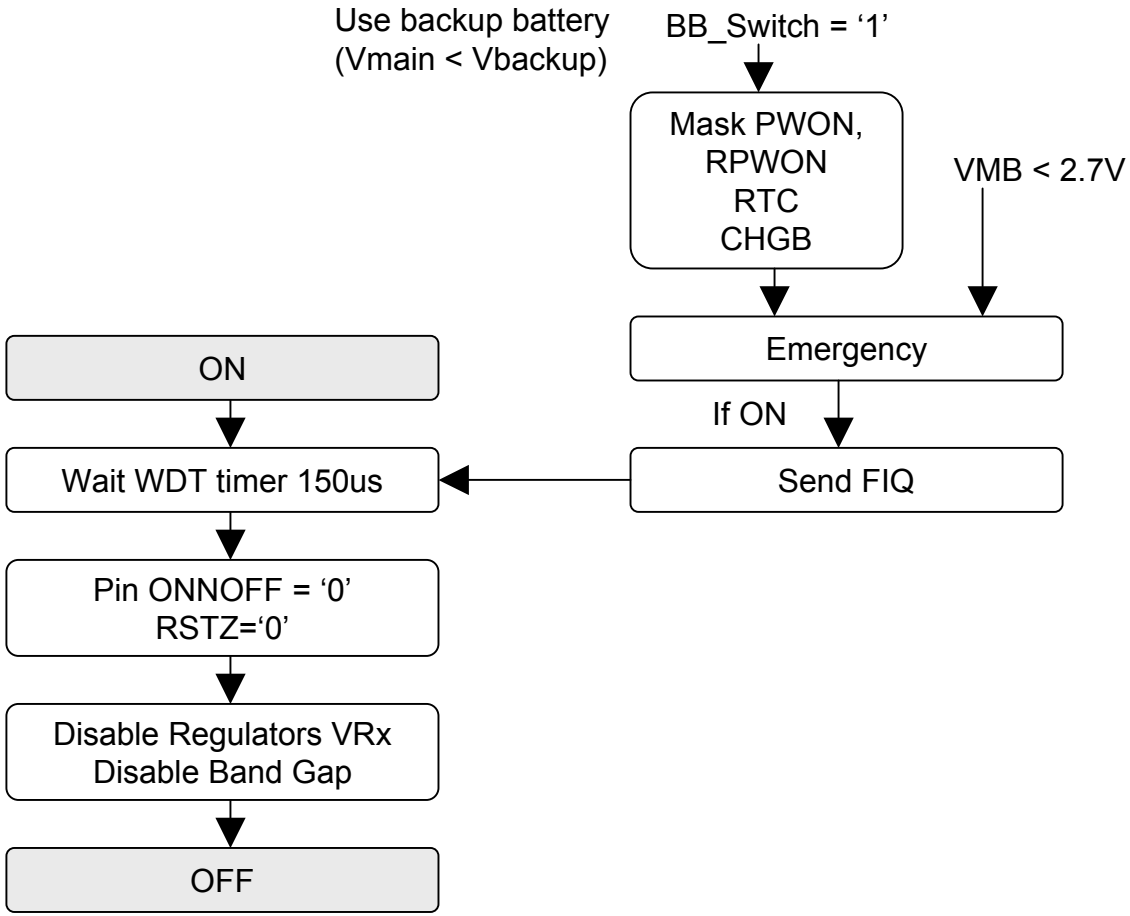
VRPC - Switch Off Logic Sequence in normal mode

1. Starts Watchdog Timer during 150us and disables the DCDC converter
2. Set pin ONNOFF to ‘0’
3. Disables all the regulators
4. Disables the Band-gap
5. Disables the local oscillator



VRPC - Switch Off Logic Sequence in emergency mode

1. Omega set a signal to set INT1 (FIQ) to low
2. Switch off logic sequence in normal mode



VRPC - Interrupt handling

VRPC is in charge to handle two kind of interrupts :

INT1, INT2

1. Interrupt related to the voltage level of the main battery Priority and set INT1 pin to low level.

2. Interrupts related to accessories plugged/unplugged or the push button, will generate a signal sent to the IBIC.

The IBIC is in charge depending on the interrupt mask register and its internal state machine to send a signal on INT2 pin.

Iota Power Management

- Voltage REGulation
- Battery Charger Interface
- Voltage Reference Power-on Control
- SIM Card Regulator&Shifters

SIM Card Shifters

The Sim Card digital interface

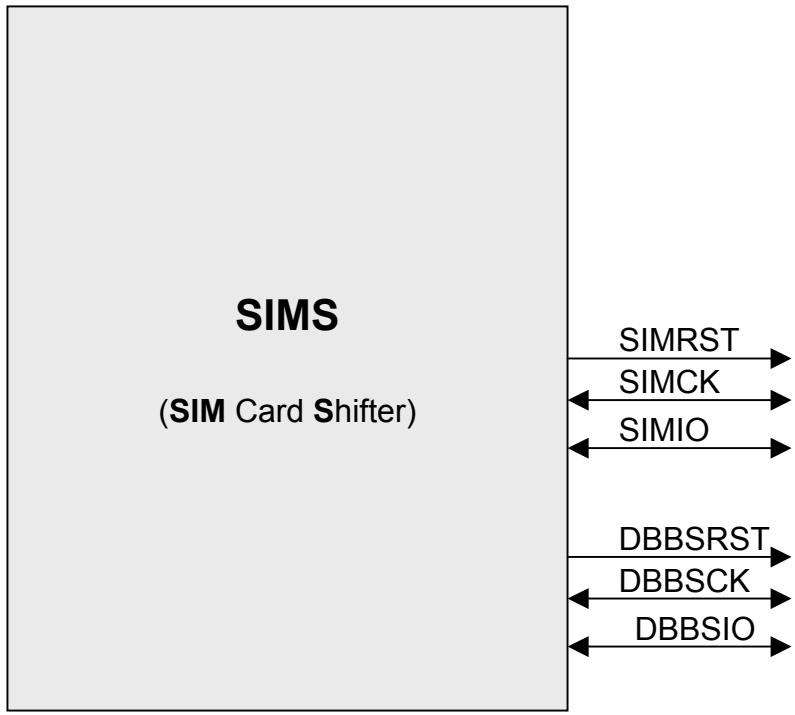
Function:

Insures the translation of logic levels between Calypso and Sim Card

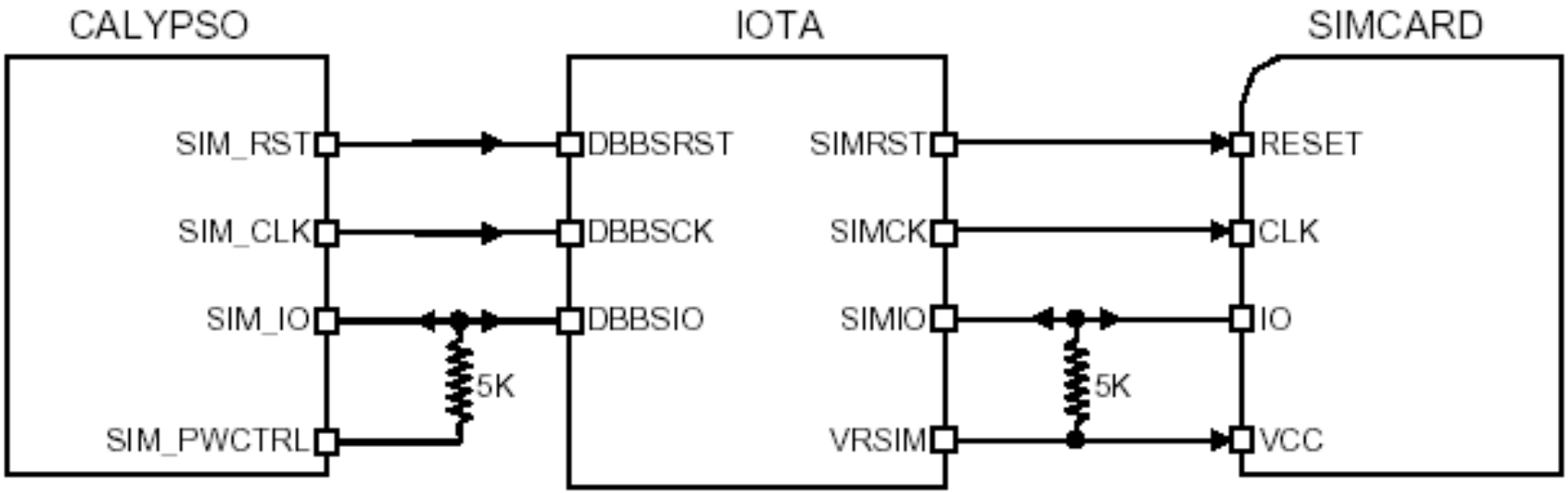
Transmission of 3 signals:

1. A clock derived from Calypso to the Sim Card (DBBSCK-SIMCK)
2. A reset signal from Calypso to the Sim Card (DBBSRST-SIMRST)
3. Serial data From Calypso to Sim card(DBBSIO-SIMIO)

SIMS - Pins Description



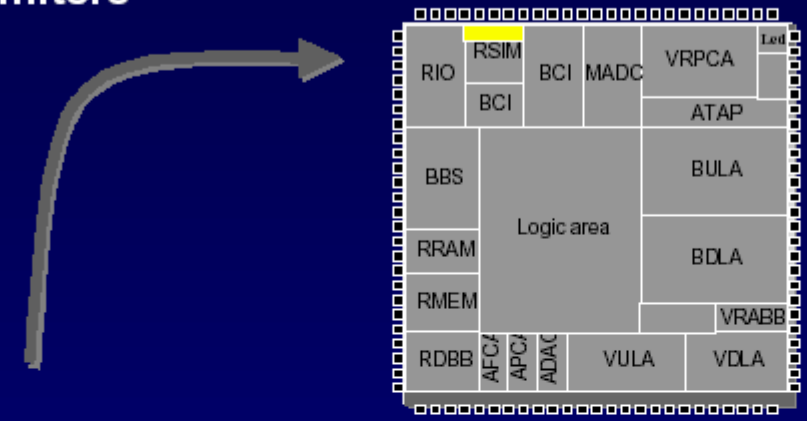
SIMS

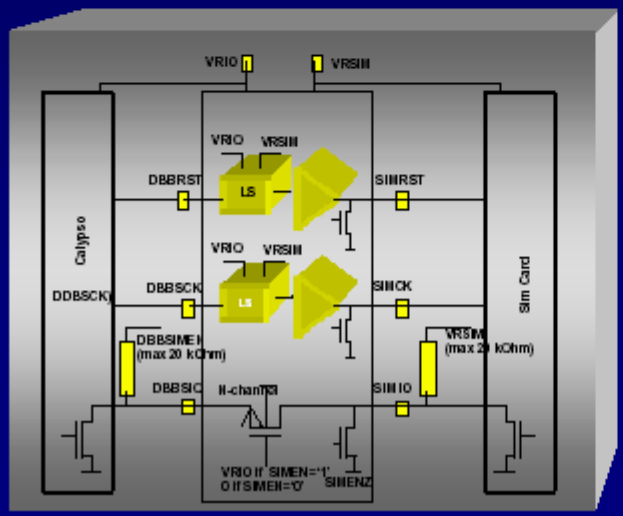


The SIM card interface can be programmed to drive a 1.8V or 3V Sim Card.

SIM card Interface

- Level shifters





- Features.
  - VRSIM
    - 1.8V / 2.9V 10mA dedicated LDO for Sim Card
  - Level shifters
    - Two unidirectionnal shifters SIMCLK & SIMRST
    - One bidirectionnal shifter SIMIO.

Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Port
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

Iota BB&VB Codec

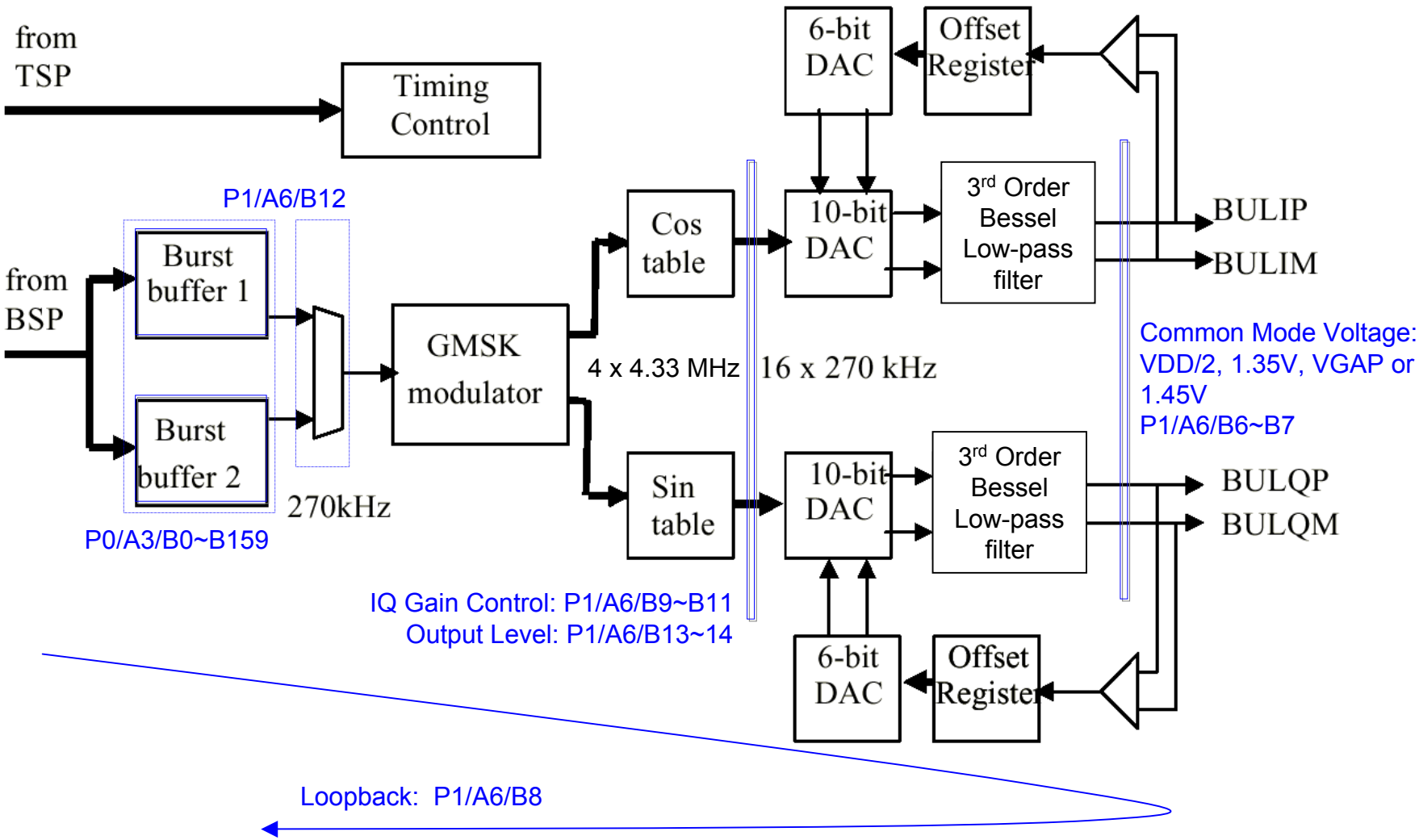
- Base Band Codec
- Voice Band Codec

Uplink General Description

The GMSK modulator is implemented digitally, the Gaussian filter computed on 4 bits of the input data stream being encoded in Sin/Cos look-up table in ROM, and it generates the In-phase (I) and Quadrature (Q) digital samples with an interpolation ratio of 16.

These digital I and Q words are sampled at 4.33 MHz rate and applied to the input of a pair of 10-bit DACs.

Baseband Uplink

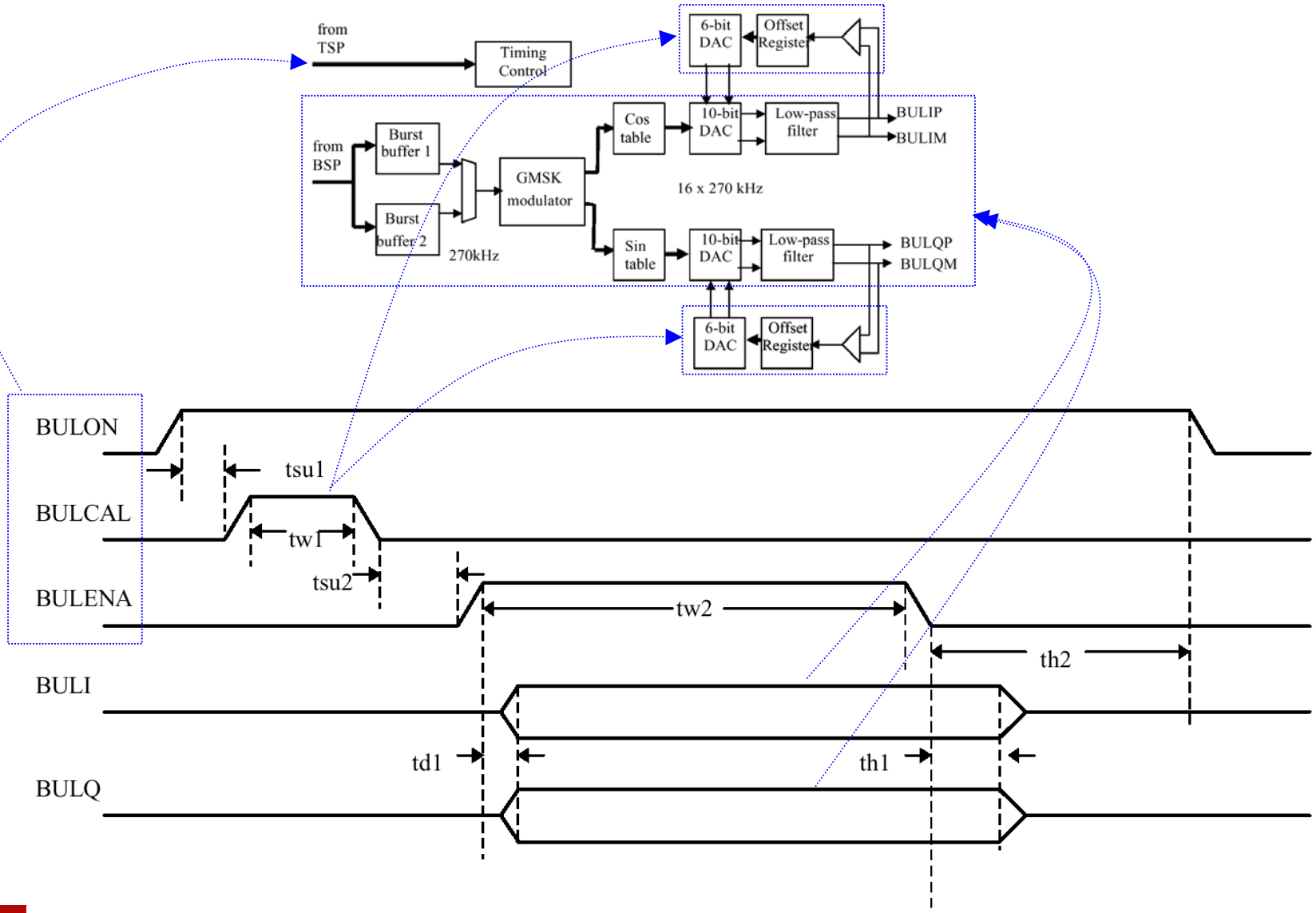


Sequence of burst transmission

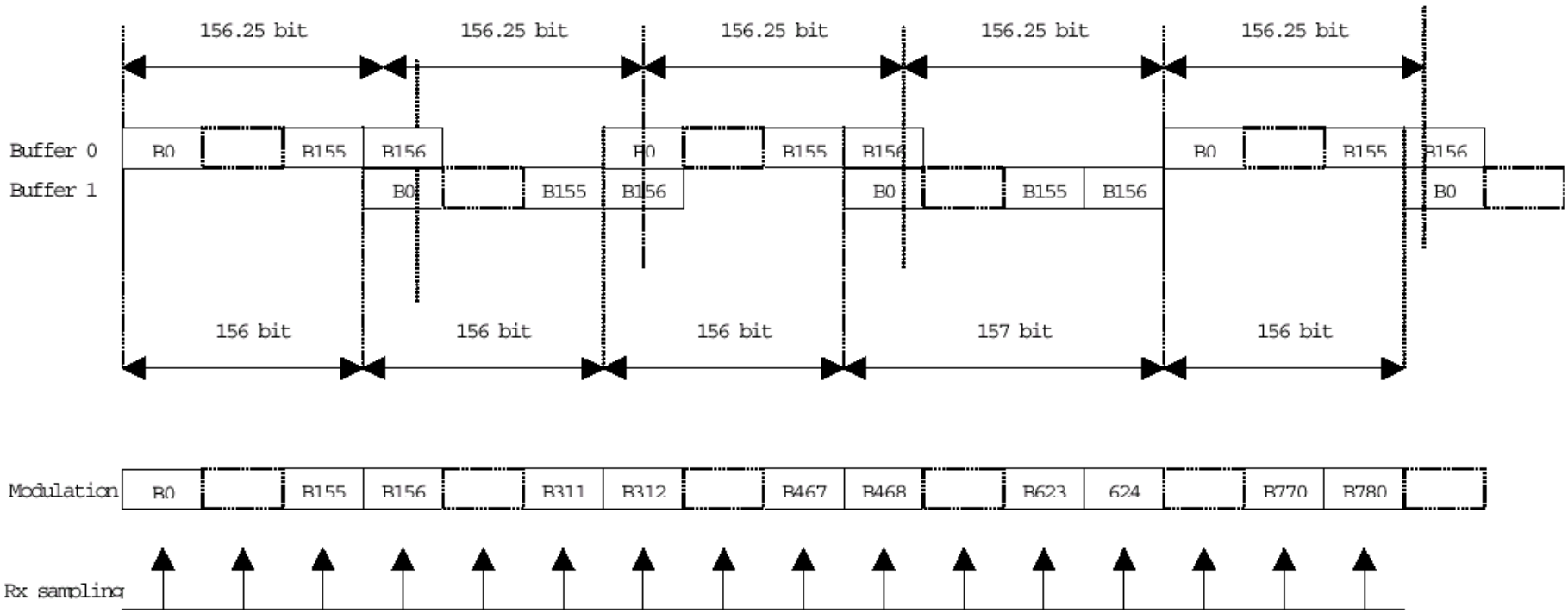
Typical sequence of burst transmission consists in :

Power on the base band uplink.
Perform an offset calibration (not mandatory)
Modulate the content of the burst buffer.

Baseband Uplink Timing



Multislot Modulation Scheme

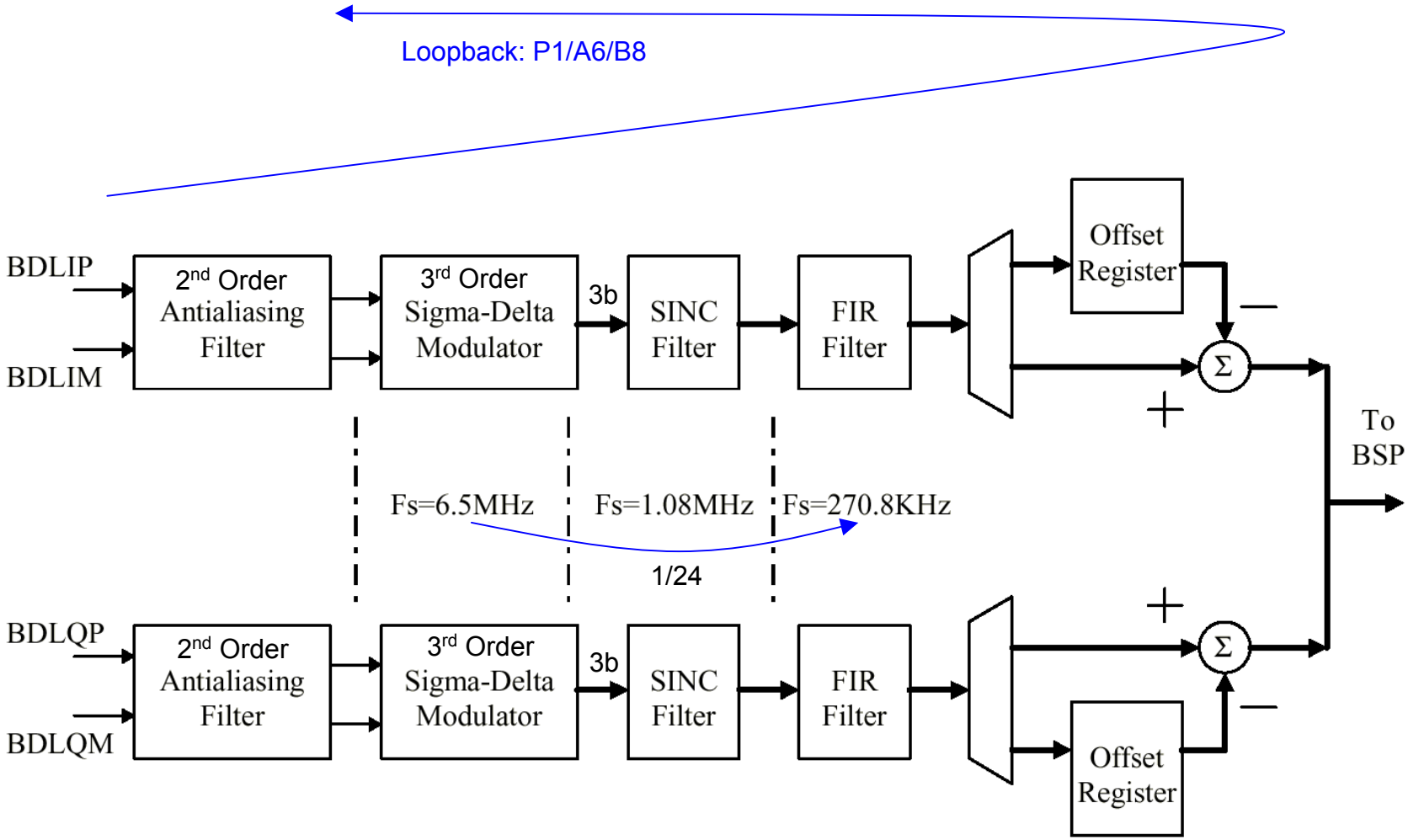


Downlink General Description

First stage of the downlink path is a continuous-time second-order antialasing filter that prevents aliasing of out of band frequency components due to sampling in the ADC.

The antialiasing filter is followed by a third-order sigma-delta modulator that performs A/D conversion at a sampling rate of 6.5 MHz.. The ADC provides 3-bit words that are fed to a digital filter that performs the decimation by a ration of 24 to lower the sampling rate to 270.8 Khz and the channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM specification.

Baseband Downlink

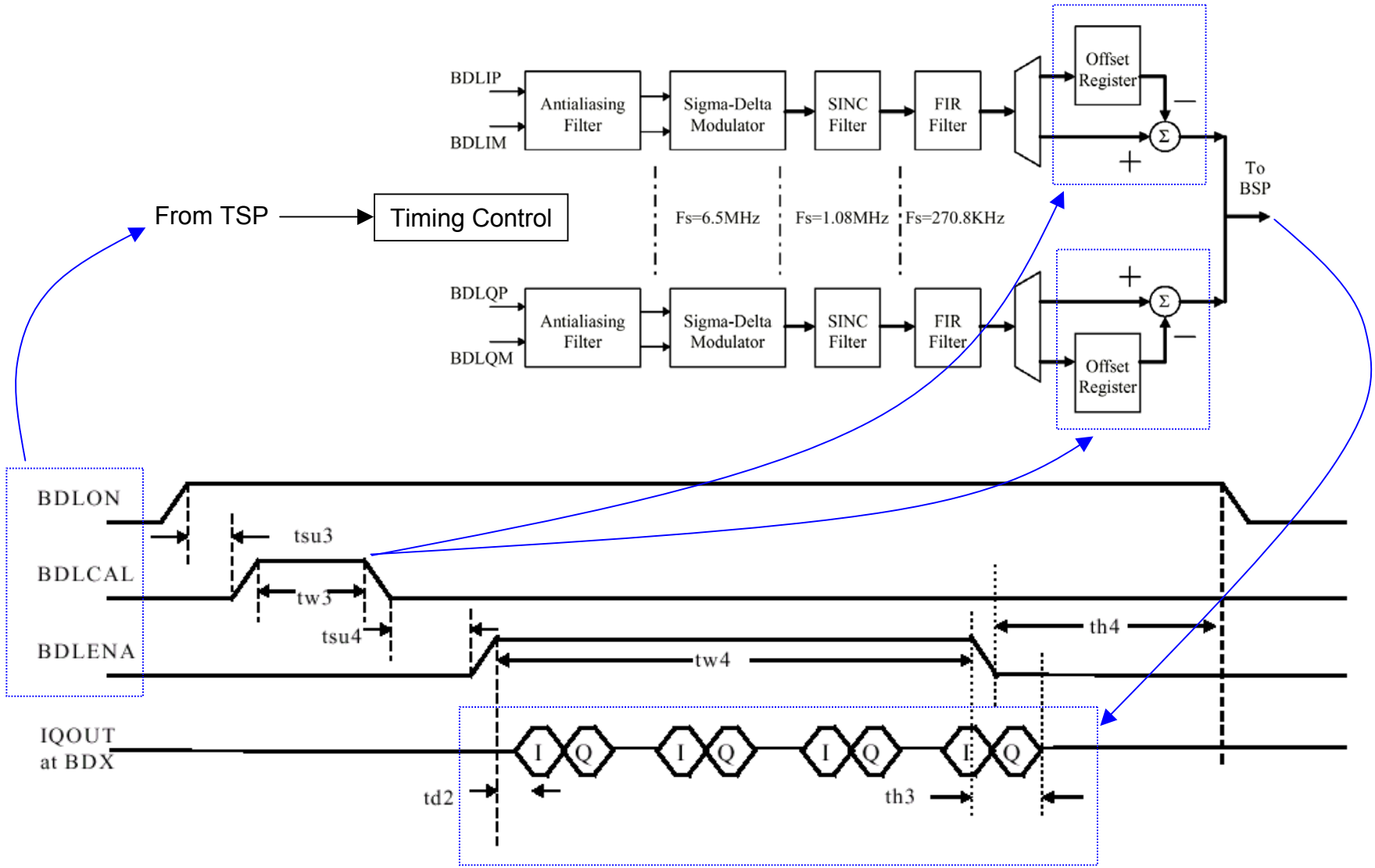


Sequence of burst Reception

Typical sequence of burst reception consists in :

Power on the baseband downlink.
Perform an offset calibration (not mandatory)
Convert and filter the I and Q component and transmit digital samples.

Baseband Downlink Timing



Iota BB&VB Codec

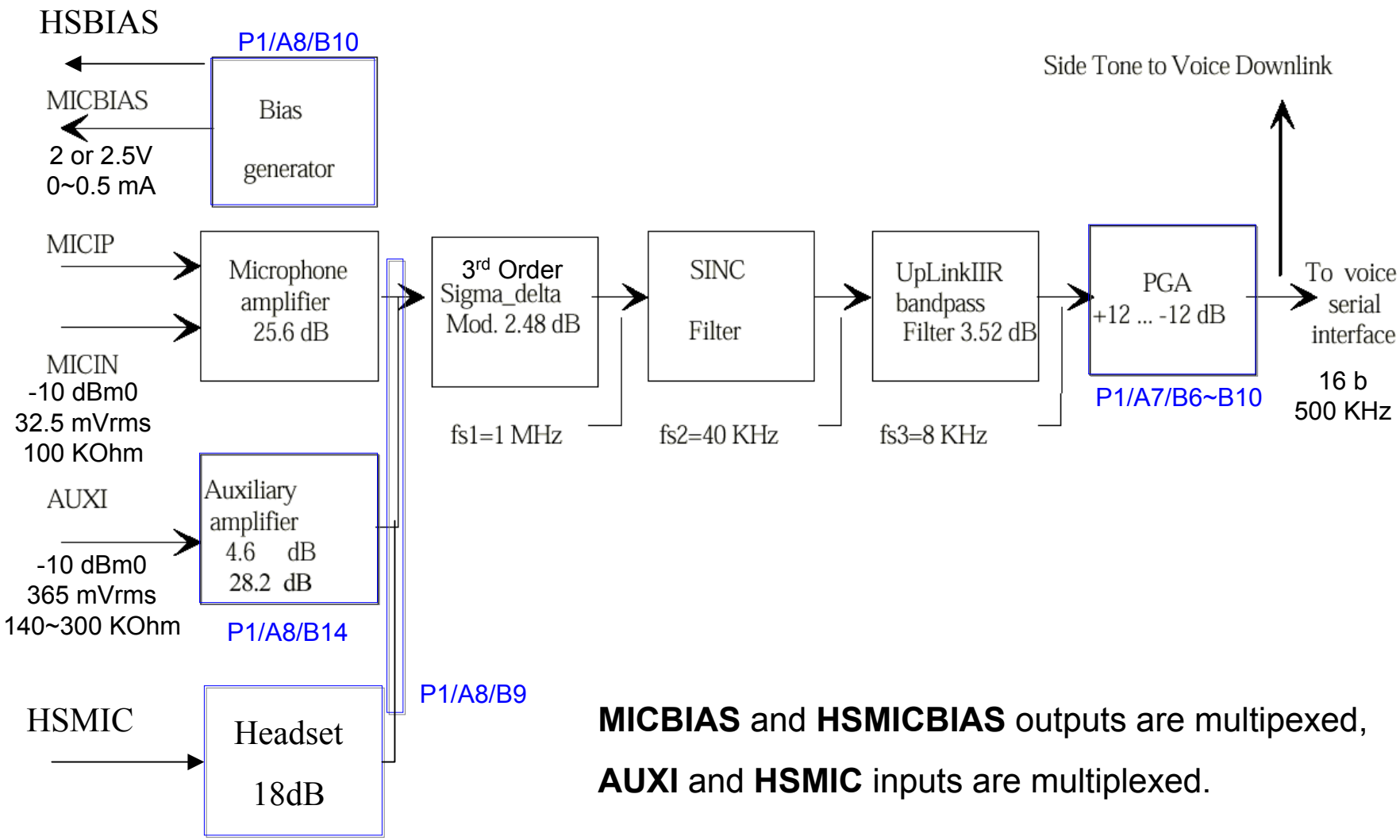
- Base Band Codec
- Voice Band Codec

VBC General Description

The voice coder/decoder (codec) circuitry processes analog audio components in the uplink path and applies this signal to the voice signal interface for eventual baseband modulation.

In the downlink path, the codec circuitry changes voice-component data received from the voice serial interface into analog audio.

Voice Band Uplink Path

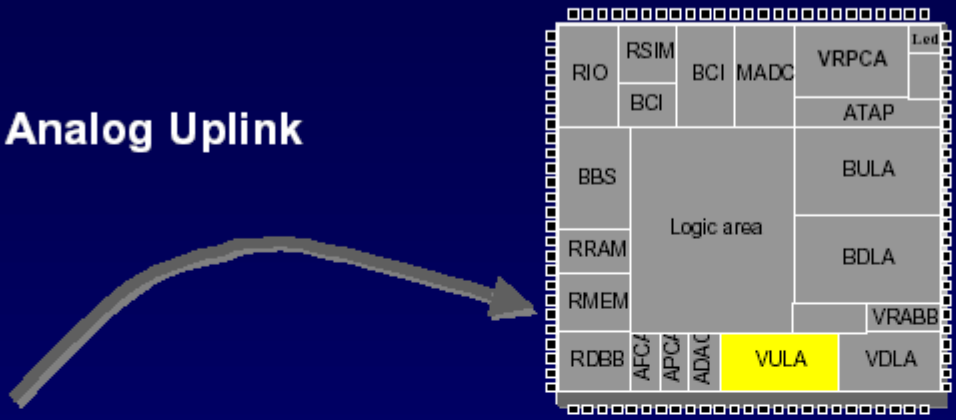


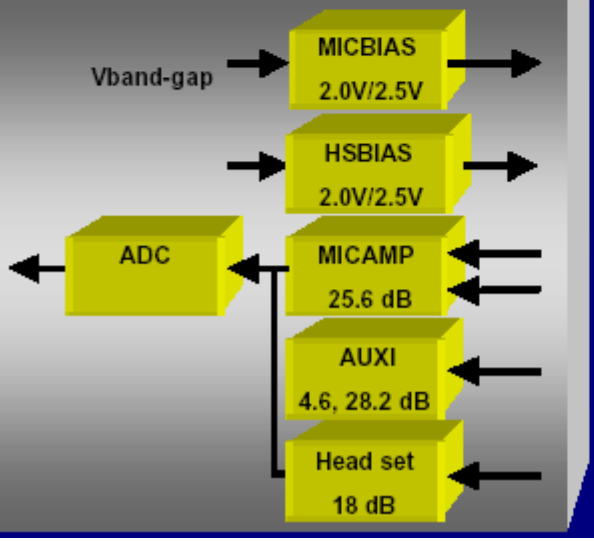
MICBIAS and **HSMICBIAS** outputs are multipexed,

AUXI and **HSMIC** inputs are multiplexed.

Voiceband Codec 1

- Analog Uplink





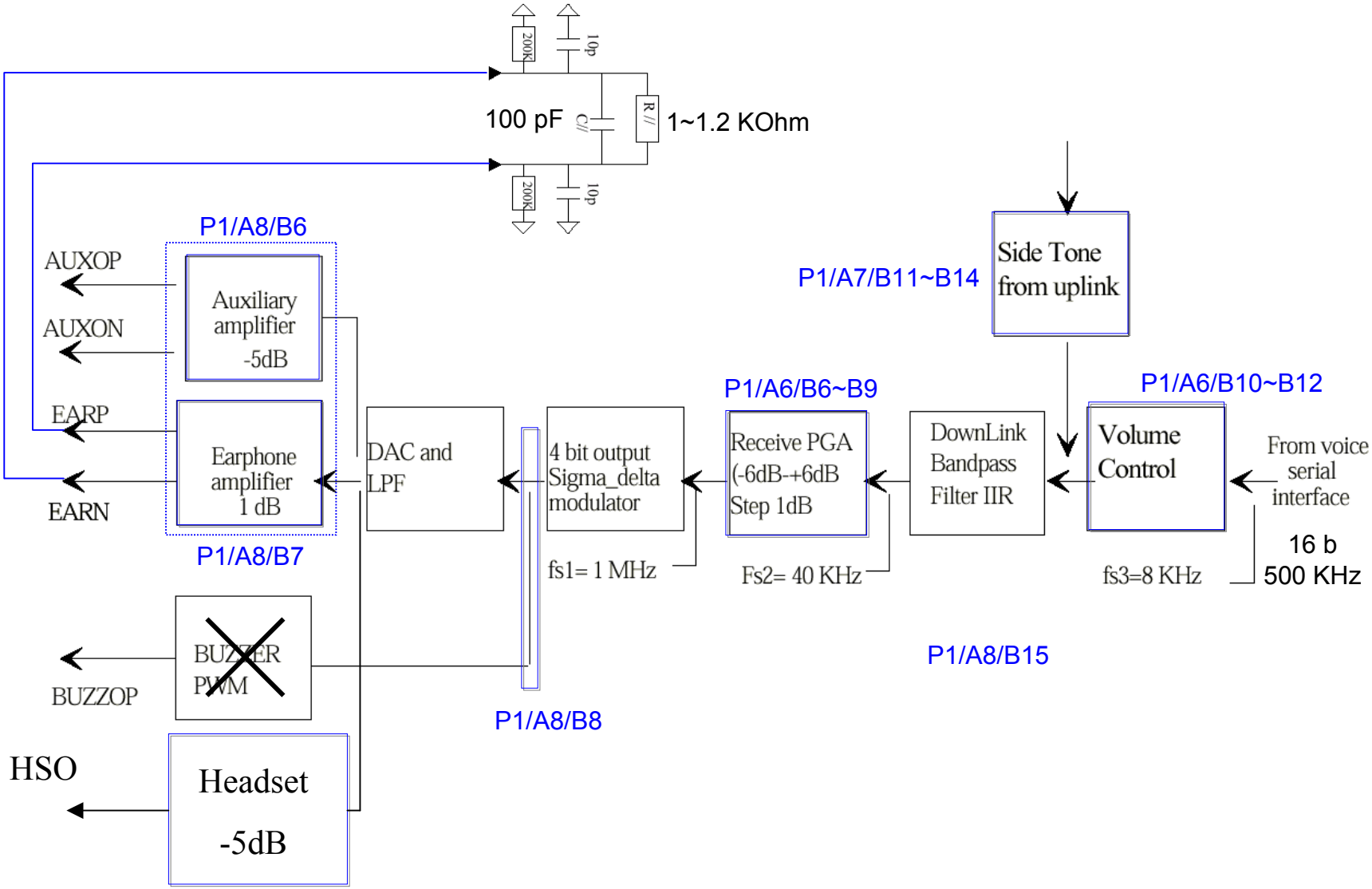
Performances.

- 13 bit dynamic range
- Limited by resistors thermal noise .

VUL Features.

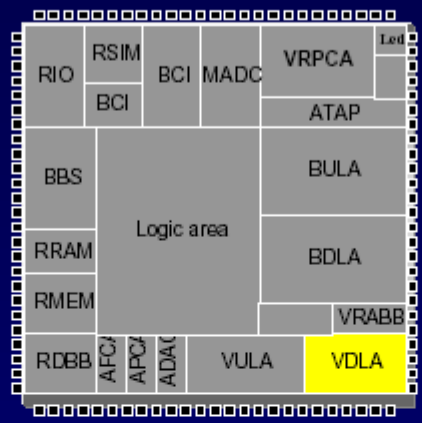
- **Microphone amplifier**
  - Differential inputs.
  - 25.6 dB gain.
- **Auxiliary input**
  - Single ended input.
  - Programmable gain 4.6dB or 28 dB.
- **Headset input**
  - Single ended input.
  - Fix gain 18dB
- **Microphone bias output.**
  - Programmable 2.0V or 2.5V DC output.
- **Headset bias output.**
  - Programmable 2.0V or 2.5V DC output
- **ADC 3rd ΣΔ**
  - 2nd order + 1st order

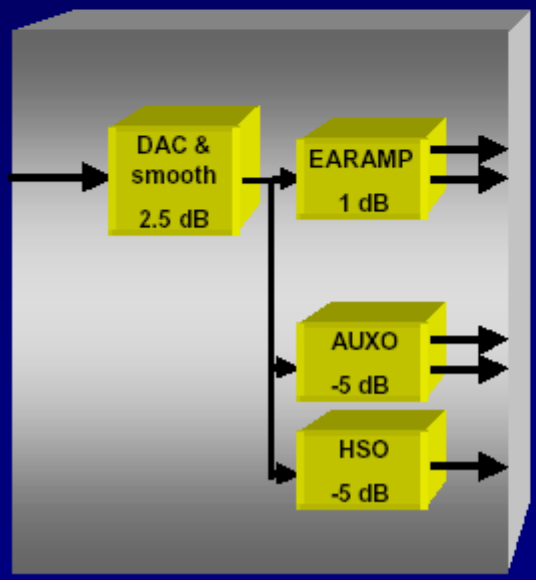
Voice Band Downlink Path



Voiceband Codec 2

- Analog downlink





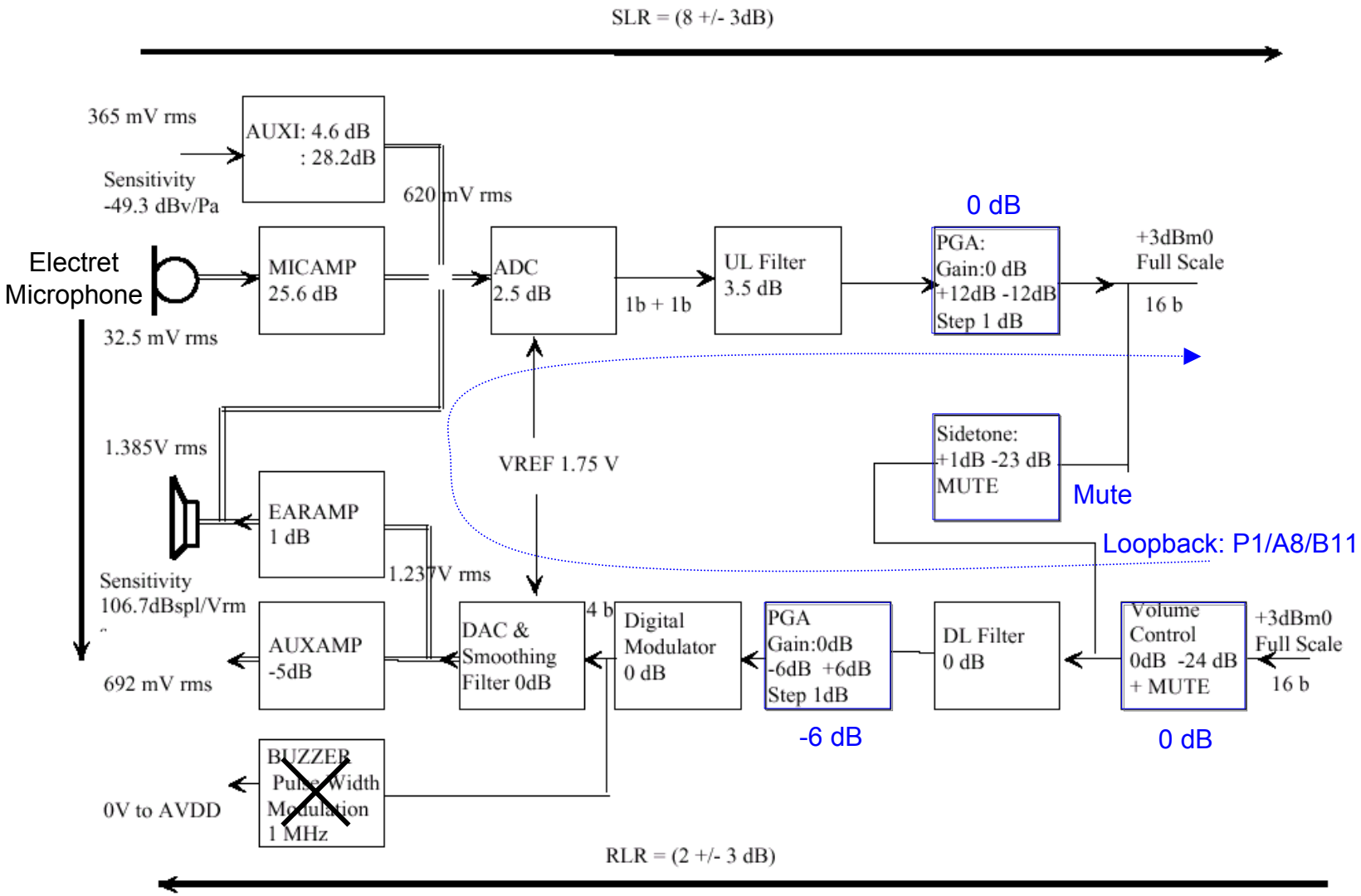
Performances.

- Target 15 bit dynamic range
- Depending on volume control gain setting.

VDL Features.

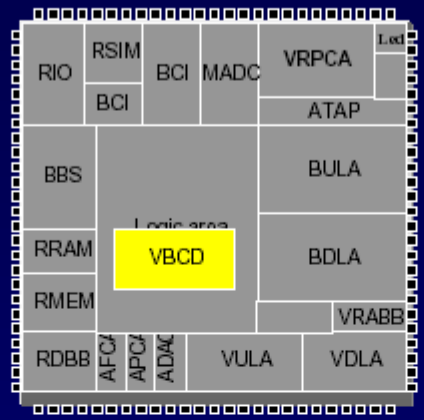
- **Earphone amplifier**
  - Differential outputs.
  - 120 Ohms load full swing(3.9V typ).
  - 32 Ohms load half swing (1.5V typ) capability.
- **Auxiliary output**
  - Differential outputs.
  - 1K Ohms load at 3.9V swing
- **Headset output**
  - Single ended output.
  - 32 Ohms load at 1.96V swing
- **DAC 2^{nd} ΣΔ**
  - 2^{nd} order multi-bit (4bit /t9 level) architecture
  - Dynamic elements matching structure.

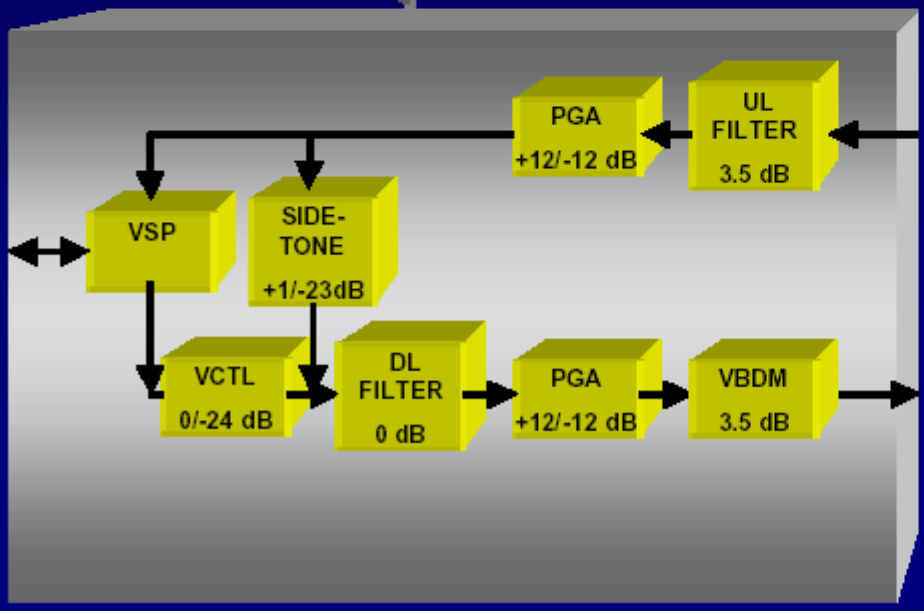
Voice Band Path



Voiceband Codec 3

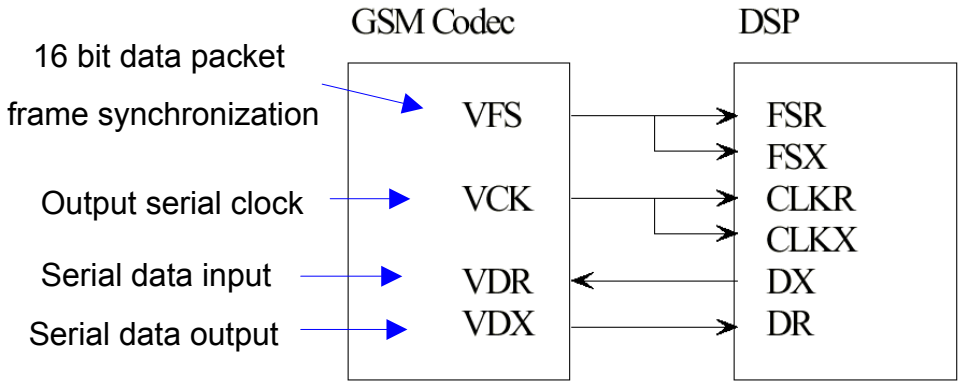
- Digital block
  - Digital filter
  - Digital modulator
  - Serial interface

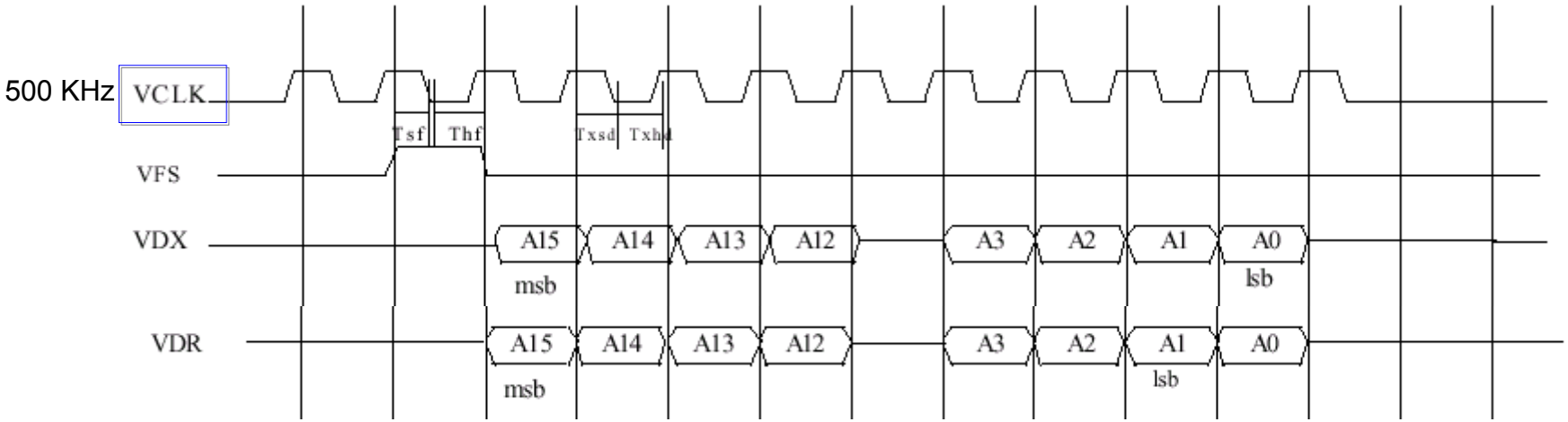




- Features.
  - Digital filter
    - Voice Band-pass filtering (300Hz / 3400Hz).
    - Uplink PGA(+12dB to -12dB by 1dB Step) .{SLR}
    - Downlink PGA(-6Db to + 6 dB by 1dB step).{RLR}
    - Sidetone PGA (+1dB to -23 dB) {STMR}
    - Volume control (0dB to -24 dB)
  - Voice Serial Port
    - 16 bit / 500KHZ transfer.

Voice Band Serial Interface





Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Port
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

Iota Public Module

- Clock Generator
- Test Access Port
- Monitoring ADC
- Internal Bus and Interrupt Controller
- Auxiliary DAC
- Led drivers

Clock Generator

- Source:
  - Squared digital system master clock, CK13M(derived from DBB).
  - VRPC Low power clock, CK32K(derived from RTC of DBB).

- Target:
  - Serial Interfaces and the Bus Controller: CKUSP (13MHz) , CKIBIC (13MHz) , CKBSP (13MHz) , CKTSP (13 MHz).
  - Baseband Codec: CKBDL (13 MHz) and CKBUL (4.3 MHz).
  - Auxiliary function: CKMADC (13 MHz), CKAPC (13 MHz) and CKAFC (4.3 MHz).
  - Voice Codec: CKVBC (13 MHz).

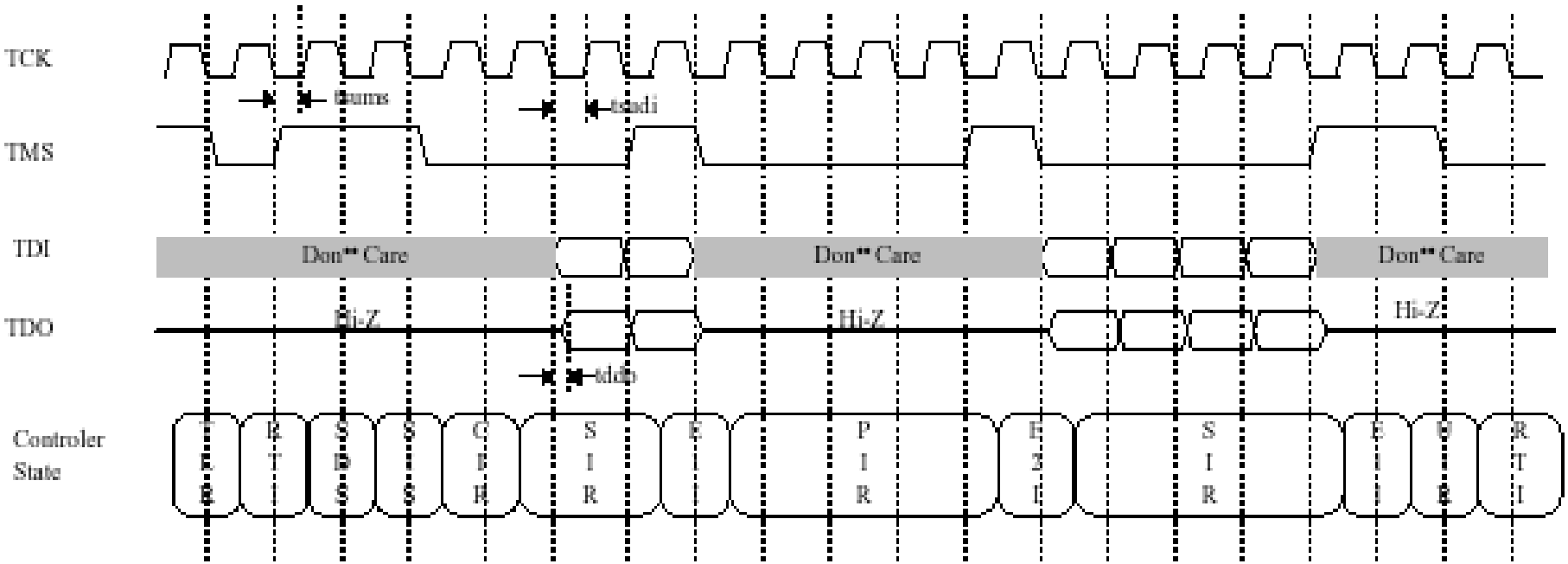
Iota Public Module

- Clock Generator
- Test Access Port
- Monitoring ADC
- Internal Bus and Interrupt Controller
- Auxiliary DAC
- Led drivers

TAP Overview

- Meets JTAG test standard (IEEE 1131.1)
- Allows JTAG instructions debug/test modes
- 4 pins: TDO, TDI, TCK, TMS
  - TCK is the test clock signal
  - TMS is the test mode select signal
  - TDI is the scan path input
  - TDO is the scan path output

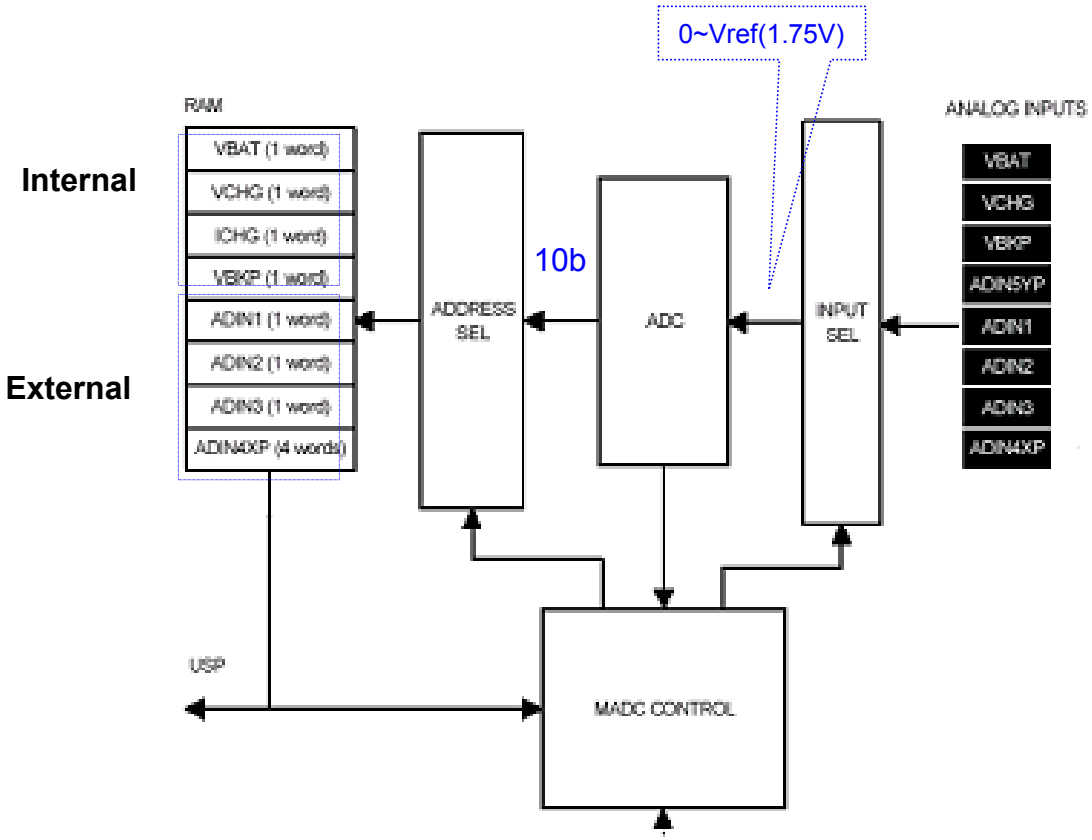
TAP Timing


TCK
TMS
TDI
TDO
Controler State
tsmtms
tsudi
tddo
Don** Care
Don** Care
Don** Care
Hi-Z
Hi-Z
Hi-Z
TLR
RTI
SDS
SDS
CDR
SIR
EI1
PIR
EI2
SIR
EI1
EI2
RTI

Nausica Public Module

- Clock Generator
- Test Access Port
- Monitoring ADC
- Internal Bus and Interrupt Controller
- Auxiliary DAC
- Led drivers

MADC Functionality



Internal:

MB voltage

BB voltage

Charger voltage

Charger current

External:

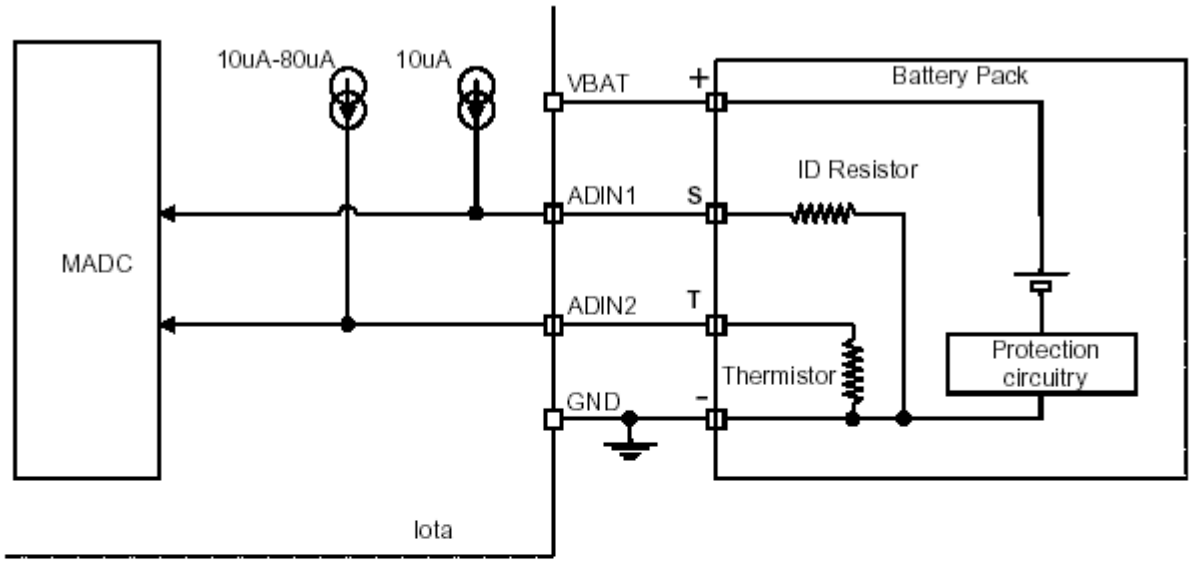
ADIN1: MB ID

ADIN2: MB Temp

ADIN3: NC

ADIN4: RF Temp

MADC Functionality



SW set up for a temperature measurement:

- Enable the MADC module writing to logic 1 the MADCS bit in TOGBR1 register.
- Configure the ADIN2 source current to deliver the appropriate current value programming the THSENS[2..0] bits in the BCICTL1 register.
- Configure the MADC to convert the ADIN2input.
- Enable the ADIN2 bias current writing a logic 1 into THEN bit BCICTL1 register
- Start the MADC conversion executing a dummy write in one of the result registers (VBATREG as example).
- Wait for the end of conversion polling the ADCBUSY flag in ADC_STATUS register.
- Read conversion result in ADIN2 register.

Iota Public Module

- Clock Generator
- Test Access Port
- Monitoring ADC
- Internal Bus and Interrupt Controller
- Auxiliary DAC
- Led drivers

IBIC

Bus controller purpose is to manage access to internal bus by BSP and USP serial ports.

Rules

1/ If there is only one request, it is treated immediately regardless the source.

2/ If the two requests are seen by the Bus Controller as simultaneous, the USP request is treated first.

Interrupt Handling

There are several internal interrupt sources:

1. the under voltage control, **UVLO_IT**;
2. the Remote Power On : when the mobile is in switch ON mode (ON_NOFF set to 1) transition from 1->0 or 0->1 on ON_REM pin after debouncing confirmation generates an **ON_REM_IT**. Transition 1->0 is required to identify an accessory plug out. Transition 0->1 is required to identify an accessory plug in while the mobile is already in switch ON condition.

3. the battery charger in or out plug, **CHARGER_IT**;
4. the ADC end of conversion, **ADC_END_IT**;
5. the user pushes button on to off, **PUSH_OFF_IT**.

Interrupt Handling

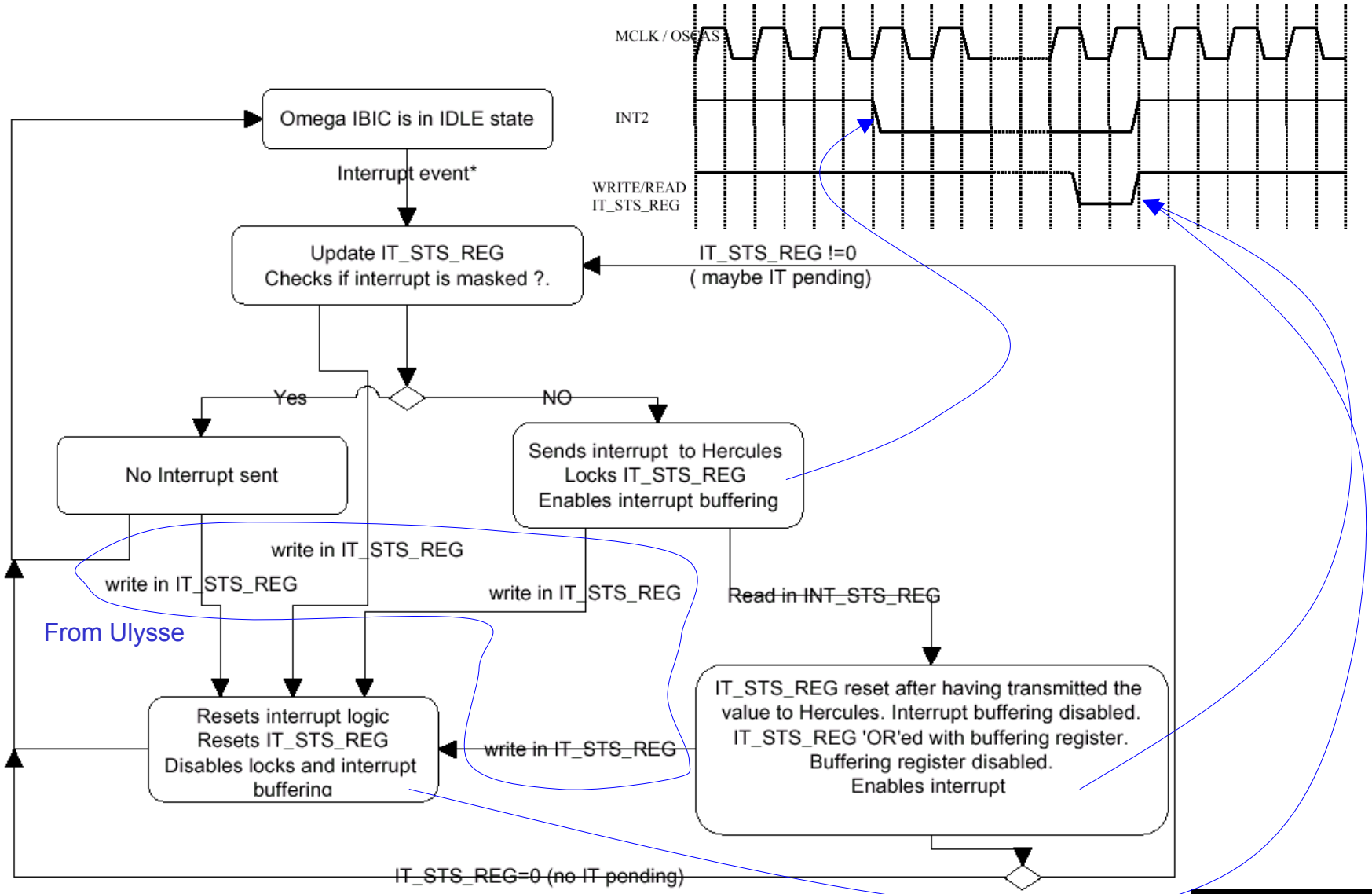
All these interrupts are reflected in (except case 1):

Interrupt Status Register **IT_STS_REG**,

And can be masked through the corresponding bits of :

Interrupt Mask Register **ITMASKREG**.

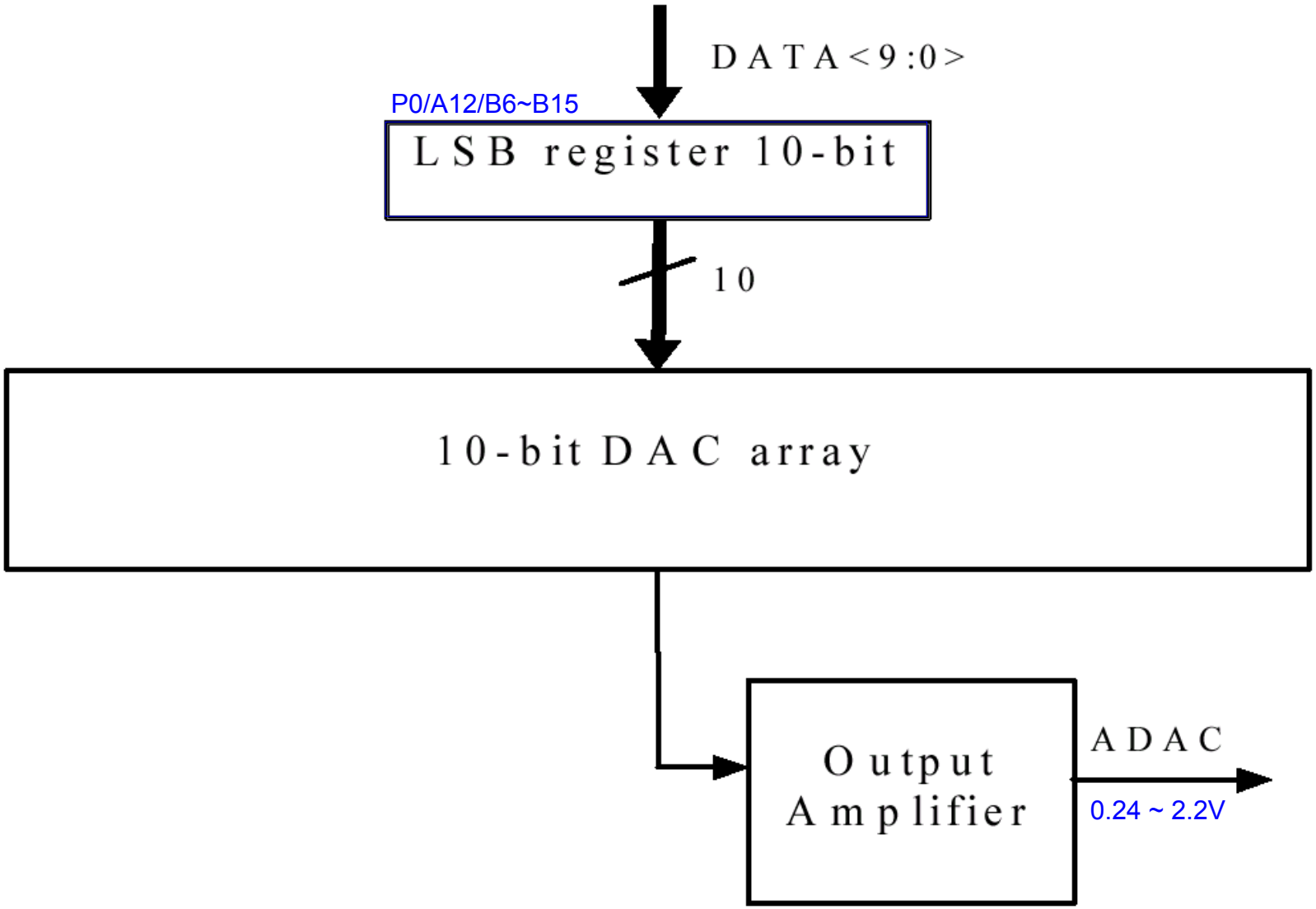
Internal Bus Interrupt Control Flow



Iota Public Module

- Clock Generator
- Test Access Port
- Monitoring ADC
- Internal Bus and Interrupt Controller
- Auxiliary DAC
- Led drivers

Auxiliary DAC

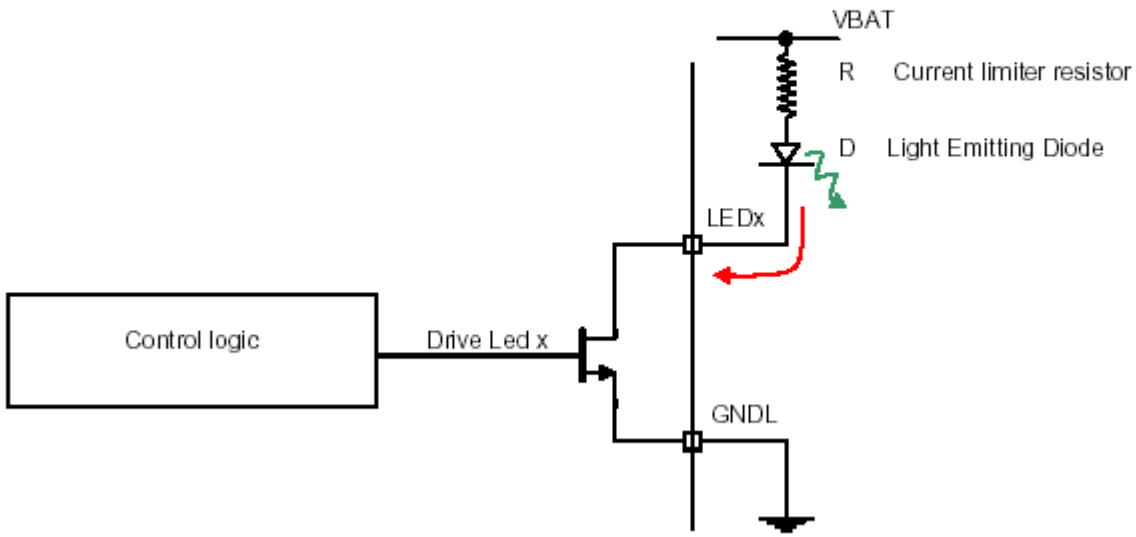


Iota Public Module

- ClocK Generator
- Test Access Port
- Monitoring ADC
- Internal Bus Controller
- Auxiliary DAC
- Led drivers

Led drivers

Pin name	Max Driven current	High level V	Low level V	Supply	Led function
LED A	10 mA	VBAT	0.4V	VBAT	Paging led
LED B	150 mA	VBAT	0.7V	VBAT	Back-light leds
LED C	10 mA	VCHG	0.4V	VCHG	Precharge indicator led



Led drivers

PWL(Calypso): LCD Backlight

LPG(Calypso): Blinking Indicator

LED-B(IOTA): Keypad Backlight

LED-A(IOTA): Paging Indicator

LED-C(IOTA): Precharge Indicator

Iota Overview

- Iota General Description
- Iota RF Control
- Iota Serial Port
- Iota Power Management
- Iota BB&VB Codec
- Iota Public Module

Iota Overview

Thank You!