Rita Intro

July,2003

Texas Instruments Shanghai

Wireless Customer Integration & Design Center

Agenda

- **Rita introduction**
  1. Rita architecture
  2. Receiver
  3. Transmitter
  4. Synthesizer
  5.Regulator
- **RF-BB interface**
  1. RF-BB connection
  2. RF controlling by BB
- **RF-SW programming and control**
  Rita registers introduction
- **Q&A**

Rita introduction

1. Rita architecture

2. Receiver

3. Transmitter

4. Synthesizer

5.Regulator

Migrating from CLARA to RITA

Clara

- Triple band
- 64Pin,TQFP64,12*12mm
- Need tank circuits
- Need 2 external VCOs
- Need external VCXO

Rita

- Quad band
- 48Pin,QFN48,7*7mm
- Fully-integrated VCO, no need tank circuits
- Including loop filter and VCO
- Including a 26MHz VCXO with external varactor and crystal

RITA GSM-GPRS 850/900/1800/1900, RF single chip

Technology

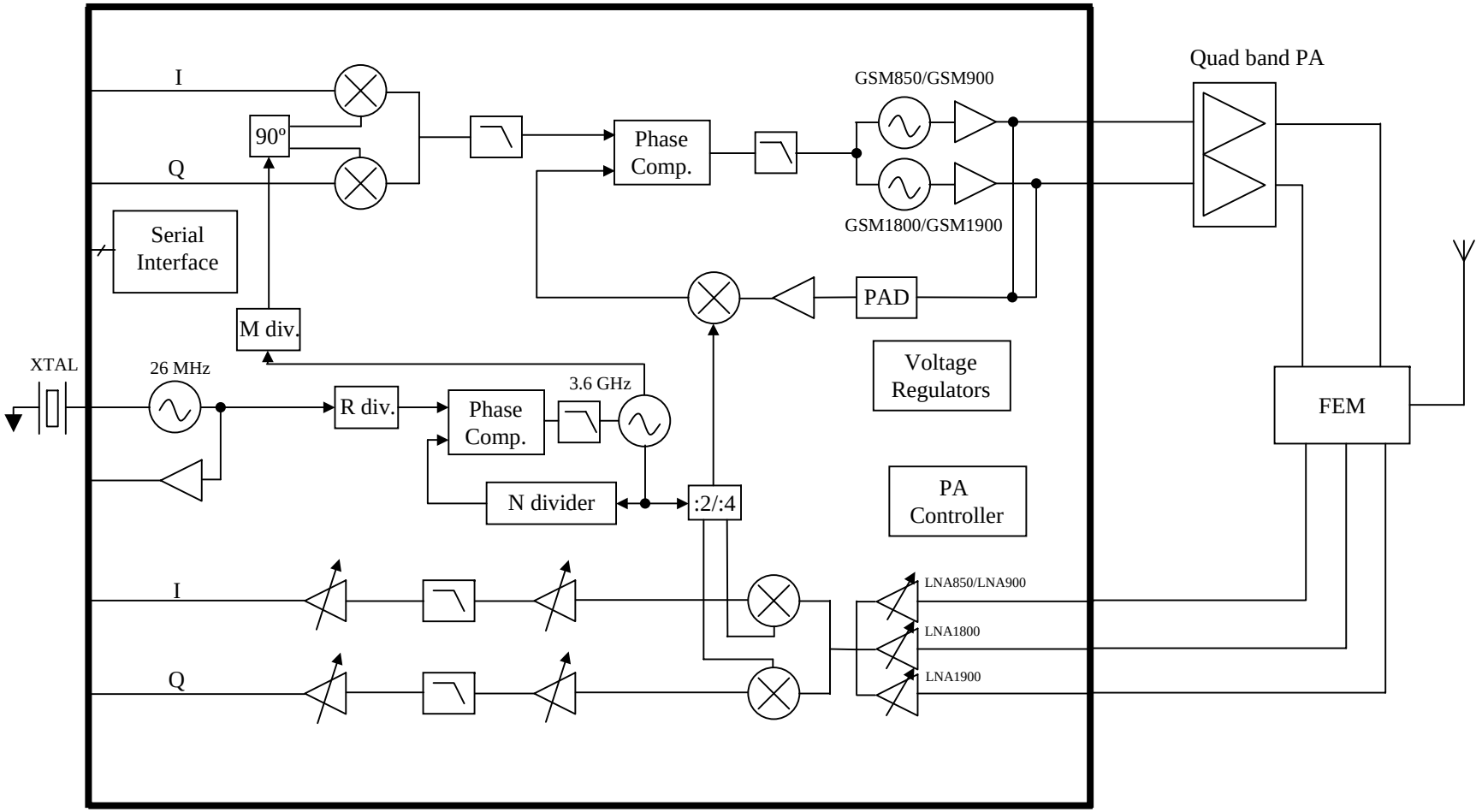
- RFSIGE1

- Direct Conversion Receiver
  - GSM850
  - EGSM
  - DCS
  - PCS
- Transmitter using Offset PLL with on chip filter
- 1 synthesizer
- 4 fully Integrated VCO
- 3 on chip regulators
- PA Controller
- 3 Wire Serial Interface
- VCXO

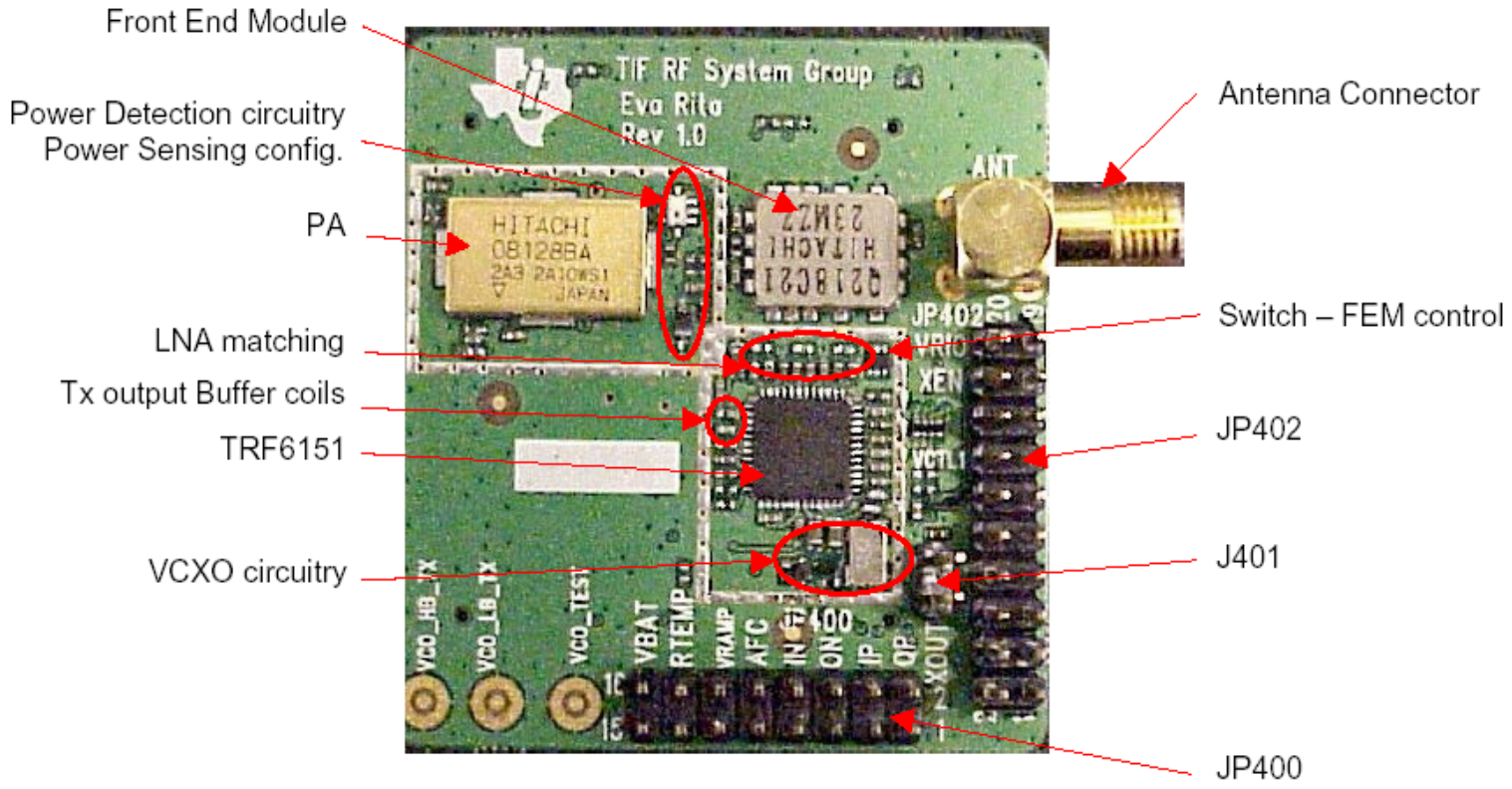
It is compatible with Iota(TWL3014) and Syren (TWL3016) ABB chips and with Calypso, Calypso20G2, Calypso-plus DBB chips.

- Area 14 sqrmm
- 48 pins QFN
- 44110 components
- 20250 Signals
- 3 Power Supply Domains
- 1 Digital Serial Port

Architecture

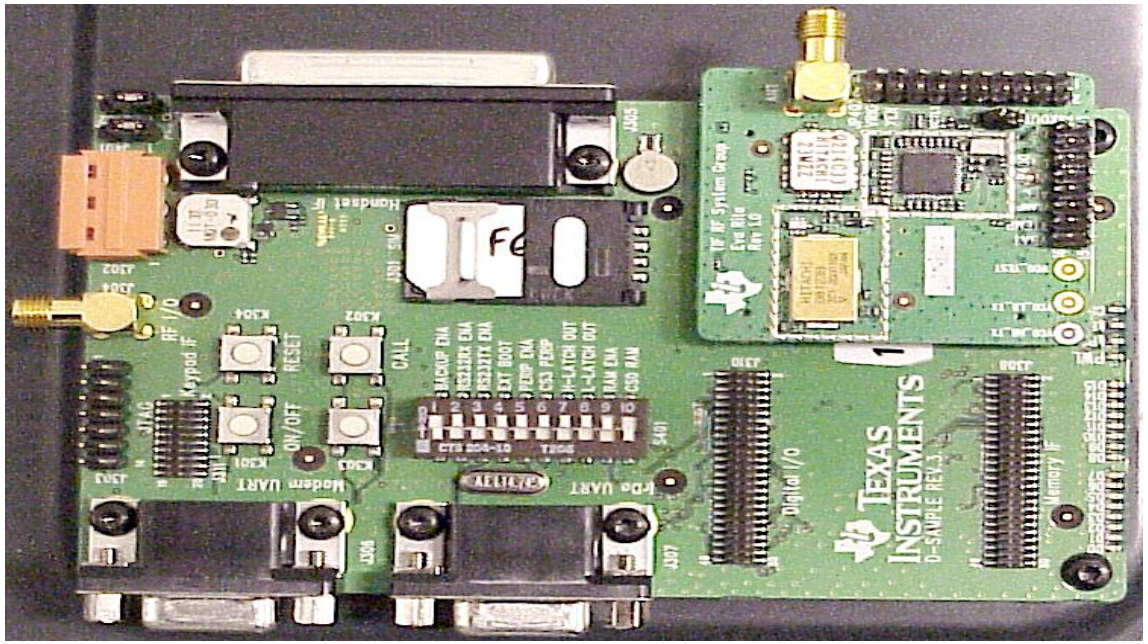


Rita EVM



Can be plugged to: Modified D-Sample

Modified D-sample



Modifications are to be applied to D-Samples to handle EvaRita

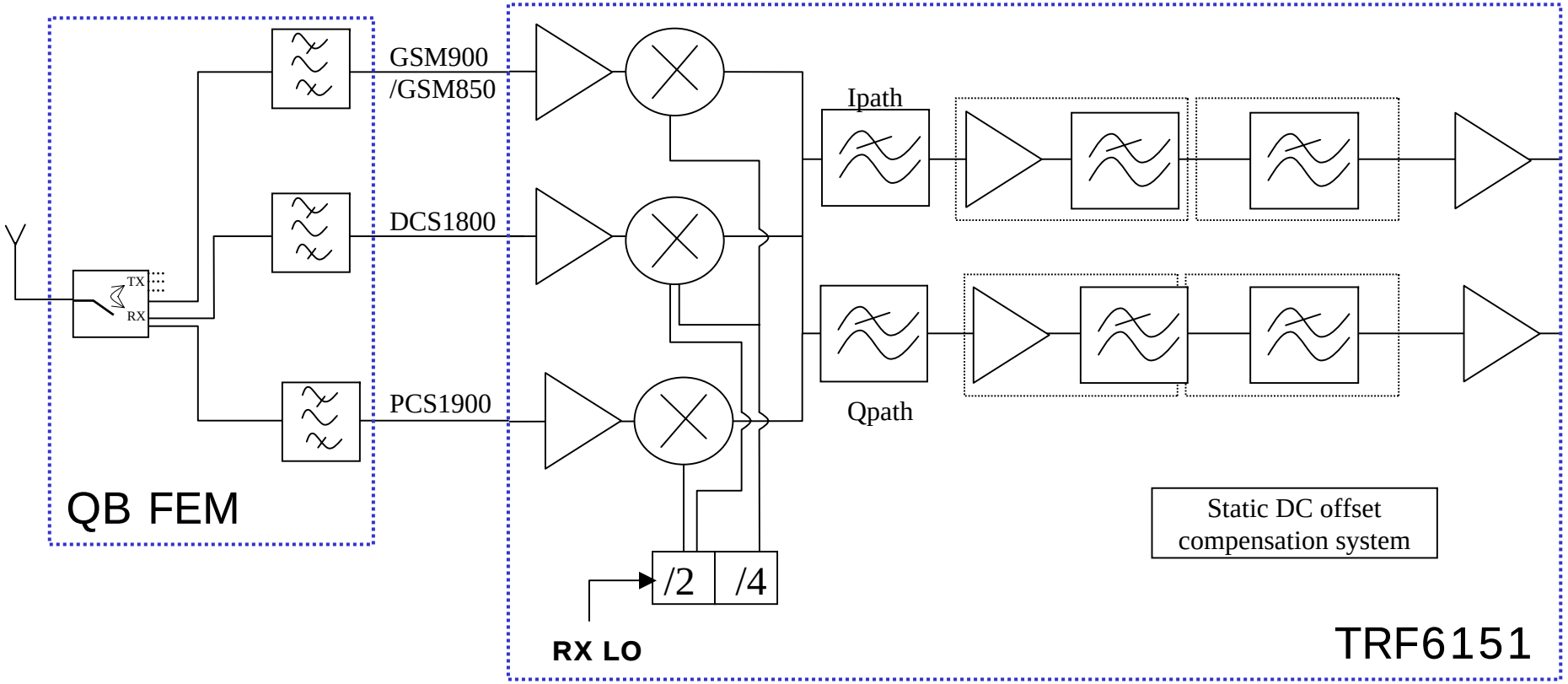
Modified D-Sample is dedicated to EvaRita

Corresponds to Calypso/Iota/Rita TI chipset

Used to emulate EvaRita in real conditions (GSM TDMA)

Useful to run tests close to the ETSI spec. requirements.

Receiver



- Direct conversion receiver
- Quad band GSM850+EGSM + DCS + PCS

Receiver

Receive section:

- - three LNA(LNAGSM/LNADCS/LNAPCS) with switchable gain
- - three quadrature demodulators for GSM900/GSM850 (MIXGSM),DCS1800 (MIXDCS) and PCS1900 (MIXPCS) bands with switchable gain
- - two base-band amplifiers with digitally programmable gain
- - two fully integrated base-band channel filters.
- - two DC offset compensation systems
- - a divider by 4 for the LO generation in GSM900 and GSM850 in order to minimize the DC offset generated by self mixing and the LO re-radiation
- - a divider by 2 for the LO generation in DCS1800 and PCS1900 in order to minimize the DC offset generated by self-mixing and the LO re-radiation.

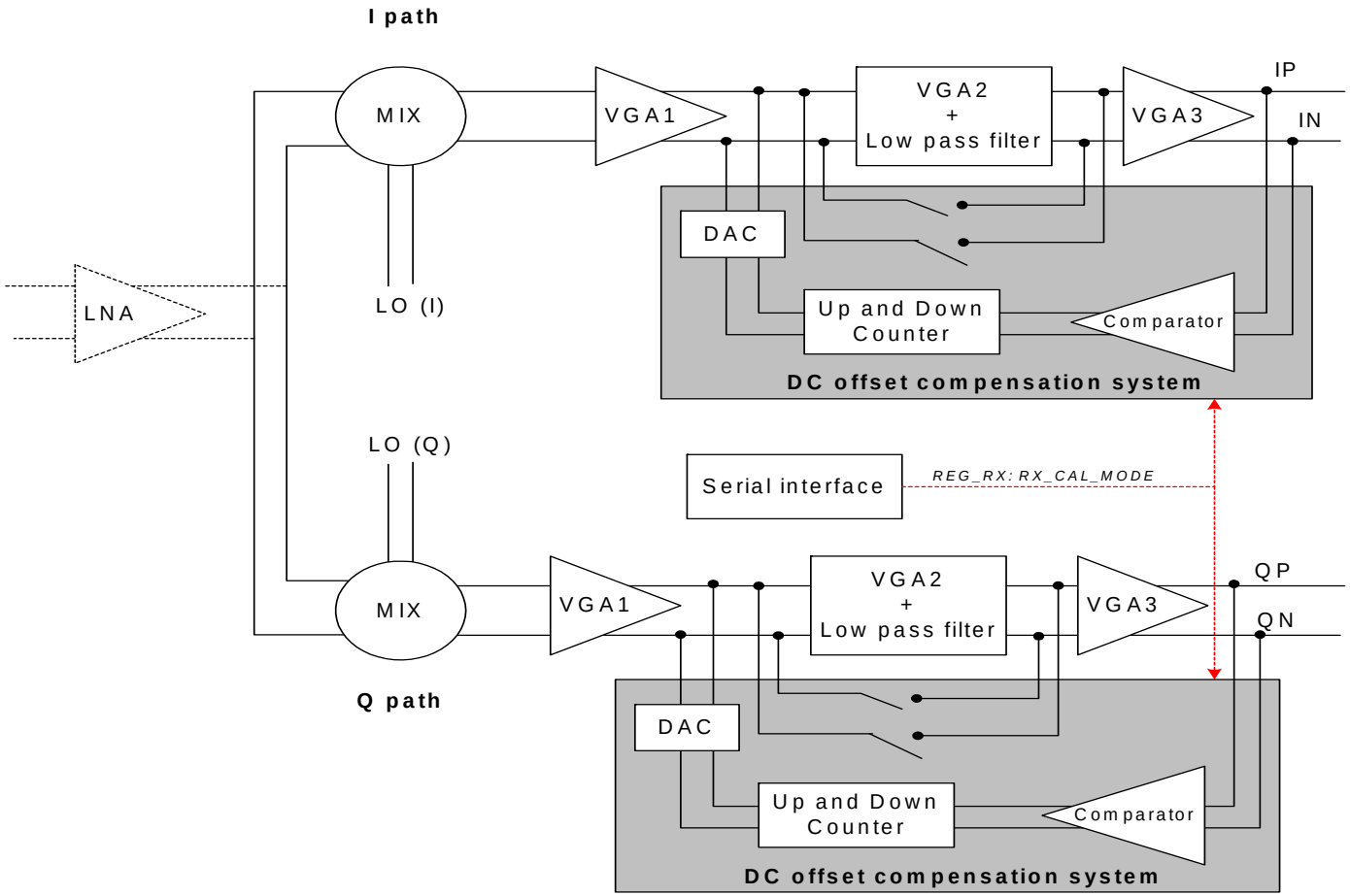
Receiver Performance

RECEIVER

Global performances

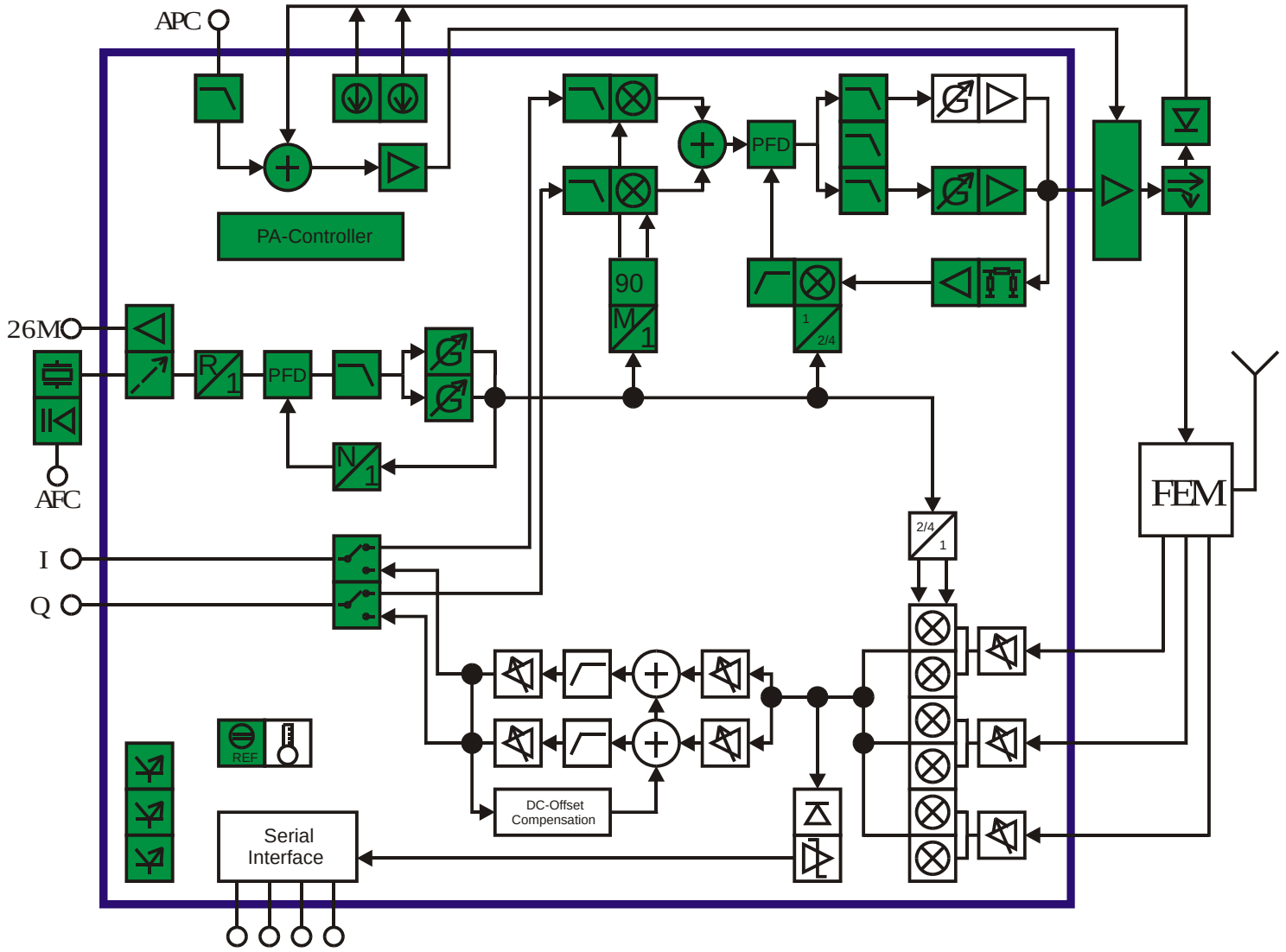
RF input frequency	LNAGSMN/P pins		869	-	960	MHz
	LNADCSN/P pins		1805	-	1880	MHz
	LNAPCSN/P pins		1930	-	1990	MHz
Balanced RF input impedance	LNAGSMN/P, LNADCSN/P or LNAPCSN/P pins		-	100	-	Ω
RF input return loss	LNAGSMN/P, LNADCSN/P or LNAPCSN/P pins Receiver gain = G_HIGH or G_MID1		-	-	-10	dB
	LNAGSMN/P, LNADCSN/P or LNAPCSN/P pins Receiver gain = G_MID2 or G_LOW		-	-	-4	dB
Voltage gain [29]	All bands Front end and VGA high gain mode	G_HIGH	63	66	69	dB
	All bands Front end in intermediate gain mode and VGA in high gain mode	G_MID1	57	60	63	dB
	All bands Front end in low gain mode and VGA in high gain mode	G_MID2	43	46	49	dB
	All bands Front end and VGA in low gain mode	G_LOW	17	20	23	dB
Noise figure [30]	LNAGSMN/P pins; G=G_HIGH GSM900 band [925,960Mhz]		-	-	5	dB
	LNAGSMN/P pins[31]; G=G_HIGH GSM850 band [869,894Mhz]		-	-	5.2	dB
	LNADCSN/P pins; G=G_HIGH DCS band [1805,1880Mhz]		-	-	5	dB
	LNAPCSN/P pins; G=G_HIGH PCS band [1930,1990Mhz]		-	-	5	dB
	All bands; G= G_MID2		-	-	20.8	dB
Input 1dB compression point	All bands Gain = G_HIGH		-50	-	-	dBm
	GSM850-GSM900 bands G= G_LOW		-19.5	-	-	dBm
	DCS1800 – PCS1900 bands G= G_LOW		-25	-	-	dBm
Input 3rd order intercept point	All bands Gain = G_HIGH [32]		-20	-18	-	dBm

DC offset compensation



- On both I and Q paths, a comparator evaluates the DC offset at receiver output:
- If a positive DC offset is detected, the Up and down counter increments the DCO_Loop_register#1.If a negative DC offset is detected, the Up and down counter decrements the DCO_Loop_register#1.
- The content of DCO_Loop_register#1 is converted to an analog value by the 8-bit DAC:compensation is done at the input of the 2nd stage of the variable gain amplifier and DC offset decreases.
- This compensation circuit acts as a closed loop: As long as a DC offset remains at the receiver output, the DAC reduces the DC offset at the demodulator output.

Transmitter



- Transmit section:
- - an offset PLL with post IQ modulator and post offset mixer filters fully integrated on chip
- - two TX VCOs fully integrated on chip
- - a TX loop filter fully integrated on chip
- - a divider by 4 for the LO generation in GSM900 and GSM850
- - a divider by 2 for the LO generation in DCS1800 and PCS1900
- - a programmable M divider for the IF generation
- - a power amplifier controller including all the functions required to design a power sensing control loop except the sensing diodes

Tx performance

TRANSMITTER

Transmitter inputs

I/Q inputs common mode voltage			1.215	1.35	1.485	V
I/Q inputs voltage swing	Single ended		0.44	0.47	0.49	Vpp
I/Q inputs resistance	Differential ended		10			kO
I/Q inputs capacitance	Differential ended				25	pF

Low Band Output

Dedicated to GSM850 and E-GSM900

GMSK modulated signal applied at the IQ inputs (unless otherwise specified)

Frequency range		f_{out}	824.2 to 914.8			MHz
Output impedance		Z_{out}		50		O
Output Return Loss					-10	dB
Output power level	into 50 O load	P_{out}	4	6	8	dBm
Phase error	Max. RMS phase error Max. Peak phase error				3 10	degree
TXVCOLB Pulling	VSWR= 2, all phases, open loop	PULL		tbd		MHz

Tx performance (cont.)

Spurious emissions[25]
Specification at the **antenna with the use of the TBD PA and the TBD FEM**

E-GSM 900

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-69	dBc
	from 1 GHz to 12.75 GHz				-63	dBc
	in the band [925 ~ 935 MHz]				-100	dBc
	in the band [935 ~ 960 MHz]				-112	dBc
	in the band [1805 ~ 1880 MHz]				-104	dBc
	in the bands [1900 ~1920 MHz], [1920 ~ 1980 MHz], [2010 ~ 2025 MHz] and [2110 ~ 2170 MHz]				-99	dBc

DCS 1800

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-66	dBc
	from 1 GHz to 12.75 GHz				-60	dBc
	in the band [925 ~ 935 MHz]				-97	dBc
	in the band [935 ~ 960 MHz]				-109	dBc
	in the band [1805 ~ 1880 MHz]				-101	dBc
	in the bands [1900 ~1920 MHz], [1920 ~ 1980 MHz], [2010 ~ 2025 MHz] and [2110 ~ 2170 MHz]				-96	dBc

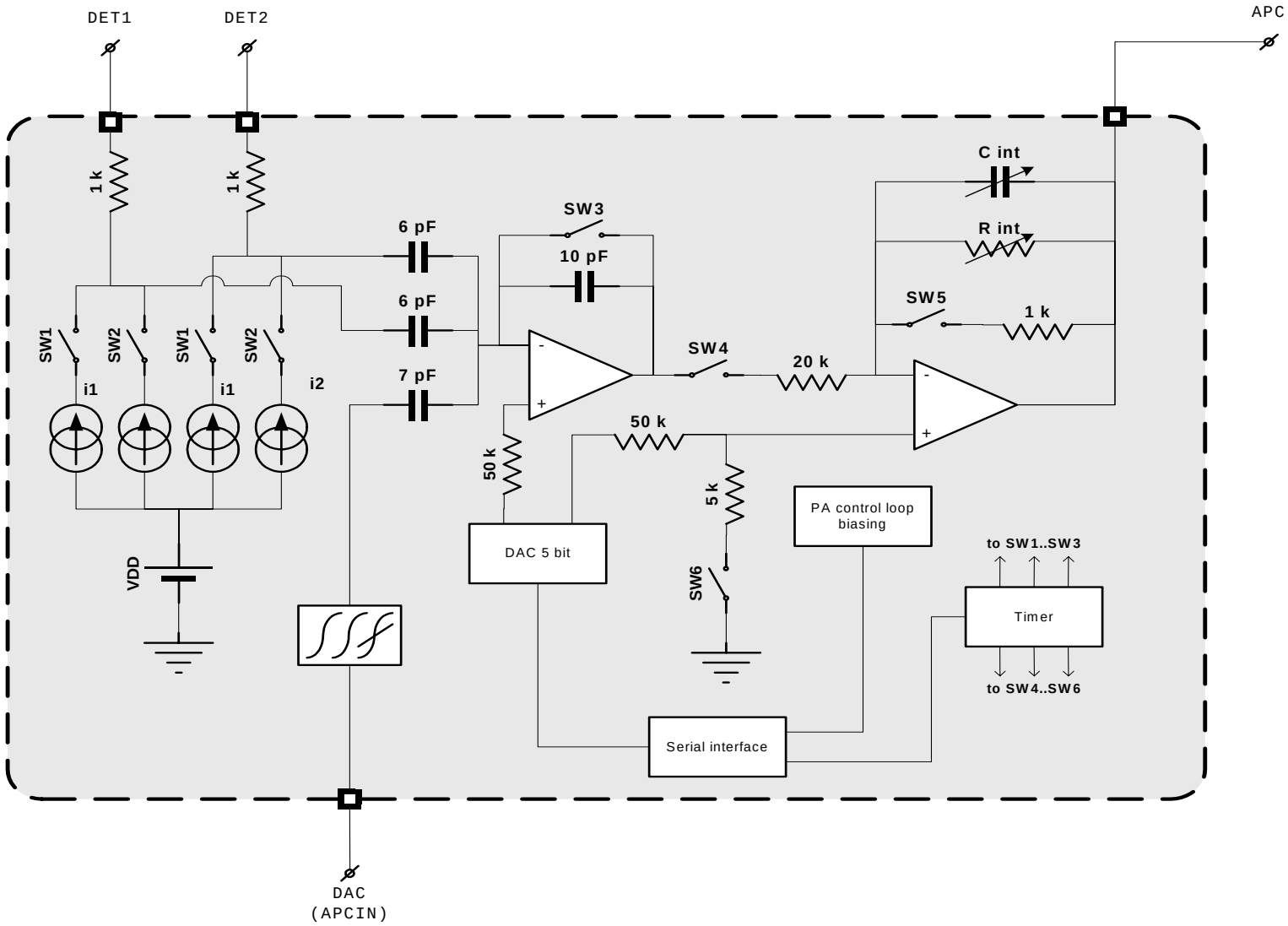
GSM 850

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-69	dBc
	from 1 GHz to 12.75 GHz				-63	dBc
	in the band [869 ~ 894 MHz]				-112	dBc
	in the band [1930 ~ 1990 MHz]				-104	dBc

PCS 1900

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-66	dBc
	from 1 GHz to 12.75 GHz				-60	dBc
	in the band [869 ~ 894 MHz]				-109	dBc
	in the band [1930 ~ 1990 MHz]				-101	dBc

PA Controller



PA controller register

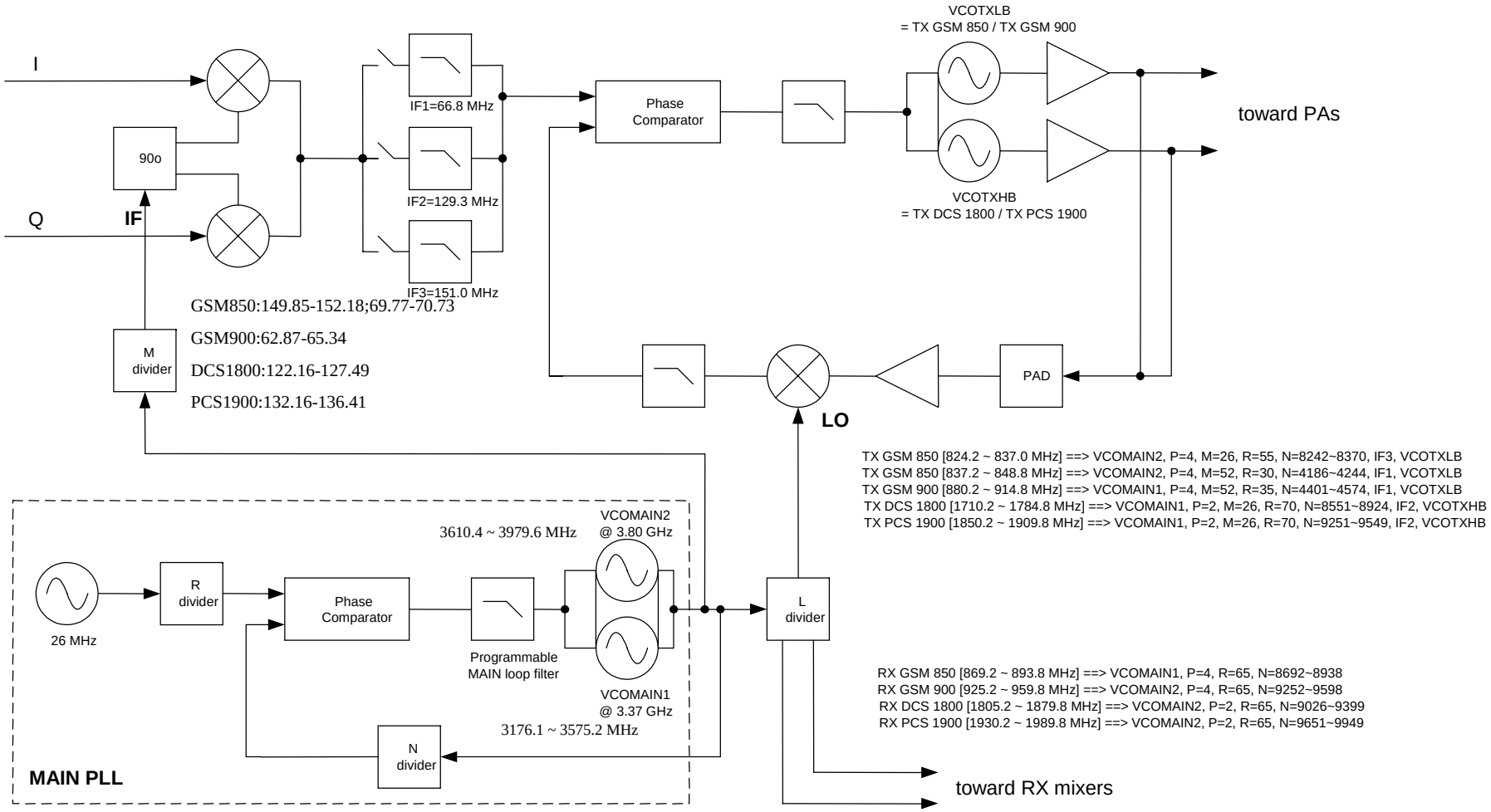
REG_PWR register

Bit	Name	Description	Value at reset
15	PACTLR_APCEN	**0:** PA controller is disabled[75] **1:** PA controller is enabled	0
14	PACTLR_APC	**0:** PA controller is OFF[1] **1:** PA controller is ON	0

REG_CFG register

13:12	PACTLR_CAP	**00:** 0 pF **01:** 12.5 pF **11:** 25 pF **10:** 50 pF	10
11:10	PACTLR_RES	**00:** open **01:** 150 kΩ **10:** 300 kΩ **11:** not used	10
9:5	PACTLR_VHOME	PA controller detection voltage setting:[1] **00000:**0*Vstep+Vlow ~ 0.46 V **00001:**1*Vstep+Vlow ~ 0.49 V **00010:** 2*Vstep+Vlow ~ 0.52 V **…** **11111:** 31*Vstep+Vlow ~ 1.39 V	01100
4	PACTLR_IDIOD	**0:** Diode bias current is low (30 uA) **1:** Diode bias current is high (300 uA)	0
3	PACTLR_TYPE	**0:** Power sensing **1:** Current sensing (for test purpose only)	0

Synthesizer



Four VCOs are used :

- - a TX LB VCO [824.2 ~ 914.8 MHz] to generate the TX GSM 850 / TX GSM 900,
- - a TX HB VCO [1710.2 ~ 1909.8 MHz] to generate the TX DCS 1800 / TX PCS 1900,
- - a MAIN VCO 1 [3176.1 ~ 3575.2 MHz] (see below) to generate the RX GSM 850 / LO

(and IF) for TX GSM 900, TX DCS 1800 and TX PCS 1900,

- - a MAIN VCO 2 [3610.4 ~ 3979.6 MHz] (see below) to generate the RX GSM 900 / RXDCS 1800 / RX PCS 1900 / LO (and IF) for the two parts of TX GSM 850.

Synthesizer

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Reference clock input[17]						
Input frequency				26		MHz
Input sensitivity			0.5	1.0	2.0	Vpp
Reference phase noise	@ 1 kHz offset				-129	dBc/Hz
Duty cycle					40/60 to 60/40	
Input resistance			10			kΩ
Input capacitance					5	pF
VCXO buffer output (XOUT pin)[18]						
Output frequency				26		MHz
Output level			0.5	1.0	2.0	Vpp

Crystal and External Varactor network [14]

XEN supply pin	@ I = 3.2mA		2.4		2.9	V
Crystal						
Nominal frequency				26.0		MHz
Frequency tolerance	at 25°C ±3°C				±10.0	ppm
Temperature characteristics	in reference to +25°C over –20 ~ +75°C				±10.0	ppm
Aging 1st year after 5 years					±1.0 ±2.5	ppm ppm
Dips vs. temperature	–20 ~ +75°C				0.3	ppm/°C
Frequency versus temperature slope at 25°C	at 25° C ± 7°C		-0.5		0	ppm/°C
Equivalent Series Resistance			0		40	Ω
Standard load capacitance				9.3 (tbc)	12.0	pF
Shunt capacitance				1.5	1.7	pF
Motional capacitance			5.4	6.3	7.2	fF
Drive level					150	µW
Varactor network						
Minimum voltage tuning		Vt	0		2.0	V
Tuning range	with Vt = 0V to 2.0V		±26.0	±33.0	±41.0	ppm
Sensitivity accuracy[15]	Over temp and over the tuning range				20 %	Hz/step^2
Frequency step					0.01	ppm/step

Main synthesizer in RX mode for GSM 850 and E-GSM 900

Specification at the mixers LO port

Prescaler input frequency range			3476 to 3840			MHz
PFD operating frequency				400		kHz
N divider ratio			8692 to 9598			
L divider by 4 output frequency range			869 to 960			MHz
Close in phase noise	@ 1 kHz offset fcomp = 400 kHz @ 960 MHz			-90	-81	dBc/Hz
Phase noise	@ 600 kHz offset @ 1.6 MHz offset @ 3.0 MHz offset @ 10 MHz offset @ 20 MHz offset			-130	-120 -135 -140 -142 -145	dBc/Hz
Reference feedthrough	@ 400 kHz offset @ 800 kHz offset @ 1.6 MHz offset			-80 -94	-53 -68 -79	dBc
Lock time	1) GSM850: From 869MHz to 894MHz 2) GSM900: From 925MHz to 960MHz 3) PCS1900 → GSM850: From 1990MHz to 869MHz 4) DCS1800 → GSM900: From 1880MHz to 925MHz @ 20 Hz averaged frequency error over one burst			100	170	us

Voltage regulators

VOLTAGE REGULATION

C_{out}=1.0uF, $C_{bandgap}$=100nF unless otherwise specified.
Table specifies regulator and bandgap together unless otherwise specified.
If an external regulation is desired, the internal voltage regulators can be bypassed (regulators shut down).

Band gap

Turn-on time	speed up mode active				25	ms
Consumption current				80		uA

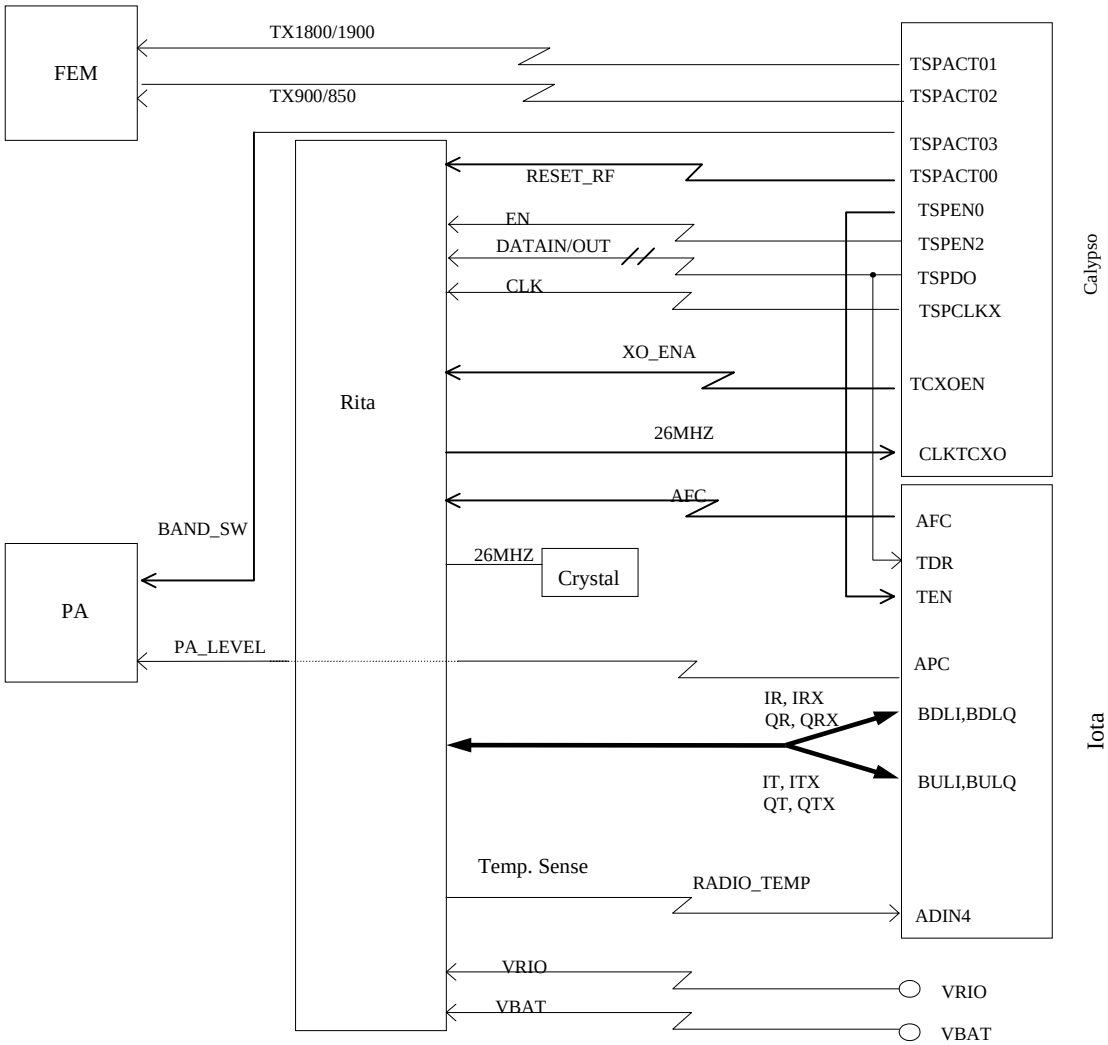
Regulator R1

Input voltage		Vin	3.0[4]	3.6	5.5	V
Output voltage	@ Ioutmax	Vout	2.7	2.8	2.9	V
Max. output current		Ioutmax	60			mA
Ground pin current	@ Ioutmax @ Iout = 0 mA				6.0 0.3	mA
DC line regulation	From Vinmin to Vinmax @ Ioutmax				50	mV
AC line regulation Overshoot Undershoot	Vin step from Vout + 0.1 to Vout + 0.5 in 30 us Vin step from Vout + 0.5 to Vout + 0.1 in 30 us				 20 20	mV
DC load regulation	Iout = 0 mA to Ioutmax				50	mV
AC load regulation Overshoot Undershoot	Iout step from Ioutmax to Ioutmax/2 in 5 us Iout step from Ioutmax/2 to Ioutmax in 5 us				 30 30	mV
Output voltage noise	f =10 Hz to 100 kHz Iout = Ioutmax Vin = Vout + 0.2 V			50		uVrms

RF-BB interface

1. *RF-BB connection*
2. *RF controlling by BB*

RF-BB connection

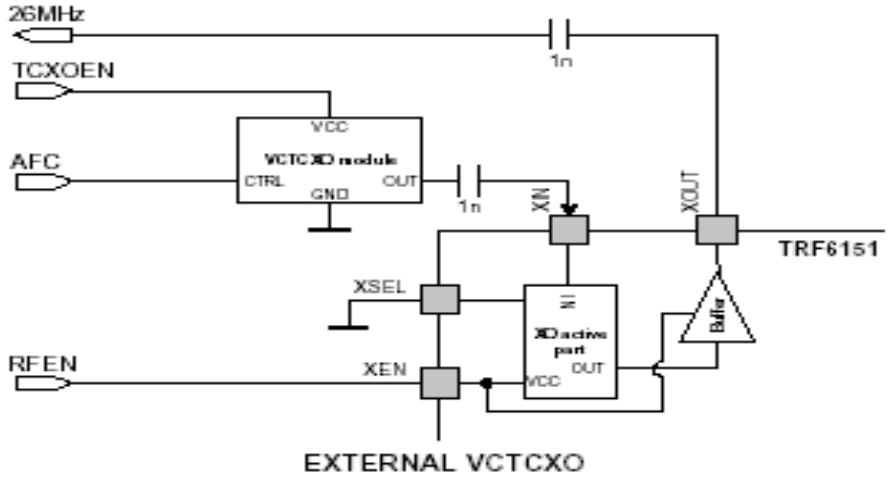


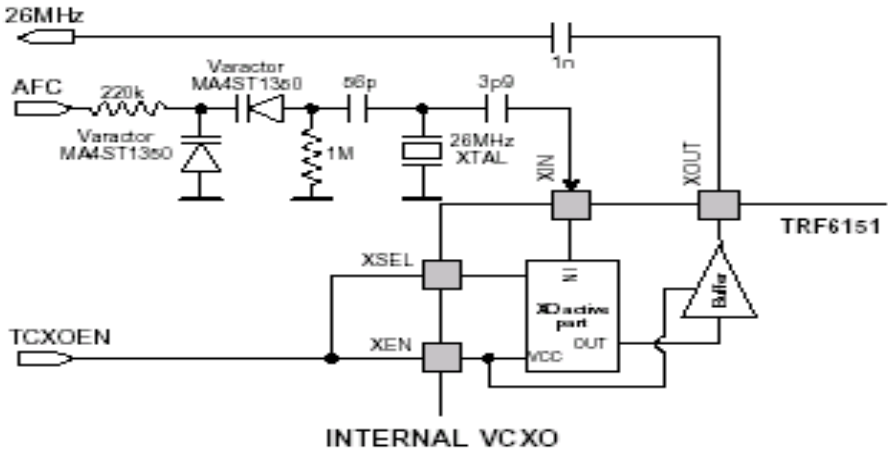
RF controlling by BB

- Auto Frequency Control
- Auto Power Control
- FEM control

AFC (Auto Frequency Control)

- AFC's purpose is to correct frequency shifts of the voltage-controlled oscillator to maintain the master clock frequency in a 0.1-PPM range



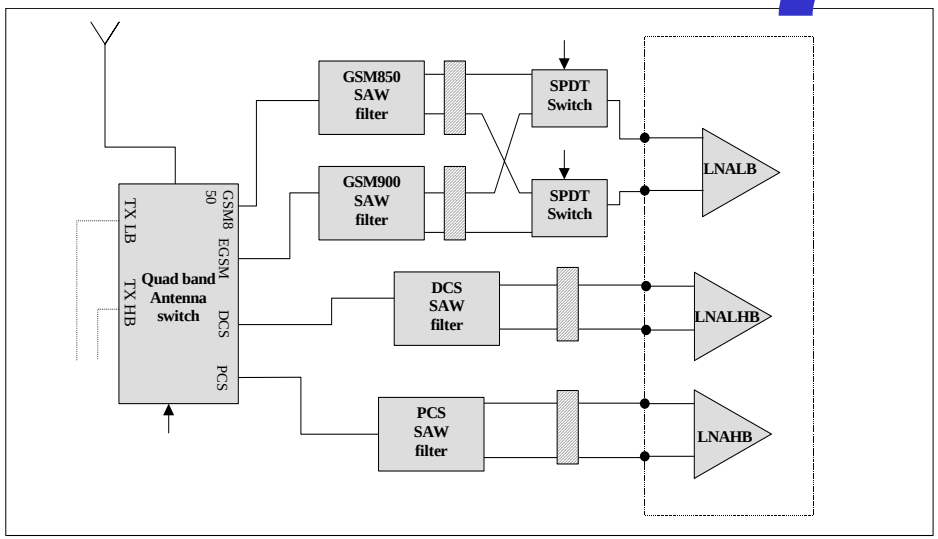


APC(Automatic Power Control)

- The automatic power control (APC) generates an envelope signal to control the power ramp up, power ramp down, and power level of the radio burst. The APC structure is intended to support single-slot and multislot transmission with smooth power transition when consecutive bursts are transmitted at different power levels.
- Refer to the PA controller loop.

RF control-FEM Control

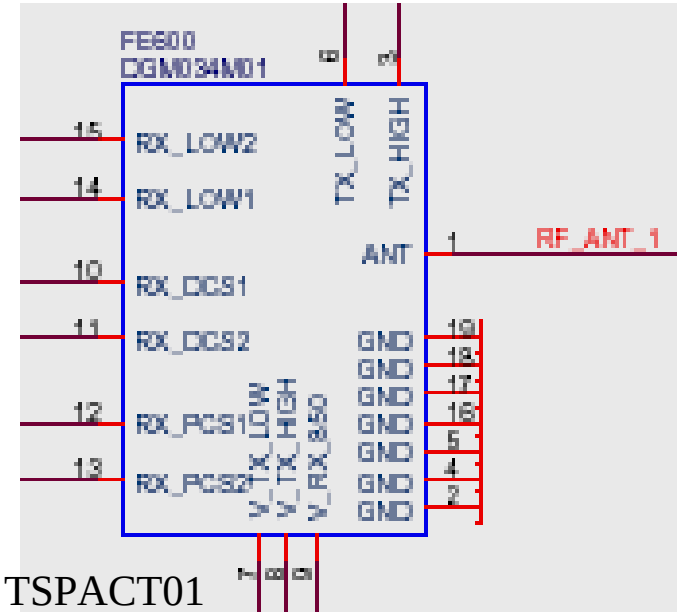
Rita – FEM QuadBand



Discrete solution

Ports (Pins)	EGSM RX	850 RX	GSM 1800RX	PCS RX	EGSM/850 TX	1800/PCS TX
TSPACT01	H	H	H	H	H	L
TSPACT02	H	H	H	H	L	H
TSPACT04	H	L	H	H	H	H

Integrated FEM



TSPACT01

TSPACT02

TSPACT04

RF-SW programming and control

1. *Rita registers introduction*

Rita registers introduction

SERIAL INTERFACE PROGRAMMING

- Serial word format

MSB															LSB
FIRST IN															LAST IN
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Registers table

Address			Serial word format	Register name	Definition
0	0	0	16 bits	REG_RX	RF general settings
0	0	1	16 bits	REG_PLL	PLLs settings
0	1	0	16 bits	REG_PWR	Power on/off all functional block of the transceiver
0	1	1	16 bits	REG_CFG	Transceiver config, PA Controller setting
1	0	0	16 bits	REG_TEST1	Reserved for test[70]
1	0	1	16 bits	REG_TEST2	
1	1	0	16 bits	REG_TEST3	
1	1	1	16 bits	REG_TEST4	

REG_RX

This register is used to configure the receiver, to launch RX calibration process

Bit	Name	Description	Value at reset
15:11	VGA_GAIN	**00000 - 00101:** reserved **00110:** VGA gain =14dB **00111:** VGA gain =16 dB **01000:** VGA gain =18 dB **01001:** VGA gain =20 dB **01010:** VGA gain =22 dB **01011:** VGA gain =24 dB **01100:** VGA gain =26 dB **01101:** VGA gain =28 dB **01110:** VGA gain =30 dB **01111:** VGA gain =32 dB **10000:** VGA gain =34 dB **10001:** VGA gain =36 dB **10010:** VGA gain =38 dB **10011:** VGA gain =40 dB **10100 - 11111:** reserved	10011
10:9	RF_GAIN	**00:** low RF gain (GRF_LOW) **01**: *reserved* **10:** *reserved* **11**: high RF gain (GRF_HIGH)	11
8	RX_CAL_MODE[76]	**0**: Stop RX calibration process **1**: power on DC offset calibration system and start RX calibration process.	0
7	READ_EN	**0:** Data serialized on SIOUT pin are 0 **1:** Data serialized on SIOUT pin are REG_RX content	0
6	*Reserved*	*Reserved*	0
5	*Reserved*	*Reserved*	0
4	*Reserved*	*Reserved*	0
3	*Reserved*	*Reserved*	0

REG_PLL

This register is used to program the synthesizer frequency according the desired RX/TX channel.

Bit	Name	Description	Value at reset
15:9	PLL_REGB	B = [64; 66; 67 ...155][69]	0000000
8:3	PLL _REGA	A = [0; 1; 2..63]	000000

Useful formulas for synthesizers are:

	P	R	L	M	B range	A range	RX/TX RF Frequency (MHz)
RX Low band	64	65	4	-	[135; 150]	[0; 62]	$\frac{(B*P+A)}{R*L}*26$
RX High band	64	65	2	-	[141; 155]	[0; 63]	
TX mode GSM850_1	64	55	4	26	[128; 130]	[0; 62]	$(\frac{1}{L}-\frac{1}{M})*\frac{(B*P+A)}{R}*26$
TX mode GSM850_2	64	30	4	52	[65; 66]	[0; 63]	
TX mode GSM900	64	35	4	52	[68; 71]	[0; 63]	$(\frac{1}{L}+\frac{1}{M})*\frac{(B*P+A)}{R}*26$
TX mode High band	64	70	2	26	[133; 149]	[0; 63]	

REG_PWR

This register is used to power on/off all functional block of the transceiver and to choose the RX/TX band.

Bit	Name	Description	Value at reset
15	PACTLR_APCEN	**0:** PA controller is disabled[70] **1:** PA controller is enabled	0
14	PACTLR_APC	**0:** PA controller is OFF[70] **1:** PA controller is ON	0
13	TX_MODE	**0:** Transmitter is OFF **1:** Transmitter is ON	0
12:11	RX_MODE	**00:** Receiver +interferer detection system are OFF **01:** Receiver is ON (RX mode A) **10:** Receiver +interferer detection system is ON (RX mode B1) **11:** Receiver +interferer detection system is ON (RX mode B2)	00
10:9	SYNTHE_MODE[71]	**00:** Synthesizer, transmitter and receiver are off **01:** RX Synthesizer is ON **10:** TX Synthesizer is ON **11:** not used	00
8:6	BAND	**000-001:** GSM900 **010-011:** DCS **100:** GSM850 (Low part) **101:** GSM850 (High part) **110-111:** PCS	000
5	REGUL_MODE	**0:** Regulators are OFF **1:** Regulators are ON	0
4:3	BANDGAP_MODE	**00-01:** Band gap is OFF **10:** Band gap is ON; speed up mode is enabled **11:** Band gap is ON; speed up mode is disabled	00

REG_CFG

This register is used to configure the transceiver and set the PA controller at mobile initialization.

Bit	Name	Description	Value at reset
15		Not used	-
14	TEMP_SENSOR	**0:** Temperature sensor is OFF **1:** Temperature sensor is ON	0
13:12	PACTLR_CAP	**00:** 0 pF **01:** 12.5 pF **10:** 25 pF **11:** 50 pF	10
11:10	PACTLR_RES	**00:** open **01:** 150 kΩ **10:** 300 kΩ **11:** not used	10
9:5	PACTLR_VHOME	PA controller detection voltage setting:[72] **00000:**0*Vstep+Vlow ~ 0.46 V **00001:**1*Vstep+Vlow ~ 0.49 V **00010:** 2*Vstep+Vlow ~ 0.52 V … **11111:** 31*Vstep+Vlow ~ 1.39 V	01100
4	PACTLR_IDIOD	**0:** Diode bias current is low (30 uA) **1:** Diode bias current is high (300 uA)	0
3	PACTLR_TYPE	**0:** Power sensing **1:** Current sensing (for test purpose only)	0

- **Q&A**

Thank you!