description

The TRF6151C is a quadruple-band transceiver IC suitable for GSM850, GSM900, DCS1800, and PCS1900 GPRS class-12 applications. This device integrates a receiver based on direct conversion architecture, a transmitter based on modulation-loop architecture, frequency synthesizing including a 26-MHz VCXO, a main N-integer synthesizer, two main VCOs, a programmable main-loop filter, two TX VCOs, a TX loop filter, voltage regulators to supply on-chip and off-chip RF functions, and a power-amplifier controller.

A *quad-band* application requires few external components, aside from a power amplifier and a front-end module.

The TRF6151C is housed in a 48-pin, 7×7-mm, 0,5-mm pitch QFN package.

The TRF6151C transceiver is part of a TI GSM chipset. It is compatible with TWL3014 and TWL3016 ABB chips and with TBB2100, PD751997AGZA, and OMAP730 chips.

This device combines the following functions:

- Transmit section:
  - An offset PLL with post-IQ modulator and post-offset mixer filters fully integrated on the chip
  - Two TX VCOs fully integrated on the chip
  - A TX loop filter fully integrated on the chip
  - A divider by 4 for local oscillator (LO) generation in GSM900 and GSM850
  - A divider by 2 for LO generation in DCS1800 and PCS1900
  - A programmable M divider for IF generation
  - A power-amplifier controller including all the functions required to design a power-sensing control loop, except for the sensing diodes
- Receive section:
  - A GSM900/GSM850 LNA (LNAGSM) with switchable gain
  - A DCS1800 LNA (LNADCS) with switchable gain
  - A PCS1900 LNA (LNAPCS) with switchable gain
  - Three quadrature demodulators for GSM900/GSM850 (MIXGSM), DCS1800 (MIXDCS), and PCS1900 (MIXPCS) bands with programmable gain
  - Two baseband amplifiers with digitally-programmable gain
  - Two fully-integrated baseband channel filters
  - Two dc-offset compensation systems
  - A divider by 4 for LO generation in GSM900 and GSM850 in order to minimize dc offset generated by self mixing and the LO reradiation
  - A divider by 2 for LO generation in DCS1800 and PCS1900 in order to minimize dc offset generated by self-mixing and LO reradiation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

description (continued)

- Common to both sections:
  - A 26-MHz VCXO with external varactor and crystal
  - A 26-MHz buffer to drive the DBBs
  - Two main VCOs fully integrated on the chip
  - A main N-integer synthesizer
  - A programmable main loop filter fully integrated on the chip
  - Three voltage regulators to supply internal functions and external RF components
  - A digital serial interface

Figure 1 shows the TRF6151C receiver block diagram. Figure 2 shows a top view of the RGZ package.

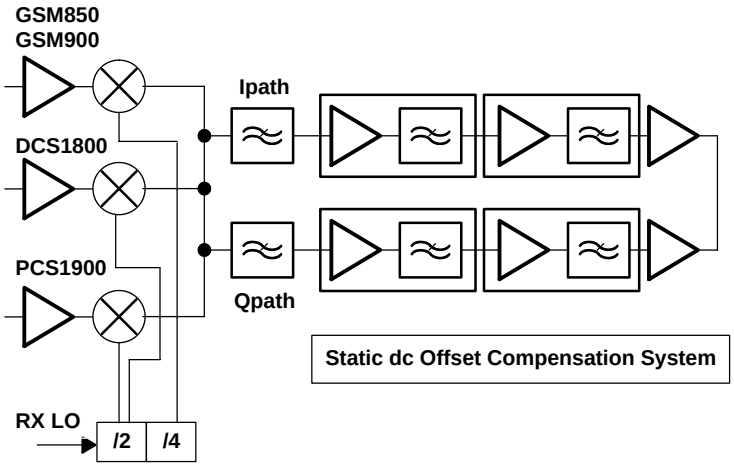


Figure 1. Receiver Block Diagram

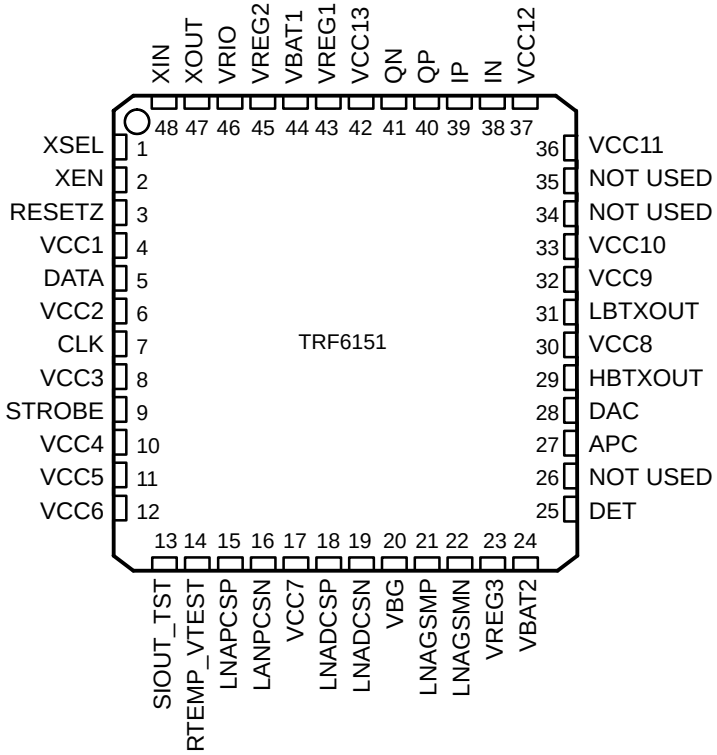


Figure 2. RGZ Package (Top View)

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
XSEL	1	I	Crystal selection (external or internal)
XEN	2	I	Crystal enable (VCXO and buffer supply)
RESETZ	3	I	Serial-interface reset
VCC1	4	VCC	PLL supply voltage
DATA	5	I	Serial-interface data
VCC2	6	VCC	PLL supply voltage
CLK	7	I	Serial interface clock
VCC3	8	VCC	PLL supply voltage
STROBE	9	I	Serial interface strobe
VCC4	10	VCC	MAIN V_{CO2} supply voltage (2.0 V internally generated)
VCC5	11	VCC	VCO divider supply voltage
VCC6	12	VCC	MAIN V_{CO1} supply voltage (2.0 V internally generated)
SIOUT_TST	13	O	Serial interface output multiplexed with PLL test
RTEMP_VTEST	14	O	Temperature sensor output and VCO test
LNAPCSP	15	I	RX PCS LNA input (+)
LNAPCSN	16	I	RX PCS LNA input (–)
VCC7	17	VCC	RX LNA supply voltage
LNADCSP	18	I	RX DCS LNA input
LNADCSN	19	I	RX DCS LNA input
VBG	20	O	Band gap voltage output
LNAGSMP	21	I	RX GSM LNA input (+)
LNAGSMN	22	I	RX GSM LNA input (–)
VREG3	23	O	Regulator 3 output dedicated to VCC8 and VCC10
VBAT2	24	I	Regulator 3 battery-voltage supply
DET	25	I	PA controller detect input (ground if not used)
Not used	26	–	Not used—grounded
APC	27	O	PA controller output (float if not used)
DAC	28	I	PA controller APC input (ground if not used)
HBTXOUT	29	O	TX DCS/PCS output
VCC8	30	VCC	TX VCO buffer supply voltage (2.7 V)
LBTXOUT	31	O	TX GSM900/GSM850 output
VCC9	32	VCC	TX HB VCO core-supply voltage (2.4 V internally generated)
VCC10	33	VCC	TX VCO and RX mixer supply voltage
Not used	34	–	Not used
Not used	35	–	Not used
VCC11	36	VCC	TX LB VCO core-supply voltage (2.4 V internally generated)
VCC12	37	VCC	IQ modulator supply voltage and RX VGA supply voltage (2.7 V)
IN	38	I/O	In-phase baseband I/O (–)
IP	39	I/O	In-phase baseband I/O (+)
QP	40	I/O	Quadrature-phase baseband I/O (+)
QN	41	I/O	Quadrature-phase baseband I/O (–)
VCC13	42	VCC	TX charge pump supply voltage (2.7 V)
VREG1	43	O	Regulator 1 output dedicated to VCC7, VCC12, and VCC13

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
VBAT1	44	I	Regulator 1 and regulator 2 battery-voltage supply
VREG2	45	O	Regulator 2 output dedicated to VCC1, VCC2, VCC3, and VCC5
VRIO	46	VCC	Serial interface supply voltage
XOUT	47	O	Crystal buffer output
XIN	48	I	Crystal input

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: V_{BAT} . . . . . –0.3 V to 5.5 V
Power dissipation, Ta = 25 °C, 48-Pin QFN 7x7 mm, 0.5 mm pitch . . . . . 3.06 W
Operating temperature range T_C . . . . . –25°C to +85°C
Storage temperature range T_{stg} . . . . . –65°C to +150°C
ESD integrity (HBM)‡ . . . . . 1.5 kV
ESD integrity (CDM) . . . . . 300 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ RF pins (LNAGSMP/N, LNADCSP/N, LNAPCSP/N, LBTXOUT & HBTXOUT) are rated at 1 KV HBM.

recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{RIO}	Supply voltage	2.7	2.8	2.9	V
V_{IH}	High-level input voltage	0.8*VRIO			V
V_{IL}	Low-level input voltage			0.22 x VRIO	V
V_{OH}	High-level output voltage	0.7*VRIO		VRIO+0.5	V
V_{OL}	Low-level output voltage	–0.5		0.3*VRIO	V
V_{cc}	Supply voltage	2.7	2.8	2.9	V
V_{BAT}	Supply voltage	3.0†	3.6	5.5	V

† 3.0 V corresponds to V_{BATMIN} ==> When MS is emitting at full power, the battery voltage must never be under 3.0 V at TRF6151C regulator inputs

total current consumption

off mode

POWER MODE	TEST CONDITIONS	BAND	MIN	TYP	MAX	UNIT
All off	All functional blocks powered off	–		20	40	μA
All off except band gap	Band gap on and all other functional blocks powered off	–		80	100	μA
All off except band gap and regulators	Band gap and regulators on and all other functional blocks powered off	–		0.6	0.7	mA

receive mode

POWER MODE	TEST CONDITIONS	BAND	MIN	TYP	MAX	UNIT
RX synthesizer on	Main PLL is locking	GSM850		8	8.2	mA
		GSM900		8	8.2	
		DCS1800		8	8.2	
		PCS1900		8	8.2	
RX on in high gain	Main PLL, LO generation, LNA, IQ demodulator, and baseband strip are on	GSM850		62	80.4	mA
		GSM900		62	80.5	
		DCS1800		66	85.3	
		PCS1900		66	85.3	

transmit mode

POWER MODE	TEST CONDITIONS	BAND	MIN	TYP	MAX	UNIT
TX synthesizer on	Main PLL is locking	GSM850L		6.3	8.2	mA
		GSM850H		6.3	8.2	
		GSM900		6.3	8.2	
		DCS1800		6.3	8.2	
		PCS1900		6.3	8.2	
TX on	Main PLL, offset PLL, LO/IF generation, IQ modulator, and PA controller are on	GSM850L		116.0	132.5	mA
		GSM850H		116.0	132.5	
		GSM900		116.0	132.4	
		DCS1800		106.0	117.8	
		PCS1900		106.0	117.8	

† VCXO (supplied by an external voltage source) typical current consumption is 2.7 mA

voltage regulation

Typical: Vcc = 2.8 V, Ta = +25°C
C_{out} = 1.0 μF, $C_{bandgap}$ = 100 nF, unless otherwise specified
Table specifies regulator and bandgap together unless otherwise specified.
If an external regulation is desired, the internal voltage regulators can be bypassed (regulators shut down).

Typical: V_{cc} = 2.8 V, T_a = +25°C – Min and max: T_a = –25°C to +85°C, V_{BAT} = 3.0 V to 5.5 V and over process.

bandgap

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Turnon time	Speed up mode active				25	ms
Current consumption				80		μA

regulators R1, R2, and R3

PARAMETERS		TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Input voltage			V_I	3.0†	3.6	5.5	V
Output voltage		@ I_{Omax}	V_O	2.7	2.8	2.9	V
Max output current			I_{Omax}	60			mA
Ground pin current		@ I_{Omax}			2.1	6.0	mA
dc line regulation	R1	From $V_I$min to $V_I$max @ I_{Omax}			–10.5	50	mV
	R2				–10	50	
	R3				–13.5	50	
ac line regulation	Overshoot‡	V_I step from V_O + 0.1 to V_O + 0.5 in 30 μs				20	mV
	Undershoot‡	V_I step from V_O + 0.5 to V_O + 0.1 in 30 μs				20	
dc load regulation	R1	I_O = 0 mA to I_{Omax}			–9	50	mV
	R2				–8	50	
	R3				–13	50	
ac load regulation	Overshoot‡	I_O step from I_{Omax} to I_{Omax}/2 in 5 μs				30	mV
	Undershoot‡	I_O step from I_{Omax}/2 to I_{Omax} in 5 μs				30	
Output voltage noise		f =10 Hz to 100 kHz I_O = I_{Omax} V_I = V_O + 0.2 V			28	50	μVrms
ESR of decoupling capacitor§				0.01		1	Ω
Turnon time		V_O step from 0 to V_{Omax} ±3% @ I_{Omax}				100¶	μs
Ripple rejection		ac amplitude = 50 mVp f = 100 Hz @ I_{Omax} V_I = 3.1 V			64	55	dB
		ac amplitude = 50 mV_p f = 500 kHz @ I_{Omax} V_I = 3.1 V			40	35	dB

† 3.0 V corresponds to V_{BATMIN} ==> When MS is emitting at full power, the battery voltage must never be under 3.0 V at TRF6151C regulators inputs
‡ Ensured by design
§ Measurements taken with decoupling capacitor having ESR within specified range
¶ Band gap turn-on time not included

voltage regulation (continued)

regulator power domains

FUNCTIONAL BLOCKS	SUPPLY VOLTAGE	REGULATED SUPPLY	VCC LINE
Receiver			
LNAGSM, LNADCS, LNAPCS	V_{BAT1}	V_{REG1}	V_{CC7}
Analog part of VGA	V_{BAT1}	V_{REG1}	V_{CC12}
IQ demodulators (MIXGSM, MIXDCS, and MIXPCS)	V_{BAT2}	V_{REG3}	V_{CC8}
Transmitter			
Charge pump	V_{BAT1}	V_{REG1}	V_{CC13}
Phase frequency detector	V_{BAT1}	V_{REG1}	–†‡
Offset mixer, post-offset mixer low-pass filter	V_{BAT1}	V_{REG1}	V_{CC7}
Offset mixer buffer	V_{BAT2}	V_{REG3}	V_{CC10}
IQ modulator, post-IQ modulator low-pass filter	V_{BAT1}	V_{REG1}	V_{CC12}
TX LB VCO	V_{CC10}	2.4-V internal regulator	V_{CC11}‡
TX HB VCO	V_{CC10}	2.4-V internal regulator	V_{CC9}‡
TX VCO output buffers	V_{BAT2}	V_{REG3}	V_{CC8}
PA controller	V_{BAT1}	V_{REG1}	V_{CC7}
Main synthesizer			
Prescaler, charge pump, phase/frequency detector	V_{BAT1}	V_{REG2}	V_{CC2}
Loop filter (operational amplifier)	V_{BAT1}	V_{REG2}	V_{CC3}
Counters A, B	V_{BAT1}	V_{REG2}	V_{CC1}
LO generation for the RX/TX (L divider, M divider)	V_{BAT1}	V_{REG2}	V_{CC5}
Main VCO2	V_{CC5}	2.0-V internal regulator	V_{CC4}§
Main VCO1	V_{CC5}	2.0-V internal regulator	V_{CC6}§
VCO calibration machine	V_{BAT2}	V_{REG3}	V_{CC10}
Reference voltage source			
Band gap	V_{BAT2}	–	–
Digital control			
PA controller timer, digital clock generator, serial interface and associated buffer, VGA digital circuitry	V_{RIO} supply from ABB chip	–	VRIO
Internal 26-MHz VCXO			
VCXO core, main PLL reference divider	TCXOEN buffer (2.7 V) from DBB chip	–	XEN
Internal VCXO selection	TCXOEN buffer (2.7 V) from DBB chip	–	XSEL
RF front end module (external component)			
Front end module	V_{BAT2}	V_{REG3}	–

† Connection is done on chip (no decoupling using a V_{CC} line)
‡ Decoupling line for 2.4-V internal regulator output
§ Decoupling line for 2.0-V internal regulator output

temperature sensor†

Typical: Vcc = 2.8 V, Ta = +25°C – Min and max: Ta = –25°C to +85°C, V_{BAT} = 3.0 V to 5.5 V and over process

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Sensor voltage	@ $T_a$min. = –25°C		0.9		1.05	V
	@ $T_a$max. = +85°C		1.35		1.5	
Sensor slope	Over –25 ~ +85°C		3.0		5.0	mV/°C

† This temperature sensor is accessible any time via pin 14 (not multiplexed with any other signal)

VCXO buffer output (XOUT pin)†

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Output frequency				26		MHz
Output level			0.5	1.0	2.0	V_{PP}
Duty cycle					40/60 to 60/40	
Start up time (including the VCXO core)	90% of output amplitude			‡	9.2	ms

† Load impedance Z_L = 25 pF in parallel with 10 kΩ @ 26 MHz
‡ Ensured by design

The internal VCXO setup shown in Figure 3 is used in production testing.

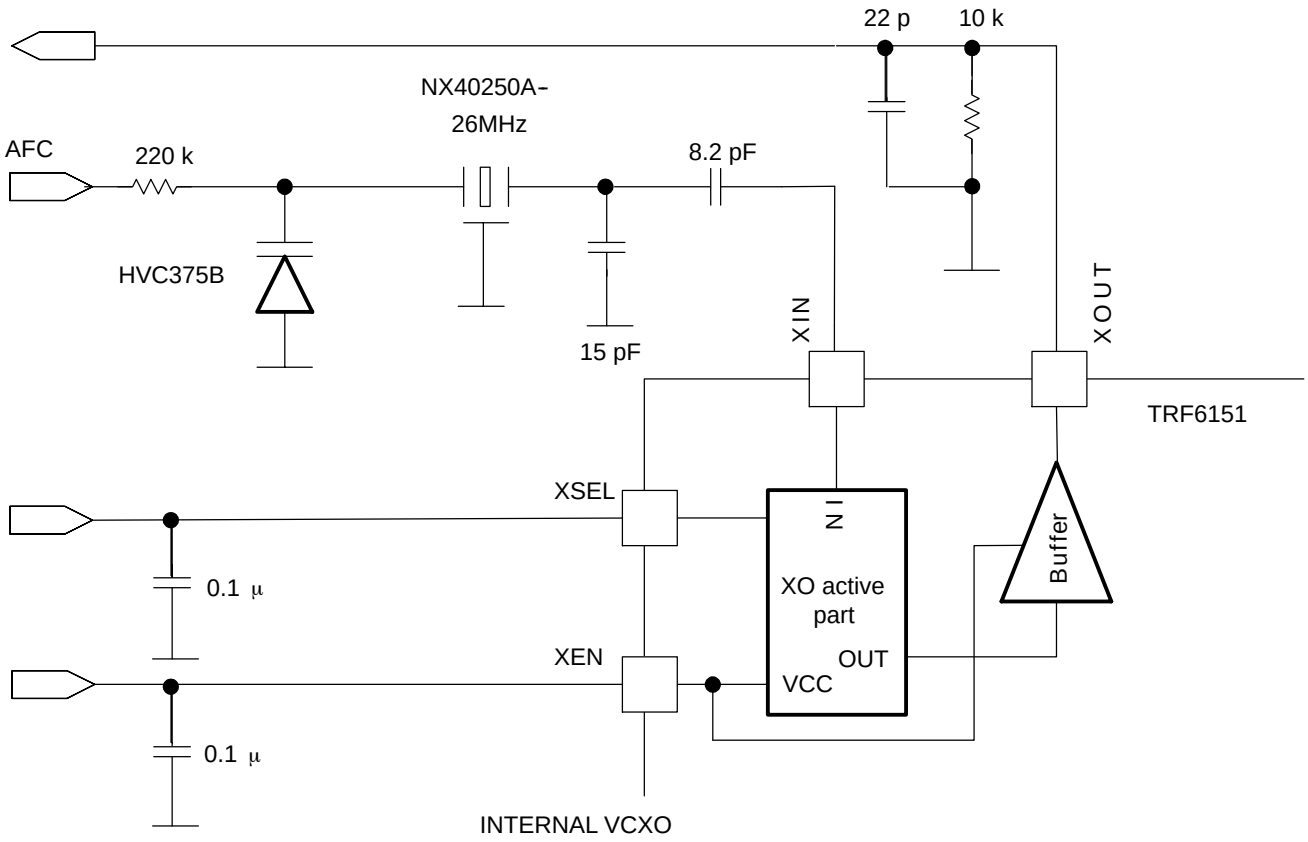
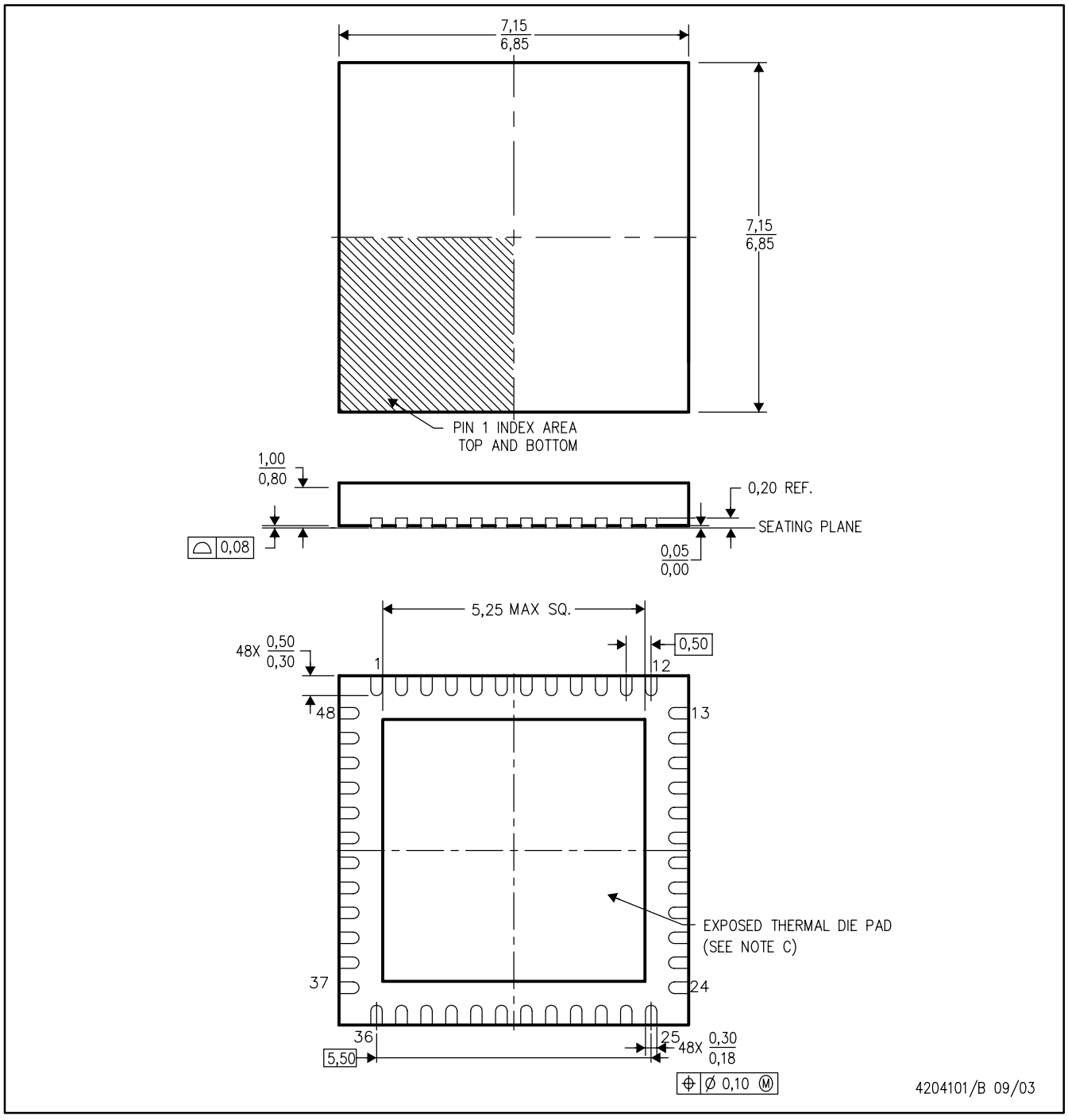


Figure 3. Internal VCXO

MECHANICAL DATA

RGZ (S-PQFP-N48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, no-leads (QFN) package configuration
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-220

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265