TEXAS INSTRUMENTS

TWL3025

GSM/DCS Baseband and Voice A/D and D/A RF Interface Circuit With Power Supply Management

Data Manual

November 2003

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1 Introduction

This chapter provides an overview of the Texas Instruments TWL3025 device and its features.

1.1 Description

The TWL3025 device is an analog baseband (ABB) device which, together with a digital baseband (DBB) device, is part of a TI TMS320™ DSP (digital signal processor) solution intended for digital cellular telephone applications. This includes the GSM 900, DCS 1800, and PCS 1900 standards (dual-band capability).

The TWL3025 device includes a complete set of baseband functions that perform the interface and processing of the following voice signals, the baseband in-phase (I) and quadrature (Q) signals, which support both the single-slot and multislot modes. The TWL3025 device also includes associated auxiliary RF control features, supply voltage regulation, battery charging controls, and switch on/off system analysis.

The TWL3025 device interfaces with the DBB device through a digital baseband serial port (BSP) and a voiceband serial port (VSP). The signal ports communicate with a DSP core (LEAD). A microcontroller serial port (USP) communicates with the microcontroller core and a time serial port (TSP) communicates with the time processing unit (TPU) for real-time control.

A specific module is dedicated to support the 1.8-V/3-V SIM card interface. The module includes the generation of the SIM card supply voltage, as well as level shifters to adapt the SIM card signal levels to the microcontroller I/O signal levels. The TWL3025 device meets JTAG testability standard (IEEE Std 1131.1 – 1990) through a standard test access port (TAP) and boundary scan.

The TW3025 device also includes an on-chip voltage reference, under-voltage detection, and power-on reset circuits. The TWL3025 device is packaged in Texas Instruments 100-terminal, 0,8-mm pitch, MicroStar™ ball grid array (GGM) and 143-terminal, 0,5-mm pitch, MicroStar™ ball grid array (GQW).

1.2 Features

The TWL3025 device supports the following features.

- Applications include GSM 900, PCS 1900, and DSC 1800 cellular telephones
- Voice coder/decoder (codec)
- Baseband codec single- and multislot with I/Q RF interface
- Auxiliary RF converters
- SIM card interface
- Li-Ion or Ni-MH battery charging control
- Six low-dropout, low-noise, linear voltage regulators
- Dedicated low quiescent current mode on regulators
- Voltage detectors (with power-off delay)
- Four-channel analog-to-digital converter (ADC)
- Dedicated very low quiescent current domain supply
- 100-terminal MicroStar™ BGA

1.3 Trademarks

MicroStar BGA is a trademark of Texas Instruments.

MicroStar Junior BGA is a trademark of Texas Instruments.

TMS320 DSP is a trademark of Texas Instruments.

Other trademarks are the property of their respective owners.

1.4 Ordering Information

ORDERING NUMBER	VOLTAGE	T_A
PTWL3025GGM	−0.3 V to 7 V	−30°C to 85°C
PTWL3025GQW	−0.3 V to 7 V	−30°C to 85°C

2 Terminal Descriptions

This section provides the terminal descriptions for the TWL3025 device. Figure 2−1 and Figure 2−2 show the signal assigned to each terminal in the package. Table 2−1 through Table 2−4 provide cross-reference between each terminal number and the signal name on that terminal. Table 2−1 and Table 2−2 are arranged in terminal number order, and Table 2−3 and Table 2−4 list signals in alphabetical order.

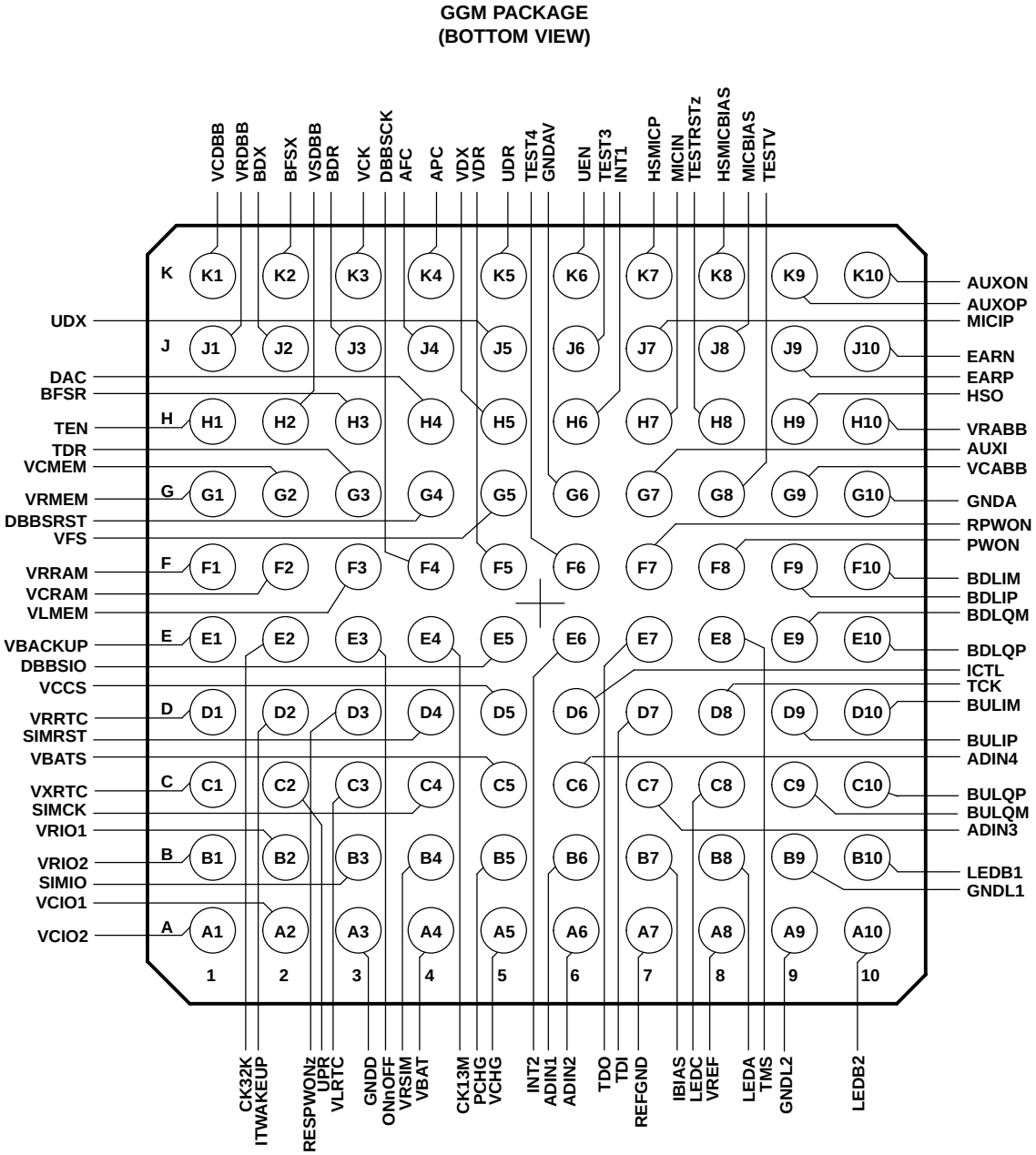
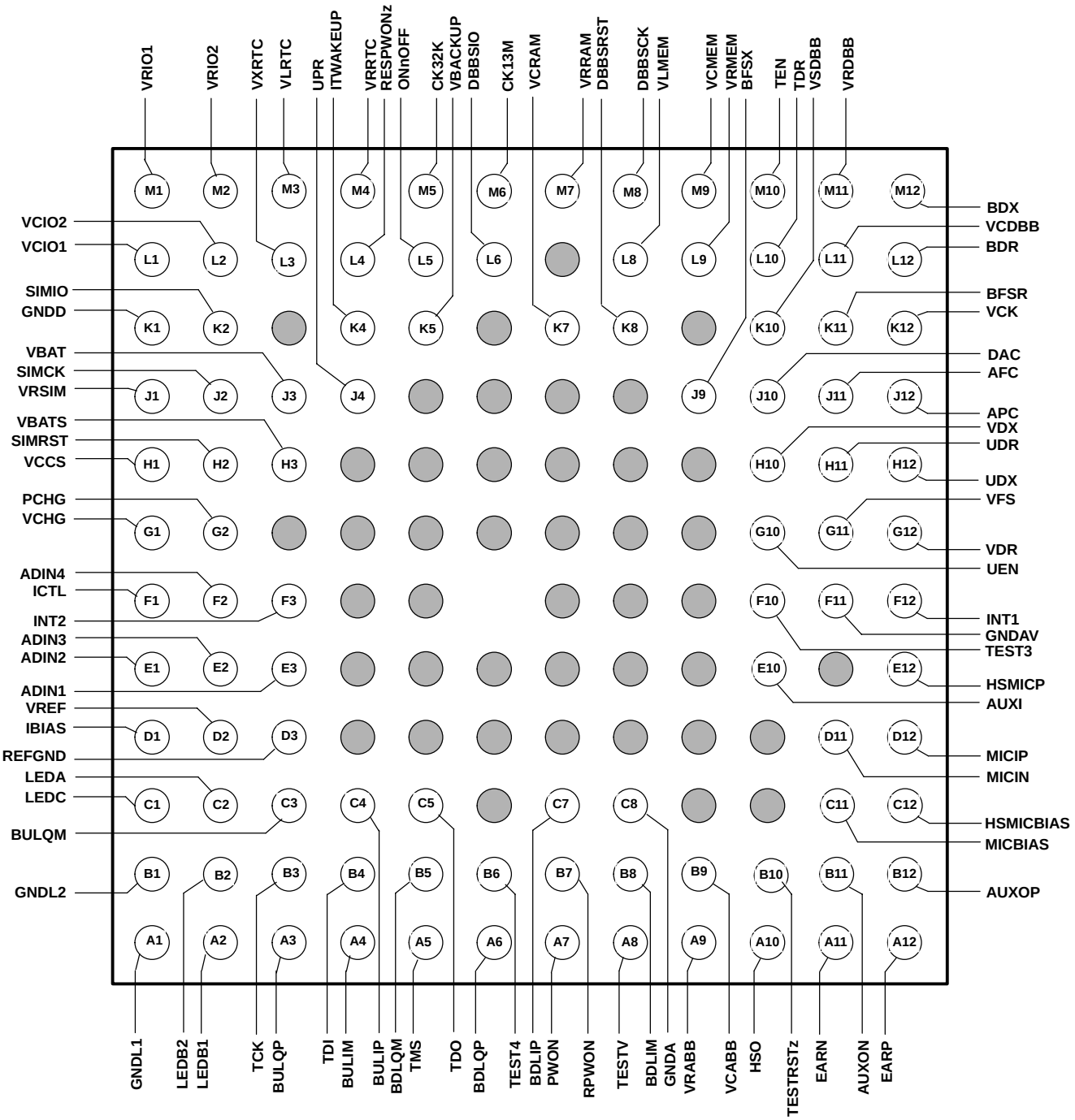


Figure 2−1. TWL3025 GGM Package Terminal Assignments

GQW PACKAGE
(BOTTOM VIEW)



NOTE: All NC terminals are connected to GND during test.

Figure 2−2. TWL3025 GQW Package Terminal Assignments

Table 2−1. Signal Names Sorted by GGM Terminal Number

NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME
A1	VCIO2	C6	ADIN4	F1	VRRAM	H6	INT1/TEST1
A2	VCIO1	C7	ADIN3	F2	VCRAM	H7	MICIN
A3	GNDD	C8	LEDC	F3	VLMEM	H8	TESTRSTz
A4	VBAT	C9	BULQM	F4	DBBSCK	H9	HSO
A5	VCHG	C10	BULQP	F5	VDR	H10	VRABB
A6	ADIN2	D1	VRRTC	F6	TEST4	J1	VRDBB
A7	REFGND	D2	ITWAKEUP	F7	RPWON	J2	BDX
A8	VREF	D3	RESPWONz	F8	PWON	J3	BDR
A9	GNDL2	D4	SIMRST	F9	BDLIP	J4	AFC
A10	LEDB2	D5	VCCS	F10	BDLIM	J5	UDX
B1	VRIO2	D6	ICTL	G1	VRMEM	J6	TEST3
B2	VRIO1	D7	TDI	G2	VCMEM	J7	MICIP
B3	SIMIO	D8	TCK	G3	TDR	J8	MICBIAS
B4	VRSIM	D9	BULIP	G4	DBBSRST	J9	EARP
B5	PCHG	D10	BULIM	G5	VFS	J10	EARN
B6	ADIN1	E1	VBACKUP	G6	GNDAV	K1	VCDBB
B7	IBIAS	E2	CK32K	G7	AUXI	K2	BFSX
B8	LEDA	E3	ON_nOFF	G8	TESTV	K3	VCK
B9	GNDL1	E4	CK13M	G9	VCABB	K4	APC
B10	LEDB1	E5	DBBSIO	G10	GNDA	K5	UDR
C1	VXRTC	E6	INT2/TEST2	H1	TEN	K6	UEN
C2	UPR	E7	TDO	H2	VSDBB	K7	HSMICP
C3	VLRTC	E8	TMS	H3	BFSR	K8	HSMICBIAS
C4	SIMCK	E9	BDLQM	H4	DAC	K9	AUXOP
C5	VBATS	E10	BDLQP	H5	VDX	K10	AUXON

Table 2−2. Signal Names Sorted by GQW Terminal Number

NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME
A1	GNDL1	D1	IBIAS	G2	PCHG	K2	SIMIO
A2	LEDB1	D2	VREF	G3	NC	K3	NC
A3	BULQP	D3	REFGND	G4	NC	K4	ITWAKEUP
A4	BULIM	D4	NC	G5	NC	K5	VBACKUP
A5	TMS	D5	NC	G6	NC	K6	NC
A6	BDLQP	D6	NC	G7	NC	K7	VCRAM
A7	PWON	D7	NC	G8	NC	K8	DBBSRST
A8	TESTV	D8	NC	G9	NC	K9	NC
A9	VRABB	D9	NC	G10	UEN	K10	VSDBB
A10	HSO	D10	NC	G11	VFS	K11	BFSR
A11	EARN	D11	MICIN	G12	VDR	K12	VCK
A12	EARP	D12	MICIP	H1	VCCS	L1	VCIO1
B1	GNDL2	E1	ADIN2	H2	SIMRST	L2	VCIO2
B2	LEDB2	E2	ADIN3	H3	VBATS	L3	VXRTC
B3	TCK	E3	ADIN1	H4	NC	L4	RESPWONz
B4	TDI	E4	NC	H5	NC	L5	ON_nOFF
B5	BDLQM	E5	NC	H6	NC	L6	DBBSIO
B6	TEST4	E6	NC	H7	NC	L7	NC
B7	RPWON	E7	NC	H8	NC	L8	VLMEM
B8	BDLIM	E8	NC	H9	NC	L9	VRMEM
B9	VCABB	E9	NC	H10	VDX	L10	TDR
B10	TESTRSTz	E10	AUXI	H11	UDR	L11	VCDBB
B11	AUXON	E11	NC	H12	UDX	L12	BDR
B12	AUXOP	E12	HSMICP	J1	VRSIM	M1	VRIO1
C1	LEDC	F1	ICTL	J2	SIMCK	M2	VRIO2
C2	LEDA	F2	ADIN4	J3	VBAT	M3	VLRTC
C3	BULQM	F3	INT2/TEST2	J4	UPR	M4	VRRTC
C4	BULIP	F4	NC	J5	NC	M5	CK32K
C5	TDO	F5	NC	J6	NC	M6	CK13M
C6	NC	F7	NC	J7	NC	M7	VRRAM
C7	BDLIP	F8	NC	J8	NC	M8	DBBSCK
C8	GNDA	F9	NC	J9	BFSX	M9	VCMEM
C9	NC	F10	TEST3	J10	DAC	M10	TEN
C10	NC	F11	GNDAV	J11	AFC	M11	VRDBB
C11	MICBIAS	F12	INT1/TEST1	J12	APC	M12	BDX
C12	HSMICBIAS	G1	VCHG	K1	GNDD		

Table 2−3. Signal Names Sorted Alphanumerically to GGM Terminal Number

SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER
ADIN1	B6	DBBSIO	E5	PCHG	B5	VCABB	G9
ADIN2	A6	DBBSRST	G4	PWON	F8	VCCS	D5
ADIN3	C7	EARN	J10	REFGND	A7	VCDBB	K1
ADIN4	C6	EARP	J9	RESPWONz	D3	VCHG	A5
AFC	J4	GNDA	G10	RPWON	F7	VCIO1	A2
APC	K4	GNDAV	G6	SIMCK	C4	VCIO2	A1
AUXI	G7	GNDD	A3	SIMIO	B3	VCK	K3
AUXON	K10	GNDL1	B9	SIMRST	D4	VCMEM	G2
AUXOP	K9	GNDL2	A9	TCK	D8	VCRAM	F2
BDLIM	F10	HSMICBIAS	K8	TDI	D7	VDR	F5
BDLIP	F9	HSMICP	K7	TDO	E7	VDX	H5
BDLQM	E9	HSO	H9	TDR	G3	VFS	G5
BDLQP	E10	IBIAS	B7	TEN	H1	VLMEM	F3
BDR	J3	ICTL	D6	TEST3	J6	VLRTC	C3
BDX	J2	INT1/TEST1	H6	TEST4	F6	VRABB	H10
BFSR	H3	INT2/TEST2	E6	TESTRSTz	H8	VRDBB	J1
BFSX	K2	ITWAKEUP	D2	TESTV	G8	VREF	A8
BULIM	D10	LEDA	B8	TMS	E8	VRIO1	B2
BULIP	D9	LEDB1	B10	UDR	K5	VRIO2	B1
BULQM	C9	LEDB2	A10	UDX	J5	VRMEM	G1
BULQP	C10	LEDC	C8	UEN	K6	VRRAM	F1
CK13M	E4	MICBIAS	J8	UPR	C2	VRRTC	D1
CK32K	E2	MICIN	H7	VBACKUP	E1	VRSIM	B4
DAC	H4	MICIP	J7	VBAT	A4	VSDBB	H2
DBBSCK	F4	ON_nOFF	E3	VBATS	C5	VXRTC	C1

Table 2−4. Signal Names Sorted Alphanumerically to GQW Terminal Number

SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER	SIGNAL NAME	NUMBER
ADIN1	E3	HSO	A10	NC	G4	TEST3	F10
ADIN2	E1	IBIAS	D1	NC	G5	TEST4	B6
ADIN3	E2	ICTL	F1	NC	G6	TMS	A5
ADIN4	F2	INT1/TEST1	F12	NC	G7	UDR	H11
AFC	J11	INT2/TEST2	F3	NC	G8	UDX	H12
APC	J12	ITWAKEUP	K4	NC	G9	UEN	G10
AUXI	E10	LEDA	C2	NC	H4	UPR	J4
AUXON	B11	LEDB1	A2	NC	H5	VBACKUP	K5
AUXOP	B12	LEDB2	B2	NC	H6	VBAT	J3
BDLIM	B8	LEDC	C1	NC	H7	VBATS	H3
BDLIP	C7	MICBIAS	C11	NC	H8	VCABB	B9
BDLQM	B5	MICIN	D11	NC	H9	VCCS	H1
BDLQP	A6	MICIP	D12	NC	J5	VCDBB	L11
BDR	L12	NC	C6	NC	J6	VCHG	G1
BDX	M12	NC	C9	NC	J7	VCIO1	L1
BFSR	K11	NC	C10	NC	J8	VCIO2	L2
BFSX	J9	NC	D4	NC	K3	VCK	K12
BULIM	A4	NC	D5	NC	K6	VCMEM	M9
BULIP	C4	NC	D6	NC	K9	VCRAM	K7
BULQM	C3	NC	D7	NC	L7	VDR	G12
BULQP	A3	NC	D8	ON_nOFF	L5	VDX	H10
CK13M	M6	NC	D9	PCHG	G2	VFS	G11
CK32K	M5	NC	D10	PWON	A7	VLMEM	L8
DAC	J10	NC	E4	REFGND	D3	VLRTC	M3
DBBSCK	M8	NC	E5	RESPWONz	L4	VRABB	A9
DBBSIO	L6	NC	E6	RPWON	B7	VRDBB	M11
DBBSRST	K8	NC	E7	SIMCK	J2	VREF	D2
EARN	A11	NC	E8	SIMIO	K2	VRIO1	M1
EARP	A12	NC	E9	SIMRST	H2	VRIO2	M2
GNDA	C8	NC	E11	TCK	B3	VRMEM	L9
GNDAV	F11	NC	F4	TDI	B4	VRRAM	M7
GNDD	K1	NC	F5	TDO	C5	VRRTC	M4
GNDL1	A1	NC	F7	TDR	L10	VRSIM	J1
GNDL2	B1	NC	F8	TEN	M10	VSDBB	K10
HSMICBIAS	C12	NC	F9	TESTRSTz	B10	VXRTC	L3
HSMICP	E12	NC	G3	TESTV	A8		

Table 2−5 shows the terminal functions for the TWL3025 device.

Table 2−5. Terminal Functions

TERMINAL			SUPPLIES	I/O	DESCRIPTION	COMMENTS
NAME	GGM NUMBER	GQW NUMBER				
ADIN1	B6	E3	VRABB/GNDA	I/O	Monitoring ADC input 1 and battery temperature current source	
ADIN2	A6	E1	VRABB/GNDA	I/O	Monitoring ADC input 2 and battery type current source	
ADIN3	C7	E2	VRABB/GNDA	I	Monitoring ADC input 3 (spare)	
ADIN4	C6	F2	VRABB/GNDA	I	Monitoring ADC input 4 (spare)	
AFC	J4	J11	VRABB/GNDA	O	Automatic frequency control DAC output	External capacitor
APC	K4	J12	VRABB/GNDA	O	Automatic power control DAC output	
AUXI	G7	E10	VRABB/GNDAV	I	Auxiliary speech signal input	
AUXON	K10	B11	VRABB/GNDA	O	Auxiliary speech signal output (−)	
AUXOP	K9	B12	VRABB/GNDA	O	Auxiliary speech signal output (+)	
BDLIM	F10	B8	VRABB/GNDA	I	In-phase input (I−) baseband codec downlink	
BDLIP	F9	C7	VRABB/GNDA	I	In-phase input (I+) baseband codec downlink	
BDLQM	E9	B5	VRABB/GNDA	I	Quadrature input (Q−) baseband codec downlink	
BDLQP	E10	A6	VRABB/GNDA	I	Quadrature input (Q+) baseband codec downlink	
BDR	J3	L12	VRIO/GNDD	I	Baseband serial port receive data	
BDX	J2	M12	VRIO/GNDD	O	Baseband serial port transmit data	
BFSR	H3	K11	VRIO/GNDD	I	Baseband serial port receive frame synchronization	
BFSX	K2	J9	VRIO/GNDD	O	Baseband serial port transmit frame synchronization	
BULIM	D10	A4	VRABB/GNDA	O	In-phase output (I−) baseband codec uplink	
BULIP	D9	C4	VRABB/GNDA	O	In-phase output (I+) baseband codec uplink	
BULQM	C9	C3	VRABB/GNDA	O	Quadrature output (Q−) baseband codec uplink	
BULQP	C10	A3	VRABB/GNDA	O	Quadrature output (Q+) baseband codec uplink	
CK13M	E4	M6	VRIO/GNDD	I	13-MHz master clock input and BSP/TSP/USP clock	
CK32K	E2	M5	VRRTC/GNDD	I	32-kHz clock input	
DAC	H4	J10	VRABB/GNDA	O	Auxiliary 10-bit DAC output	
DBBSCK	F4	M8	VRIO/GNDD	I	SIM card shifters clock input	
DBBSIO	E5	L6	VRIO/GNDD	I/O	SIM card shifters data	External pullup
DBBSRST	G4	K8	VRIO/GNDD	I	SIM card shifters reset input	
EARN	J10	A11	VRABB/GNDA	O	Earphone amplifier output (−)	
EARP	J9	A12	VRABB/GNDA	O	Earphone amplifier output (+)	
GNDA	G10	C8	GNDA	I/O	Power ground return for VRABB	
GNDAV	G6	F11	REFGND	I/O	MICBIAS and AUXI ground	
GNDD	A3	K1	GNDD	I/O	Power ground return for VRIO/UPR	
GNDL1	B9	A1	GNDL	O	Ground for LED driver	
GNDL2	A9	B1	GNDL	O	Ground for LED driver (internally connected to GNDL1)	
HSMICBIAS	K8	C12	VRABB/GNDAV	O	Headset microphone bias supply	
HSMICP	K7	E12	VRABB/GNDAV	I	Headset microphone amplifier input	
HSO	H9	A10	VRABB/GNDAV	O	Headset 32-Ω driver (single ended)	

Table 2−5. Terminal Functions (Continued)

TERMINAL			SUPPLIES	I/O	DESCRIPTION	COMMENTS
NAME	GGM NUMBER	GGM NUMBER				
IBIAS	B7	D1	VRABB/REFGND	I/O	Bias current reference resistor (100 kΩ)	External resistor
ICTL	D6	F1	VCHG/GNDA	O	Charger external transistor control	
INT1/TEST1	H6	F12	VRIO/GNDD	I/O	Fast interrupt / Test pad 1 (default is INT1)	
INT2/TEST2	E6	F3	VRIO/GNDD	I/O	Microcontroller interrupt / Test pad 2 (default is INT2)	
ITWAKEUP	D2	K4	VRRTC/GNDD	I	Real-time wake-up input	
LEDA	B8	C2	VBAT/GNDL	I	LED driver: paging indicator	
LEDB1	B10	A2	VBAT/GNDL	I	LED driver: backlight (input 1)	
LEDB2	A10	B2	VBAT/GNDL	I	LED driver: backlight (input 2) (internally connected to LEDB1)	
LEDC	C8	C1	VCHG/GNDL	I	LED driver: charging device indicator	
MICBIAS	J8	C11	VRABB/GNDAV	O	Microphone bias supply	
MICIN	H7	D11	VRABB/GNDAV	I	Microphone amplifier input (−)	
MICIP	J7	D12	VRABB/GNDAV	I	Microphone amplifier input (+)	
ON_nOFF	E3	L5	VRRTC/GNDD	O	Digital baseband reset (@ each switch on)	
PCHG	B5	G2	VCHG/GNDA	O	Battery precharge output current	
PWON	F8	A7	VBAT/GNDD	I	On button input	Pullup
REFGND	A7	D3	REFGND	I/O	Reference voltage ground	
RESPWONz	D3	L4	VRRTC/GNDD	O	Digital baseband power-on reset (first battery plug)	
RPWON	F7	B7	VBAT/GNDD	I	Remote power-on (other than button)	Pullup
SIMCK	C4	J2	VRSIM/GNDD	O	SIM card shifters clock output (1.8 V/3 V)	
SIMIO	B3	K2	VRSIM/GNDD	I/O	SIM card shifters data (1.8 V/3 V)	External pullup
SIMRST	D4	H2	VRSIM/GNDD	O	SIM card shifters reset output (1.8 V/3 V)	
TCK	D8	B3	VRIO/GNDD	I	Scan test clock	Pulldown
TDI	D7	B4	VRIO/GNDD	I	Scan path input	Pullup
TDO	E7	C5	VRIO/GNDD	O	Scan path output	3-state
TDR	G3	L10	VRIO/GNDD	I	Time serial port input	
TEN	H1	M10	VRIO/GNDD	I	Time serial port enable	
TESTRSTz	H8	B10	UPR/GNDD	I	Reset input for test mode only	Pullup
TESTV	G8	A8	VBAT/GNDA	O	Voltage regulator output sense (reserved for test purpose)	
TEST3	J6	F10	VRIO/GNDD	I/O	Special test I/O terminals	Pullup
TEST4	F6	B6	VRIO/GNDD	I/O	Special test I/O terminals	Pullup
TMS	E8	A5	VRIO/GNDD	I	JTAG test mode select	Pullup
UDR	K5	H11	VRIO/GNDD	I	Microcontroller serial port receive data	
UDX	J5	H12	VRIO/GNDD	O	Microcontroller serial port transmit data	3-state
UEN	K6	G10	VRIO/GNDD	I	Microcontroller serial port enable	
UPR	C2	J4	UPR/GNDD	O	Uninterrupted power rail output	External capacitor
VBACKUP	E1	K5	VBACKUP/GNDD	I/O	Backup battery input	External capacitor
VBAT	A4	J3	VBAT/GNDA	I/O	Battery voltage sense input	External capacitor
VBATS	C5	H3	VBAT/GNDA	I	Battery voltage sense	
VCABB	G9	B9	VCABB/GNDA	I/O	Input of voltage regulator VRABB	
VCCS	D5	H1	VCHG/GNDA	I	Charging current sense	

Table 2−5. Terminal Functions (Continued)

TERMINAL			SUPPLIES	I/O	DESCRIPTION	COMMENTS
NAME	GGM NUMBER	GGM NUMBER				
VCDBB	K1	L11	VCDBB/GNDD	I/O	Input of voltage regulator VRDBB	
VCHG	A5	G1	VCHG/GNDA	I/O	Charger voltage input	External capacitor
VCIO1	A2	L1	VCIO/GNDD	I/O	Input 1 of voltage regulators VRIO and VRSIM	
VCIO2	A1	L2	VCIO/GNDD	I/O	Input 2 of voltage regulators VRIO and VRSIM (internally connected to VCIO1)	
VCK	K3	K12	VRIO/GNDD	O	Voiceband serial port clock	
VCMEM	G2	M9	VCMEM/GNDD	I/O	Input of voltage regulator VRMEM	
VCRAM	F2	K7	VCRAM/GNDD	I/O	Input of voltage regulator VRRAM	
VDR	F5	G12	VRIO/GNDD	I	Voiceband serial port receive data	
VDX	H5	H10	VRIO/GNDD	O	Voiceband serial port transmit data	
VFS	G5	G11	VRIO/GNDD	O	Voiceband serial port frame synchronization	
VLMEM	F3	L8	UPR/GNDD	I	Select output voltage of VRMEM	
VLRTC	C3	M3	UPR/GNDD	I	Select output voltage of VRRTC and VRDBB	
VRABB	H10	A9	VRABB/GNDA	O	Voltage regulator VRABB output	External capacitor
VRDBB	J1	M11	VRDBB/GNDD	O	Voltage regulator VRDBB output	External capacitor
VREF	A8	D2	VRABB/REFGND	I/O	Reference voltage (1.18 V)	External capacitor
VRIO1	B2	M1	VRIO/GNDD	O	Voltage regulator VRIO output 1	External capacitor
VRIO2	B1	M2	VRIO/GNDD	O	Voltage regulator VRIO output 2 (internally connected to VRIO1)	External capacitor
VRMEM	G1	L9	VRMEM/GNDD	O	Voltage regulator VRMEM output	External capacitor
VRRAM	F1	M7	VRRAM/GNDD	O	Voltage regulator VRRAM output	External capacitor
VRRTC	D1	M4	VRRTC/GNDD	O	Voltage regulator VRRTC output	External capacitor
VRSIM	B4	J1	VRSIM/GNDD	O	Voltage regulator VRSIM output	External capacitor
VSDBB	H2	K10	VRDBB/GNDD	I	Voltage regulator VRDBB input feedback	
VXRTC	C1	L3	VRRTC/GNDD	I/O	Reserved for test purposes	No external connection

3 Functional Description

This section describes the functional blocks that comprise the TWL3025 device. Figure 3−1 is a block diagram of the device.

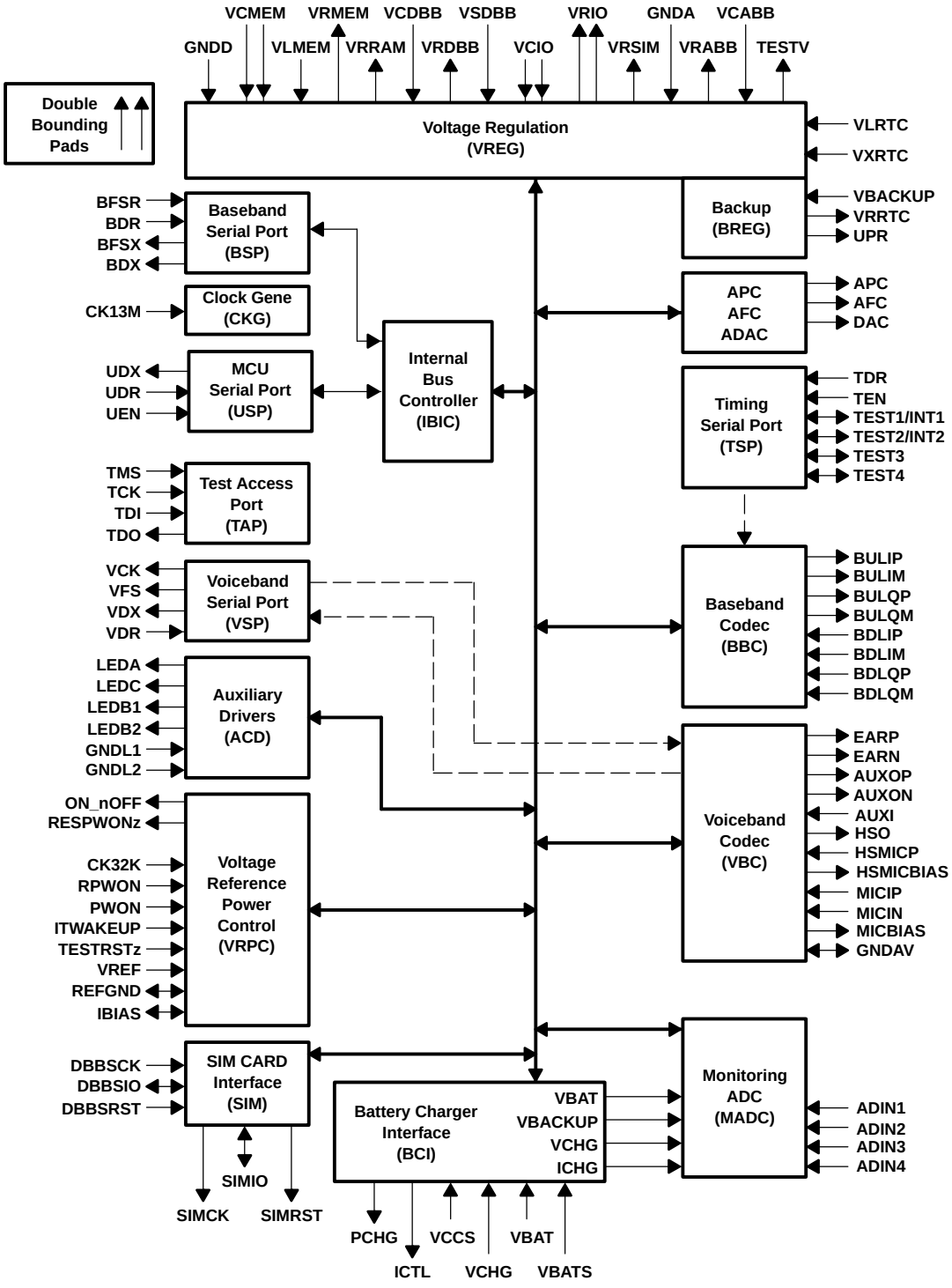


Figure 3−1. TWL3025 Functional Block Diagram

3.1 Voiceband Codec

The voiceband coder-decoder (codec) (VBC) circuit processes analog audio components in the voice uplink (VUL) path and transmits this signal to the DSP speech coder through the voiceband serial port (VSP). In the voice downlink (VDL) path, the codec converts the digital samples of speech data received from the DSP via the VSP port into analog audio signals.

The VBC includes an input amplifier for microphones (headset, phone, auxiliary) and an output amplifier (headset, phone speaker, auxiliary).

The VBC also performs the programmable gain, volume control, and side-tone functions.

3.2 Baseband Codec

The baseband codec (BBC) is composed of a baseband uplink (BUL) path and a baseband downlink (BDL) path.

The BUL path modulates the data bursts coming from the DSP via the baseband serial port (BSP). Modulation is performed by a Gaussian minimum shift keying (GMSK) modulator, according to GSM specification 5.04. The GMSK modulator, which is implemented digitally, generates the in-phase (I) and quadrature (Q) components. These components are converted into analog baseband by two 10-bit DACs and filtered by third-order low-pass filters. The BUL path includes secondary functions such as dc offset calibration and I/Q gain unbalance.

The BDL path converts the baseband analog I and Q components from the RF receiver into digital samples. The resulting signals are filtered through a digital FIR to isolate the desired data from the adjacent channels. During reception of the burst I and Q components, the digital data are sent to the DSP via the BSP at a rate of 270.833 kHz. The BDL path includes a dc offset calibration.

Timing windows of the BUL and BDL paths are controlled through the time serial port (TSP) by the TPU of the digital baseband (DBB) device.

Implementation of the BBC allows multislot and full-duplex operation.

3.3 Low-Dropout Linear Voltage Regulator

Several low-dropout (LDO) linear voltage regulators supply power to internal analog and digital circuits, to the DBB processor, and to external memory.

The first LDO (VRDBB) is a programmable regulator that generates the supply voltages (1.8 V, 1.5 V, and 1.3 V) for the core of the DBB processor. During all modes, the main battery directly supplies VRDBB.

The second LDO (VRIO) generates the supply voltage (2.8 V) for the digital core and I/Os of the TWL3025 device. During all modes, the main battery directly supplies VRIO.

The third LDO (VRMEM) is a programmable regulator that generates the supply voltages (2.8 V and 1.8 V) for external memories (typically flash memories) and DBB memory interface I/Os. During all modes, the main battery directly supplies VRMEM.

The fourth LDO (VRRAM) is a programmable regulator that generates the supply voltages (2.8 V and 1.8 V) for external memories (typically SRAM memories) and DBB memory interface I/Os. During all modes, the main battery directly supplies VRRAM. This LDO is also protected against reverse current.

The fifth LDO (VRABB) generates the supply voltage (2.8 V) for the analog functions of the TWL3025 device. During all modes, the main battery directly supplies VRABB.

The sixth LDO (VRSIM) is a programmable regulator that generates the supply voltages (2.9 V and 1.8 V) for SIM card and SIM card drivers. During all modes, the main battery directly supplies VRSIM.

3.4 Ultralow Current Consumption Features/Backup Battery Switch

Several low power features are implemented in the TWL3025 device:

The backup battery switch (BBS) generates at its output an uninterrupted power rail (UPR) to supply the minimum necessary circuitry of the power-control functions continuously, from either the main battery or the backup battery. This UPR is connected to the UPR terminal for decoupling purposes.

A seventh LDO (VRRTC) is a programmable regulator that generates the supply voltages (1.8 V, 1.5 V, and 1.3 V) for the real-time clock of the DBB processor and dedicated I/Os. During all modes, UPR supplies VRRTC. This LDO has an ultralow current consumption.

All other LDOs (VRDBB, VRIO, VRRAM, VRMEM, VRSIM, VRABB) have three modes:

- The OFF mode, LDO is not enabled.
- The SLEEP mode, LDO has a very low current consumption and can provide 1 mA.
- The ACTIVE mode, LDO can provide full range of current on its regulated output.

3.5 Monitoring ADC

The monitoring ADC (MADC) consists of a 10-bit analog-to-digital converter (ADC) combined with an 8-input analog multiplexer. Four of the eight inputs are available externally, and the remaining four inputs are dedicated to main battery voltage, backup battery voltage, charger voltage, and charger current monitoring. Of the four available external inputs, two are standard inputs, and the two that are associated with current sources are intended for battery temperature and battery type measurements.

Conversion requests, input/output channels, and results reading can be performed either through the BSP, through the USP, or through the TSP interface.

3.6 SIM Card Shifters (SIMS)

To allow the use of both 1.8-V and 3-V SIM card types, a SIM level-shifter module in the TWL3025 device interfaces the SIM signals (DBBSRST, DBBSIO, and DBBSCK) at a constant VRIO level from the DBB device with the SIM card (SIMRST, SIMIO, and SIMCK) at a 1.8-V or 3-V level depending on SIM type.

An LDO generates a 1.8-V or 2.9-V supply at the VRSIM terminal from the main battery voltage.

3.7 Voltage Reference/Power-On Control

The external resistor connected between the IBIAS and REFGND terminals sets the value of the bias currents of the analog functions from the band-gap voltage.

The voltage reference/power-on control (VRPC) block controls the power on, power off, switch on, and switch off sequences.

Some block functions are performed even in the off state. These permanent functions ensure the wake-up of the device, such as, ON/OFF button detection or charger detection.

Interrupts are generated either when a PWON event, RPWON event, or a charger plug/unplug is detected while the device is in power on or when abnormal voltage conditions are detected.

3.8 Baseband Serial Port

The baseband serial port (BSP) is a bidirectional (transmit/receive) serial port. Both receive and transmit operations are double-buffered and permit a continuous communication stream. Format is a 16-bit data packet with frame synchronization.

The CK13M master clock is used as a clock for both transmit and receive.

The BSP allows read and write access of all internal registers under the arbitration of the internal bus controller. But its transmit path is allocated to the BDL path during burst reception for I and Q data transmissions.

3.9 Time Serial Port

The time serial port (TSP) controls in real time the radio activation windows of the TWL3025 device: BUL power-on, BUL calibration, BUL transmit, BDL power-on, BDL calibration, BDL receive, and the ADC conversion start.

These real-time control signals are processed by the TPU of the DBB device and transmitted serially to the TWL3025 device via the TSP, which consists of a very simple two-terminal serial port. The TEN terminal is an enable, the TDR terminal is the data receive. The CK13M master clock divided by 2 is used internally as the clock for this serial port.

3.10 Microcontroller Serial Port

The microcontroller serial port (USP) is a synchronous serial port. It consists of three terminals: data transmit (UDX), data receive (UDR), and port enable (UEN). The clock signal is the CK13M master clock.

Transfers are initiated by the external microcontroller, which pushes data into the USP via the UDR, while synchronous data contained in the transmit buffer of the USP is pushed out via the UDX.

The USP allows read and write access of all internal registers under the arbitration of the internal bus controller.

3.11 Automatic Frequency Control

The automatic frequency control (AFC) function consists of a digital-to-analog converter (DAC) optimized for high-resolution dc conversion. The AFC controls the frequency of the GSM 13-MHz oscillator to maintain mobile synchronization on the base station and to allow proper transmission and demodulation.

The AFC provides 13-bit accuracy and a 2-V dynamic range.

3.12 Automatic Power Control

The automatic power control (APC) generates an envelope signal to control the power ramp up, power ramp down, and power level of the radio burst. The APC structure is intended to support single-slot and multislot transmissions with smooth power transitions when consecutive bursts are transmitted at different power levels.

The APC includes a DAC and a RAM, in which the shape of the edges (ramp up and ramp down) of the envelope signals are stored digitally. This envelope signal is converted to an analog signal by a 10-bit DAC.

Timing of the APC is generated internally and depends on the real-time signals coming from the TSP and the contents of two registers that control the relative position of the envelope signal versus the modulated I and Q components.

3.13 Auxiliary DAC

The auxiliary DAC (ADAC) is a general-purpose 10-bit DAC.

3.14 Battery Charger Interface

The main function of the TWL3025 battery charger interface (BCI) is to control the charging of either a 1-cell Li-Ion battery or a 3-series Ni-MH/Ni-Cd cell battery with the support of the microcontroller (the DBB device).

The battery is monitored using the 10-bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, and battery charger input voltage.

The magnitude of the charging current is set by 10 bits of a programming register converted by the 10-bit DAC, whose output sets the reference input of the charging current control loop.

The BCI also performs some auxiliary functions. These functions are battery precharge and back-up battery charge, if it is rechargeable.

The BCI is under register control. These registers can be programmed either through the BSP or through the USP.

3.15 Auxiliary Current Driver

Three LED drivers are also embedded.

The first one (LEDA) is dedicated for paging indication. The maximum current is 10 mA.

The second one (LEDB) is dedicated for keypad and screen backlight. The maximum current is 150 mA.

The third one (LEDC) is dedicated for charging indication. The maximum current is 10 mA. There is both a software control through the UPS or BSP interface and an automatic hardware control when the main battery precharge is enabled.

4 Detailed Description

4.1 Voice Codec

The voice codec circuitry processes analog audio components in the voice uplink (VUL) path and applies this signal to the voice signal interface for eventual baseband modulation. In the voice downlink (VDL) path, the codec circuitry changes voice component data received from the voice serial interface (VSP) into analog audio. The following paragraphs describe these uplink/downlink functions in more detail.

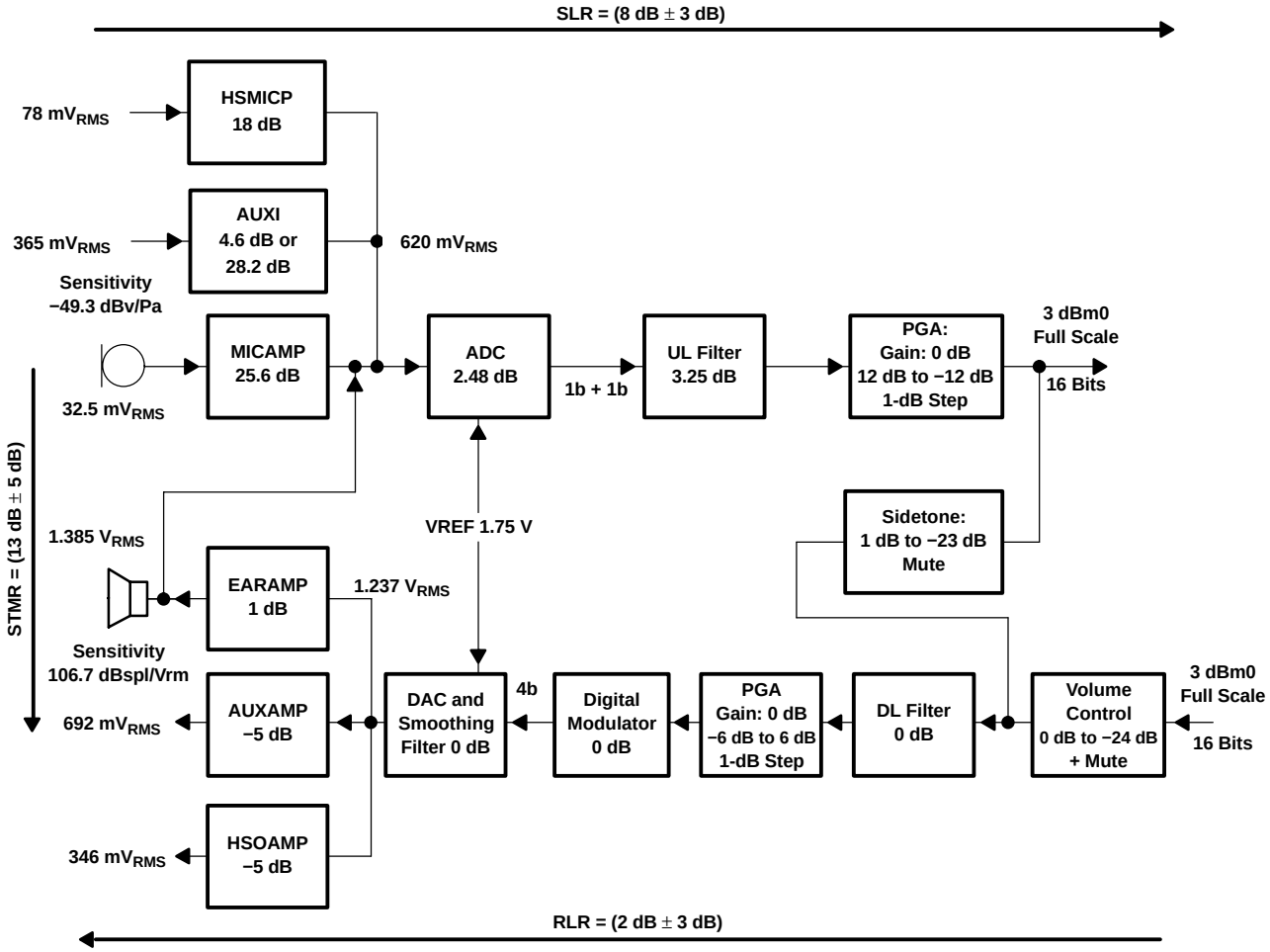


Figure 4−1. Voice Codec Block Diagram

4.2 Voice Uplink Path

The VUL path includes two input stages. The first stage is a microphone amplifier, compatible with electret microphones containing a FET buffer with open drain output. The microphone amplifier has a gain of typically 25.6 dB (±1 dB) and provides an external voltage of 2.0 V or 2.5 V to bias the microphone (MICBIAS). The auxiliary audio input can be used as an alternative source for higher level speech signals. This stage performs single-ended-to-differential conversion and provides a programmable gain of 4.6 dB or 28.2 dB. The third stage is a headset microphone amplifier, compatible with electret microphones. The headset microphone amplifier has a gain of typically 18 dB and provides an external voltage of 2.0 V or 2.5 V to bias the headset microphone (HSMICBIAS). When one of the input stages (MICI, AUXI, HSMICP) is in use, the two other input stages are disabled and powered down.

The resulting fully differential signal is fed to the analog-to-digital converter (ADC). The ADC conversion slope depends on the value of the internal voltage reference.

Analog-to-digital conversion is performed by a third-order Σ-Δ modulator with a sampling rate of 1 MHz. Output of the ADC is fed to a speech digital filter, which performs the decimation down to 8 kHz and band-limits the signal with both low-pass and high-pass transfer functions. Programmable gain can be set digitally from −12 dB to +12 dB in 1-dB steps and is programmed with bits 4−0 (VULPG(4:0)) of the voiceband uplink register (see Section 5.3.13.4). The speech samples are then transmitted to the DSP via the VSP at a rate of 8 kHz. There are 15 meaningful output bits.

Programmable functions of the VUL path, power-up, input selection, and gain are controlled by the BSP or the USP via the serial interfaces. The VUL path can be powered down by bit 0 (VULON) of the power down register (see Section 5.3.4.3).

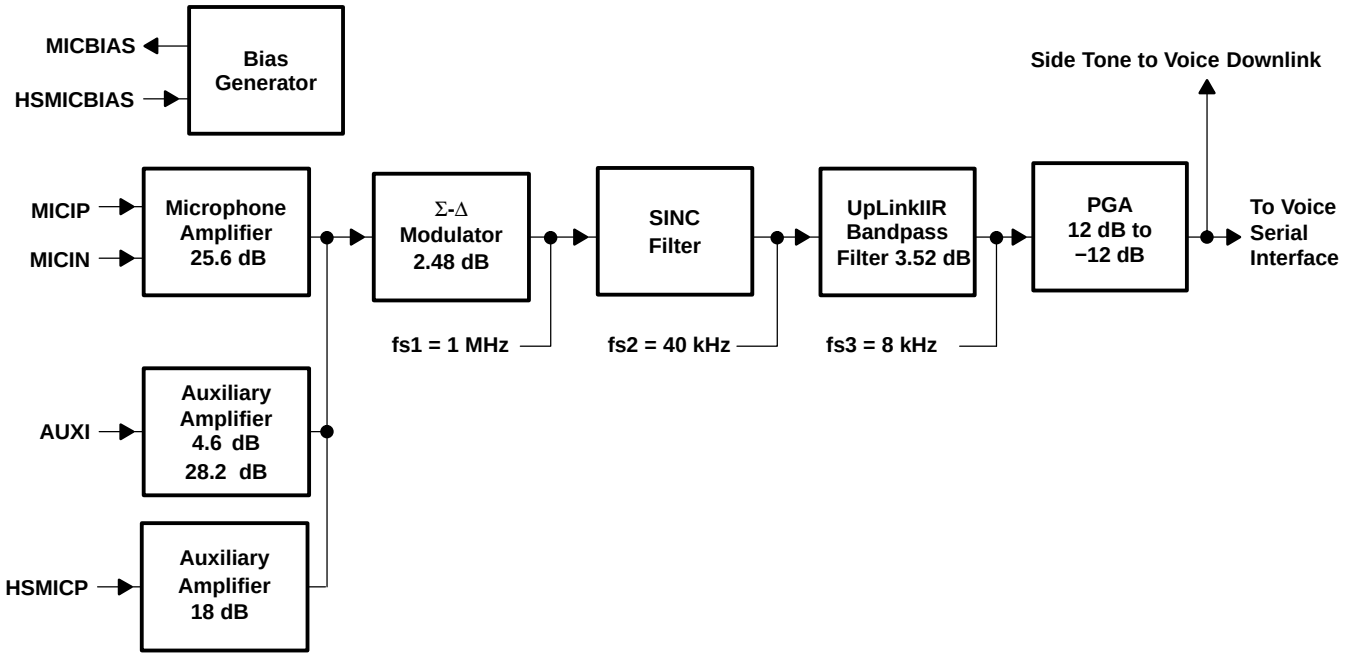


Figure 4−2. Voice Uplink Path

4.3 Voice Downlink Path

The VDL path receives speech samples at the rate of 8 kHz from the DSP via the VSP and converts them to analog signals to drive the external speech transducer.

The digital speech coming from the DSP is first fed to a speech digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate from 8 kHz up to 40 kHz to allow the digital-to-analog conversion to be performed by an oversampling digital modulator. The second function is to band-limit the speech signal with both low-pass and high-pass transfer functions. The filter, the PGA gain, and the volume gain can be bypassed by programming bit 9 (VFBYP) in the voiceband control register 1 (see Section 5.3.13.1).

The interpolated and band-limited signal is fed to a second order Σ-Δ digital modulator sampled at 1 MHz to generate a 4-bit (9 levels) oversampled signal. This signal is then passed through a dynamic element matching block and then to a 4-bit digital-to-analog converter (DAC).

The volume control and the programmable gain are performed in the voiceband digital filter. Volume control is performed in steps of 6 dB from 0 dB to −24 dB. In mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from −6 dB to +6 dB in 1-dB steps to calibrate the system depending on the earphone characteristics. This configuration is programmed with the voiceband downlink control register (see Section 5.3.13.5).

The earphone amplifier provides a full differential signal on the EARP and EARN terminals, an auxiliary output amplifier provides a differential signal on the AUXOP and AUXON terminals, and a headset output amplifier provides a single-ended signal on the HSO terminal. The VDL path can be powered down by bit 1 (VDLON) of the power down register (see Section 5.3.4.3).

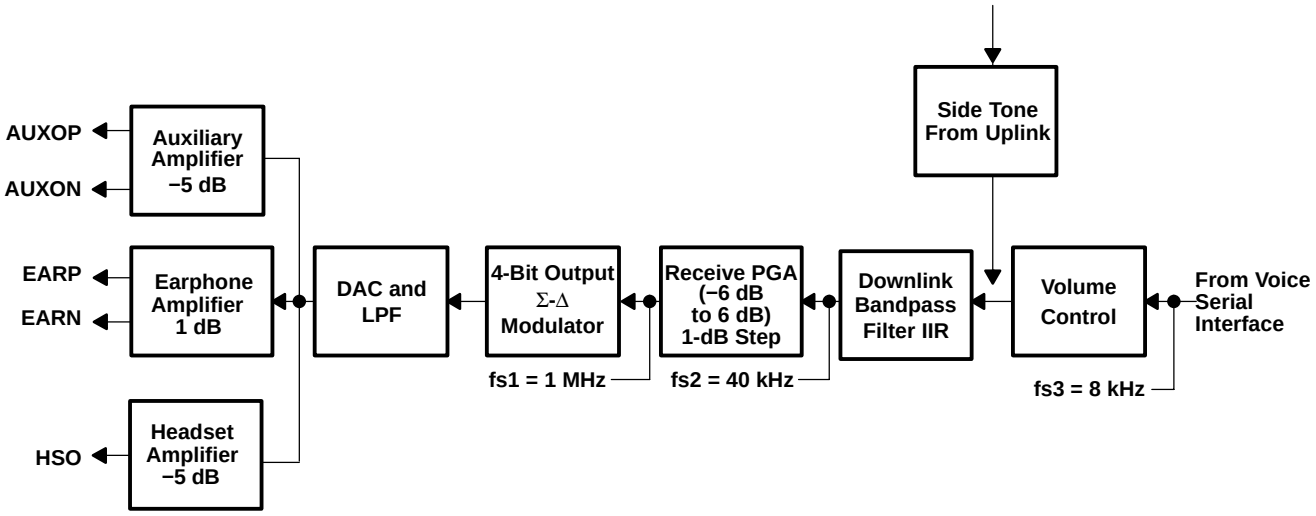


Figure 4−3. Voice Codec Downlink Path

4.4 Baseband Uplink and Downlink Path

The baseband codec includes a two-channel baseband uplink (BUL) path and a two-channel baseband downlink (BDL) path.

4.4.1 Baseband Uplink Path

The modulator circuit in the BUL path performs the Gaussian minimum shift keying (GMSK) in accordance with the GSM specification 5.04. The data to be modulated flows from the DSP radio interface (RIF) through the baseband serial port (BSP).

The GMSK modulator is implemented digitally, the Gaussian filter computed on 4 bits of the input data stream being encoded in the sine/cosine look-up tables in ROM, and it generates the in-phase (I) and quadrature (Q) digital samples with an interpolation ratio of 16.

These digital I and Q words are sampled at 4.33 MHz and applied to the inputs of a pair of 10-bit DACs. The analog outputs are then passed through third-order Bessel filters to reduce out-of-band noise and image frequency and to obtain a modulated output spectrum consistent with GSM specification 05.05.

Fully differential signals are available at the BULIP, BULIM, BULQP, and BULQM terminals.

To minimize phase trajectory error, the dc offset of the I and Q channels can be minimized using offset calibration capability. During offset calibration, input words of the 10-bit DACs are set to zero code and a 6-bit sub-DAC is used to minimize the dc offset at analog outputs.

The entire content of a burst, including guard bits, tail bits, and data bits, is stored in one of two 160-bit burst buffers before starting the transmission. The presence of two burst buffers is dictated by the need to support multislot transmission: one buffer is loaded with new data while the content of the second buffer is pushed into the GMSK modulator for transmission.

Single-slot or multislot mode is selected by bit 5 (MSLOT) of the baseband codec control register (see Section 5.3.12.8). When single-slot mode is selected, only the content of burst buffer 1 is used for modulation.

Output level can be selected with bits 8−6 (OUTLEV[2:0]) of the baseband codec control register.

The typical sequence of burst transmission consists of:

1. Power up the BUL path
2. Perform an offset calibration (not mandatory)
3. Modulate the content of the burst buffer

Timing of this sequence is controlled via the TSP, which receives serial real-time control signals from the TPU of the digital baseband (DBB) device. Three real-time signals control the transmission of a burst: BULON, BULCAL, and BULENA. Each signal corresponds to a time window.

BULON high sets the BUL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. BULCAL enables the offset calibration window. During BULCAL, inputs of 10-bit DACs are forced to code zero and a low-offset comparator senses the dc level at the BULIP/BULIM and BULQP/BULQM terminals. The result of the comparison modifies the content of the offset registers, which drives the 6-bit sub-DACs to minimize the offset error. The duration of the calibration phase depends on the time needed to sweep the sub-DAC dynamic range. Modulation starts with the rising edge of BULENA and ends 32 one-quarter bits after the falling edge of BULENA. At the end of modulation, the modulator is reinitialized by setting the pointers of burst buffers and the filter ROM to the base address. The I vector is set to its maximum value, while the Q vector is set to 0.

The output common mode voltage of the BULIP, BULIM, BULQP, and BULQM terminals can be set to several values by bits 2−0 (SELVMID[2:0]) of the baseband codec control register.

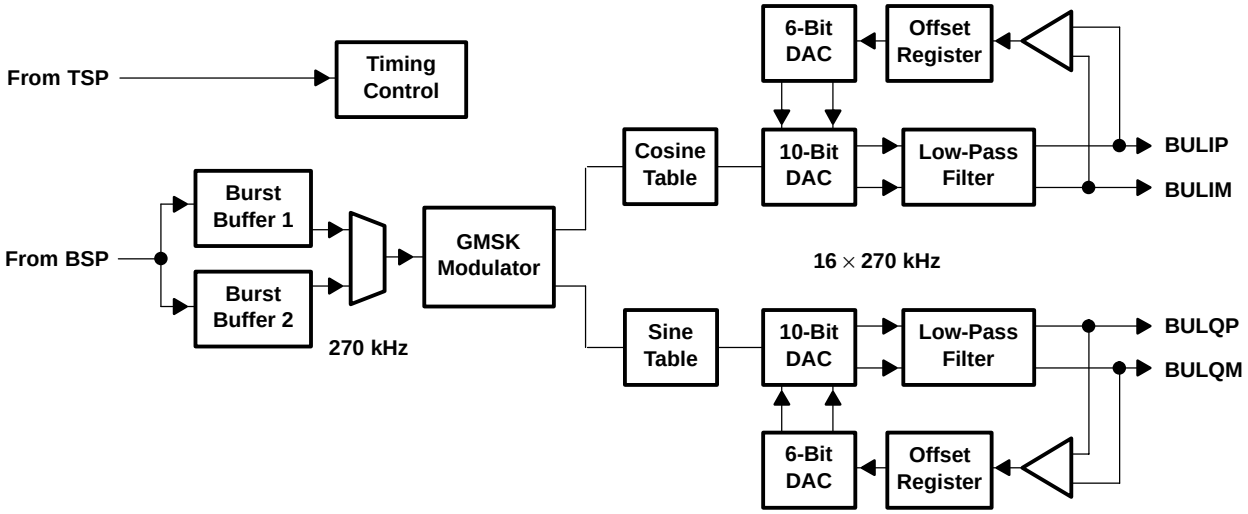


Figure 4−4. Baseband Uplink Block Diagram

4.4.2 Baseband Downlink Path

The BDL path includes two identical circuits for processing the analog baseband I and Q components generated by the RF circuits. The first stage of the BDL path is a continuous second-order antialiasing filter that prevents aliasing of out-of-band frequency components due to sampling in the ADC. This filter serves also as an adaptation stage between external and on-chip circuitry.

The antialiasing filter is followed by a fourth-order Σ-Δ modulator that performs analog-to-digital conversion at a sampling rate of 6.5 MHz. The ADC provides 2-bit words to a digital filter that performs the decimation by a ratio of 24 to lower the sampling rate to 270.833 kHz. The ADC also provides channel separation by providing enough rejection of the adjacent channels to allow the demodulation performances required by the GSM specification.

The BDL path includes an offset register, in which the value representing the channel dc offset is stored. This value is subtracted from the output of the digital filter before transmitting the digital samples to the DSP via the BSP. Upon reset, the offset register is loaded with 0s; its content is updated during the calibration process.

The typical sequence of burst reception consists of:

1. Power up the BDL path
2. Perform an offset calibration
3. Convert and filter the I and Q components and transmit digital samples

Timing of this sequence is controlled via the TSP, which receives serial real-time control signals from the TPU of the DBB device. Three real-time signals control the transmission of a burst: BDLON, BDLCAL, and BDLENA. Each signal corresponds to a time window.

BDLON high sets the BDL path in power-on mode after a delay corresponding to the power-on settling time of the analog block. BDLCAL enables the offset calibration window. Two offset calibration modes are possible and are selected by the state of bit 9 (EXTCAL) of the baseband codec control register. When EXTCAL is 0, the analog inputs are disconnected from the external world and internally shorted. The result of conversion done in this state is stored in the offset register. When EXTCAL is 1, the analog input remains connected to external circuitry, and the result of conversion, including in this case internal offset plus external circuitry offset, is stored in the offset register. The duration of the calibration window depends mainly on the settling time of the digital filter.

Data conversion starts with the rising edge of the BDLENA signal; however the first eight I and Q samples are not transmitted to the DSP, because they are not meaningful due to the group delay of the digital filter. The rising edge of BDLENA is also used by the IBIC to affect the transmit path of the BSP to the BUL path during the entire reception window. At the falling edge of BDLENA, the conversion in progress is completed and samples transmitted before stopping the conversion process. Finally, BDLON low sets the BDL path in power-down mode.

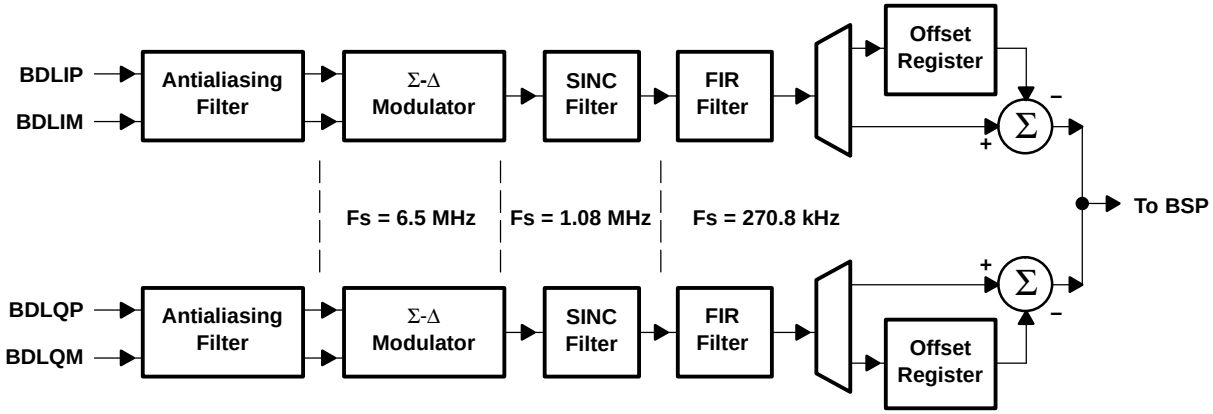


Figure 4−5. Baseband Downlink Block Diagram

4.5 Low-Dropout Voltage Regulators

The voltage regulation block consists of seven subblocks.

Several low-dropout (LDO) regulators perform linear voltage regulation. These regulators supply power to internal analog and digital circuits, to the DBB processor, and to external memory.

The first LDO (VRDBB) is a programmable regulator that generates the supply voltages (1.8 V, 1.5 V, and 1.3 V) for the core of the DBB processor. During all modes, the main battery directly supplies VRDBB.

The second LDO (VRIO) generates the supply voltage (2.8 V) for the digital core and I/Os of the TWL3025 device. During all modes, the main battery directly supplies VRIO.

The third LDO (VRMEM) is a programmable regulator that generates the supply voltages (2.8 V and 1.8 V) for external memories (typically flash memories) and DBB memory interface I/Os. During all modes, the main battery directly supplies VRMEM.

The fourth LDO (VRRAM) is a programmable regulator that generates the supply voltages (2.8 V and 1.8 V) for external memories (typically SRAM memories) and DBB memory interface I/Os. During all modes, the main battery directly supplies VRRAM.

The fifth LDO (VRABB) generates the supply voltage (2.8 V) for the analog functions of the TWL3025 device. During all modes, the main battery directly supplies VRABB.

The sixth LDO (VRSIM) is a programmable regulator that generates the supply voltages (2.9 V and 1.8 V) for SIM card and SIM card drivers. During all modes, the main battery directly supplies VRSIM.

The TWL3025 allows three operating modes for each of these voltage regulators:

1. ACTIVE mode during which the regulator is able to deliver its full power
2. SLEEP mode during which the output voltage is maintained with a very low power consumption but with a low current capability
3. OFF mode during which the output voltage is not maintained and the power consumption is null

The regulators rise up in ACTIVE mode only and each of them has a regulation ready signal RSU. In switched-off and backup states of the mobile phone, the voltage regulators will be set to a SLEEP or OFF mode depending on the system requirements. The regulator voltages are decoupled by a low ESR capacitor connected across the corresponding V_{CC} and ground terminals. Besides its voltage filtering function, this capacitor also has a voltage storage function that could give a delay for data protection purposes when the main battery is unplugged.

The seventh LDO (VRTC) is a programmable regulator that generates the supply voltages (1.8 V, 1.5 V, and 1.3 V) for the real-time clock and the 32-kHz oscillator located in the DBB device during all modes. The main or backup battery supplies VRTC.

4.5.1 VRDBB

VRDBB is an LDO voltage regulator that provides the power to the digital core located in the DBB device. VRDBB is supplied from the main battery (VCDBB) and delivers a programmable regulated voltage (VRDBB). The external sense (VSDBB) has to be connected to the VRDBB terminal. The VRDBB value is programmable (three values) through the use of bits 6−5 (RDBB1 and RDBB0) of the VRPC configuration register (see Section 5.3.1.1) and the VLRTC terminal which gives the reset value of this register.

4.5.2 VRRAM

VRRAM is an LDO voltage regulator that provides the power to external memory devices used in the GSM system (SRAM). VRRAM is supplied from the main battery (VCRAM) and provides a programmable regulated voltage (VRRAM). The VRRAM output value can be set to 1.8 V or 2.8 V using an external input signal (VLMEM). The voltage regulator prevents reverse current leakage.

4.5.3 VRMEM

VRMEM is an LDO voltage regulator that provides the power supply to external memory devices used in the GSM system (FLASH). VRMEM is supplied from the main battery (VCMEM) and provides a programmable regulated voltage (VRMEM). The VRMEM output value can be set to 1.8 V or 2.8 V using an external input signal (VLMEM).

4.5.4 VRIO

VRIO is an LDO voltage regulator providing the power supply to peripherals of the DBB device (including the I/O and the digital core of the TWL3025 device). VRIO is supplied from the main battery with two terminals (VCIO1) and (VCIO2), which are connected together internally. VRIO provides a 2.8-V regulated voltage on two output terminals (VRIO1) and (VRIO2), which are also connected together internally. The TWL3025 device requires also externally connecting VCIO1 to VCIO2 and VRIO1 to VRIO2.

4.5.5 VRABB

VRABB is an LDO voltage regulator providing the power supply to the analog blocks of the TWL3025 device. VRABB is supplied from the main battery (VCABB) and delivers a 2.8-V regulated voltage (VRABB). A separate ground return terminal (GNDA) is provided for the internal TWL3025 analog circuitry.

4.5.6 VRSIM

VRSIM is an LDO voltage regulator providing the power supply to the SIM card driver of the TWL3025 device. VRSIM is supplied from the main battery (VCIO1 and VCIO2) and delivers a 2.9-V or 1.8-V regulated voltage (VRSIM). The SimCard control register (see Section 5.3.8) controls the VRSIM voltage regulator.

4.5.7 VRRTC

VRRTC is an LDO voltage regulator that provides the power supply to the real-time clock and the 32-kHz oscillator located in the DBB device. VRRTC is supplied from the UPR line, switched on the main or backup battery, depending on the mobile phone state. VRRTC provides a programmable regulated voltage (VRRTC) and is always ON, as long as a valid energy source is present. The VRRTC output value can be set to 1.3 V, 1.5 V, or 1.8 V using an external input signal (VLRTC) and bits 8−7 (RRTC[1:0]) in the VRPC configuration register (see Section 5.3.1.1). The current load capability and the power consumption of this regulator are very low.

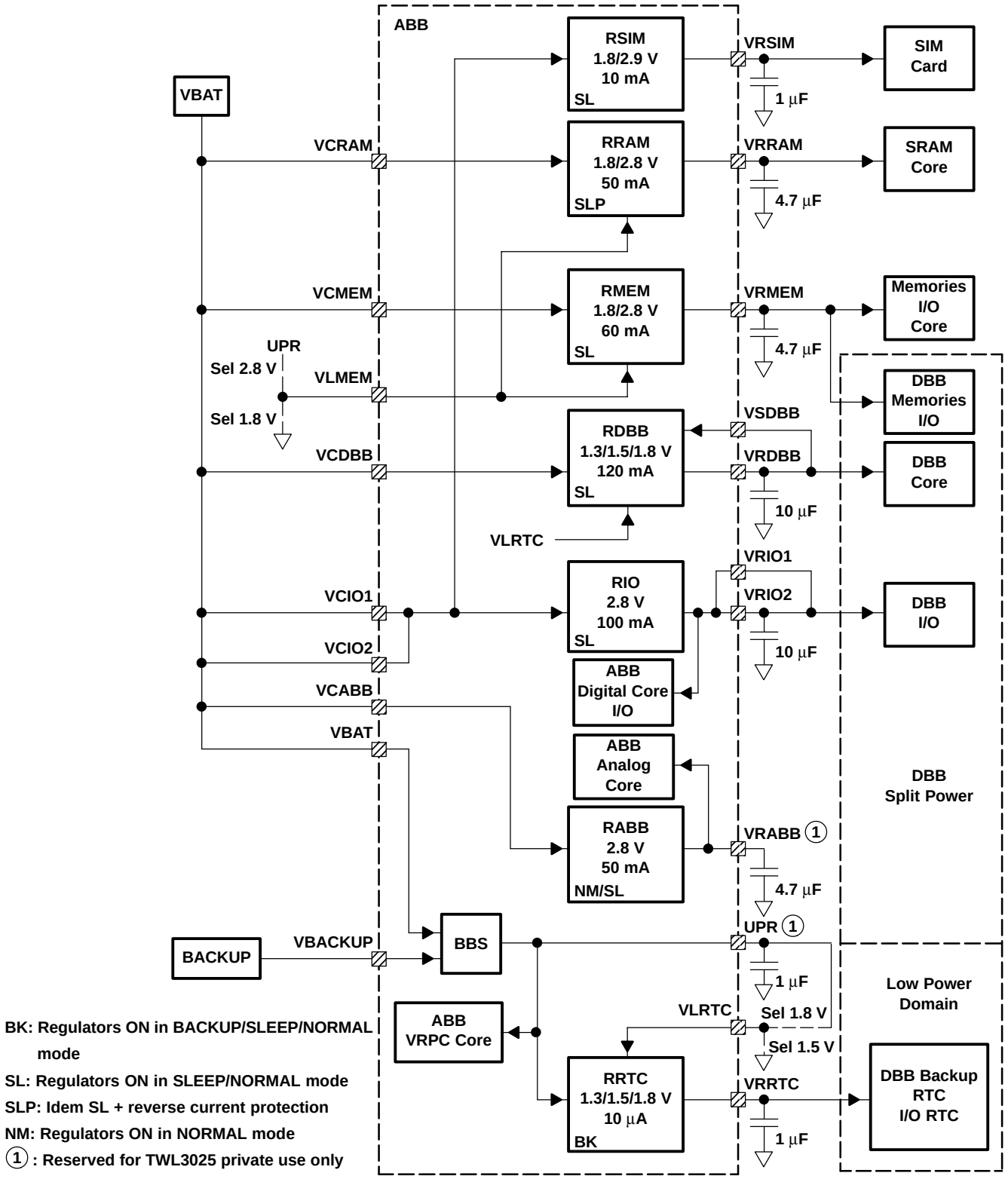


Figure 4−6. Voltage Supply System Block Diagram

4.6 Monitoring ADC

The monitoring section includes a 10-bit ADC and 10-bit/15-word RAM. The ADC monitors:

- Four internal analog values:
  - Battery voltage (VBAT)
  - Battery charger voltage (VCHG)
  - Current charger (current-to-voltage (I-to-V) converter) (ICHG)
  - Backup battery voltage (VBACKUP)
- Four external analog values:
  - Battery type (ADIN1)
  - Battery temperature (ADIN2)
  - ADIN3
  - ADIN4

The selection of the input and reading of the control registers is done via the serial interfaces.

The power down is controlled by bit 4 (MADCON) of the power down register (see Section 5.3.4.3). If bit 5 (KEEPON) of the power down register is high, the ADC converter is always on, even after a sequence of conversions. If KEEPON is low, the ADC converter is on after a conversion request and it is automatically off at the end of a sequence of conversions.

- Process to start a conversion:
  - Enable MADC (bit 9 (MADCS) in the toggle bits register 1 (see Section 5.3.4.1))
  - Select a channel to convert
  - Select MESBAT (bit 0 of the battery control 1 register (see Section 5.3.10.2)) or MESBB (bit 6 of the battery charging configuration register (see Section 5.3.10.4)) in case of a main battery or backup battery measurement
  - Start conversion:

    USP or BSP access (see the monitoring ADC control registers (Section 5.3.2.1)), or

    TSP access (see TSP interface timing requirements (Section 6.12), set the STARTADC bit and then clear the STARTADC bit)
  - Wait for the end of conversion by either:

    Waiting for the clearing of ADCBUSY (bit 0 of the monitoring ADC status register (see Section 5.3.3.1)), or

    Waiting for an INT2 MADC event
  - Read results
- At the end of a conversion cycle, an interrupt INT2 can be sent to the DBB

4.7 SIM Card Supply Voltage Generation

To accommodate the 1.8-V or 3-V SIM cards, the SIMS block includes an LDO voltage regulator that delivers supply voltage VRSIM to the SIM module.

The LDO voltage regulator is configured to generate the 1.8-V or 2.9-V (VRSIM) supply. The VRSIM terminal is decoupled by a capacitor (1-µF range).

The SIM card supply voltage generation is controlled by the following setoff control bits:

- Bit 0 (SIMSEL) of the SimCard control register (see Section 5.3.8) selects the VRSIM output voltage (1.8 V or 2.9 V).
- Bit 1 (RSIMEN) of the SimCard control register enables the 1.8-V/2.9-V series regulator.
- Bit 2 (SIMRSU) of the SimCard control register is the VRSIM regulator status.
- Bit 3 (SIMLEN) of the SimCard control register enables the SIM interface level shifter (on the SIMCK, SIMRST, and SIMIO terminals).

The above control bit default and initial values when the microcontroller is not active are entirely under the control of the VRPC block.

4.8 SIM Card Digital Interface

The SIM card digital interface ensures the translation of logic levels between the DBB device and the SIM card for the transmission of three different signals: a clock derived from a clock elaborated in the DBB device to the SIM card (DBBSCK−SIMCK), a reset signal from the DBB device to the SIM card (DBBSRST−SIMRST), and serial data from the DBB device to SIM card (DBBSIO−SIMIO) and vice-versa.

External pullup resistors must be connected between the DBBSIO terminal and either the VRIO1 or VRIO2 terminal and between the SIMIO and VRSIM terminals.

Control bit 3 (SIMLEN) (1/0) of the SimCard control register (see Section 5.3.8) activates/deactivates the transmission of these signals.

When SIMLEN is 0, there is a low impedance 0 on the SIMRST, SIMCK, and SIMIO terminals. This is also the case when there is no power on the SIM card, that is, when VRSIM = 0 V.

4.9 SIM Card Presence Detection

This function is not implemented on the TWL3025 device but on the DBB device. However, a description of this function can contribute to understanding of the SIM card operation. When the SIM card is inserted, a mechanical contact connected on the DBB device terminal SIMDETECT is tripped and, after debouncing, an interruption of the microcontroller is generated. Bit 1 (RSIMEN) of the SimCard control register (see Section 5.3.8) in the TWL3025 device is then set to 1 through the USP interface. The microcontroller has to wait for the regulation ready signal RSU from the VRSIM regulator by reading bit 2 (SIMRSU) in SimCard control register, and then setting bit 3 (SIMLEN) of the SimCard control register. A reset, a clock, and data can be sent to the SIM card.

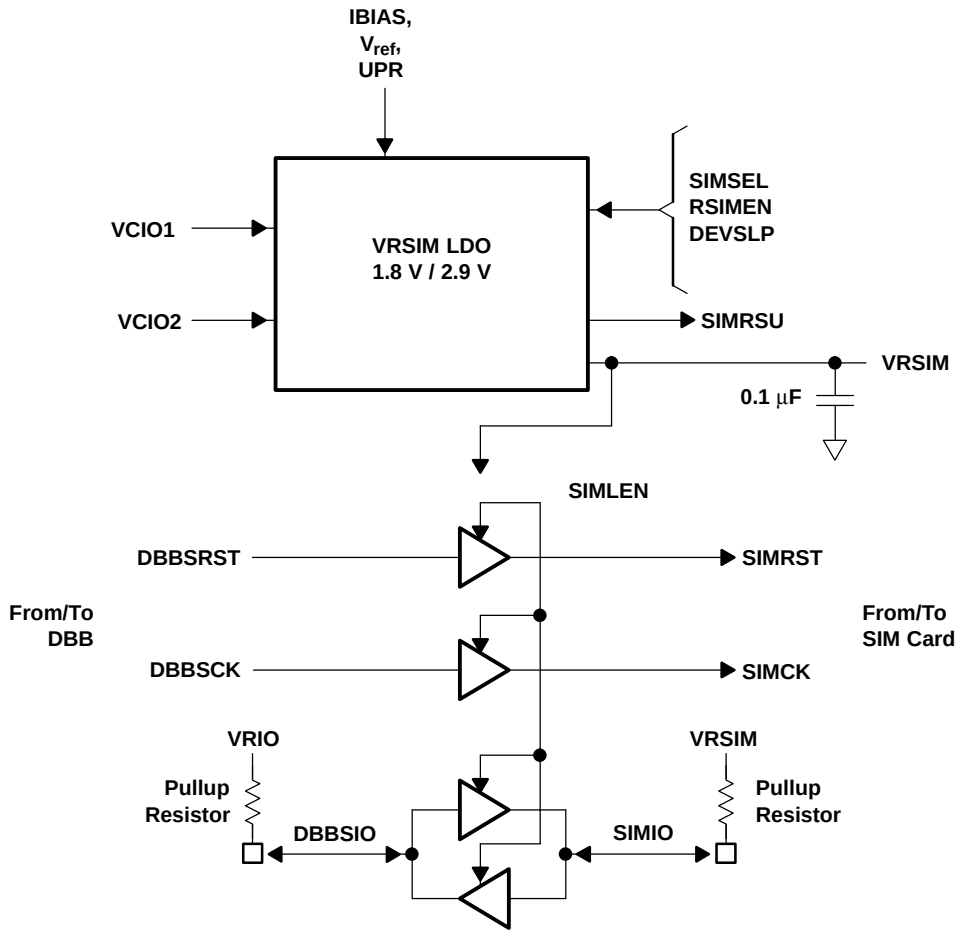


Figure 4−7. SIM Interface Block Diagram

4.10 Reference Voltage and Power Control

The band-gap voltage reference is filtered (RC filter) using an external capacitor connected across the VREF output and an analog ground (REFGND). The VREF voltage is scaled, distributed, and buffered inside the device. The band-gap is started in the fast mode (not filtered) and is set automatically by the VRPC in the slow mode (filtered, less noisy) after a switch-on sequence.

The bias currents of the TWL3025 analog blocks are generated using an external resistor connected across the IBIAS terminal and an analog ground (REFGND). The current flowing through this resistor is then multiplied, mirrored, and distributed across the device.

A power-on reset (POR) block provides a reset signal for the VRPC state machine. This reset signal becomes high when the internal power supply rail (UPR) reaches (2.6 V) on a rising edge and comes back low when the power supply rail reaches (2.1 V) on a falling edge. The POR block forces internal signal RSTz low as soon as possible during UPR ramp-up until UPR has passed the minimum operating voltage limit. For testing purposes, the TESTRSTz terminal provides an unconditional reset to the TWL3025 device.

UVLO is a comparison block. It compares the battery voltage to a reference (3.2 V). This second comparator has an hysteresis of 200 mV (below the threshold voltage of 3.2 V) to avoid the effects of variations of the main battery voltage when exceeding 3.2 V. The result of this comparison determines whether the next step can be reached during the logic from the OFF state to the ACTIVE state during a switch-on sequence.

BBS has also a comparison block. It compares the battery voltage to a reference (2.8 V). The result of this comparison generates an INT1 interrupt, the VRPC automatically executes a switch-off sequence from any state to the BACKUP state.

VRPCD is a digital block that is mainly composed of state machines and timers to control the switch-on and switch-off sequences.

4.10.1 Definitions

States:

- NOBAT state: the mobile phone is not powered by any battery.
- BACKUP state: the mobile phone is powered only with the backup battery and maintains only the VRRTC supply.
- OFF state: the mobile phone is powered by the main battery and maintains only the VRRTC supply.
- ACTIVE state: the mobile phone is powered by the main battery, all supplies are enabled, internal ABB reset is released.
- SLEEP state: the mobile phone is powered by the main battery, selected supplies are enabled, ABB device is in low consumption mode.

State transitions:

- Power on: charged main battery or backup battery plug
- Power off: the mobile phone is not powered by any battery and is switched from any state to the NOBAT state.
- Switch on: the mobile phone is powered and awaken from the OFF state to reach the ACTIVE state.
- Switch off: the mobile phone is powered and switched from the ACTIVE or SLEEP state to reach the OFF or BACKUP state.

4.10.2 Power-On Condition

On the plug-in of the valid main battery, an internal reset is generated (POR).

After a power-on sequence, the TWL3025 device is in the OFF state.

4.10.3 Power-Off Condition

This state is reached when there is not enough voltage in the main battery and the backup battery or when both batteries are disconnected.

4.10.4 Switch-On Condition

The PWON or RPWON button is debounced by embedded hardware. Only one button can be debounced at a time. If the other button is pushed when the first button is currently in the debounce process, the second is queued and will be debounced after the first debouncing is finished. The debounce time is approximately 30 ms.

ON PWON: When a falling edge, after debouncing, is detected on the PWON terminal.

ON REMOTE: When a falling edge, after debouncing, is detected on the RPWON terminal.

IT_WAKE_UP: When a rising edge is detected on the ITWAKEUP terminal.

CHARGER_IC plugged. When a charger voltage is above VBAT + 0.4 V on the VCHG terminal.

When these conditions occur in the switch-off state, the switch-on sequence is started and controlled by the VRPC.

There are two cases when these conditions do not start the switch-on sequence:

- When the main battery is under 3.2 V
- When the system is in backup mode (power is supplied by the backup battery)

NOTE: The switch-on and switch-off sequences require the 32-kHz clock on the CK32K terminal.

PARAMETER	TEST CONDITIONS	TESTRSTz = 1
NBG	No switch-on on TESTRSTz	1031
NDL1	No switch-on on TESTRSTz	21
NDL2	No switch-on on TESTRSTz	14

4.10.5 Switch-Off Condition

On MCU command: when the microcontroller sets bit 0 (DEVOFF) of VRPC device mode register (see Section 5.3.1.2) to 1

On main battery removal, when the main battery voltage is lower than 2.8 V (emergency condition)

When the level of the main battery decreases below 2.8 V and below the level of the backup battery (emergency condition)

NOTE: When a switch-off sequence is started, the sequence is completed even if a switch-on condition occurs.

In the switch-on state, any switch-on condition is not considered but can generate an interrupt (charger IC plug, PWON terminal, RPWON terminal).

4.10.6 Interrupt Handling

The VRPC block handles two kinds of interrupts.

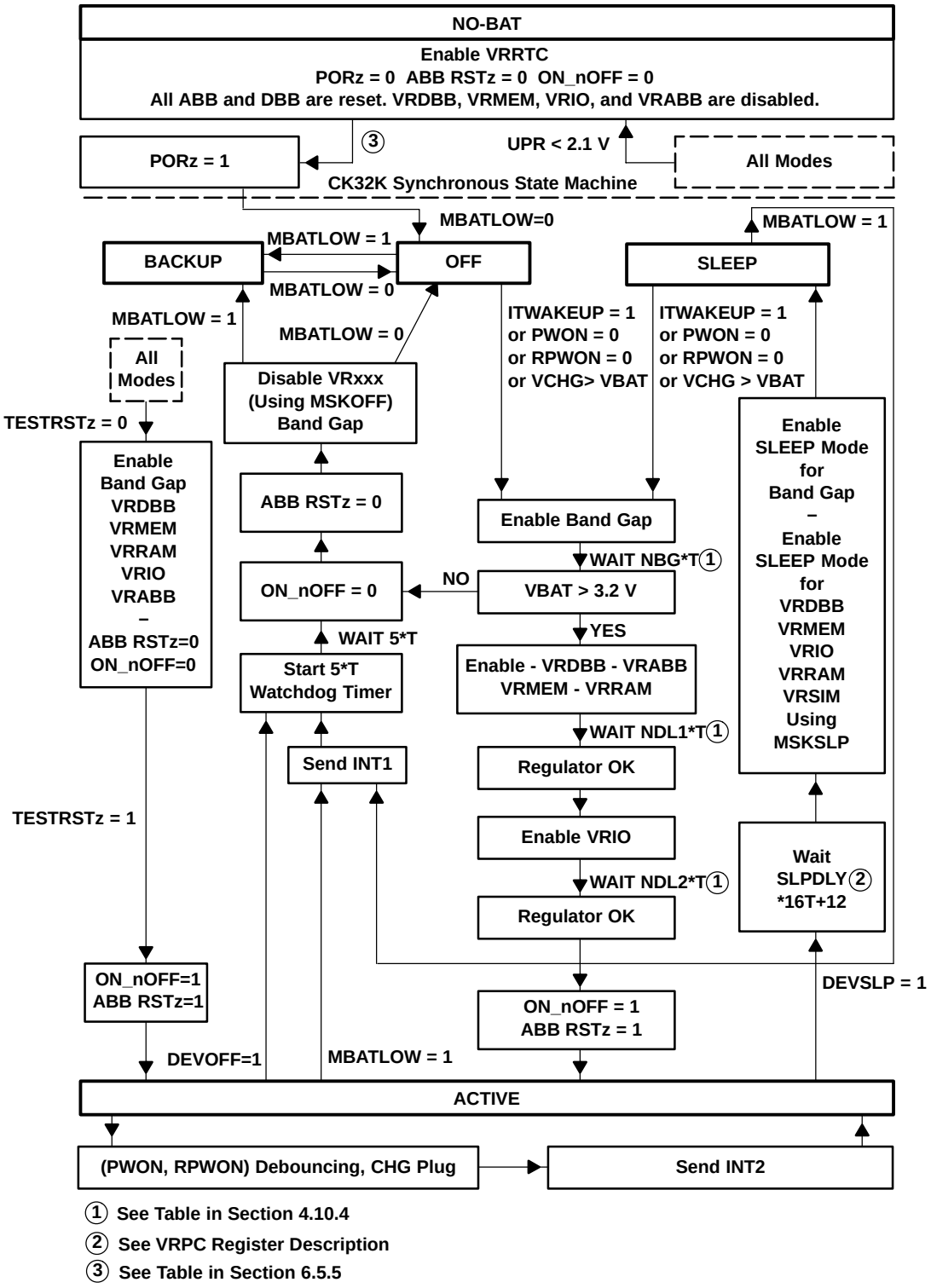
- INT1: This interrupt is related to the voltage level of the main battery resulting in an emergency switch-off procedure. This interrupt is considered as priority and sets the INT1 terminal to low level. This interrupt is masked if the ABB device is switched on with a TESTRSTz signal.
- INT2: This interrupt is related to accessories being plugged/unplugged or the push button. These interrupts can generate a signal sent on the INT2 terminal active on low level, depending on the interrupt mask register. Events generating an INT2 are:
  - The charger is plugged or unplugged (managed by battery charger interface).
  - The user pushes ON button (to activate a switch off).
  - There is a rising edge or a falling edge after debouncing on the RPWON terminal.

  NOTE: There is another source of INT2: the monitoring ADC end-of-conversion interrupt.

The INT2 interrupts are generated in the ACTIVE and SLEEP modes. INT2 generation needs an internal clock CK13M or CK32K. Set bit 6 (ACTIVMCLK) in the power down register (see Section 5.3.4.3) properly in case CK13M is not present.

PARAMETER	TEST CONDITIONS	NDEB
Debouncing PWON or RPWON	RPWON = 1, measure between falling edge PWON and INT2. No switch-on on TESTRSTz.	1034

Debouncing delay is NDEB*period of CK32K clock.



① See Table in Section 4.10.4
② See VRPC Register Description
③ See Table in Section 6.5.5

Figure 4−8. VRPC State Machine Flowchart

4.11 Automatic Frequency Control

The automatic frequency control function (AFC) consists of a DAC optimized for high-resolution dc conversion. The AFC digital interface includes two registers that can be written or read using either the BSP or the USP under the arbitration of the IBIC. The content of these registers controls a 13-bit DAC, operating at a sampling frequency of 2.165 MHz (or 1.08 MHz, 541 kHz, 270 kHz setting correctly the AFC working frequency register (see Section 5.3.5.3)), whose purpose is to correct frequency shifts of the voltage-controlled oscillator to maintain the GSM 13-MHz master clock frequency in a 0.1-PPM range.

The AFC value is programmed with the automatic frequency control register 1 (which contains the 10 LSBs) (see Section 5.3.5.1) and automatic frequency control register 2 (which contains the 3 MSBs) (see Section 5.3.5.2). The three MSBs are fed to the DAC through automatic frequency control register 2, whose content is updated with the content of a shadow register when LSBs are written in automatic frequency control register 1, so proper operation of the AFC is ensured by writing the MSBs first and then the LSBs.

Monotonicity is ensured by the structure of the DAC, with Σ-Δ digital modulators followed by an analog FIR, which performs one-bit digital-to-analog conversion and low-pass filtering. Further low-pass filtering is provided by the RC formed by the internal output resistor (25 kΩ) and an external capacitor (33 nF). However, most of the filtering is ensured by a voltage-controlled oscillator with a high quality factor to provide a very low-frequency low-pass filtering.

Bit 3 (AFCON) of the power down register (see Section 5.3.4.3) controls the power up of the AFC.

4.12 Automatic Power Control

The automatic power control (APC) generates an envelope signal to control the power ramp up, power ramp down, and power level of the radio burst. The APC structure is intended to support single-slot and multislot transmission with smooth power transition when consecutive bursts are transmitted at different power levels.

The APC includes a simple processor that generates 10-bit words at a rate of 2167 kHz. This processor computes the shape of the ramp-up and ramp-down transitions of the envelope signal from the value of the power level step and from the 16 coefficients of the desired shaping filter, which are stored in a random access memory (APCRAM) with an interpolation factor of 4. The power step is obtained by subtracting the content of the y-level registers which contain the previous power level from the x-level register the new power level. The automatic power control RAM register (see Section 5.3.6.4) includes 16 10-bit words. The 5 LSBs of each word represent the coefficients of the ramp-up shaping filter, while the 5 MSBs represent the coefficients of the ramp-down shaping filter. Ramp-up or ramp-down coefficient selection depends on the sign of the power step to be done—ramp-up for positive step and ramp-down for negative step.

Bit 6 (SEL256128) of the offset DAC input register (see Section 5.3.6.5) allows selection of two slopes for ramp-up and ramp-down: a normal slope when SEL256128 is 0 and a multiplied-by-two slope when at 1.

The sum of the coefficients is normalized and must be equal to 256 for both ramp-up and ramp-down coefficients in the case of normal slope and equal to 128 in the case of X2 slope. The APCRAM register is loaded once with ramp-up and ramp-down shaping filter coefficients adapted to the power amplifier used if the RF section and only the power register need to be updated from burst to burst depending on the desired power of the radio burst. The sequence of digital input words of the DAC10 is given by the following expressions:

When SEL256128 = 0:

$$\text{level} = \text{level}_{\text{init}} + \Sigma_{I=0..15}\left(\text{step}_{\text{lev}}/256\right) * \left(\text{up[i]} * \left(1 - \text{sign}_{\text{step}}\right) + \text{dw[i]} * \text{sign}_{\text{step}}\right) \quad (1)$$

When SEL256128 = 1:

$$\text{level} = \text{level}_{\text{init}} + \Sigma_{I=0..15}\left(2 * \text{step}_{\text{lev}}/256\right) * \left(\text{up[i]} * \left(1 - \text{sign}_{\text{step}}\right) + \text{dw[i]} * \text{sign}_{\text{step}}\right) \quad (2)$$

Where:

$\text{level}_{\text{init}}$ is the current power level.

$step_{lev}$ is the power level step to be done.

up[i] are the coefficients of the ramp-up shaping filter.

dw[i] are the coefficients of the ramp-down shaping filter.

$sign_{step}$ is the sign of $step_{lev}$ (0 for plus, 1 for minus).

The shaping filter generates 16 steps for ramp-up and 16 steps for ramp-down. In order to minimize image frequencies due to this sampling, a 4-time linear interpolation generates a 64-step signal at the input of the DAC.

Before being fed to the 10-bit DAC (DAC10) the content of the offset register is added to the 10-bit words computed by the APC processor. The sum of the level register and the offset register must not be more than 1023. This offset generates a voltage at APC output at power on to set the RF power amplifier to its conduction threshold.

The output of the 10-bit DAC is finally sent to the APC output through the output amplifier stage, which provides some low-pass continuous time filtering to smooth the APC signal.

Timing of the APC is generated by a control logic block for the signals coming from the TPS (BULON) and the BUL digital BULD (BULDRAMP).

Two delay registers (APC ramp delay 1 (see Section 5.3.6.1) and APC ramp delay 2 (see Section 5.3.6.2)) contain two 10-bit words to control the effective start of the ramp-up or ramp-down relative to the BULDRAMP signal. APC ramp delay 1 register contains the 5 LSBs of the two 10-bit words while APC ramp delay 2 register contains the 5 MSBs of the two 10-bit words. This delay can be adjusted independently for ramp-up and ramp-down from 0 to 1023 by quarter-bit units.

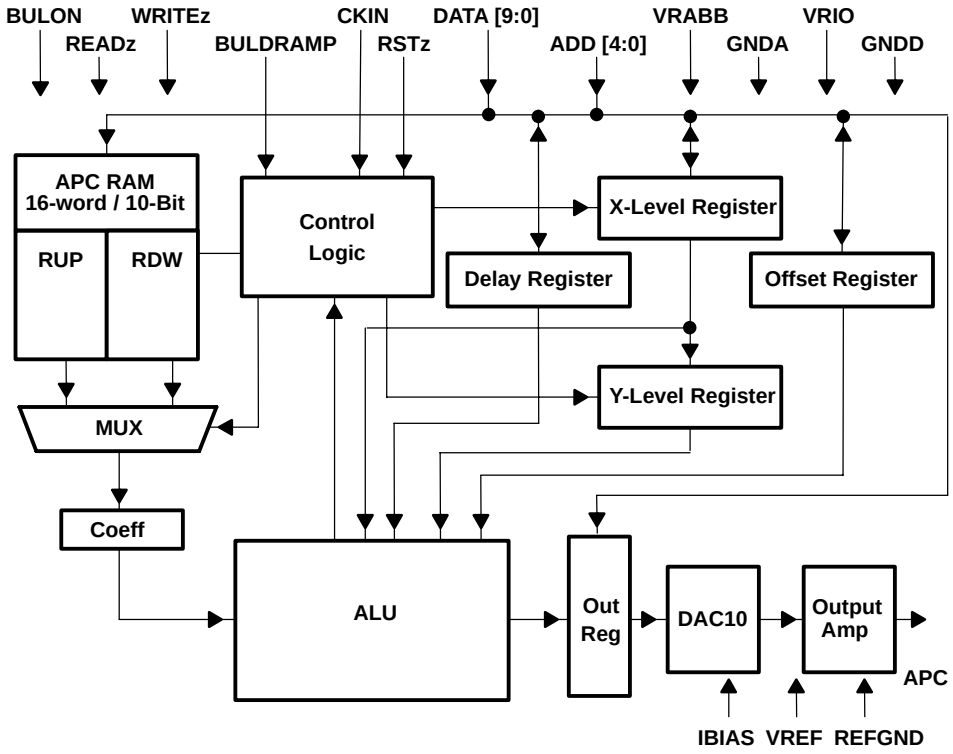


Figure 4−9. APC Block Diagram

4.13 Auxiliary DAC

Auxiliary DAC10 is a general-purpose 10-bit DAC. It includes a 10-bit register which can be accessed in read or write mode via the BSP or the USP under the arbitration of the IBIC, a 10-bit DAC, and an output amplifier.

4.14 Battery Charger Interface

The charging device is a low-output impedance dc voltage source of 7 V absolute maximum. An external PMOS power transistor in series with a power Schottky diode connected between the VCHG and VCCS terminals of the TWL3025 device controls the current flow from the charging device to the main battery. The role of the Schottky diode is to prevent reverse leakage current from the main battery in case the charging device is connected to the mobile phone without delivering any voltage at its output (charging device not plugged into the ac wall outlet, for example).

The main function of the battery charger interface is the charging control of both 1-cell Li-Ion battery or 3-series Ni-MH/Ni-Cd cell battery with the support of the microcontroller. In case of a rechargeable backup battery, it also delivers a trickle charge current to the backup battery from the main battery.

The charging scheme for the Li-Ion battery is constant current first (typical current is 1xC) followed by constant voltage charging once a certain voltage threshold is reached (4.2 V typical). Charging is stopped when the charging current at constant voltage has decreased down to C/20 (typical). Because the BCI works in the linear mode, the power dissipation around the external components must be taken into account.

For the Ni-MH/Ni-Cd, the battery charging scheme is constant current only. Charging is stopped when ΔV across battery terminals versus time inverts from positive to slightly negative (typically, a few mV per cell) or by any other criteria involving battery voltage or battery temperature. Ni-MH/Ni-Cd 3-cell battery voltage can reach 5.5 V at the end of a charge cycle.

In addition to the above charging schemes, another scheme is systematically applied when a battery charger is connected to a switched-off mobile phone: a charging current (precharge current) is applied to the battery when the battery voltage is lower than 3.6 V. If the battery voltage is lower than 3.2 V (battery partially discharged or fully discharged), the mobile phone is not started until the battery gets sufficiently recharged to greater than 3.2 V. When this happens, the microcontroller is started to control the fast charge cycle of the main battery, and the C/20 current is switched off.

4.14.1 Battery Monitoring

Battery monitoring is performed by the MADC block used to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage, and the backup battery voltage. The signals are converted into digital 10-bit words, stored in auxiliary ADC output registers (respectively, battery voltage conversion (see Section 5.3.3.2), analog 2 voltage conversion (see Section 5.3.3.7), analog 1 voltage conversion (see Section 5.3.3.6), battery current charger conversion (see Section 5.3.3.4), battery voltage charger conversion (see Section 5.3.3.3), and backup battery voltage conversion (see Section 5.3.3.5)) and transmitted to the microcontroller via the microcontroller interface.

Battery charging current is sensed by a 200-mΩ external sense resistor connected across the VCCS and VBATS terminals; the small differential voltage across the sense resistor is amplified by the amplifier A1. A1 and this resistor form a current-to-voltage (I-to-V) converter. This I-to-V converter has a conversion slope of 2 mA/mV typically. Also, a built-in positive offset (200 mV typical) is introduced in the I-to-V conversion so that for a 0-mA current, the output voltage after conversion is 200 mV typical. Internal switches are provided to disconnect the I-to-V converters input from VCCS and VBATS, and apply a true zero across the I-to-V converter inputs. The switches are positioned on or off by the microcontroller allowing a zero calibration subroutine of the I-to-V converters be performed under the supervision of the microcontroller; this routine is a part of the charging current measurement routine.

Voltages present at the VCHG and VBAT terminals are also suitably scaled by resistive dividers (respectively 1:5 and 1:4) to fit into the input dynamic range of the MADC. The resistive divider connected to VBAT is controlled by bit 0 (MESBAT) of the battery control 1 register (see Section 5.3.10.2).

Voltages at the ADIN2 and ADIN1 terminals are generated by internal current sources which develop voltages across the resistive temperature sensor (battery temperature measurement) and across the battery coding resistor (battery type identification). The current source on ADIN2 is programmable (3 bits) in the 10-µA to 80-µA range.

The current source on ADIN1 is set by default at 10 µA (typical).

4.14.2 Basic Operation at Plug-In of a Charging Device

What happens at charging device plug IN depends on the mobile phone state:

If the mobile phone is in switched-on state (ON_nOFF terminal = 1), the charging device plug IN generates an INT2 interrupt: CHARGER_IT and sets bit 3 (CHRGER) of the interrupt status register to 1 (see Section 5.3.11.2) to warn the microcontroller of its presence.

If the mobile phone is in switched-off state (ON_nOFF = 0) when the charging device is plugged IN, a precharge of the main battery is started if the main battery voltage is lower than 3.6 V. The transition of bit 3 (CHGSTS) of the VRPC status register (see Section 5.3.1.5) from 0 to 1 puts the central band-gap reference and the main battery comparator into power-up from the main battery.

When the main battery >3.2-V signal from the main battery comparator goes from 0 to 1, the VRPC pursues the switch-on procedure of the mobile phone (all regulators are ramped up, bit 3 (CHGSTS) of the VRPC status register is set to 1 (ON_nOFF = 1), and the microcontroller is started). Once wakened, the microcontroller recognizes that the charger was plugged in (and is still plugged in), from the CHGSTS bit being 1, and takes control of the main battery charging process.

At charger plug out, the CHGSTS bit is driven from 1 to 0 and an interrupt CHARGER_IT of the INT2 type is generated, making the microcontroller aware of the charging device unplug.

4.14.3 Constant Current/Constant Voltage Charging

The magnitude of the charging current is set by 10 bits of the main battery charging register (see Section 5.3.10.1), which is loaded by the microcontroller via the microcontroller serial interface and converted by the 10-bit DAC. The DAC output sets the reference input of the charging current control loop.

Current in constant current mode cannot be set to 0 exactly. A typical value for the maximum charging current in constant current mode is 0.98 A.

Bits 4 (CHDISPA) and 2 (CHBPASSPA) of the battery control 2 register (see Section 5.3.10.3) allow the microcontroller to temporarily disable or set at full charge the charger. Constant voltage charging (Li-Ion battery).

For Li-Ion rechargeable batteries, when the battery voltage measured at the VBAT terminal by the ADC MADC reaches the maximum charged voltage, the microcontroller sets the charging control loop into constant voltage mode by changing bit 1 (CHIV) of the battery control 2 register from 1 to 0.

The microcontroller terminates the charge by forcing bit 0 (CHEN) of the battery control 2 register to 0.

Bit 0 (MESBAT) in the battery control 1 register (see Section 5.3.10.2) must be enabled in order to close the constant current loop.

4.14.4 Main Battery Temperature and Main Battery Type Measurements

In order to measure the temperature of the battery, the battery charger interface includes dc current sources that deliver a bias current to the thermal sensing device (thermistor) and to the battery type resistor; the corresponding voltages are converted by the MADC.

Bit 6 (THEN) bit of the battery control 1 register (see Section 5.3.10.2) enables the thermistor current source. Bits 5−3 (THSENS(0−2)) of the battery control 1 register set the current magnitude between 10 and 80 μA. The battery type current source has a fixed value of 10 μA and is enabled by bit 7 (TYPEN) of the battery control 1 register.

4.14.5 Backup Battery Charge

The backup battery, in case it is rechargeable, can be recharged from the main battery. A voltage regulator powered by the main battery allows recharging of the backup battery to a selectable value (bits 8−7 (BBSEL[1:0]) in the battery charging configuration register) (see Section 5.3.10.4).

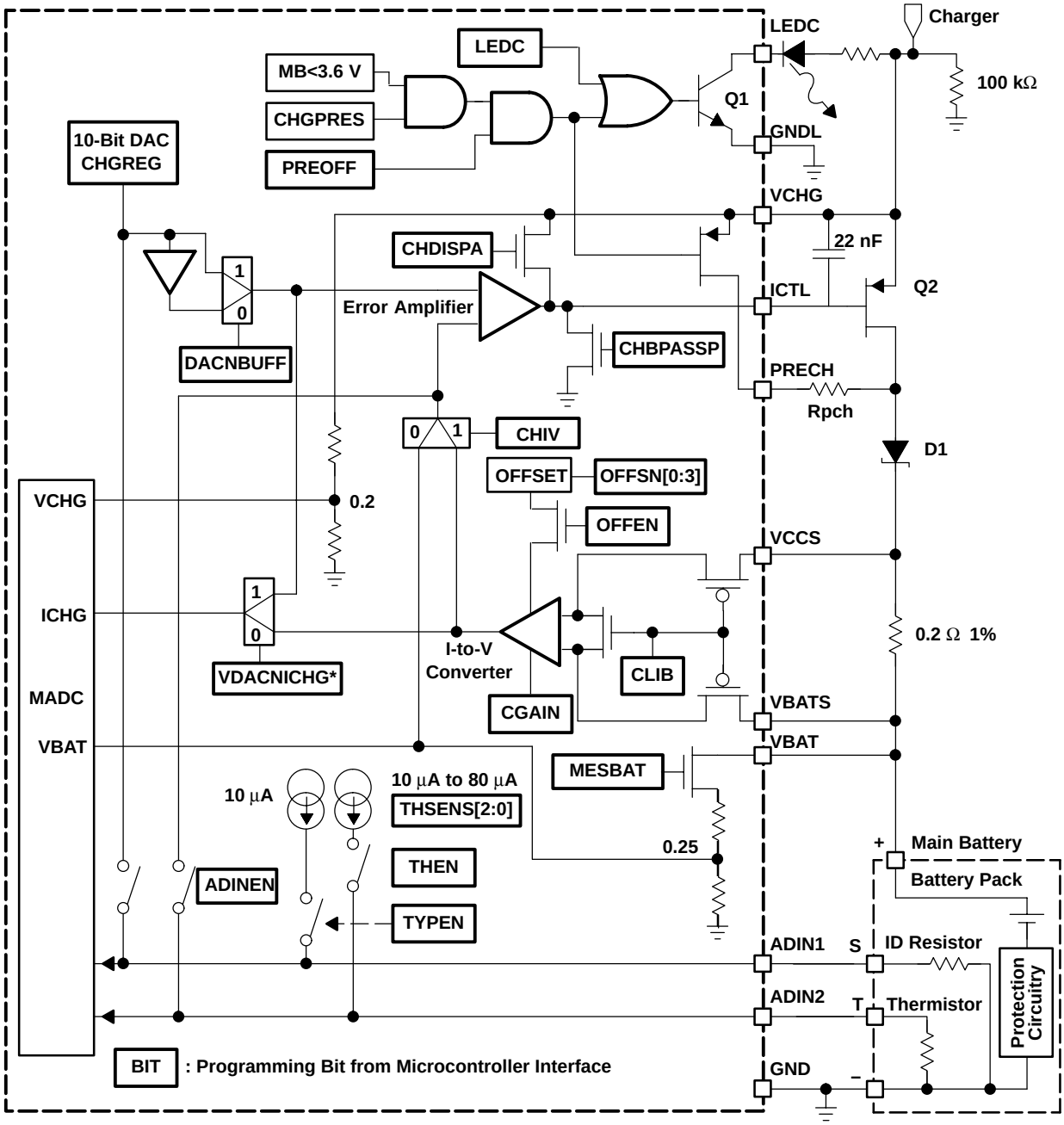


Figure 4−10. Battery Charger Block Diagram

4.15 Test Access Port

The TAP module provides a JTAG interface according to IEEE Std 1149.1. This interface uses the four dedicated I/O signals: TMS, TCK, TDI, and TDO.

The inputs TMS and TDI contain a pullup device which makes their state high when they are not driven; the input TCK contains a pulldown device which makes its state low when it is not driven; and the output TDO is a 3-state output which is high impedance except when data are shifted between TDI and TDO.

TCK is the test clock signal.

TMS is the test mode select signal.

TDI is the scan path input.

TDO is the scan path output.

The JTAG operations are controlled by a state machine, which is reset by the internal global reset.

A test mode is selected by writing a 6-bit word (instruction) into the instruction register (IR). This register is made of two stages: a shift register and a buffer register. The shift register is connected between TDI and TDO and allows a serial shift in of the instruction.

4.15.1 Scan Registers

The TAP includes three scan registers.

The boundary scan register is inserted between the physical boundary (terminal) and the system boundary (internal signal). It is mainly intended for test at board level to capture input terminal state, force output terminal state, force internal input signal or capture internal output signals, depending on the selected test mode (SAMPLE / PRELOAD, EXTEST, or INTEST). These features allow checking of the board connectivity between devices (EXTEST) or internally activating the device independently of the state of its input terminals (INTEST).

The identification register contains the ID code of the device.

The bypass register accesses test data registers in other components on a board-level test data path.

The scan registers are reset by the TWL3025 internal global reset RSTz during the test-logic-reset state from the state machine.

4.15.2 Public Instructions

As defined in IEEE Std1149.1 the public instructions are:

NAME	OPCODE	DESCRIPTION
BYPASS	11111 (63)	Connects the bypass register between TDI and TDO.
SAMPLE/ PRELOAD	00010 (02)	Connects the boundary scan register between TDI and TDO. This mode allows capturing a snapshot of device I/O states.
EXTEST	00000 (00)	Connects the boundary scan register between TDI and TDO. This mode allows capturing the state of the input terminals and forces the state of the output terminals. For example, it can be used for printed-circuit board connections test.
IDCODE	00001 (01)	Connects the identification register between TDI and TDO. This is the default configuration at reset. The identification register's content is: xxxx 0000 0000 0111 1111 0000 0010 1111 (xxxx represents the revision number)
INTEST	01001 (09)	Connects the boundary scan register between TDI and TDO. This mode allows forcing the internal system input signals via the parallel latches of the boundary register and to capture internal system outputs. (This mode can be used for device internal test independently of the state of its input terminals.) The internal master clock is derived from TCK and is active in the run-test-idle state of the state machine to allow single step operation of the device.

4.15.3 Private Instructions

A private instructions set exists for the specific test features.

In addition to the public instruction set, the TWL3025 device contains a set of private instructions, in order to put the device in the various test configurations.

The private instructions set connects specific internal signals to the four dedicated terminals: TEST1, TEST2, TEST3, and TEST4. These terminals are I/Os, set to inputs by default, and have pullup devices to ensure a driven state to the internal bus in this case.

NAME	OPCODE	DESCRIPTION			
BSPLOOP	000111 (07)	The data written to any register is automatically sent back (read) by the bus controller.			
VSPLOOP	001010 (10)	Connects the output of the voice serial interface to its input. This is done in the filter.			
AFCTEST	010000 (16)	AFCA test: connects the internal data bus (bit 7 to bit 0) directly to the input of the AFCA.			
MADCTEST	010010 (18)	Connects TEST pin on the MADC outputs			
		1−O	ADC_END_IT	3−I	Not used
		2−O	ADC_END_IT	4−I	Not used
TSPADC	010101 (21)	Connects baseband window control signals on the test pins.			
		1−I	Not used	3−O	BULENA
		2−I	Not used	4−O	STARTADC
TSPUP	010111 (23)	Connects baseband window control signals on the test pins.			
		1−I	Not used	3−O	BULON
		2−I	Not used	4−O	BULENA
TSPDN	011000 (24)	Connects baseband window control signals on the test pins.			
		1−I	Not used	3−O	BDLON
		2−I	Not used	4−O	BDLENA
TSPENA	011010 (26)	Connects baseband window control signals on the test pins.			
		1−I	Not used	3−O	BULENA
		2−I	Not used	4−O	BDLENA
TSPTEST1	011101 (29)	Connects baseband window control signals on the test pins.			
		1−O	BULON	3−O	BDLON
		2−O	BULENA	4−O	BDLENA
TSPTEST2	011110 (30)	Connects baseband window control signals on the test pins and the ADC conversion start bit on the test pins.			
		1−O	BULCAL	3−O	STARTADC
		2−O	BDLCAL	4−I	Not used
APCRAMP	011111 (31)	Connects ramp window control signals on the test pins.			
		1−I	External RAMP pulse	3−O	CKAPC
		2−I	Not used	4−O	Internal RAMP pulse

4.15.4 Boundary Scan

The boundary scan on analog terminals are only available as input boundary scan cell for capture mode only.

TERMINAL	TYPE	NB SCAN CELL	ORDER	BOUNDARY SCAN CELL
TDI	Digital	0	0	–
BDLQM	Analog	1	1	Analog input
BDLQP	Analog	1	2	Analog input
TEST4	Digital	3	3	Output disable
			4	Digital output
			5	Digital input
BDLIP	Analog	1	6	Analog input
BDLIM	Analog	1	7	Analog input
HSO	Analog	1	8	Analog input
EARN	Analog	1	9	Analog input
EARP	Analog	1	10	Analog input
AUXON	Analog	1	11	Analog input
AUXOP	Analog	1	12	Analog input
MICBIAS	Analog	1	13	Analog input
HSMICBIAS	Analog	1	14	Analog input
MICIN	Analog	1	15	Analog input
MICIP	Analog	1	16	Analog input
HSMICIP	Analog	1	17	Analog input
AUXI	Analog	1	18	Analog input
INT1TEST1	Digital	1	19	Digital output
TEST3	Digital	3	20	Output disable
			21	Digital output
			22	Digital input
UEN	Digital	1	23	Digital input
VDR	Digital	1	24	Digital input
VFS	Digital	1	25	Digital output
VDX	Digital	1	26	Digital output
UDX	Digital	2	27	Output disable
			28	Digital output
UDR	Digital	1	29	Digital input
DAC	Analog	1	30	Analog input
APC	Analog	1	31	Analog input
AFC	Analog	1	32	Analog input
VCK	Digital	1	33	Digital input
BFSR	Digital	1	34	Digital input
BDR	Digital	1	35	Digital input
BFSX	Digital	1	36	Digital output
BDX	Digital	1	37	Digital output
TEN	Digital	1	38	Digital input
TDR	Digital	1	39	Digital input
DBBSRST	Digital	1	40	Digital input
DBBSCK	Digital	1	41	Digital input

TERMINAL	TYPE	NB SCAN CELL	ORDER	BOUNDARY SCAN CELL
CK13M	Digital	1	42	Digital input
INT2TEST2	Digital	1	43	Digital output
ADIN4	Analog	1	44	Analog input
ADIN1	Analog	1	45	Analog input
ADIN2	Analog	1	46	Analog input
ADIN3	Analog	1	47	Analog input
LEDA	Analog	1	48	Analog input
LEDB	Analog	1	49	Analog input
BULQM	Analog	1	50	Analog input
BULQP	Analog	1	51	Analog input
BULIP	Analog	1	52	Analog input
BULIM	Analog	1	53	Analog input
TDO	Digital	0	53	–

5 Principles of Operation

5.1 Data and Address Format

Writing or reading registers via a serial interface is performed by transferring 16-bit words through the serial interface. Each word is split into three fields as follows:

- Data
- Address
- Read/Write

5.2 Internal Register Operations

DATA										ADDRESS					R/W
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A4	A3	A2	A1	A0	1/0

Bits (15:6) 10 bits of data to be written or read

Bits (5:1) 5-bit address to be used in conjunction with the page register (see Section 5.3.11.3, *Page Select Register*)

Bit (0) Cleared to 0 for a write, set to 1 for a read

5.2.1 Writing to Internal Register (Baseband Serial or Microcontroller Serial Port)

Bits (15:6) This field contains the data to be written into the internal register

Bits (5:1) This field contains the address to the register to be accessed

Bit (0) Cleared to 0 indicates a write operation

5.2.2 Reading From Internal Register (Baseband Serial or Microcontroller Serial Port)

Bits (15:6) This field is a don’t care in a read request operation

Bits (5:1) This field contains the address of the register to be accessed

Bit (0) Set to 1 indicates a read operation

5.2.3 Baseband Burst Operations

During reception of a burst, transfer of radio data from the downlink baseband codec is accomplished by the TX part of the BSP serial interface in the following 16-bit word format.

DATA										ADDRESS					I/Q
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	1/0

As the I/Q samples are coded with 16-bit words, the data rate is 8.66 Mbps (or 270833 * 16 * 2). Since the digital clock CK13M is 13 MHz, the transfer is performed at 13 Mbps in burst mode. During burst reception, the DSP serial interface is idled about 33% of the time. Two adjacent transmissions are separated by a delay of about one 16-bit word transfer time.

Table 5−1. Register Cross Reference Listing

REGISTER	NAME	SECTION	REGISTER	NAME	SECTION
ADIN1REG	Analog 1 voltage conversion	5.3.3.6	CHGREG	Main battery charging	5.3.10.1
ADIN2REG	Analog 2 voltage conversion	5.3.3.7	ICHGREG	Battery current charger conversion	5.3.3.4
ADIN3REG	Analog 3 voltage conversion	5.3.3.8	ITMASK	Interrupt mask	5.3.11.1
ADIN4REG	Analog 4 voltage conversion	5.3.3.9	ITSTATREG	Interrupt status	5.3.11.2
AFCCTLADD	AFC working frequency	5.3.5.3	MADCCTRL	Monitoring ADC control	5.3.2.1
AFCOUT	AFC digital output	5.3.5.4	MADCSTAT	Monitoring ADC status	5.3.3.1
APCDEL1	APC ramp delay 1	5.3.6.1	PAGEREG	Page select	5.3.11.3
APCDEL2	APC ramp delay 2	5.3.6.2	PWDNRG	Power down	5.3.4.3
APCOFF	Offset DAC input	5.3.6.5	TAPCTRL	Test access port control	5.3.4.4
APCOUT	APC output	5.3.6.6	TAPREG	Test access port instruction	5.3.4.5
APCRAM	Automatic power control RAM	5.3.6.4	TOGBR1	Toggle bits register 1	5.3.4.1
AUXAFC1	Automatic frequency control register 1	5.3.5.1	TOGBR2	Toggle bits register 2	5.3.4.2
AUXAFC2	Automatic frequency control register 2	5.3.5.2	VBATREG	Battery voltage conversion	5.3.3.2
AUXAPC	Automatic power control	5.3.6.3	VBCTRL1	Voiceband control register 1	5.3.13.1
AUXDAC	Auxiliary DAC control	5.3.7	VBCTRL2	Voiceband control register 2	5.3.13.2
AUXLED	LED driver	5.3.9	VBDCTRL	Voiceband downlink control	5.3.13.5
BBCTRL	Baseband codec control	5.3.12.8	VBKPREG	Backup battery voltage conversion	5.3.3.5
BCICONF	Battery charging configuration	5.3.10.4	VBPOP	Voiceband pop reduction	5.3.13.3
BCICTL1	Battery control 1	5.3.10.2	VBUCTRL	Voiceband uplink	5.3.13.4
BCICTL2	Battery control 2	5.3.10.3	VCHGREG	Battery voltage charger conversion	5.3.3.3
BULDATA1	Baseband uplink data buffer 1	5.3.12.6	VRPCCFG	VPRC configuration	5.3.1.1
BULDATA2	Baseband uplink data buffer 2	5.3.12.7	VRPCDEV	VPRC device mode	5.3.1.2
BULGCAL	Baseband uplink absolute gain calibration	5.3.12.5	VRPCMSK	VPRC mask	5.3.1.3
BULIDAC	Baseband uplink I DAC	5.3.12.3	VRPCMSKABB	VPRC mask VRABB	5.3.1.4
BULIOFF	Baseband uplink I offset	5.3.12.1	VRPCSIM	SimCard control	5.3.8
BULQDAC	Baseband uplink Q DAC	5.3.12.4	VRPCSTS	VRPC status register	5.3.1.5
BULQOFF	Baseband uplink Q offset	5.3.12.2			

Table 5−2. Register Map

PG	ADD	REGISTER	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	−	Reserved									
0	1	PAGEREG	Reserved						BSPP1	BSPP0	UCP1	UCP0
0	2	APCDEL1	DELD(4:0)					DELU(4:0)				
0	3	BULDATA1, 2	bit 0	//	//	//	//	//	//	//	//	bit 159
0	4	TOGBR1	MADCS	MADCR	AFCS	AFCR	ADACS	ADACR	VDLS	VDLR	VULS	VULR
0	5	TOGBR2	Reserved			IAPCTR	IBUFPTR2	IBUFPTR1	ACTS	ACTR	KEEPS	KEEPR
0	6	VBDCTRL	Reserved			VOLCTL(2:0)			VDLPG(3:0)			
0	7	AUXAFC1	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	8	AUXAFC2	−							bit 12	bit 11	bit 10
0	9	AUXAPC	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	10	APCRAM	DWN-0 to DWN-15					UP-0 to UP-15				
0	11	APCOFF	Reserved			SEL256128	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	12	AUXDAC	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	13	MADCCTRL	Reserved		ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
0	14	−	Reserved									
0	15	VBATREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	16	VCHGREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	17	ICHGREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	18	VBKPREG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	19	ADIN1REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	20	ADIN2REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	21	ADIN3REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	22	ADIN4REG	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	23	−	Reserved									
0	24	MADCSTAT	Reserved									ADCBUSY
0	25	CHGREG	CHG(9:0)									
0	26	ITMASK	Reserved				ADCEND _IT_MSK	Reserved	CHRGER _IT_MSK	PUSHOFF_ IT_MSK	REMOTE _IT_MSK	Reserved
0	27	ITSTATREG	Reserved				ADCEND	Reserved	CHRGER	PUSHOFF	REMOTE	Reserved
0	28	BCICTL1	Reserved		TYPEN	THEN	THSENS(2:0)			Reserved	DACNBUF	MESBAT
0	29	BCICTL2	Reserved		PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHBPASSPA	CHIV	CHEN
0	30	VRPCDEV	Reserved								DEVSLP	DEVOFF
0	31	VRPCSTS	Reserved			CHGPRES	ONMRFLT	ONREFLT	CHGSTS	ITWSTS	ONRSTS	ONBSTS

Table 5−2. Register Map (continued)

PG	ADD	REGISTER	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	0	−	Reserved									
1	1	PAGEREG	Reserved						BSPP1	BSPP0	UCP1	UCP0
1	2	BULIOFF	Reserved	ULIOFF(8:0)								
1	3	BULQOFF	Reserved	ULQOFF(8:0)								
1	4	BULQDAC	ULQDAC(9:0)									
1	5	BULIDAC	ULIDAC(9:0)									
1	6	BBCTRL	EXTCAL	OUTLEV(2:0)			MSLOT	BBMOD	BALOOP	SELVMID(2:0)		
1	7	VBUCTRL	DXEN	VDLST3	VDLST2	VDLST1	VDLST0	VULPG4	VULPG3	VULPG2	VULPG1	VULPG0
1	8	VBCTRL1	VFBYP	VBDF AUXG	VSYNC	VCLK MODE	VALOOP	MICBIAS	VUL SWITCH	VBUZ	VDLEAR	VDLAUX
1	9	PWDNRG	Reserved			ACTIV MCLK	KEEPON	MADCON	AFCON	ADACON	VDLON	VULON
1	10	VBPOP	Reserved	AUXAUTO	AUXCHG	AUXDIS	EARAUTO	EARCHG	EARDIS	HSOAUTO	HSOCHG	HSODIS
1	11	VBCTRL2	Reserved							MICNAUX	VDLHSO	MICBIASEL
1	12	APCOUT	APC(9:0)									
1	13	BCICONF	Reserved	BBSEL1	BBSEL0	MESBB	BBCHGEN	OFFEN	OFFSN3	OFFSN2	OFFSN1	OFFSN0
1	14	BULGCAL	Reserved	QAG3	QAG2	QAG1	QAG0	Reserved	IAG3	IAG2	IAG1	IAG0
1	15	−	Reserved									
1	16	−	Reserved									
1	17	−	Reserved									
1	18	−	Reserved									
1	19	TAPCTRL	Reserved									WRTEN
1	20	TAPREG	VER3	VER2	VER1	VER0	IR5	IR4	IR3	IR2	IR1	IR0
1	21	AFCCTLADD	Reserved							AFCBYP	AFCCK1	AFCCK0
1	22	AFCOUT	Reserved		DOUT(7:0)							
1	23	VRPCSIM	Reserved						SIMLEN	SIMRSU	RSIMEN	SIMSEL
1	24	AUXLED	Reserved								LEDB	LEDA
1	25	−	Reserved									
1	26	APCDEL2	DELD(9:5)					DELU(9:5)				
1	27	ITSTATREG	Reserved				ADCEND	Reserved	CHRGER	PUSHOFF	REMOTE	Reserved
1	28	−	Reserved									
1	29	VRPCMSK ABB	Reserved								MSKOFF ABB	MSKSLP ABB
1	30	VRPCCFG	RSVD	RRTC1	RRTC0	RDBB1	RDBB0	SLPDLY4	SLPDLY3	SLPDLY2	SLPDLY1	SLPDLY0
1	31	VRPCMSK	MSKOFF SIM	MSKOFF DBB	MSKOFF RAM	MSKOFF MEM	MSKOFF IO	MSKSLP SIM	MSKSLP DBB	MSKSLP RAM	MSKSLP MEM	MSKSLP IO

5.3 Register Description

5.3.1 Voltage Reference and Power Control (VRPC) Registers

5.3.1.1 VPRC Configuration Register

Register: **VRPCCFG**
Page: 1
Address: 30 (11110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	RRTC1	RRTC0	RDBB1	RDBB0	SLPDLY(4:0)				
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	Keep Value	Keep Value	Keep Value	Keep Value	1	1	1	1	1
Value at POR	0	VLRTC	0	VLRTC	0	1	1	1	1	1

Table 5−3. VPRC Configuration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8−7	RRTC(1:0)	Configure VRRTC output voltage as follows: 01 = 1.3 V 00 = 1.5 V 10 = 1.8 V
6−5	RDBB(1:0)	Configure VRDBB output voltage as follows: 01 = 1.3 V 00 = 1.5 V 10 = 1.8 V
4−0	SLPDLY(4:0)	Delay before going into sleep mode is [SLPDLY(4..0)*16+12]*TCK32K.

5.3.1.2 VPRC Device Mode Register

Register: **VRPCDEV**
Page: 0
Address: 30 (11110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD								DEVSLP	DEVOFF
Access Type	R	R	R	R	R	R	R	R	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−4. VPRC Device Mode Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−2	RSVD	Reserved
1	DEVSLP	When this bit is set to 1, start the SLT to switch the voltage regulators into SLEEP mode.
0	DEVOFF	When this bit is set to 1, start the WDT to switch the voltage regulators into OFF mode.

5.3.1.3 VPRC Mask Register

Register: **VRPCMSK**
Page: 1
Address: 31 (11111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	MSKOFF SIM	MSKOFF DBB	MSKOFF RAM	MSKOFF MEM	MSKOFF IO	MSKSLP SIM	MSKSLP DBB	MSKSLP RAM	MSKSLP MEM	MSKSLP IO
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−5. VPRC Mask Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	MSKOFFSIM	When this bit is set to 1 and the ABB device is in off mode, VRSIM is in sleep mode.
8	MSKOFFDBB	When this bit is set to 1 and the ABB device is in off mode, VRDBB is in sleep mode.
7	MSKOFFRAM	When this bit is set to 1 and the ABB device is in off mode, VRRAM is in sleep mode.
6	MSKOFFMEM	When this bit is set to 1 and the ABB device is in off mode, VRMEM is in sleep mode.
5	MSKOFFIO	When this bit is set to 1 and the ABB device is in off mode, VRIO is in sleep mode.
4	MSKSLPSIM	When this bit is cleared to 0 and the ABB device is in sleep mode, VRSIM is in sleep mode.
3	MSKSLPDBB	When this bit is cleared to 0 and the ABB device is in sleep mode, VRDBB is in sleep mode.
2	MSKSLPRAM	When this bit is cleared to 0 and the ABB device is in sleep mode, VRRAM is in sleep mode.
1	MSKSLPMEM	When this bit is cleared to 0 and the ABB device is in sleep mode, VRMEM is in sleep mode.
0	MSKSLPIO	When this bit is cleared to 0 and the ABB device is in sleep mode, VRIO is in sleep mode.

5.3.1.4 VPRC Mask VRABB Register

Register: **VRPCMSKABB**
Page: 1
Address: 29 (11101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD								MSKOFF ABB	MSKSLP ABB
Access Type	R	R	R	R	R	R	R	R	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	1

Table 5−6. VPRC Mask VRABB Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−2	RSVD	Reserved
1	MSKOFFABB	When this bit is set to 1 and the ABB device is in off mode, VRABB is in sleep mode.
0	MSKSLPABB	When this bit is cleared to 0 and the ABB device is in sleep mode, VRABB is in sleep mode.

5.3.1.5 VRPC Status Register

Register: **VRPCSTS**
Page: 0
Address: 31 (11111b)
Read/Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			CHGPRES	ONMRFLT	ONREFLT	CHGSTS	ITWSTS	ONRSTS	ONBSTS
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Table 5−7. VRPC Status Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−7	RSVD	Reserved
6	CHGPRES	When this bit is set to 1, it indicates the presence of a battery charger.
5	ONMRFLT	This bit reflects the state of the RPWON terminal after debouncing.
4	ONREFLT	This bit reflects the state of the PWON terminal after debouncing.
3	CHGSTS	This bit is set to 1 when a charger IC plug initiates a switch-on condition or an exit from the sleep mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
2	ITWSTS	This bit is set to 1 when the ITWAKEUP terminal initiates a switch-on condition or an exit from the sleep mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
1	ONRSTS	This bit is set to 1 when a the RPWON terminal transition from 0 to 1 initiates a switch-on condition or an exit from the sleep mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.
0	ONBSTS	This bit is set to 1 when an on button push initiates a switch-on condition or an exit from the sleep mode. This bit is not cleared when the ABB device changes its mode from ACTIVE to SLEEP.

5.3.2 Monitoring ADC Registers

A buffer register is used for the monitoring ADC control register. A write in the register accesses the buffer register. Upon a request for conversion, the master register is updated with the contents of the buffer register. A read from the register accesses the master register. If the read occurs before a conversion request, the configuration of the last conversion is read. If the read occurs after a conversion request and before the interrupt signaling the end of conversion, the configuration of the current conversion is read. A write to these registers during a conversion sequence has no effect on the current conversion (see Table 5−8). The user need not be concerned with the distinction between the two registers, only the behavior of the register accessed by the address.

5.3.2.1 Monitoring ADC Control Registers

Register: **MADCCTRL**
Page: 0
Address: 13 (01101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
Access Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Register: **MADCCTRL Buffer**
Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
Access Type	−	−	W	W	W	W	W	W	W	W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Register: **MADCCTRL Master**
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		ADIN4CV	ADIN3CV	ADIN2CV	ADIN1CV	VBKPCV	ICHGCV	VCHGCV	VBATCV
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−8. Monitoring ADC Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−8	RSVD	Reserved
7	ADIN4CV	This bit selects a conversion of the ADIN4 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
6	ADIN3CV	This bit selects a conversion of the ADIN3 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
5	ADIN2CV	This bit selects a conversion of the ADIN2 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
4	ADIN1CV	This bit selects a conversion of the ADIN1 input. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
3	VBKPCV	This bit selects a conversion of the backup battery voltage. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
2	ICHGCV	This bit selects a conversion of the charger battery current. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
1	VCHGCV	This bit selects a conversion of the charger battery voltage. When it is set to 1, a conversion of this input is expected during the next conversion sequence.
0	VBATCV	This bit selects a conversion of the battery voltage. When it is set to 1, a conversion of this input is expected during the next conversion sequence.

5.3.3 Monitoring ADC Output Status Registers

5.3.3.1 Monitoring ADC Status Register

Register: **MADCSTAT**
Page: 0
Address: 24 (11000b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD									ADCBUSY
Access Type	–	–	–	–	–	–	–	–	–	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−9. Monitoring ADC Status Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−1	RSVD	Reserved
0	ADCBUSY	If this bit is set to 1, a conversion is currently on-going.

5.3.3.2 Battery Voltage Conversion Register

Register: **VBATREG**
Page: 0
Address: 15 (01111b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−10. Battery Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the voltage of the battery. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.3 Battery Voltage Charger Conversion Register

Register: **VCHGREG**
Page: 0
Address: 16 (10000b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−11. Battery Voltage Charger Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the voltage of the battery charger. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.4 Battery Current Charger Conversion Register

Register: **ICHGREG**
Page: 0
Address: 17 (10001b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−12. Backup Current Charger Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the current of the battery charger. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.5 Backup Battery Voltage Conversion Register

Register: **VBKPREG**
Page: 0
Address: 18 (10010b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−13. Backup Battery Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the voltage of the backup battery. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.6 Analog 1 Voltage Conversion Register

Register: **ADIN1REG**
Page: 0
Address: 19 (10011b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−14. Analog 1 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the ADIN1 input. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.7 Analog 2 Voltage Conversion Register

Register: **ADIN2REG**
Page: 0
Address: 20 (10100b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−15. Analog 2 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the ADIN2 input. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.8 Analog 3 Voltage Conversion Register

Register: **ADIN3REG**
Page: 0
Address: 21 (10101b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−16. Analog 3 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the ADIN3 terminal. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.3.9 Analog 4 Voltage Conversion Register

Register: **ADIN4REG**
Page: 0
Address: 22 (10110b)
Read: 1

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−17. Analog 4 Voltage Conversion Register Description

DATA BIT	DESCRIPTION
9−0	Output of the 10-bit monitoring ADC for the ADIN4 terminal. This register is read-only.†

† A read is valid only when bit 0 (ADCBUSY) of the monitoring ADC output status register (see Section 5.3.3.1) is 0 and the MADC module is powered on.

5.3.4 Clock Generator (CKG) Registers

5.3.4.1 Toggle Bits Register 1

The bits in this register are not memory cells. They only set or reset internal latches. Writing 0 to any of these bits has no action. But writing to the reset toggle and the set toggle at the same time is interpreted as a reset toggle.

Register: **TOGBR1**
Page: 0
Address: 4 (00100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	MADCS	MADCR	AFCS	AFCR	ADACS	ADACR	VDLS	VDLR	VULS	VULR
Access Type	W	W	W	W	W	W	W	W	W	W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−18. Toggle Bits Register 1 Description

DATA BIT	FIELD NAME	DESCRIPTION
9	MADCS	Writing a 1 to this bit sets bit 4 (MADCON) of the power-down register to 1 (see Section 5.3.4.3).
8	MADCR	Writing a 1 to this bit clears bit 4 (MADCON) of the power-down register to 0 (see Section 5.3.4.3).
7	AFCS	Writing a 1 to this bit sets bit 3 (AFCON) of the power-down register to 1 (see Section 5.3.4.3).
6	AFCR	Writing a 1 to this bit clears bit 3 (AFCON) of the power-down register to 0 (see Section 5.3.4.3).
5	ADACS	Writing a 1 to this bit sets bit 2 (ADACON) of the power-down register to 1 (see Section 5.3.4.3).
4	ADACR	Writing a 1 to this bit clears bit 2 (ADACON) of the power-down register to 0 (see Section 5.3.4.3).
3	VDLS	Writing a 1 to this bit sets bit 1 (VDLON) of the power-down register to 1 (see Section 5.3.4.3).
2	VDLR	Writing a 1 to this bit clears bit 1 (VDLON) of the power-down register to 0 (see Section 5.3.4.3).
1	VULS	Writing a 1 to this bit sets bit 0 (VULON) of the power-down register to 1 (see Section 5.3.4.3).
0	VULR	Writing a 1 to this bit clears bit 0 (VULON) of the power-down register to 0 (see Section 5.3.4.3).

† The VUL and VDL paths share the same digital filter. In order to ensure a perfect initialization of this digital filter, bits 0 (VULON) and 1 (VDLON) of the power-down register have to be set to on at the same time for at least 125 μs after turning VRIO from off to on.

5.3.4.2 Toggle Bits Register 2

The bits in this register are not memory cells. They only set or reset internal latches. Writing 0 to any of these bits has no action. But writing to the reset toggle and the set toggle at the same time is interpreted as a reset toggle.

Register: **TOGBR2**
Page: 0
Address: 5 (00101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			IAPCTR	IBUFPTR2	IBUFPTR1	ACTS	ACTR	KEEPS	KEEPR
Access Type	W	W	W	W	W	W	W	W	W	W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−19. Toggle Bits Register 2 Description

DATA BIT	FIELD NAME	DESCRIPTION
9−7	RSVD	Reserved
6	IAPCTR	Writing a 1 to this bit initializes the pointer of the APC RAM.
5	IBUFPTR2	Writing a 1 to this bit initializes the pointer of burst buffer 2.
4	IBUFPTR1	Writing a 1 to this bit initializes the pointer of burst buffer 1.
3	ACTS	Writing a 1 to this bit sets bit 6 (ACTIVMCLK) of the power-down register to 1 (see Section 5.3.4.3).
2	ACTR	Writing a 1 to this bit clears bit 6 (ACTIVMCLK) of the power-down register to 0 (see Section 5.3.4.3).
1	KEEPS	Writing a 1 to this bit sets bit 5 (KEEPON) of the power-down register to 1 (see Section 5.3.4.3).
0	KEEPR	Writing a 1 to this bit clears bit 5 (KEEPON) of the power-down register to 0 (see Section 5.3.4.3).

† Setting bit 4 (IBUFPTR1) or 5 (IBUFPTR2) to 1 is not permitted during the baseband uplink burst (the BULENA signal is set to 1).

5.3.4.3 Power-Down Register

Register: **PWDNRG**
Page: 1
Address: 9 (01001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			ACTIVMCLK	KEEPON	MADCON	AFCON	ADACON	VDLON	VULON
Access Type	R	R	R	R	R	R	R	R	R	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−20. Power-Down Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−7	RSVD	Reserved
6	ACTIVMCLK	When this bit is cleared to 0, the MADC, IBIC, and SIMS are in low power mode, using OSCAS clock. This bit is set to 1 by bit 3 (ACTS) and reset by bit 2 (ACTR) of toggle bits register 2 (see Section 5.3.4.2).
5	KEEPON	When this bit is set to 1, the ADC of MADC block is always on even after a conversion. When this bit is cleared to 0, the ADC of MADC block sets itself automaticaly off after a conversion. This bit is set to 1 by bit 1 (KEEPS) and reset by bit 0 (KEEPR) of toggle bits register 2 (see Section 5.3.4.2).
4	MADCON	When this bit is cleared to 0, the MADC is in power-down mode. This bit is set to 1 by bit 9 (MADCS) and reset by bit 8 (MADCR) of toggle bits register 1 (see Section 5.3.4.1).
3	AFCON	When this bit is cleared to 0, the AFC is in power-down mode. This bit is set to 1 by bit 7 (AFCS) and reset by bit 6 (AFCR) of toggle bits register 1 (see Section 5.3.4.1).
2	ADACON	When this bit is cleared to 0, the auxiliary DAC is in power-down mode. This bit is set to 1 by bit 5 (ADACS) and reset by bit 4 (ADACR) of toggle bits register 1 (see Section 5.3.4.1).
1	VDLON	When this bit is cleared to 0, the voiceband downlink path is in power-down mode. This bit is set to 1 by bit 3 (VDLS) and reset by bit 2 (VDLR) of toggle bits register 1 (see Section 5.3.4.1).
0	VULON	When this bit is cleared to 0, the voiceband uplink path is in power-down mode. This bit is set to 1 by bit 1 (VULS) and reset by bit 0 (VULR) of toggle bits register 1 (see Section 5.3.4.1).

5.3.4.4 Test Access Port Control Register

Register: **TAPCTRL**
Page: 1
Address: 19 (10011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD									WRTEN
Access Type	−	−	−	−	−	−	−	−	−	W
Value at Reset	−	−	−	−	−	−	−	−	−	0

Table 5−21. Test Access Port Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−1	RSVD	Reserved
0	WRTEN	If this bit is set to 1, the test mode is selected by writing in the test access port instruction register (see Section 5.3.4.5). If this bit is cleared to 0, the test mode is selected by loading the shift register (use of TMS, TDI).

5.3.4.5 Test Access Port Instruction Register

Register: **TAPREG**
Page: 1
Address: 20 (10100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	VER3	VER2	VER1	VER0	IR5	IR4	IR3	IR2	IR1	IR0
Access Type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0/1	0/1	0/1	0/1	0	0	0	0	0	0

Table 5−22. Test Access Port Instruction Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−6	VER(3:0)	Version number (version part of the ABB device IDCODE)
5−0	IR(5:0)	JTAG instruction register data (see Section 4.15.2)

5.3.5 Automatic Frequency Control (AFC) Registers

5.3.5.1 Automatic Frequency Control Register 1

Register: **AUXAFC1**
Page: 0
Address: 7 (00111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−23. Automatic Frequency Control Register 1 Description

DATA BIT	DESCRIPTION
9−0	LSB input of the 13-bit AFC DAC in twos complement

5.3.5.2 Automatic Frequency Control Register 2

Register: **AUXAFC2**
Page: 0
Address: 8 (01000b)
Read/Write: 1/0

Data Bit	−	−	−	−	−	−	−	12	11	10
Access Type	−	−	−	−	−	−	−	R/W	R/W	R/W
Value at Reset	−	−	−	−	−	−	−	0	0	0

Table 5−24. Automatic Frequency Control Register 2 Description

DATA BIT	DESCRIPTION
12−10	MSB input of the 13-bit AFC DAC in twos complement. The AFC value is loaded after a successive write of AFC-MSB and AFC-LSB.

5.3.5.3 AFC Working Frequency Register

Register: **AFCCTLADD**
Page: 1
Address: 21 (10101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD							AFCBYP	AFCCK1	AFCCK0
Access Type	−	−	−	−	−	−	−	R/W	R/W	R/W
Value at Reset	−	−	−	−	−	−	−	0	0	0

Table 5−25. AFC Working Frequency Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−3	RSVD	Reserved
2	AFCBYP	Disables write access in AFC digital output register by Σ-Δ modulator. Enables write access in AFC digital output register by USP or BSP access.
1−0	AFCCK(1:0)	AFCCK1 / AFCCK0 / AFC Clock Frequency 0 / 0 / Reserved 0 / 1 / 2.16 MHz 1 / 0 / 1.08 MHz 1 / 1 / 541 kHz Note: The AFCCK(1:0) clock frequency mode must not equal 00.

5.3.5.4 AFC Digital Output Register

Register: **AFCOUT**
Page: 1
Address: 22 (10110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	DOUT0
Access Type	−	−	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	−	−	0	0	0	0	0	0	0	0

Table 5−26. AFC Digital Output Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−8	RSVD	Reserved
7−0	DOUT(7:0)	The serial-to-parallel output of the AFC modulator (for test purposes) Bit 2 (AFCBYP) in the AFC working frequency register (see Section 5.3.5.3) must be set to enable write access.

5.3.6 Automatic Power Control (APC) Registers

In all cases, the value of DELU(9:0) and DELD(9:0) must be set to avoid any ramp-up or ramp-down start delays after the falling edge of BULENA.

5.3.6.1 APC Ramp Delay 1 Register

Register: **APCDEL1**
Page: 0
Address: 2 (00010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	DELD4	DELD3	DELD2	DELD1	DELD0	DELU4	DELU3	DELU2	DELU1	DELU0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−27. APC Ramp Delay 1 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−5	DELD(4:0)	LSB part of ramp-down start delay relative to the falling edge of BENA. See Section 4.12 for a description of the adjustment delay.
4−0	DELU(4:0)	LSB part of ramp-up start delay relative to the rising edge of BENA. See Section 4.12 for a description of the adjustment delay.

5.3.6.2 APC Ramp Delay 2 Register

Register: **APCDEL2**
Page: 1
Address: 26 (11010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	DELD9	DELD8	DELD7	DELD6	DELD5	DELU9	DELU8	DELU7	DELU6	DELU5
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−28. APC Ramp Delay 2 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−5	DELD(9:5)	MSB ramp-down start delay relative to the falling edge of BENA. See Section 4.12 for a description of the adjustment delay.
4−0	DELU(9:5)	MSB ramp-up start delay relative to the rising edge of BENA. See Section 4.12 for a description of the adjustment delay.

5.3.6.3 Automatic Power Control Register

Register: **AUXAPC**
Page: 0
Address: 9 (01001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−29. Automatic Power Control Register Description

DATA BIT	DESCRIPTION
9−0	10-bit APC power level

5.3.6.4 Automatic Power Control RAM Register

The contents of the APC RAM register are the coefficients of the ramp-up and ramp-down shaping filters.

Register: **APCRAM**
Page: 0
Address: 10 (01010b)
Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	DWN−0 (5-bit)					UP−0 (5-bit)				
	DWN−1 (5-bit)					UP−1 (5-bit)				
	…					…				
	DWN−14 (5-bit)					UP−14 (5-bit)				
	DWN−15 (5-bit)					UP−15 (5-bit)				
Access Type	W	W	W	W	W	W	W	W	W	W
Value at Reset	0	0	0	0	0	0	0	0	0	0

5.3.6.5 Offset DAC Input Register

Register: **APCOFF**
Page: 0
Address: 11 (01011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			SEL256128	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Access Type	−	−	−	W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−30. Offset DAC Input Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−7	RSVD	Reserved
6	SEL256128	At 0, select normal slope for ramp-up and ramp-down. At 1, select 2X slope for ramp-up and ramp-down.
5−0	Bits (5:0)	Input of the 6-bit offset DAC

5.3.6.6 APC Output Register

Register: **APCOUT**
Page: 1
Address: 12 (01100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	APC9	APC	APC7	APC6	APC5	APC	APC	APC2	APC1	APC0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−31. APC Output Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−0	APC(9:0)	Value of data to APC DAC 10

5.3.7 Auxiliary DAC Control Register

Register: **AUXDAC**
Page: 0
Address: 12 (01100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−32. Auxiliary DAC Control Register Description

DATA BIT	DESCRIPTION
9−0	Input of the 10-bit ADAC

5.3.8 SimCard Control Register

Register: **VRPCSIM**
Page: 1
Address: 23 (10111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD						SIMLEN	SIMRSU	RSIMEN	SIMSEL
Access Type	R	R	R	R	R	R	R/W	R	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−33. SimCard Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−4	RSVD	Reserved
3	SIMLEN	When this bit is set to 1, the SimCard level shifter is enabled (SIMCK, SIMIO, and SIMRST are enabled).
2	SIMRSU	VRSIM voltage regulator output status: 0 = The voltage regulator is not in regulation mode. 1 = The regulation is on, the SIM card is correctly supplied.
1	RSIMEN	When this bit is set to 1, the VRSIM voltage regulator is enabled.
0	SIMSEL	Select the VRSIM output voltage: 1 = 2.9 V 0 = 1.8 V

5.3.9 LED Driver Register

Register: **AUXLED**
Page: 1
Address: 24 (11000b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD								LEDB	LEDA
Access Type	R	R	R	R	R	R	R	R	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−34. LED Driver Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−2	RSVD	Reserved
1	LEDB	When this bit is set to 1, the LED B driver is enabled. The LED B driver is connected to the LEDB1 and LEDB2 terminals. The LED B driver needs a 13-MHz clock.
0	LEDA	When this bit is set to 1, the LED A driver is enabled. The LED A driver needs a 32-kHz clock.

5.3.10 Battery Charger Interface (BCI) Registers

Controlling the operation of the BCI requires the exchange of two types of programming signals between the BCI itself and the rest of the system, that is, the power control state machine contained in the VRPCD block of the TWL3025 device, and the microcontroller contained in the DBB device.

1. Some programming signals are sent or received by the microcontroller exclusively, when it is fully awake; the path for these signals includes the microcontroller interface registers only.
2. Other programming signals are also sent or received by the power control state machine located in the VRPCD block, before the microcontroller gets awakened; the path for these signals includes a multiplexing operation between the microcontroller interface registers (VRIO supply domain) and the power control state machine. A signal driving the direction of the multiplex decides which device, the power control state machine or the microcontroller, sends or receives programming data to or from the BCI.

5.3.10.1 Main Battery Charging Register

Register: **CHGREG**
Page: 0
Address: 25 (11001b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	CHG9	CHG8	CHG7	CHG6	CHG5	CHG4	CHG3	CHG2	CHG1	CHG0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−35. Main Battery Charging Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−0	CHG(9:0)	10-bit DAC register for setting a voltage or a current for main battery charging

5.3.10.2 Battery Control 1 Register

Register: **BCICTL1**
Page: 0
Address: 28 (11100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		TYPEN	THEN	THSENS2	THSENS1	THSENS0	RSVD	DACNBUF	MESBAT
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−36. Battery Control 1 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−8	RSVD	Reserved (write only 0)
7	TYPEN	Enables the bias current for the main battery type reading
6	THEN	Enables the bias current for the main battery temperature sensing
5−3	THSENS(2:0)	Sets eight possible values for the thermal sensor bias current
3	RSVD	Reserved
1	DACNBUF	Bypasses the BCIDAC output amplifier
0	MESBAT	Connects the resistive divider to the main battery

5.3.10.3 Battery Control 2 Register

Register: **BCICTL2**
Page: 0
Address: 29 (11101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD		PREOFF	CGAIN4	LEDC	CHDISPA	CLIB	CHBPASSPA	CHIV	CHEN
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0
Value read if Charger is not present	1	1	1	1	1	1	1	1	1	1

Table 5−37. Battery Control 2 Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−8	RSVD	Reserved (write only 0)
7	PREOFF	Disables the main battery precharge
6	CGAIN4	Reduces the gain of the I-to-V converter from 10 to 4
5	LEDC	Enables the LED C driver to indicate a battery charge
4	CHDISPA	Controls the charging of the main battery during pulse radio
3	CLIB	Allows a zero calibration routine to the I-to-V converter
2	CHBPASSPA	Controls full charging of the main battery during pulse radio
1	CHIV	Selects constant current or constant voltage charging
0	CHEN	Enables the charger

5.3.10.4 Battery Charging Configuration Register

Register: **BCICONF**
Page: 1
Address: 13 (01101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	BBSEL1	BBSEL0	MESBB	BBCHGEN	OFFEN	OFFSN3	OFFSN2	OFFSN1	OFFSN0
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	Keep value	Keep value	0	Keep value	Keep value	Keep value	Keep value	Keep value	Keep value
Value at POR	0	0	0	0	0	0	0	0	0	0

Table 5−38. Battery Charging Configuration Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8−7	BBSEL(1:0)	Selects the end of backup battery charging voltage: 00 = VBBCHGEND + 0 mV 01 = VBBCHGEND + 100 mV 10 = VBBCHGEND + 200 mV 11 = VBBCHGEND + 200 mV
6	MESBB	Connects a resistive divider to the backup battery
5	BBCHGEN	Enables the charging of the backup battery

4	OFFEN	Enables the I-to-V offset compensation with bits 3−0 (OFFSN[3:0])
3−0	OFFSN(3:0)	Selects 16 possible values for the I-to-V conversion offset: 0000 = 0 mV N = N*12.5 mV 1111 = 187.5 mV

5.3.11 Interrupt and Bus Control Registers (IBIC)

5.3.11.1 Interrupt Mask Register

Register: **ITMASK**
Page: 0
Address: 26 (11010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD				ADCEND_IT_MSK	RSVD	CHRGER_IT_MSK	PUSHOFF_IT_MSK	REMOTE_IT_MSK	RSVD
Access Type	R	R	R	R	R/W	R	R/W	R/W	R/W	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−39. Interrupt Mask Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−6	RSVD	Reserved
5	ADCEND_IT_MSK	If this bit is set to 1, the ADC end-of-conversion interrupt is not generated.
4	RSVD	Reserved
3	CHRGER_IT_MSK	If this bit is set to 1, the charger plug in or out interrupt is not generated.
2	PUSHOFF_IT_MSK	If this bit is set to 1, the push button from on to off interrupt is not generated.
1	REMOTE_IT_MSK	If this bit is set to 1, the remote power from on to off interrupt is not generated.
0	RSVD	Reserved

5.3.11.2 Interrupt Status Register

Register: **ITSTATREG**
Pages: 0 and 1
Address: 27 (11011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD				ADCEND	RSVD	CHRGER	PUSHOFF	REMOTE	RSVD
Access Type	R	R	R	R	R/W	R	R/W	R/W	R/W	R
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−40. Interrupt Status Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−6	RSVD	Reserved
5	ADCEND	ADC end-of-conversion interrupt bit
4	RSVD	Reserved
3	CHRGER	Charger plug in or out interrupt bit
2	PUSHOFF	Push button (the PWON terminal) from on to off interrupt bit
1	REMOTE	Remote power (the RPWON terminal) from on to off interrupt bit
0	RSVD	Reserved

5.3.11.3 Page Select Register

This register is a read/write register. It can be accessed through both the USP and BSP serial interfaces. The USP access to this register does not affect the current page selected by the BSP. The BSP access to this register does not affect the current page selected by the USP. Therefore, the users' software must know the last page that was selected by the serial interface that is being used. Furthermore, if the last page selected by the BSP/USP differs from the last page selected by the USP/BSP, there is no need to rewrite to the page register as the device knows which serial port is accessing registers and uses the current page setting for that port.

Register: **PAGEREG**
Pages: 0 and 1
Address: 1 (00001b)
Write: 0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD						BSPP1	BSPP0	UCP1	UCP0
Access Type	−	−	−	−	−	−	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−41. Page Select Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−4	RSVD	Reserved
3	BSPP1	Writing a 1 sets page 1 for BSP access. Only accessible by the BSP.
2	BSPP0	Writing a 1 sets page 0 for BSP access. Only accessible by the BSP.
1	UCP1	Writing a 1 sets page 1 for USP access. Only accessible by the USP.
0	UCP0	Writing a 1 sets page 0 for USP access. Only accessible by the USP.

5.3.12 Baseband Codec (BBC) Registers

5.3.12.1 Baseband Uplink I Offset Register

Write access to this register is disabled during offset calibration (BULCAL high).

Register: **BULIOFF**
Page: 1
Address: 2 (00010b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ULIOFF(8:0)								
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	1	1	1	1	1	1	1	1

Table 5−42. Baseband Uplink I Offset Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8−0	ULIOFF(8:0)	I channel offset value

5.3.12.2 Baseband Uplink Q Offset Register

Write access to this register is disabled during offset calibration (BULCAL high).

Register: **BULQOFF**
Page: 1
Address: 3 (00011b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	ULQOFF(8:0)								
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	1	1	1	1	1	1	1	1

Table 5−43. Baseband Uplink Q Offset Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8−0	ULQOFF(8:0)	Q channel offset value

5.3.12.3 Baseband Uplink I DAC Register

Register: **BULIDAC**
Page: 1
Address: 5 (00101b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	ULIDAC(9:0)									
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	1	1	1	1	1	1	1	1	1

Table 5−44. Baseband Uplink I DAC Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−0	ULIDAC(9:0)	Data applied to I channel DAC. Write is disabled during modulation.

5.3.12.4 Baseband Uplink Q DAC Register

Register: **BULQDAC**
Page: 1
Address: 4 (00100b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	ULQDAC(9:0)									
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−45. Baseband Uplink Q DAC Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−0	ULQDAC(9:0)	Data applied to Q channel DAC. Write is disabled during modulation.

5.3.12.5 Baseband Uplink Absolute Gain Calibration Register

Register: **BULGCAL**
Page: 1
Address: 14 (01110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	QAG3	QAG2	QAG1	QAG0	RSVD	IAG3	IAG2	IAG1	IAG0
Access Type	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−46. Baseband Uplink Absolute Gain Calibration Register Description

DATA BIT	FIELD NAME	DESCRIPTION			
9	RSVD	Reserved			
8−5	QAG(3:0)	Absolute gain calibration for Q DAC			
		QAG(3:0)	Relative Gain	QAG(3:0)	Relative Gain
		0000	0 db	0000	0 db
		0001	0.27 db	1111	−0.27 db
		0010	0.53 db	1110	−0.56 db
		0011	0.78 db	1101	−0.85 db
		0100	1.02 db	1100	−1.16 db
		0101	1.26 db	1011	−1.48 db
		0110	1.49 db	1010	−1.80 db
4	RSVD	Reserved			
3−0	IAG(3:0)	Absolute gain calibration for I DAC			
		IAG(3:0)	Relative Gain	IAG(3:0)	Relative Gain
		0000	0 db	0000	0 db
		0001	0.27 db	1111	−0.27 db
		0010	0.53 db	1110	−0.56 db
		0011	0.78 db	1101	−0.85 db
		0100	1.02 db	1100	−1.16 db
		0101	1.26 db	1011	−1.48 db
		0110	1.49 db	1010	−1.80 db

5.3.12.6 Baseband Uplink Data Buffer 1 Register

Register: **BULDATA1**
Page: 0 (16 words)
Address: 3 (00011b)
Write: 0

Data Bit	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9
	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	bit 16	bit 17	bit 18	bit 19
	bit 20	bit 21	bit 22	bit 23	bit 24	bit 25	bit 26	bit 27	bit 28	bit 29
	bit 30	bit 31	bit 32	bit 33	bit 34	bit 35	bit 36	bit 37	bit 38	bit 39
	bit 40	bit 41	bit 42	bit 43	bit 44	bit 45	bit 46	bit 47	bit 48	bit 49
	bit 50	bit 51	bit 52	bit 53	bit 54	bit 55	bit 56	bit 57	bit 58	bit 59
	bit 60	bit 61	bit 62	bit 63	bit 64	bit 65	bit 66	bit 67	bit 68	bit 69
	bit 70	bit 71	bit 72	bit 73	bit 74	bit 75	bit 76	bit 77	bit 78	bit 79
	bit 80	bit 81	bit 82	bit 83	bit 84	bit 85	bit 86	bit 87	bit 88	bit 89
	bit 90	bit 91	bit 92	bit 93	bit 94	bit 95	bit 96	bit 97	bit 98	bit 99
	bit 100	bit 101	bit 102	bit 103	bit 104	bit 105	bit 106	bit 107	bit 108	bit 109
	bit 110	bit 111	bit 112	bit 113	bit 114	bit 115	bit 116	bit 117	bit 118	bit 119
	bit 120	bit 121	bit 122	bit 123	bit 124	bit 125	bit 126	bit 127	bit 128	bit 129
	bit 130	bit 131	bit 132	bit 133	bit 134	bit 135	bit 136	bit 137	bit 138	bit 139
	bit 140	bit 141	bit 142	bit 143	bit 144	bit 145	bit 146	bit 147	bit 148	bit 149
	bit 150	bit 151	bit 152	bit 153	bit 154	bit 155	bit 156	bit 157	bit 158	bit 159
Access Type	W	W	W	W	W	W	W	W	W	W

Table 5−47. Baseband Uplink Data Buffer 1 Register Description

DATA BIT	DESCRIPTION
0:3	4 guard bits
4:6	3 tail bits
7:64	58 data bits
65:90	26 training sequence bits
91:148	58 data bits
149:151	3 tail bits
152:159	8 guard bits

NOTE 1: Bit 0 is transmitted first. At reset and after each transmission the burst buffer is not reinitialized.

5.3.12.7 Baseband Uplink Data Buffer 2 Register

Register: **BULDATA2**
Page: 0 (16 words)
Address: 3 (00011b)
Write: 0

Data Bit	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9
	bit 10	bit 11	bit 12	bit 13	bit 14	bit 15	bit 16	bit 17	bit 18	bit 19
	bit 20	bit 21	bit 22	bit 23	bit 24	bit 25	bit 26	bit 27	bit 28	bit 29
	bit 30	bit 31	bit 32	bit 33	bit 34	bit 35	bit 36	bit 37	bit 38	bit 39
	bit 40	bit 41	bit 42	bit 43	bit 44	bit 45	bit 46	bit 47	bit 48	bit 49
	bit 50	bit 51	bit 52	bit 53	bit 54	bit 55	bit 56	bit 57	bit 58	bit 59
	bit 60	bit 61	bit 62	bit 63	bit 64	bit 65	bit 66	bit 67	bit 68	bit 69
	bit 70	bit 71	bit 72	bit 73	bit 74	bit 75	bit 76	bit 77	bit 78	bit 79
	bit 80	bit 81	bit 82	bit 83	bit 84	bit 85	bit 86	bit 87	bit 88	bit 89
	bit 90	bit 91	bit 92	bit 93	bit 94	bit 95	bit 96	bit 97	bit 98	bit 99
	bit 100	bit 101	bit 102	bit 103	bit 104	bit 105	bit 106	bit 107	bit 108	bit 109
	bit 110	bit 111	bit 112	bit 113	bit 114	bit 115	bit 116	bit 117	bit 118	bit 119
	bit 120	bit 121	bit 122	bit 123	bit 124	bit 125	bit 126	bit 127	bit 128	bit 129
	bit 130	bit 131	bit 132	bit 133	bit 134	bit 135	bit 136	bit 137	bit 138	bit 139
	bit 140	bit 141	bit 142	bit 143	bit 144	bit 145	bit 146	bit 147	bit 148	bit 149
	bit 150	bit 151	bit 152	bit 153	bit 154	bit 155	bit 156	bit 157	bit 158	bit 159
Access Type	W	W	W	W	W	W	W	W	W	W

Table 5−48. Baseband Uplink Data Buffer 2 Register Description

DATA BIT	DESCRIPTION
0:3	4 guard bits
4:6	3 tail bits
7:64	58 data bits
65:90	26 training sequence bits
91:148	58 data bits
149:151	3 tail bits
152:159	8 guard bits

NOTE 2: Bit 0 is transmitted first. At reset and after each transmission the burst buffer is not reinitialized.

5.3.12.8 Baseband Codec Control Register

Register: **BBCTRL**
Page: 1
Address: 6 (00110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	EXTCAL	OUTLEV2	OUTLEV1	OUTLEV0	MSLOT	BBMOD	BALOOP	SELVMID2	SELVMID1	SELVMID0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−49. Baseband Codec Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	EXTCAL	Downlink auto calibration mode: 0 = Auto calibration 1 = External calibration
8−6	OUTLEV(2:0)	Selects the value of the baseband output level (V_{DD}): 000 = 2 x VREF 001 = (16/15) x VREF 010 = (22/15) x VREF 011 = (8/15) x VREF 10x = (18/15) x VREF 11x = (20/15) x VREF
5	MSLOT	When this bit is cleared to 0, it sets single-slot modulation (only burst buffer 1 is used). When this bit is set to 1, it enables multislot mode modulation (burst buffer 0 and burst buffer 1 are used alternately).
4	BBMOD	When this bit is cleared to 0, it enables the GMSK mode.
3	BALOOP	When this bit is set to 1, internal analog loop of the I/Q uplink terminals is sent to the I/Q downlink terminals.
2−0	SELVMID(2:0)	Selects the value of output common mode of baseband uplink. 000 = VRABB/2 001 = 1.35 V 010 = 1.45 V 011 = 1.18 V 1xx = 1.25 V

5.3.13 Voiceband Codec Registers (VBC)

5.3.13.1 Voiceband Control Register 1

Register: **VBCTRL1**
Page: 1
Address: 8 (01000b)
Read/Write 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	VFBYP	VBDFAUXG	VSYNC	VCLKMODE	VALOOP	MICBIAS	VULSWITCH	VBUZ	VDLEAR	VDLAUX
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−50. Voiceband Control Register 1 Description

DATA BIT	FIELD NAME	DESCRIPTION
9	VFBYP	When this bit is cleared to 0, the voice filter, PGA, and volume control are not bypassed. If this bit is set to 1, the voice filter, PGA, and volume control are bypassed.
8	VBDFAUXG	When this bit is cleared to 0, the gain of AUXIN amplifier is 4.6 dB. When this bit is set to 1, the gain of AUXIN amplifier is 28.2 dB.
7	VSYNC	When this bit is set to 1, the digital modulator, the digital voice serial port, and the digital filter can be reset externally using the VDR terminal. At the reset using VDR, the filter will set VSYNC to 0.
6	VCLKMODE	When this bit is cleared to 0, this bit allows selection of the VCK terminal in burst mode. When this bit is set to 1, this bit allows selection of the VCK in continuous mode.
5	VALOOP	When this bit is set to 1, the internal analog loop of the output samples is sent to the input of the audio ADC. To avoid saturation of the analog path in this mode you must set: PGA downlink = −6 dB, PGA uplink = 0 dB, Volume = 0 dB, and SideTone = MUTE
4	MICBIAS	When this bit is cleared to 0, the analog bias for the electric microphone and external decoupling is driven to 2 V. When this bit is set to 1, the bias is driven to 2.5 V.
3	VULSWITCH	Enables the auxiliary input if this bit is cleared to 0. Enables the MICIN terminal if this bit is set to 1 and bit 0 (VULON) of the power-down register is set to 1 (see Section 5.3.4.3).
2	VBUZ	When this bit is set to 1, the auxiliary and ear stage are powered down even if bit 0 (VDLAUX) or bit 1 (VDLEAR) is 1.
1	VDLEAR	Enables the ear amplifier if bit 1 (VDLON) of the power-down register is set to 1 (see Section 5.3.4.3).
0	VDLAUX	Enables the auxiliary output amplifier if bit 1 (VDLON) of the power-down register is set to 1 (see Section 5.3.4.3).

5.3.13.2 Voiceband Control Register 2

Register: **VBCTRL2**
Page: 1
Address: 11 (01011b)
Read/Write 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD							MICNAUX	VDLHSO	MICBIASEL
Access Type	R	R	R	R	R	R	R	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−51. Voiceband Control Register 2 Description

DATA BIT	FIELD NAME	DESCRIPTION
9−3	RSVD	Reserved
2	MICNAUX	When this bit is set to 1, the HSMICP terminal is used. When this bit is 0, the AUXI terminal is used (these inputs are multiplexed in the ABB device).
1	VDLHSO	Enables the headset amplifier if bit 1 (VDLON) of the power-down register is set to 1 (see Section 5.3.4.3).
0	MICBIASEL	When this bit is set to 1, the HSMICBIAS terminal is active. When this bit is 0, the MICBIAS terminal is active.

5.3.13.3 Voiceband Pop Reduction Register

Register: **VBPOP**
Page: 1
Address: 10 (01010b)
Read/Write 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD	AUXAUTO	AUXCHG	AUXDIS	EARAUTO	EARCHG	EARDIS	HSOAUTO	HSOCHG	HSODIS
Access Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−52. Voiceband Pop Reduction Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	RSVD	Reserved
8,5,2	xAUTO†	1 = xCHG functionality runs in AUTOMATIC mode 0 = xCHG functionality runs in NORMAL mode
7,4,1	xCHG†	Enables the charging of the external capacitor (up to VRABB/2) This bit has no effect when bit 1 (VDLON) of the power-down register is set to 0 (see Section 5.3.4.3). Mode AUTOMATIC: This bit is set automatically to 1 when VDLON rise. This bit is cleared automatically to 0 when the corresponding VDLxxx bit of voiceband control register 1 is on (see Section 5.3.13.1). Write accesses have no effect. Mode NORMAL: This bit has no effect when the corresponding VDLxxx bit of voiceband control register 1 is set to 1 (see Section 5.3.13.1). Write accesses enable/disable the charge.
6,3,0	xDIS†	Enables the discharge of the external capacitor. This bit has no effect when either xCHG is set to 1, VDLON is set to 0, or VDLxxx is set to 1.

† x is AUX for AUXO outputs, EAR for earphone EAR outputs, or HSO for headset output.

5.3.13.4 Voiceband Uplink Register

Register: **VBUCTRL**
Page: 1
Address: 7 (00111b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	DXEN	VDLST3	VDLST2	VDLST1	VDLST0	VULPG4	VULPG3	VULPG2	VULPG1	VULPG0
Access Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−53. Uplink Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9	DXEN	When this bit is set to 1, the VDX signal is in mute mode. If this bit is cleared to 0, the VDX signal is in normal mode.
8−5	VDSLT(3:0)	Side tone levels: VDSLT3 / VDSLT2 / VDSLT1 / VDSLT0 / Relative Gain 1 1 0 1 −23 dB 1 1 0 0 −20 dB 0 1 1 0 −17 dB 0 0 1 0 −14 dB 0 1 1 1 −11 dB 0 0 1 1 −8 dB 0 0 0 0 −5 dB 0 1 0 0 −2 dB 0 0 0 1 1 dB 0 1 0 1 1 dB 1 0 0 0 Mute 1 0 0 1 Mute 1 0 1 0 Mute 1 0 1 1 Mute 1 1 1 0 Mute 1 1 1 1 Mute
4−0	VULPG(4:0)	Gain of the voice uplink programmable gain amplifier (−12 dB to +12 dB in 1-dB steps): VULPG4 / VULPG3 / VULPG2 / VULPG1 / VULPG0 / Relative Gain 1 0 0 0 0 −12 dB 1 0 1 1 1 −11 dB 1 1 0 0 0 −10 dB 1 1 0 0 1 −9 dB 1 1 0 1 0 −8 dB 1 1 0 1 1 −7 dB 0 0 0 0 0 −6 dB 0 0 0 0 1 −5 dB 0 0 0 1 0 −4 dB 0 0 0 1 1 −3 dB 0 0 1 0 0 −2 dB 0 0 1 0 1 −1 dB 0 0 1 1 0 0 dB 0 0 1 1 1 1 dB 0 1 0 0 0 2 dB 0 1 0 0 1 3 dB 0 1 0 1 0 4 dB 0 1 0 1 1 5 dB 0 1 1 0 0 6 dB 1 0 0 0 1 7 dB 1 0 0 1 0 8 dB 1 0 0 1 1 9 dB 1 0 1 0 0 10 dB 1 0 1 0 1 11 dB 1 0 1 1 0 12 dB

5.3.13.5 Voiceband Downlink Control Register

Register: **VBDCTRL**
Page: 0
Address: 6 (00110b)
Read/Write: 1/0

Data Bit	9	8	7	6	5	4	3	2	1	0
Name	RSVD			VOLCTL2	VOLCTL1	VOLCTL0	VDLPG3	VDLPG2	VDLPG1	VDLPG0
Access Type	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Value at Reset	0	0	0	0	0	0	0	0	0	0

Table 5−54. Voiceband Downlink Control Register Description

DATA BIT	FIELD NAME	DESCRIPTION
9−7	RSVD	Reserved
6−4	VOLCTL(2−0)	Volume control: VOLCTL2 / VOLCTL1 / VOLCTL0 / Relative Gain 0 / 1 / 0 / 0 dB 1 / 1 / 0 / −6 dB 0 / 0 / 0 / −12 dB 1 / 0 / 0 / −18 dB 0 / 1 / 1 / −24 dB 1 / 0 / 1 / Mute 0 / 0 / 1 / Mute 1 / 1 / 1 / Mute
3−0	VDLPG(3−0)	Gain of the voice downlink programmable gain amplifier: VDLPG3 / VDLPG2 / VDLPG1 / VDLPG0 / Relative Gain 0 / 0 / 0 / 0 / −6 dB 0 / 0 / 0 / 1 / −5 dB 0 / 0 / 1 / 0 / −4 dB 0 / 0 / 1 / 1 / −3 dB 0 / 1 / 0 / 0 / −2 dB 0 / 1 / 0 / 1 / −1 dB 0 / 1 / 1 / 0 / 0 dB 0 / 1 / 1 / 1 / 1 dB 1 / 0 / 0 / 0 / 2 dB 1 / 0 / 0 / 1 / 3 dB 1 / 0 / 1 / 0 / 4 dB 1 / 0 / 1 / 1 / 5 dB 1 / 1 / 0 / 0 / 6 dB 1 / 1 / 0 / 1 / −6 dB 1 / 1 / 1 / 0 / −6 dB 1 / 1 / 1 / 1 / −6 dB

6 Electrical Characteristics

6.1 Absolute Maximum Ratings Over Operating Free-Air Temperature (unless otherwise noted) †

Supply voltage range, VCDBB, VCIO, VCMEM, VCRAM, VCABB, and VCHG . . . . . –0.3 V to 7 V
Voltage on any input (Note 1) . . . . . –0.3 V to V_{DD} +0.3 V
Peak output current on the VRDBB terminal . . . . . 240 mA
Peak output current on the VRMEM terminal . . . . . 100 mA
Peak output current on the VRIO terminals . . . . . 240 mA
Peak output current on the VRRAM terminal . . . . . 100 mA
Peak output current on the VRABB terminal . . . . . 150 mA
Peak output current on all other terminals . . . . . –5 to 5 mA
Free-air temperature range . . . . . –30°C to 85°C
Maximum junction temperature T_j . . . . . 150°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: V_{DD} is UPR for terminals operated to battery voltage, VRIO is for terminals connected to the digital baseband device.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 80°C POWER RATING
GGM	2083 mW	16.7 mW/°C	1333 mW	1083 mW
GQW	1985 mW	15.3 mW/°C	1298 mW	1069 mW

NOTE: Board conditions are under JEDEC Standard 1S0P.

6.2 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
Main battery supply voltage VCDBB, VCIO1, VCIO2, VCMEM, VCRAM, VCABB	In regulation	3.0	3.6	5.5	V
Backup battery supply voltage VBACKUP	Main battery connected on VBACKUP	†	3.0	5.5	V
	Backup battery connected on VBACKUP	†	3.0	3.6	V
Battery charger supply voltage VCHG		4.8		7	V

† Minimum value depends on RESPWONz reset hysteresis and VRRTC characteristics.

6.3 Electrical Characteristics

Digital outputs (SIM card level shifter excepted)

PARAMETER	MIN	TYP	MAX	UNIT
Low level output voltage for ON_nOFF, RESPWONz, V_{OL} (I_{OL} = 10 µA) (Note 1)			0.2 VRRTC	V
High level output voltage for ON_nOFF, RESPWONz, V_{OH} (I_{OH} = 10 µA) (Note 1)	0.8 VRRTC			V
Low level voltage for outputs related to VRIO, V_{OL} (I_{OL} = 1 mA) (Note 1)			0.2 VRIO	V
High level voltage for outputs related to VRIO, V_{OH} (I_{OH} = 1 mA) (Note 1)	0.8 VRIO			V
Output current on 3-state outputs	−15		15	µA

Digital inputs (SIM card level shifter excepted)

PARAMETER		MIN	TYP	MAX	UNIT
High-level input voltage for ITWAKEUP, CK32K, V_{IH}		0.7 VRRTC			V
Low-level input voltage for ITWAKEUP, CK32K, V_{IL}				0.3 VRRTC	V
High-level voltage for all inputs, related to VRIO, V_{IH}		0.7 VRIO			V
Low-level voltage for all inputs, related to VRIO, V_{IL}				0.3 VRIO	V
High-level input voltage for TESTRSTz, VLRTC, VLMEM, V_{IH}		0.7 UPR			V
Low-level input voltage for TESTRSTz, VLRTC, VLMEM, V_{IL}				0.3 UPR	V
High-level input voltage for PWON, RPWON, V_{IH}		0.7 VBAT			V
Low-level input voltage for PWON, RPWON, V_{IL}				0.3 VBAT	V
Low-level input current @ 0 V	Standard and pulldown inputs	−1			µA
High-level input current @ 2.9 V (all inputs related to VRIO)	Standard and pullup inputs			1	µA
High-level input current @ 3.6 V (all inputs related to VBAT or UPR)	Standard and pullup inputs			1	µA
Low-level input current @ 0 V (TEST3, TEST4, TMS, TDI)	Pullup inputs	−20		−2	µA
Low-level input current @ 0 V (RPWON, PWON)	Pullup inputs	−40		−2	µA
Low-level input current @ 0 V (TESTRSTz)	Pullup inputs	−40		−2	µA
High-level input current @ 2.9 V (TCK)	Pulldown inputs	2		20	µA

SIM card level shifters

PARAMETER		MIN	TYP	MAX	UNIT
SIMCK	Low level output voltage V_{OL} (I_{OL} = 20 µA), SIMEN = 1			0.2 VRSIM	V
SIMCK	High level output voltage V_{OH} (I_{OH} = 20 µA), SIMEN = 1	0.7 VRSIM			V
SIMRST	Low level output voltage V_{OL} (I_{OL} = 200 µA), SIMEN = 1			0.2 VRSIM	V
SIMRST	High level output voltage V_{OH} (I_{OH} = 200 µA), SIMEN = 1	0.7 VRSIM			V
SIMIO	Low level output voltage V_{OL} (I_{OL} = 1 mA)			0.4	V

6.4 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Free-Air Temperature (unless otherwise noted)

6.4.1 Voltage Regulator VRDBB (Under Active Mode)

Voltage regulator VRDBB needs a 10-µF decoupling capacitor† connected between the VRDBB and GNDD terminals. The sense input feedback terminal (VSDBB) must be connected to the VRDBB terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCDBB		3.00	VBAT	5.5	V
Output voltage VRDBB	RDBB0 = 0 and RDBB1 = 1 (Default if VLRTC = 1)	1.65	1.80	1.95	V
	RDBB0 = 0 and RDBB1 = 0 (Default if VLRTC = 0)	1.35	1.50	1.65	
	RDBB0 = 1 and RDBB1 = 0	1.25	1.30	1.45	
Rated output current I_{OUT}				120	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum RDBB0 = 0 and RDBB1 = 0			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRDBB = final ±3%		10		µs
Turnon time	From RDBBEN = 0 to 1 @ I_{OUT} = maximum, VRDBB = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

† 0.1 Ω < ESR < 0.8 Ω

6.4.2 Voltage Regulator VRDBB (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCDBB		3.00	VBAT	5.5	V
Output voltage VRDBB	RDBB0 = 0 and RDBB1 = 1 (Default if VLRTC = 1)	1.65	1.85	1.95	V
	RDBB0 = 0 and RDBB1 = 0 (Default if VLRTC = 0)	1.35	1.50	1.65	
	RDBB0 = 1 and RDBB1 = 0	1.25	1.35	1.45	
Rated output current				1	mA

6.4.3 Voltage Regulator VRIO (Under Active Mode)

Voltage regulator VRIO needs a 10-µF decoupling capacitor† connected between the GNDD terminal and either the VRIO1 or VRIO2 terminal. The VRIO1 and VRIO2 terminals must be connected externally. The VCIO1 and VCIO2 terminals must also be connected externally.

NOTE: VRIO supplies the TWL3025 digital I/O and digital core.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCIO1 and VCIO2		3.00	VBAT	5.5	V
Output voltage VRIO1 and VRIO2		2.70	2.80	2.90	V
Rated output current I_{OUT}				100	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRIO = final ±3%		10		µs
Turnon time	From RIOEN = 0 to 1 @ I_{OUT} = maximum, VRIO = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

† 0.01 Ω < ESR < 0.5 Ω

6.4.4 Voltage Regulator VRIO (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCIO1 and VCIO2		3.00	VBAT	5.5	V
Output voltage VRIO1 and VRIO2		2.70	2.80	3.00	V
Rated output current				1	mA

6.4.5 Voltage Regulator VRRAM (Under Active Mode)

Voltage regulator VRRAM needs a 4.7-µF decoupling capacitor† connected between the VRRAM and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCRAM		3.00	VBAT	5.5	V
Output voltage VRRAM	VLMEM = 1	2.70	2.80	2.90	V
	VLMEM = 0	1.65	1.80	1.95	
Rated output current I_{OUT}				50	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum VLMEM = 0			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRRAM = final ±3%		10		µs
Turnon time	From RRAMEN = 0 to 1 @ I_{OUT} = maximum, VRRAM = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

† 0.01 Ω < ESR < 0.5 Ω

6.4.6 Voltage Regulator VRRAM (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCRAM		3.00	VBAT	5.5	V
Output voltage VRRAM	VLMEM = 1	2.70	2.80	3.00	V
	VLMEM = 0	1.65	1.80	1.95	
Rated output current				1	mA

6.4.7 Voltage Regulator VRMEM (Under Active Mode)

Voltage regulator VRMEM needs a 4.7-µF decoupling capacitor† connected between the VRMEM and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCMEM		3.00	VBAT	5.5	V
Output voltage VRMEM	VLMEM = 1	2.70	2.80	2.90	V
	VLMEM = 0	1.65	1.80	1.95	
Rated output current I_{OUT}				60	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum VLMEM = 0			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRMEM = final ±3%		10		µs
Turnon time	From RMEMEN = 0 to 1 @ I_{OUT} = maximum, VRMEM = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

† 0.01 Ω < ESR < 0.5 Ω

6.4.8 Voltage Regulator VRMEM (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCMEM		3.00	VBAT	5.5	V
Output voltage VRMEM	VLMEM = 1	2.70	2.85	3.00	V
	VLMEM = 0	1.65	1.85	1.95	
Rated output current				1	mA

6.4.9 Voltage Regulator VRSIM (Under Active Mode)

Voltage regulator VRSIM needs a 1-µF decoupling capacitor† connected between the VRSIM and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltages VCIO1 and VCIO2		3.00	VBAT	5.5	V
Output voltage VRSIM	SIMSEL = 1	2.75	2.85	3.0	V
	SIMSEL = 0	1.65	1.80	1.95	
Rated output current I_{OUT}				10	mA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum SIMSEL = 1			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRSIM = final ±3%		10		µs
Turnon time	From RSIMEN = 0 to 1 @ I_{OUT} = maximum, VRSIM = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

† 0.01 Ω < ESR < 0.5 Ω

6.4.10 Voltage Regulator VRSIM (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltages VCIO1 and VCIO2		3.00	VBAT	5.5	V
Output voltage VRSIM	SIMSEL = 1	2.75	2.85	3.1	V
	SIMSEL = 0	1.7	1.80	1.95	
Rated output current				1	mA

6.4.11 Voltage Regulator VRABB (Under Active Mode)

Voltage regulator VRABB needs a 4.7-µF decoupling capacitor† connected between the VRABB and GNDA terminals. VRABB is intended to supply the TWL3025 analog part only. Connecting any external device to the VRABB terminal may decrease device performance.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCABB		3.0	3.6	5.5	V
Output voltage VRABB		2.7	2.8	2.9	V
Rated output current I_{OUT}				50	mA
Load regulation	From I_{OUT} = maximum to I_{OUT} = 0			100	mV
Line regulation	Input voltage = 3.0 V to 5.5 V @ I_{OUT} = maximum			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRABB = final ±3%		10		µs
Turnon time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRABB = final ±3%		0.5		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		

† 0.01 Ω < ESR < 0.5 Ω

6.4.12 Voltage Regulator VRABB (Under Sleep Mode)

The switch between active/sleep mode is under the control of the VRPC device mode register.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage VCABB		3.00	VBAT	5.5	V
Output voltage VRABB		2.70	2.80	3.0	V
Rated output current				1	mA

6.4.13 Voltage Regulator VRRTC

Voltage regulator VRRTC needs a 1-µF decoupling capacitor† connected between the VRRTC and GNDD terminals.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage		2.7	UPR	5.5	V
Output voltage VRRTC	RRTC0 = 0 and RRTC1 = 1 (Default if VLRTC = 1)	1.65	1.80	1.95	V
	RRTC0 = 0 and RRTC1 = 0 (Default if VLRTC = 0)	1.35	1.50	1.65	
	RRTC0 = 1 and RRTC1 = 0	1.25	1.30	1.45	
Rated output current I_{OUT}				30	µA
Load regulation	I_{OUT} = maximum to 0			100	mV
Line regulation	Input voltage = 2.7 V to 5.5 V @ I_{OUT} = maximum RRTC0 = 0 and RRTC1 = 0			50	mV
Response time	I_{OUT} steps from 0 to I_{OUT} maximum I_{OUT} steps from I_{OUT} maximum to 0 @ VRRTC = final ±3%		100		µs
Turnon time	From VBAT = 0 V to 3.6 V @ I_{OUT} = maximum, VRRTC = final ±3%		0.2		ms
Ripple rejection	f = 100 Hz @ I_{OUT} maximum		55		dB
	f = 500 kHz @ I_{OUT} maximum		35		
Quiescent current			2	4	µA

† 0.01 Ω < ESR < 0.5 Ω

6.4.14 Band Gap Reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage on VREF	ACTIV mode	1.16	1.18	1.20	V
Output voltage on IBIAS	RBIAS = 100 kΩ	1.14	VREF	1.21	V

6.5 Current Consumption

All current consumption measurements are done with:

- RBIAS is 100 kΩ

6.5.1 Device OFF Modes

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF mode	Battery 5.5 V, CK13M clock off, no load on any LDO, BBCHGEN = 0, MSKOFFxxx = 0, measured on main battery, MESBB = 0, MESBAT = 0, Backup battery 3.2 V		25	55	µA
SLEEP mode	Main battery 5.5 V, CK13M clock off, no load, BBCHGEN = 0, measure on main battery, all regulators are on except VRABB, MESBB = 0, MESBAT = 0, Backup battery 3.2 V, −30°C to 25°C		80	150	µA
SLEEP mode	Main battery 5.5 V, CK13M clock off, no load, BBCHGEN = 0, measure on main battery, all regulators are on except VRABB, MESBB = 0, MESBAT = 0, Backup battery 3.2 V, 85°C		80	200	µA
SLEEP mode VRABB	Main battery 5.5 V, CK13M clock off, no load, BBCHGEN = 0, measure on main battery, all regulators are on, MESBB = 0, MESBAT = 0, Backup battery 3.2 V, −30°C to 25°C		160	300	µA
BACKUP on backup battery	Backup battery 3.2 V, main battery 0 V, CK13M clock off, no load, measured on backup battery, RESPWONz = 1		3.0	6	µA

6.5.2 Device ON Modes

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACTIV mode: idle	Battery 5.5 V CK13M clock is off. CK32K clock is on. No external loads are on LDO.		0.7	1	mA
ACTIV mode: power on	Battery 5.5 V CK13M clock is on. All blocks are in power down, power management is excepted. No external loads are on LDO.		1.3	2.0	mA

6.5.3 Blocks Power Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voiceband codec (VBC)	See Note 2		6.5		mA
Baseband codec (BBC + APC)	BULENA = 1, BDLENA = 1		22		mA
Frequency control (AFC)			0.6		mA
Auxiliary DAC (ADAC)			0.4		mA
Monitoring ADC (MADC)			0.5		mA
SIM interface			0.3		mA

NOTE 2: Measurements are for blocks in power up mode without transmit or receive activity. System clock is running on 13 MHz.

The consumption is given for a standalone block. To have the total consumption, add the current described in Section 6.5.2, *Device ON Modes*.

6.5.4 Power ON / Power OFF Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery voltage to enter ACTIV mode from OFF mode	Measured on the VBAT terminal		3.2		V
Battery voltage to enter BACKUP mode from ACTIV mode	VBACKUP 3.2, measured on the VBAT terminal, monitored on the ON_nOFF terminal	2.6		2.9	V

6.5.5 Backup ON / Backup OFF Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery voltage to enter OFF mode from NOBAT mode RESPWONz high level	Measured on the UPR terminal Monitored on the RESPWONz terminal	2.5		3.2	V
Battery voltage to enter NOBAT mode from BACKUP mode RESPWONz low level	Measured on the UPR terminal Monitored on the RESPWONz terminal	1.8	2.1	2.4	V

6.6 SIM Card Interface

6.6.1 Switching Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock frequency DBBSCK/SIMCK	C_L = 30 pF	1.0		5.0	MHz
Rise and fall time at SIMCK	C_L = 30 pF			20	ns
Rise and fall time at DBBSIO/SIMIO	C_L = 30 pF			1	µs
Rise and fall time at SIMRST	C_L = 30 pF			400	µs
Data rate on DBBSIO/SIMIO				CK13M/32	MHz

6.7 Battery Charger Interface

VBAT = 3.6 V unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCHG input voltage range (see Note 3)		4.8		6.8	V
VCHG to MADC input attenuation	VCHG from 4.8 V to 6.8 V	0.15	0.20	0.30	V/V
VBACKUP to MADC input attenuation	VBACKUP from 2.4 V to 5.5 V	0.2	0.25	0.35	V/V
VBAT to MADC input attenuation	VBAT from 3.0 V to 5.5 V	0.2	0.25	0.35	V/V
ICTL output voltage swing	CHEN = 1, VCHG = 6.8 V, CHBPASSPA = 1			0.8	V
	CHEN = 1, VCHG = 6.8 V, CHDISPA = 1	VCHG−0.3			
Precharge R_{ON}	Measure between VCHG and PRECH. I_{PRECH} = 100 mA, VBAT = 0.5 V			8	Ω
Battery voltage at precharge end	VBAT open. Maximum current depends on an external resistor.	3.6	3.8	4.0	V
Current-to-voltage conversion slope (see Note 4)	R_S = 0.2 Ω (VCCS−VBATS) from 0.1 V to 0.17 V	1.6	2	2.4	mV/mA
Current-to-voltage conversion offset	R_S = 0.2 Ω		0.2		V
ADIN2 dc current source for temperature measurement	R(IBIAS) = 100 kΩ, ADIN2 = 1 V 8 possible ranges (register BCICTL1, bits THSENS2−0)				µA
	Code = 0	8		12	
	Code = 1	16		24	
	Code = 2	26		34	
	Code = 3	36		44	
	Code = 4	46		54	
	Code = 5	55.5		64.5	
	Code = 6	65.5		74.5	
	Code = 7	75		85	
ADIN1 dc current source for battery identification	R_{IBIAS} = 100 kΩ, ADIN1 = 1 V	8		12	µA
Backup battery charging current	VBACKUP = 2.8 V, BBCHEN = 1	400	500	1200	µA
End backup battery charging voltage: VBBCHGEND	$I_{VBACKUP}$ = −10 µA, BBSEL = 00	2.9	3.1	3.3	V
	$I_{VBACKUP}$ = −10 µA, BBSEL = 01	3.0	3.2	3.4	V
	$I_{VBACKUP}$ = −10 µA, BBSEL = 10	3.1	3.3	3.5	V

NOTES: 3. The maximum voltage value of the charging device is 6.8 V (process limitation). The minimum voltage value of the charging device is:
VBATMAX + diode drop + 0.2-Ω resistor drop + VDC drop.
Where VBATMAX is the maximum voltage value of the battery (4.2 V for Li-Ion battery). For example, to charge Li-Ion battery with 1-A fast current charge, the minimum voltage value of the charging device must be 5.1 V.

4. MADC output code = (VCCS − VBATS) * 10 + offset

6.8 ADC Characteristics

6.8.1 Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			10		Bit
MADC voltage reference			1.75		V
Input leakage current ADINx				1	µA
Differential nonlinearity	Input range 0 to 1.75 V	−2		2	LSB
Integral nonlinearity	Best fitting, input range 0 to 1.5 V	−1		1	LSB
	Best fitting, input range 1.5 V to 1.75 V	−3		3	LSB

6.8.2 Switching Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Running frequency F		1		MHz
Clock period t = 1/F		1		µs
Conversion time (16t = delay before the sampling of the analog input)		16t + 8.5t		µs

6.8.3 Global Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Input resistance		5.7		kΩ

6.9 Automatic Power Control (APC)

6.9.1 DAC 10 Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			10		Bit
Integral nonlinearity	Best fitting line	−1		+1	LSB
Differential nonlinearity		−1		+1	LSB
Settling time			5		µs

6.9.2 Output Stage Characteristics

The recommended load on the APC terminal is a 50-pF (maximum value) capacitor in parallel with a 10-kΩ (minimum value) resistor.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage with code maximum		2	2.2	2.4	V
Offset voltage	AUXAPC = 0 APCOFF = 0		110	200	mV
Offset voltage adjustment			130	150	mV
Offset voltage adjustment step			2	2.3	mV
Output impedance in power down				150	Ω
Output voltage in power down				50	mV

6.9.3 Timings

PARAMETER		MIN	TYP	MAX	UNITS
t_{DELUP}	Delay BULEN ↑ to ramp-up start	2		1025	1/4-bit
t_{DELCHG}	Delay SLOT N modulation start to SLOT N ramp-up start	2		1025	bit
t_{DELDWN}	Delay BULEN ↓ to ramp-down start	2		1025	1/4-bit
t_{RUP}	Ramp-up duration	0		16	1/2-bit
t_{RDWN}	Ramp-down duration	0		16	1/2-bit
t_{TAIL}	Modulation after BULEN ↓		32		1/4-bit
t_{SLOT}	Delay SLOT N ramp-up to SLOT N+1 ramp-up start (same DELUP settings)		156.25		bit

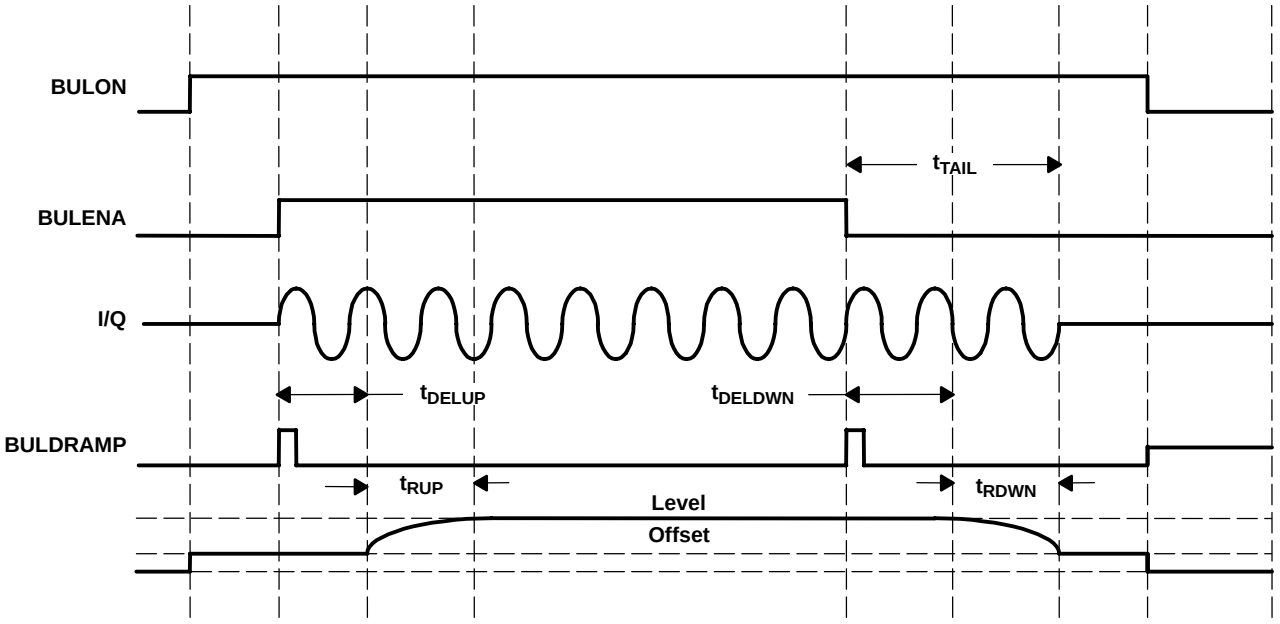


Figure 6−1. APC Single-Slot Timing

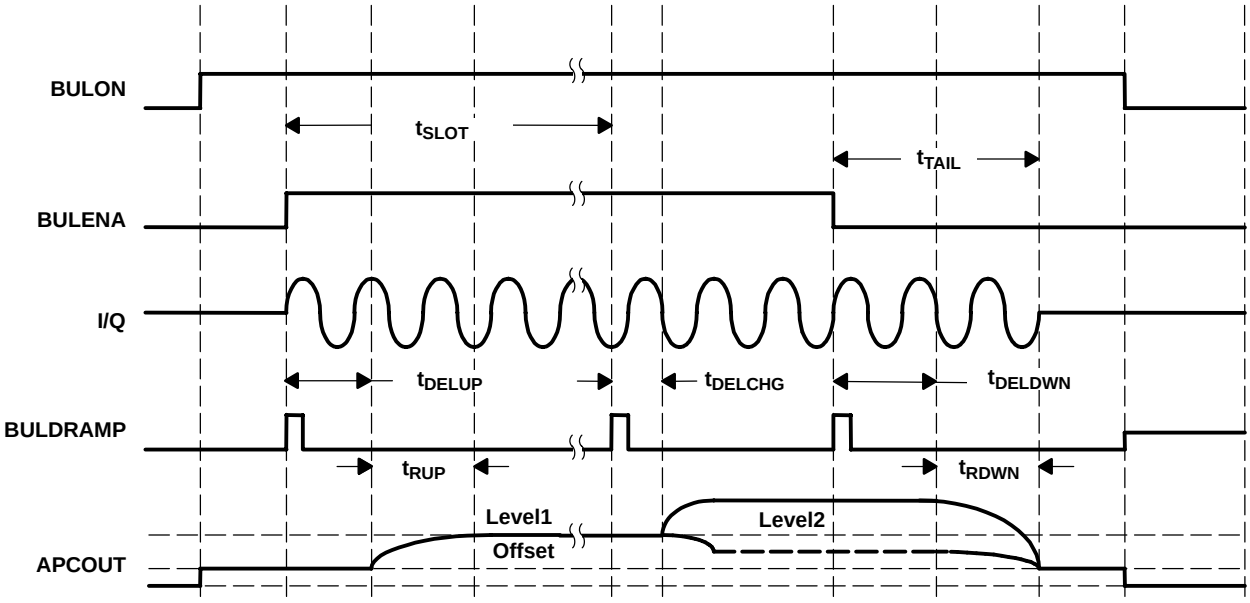


Figure 6−2. APC Multislot Timing

6.10 Clocks and Interrupts

PARAMETER	MIN	TYP	MAX	UNITS
Master clock signal frequency CK13M		13		MHz
Master clock duty-cycle CK13M	45	50	55	%
Real-time clock signal frequency CK32K		32.668		kHz
Real-time clock duty-cycle CK32K	45	50	55	%

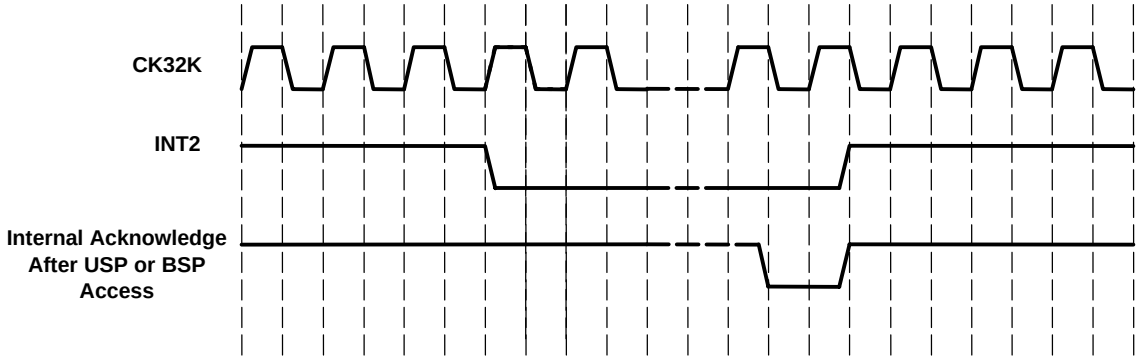


Figure 6−3. Interrupt 2 Timing

6.11 USP Interface Timings Requirements

PARAMETER		MIN	TYP	MAX	UNITS
t_{SU1}	UEN setup delay before CK13M ↑	15			ns
t_{H1}	UEN hold after CK13M ↑ − (CK13M period − t1)	15			ns
t_{SU2}	UDR setup delay before CK13M low	15			ns
t_{H2}	UDR hold after CK13M ↓	15			ns
t_{D1}	UDX delay after CK13M ↑			28	ns
Time between continuous words (with no BSP access)		3			t
Time between continuous words (with a BSP concurrent access)		7			t

t = CK13M clock period = 77 ns

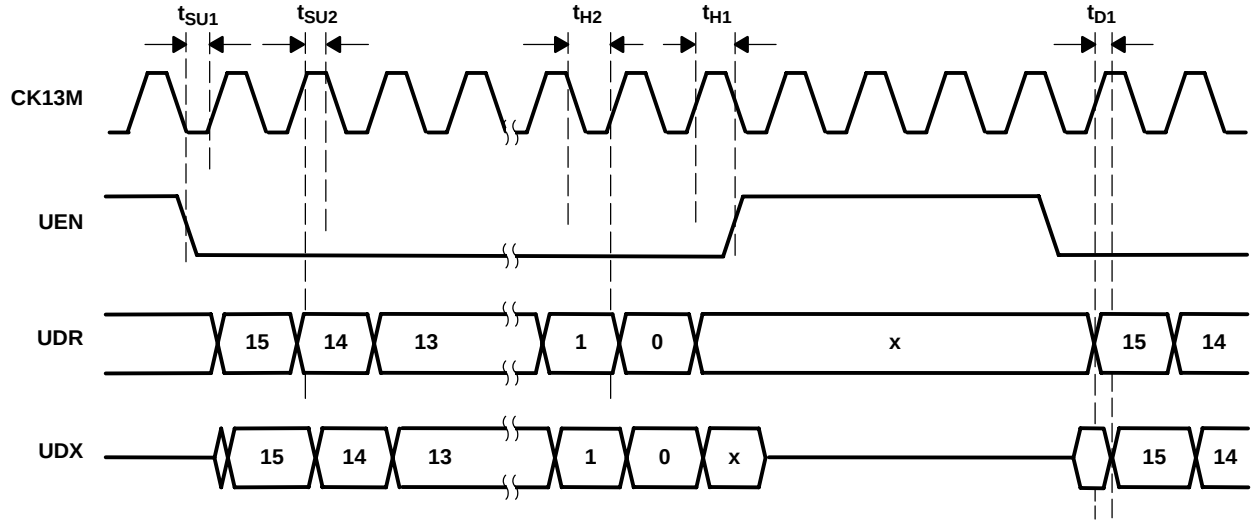


Figure 6−4. Receive and Transmit USP Operations

6.12 TSP Interface Timings Requirements

	PARAMETER	MIN	TYP	MAX	UNITS
t1	TEN ↓ setup time before CK13M ↑	0	65		ns
t2	TDR valid after TEN ↓		t		ns
t3	Bit duration		2t		ns
t4	Data duration		14t		ns
t5	TEN low hold time after last bit		t		ns
t6	TEN setup time (low to high) before CK13M high		65		ns

t = CK13M clock period = 77 ns

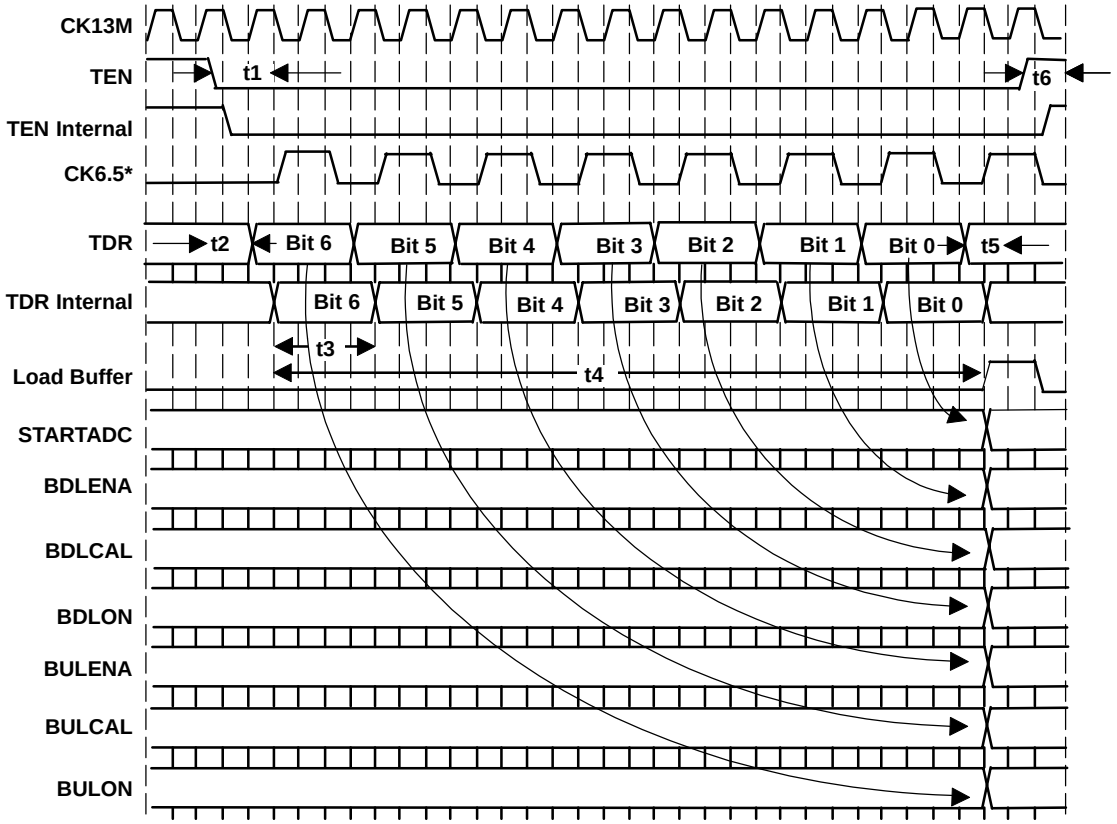
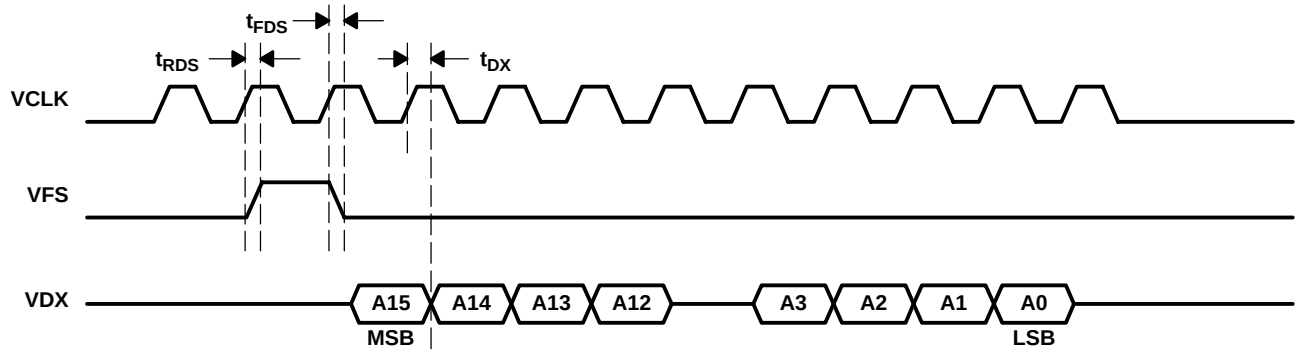


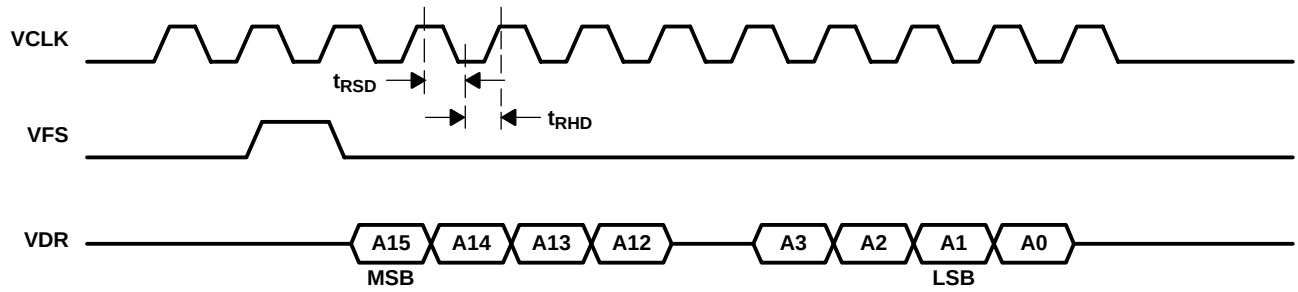
Figure 6−5. TSP Interface Timing Diagram

6.13 VSP Interface Timings Requirements

PARAMETER	MIN	TYP	MAX	UNITS
VCK signal frequency		CK13M/26		kHz
VCK signal jitter	−2		2	µs
VCK duty cycle	40	50	60	%
t_{RDS} VFS ↑ delay after VCK ↑ (CL = 10 pf, VCK = 0.3*VRIO, VFS = 0.3*VRIO)	−7		2	ns
t_{FDS} VFS ↓ delay after VCK ↑ (CL = 10 pf, VCK = 0.3*VRIO, VFS = 0.7*VRIO)	−7		2	ns
t_{DX} VDX delay after VCK ↑	0		100	ns
t_{RSD} VDR setup time before VCK ↓	100			ns
t_{RHD} VDR hold time after VCK ↓	100			ns



Transmit Operation



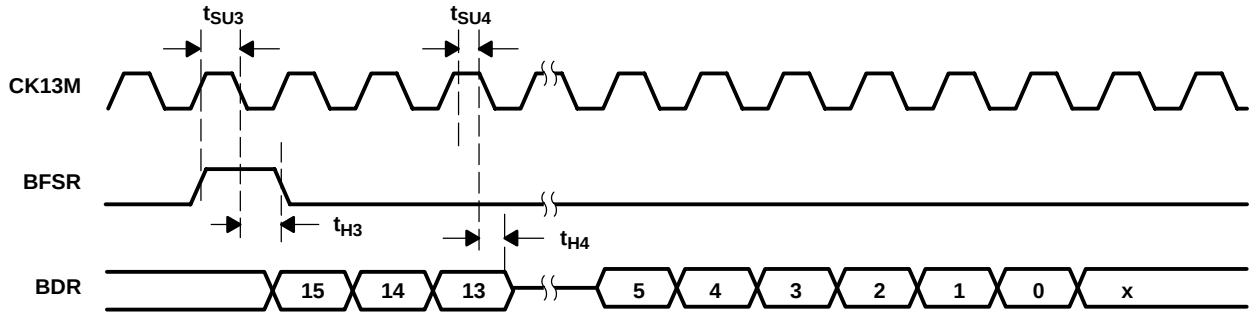
Receive Operation

Figure 6−6. Audio Serial Port Operations

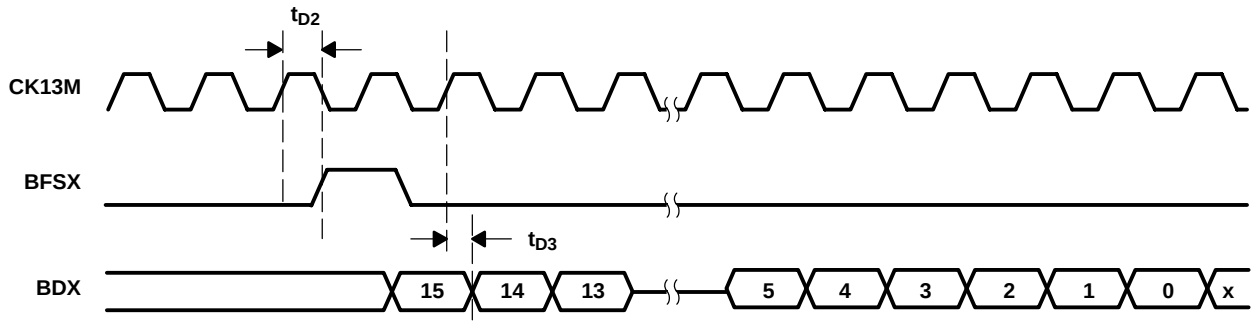
6.14 BSP Interface Timings Requirements

	PARAMETER	MIN	TYP	MAX	UNITS
t_{SU3}	BFSR setup time before CK13M ↓	15			ns
t_{H3}	BFSR hold time after CK13M ↓	15			ns
t_{SU4}	BDR setup time before CK13M ↓	15			ns
t_{H4}	BDR hold time after CK13M ↓	15			ns
t_{D2}	BFSX delay from CK13M ↑			28	ns
t_{D3}	BDX delay after CK13M ↑			28	ns

t = CK13M clock period = 77 ns



Receive Operation



Transmit Operation

Figure 6−7. Single BSP Operations

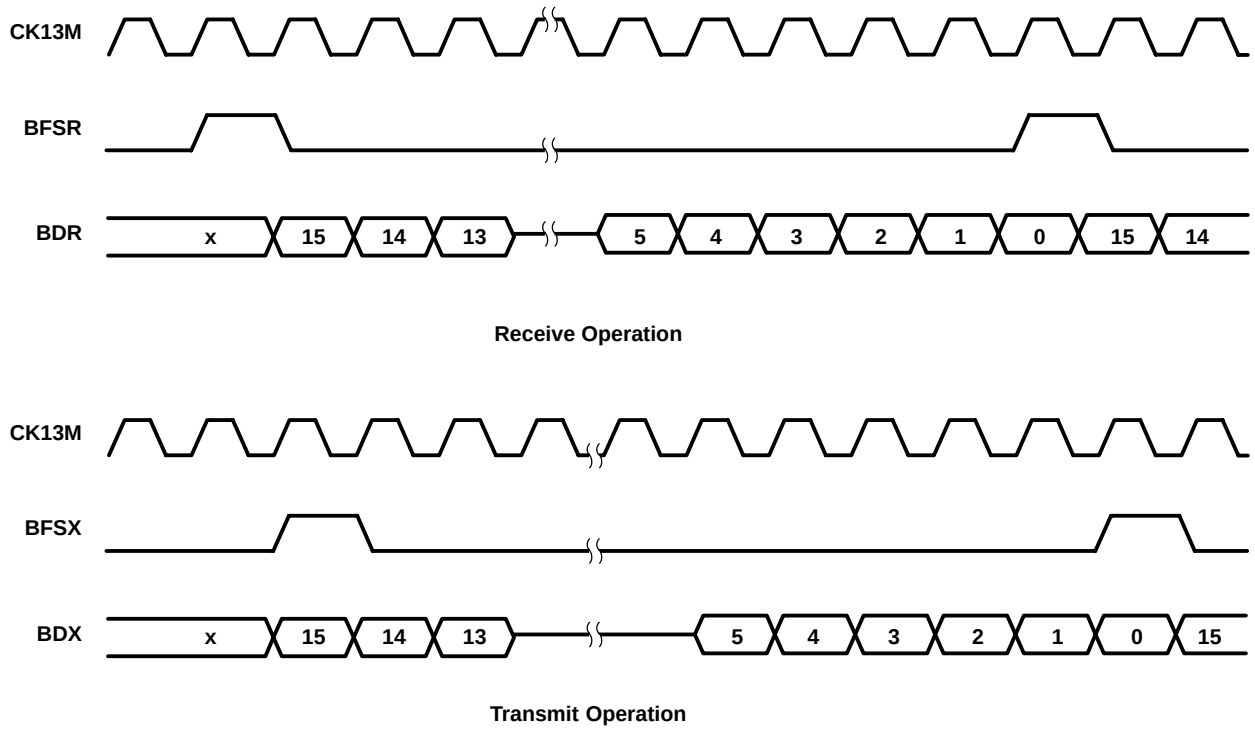


Figure 6−8. Adjacent BSP Operations

6.15 JTAG Interface Timings Requirements

PARAMETER		MIN	TYP	MAX	UNITS
TCK frequency			6.5		MHz
t_{SUMS}	Setup time TMS to TCK ↑	15			ns
t_{SUDI}	Setup time TDI to TCK ↑	15			ns
t_{DDO}	Delay time TDO from TCK ↓			30	ns

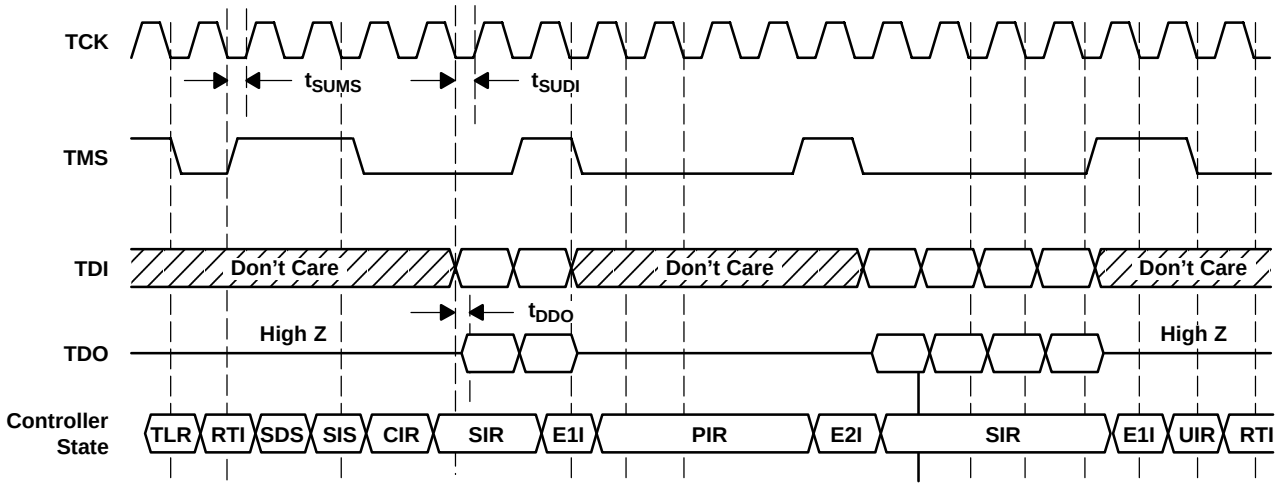


Figure 6−9. Controller State

6.16 Operating Characteristics

6.16.1 Voiceband Codec

6.16.1.1 Voiceband: Uplink Path

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum input range (MICIP−MICIN)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB)		32.5		mVrms
Maximum input range (AUXI)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB) and VBDFAUXG = 0		365		mVrms
	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB) and VBDFAUXG = 1		24		mVrms
Maximum input range (HSMICP)	Inputs 3 dBm0 (maximum digital sample amplitude with PGA gain set to 0 dB)		78		mVrms
Nominal reference level (MICIP−MICIN)			−10		dBm0
Nominal reference level at AUXI			−10		dBm0
Nominal reference level at HSMICP			−10		dBm0
Differential input resistance (MICIP−MICIN)			36		kΩ
Microamplifier gain (MICIP−MICIN)			25.6		dB
Auxiliary gain amplifier (AUXI)	VBDFAUXG = 0		4.6		dB
	VBDFAUXG = 1		28.2		
Headset microamplifier gain (HSMICP)			18		dB
Input resistance at AUXI	VBDFAUXG = 0	100	160	240	kΩ
DC level at MICBIAS	MICBIAS bit = 0, $I_{MICBIAS}$ = 0 to 2 mA	1.9		2.1	V
	MICBIAS bit = 1, $I_{MICBIAS}$ = 0 to 2 mA	2.4		2.6	
DC level at HSMICBIAS	MICBIAS bit = 0, $I_{MICBIAS}$ = 0 to 2 mA	1.9		2.1	V
	MICBIAS bit = 1, $I_{MICBIAS}$ = 0 to 2 mA	2.4		2.6	
Current capability at MICBIAS		0		2	mA
Current capability at HSMICBIAS		0		2	mA
PGA absolute gain	VULPGA code 10000 −12 dB	−12.5	−12	−11.5	dB
	VULPGA code 10111 −11 dB	−11.5	−11	−10.5	
	VULPGA code 11000 −10 dB	−10.5	−10	−9.5	
	VULPGA code 11001 −9 dB	−9.5	−9	−8.5	
	VULPGA code 11010 −8 dB	−8.5	−8	−7.5	
	VULPGA code 11011 −7 dB	−7.5	−7	−6.5	
	VULPGA code 00000 −6 dB	−6.5	−6	−5.5	
	VULPGA code 00001 −5 dB	−5.5	−5	−4.5	
	VULPGA code 00010 −4 dB	−4.5	−4	−3.5	
	VULPGA code 00011 −3 dB	−3.5	−3	−2.5	
	VULPGA code 00100 −2 dB	−2.5	−2	−1.5	
	VULPGA code 00101 −1 dB	−1.5	−1	−0.5	
	VULPGA code 00110 0 dB	−0.5	0	0.5	
	VULPGA code 00111 1 dB	0.5	1	1.5	
	VULPGA code 01000 2 dB	1.5	2	2.5	
	VULPGA code 01001 3 dB	2.5	3	3.5	
	VULPGA code 01010 4 dB	3.5	4	4.5	
	VULPGA code 01011 5 dB	4.5	5	5.5	

Global characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PGA absolute gain (continued)	VULPGA code 01100 6 dB	5.5	6	6.5	dB
	VULPGA code 10001 7 dB	6.5	7	7.5	
	VULPGA code 10010 8 dB	7.5	8	8.5	
	VULPGA code 10011 9 dB	8.5	9	9.5	
	VULPGA code 10100 10 dB	9.5	10	10.5	
	VULPGA code 10101 11 dB	10.5	11	11.5	
	VULPGA code 10110 12 dB	11.5	12	12.5	
	Others cases	−6.5	−6	−5.5	
Power supply rejection	0 Hz to 100 kHz	40			dB

Frequency response

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency response relative to reference gain at 1 kHz	$\leq$ 100 Hz			−20	dB
	100 Hz to 200 Hz			−10	
	300 Hz to 400 Hz	−2	0	1	
	400 Hz to 3300 Hz	−1	0	1	
	3300 Hz to 3400 Hz	−2	0	1	
	4000 Hz to 4600 Hz			−17	
	4600 Hz to 6000 Hz			−40	
	$\geq$ 6000 Hz			−45	

Psophometric SNR

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Psophometric SNR	3 dBm0	35			dB
	0 dBm0	40			
	−5 dBm0	42			
	−10 dBm0	45			
	−20 dBm0	42			
	−30 dBm0	40			
	−40 dBm0	30			
	−50 dBm0	20			
Maximum idle channel noise	Measure with MICIN−MICIP inputs			−72	dB
Crosstalk with the downlink path	With 33 Ω on EAR output and 26 dB on AUXI gain			−66	dB

Gain characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute gain error	At 0 dBm0 and 1 kHz	−1		1	dB
	At −10 dBm0 and 1 kHz	−11		−9	
Gain tracking error relative to −10 dBm0 reference level	3 dBm0	−0.25		0.25	dB
	0 dBm0	−0.25		0.25	
	−5 dBm0	−0.25		0.25	
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.35		0.35	
	−50 dBm0	−0.5		0.5	
Number of meaningful output bits	PGA set to 0 dB		13		Bit

6.16.1.2 Voiceband: Downlink Path

Output load conditions (see Figure 6−10)

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential	Output swing 3.9 V_{PP}	120			Ω
Minimum resistive load between EARP and EARN: R//	Output swing 1.5 V_{PP}	33			
Differential Maximum capacitor load between EARP and EARN: C//				100	pF
Common mode Minimum resistive load at EARP or EARN			200		kΩ
Common mode Maximum capacitor load at EARP or EARN				10	pF
Minimum output resistive load between AUXOP and AUXON: R//		1	1.2		kΩ
Maximum capacitor load between AUXOP and AUXON: C//				100	pF
Common mode Minimum resistive load at AUXOP or AUXON			200		kΩ
Common mode Maximum capacitor load at AUXOP or AUXON				10	pF
Minimum output resistive load at HSO: R//			32		Ω
Maximum capacitor load at HSO: C//				100	pF
Coupling capacitor load at HSO			22		µF

Global characteristics

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum output swing (EARP−EARN)	5% distortion and 120 Ω	3.1	3.92		V_{PP}
	5% distortion and 33 Ω	1.2	1.5		
Earphone amplifier gain			1		dB
Earphone amplifier state in power down			High Z		
Maximum output swing at (AUXOP − AUXON)	5% distortion maximum, load = 1 kΩ	1.6	1.96		V_{PP}
Auxiliary amplifier gain			−5		dB
Auxo amplifier state in power down			High Z		
Maximum output swing at (HSO)	5% distortion maximum, load = 32 Ω	1.6	1.96		V_{PP}
Headset amplifier gain		−7		−5	dB
Headset amplifier state in power down			High Z		
Power supply rejection		40			dB

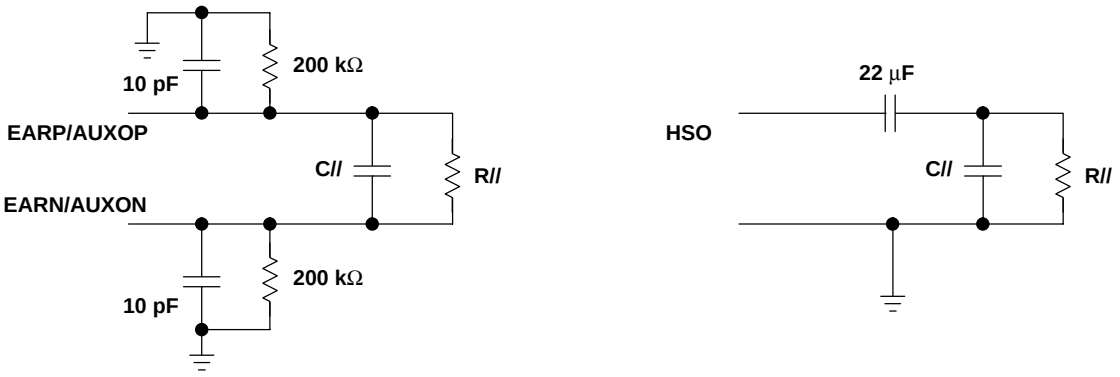


Figure 6−10. Output Loading

Volume Control Gain

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Default and reference	VOCTL code 010	−1	0	1	dB
	VOCTL code 110	−7	−6	−5	
	VOCTL code 000	−13	−12	−11	
	VOCTL code 100	−19	−18	−17	
	VOCTL code 011	−25	−24	−23	
Mute	VOCTL code 101, 001, 111			−40	dB

PGA Gain Step

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Default	VDLPGA code 0000 −6 dB	−6.5	−6	−5.5	dB
	VDLPGA code 0001 −5 dB	−5.5	−5	−4.5	
	VDLPGA code 0010 −4 dB	−4.5	−4	−3.5	
	VDLPGA code 0011 −3 dB	−3.5	−3	−2.5	
	VDLPGA code 0100 −2 dB	−2.5	−2	−1.5	
	VDLPGA code 0101 −1 dB	−1.5	−1	−0.5	
Reference	VDLPGA code 0110 0 dB	−0.5	0	0.5	dB
	VDLPGA code 0111 1 dB	0.5	1	1.5	
	VDLPGA code 1000 2 dB	1.5	2	2.5	
	VDLPGA code 1001 3 dB	2.5	3	3.5	
	VDLPGA code 1010 4 dB	3.5	4	4.5	
	VDLPGA code 1011 5 dB	4.5	5	5.5	
	VDLPGA code 1100 6 dB	5.5	6	6.5	
	Other cases	−6.5	−6	−5.5	

Sidetone Gain Step

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference	VDLST code 1101	−23 dB	−24	−23	−22	dB
	VDLST code 1100	−20 dB	−21	−20	−19	
	VDLST code 0110	−17 dB	−18	−17	−16	
	VDLST code 0010	−14 dB	−15	−14	−13	
	VDLST code 0111	−11 dB	−12	−11	−10	
	VDLST code 0011	−8 dB	−9	−8	−7	
	VDLST code 0000	−5 dB (reference)	−6	−5	−4	
	VDLST code 0100	−2 dB	−3	−2	−1	
	VDLST code 0001	1 dB	0	1	2	
	VDLST code 0101	1 dB	0	1	2	
	VDLST code 1000	Mute			−66	
	other cases	Mute			−66	

Frequency response

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency response relative to reference gain at 1 kHz	≤ 50 Hz			−10	dB
	50 Hz to 160 Hz			−3	
	300 Hz to 400 Hz	−2	0	1	
	400 Hz to 3300 Hz	−1	0	1	
	3300 Hz to 3400 Hz	−2	0	1	
	4000 Hz to 4600 Hz			−17	
	4600 Hz to 6000 Hz			−40	
	≥ 6000 Hz			−45	

Psophometric SNR

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Psophometric SNR	3 dBm0	35			dB
	0 dBm0	45			
	−5 dBm0	52			
	−10 dBm0	57			
	−20 dBm0	54			
	−30 dBm0	52			
	−40 dBm0	42			
	−50 dBm0	32			
Maximum idle channel noise				−86	dBm0
Crosstalk with the uplink path	With 33 Ω on EAR output and 26 dB on AUXI gain			−66	dB

Gain characteristics

NOTE: For the EAR output, the test condition includes only a 120-Ω output load unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute gain error	At 0 dBm0 and 1 kHz (with 120 Ω on EAR output)	−1	0	1	dB
	At −10 dBm0 and 1 kHz (with 120 Ω on EAR output)	−11	−10	−9	
Gain tracking error	3 dBm0	−0.25		0.25	dB
	0 dBm0	−0.25		0.25	
	−5 dBm0	−0.25		0.25	
	−10 dBm0 (reference)		0		
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.35		0.35	
	−50 dBm0	−0.5		0.5	
Number of meaningful output bits	PGA and VOCTL set to 0 dB		15		Bit

6.16.1.3 Voiceband Timing Characteristics

After turning VRIO from OFF to ON, bits 1 (VDLON) and 0 (VULON) of the power down register (see Section 5.3.4.3) have to be set to 1 at the same time for at least 125 μs to allow proper initialization of the RAM in the voice digital filter. This initialization is required to avoid potential limit cycle oscillations in the digital filter due to random initial RAM content.

6.16.2 Baseband Uplink General Characteristics

6.16.2.1 Baseband: Uplink Path

dc characteristics

Output load is 10 kΩ in parallel with 47 pF from the BULIP terminal to the BULIM terminal and from the BULQP terminal to the BULQM terminal + 50 kΩ in parallel with 10 pF on the BULIP, BULIM, BULQP, and BULQM terminals to the VSS terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I and Q DAC resolution			10		bit
Voltage reference BBVREF†			1.75		V
Dynamic range on each output	Centered on VVMID		1.75		V_{PP}
Differential output dynamic range between BULIP and BULIM or between BULQP and BULQM	OUTLEV0 = 0 OUTLEV1 = 0 OUTLEV2 = 0		3.5		V_{PP}
	OUTLEV0 = 0 OUTLEV1 = 1 OUTLEV2 = 0		2.56		
	OUTLEV0 = 1 OUTLEV1 = 0 OUTLEV2 = 0		1.86		
	OUTLEV0 = 1 OUTLEV1 = 1 OUTLEV2 = 0		0.93		
	OUTLEV0 = 0 or 1 OUTLEV1 = 0 OUTLEV2 = 1		2.10		
	OUTLEV0 = 0 or 1 OUTLEV1 = 1 OUTLEV2 = 1		2.33		
Output common mode voltage VVMID	SELMID0 = 0 SELMID1 = 0 SELMID2 = 0	VRABB/2 − 5%	VRABB/2	VRABB/2 + 5%	V
	SELMID0 = 1 SELMID1 = 0 SELMID2 = 0	1.30	1.35	1.40	
	SELMID0 = 0 SELMID1 = 1 SELMID2 = 0	1.40	1.45	1.50	
	SELMID0 = 0 or 1 SELMID1 = 0 or 1 SELMID2 = 1	1.20	1.25	1.30	
	SELMID0 = 1 SELMID1 = 1 SELMID2 = 0	1.12	1.18	1.25	
Offset error before calibration		−100		100	mV
Offset error after calibration		−10		10	mV
I and Q output state in power down			High Z		

† Internal reference

ac characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute gain error relative to V_{VREF}	Measured on 67.7 kHz sine wave	−0.9		0.9	dB
Gain matching between channels I and Q	Measured on 67.7 kHz	−0.3	0	0.3	dB
Modulation spectrum mask. Measured by average of FFTs on random modulated bursts using a flat-top window with 30-kHz bandwidth	100 kHz			0.5	dB
	200 kHz			−34	dB
	250 kHz			−37	dBc
	400 kHz			−65	dBc
	600 kHz			−72	dBc
	800 kHz			−72	dBc
GMSK phase trajectory error				6	°Peak
				1.5	°Rms

Timing characteristics: these values are given for system information only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{SU1}	Setup time, BULON ↑ to BULCAL ↑		15			µs
t_{W1}	Pulse duration BULCAL high		72			1/4-bit†
t_{SU2}	Setup time, BULCAL ↓ to BULENA ↑		0			1/4-bit†
t_{W2}	Pulse duration BULENA high	N effective duration of burst		N − 32		1/4-bit†
t_{H1}	Modulation hold time after BULENA ↓			32		1/4-bit†
t_{H2}	Hold time BULON after BULENA ↓		32			1/4-bit†
t_{D1}	Modulator input to output delay	From BULENA ↑ to middle of first bit		2.5		1/4-bit†

† Bit is relative to GSM bit = 1/270.833 kHz.

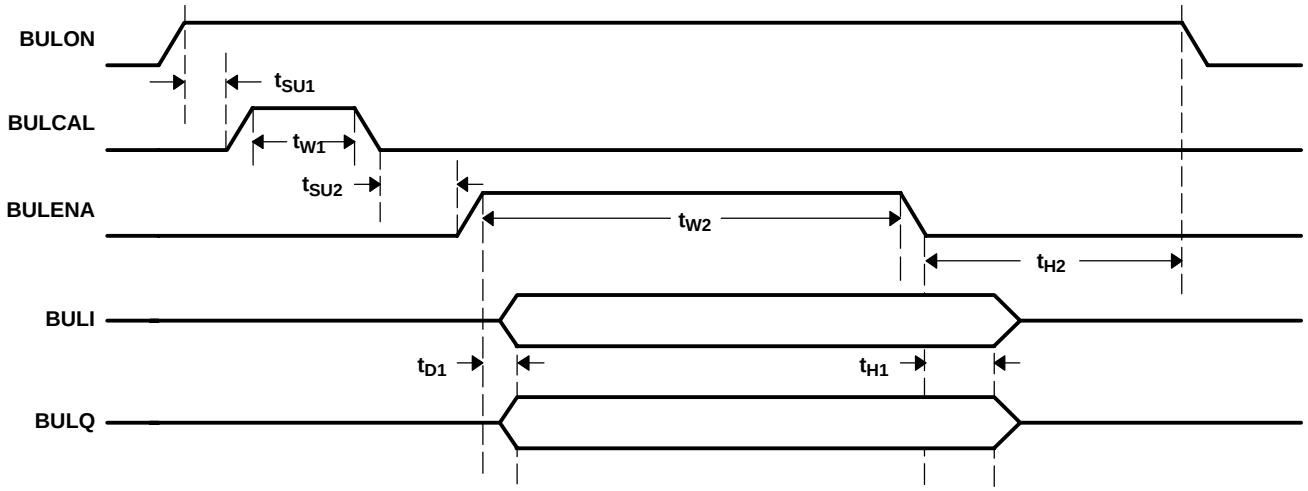
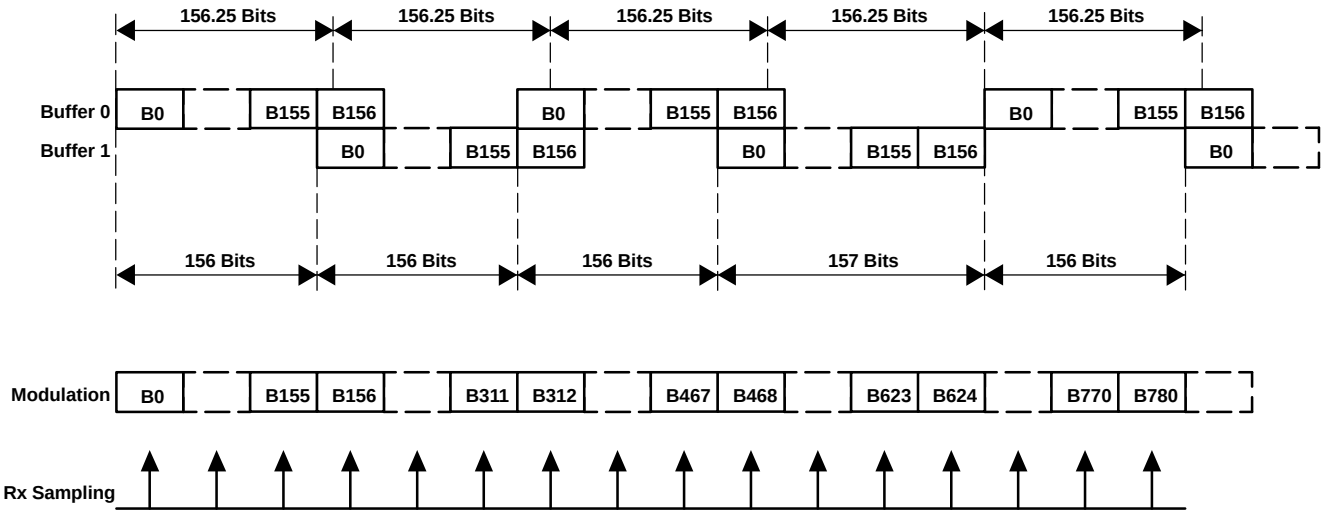


Figure 6−11. Baseband Uplink Timing



NOTE: B0 and B156 are guard bits

Figure 6−12. Multislot Modulation Scheme

6.16.2.2 Baseband Downlink Path

dc characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic range on each input			BBVREF		V_{PP}
Differential input dynamic range	BDLIP − BDLIM or BDLQP − BDLQM		2 BBVREF		V_{PP}
Differential input resistance	BDLIP − BDLIM or BDLQP − BDLQM	130	200	270	kΩ
Differential input capacitance	BDLIP − BDLIM or BDLQP − BDLQM		4		pF
Single-ended input resistance to ground	BDLIP or BDLIM or BDLQP or BDLQM	50	110	150	kΩ
Single-ended input capacitance to ground			8		pF
External input common mode voltage		0.8	VRABB/2	VRABB − 0.8	V
Range of digital ouput data samples		−32768		+32767	
Offset error after calibration	Internal calibration	−25		25	LSB†
	External calibration	−25		25	
I and Q input states in power down			High Z		

† The LSB corresponds to the one of the ADC which is specified as 82-dB dynamic range, which means 13.3 bits, but the output data bits are transmitted through the BSP in a 16-bit word format. The decimation ratio of 24 (6.5 MHz/270 kHz) makes the maximum code on a 16-bit word to be 32767 which corresponds to −3.07 dBm0.

‡ External offset correction range is limited by: output code (external offset + signal) < 32767.

ac characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain matching between channels	Measured on 18 kHz	−0.5	0.0	0.5	dB
Delay matching between channels	Sine wave	−16	0.0	16	ns
Frequency response of the total downlink path with values related to 18 kHz	800 Hz	0.0		0.35	dB
	18 kHz (Reference)		0.0		
	35 kHz	−0.40		0.25	
	59 kHz	−0.40		0.30	
	68 kHz	−0.70		0.30	
	81 kHz	−3.0		0.0	
	97 kHz	−6.0		−3.0	
	110 kHz			−8.0	
	120 kHz			−15.0	
	135 kHz			−35	
	200 kHz			−45	
	>200 kHz			−45	
Signal-to-noise ratio on 100-kHz bandwidth	−50 dBm0	32			dB
	−40 dBm0	42			
	−30 dBm0	52			
	−20 dBm0	62			
	−10 dBm0	72			
	−6 dBm0	72			
Idle channel noise 0 to 100 kHz				−82	dBm0
Gain tracking error at 18 kHz with reference at −10 dBm	−6 dBm0	−0.25		0.25	dB
	−10 dBm0 (Reference)		0		
	−20 dBm0	−0.25		0.25	
	−30 dBm0	−0.25		0.25	
	−40 dBm0	−0.25		0.25	
	−50 dBm0	−0.50		0.50	
Group delay	0 Hz to 100 kHz		28		µs

Timing characteristics: these values are given for system information only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{SU3}	Setup time, BDLON ↑ to BDLCAL ↑		5			µs
t_{W3}	Pulse duration BDLCAL high		60			µs
t_{SU4}	Setup time, BDLCAL ↓ to BDLENA ↑		3.7			µs
t_{W4}	Pulse duration BDLENA high	N effective duration of burst		N		1/4-bit†
t_{D2}	Setup time after BDLENA ↑ before DATA valid				32.7	µs
t_{H3}	Hold time DATA valid after BDLENA ↓				3.7	µs
t_{H4}	Hold time BDLON high after BDLENA ↓		3.7			µs

† Bit is relative to GSM bit = 1/270.833 kHz.

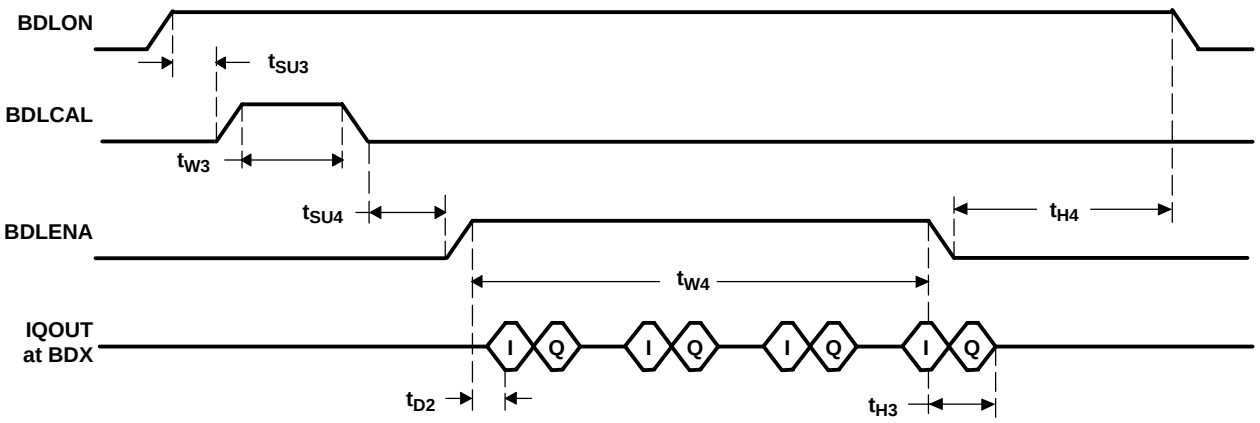


Figure 6−13. Baseband Downlink Timing

6.16.3 Auxiliary DAC

6.16.3.1 10-Bit DAC Characteristics

The recommended load on the DAC terminal is a 50-pF (maximum value) capacitor in parallel with a 10-kΩ (minimum value) resistor.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC resolution			10		bit
Integral nonlinearity	Best fitting line	−1		1	LSB
Differential nonlinearity		−1		1	LSB
Settling time			10		µs
Output voltage with code maximum		2.0	2.2	2.4	V
Output voltage with code minimum		0.18	0.24	0.3	V
Output voltage in power down				50	mV
Output impedance in power down				200	Ω
DC power supply sensitivity			1		%

6.16.4 Automatic Frequency Control

6.16.4.1 AFC DAC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC resolution			13		bit
Sampling frequency	AFCCTLADD reg = 00		2.165		MHz
	AFCCTLADD reg = 01		1.08		MHz
	AFCCTLADD reg = 10		541		kHz
	AFCCTLADD reg = 11		270		kHz
LSB value		250		340	µV
Integral nonlinearity	(0 to 75% range)	−5		5	LSB
Differential nonlinearity	(0 to 75% range)	−1		1	LSB
Settling time			100		µs
DC power supply sensitivity			1		%

6.16.4.2 AFC Output Stage

The recommended load on the AFC terminal is a 33-nF capacitor in parallel with a 25-kΩ resistor.

PARAMETER	MIN	TYP	MAX	UNITS
Output voltage at code minimum			45	mV
Output voltage at code maximum	2.0	2.3	2.8	V
Output voltage in power down			50	mV
Output resistance	15	22.5	31	kΩ

6.16.5 LED Outputs

6.16.5.1 Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LEDA maximum voltage				VBAT	V
LEDB maximum voltage				VBAT	V
LEDC maximum voltage				VCHG	V
LEDA driven current	Current sink			10	mA
LEDB driven current	Current sink			150	mA
LEDC driven current	Current sink			10	mA
LEDA drop	ILEDA = −10 mA, measure vs GNDL, LED A ON			400	mV
LEDB drop	ILEDB = −150 mA, measure vs GNDL, LED B ON			700	mV
LEDC drop	ILEDC = −10 mA, measure vs GNDL, LED C ON			400	mV

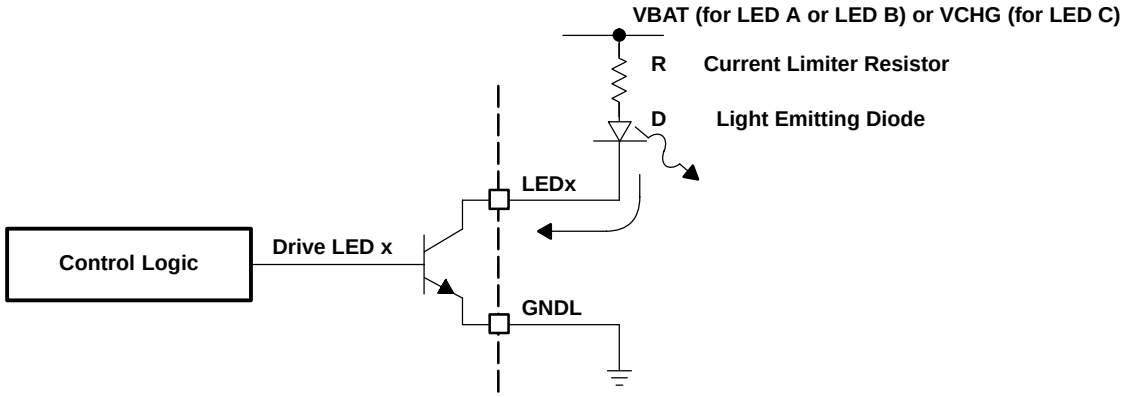


Figure 6−14. LED Schematic

6.17 ESD Performance

The TWL3025 device meets Texas Instruments standard requirements relative to the electrostatic discharge (ESD) sensitivity.

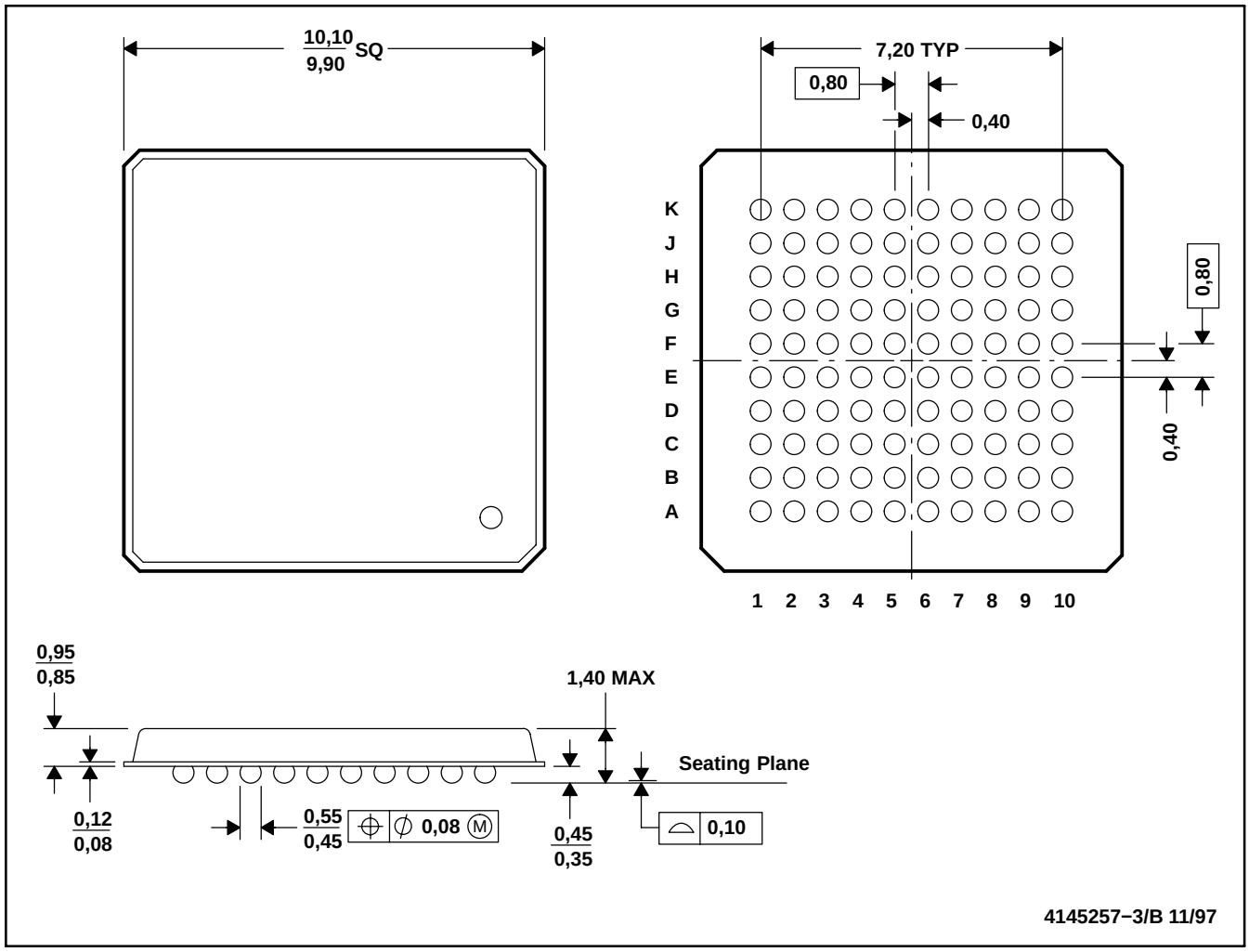
The following list details the TWL3025 ESD performance relative to TI requirements:

ESD METHOD	STANDARD REFERENCE	TWL3025 PERFORMANCE	TI STANDARD REQUIREMENTS
Human body model	EIA/JEDEC22−A114−A	2000 V	2000 V
Machine model	EIA/JEDEC22−A115−A	100 V	100 V
Charge device model	EIA/JEDEC22−C101−A	750 V	750 V

7 Mechanical Information

The TWL3025 device is packaged in a 100-terminal GGM package or a 143-terminal GQW package. The following shows the mechanical dimensions for the GGM and GQW packages.

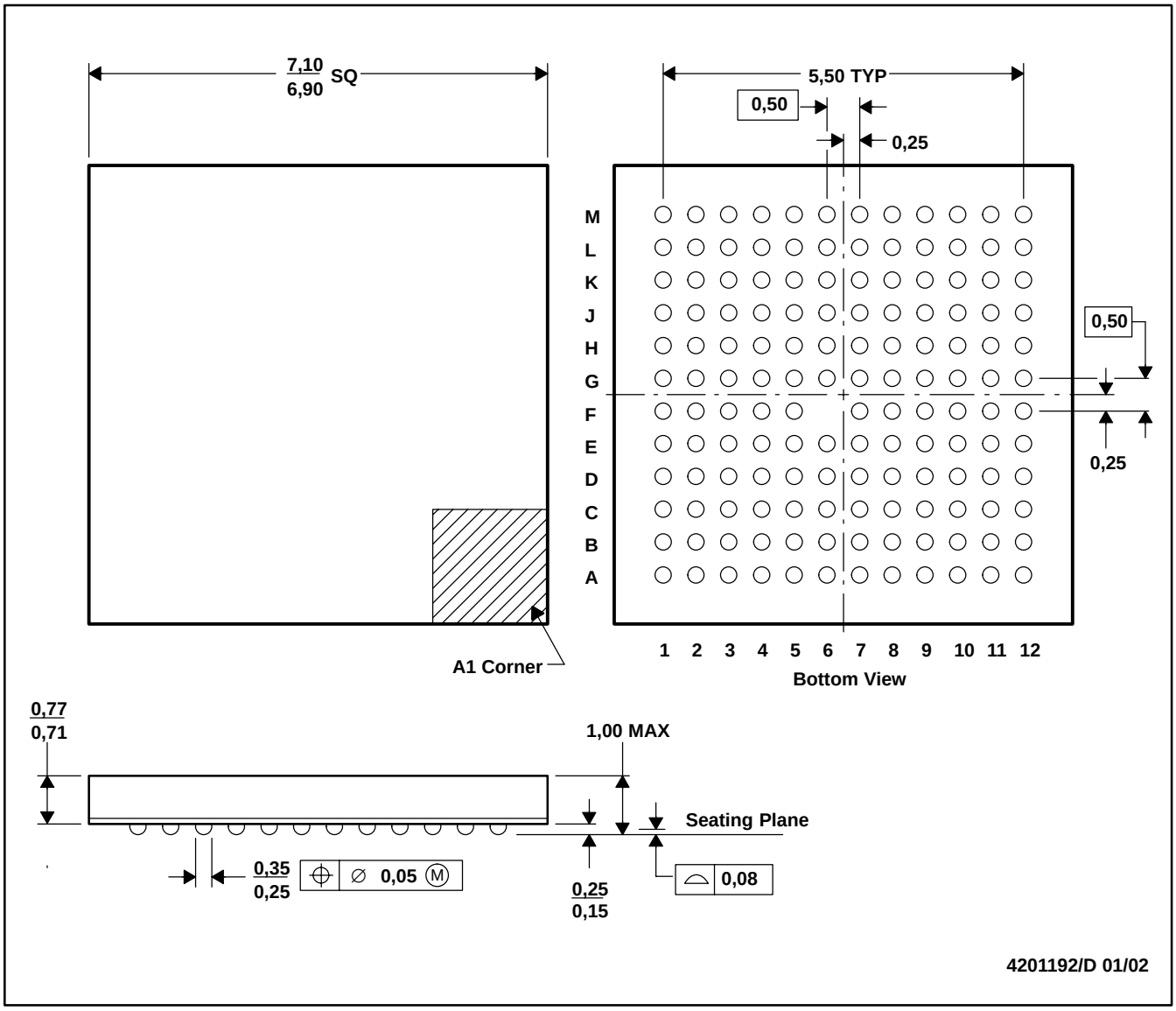
GGM (S-PBGA-N100) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments.

GQW (S-PBGA-N143) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.