HERCROM200G2c035

Design modifications

F751988 versus F751619

CAL023c

V1.0

CALYPSO

	Originator
Name	Benoit Drevet
Date	Feb-18-2002
Signature	

HISTORY

Version	Date	Author	Approval manager	Approval date	Notes
1.0	July - 11 - 2002	Rodolphe Servato	Michel Gac	July – 12 -2002	1

Notes:

1. Creation of the document.
2.

SUMMARY

1. REFERENCE DOCUMENTS

Teamtrack database: H/W bug entry / Calypso

2. INTRODUCTION

This document describes the functional modifications introduced in the HERCROM200G2 device processed in C035 technology versus the HERCROM400G2 device processed in c035 technology.
The modifications listed hereafter are only related to the hardware implementation and doesn't include changes in the DSP ROM code.
These modifications are corresponding to both design bug corrections and functional improvements.

3. MODULES

3.1 Internal RAM

HERCROM400G2 is a 2Mb internal RAM chip including 2 MVYE3276803232 instances

3.2 MPU

MPU granularity has been downsized to fit 2Mb RAM

3.3 Memory Interface

The following registers have been modified. Bit(12) has been added for test purpose. In functional mode, the reset value must not be modified.

nCSx memory range (Read/Write) register – FFFF:FBXX

Bit	Name	Function	Reset (dec)
4:0	WS	number of wait state for nCS0 memory access	31
6:5	DVS	Device data size: 00 = 8-bit, 01 = 16-bit, 10 = 32-bit	01
7	WE	0 = ABORT when write operation on a nCS0 1= Write enable	0
8	-	*Reserved*	0
9:11	DC	Dummy Cycles that should be inserted while bank switching from nCS0 to a faster memory bank.	7
12	reserved	Test purpose	1

4. CHIP LEVEL

4.1 Identification codes

Description:
New part number for the JTAG identification code: Device-ID is now B4FB.
Device-Ver = 000

Notes: new JTAG Id generated automatically by Hawkeye tool.