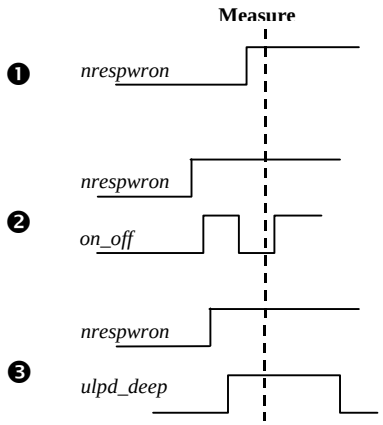
CALYPSO with NAUSICA: Pin status after RESPWRON, in OFF Mode DeepSleep MODE

Ball	PW Domain	PAD	PAD_name	❶ Reset (nrespwron)	❷ Off Mode	❸ Deep sleep mode
B2		IO	RnW	1	1	/
C2		O	nCS0	1	1	/
C3		O	nCS1	1	1	/
B1*		PWR	VSS			
C1		O	nCS2	1	1	/
D3		IO	nCS3	1	1	/
D2		IO	CS4	0	0	/
D1		PWR	VDDSHV1			
F5		IO	nBHE	0	0	/
E4		IO	nBLE	0	0	/
E2		O	nFOE	1	1	/
E3		IO	nFWE	1	1	/
E1		PWR	VDD			
F4		IO	FDP	0	0	/
F3		O	ADD_15_0(0)	0	0	/
F2		O	ADD_15_0(1)	0	0	/
F1		PWR	VSS			
G5		O	ADD_15_0(2)	0	0	/
4		O	ADD_15_0(3)	0	0	/
G2	VDDS-MIF	O	ADD_15_0(4)	0	0	/
G3		O	ADD_15_0(5)	0	0	/
G1		PWR	VDDSHV1			
H1		O	ADD_15_0(6)	0	0	/
H3		O	ADD_15_0(7)	0	0	/
H2		O	ADD_15_0(8)	0	0	/
H4		O	ADD_15_0(9)	0	0	/
H5		O	ADD_15_0(10)	0	0	/
J1		O	ADD_15_0(11)	0	0	/
J2		O	ADD_15_0(12)	0	0	/
J3		O	ADD_15_0(13)	0	0	/
J4		O	ADD_15_0(14)	0	0	/
K1		PWR	VSS			
K3		O	ADD_15_0(15)	0	0	/
K2		IO	ADD_20_16(16)	0	0	/
K4		IO	ADD_20_16(17)	0	0	/
J5		IO	ADD_20_16(18)	0	0	/
L1		IO	ADD_20_16(19)	0	0	/
L2		IO	ADD_20_16(20)	0	0	/
L3		O	ADD_21	0	0	/

Legend:
/ : Same state
-- : No effects



M1	VDDS-1	PWR	VDD			
N1*		I	nIBOOT	Input	Input	Input
M3		I	EXT_IRQ	Input	Input	Input
M2		I	IDDQ	Input	Input	Input
P1*		I	EXT_FIQ	Input	Input	Input
N2		IO	nRESET_OUT	0	0	/
P2*		PWR	VSS			
N3		IO	IO(0)	Input	Input	/
P3		IO	IO(1)	Input	Input	/
L4		IO	IO(2)	Input	Input	/
M4		IO	IO(3)	Input	Input	/
N4		IO	KBC(0)	1	1	/
P4		PWR	VSS			
K5		IO	KBC(1)	1	1	/
L5		IO	KBC(2)	1	1	/
N5		PWR	VDDSHV2			
P5		IO	KBC(3)	1	1	/
M5		IO	KBC(4)	1	1	/
K6		IO	KBR(0)	Input	Input	/
M6		IO	KBR(1)	Input	Input	/
P6		IO	KBR(2)	Input	Input	/
N6		IO	KBR(3)	Input	Input	/
L6		IO	KBR(4)	Input	Input	/
K7		O	BU	0	0	/
L7		O	LT	0	0	/
P7		PWR	VDD			
N7		I	MCUDI	Input	Input	Input
M7		O	MCUDO	0	0	/
M8		IO	MCUEN(0)	1	1	/
N8		PWR	VSS			
P8		IO	MCUEN(1)	1	1	/
L8		IO	MCUEN(2)	1	1	/
K8		O	SDO	0	0	/
L9		O	nSCS0	1	1	/
N9		O	nSCS1	1	1	/
P9		O	SCLK	0	0	/
M9		IO	SDI	Input	Input	/
K9		IO	MCSI_FSYNCH	Input	Input	/
M10		IO	MCSI_RXD	Input	Input	/
P10		PWR	VSS			
N10		IO	MCSI_CLK	Input	Input	/
L10		IO	MCSI_TXD	0	0	/
K10		I	BDR	Input	Input	Input
P11		I	BCLKR	Input	Input	Input
N11		IO	BCLKX	Input	Input	/
M11		O	BDX	0	0	/
L11		I	BFSR	Input	Input	Input

P12		IO	BFSX	0	0	/
N12		I	VCLKRX	Input	Input	Input
P13*		PWR	VSS			
N13		I	VDR	Input	Input	Input
P14*		O	VDX	0	0	/
M13		I	VFSRX	Input	Input	Input
M12		IO	TSPACT_4_0(0)	0	0	/
N14*		PWR	VDD			
M14		IO	TSPACT_4_0(1)	0	0	/
L12		IO	TSPACT_4_0(2)	0	0	/
L13		IO	TSPACT_4_0(3)	0	0	/
L14		PWR	VDDSHV2			
J10		IO	TSPACT_4_0(4)	0	0	/
K11		O	TSPACT_12_5(5)	0	0	/
K13		O	TSPACT_12_5(6)	0	0	/
K12		O	TSPACT_12_5(7)	0	0	/
K14		O	TSPACT_12_5(8)	0	0	/
J11		O	TSPACT_12_5(9)	0	0	/
J12		O	TSPACT_12_5(10)	0	0	/
J13		O	TSPACT_12_5(11)	0	0	/
J14		O	TSPCLKX	0	0	/
H10		IO	TSPDI	Input	Input	/
H11		IO	TSPDO	0	0	/
H13		O	TSPEN_0	1	1*	/
H12		IO	TSPEN_3_1(1)	1	1*	/
H14		IO	TSPEN_3_1(2)	0	0*	/
G14		PWR	VSS			
G12		IO	TSPEN_3_1(3)	1	1*	/
G13		IO	SIM_IO	0	0	/
G11		IO	SIM_CD	Input	Input	/
G10		IO	SIM_RST	0	0	/
F14		IO	SIM_PWRCTRL	0	0	/
F13		IO	SIM_CLK	0	0	/
F12		IO	CLK13M_OUT	0	0	0
F11	VDDS-RTC	PWR	VDD1			
E14		PWR	VSS1			
E12		PWR	VSSA			
E13		I	CLKTCXO	Input	Input	Input
E11		PWR	VDDAHV			
F10		I	ON_OFF	Input	Input	Input
D14		PWR	VDD2			
D13		PWR	VDDSHV3			
D12		I	nRESPWRON	Input	Input	Input
C14		PWR	VSS2			
B14*		O	IT_WAKEUP	0	0	/
C12		O	CLK32K_OUT	0	0	--
C13		I	OSC32K_IN	Input	Input	Input

***from Calypso C035-F751619**

1	/	/
1	/	/
0	/	/

1	/	/

A14*		**PWR**	**VSSO**			
B13		I	OSC32K_OUT	Input	Input	Input
A13*		O	RFEN	0	0	/
B12		**PWR**	**VDD**			
A12		O	TCXOEN	0	0	/
D11		I	nBSCAN	Input	Input	Input
C11		**PWR**	xxxAVAILABLExxx			
B11		IO	nEMU0	Input	Input	/
A11		**PWR**	**VDDSHV4**			
E10		IO	nEMU1	Input	Input	/
D10		I	TDI	Input	Input	Input
B10		I	TCK	Input	Input	Input
A10		**PWR**	**VSS**			
C10	VDDS-2	O	TDO	Input	Input	/
E9		I	TMS	Input	Input	Input
C9		IO	CTS_MODEM	Input	Input	/
A9		IO	***RX_MODEM***	Input	Input	/
B9		O	***TX_MODEM***	1	1	/
D9		IO	DSR_MODEM	Input	Input	/
E8		O	RTS_MODEM	1	1	/
D8		I	RX_IRDA	Input	Input	Input
A8		IO	RXIR_IRDA	Input	Input	/
B8		O	SD_IRDA	1	1	/
C8		IO	TX_IRDA	1	1	/
C7		IO	TXIR_IRDA	1	1	/
B7		IO	DATA(0)	Input	Input	/
A7		**PWR**	**VSS**			
D7		IO	DATA(1)	Input	Input	/
E7		IO	DATA(2)	Input	Input	/
D6		IO	DATA(3)	Input	Input	/
B6		**PWR**	**VDDSHV1**			
A6		IO	DATA(4)	Input	Input	/
C6		IO	DATA(5)	Input	Input	/
E6		IO	DATA(6)	Input	Input	/
C5		IO	DATA(7)	Input	Input	/
A5	VDDS-MIF	**PWR**	**VDD**			
B5		IO	DATA(8)	Input	Input	/
D5		IO	DATA(9)	Input	Input	/
E5		IO	DATA(10)	Input	Input	/
A4		**PWR**	**VDDSHV1**			
B4		IO	DATA(11)	Input	Input	/
C4		IO	DATA(12)	Input	Input	/
D4		IO	DATA(13)	Input	Input	/
A3		IO	DATA(14)	Input	Input	/
B3		IO	DATA(15)	Input	Input	/
A2*		**PWR**	**VSS**			

CALYPSO with IOTA: Pin status after RESPWRON, in OFF Mode DeepSleep MODE

Ball	PW Domain	PAD	PAD_name	Reset (respwron)	Off Mode	Deep sleep mode
B2		IO	RnW			/
C2		O	nCS0			/
C3		O	nCS1			/
B1*		PWR	VSS			
C1		O	nCS2			/
D3		IO	nCS3			/
D2		IO	CS4			/
D1		PWR	VDDSHV1			
F5		IO	nBHE			/
E4		IO	nBLE			/
E2		O	nFOE			/
E3		IO	nFWE			/
E1		PWR	VDD			
F4		IO	FDP			/
F3		O	ADD_15_0(0)			/
F2		O	ADD_15_0(1)			/
F1		PWR	VSS			
G5		O	ADD_15_0(2)			/
G4		O	ADD_15_0(3)			/
G2	VDDS-MIF	O	ADD_15_0(4)			/
G3		O	ADD_15_0(5)			/
G1		PWR	VDDSHV1			
H1		O	ADD_15_0(6)			/
H3		O	ADD_15_0(7)			/
H2		O	ADD_15_0(8)			/
H4		O	ADD_15_0(9)			/
H5		O	ADD_15_0(10)			/
J1		O	ADD_15_0(11)			/
J2		O	ADD_15_0(12)			/
J3		O	ADD_15_0(13)			/
J4		O	ADD_15_0(14)			/
K1		PWR	VSS			
K3		O	ADD_15_0(15)			/
K2		IO	ADD_20_16(16)			/
K4		IO	ADD_20_16(17)			/
J5		IO	ADD_20_16(18)			/
L1		IO	ADD_20_16(19)			/
L2		IO	ADD_20_16(20)			/
L3		O	ADD_21			/

M1	VDDS-1	PWR	VDD			
N1*		I	nIBOOT			Input
M3		I	EXT_IRQ			Input
M2		I	IDDQ			Input
P1*		I	EXT_FIQ			Input
N2		IO	nRESET_OUT			/
P2*		PWR	VSS			
N3		IO	IO(0)			/
P3		IO	IO(1)			/
L4		IO	IO(2)			/
M4		IO	IO(3)			/
N4		IO	KBC(0)			/
P4		PWR	VSS			
K5		IO	KBC(1)			/
L5		IO	KBC(2)			/
N5		PWR	VDDSHV2			
P5		IO	KBC(3)			/
M5		IO	KBC(4)			/
K6		IO	KBR(0)			/
M6		IO	KBR(1)			/
P6		IO	KBR(2)			/
N6		IO	KBR(3)			/
L6		IO	KBR(4)			/
K7		O	BU			/
L7		O	LT			/
P7		PWR	VDD			
N7		I	MCUDI			Input
M7		O	MCUDO			/
M8		IO	MCUEN(0)			/
N8		PWR	VSS			
P8		IO	MCUEN(1)			/
L8		IO	MCUEN(2)			/
K8		O	SDO			/
L9		O	nSCS0			/
N9		O	nSCS1			/
P9		O	SCLK			/
M9		IO	SDI			/
K9		IO	MCSI_FSYNCH			/
M10		IO	MCSI_RXD			/
P10		PWR	VSS			
N10		IO	MCSI_CLK			/
L10		IO	MCSI_TXD			/
K10		I	BDR			Input
P11		I	BCLKR			Input
N11		IO	BCLKX			/
M11		O	BDX			/
L11		I	BFSR			Input

P12		IO	BFSX			/
N12		I	VCLKRX			Input
P13*		PWR	VSS			
N13		I	VDR			Input
P14*		O	VDX			/
M13		I	VFSRX			Input
M12		IO	TSPACT_4_0(0)			/
N14*		PWR	VDD			
M14		IO	TSPACT_4_0(1)			/
L12		IO	TSPACT_4_0(2)			/
L13		IO	TSPACT_4_0(3)			/
L14		PWR	VDDSHV2			
J10		IO	TSPACT_4_0(4)			/
K11		O	TSPACT_12_5(5)			/
K13		O	TSPACT_12_5(6)			/
K12		O	TSPACT_12_5(7)			/
K14		O	TSPACT_12_5(8)			/
J11		O	TSPACT_12_5(9)			/
J12		O	TSPACT_12_5(10)			/
J13		O	TSPACT_12_5(11)			/
J14		O	TSPCLKX			/
H10		IO	TSPDI			/
H11		IO	TSPDO			/
H13		O	TSPEN_0			/
H12		IO	TSPEN_3_1(1)			/
H14		IO	TSPEN_3_1(2)			/
G14		PWR	VSS			
G12		IO	TSPEN_3_1(3)			/
G13		IO	SIM_IO			/
G11		IO	SIM_CD			/
G10		IO	SIM_RST			/
F14		IO	SIM_PWRCTRL			/
F13		IO	SIM_CLK			/
F12		IO	CLK13M_OUT			0
F11	VDDS-RTC	PWR	VDD1			
E14		PWR	VSS1			
E12		PWR	VSSA			
E13		I	CLKTCXO			Input
E11		PWR	VDDAHV			
F10		I	ON_OFF	Input	Input	Input
D14		PWR	VDD2			
D13		PWR	VDDSHV3			
D12		I	nRESPWRON	Input	Input	Input
C14		PWR	VSS2			
B14*		O	IT_WAKEUP	0	0	/
C12		O	CLK32K_OUT	0	0	--
C13		I	OSC32K_IN	Input	Input	Input

A14*		PWR	VSSO			
B13		I	OSC32K_OUT	Input	Input	Input
A13*	VDDS-2	O	RFEN			/
B12		PWR	VDD			
A12		O	TCXOEN			/
D11		I	nBSCAN			Input
C11		PWR	xxxAVAILABLExxx			
B11		IO	nEMU0			/
A11		PWR	VDDSHV4			
E10		IO	nEMU1			/
D10		I	TDI			Input
B10		I	TCK			Input
A10		PWR	VSS			
C10		O	TDO			/
E9		I	TMS			Input
C9		IO	CTS_MODEM			/
A9		IO	***RX_MODEM***			/
B9		O	***TX_MODEM***			/
D9		IO	DSR_MODEM			/
E8		O	RTS_MODEM			/
D8		I	RX_IRDA			Input
A8		IO	RXIR_IRDA			/
B8		O	SD_IRDA			/
C8		IO	TX_IRDA			/
C7		IO	TXIR_IRDA			/
B7	VDDS-MIF	IO	DATA(0)			/
A7		PWR	VSS			
D7		IO	DATA(1)			/
E7		IO	DATA(2)			/
D6		IO	DATA(3)			/
B6		PWR	VDDSHV1			
A6		IO	DATA(4)			/
C6		IO	DATA(5)			/
E6		IO	DATA(6)			/
C5		IO	DATA(7)			/
A5		PWR	VDD			
B5		IO	DATA(8)			/
D5		IO	DATA(9)			/
E5		IO	DATA(10)			/
A4		PWR	VDDSHV1			
B4		IO	DATA(11)			/
C4		IO	DATA(12)			/
D4		IO	DATA(13)			/
A3		IO	DATA(14)			/
B3		IO	DATA(15)			/
A2*		PWR	VSS			