CALYPSO OVERVIEW

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Calypso General Description

- GPRS class 12 capability;
- Full-Rate, Enhanced Full-Rate and Half-Rate speech coding capability
- 2 Processor Cores:

  ARM7TDMIE: 0~39MHz

  DSP TMS320C54x: 0~91MHz
- 179-PIN

Calypso ARM Block Overview (1)

- General purpose peripherals:
  - 4 M-bit (512K-byte) SRAM
  - ARM Memory Interface for External RAM & Flash
  - MPU (Memory Protection Unit):512K-byte for 4 regions
  - Debug Unit (DU)

Calypso ARM Block Overview (2)

- Application peripherals:
  - GPIO: Keyboard & 2 PWM (Light, Buzzer)
  - UWIRE(3.25MHz)/I2C(100/400KHz): LCD/EPROM
  - 3 Timers: 2 General, 1 Watchdog
  - UART_IRDA: Debug (Max 115.2k baudrate)
  - UART_MODEM: (Max 115.2k baudrate)
  - SIM Interface: 3V, Static SIM
  - INTH: ARM Interrupts Handler: (21 INTs)
  - TPU: Real-time Sequencer
  - TSP: Control ABB & RF (6.5MHz)

Calypso ARM Block Overview (3)

- DMA controller
- RTC: Real Time Clock
- ULPD: Ultra Low-Power Device for Deep Sleep Mode management
- CLKM: CLK, Sleep-Mode Control
- LPG: Blinking LED
- PWT: Enhanced tone generator for Buzzer (349~5276Hz)
- PWL: LCD Backlight (32KHz)
- SPI: Serial Port Interface (Max. 13MHz)
- GEA: GPRS Encryption Algorithm module

Calypso DSP Block Overview

- 28Kw RAM & 128Kw ROM
- RIF: Radio interface (13MHz)
- MCSI: Multi-Channel (x16) Serial Interface
- CRYPT: A51/A52 ciphering
- INTH: DSP interrupts Handler (x21)
- SPI: Speech Signal Flow between ABB

Calypso - Block Diagram

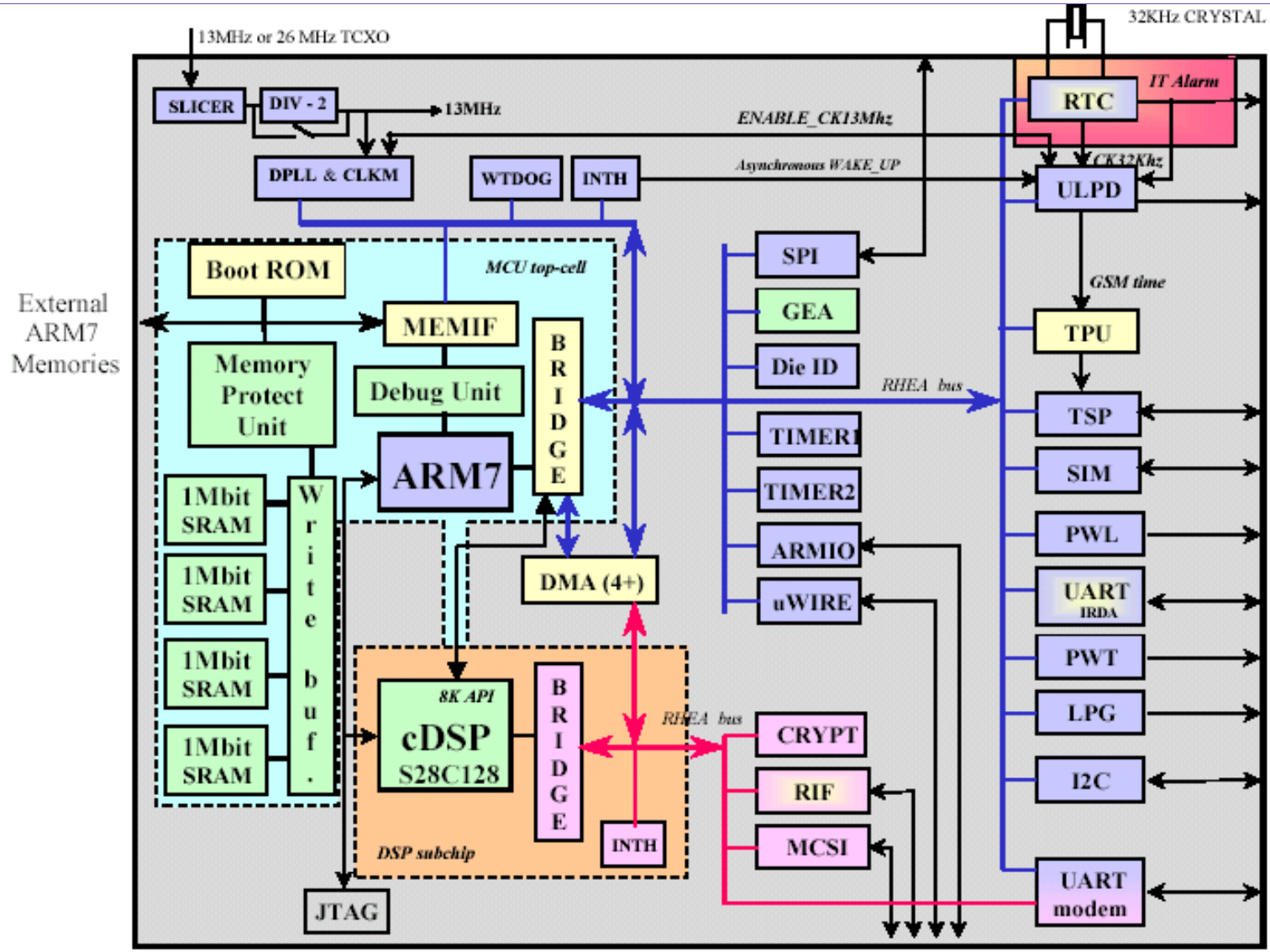
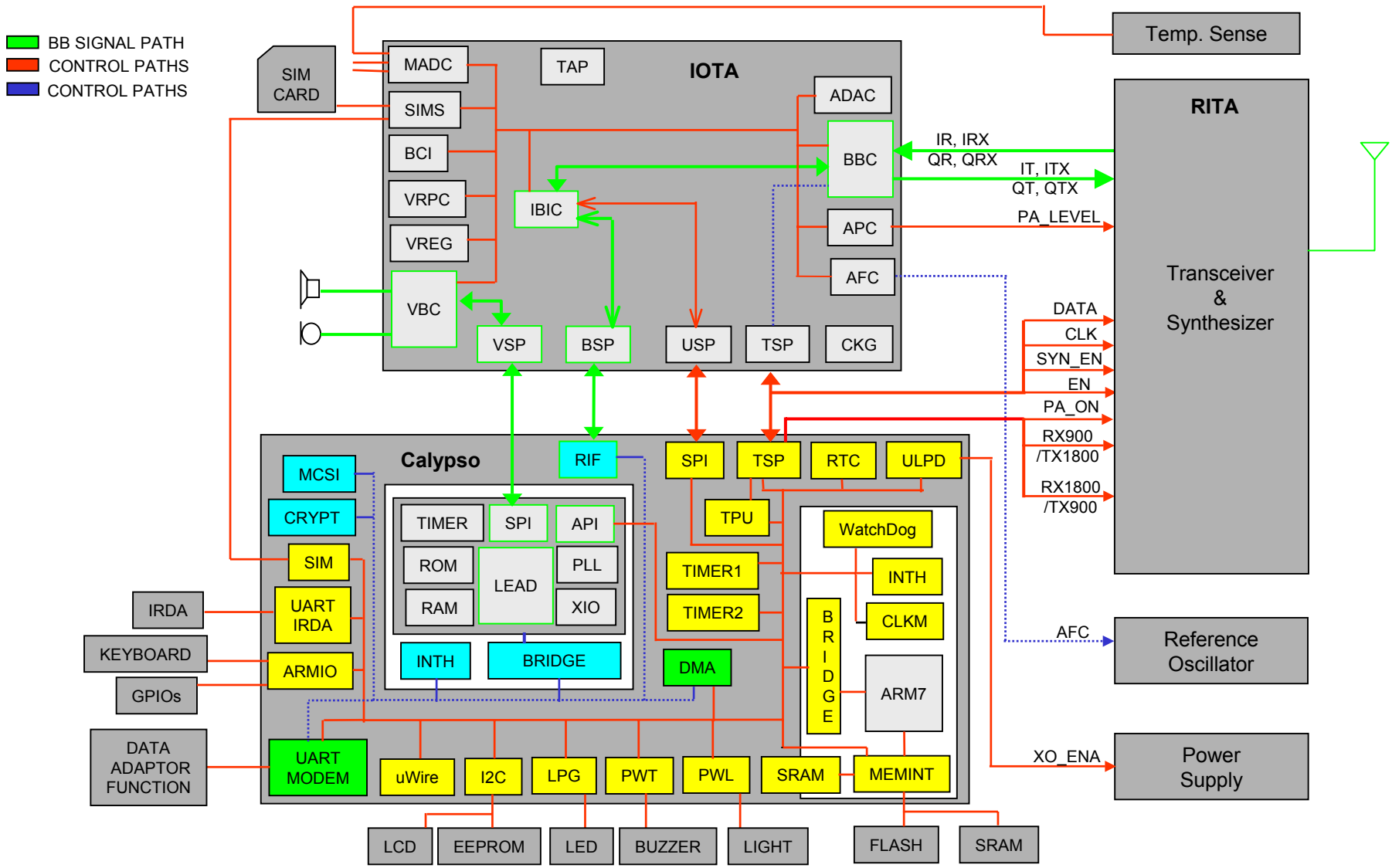


Figure 1: CALYPSO internal architecture

Calypso - MS Signal Flow



Memory Interface

Calypso - ARM memory interface function

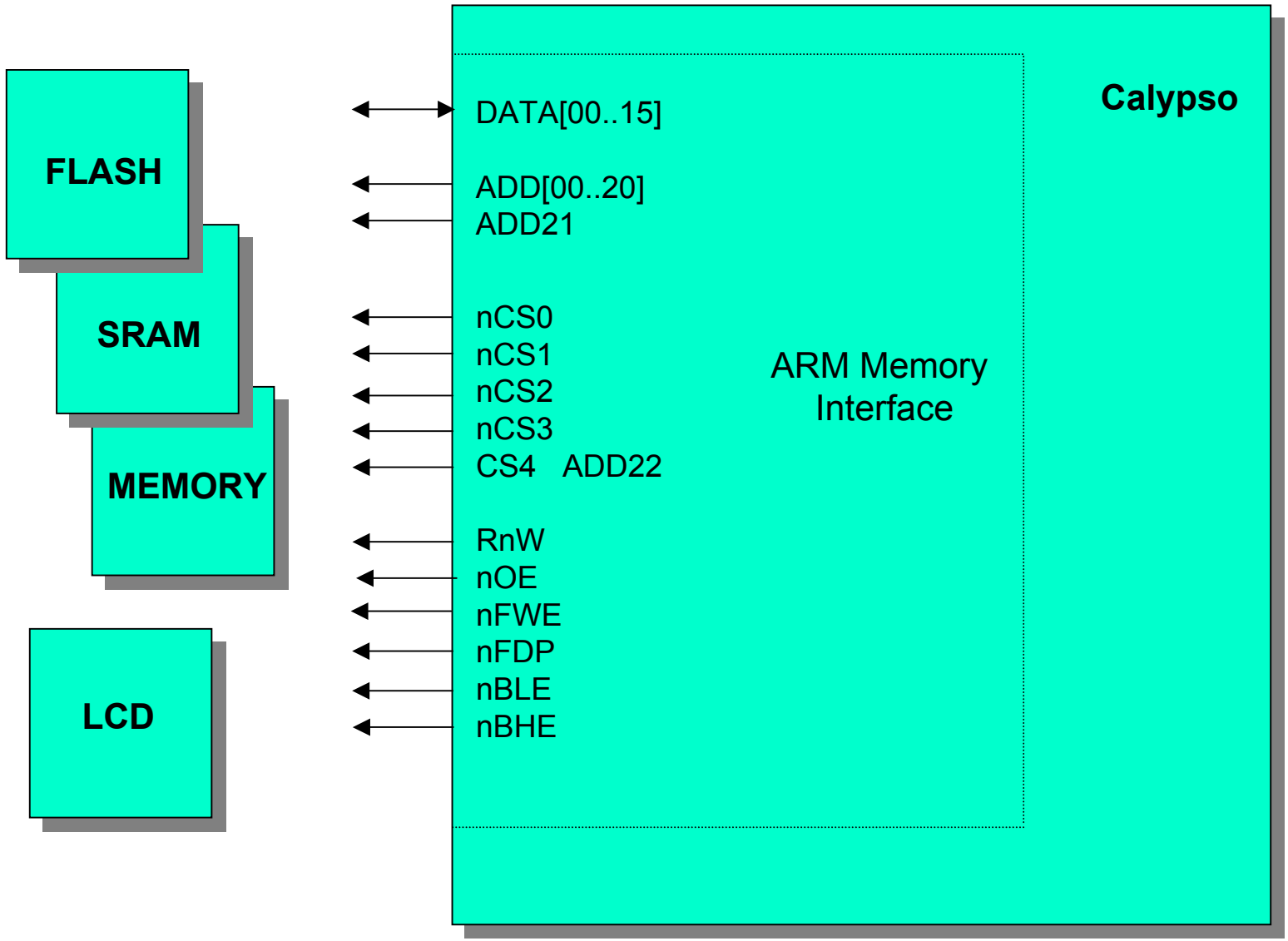
- **External Arm memory access management**:
  - ⇒Access Size from 8-bit up to 32-bit
  - ⇒Enable the connection of slow device (wait state insertion)
  - ⇒Memory control signal (chip-select, write strobe generation)

- **Arm to API memory access management**:
  - ⇒Support 16-bit and 32-bit API read and write access

- **Arm to Rhea bridge access management**:
  - ⇒Access size adaptation for RHEA access

- **Arm nWAIT and access control flags generation(byte-latch, etc...).**

Calypso - MEMINT : Pins Description



Interrupt Handler

Calypso - ARM Interrupt Handler

- Provides up to 21 prioritized and maskable interrupt to the ARM core.
- low level or edge sensitive selectable
- Flexible routing to FIQ or IRQ of ARM
- 3+ N*2 cycles latency(N interrupt)

Calypso - INTH ‘s registers summary

Register	Address	Access	HW Reset value
IT_REG1	FFFF:FA00	16 bits R	0000 0000 0000 0000
IT_REG2	FFFF:FA02	4 bits R	???? ???? ???0 0000
MASK_IT_REG1	FFFF:FA08	16 bits R/W	1111 1111 1111 1111
MASK_IT_REG2	FFFF:FA0A	4 bits R/W	1111 1111 1111 1111
SRC_IRQ_BIN_REG	FFFF:FA10	5bits R	???? ???? ???0 0000
SRC_FIQ_BIN_REG	FFFF:FA12	5bits R	???? ???? ???0 0000
INT_CTRL_REG	FFFF:FA14	2bits R/W	???? ???? ???? ??00
ILR_IRQ0_REG	FFFF:FA20	7 bits R/W	???? ???? ?000 0000
ILR_IRQ1_REG	FFFF:FA22	7 bits R/W	???? ???? ?000 0000
ILR_IRQ2_REG	FFFF:FA24	7 bits R/W	???? ???? ?000 0000
ILR_IRQ3_REG	FFFF:FA26	7 bits R/W	???? ???? ?000 0000
ILR_IRQ4_REG	FFFF:FA28	7 bits R/W	???? ???? ?000 0000
ILR_IRQ5_REG	FFFF:FA2A	7 bits R/W	???? ???? ?000 0000
ILR_IRQ6_REG	FFFF:FA2C	7 bits R/W	???? ???? ?000 0000
ILR_IRQ7_REG	FFFF:FA2E	7 bits R/W	???? ???? ?000 0000
ILR_IRQ8_REG	FFFF:FA30	7 bits R/W	???? ???? ?000 0000
ILR_IRQ9_REG	FFFF:FA32	7 bits R/W	???? ???? ?000 0000
ILR_IRQ10_REG	FFFF:FA34	7 bits R/W	???? ???? ?000 0000
ILR_IRQ11_REG	FFFF:FA36	7 bits R/W	???? ???? ?000 0000
ILR_IRQ12_REG	FFFF:FA38	7 bits R/W	???? ???? ?000 0000
ILR_IRQ13_REG	FFFF:FA3A	7 bits R/W	???? ???? ?000 0000
ILR_IRQ14_REG	FFFF:FA3C	7 bits R/W	???? ???? ?000 0000
ILR_IRQ15_REG	FFFF:FA3E	7 bits R/W	???? ???? ?000 0000
ILR_IRQ16_REG	FFFF:FA40	7 bits R/W	???? ???? ?000 0000
ILR_IRQ17_REG	FFFF:FA42	7 bits R/W	???? ???? ?000 0000
ILR_IRQ18_REG	FFFF:FA44	7 bits R/W	???? ???? ?000 0000
ILR_IRQ19_REG	FFFF:FA46	7 bits R/W	???? ???? ?000 0000
ILR_IRQ20_REG	FFFF:FA48	7 bits R/W	???? ???? ?000 0000

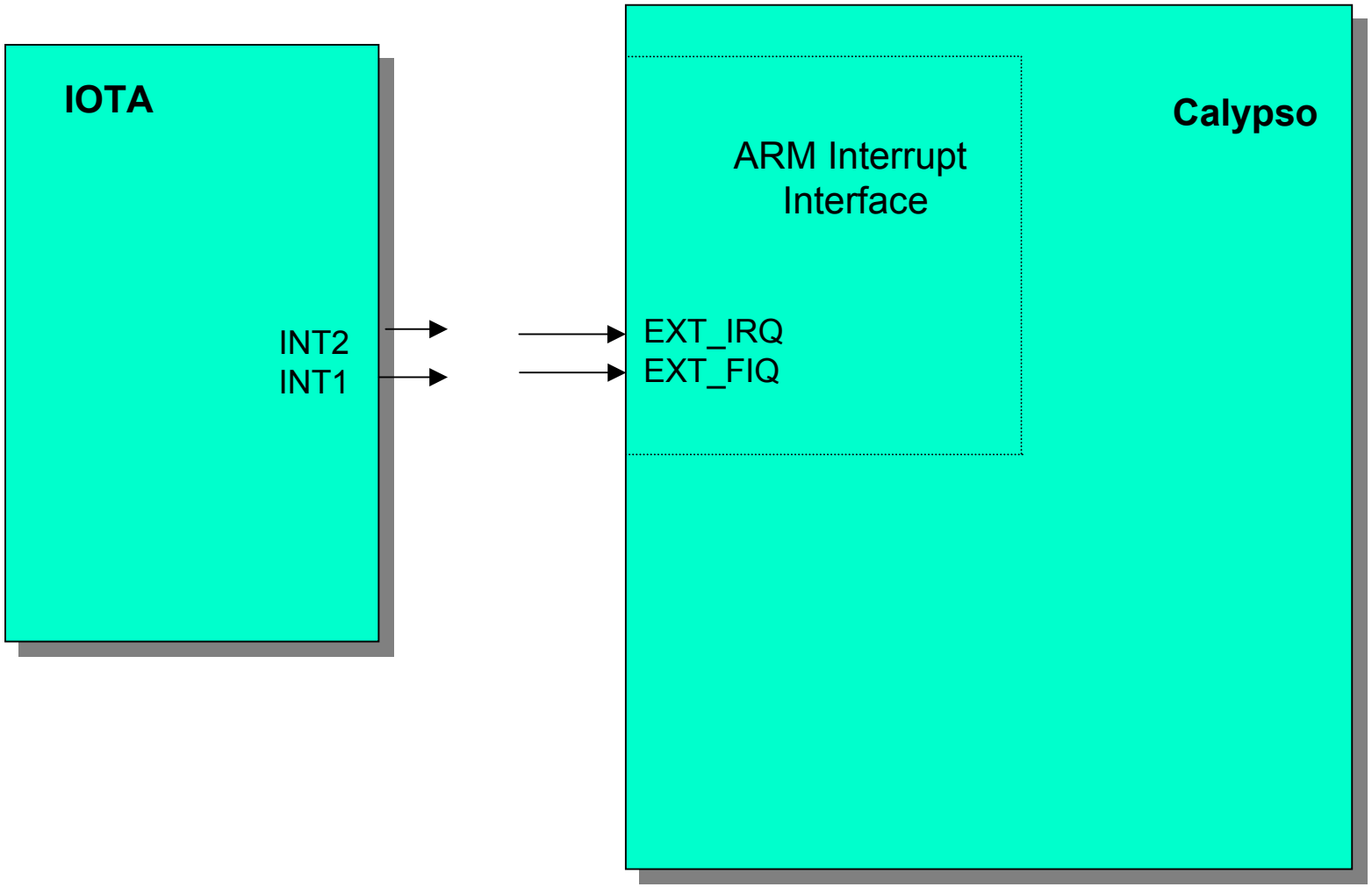
Calypso - ARM Interrupts

Name	Sense	IRQ	FIQ	Function
IRQ0	edge	✔		Watchdog TIMER interrupts
IRQ1	edge	✔		TIMER1 interrupt
IRQ2	edge	✔		TIMER2 interrupt
IRQ3			✔	TSP receives interrupt
IRQ4	edge	✔		TPU frame interrupt
IRQ5	edge	✔		TPU page interrupt
IRQ6	edge	✔		SIM interrupt 1. no answer to reset 2. character underflow 3. character overflow 4. character to transmit 5. received character 6. SIM card insertion/extraction
IRQ7	level	✔		UART_MODEM interrupts 1. error on receiver line 2. receive timeout 3. received character 4. character to transmit 5. modem status change 6. Received XOFF / special character detected 7. CTS/RTS deactivation 8. DSR/RxD activity detection (OFF mode only)
IRQ8	level	✔		Keyboard ***or*** JogDial interrupt
IRQ9	edge	✔		RTC periodical timer interrupt
IRQ10	level	✔		RTC ALARM ***or*** I2C data transfer error / completion

Calypso - ARM Interrupts

IRQ11	edge	✔		ULPD end of gauging interrupt
IRQ12	level	✔		External interrupt
IRQ13	edge	✔		SPI interrupt 1. received data 2. data to transmit
IRQ14	level	✔		DMA interrupt
IRQ15	edge	✔		API interrupts (nHINT)
IRQ16			✔	SIM card-detect fast interrupt
IRQ17			✔	Fast external interrupt
IRQ18	level	✔		UART_IRDA interrupts 1. error on receiver line 2. receive timeout 3. received character 4. character to transmit 5. modem status change 6. Received XOFF / special character detected 7. CTS/RTS deactivation
IRQ19	level	✔		ULPD GSM timer
IRQ20	level	✔		GEA interrupt

Calypso - Pins Description of ARM Interrupt Interface



Calypso - Clocks Generator and Control

CLKM

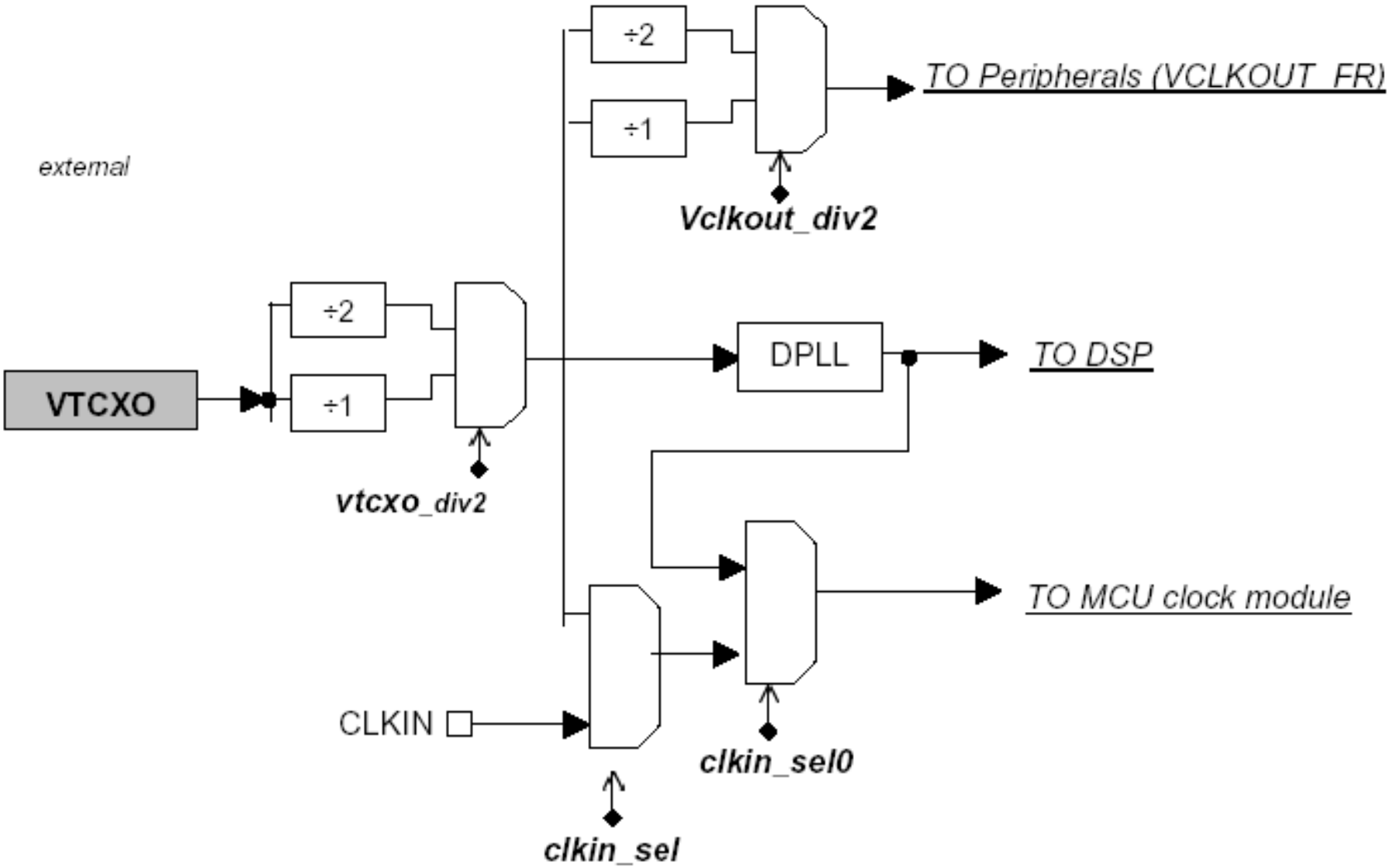
Calypso - CLKM : Features

- Generate and control clocks distribution to the ARM core, Lead core, internal and external peripherals.

- Control reset signals of ARM core, LEAD core, internal and external peripherals.

- Control deep power mode of external FLASH

Calypso - CLKM: Block Diagram

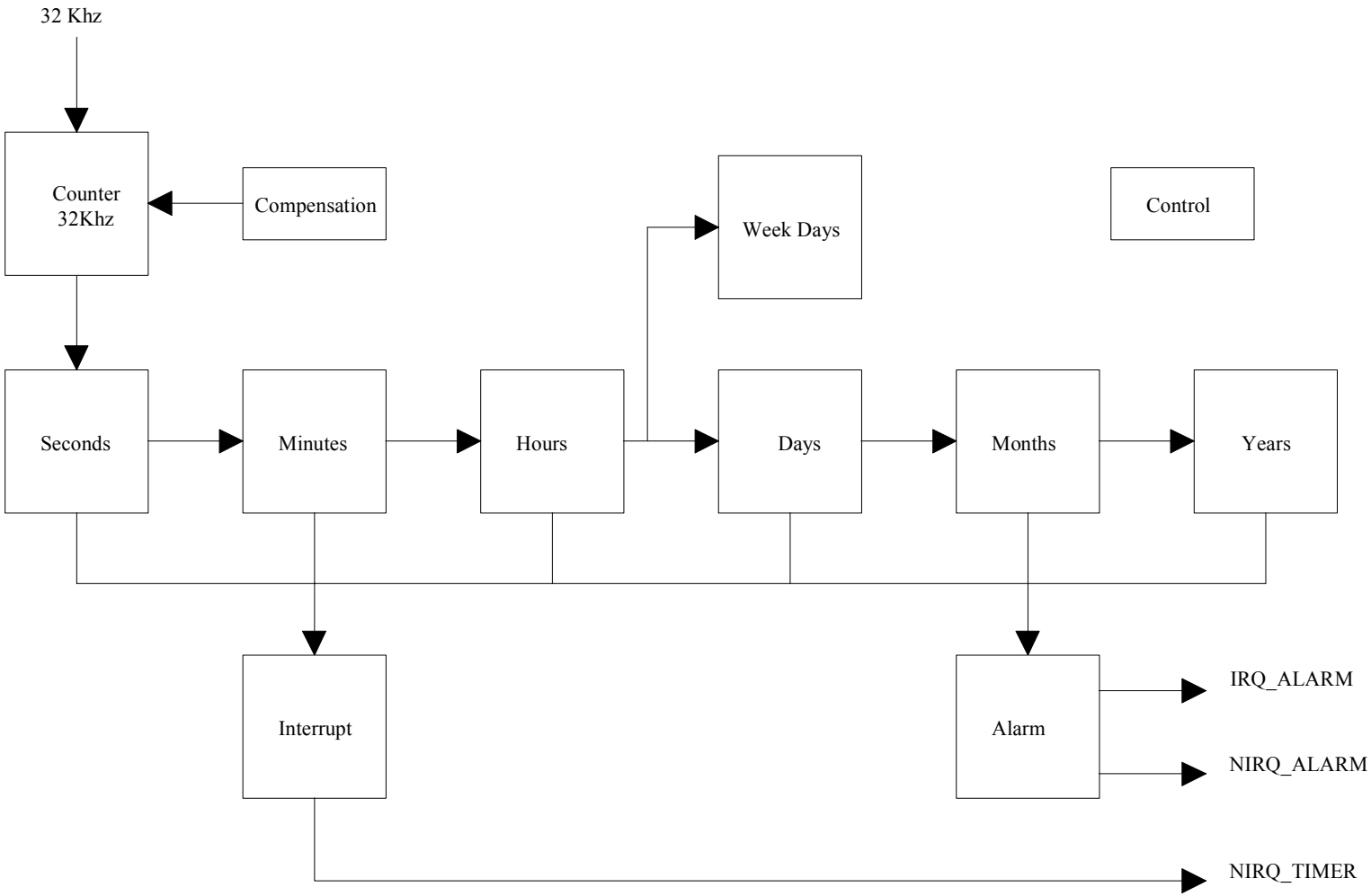


Real Time Clock

Calypso - RTC: Features

- Time information in BCD code
- Calendar Information in BCD code up to year 2099
- Interrupt generation
- 30s time correction
- oscillator frequency calibration

Calypso - RTC: Block Diagram



Calypso - ARM Interrupts (RTC)

IRQ0	IRQ	(edge)	WatchDog TIMER
IRQ1	IRQ	(edge)	TIMER1
IRQ2	IRQ	(edge)	TIMER2
IRQ3	FIQ	(level)	EXT_FIQ, TSP Rx, SIM card insertion/extraction
IRQ4	IRQ	(edge)	TPU frame
IRQ5	IRQ	(edge)	TPU page
IRQ6	IRQ	(edge)	SIM
IRQ7	IRQ	(level)	UART_MODEM or UART_IRDA
IRQ8	IRQ	(level)	Keyboard
IRQ9	IRQ	(edge)	RTC
IRQ10	IRQ	(level)	RTC Alarm, ULPD GSM timer, I2C
IRQ11	IRQ	(edge)	ULPD end of gauging
IRQ12	IRQ	(level)	EXT_IRQ
IRQ13	IRQ	(edge)	SPI
IRQ14	IRQ	(level)	DMA
IRQ15	IRQ	(edge)	API

ULPD Controller

Calypso - ULPD: Features

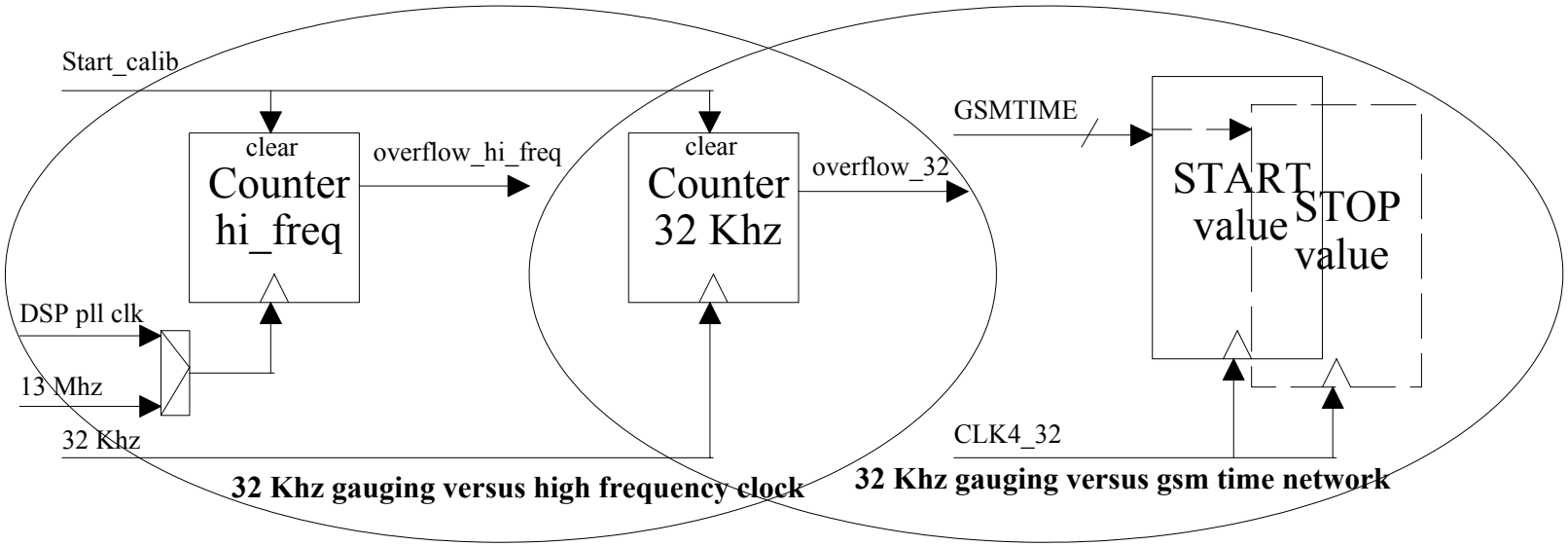
- Maintenance of the GSM time whatever the mobile activity mode (big sleep, deep sleep, switch off)

- Perform the power on/off and off/on of the chip

- Gauging of an external quartz based oscillator (32kHz) to keep the time accuracy during sleep

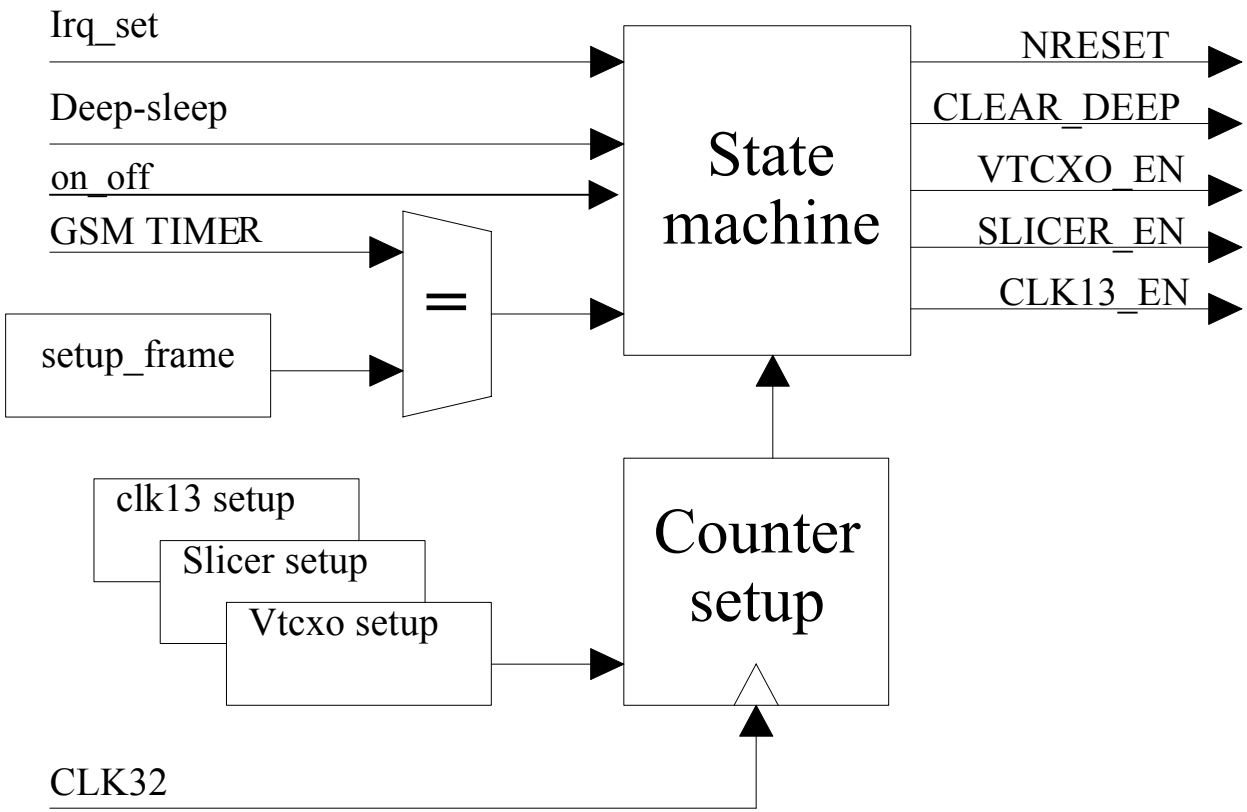
- TDMA frame based timer for power on control & interrupt generation to MCU

Calypso - ULPD: Gauging 32 KHz Clock

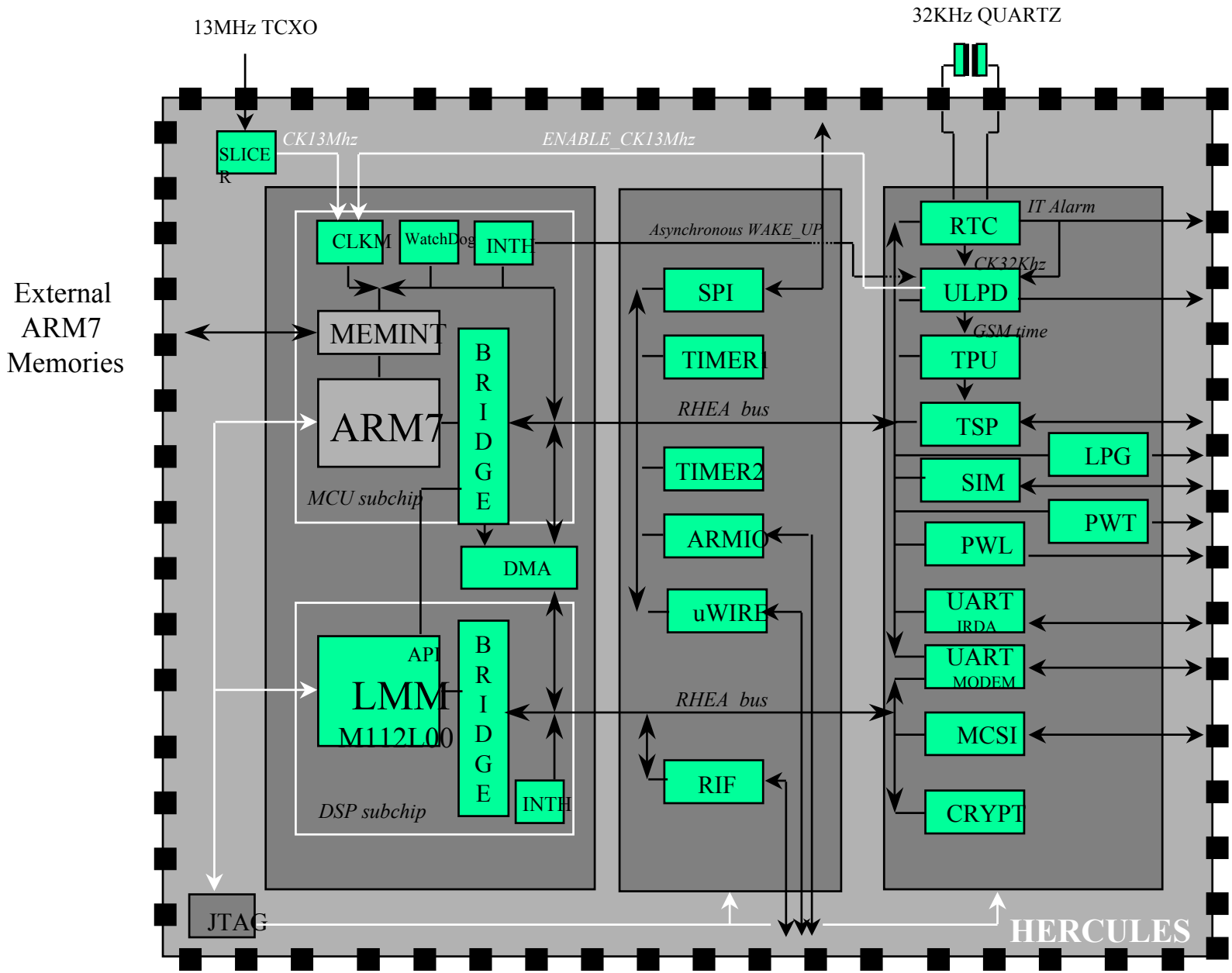


- Compare 32 KHz with a high frequency clock during any active period.
- Compare 32 KHz with the GSM network time.

Calypso - ULPD: Deep Sleep Functional block diagram



Calypso – Small sleep(1)



Calypso - Small sleep(2)

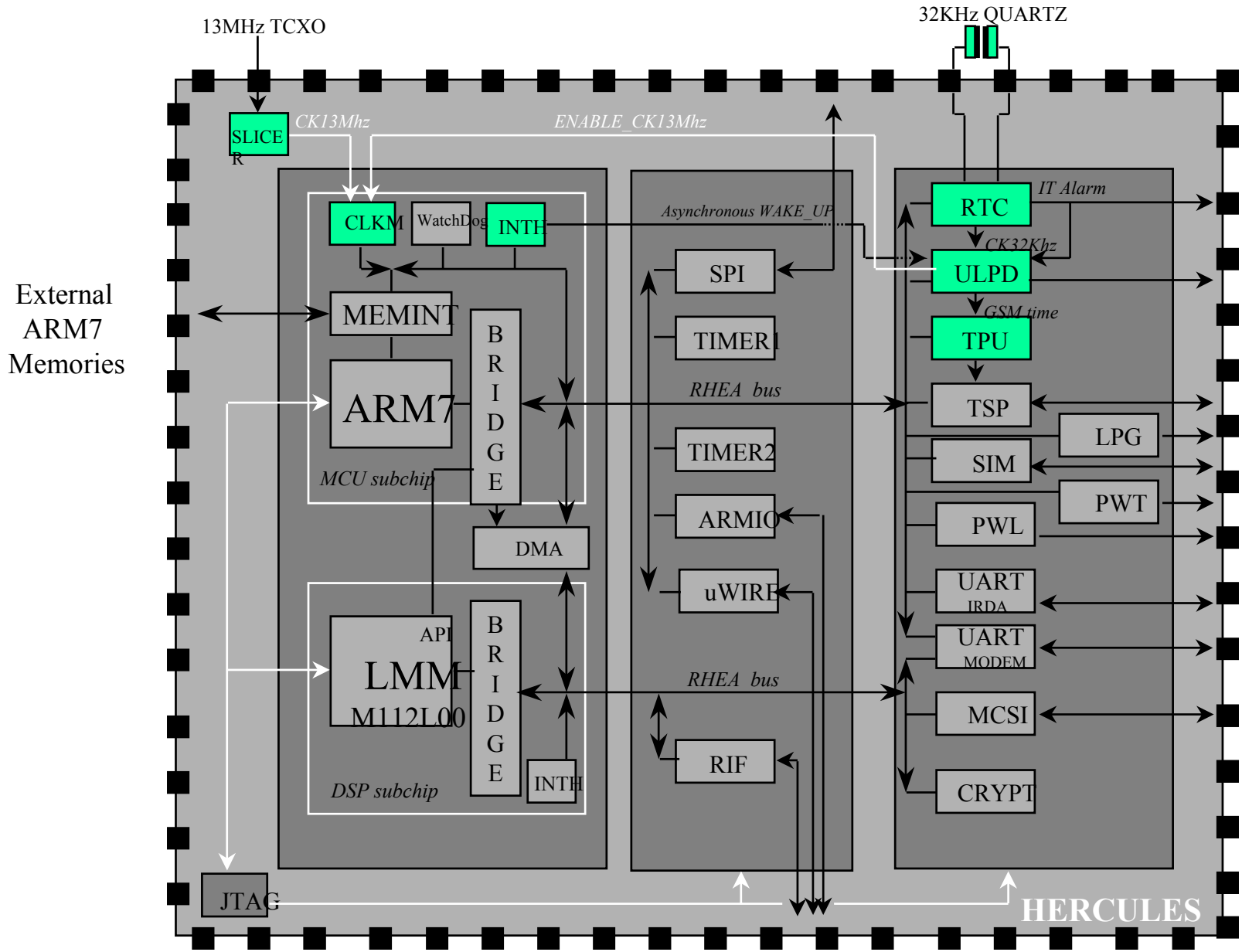
- Small Sleep

  - VTCXO ON
  - ARM clock OFF
  - TDMA interrupt enabled
  - LEAD clock stopped

- Small Sleep Wake-up Events

  - TDMA interrupt
  - ARMIO (keypad)
  - UART
  - External IRQ/FIQ (if not masked)
  - GSM Timer interrupt

Calypso - Big Sleep(1)



Calypso - Big sleep(2)

- Big Sleep

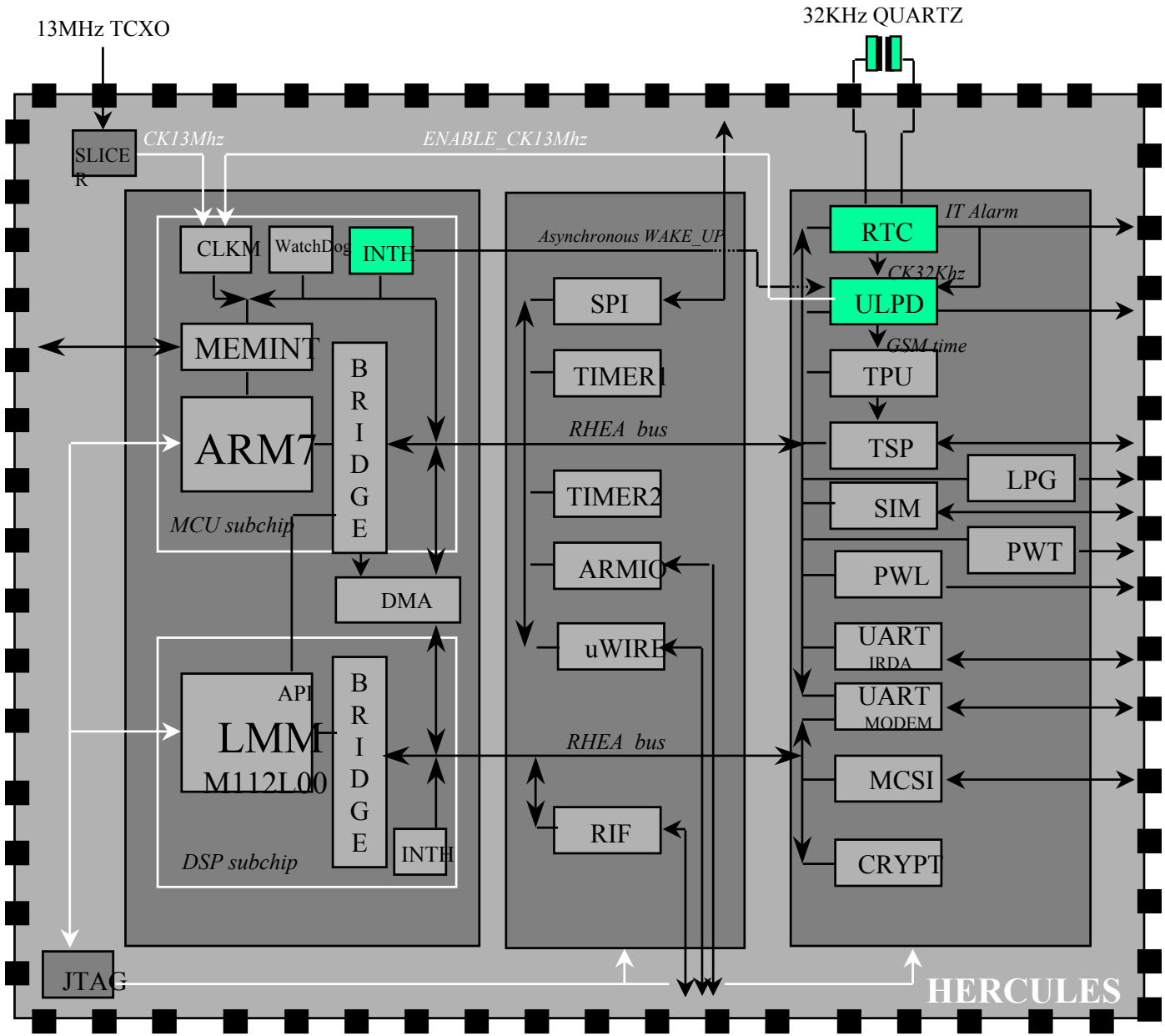
  - VTCXO ON
  - ARM clock OFF
  - TDMA interrupt disabled
  - GSM Timer interrupt enabled
  - CLKM, INTH, RTC, ULPD, TPU remain ON
  - LEAD clock stopped

- Big Sleep Wake-up Events

  - GSM Timer interrupt
  - ARMIO (keypad)
  - UART
  - RTC
  - All unmasked interrupts
  - WatchDog timer

Calypso - Deep Sleep(1)

External ARM7 Memories



Calypso - Deep Sleep(2)

- Deep Sleep

  - VTCXO, ARM clock and all clocks derived from 13 MHz are OFF
  - TDMA interrupt disabled
  - GSM Timer interrupt enabled
  - INTH, RTC, ULPD remain ON
  - GSM time base on 32 KHz
  - LEAD clock stopped

- Deep Sleep Wake-up Events

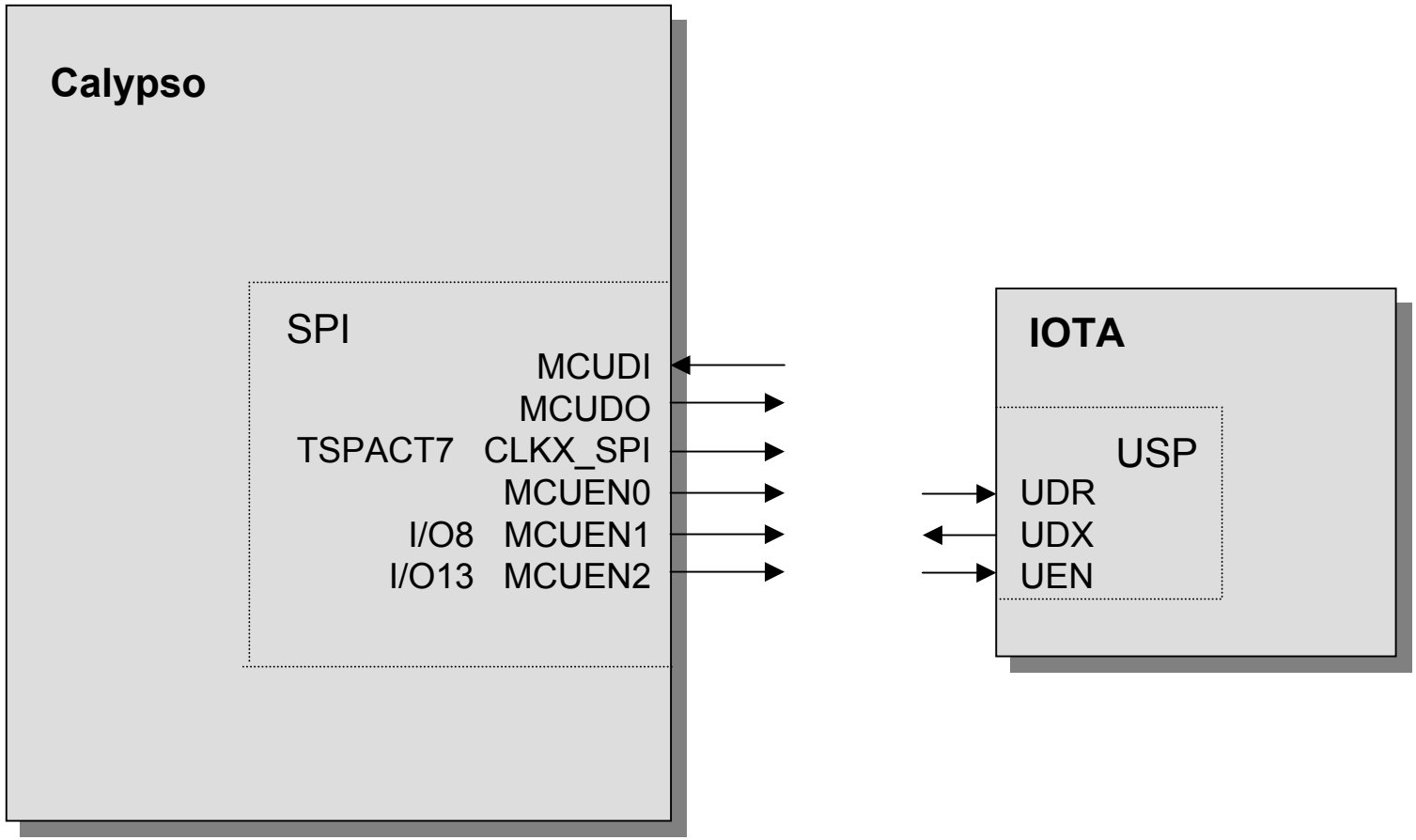
  - GSM Timer interrupt
  - ARMIO (keypad)
  - UART
  - RTC
  - External IRQ/FIQ (if not masked)

Serial Port Interface

Calypso - SPI: Interface

ARM SERIAL PORT : 5 pins.			Reset
MCUDI	IN	Input serial data.	input
MCUDO	OUT	Output serial data.	0
CLKX_SPI	OUT	Serial clock	0
MCUEN(2:0)	OUT	Configurable enable triggers (edge/level,positive/negative)	111

Calypso - Pins Description of SPI

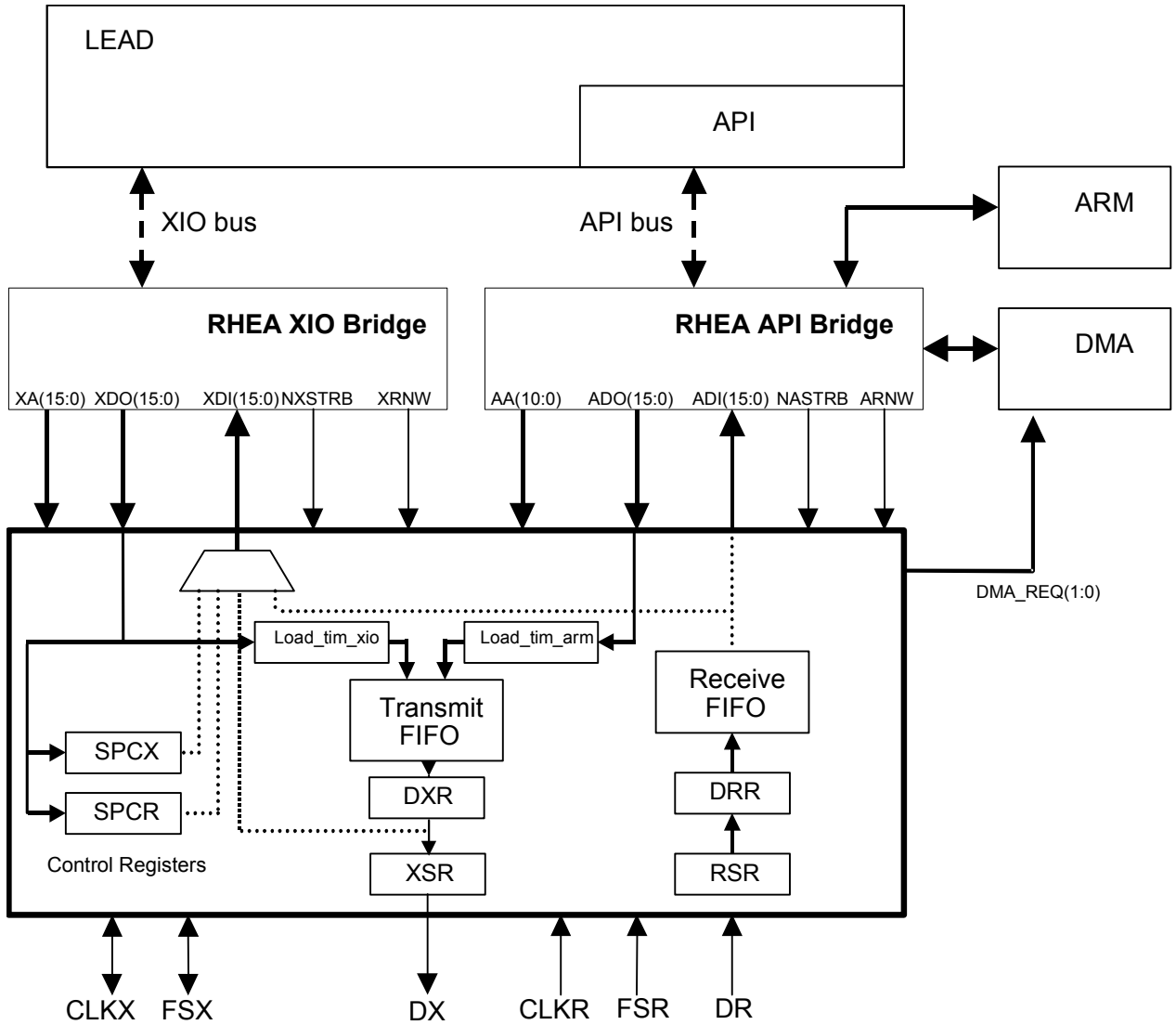


Calypso - ARM Interrupts (SPI)

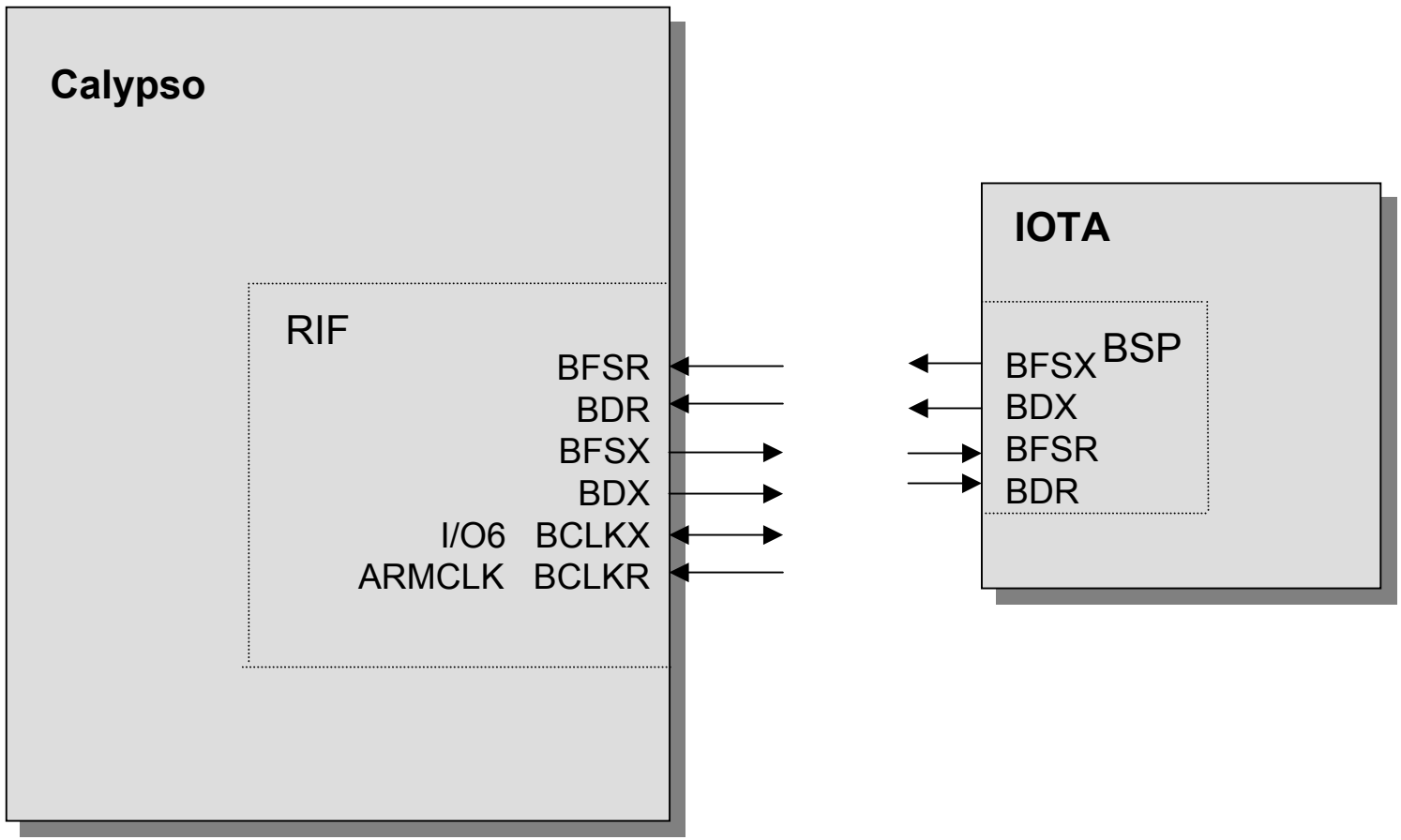
IRQ0	IRQ	(edge)	WatchDog TIMER
IRQ1	IRQ	(edge)	TIMER1
IRQ2	IRQ	(edge)	TIMER2
IRQ3	FIQ	(level)	EXT_FIQ, TSP Rx, SIM card insertion/extraction
IRQ4	IRQ	(edge)	TPU frame
IRQ5	IRQ	(edge)	TPU page
IRQ6	IRQ	(edge)	SIM
IRQ7	IRQ	(level)	UART_MODEM or UART_IRDA
IRQ8	IRQ	(level)	Keyboard
IRQ9	IRQ	(edge)	RTC
IRQ10	IRQ	(level)	RTC Alarm, ULPD GSM timer, I2C
IRQ11	IRQ	(edge)	ULPD end of gauging
IRQ12	IRQ	(level)	EXT_IRQ
IRQ13	IRQ	(edge)	SPI
IRQ14	IRQ	(level)	DMA
IRQ15	IRQ	(edge)	API

Radio Interface

Calypso - Radio Interface



Calypso - Pins Description of RIF

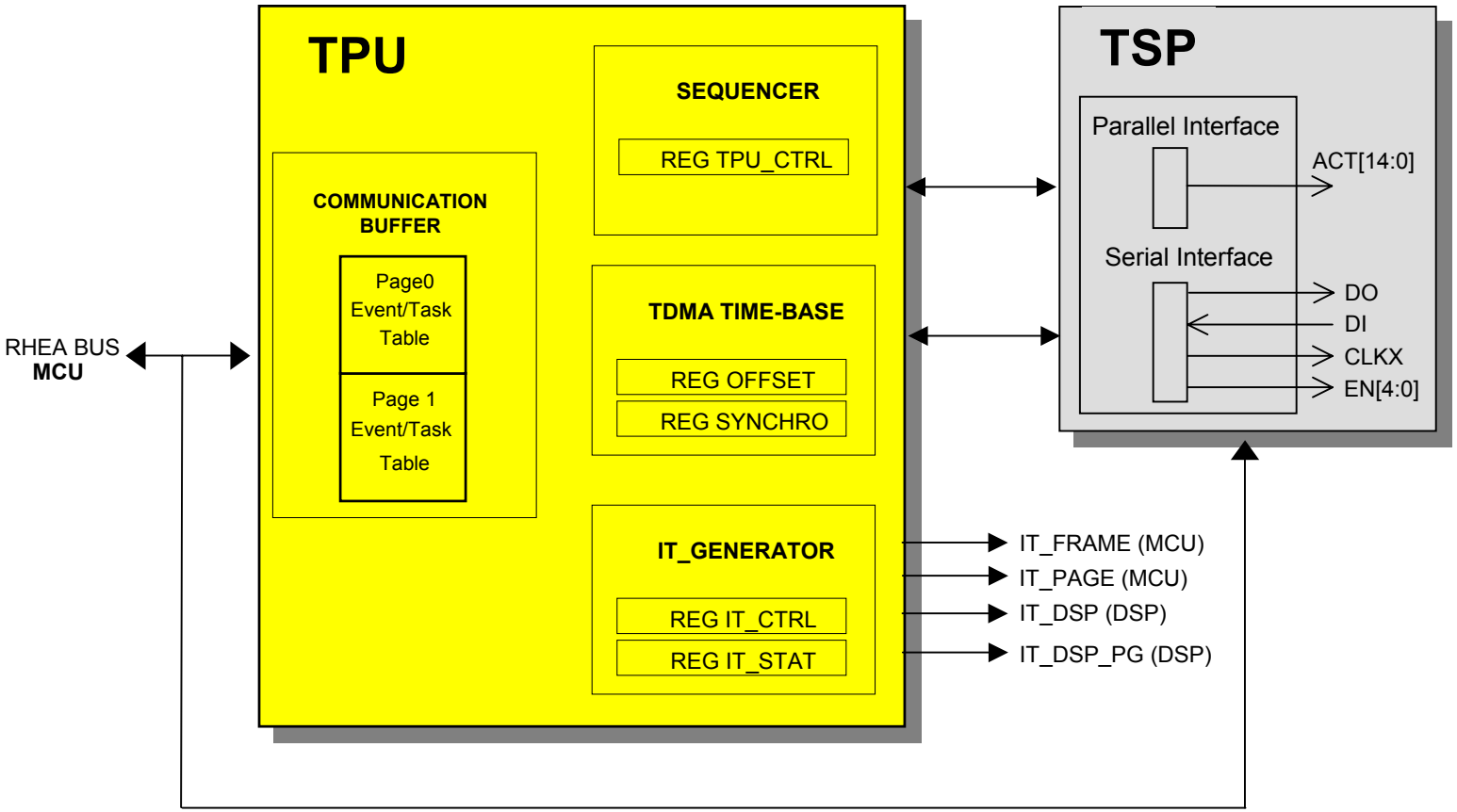


Calypso - DSP Interrupts (RIF)

RSN	reset (HW or SW)
INT0n	RIF receive interrupt
INT1n	RIF transmit interrupt

Time Processing Unit

Calypso - TPU with TSP



Calypso - TPU : micro-instruction set

TPU

- Micro instructions for ***time scheduling***

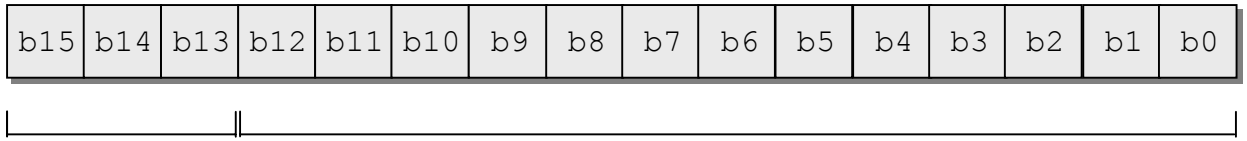
- start a process at a relative time in the frame	AT
- load the offset value for the network time	OFFSET
- load the offset value for the synchronization time	SYNCHRO
- load the waiting time before execution of next instruction	WAIT
- stop the squencer	SLEEP

- Micro instruction for ***data processing***

- write a word (max 8 bits) to a register	MOVE

Calypso - TPU : Gerneal format of micro-instruction

INSTRUCTION FOR TIME SCHEDULING

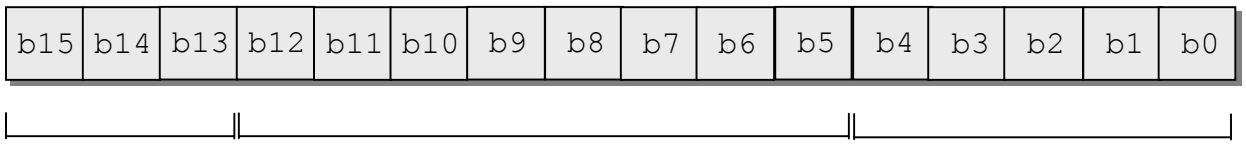


Instruction code

Absolute time 0..4999
(qbit GSM step)

000 SLEEP
001 AT
010 OFFSET
011 SYNCHRO
101 WAIT

INSTRUCTION FOR DATA TRANSFER



Instruction code

Data operand

Destination address

100 MOVE

Calypso - TPU : Interrupt Generation

- MCU Interrupts

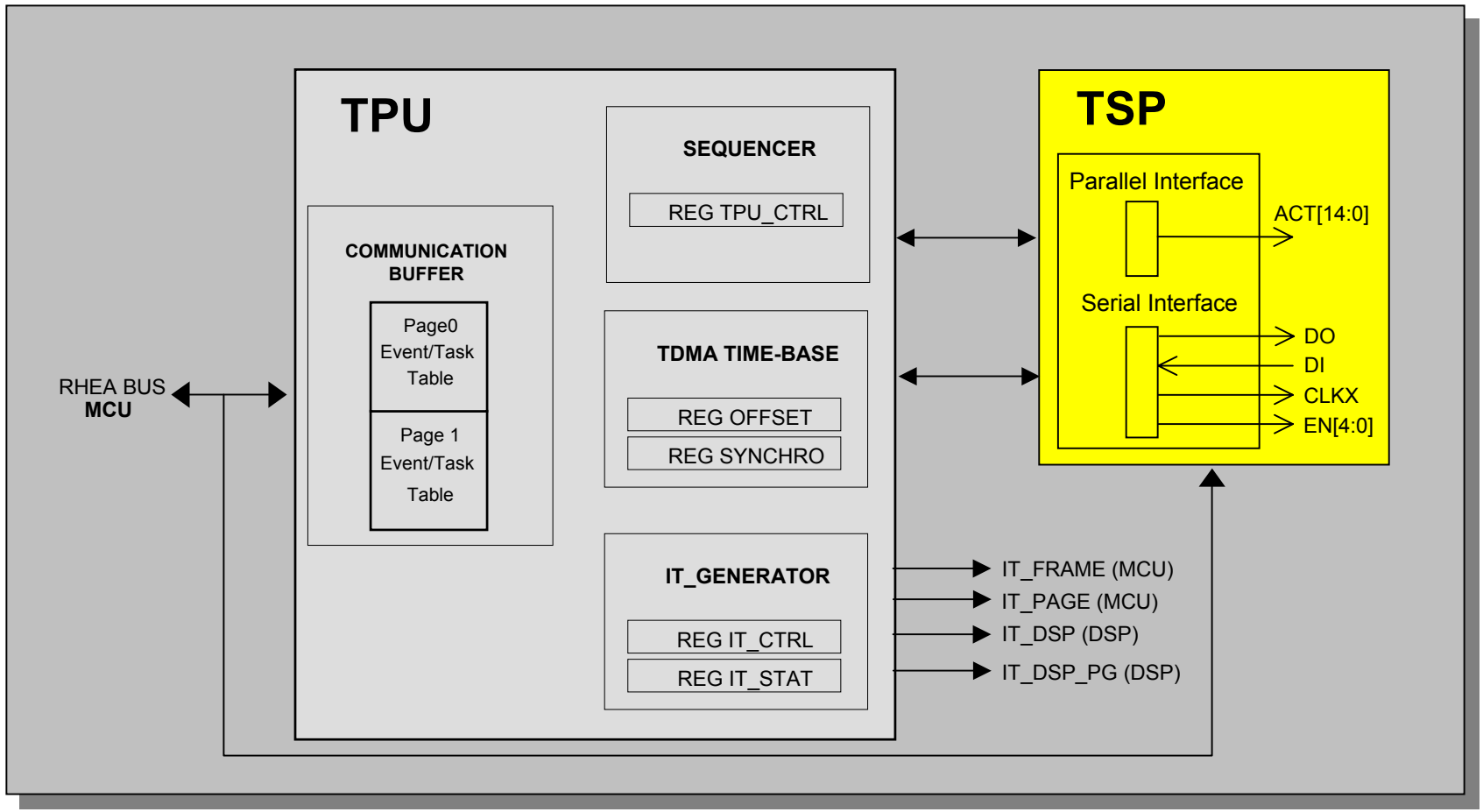
  - IT_FRAME: *at the start of the frame*
  - IT_PAGE: *the active page transition occurred*

- DSP Interrupts

  - IT_DSP: *at the start of the frame*
  - IT_DSP_PG: *programmable anytime through the use of MOVE instruction*

Time Serial Port

Calypso - TSP with TPU



Calypso - Features of TSP

- TSP is a peripheral of the TPU which includes:

  - a serial port
  - a parallel interface

- Both interfaces are TPU programmable with a time accuracy of the quarter of GSM bit.

- The serial port is bi-directional and the received data can be directly accessed by the MCU on the occurrence of an interrupt

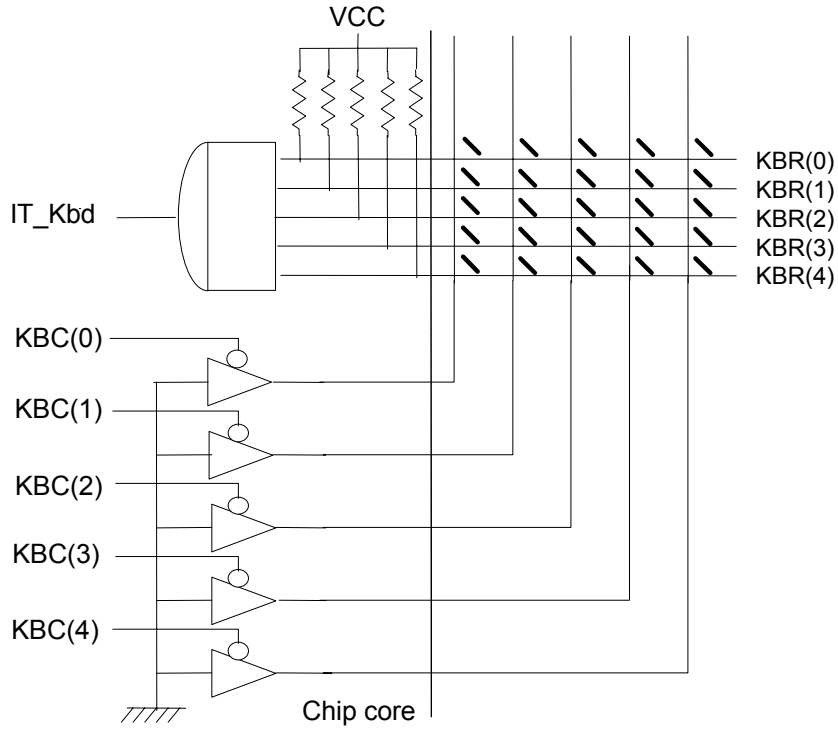
ARM I/O

Calypso – ARMIO Function

Features:

- 16 general purpose I/O
- specific I/O for 5X5 keyboard connection
- buzzer and light control
- One of the GPIO can be selected to generate an interrupt on a level change.
- Each keyboard input state change generates an interrupt to the MCU

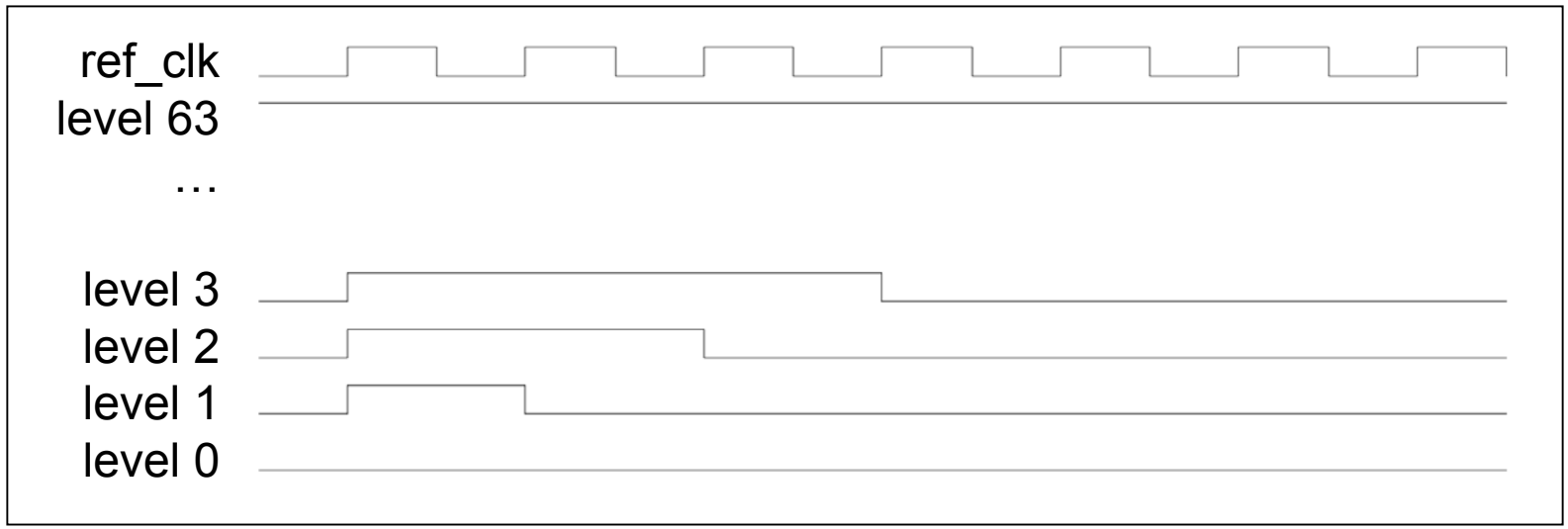
Calypso - ARMIO : Keyboard connection



	IDLE	KEYBOARD SCAN						IDLE
KBC(0)	0	1	0	1	1	1	1	0
KBC(1)	0	1	1	0	1	1	1	0
KBC(2)	0	1	1	1	0	1	1	0
KBC(3)	0	1	1	1	1	0	1	0
KBC(4)	0	1	1	1	1	1	0	0

Calypso - ARMIO : PWM and Tone Creation

- The reference clock of PWM is 2MHz



- Ttone = Tclk*(LOAD_TIM+1)*2^(9)

Fclk = 13MHz, LOAD_TIM = 1 => Ftone = 12.695kHz
LOAD_TIM = 2 => Ftone = 8.464kHz
LOAD_TIM = 255 => Ftone = 99Hz

General Purpose Timer

Calypso - Features of Timers

- Three 16 bits Timer
- Timer Clock is 13/16 MHz
- auto reload mode or one shot
- Watchdog can be configured as a general-purpose timer.

Calypso - Timer interrupts period of Timers

$$Tint = Tclk * (LOAD\_TIM+1) * 2^{(PTV+1)}$$

PTV	Divisor
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256

Tclk = Ext_Tclk * 16

Ext_Tclk = 1/13 MHz => Ext_Tclk = 0.0769 us Tclk = 1.2308us

LOAD_TIM	PTV=0	PTV=7
0000	2.4615 us	315.07us
FFFF	161.32ms	20.649 s

Calypso - Timer interrupt period of WatchDog

Tint = Tclk * (LOAD_TIM+1) * 2 $^{(PTV+1)}$

PTV	Divisor
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256

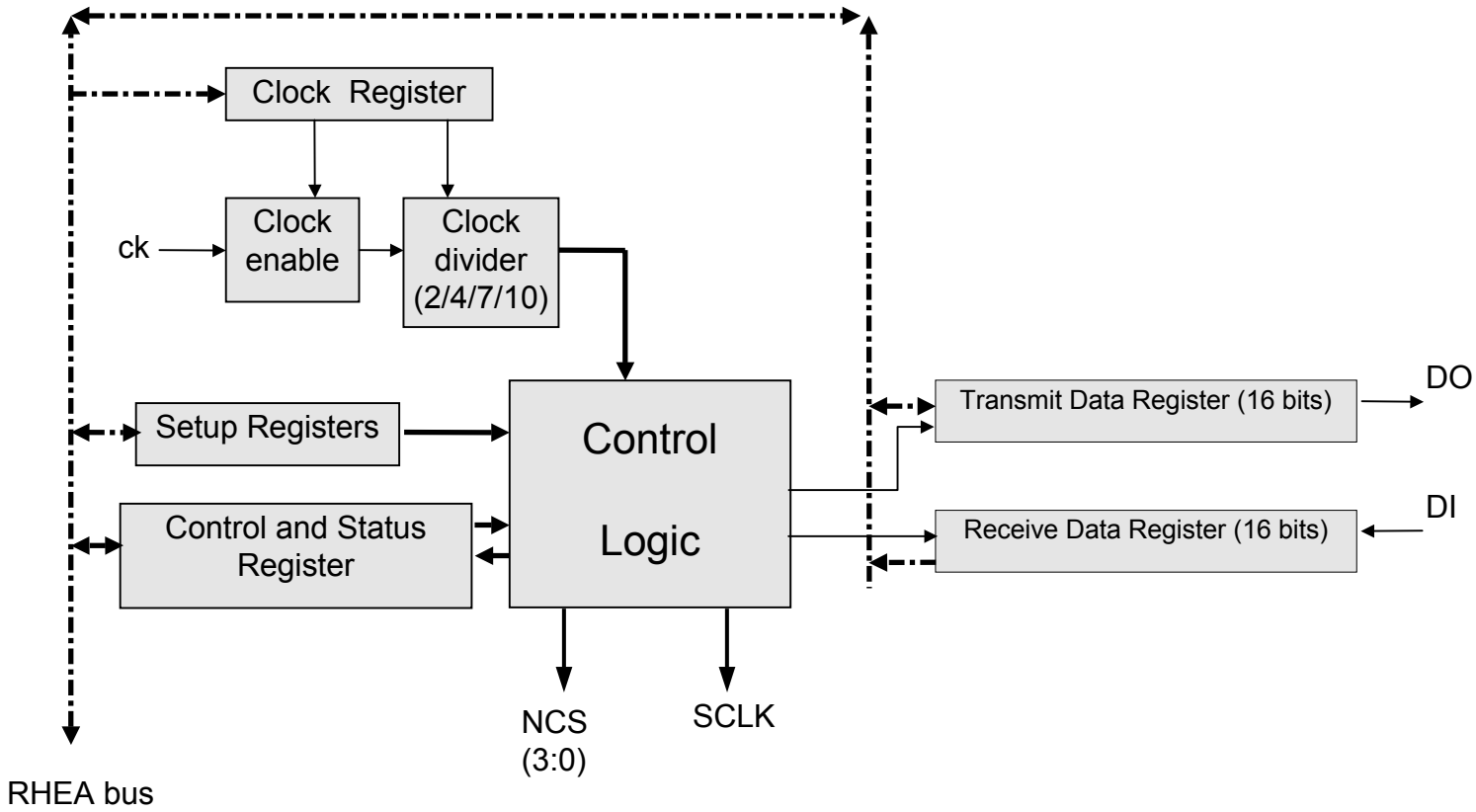
Tclk = Ext_Tclk * 16
Ext_Tclk = 1/13 MHz => Ext_Tclk = 0.0769 us Tclk = 1.2308us

LOAD_TIM	PTV=0	PTV=7
0000	2.156 us	275.8us
FFFF	141.3ms	18.078 s

Note: PTV = 7 in WatchDog mode

Uwire

Calypso - Block diagram of uWire



TSCLK = CK_FREQ * Csi_FRQ * T13M = [2/4/7/10] * [2/4/8] * T13M

I2C Interface

Calypso - I2C : Features

The Master 12C Interface Module supports I2C Master Only mode with

1. 7 bits device address
2. 8 bits sub address
3. Master write to slave receiver in single or multiple mode
4. Master simple read to slave receiver
5. Read Combined cycle
6. Programmable clock
7. Error Handling Capability during I2C bus access

Calypso - I2C : Programmable Clock

SCL clock output = Fclk / (Divisor_1 * (Divisor_2+1) * 3)

Divisor_1 = 1,2,4,8,16
Divisor_2 = 1,2,3,4,..,128

For SCL_OUT = 100 kHz
Divisor_1 = 4
Divisor_2 = 10

Calypso - I2C : Error Handling

- Interrupt generated if no ACK on Device, Sub-address and Data

UART

Calypso - UART

– **UART/IrDA module:**
  • an IrDA SIR protocol encoder/decoder can be optionally selected to manage the RXIR and TXIR signals to an IrDA transceiver.

– **UART/modem module:**
  • incorporates an autobauding mechanism and the possibility to connect dynamically the UART/modem to the DSP or MCU Rhea buses.

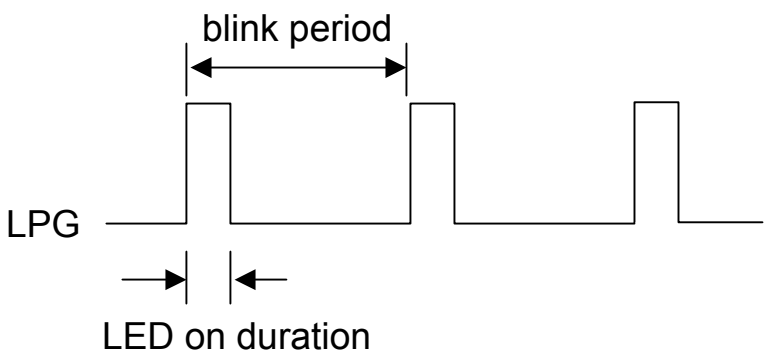
Calypso - UART Common Features

- 64-word deep FIFO for received/transmitted characters
- The trigger levels for the FIFOs are independently
- Selectable/programmable for DMA and interrupt purposes.
- Configurable to send even, odd or no parity and 1, 1½ or 2 stop bits.
- The number of data bits can be configured between 5 and 8.
- Break characters are detected and can be generated.
- They generate their own baud rate based upon a programmable divisor.

Calypso - LED Pulse Generator (LPG)

LPG control register (LCR_REG)

Bit	Name	Function	R/W	Value at reset
2:0	PERCTRL	LED blink frequency	R/W	000
5:3	ONCTRL	time LED is on parameter	R/W	000
6	LPGRES	LPG counter reset, active low	R/W	0
7	PERM_ON	set high to force permanent light on	R/W	0



PERCTRL

Bit 2:0	Blink Period (sec)
000	0.125
001	0.25
010	0.5
011	1
100	1.5
101	2
110	2.5
111	3

ONCTRL

Bit 5:3	LED on (ms)
000	15.63
001	31.25
010	46.88
011	62.5
100	78.13
101	93.75
110	109.38
111	125

Calypso - Pulse Width Light modulator (PWL)

PWL_LEVEL_REG

Bit	Name	Function	Value at hardware reset	Access
7:0	PWL_LEVEL	Defines the mean value of the PWL output signal. 0 leads to a continuous ‘0’ output, 255 to a continuous ‘1’ output	0000 0000	R/W

Calypso - Pulse Width modulation Tone (PWT)

Frequency Control Register (FRC_REG)

Bit	Name	Function	R/W	Value at reset
1:0	OCT	octave select	R/W	00
5:2	FRQ	frequency select (12 frequencies)	R/W	0000

FRC bits 5-2 1-0	Buzzer frequency	FRC bits 5-2 1-0	Buzzer frequency	FRC bits 5-2 1-0	Buzzer frequency	FRC bits 5-2 1-0	Buzzer Frequency
0000 00	5274Hz e^5	0000 01	2637Hz e^4	0000 10	1319Hz e^3	0000 11	659Hz e^2
0001 00	4978Hz dis^5	0001 01	2489Hz dis^4	0001 10	1245Hz dis^3	0001 11	622Hz dis^2
0010 00	4699Hz d^5	0010 01	2349Hz d^4	0010 10	1175Hz d^3	0010 11	587Hz d^2
0011 00	4435Hz cis^5	0011 01	2217Hz cis^4	0011 10	1109Hz cis^3	0011 11	554Hz cis^2
0100 00	4186Hz c^5	0100 01	2093Hz c^4	0100 10	1047Hz c^3	0100 11	523Hz c^2
0101 00	3951Hz h^4	0101 01	1976Hz h^3	0101 10	988Hz h^2	0101 11	494Hz h^1
0110 00	3729Hz ais^4	0110 01	1865Hz ais^3	0110 10	932Hz ais^2	0110 11	466Hz ais^1
0111 00	3520Hz a^4	0111 01	1760Hz a^3	0111 10	880Hz a^2	0111 11	440Hz a^1
1000 00	3322Hz gis^4	1000 01	1661Hz gis^3	1000 10	831Hz gis^2	1000 11	415Hz gis^1
1001 00	3136Hz g^4	1001 01	1568Hz g^3	1001 10	784Hz g^2	1001 11	392Hz g^1
1010 00	2960Hz fis^4	1010 01	1480Hz fis^3	1010 10	740Hz fis^2	1010 11	370Hz fis^1
1011 00	2794Hz f^4	1011 01	1397Hz f^3	1011 10	698Hz f^2	1011 11	349Hz f^1

Thank you!