



Product Datasheet

WM3236AQ

WLAN 802.11b/g SiP Module ***QFN Package/SDIO Interface***

Version : v0.2

Issue Date: July 1st 2007

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■ Revision History

Date	Revision	Comments
2007/06/06	0.1	First draft
2007/06/25	0.2	Second draft

■ Description

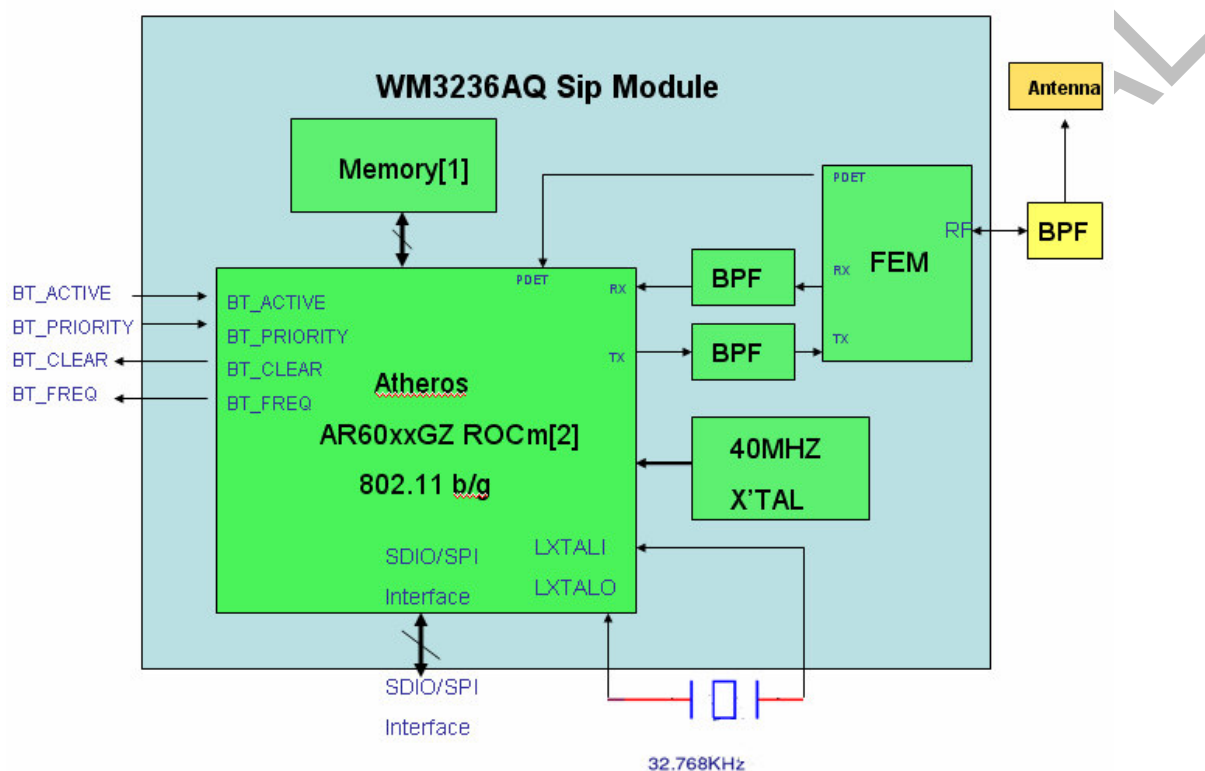
WM3236AQ is a highly integrated WiFi SiP Module solution for handheld or WiFi enabled consumer devices. It includes a 2.4GHz radio, analog-to-digital and digital-to-analog converters, a base-band processor, multi-protocol media access control (MAC), CPU, RF Front End Module (FEM), Band Pass Filter, 40MHz Crystal, and 4Mbit Flash(Flash version),and 8k bit EEPROM (ROM version). It enables a high performance, cost effective, low power, compact solution in a Digital Camera, cellular/WLAN handset, PDA, VoIP handset, or MP3/4 player.

The WM3236AQ implements half-duplex OFDM, CCK and DSSS base-band processing supporting all IEEE 802.11b/g data rates. The MAC supports the IEEE 802.11 wireless MAC protocol as well as 802.11i security, receive and transmit filtering, error recovery, and quality of service (QoS).

■ Features

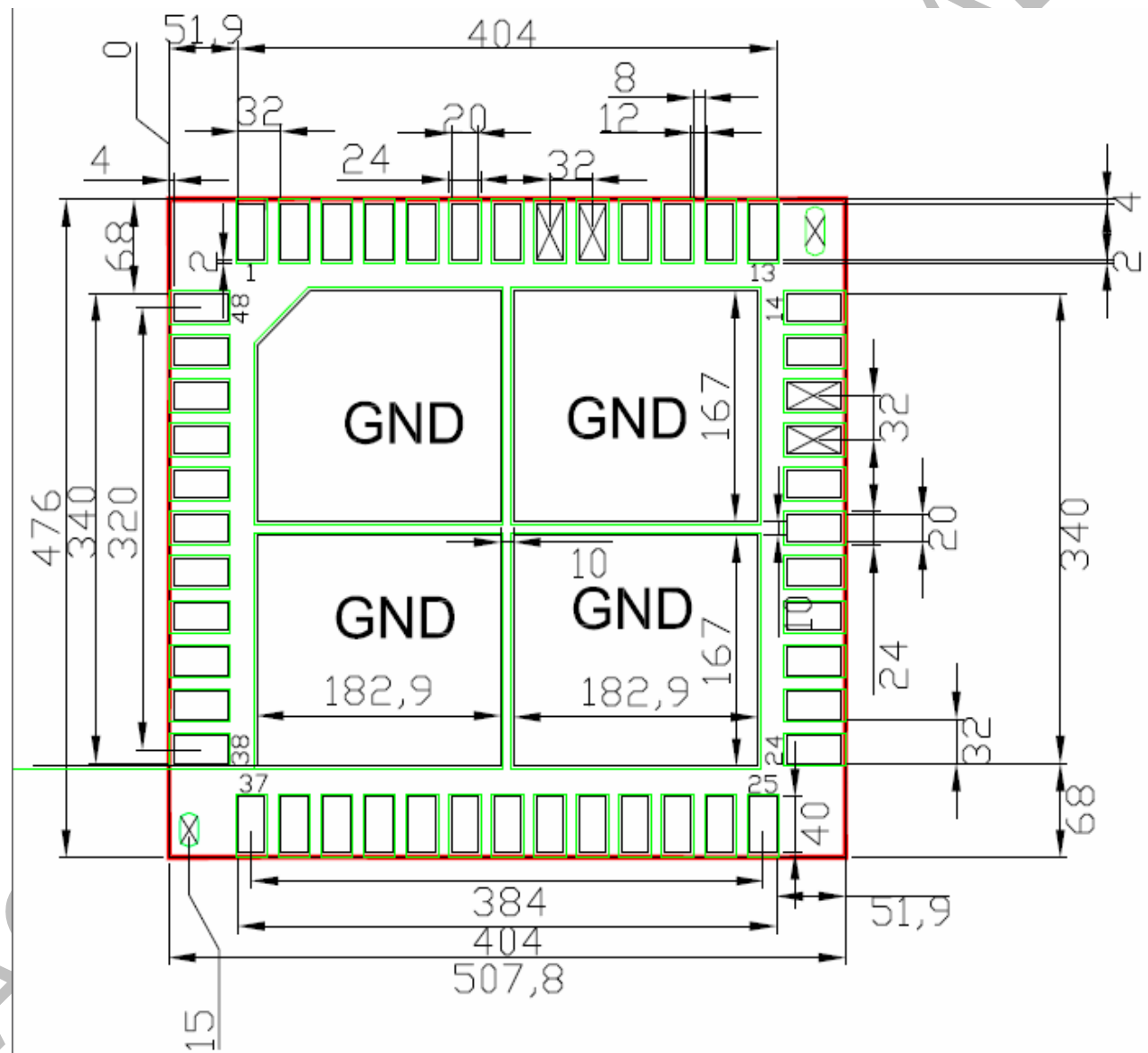
- 3.3V, 1.8V Power Supply
- Highly Integrated System in Package (SiP) for IEEE 802.11b/g compatible WLAN
- Operates in 2.4GHz frequency bands: 2.412-2.472GHz, 2.484GHz
- Data rates of 1-54Mbps for 802.11g
- Bluetooth coexistence handshaking
- Integrated Atheros AR6001GZ ROCm(Flash version),AR6031GZ ROCm(ROM version)
- Integrated high performance Front End Module (FEM), Band Pass Filter, 40MHz Crystal
- 4Mbit Flash memory(Flash version) or 8k bit EEPROM(ROM version) and UART
- SDIO interface support
- Advanced power management to minimize standby and active power
- Package size is 12.9mm*12.1mm*1.25mm, 48 pins QFN

Block Diagram

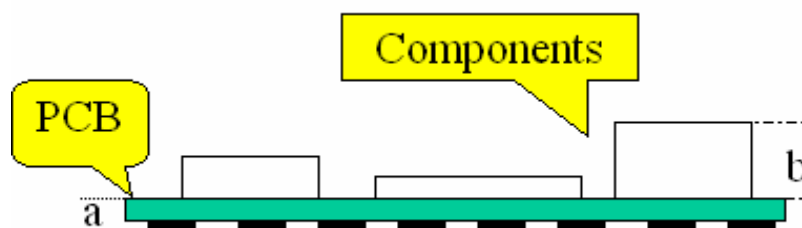


[1] Flash version: Flash Memory
ROM version: EEPROM Memory

[2] Flash version: Atheros AR6001GZ
ROM version: Atheros AR6031GZ

Package Mechanical Drawing – 48 pin,**Unit: mil****Top view**

Appearance - QFN



a: 0.4 mm

b: 0.8 mm(the peak component height, TBD)

Package size is 12.9mm*12.1mm*1.25mm(Add shielding cover)

Pin Assignment

Pin Descriptions

NC: No connection should be made to this pin

P: Power or ground signal

I: Digital input signal

O: Digital output signal

I/O: Digital bidirectional signal

IH: Input signals with weak internal pull-up, to prevent signals from floating when left open

IL: Input signals with weak internal pull-down, to prevent signals from floating when left open

Number	Pin Name		Type	External PAD Power	Description
	Flash ver.	ROM ver.			
1	GND	GND	P		Ground
2	NC	NC			
3	GPIO8	GPIO8	I/OL	VDD18	General purpose I/O.
4	GPIO10	GPIO10	I/OL	VDD18	General purpose I/O.
5	NC	NC			
6	LDO_BYPASS	LDO_BYPASS	I	VDD33	Assert to bypass on-chip LDO for the digital. If bypassed, the main board must supply 1.8V to module .via the VDD18
7	VDD18	VDD18	P	-	1.8V power supply When LDO_BYPASS is asserted ,the main board must supply 1.8V to module
8	GND	GND	P		Ground
9	NC	EJTAG_SEL	I	VDD33	10K ohm pull high
10	NC	NC		-	
11	VDD33	VDD33	P	-	3.3V Power supply
12	VDD33	VDD33	P	-	3.3V Power supply
13	GND	GND	P	-	Ground
14	GND	GND	P	-	Ground
15	NC	NC		-	
16	NC	NC		-	
17	VDD18	VDD18	P	-	1.8V power supply When LDO_BYPASS is asserted ,the main board must supply 1.8V to module
18	VDD18	VDD18	P	-	1.8V power supply When LDO_BYPASS is asserted ,the main board must supply 1.8V to module
19	CLK_REQ	CLK_REQ	O	VDD_SDIO	10Kohm pull low

20	LF_XTALI	LF_XTALI	CRYSTAL/I	-	32.768KHz clock input
21	LF_XTALO	LF_XTALO	CRYSTAL/O	-	32.768KHz clock output
22	GPIO9	GPIO9	I/OL	VDD_SDIO	General purpose I/O.
23	NC	NC		-	
24	RF	RF	I/O	-	RF output
25	VDD18_SDIO	VDD18_SDIO	P	-	1.8V supply When SDIO_LDO-BYPASS be asserted ,the main board must supply 1.8V to module.
26	VDD_SDIO	VDD_SDIO	P	-	Digital power supply for:SDIO_CLK,SDIO_CMD,SDIO_DATA0,SDIO_DATA1,SDIO_DATA2,SDIO_DATA3,SDIO_LDO_BYPASS,CLK_REQ,SYS_RST_L,GPIO9,CHIP_PWD,TDO
27	SDIO_DATA3	SDIO_DATA3	I/O	VDD_SDIO	SDIO: Data line bit3
28	SDIO_DATA0	SDIO_DATA0	I/O	VDD_SDIO	SDIO: Data line bit0
29	SDIO_DATA0	SDIO_DATA2	I/O	VDD_SDIO	SDIO: Data line bit2
30	SDIO_DATA1	SDIO_DATA1	I/O	VDD_SDIO	SDIO: Data line bit1
31	SDIO_CLK	SDIO_CLK	I	VDD_SDIO	SDIO input clock for host (up to 25MHz)
32	SDIO_CMD	SDIO_CMD	I	VDD_SDIO	SDIO command line.
33	SDIO_LDO_BYPASS	SDIO_LDO_BYPASS	IL	VDD_SDIO	Assert to bypass on-chip LDO for SDIO block, the main board must supply 1.8V to SDIO block via the VDD18_SDIO pin.
34	SYS_RST_L	SYS_RST_L	IH	VDD_SDIO	Module reset; Must be asserted when power is first applied to the chip; then released before any transaction can start.
35	NC	NC		-	
36	VDD18	VDD18	P	-	1.8V power supply When LDO_BYPASS is asserted ,the main board must supply 1.8V to module
37	GND	GND	P	-	Ground
38	GND	GND	P	-	Ground
39	TDO	TDO	IL	VDD_SDIO	This pin must be pulled to the appropriate level during reset for interface configuration.
40	CHIP_PWD	CHIP_PWD	I	VDD_SDIO	Assertion powers down the module to minimal power, NO LDO in enabled, no state retained , and no transaction performed while CHIP_PWD is asserted.

					When de-asserting CHIP_PWD ,SYS_RST_L must be asserted to restart the module.
41	BT_FREQ	BT_FREQ	I	VDD18	Indicates external source is transmitting on a restricted frequency band. Tie to GND when not in use
42	BT_PRIORITY	BT_PRIORITY	I	VDD18	When BT_ACTIVE is asserted, indicates the external device transmits or receives at high priority. Tie to GND when not in use.
43	BT_ACTIVE	BT_ACTIVE	I	VDD18	Indicates medium busy from an external sources; can be asserted to prevent the AR6001 from transmitting a new frame. Tie to GND when not in use.
44	RX_CLEAR	RX_CLEAR	O	VDD18	Indicates medium clear to an external device, which should transmit only when RX_CLEAR is asserted.
45	RXD0	RXD0	I	VDD18	UART:RX
46	TXD0	TXD0	O	VDD18	UART:TX
47	VDD18	VDD18	P		1.8V power supply When LDO_BYPASS is asserted ,the main board must supply 1.8V to module
48	NC	NC			

Mode Configuration

GPIO9	TD0	Configuration
0	0	Generic SPI Mode
0	1	SDIO Mode

Application Note

■ Bluetooth Co-Existence

◆ CSR 3 wire

- BT_PRIORITY ↔ BT_PRIORITY_AND_STATUS
- BT_ACTIVE ↔ BT_ACTIVITY
- RX_CLEAR ↔ WLAN_ACTIVITY
- BT_FREQ ↔ GROUND

◆ CSR 2 wire

- BT_PRIORITY ↔ BT_ACTIVITY
- BT_ACTIVE ↔ BT_ACTIVITY
- RX_CLEAR ↔ WLAN_ACTIVITY
- BT_FREQ ↔ GROUND

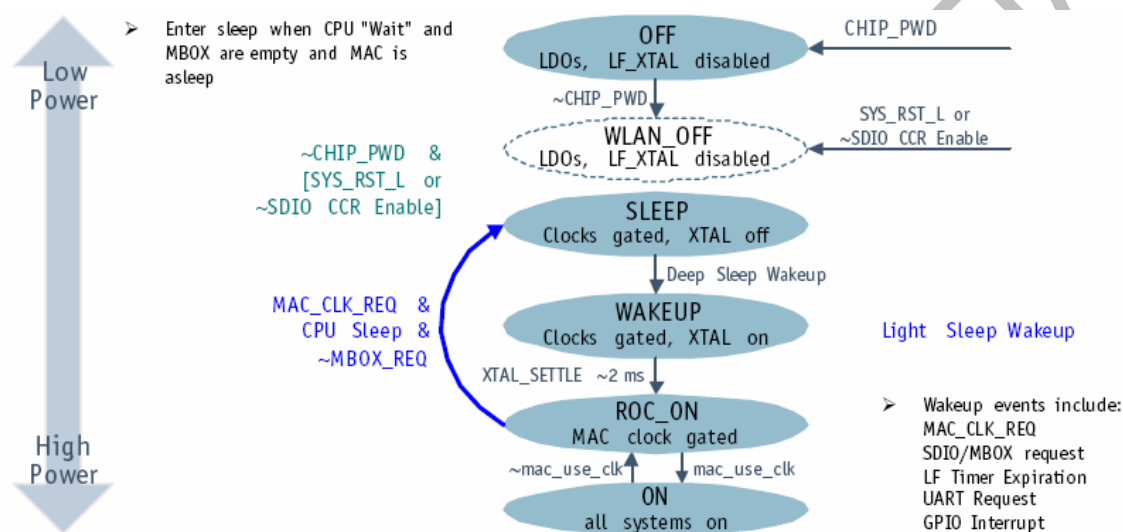
■ GSM Coexistence

- ◆ Add an external SOSHIN HMD842 BandPass Filter (or equal) for out band noise suppressing.

Power Management States

State	Description
OFF	CHIP_PWD pin assertion immediately brings the chip to this state
	LF_XTAL (32.768 KHz sleep clock) is disabled
	LDOs are all off
	No state is preserved
	When CHIP_PWD de-asserts, the system must assert SYS_RST_L until the power has stabilized
WLAN _OFF	WLAN is turned off
	LF_XTAL (32.768 KHz sleep clock) is disabled
	This state can be bypassed by asserting CLK_REQ; state transitions from OFF to WAKEUP on SYS_RST_L/CHIP_PWD de-assertion
	Host software can expedite the transition out of WLAN_OFF state by writing to the CCCR
	SDIO interface is on
	Once the host enables the SDIO with a CCCR register write, the system begins to boot
	Embedded CPU and MAC do not retain state
SLEEP	Only the 32.768 KHz sleep clock is operating
	The high speed crystal or oscillator is disabled for deep sleep
	The digital core block is powered on, but its clocks are gated off
	All internal states are maintained
WAKEUP	The system transitions from deep sleep to ON
	The high frequency clock is gated off as the crystal or oscillator is brought up and the PLL is enabled
	WAKEUP duration is programmable (default 3.8 ms); the WAKEUP state is bypassed for light sleep
ROC_ON	The high speed clock is operational and sent to each block
	The MAC is asleep, and MAC clocks are gated off
	CPU, memory, MBOX, SDIO, and peripheral blocks are all operational
	The CPU may be in WAIT state
ON	The high speed clock is operational and sent to each block enabled by the clock control register
	Lower level clock gating is implemented at the block level, including the CPU, which can be gated off from WAIT instruction while the system is on

AR6001(AR6031)GZ State Transitions



Sleep State Management

Sleep state minimizes power consumption while saving system states. In deep sleep state, all high speed clocks are gated off and the external crystal is powered off. Light sleep is similar to deep sleep, but the XTAL remains running for faster WAKEUP. For the module to enter sleep state, the MAC, SDIO/MBOX, and CPU systems must be in sleep state. When the embedded MIPS CPU executes the WAIT command, the SDIO/MBOX is idle and the MAC system is in sleep state, the module enters the system Sleep state. In sleep state, the system gates all clock trees based on REF_CLK with only the sleep clock logic operating. The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the high frequency clock source to stabilize, and finally ungate all enabled clock trees. The CPU exits the WAIT state only when an interrupt arrives, which may result from the system WAKEUP event.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Max Rating	Unit
VDD18	1.8 V supply voltage	-0.3 to 2.5	V
VDD33	3.3 V supply voltage	-0.3 to 4	V
VDD_SDIO	VDD_SDIO supply voltage	-0.3 to 4	V
RF _{in}	Maximum RF input (reference to 50 Ω)	+10	dBm
T _{store}	Storage temperature	-45 to 135	degree
ESD	Electrostatic discharge tolerance	2000	V

Recommended Operating Conditions

Symbol	Parameter	Min	Type	Max	Unit
VDD18	Supply voltage	1.71		1.91	V
VDD33	Supply voltage	2.9		3.6	V
VDD_SDIO	Supply voltage	1.71		3.6	V
T _{ambient}	Ambient temperature	-40	25	85	Degree

DC Electrical Characteristics

General DC Electrical Characteristics (For 3.3 V I/O Operation, Vdd = VDD33 or VDD_SDIO)						
	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High Level Input Voltage		$0.8 \times V_{dd}$	-	$V_{dd} + 0.3$	V
V_{IL}	Low Level Input Voltage		-0.3	-	$0.2 \times V_{dd}$	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down $0 V < V_{in} < V_{dd}$ $0 V < V_{out} < V_{dd}$	-10	-	10	μA
		With Pull-up or Pull-down $0 V < V_{in} < V_{dd}$ $0 V < V_{out} < V_{dd}$	-65	-	65	μA
V_{OH}	High Level Output Voltage	$I_{OH} = -6 \text{ mA}$	$V_{dd} - 0.35$	-	-	V
		$I_{OH} = -12 \text{ mA}[1]$	$V_{dd} - 0.40$	-	-	V
		$I_{OH} = -24 \text{ mA}[1]$	$V_{dd} - 0.45$	-	-	V
V_{OL}	Low Level Output Voltage	$I_{OH} = 6 \text{ mA}$	-	-	0.35	V
		$I_{OH} = 12 \text{ mA}[1]$	-	-	0.4	V
		$I_{OH} = 24 \text{ mA}[1]$	-	-	0.45	V
C_{IN}	Input Capacitance[2]	-	-	6	-	pF

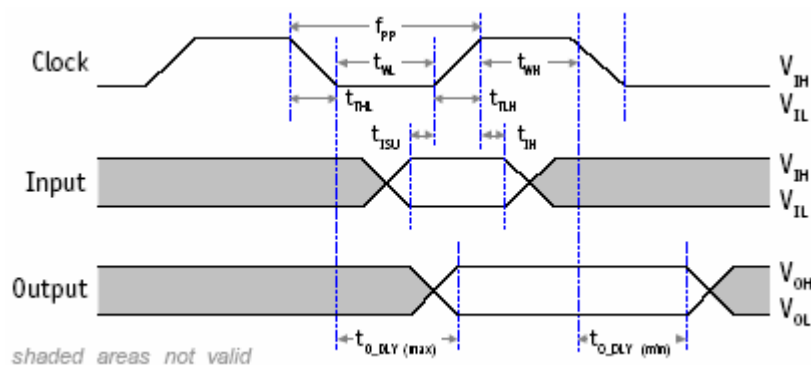
[1]For these pins only: CLK_REQ, GPIO9, SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_3
[2]Parameter not tested; value determined by design simulation

General DC Electrical Characteristics (For 1.8 V I/O Operation, Vdd = VDD18 or VDD_SDIO)						
	Parameter	Condition	Min	Type	Max	Unit
V_{IH}	High Level Input Voltage		$0.8 \times V_{dd}$	-	$V_{dd} + 0.3$	V
V_{IL}	Low Level Input Voltage		-0.3	-	$0.2 \times V_{dd}$	V
I_{IL}	Input Leakage Current	Without Pull-up or Pull-down $0 V < V_{in} < V_{dd}$ $0 V < V_{out} < V_{dd}$	-10	-	10	μA
		With Pull-up or Pull-down $0 V < V_{in} < V_{dd}$ $0 V < V_{out} < V_{dd}$	-35	-	35	μA
V_{OH}	High Level Output Voltage	$I_{OH} = -3 \text{ mA}$	$V_{dd} - 0.35$	-	-	V
		$I_{OH} = -6 \text{ mA}[1]$	$V_{dd} - 0.40$	-	-	V
		$I_{OH} = -12 \text{ mA}[1]$	$V_{dd} - 0.45$	-	-	V
V_{OL}	Low Level Output Voltage	$I_{OL} = 3 \text{ mA}$	-	-	0.35	V
		$I_{OL} = 6 \text{ mA}[1]$	-	-	0.4	V
		$I_{OL} = 12 \text{ mA}[1]$	-	-	0.45	V
C_{IN}	Input Capacitance[2]	-	-	6	-	pF

[1]For these pins only: CLK_REQ, GPIO9, SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_3
[2]Parameter not tested; value determined by design simulation

SD/SPI Interface Timing

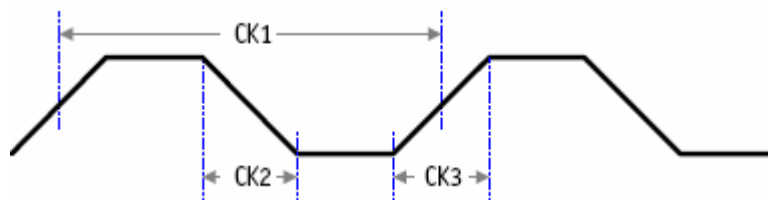
Shows the write timing for a SD/SPI style transaction.



SD/SPI Timing Constraints

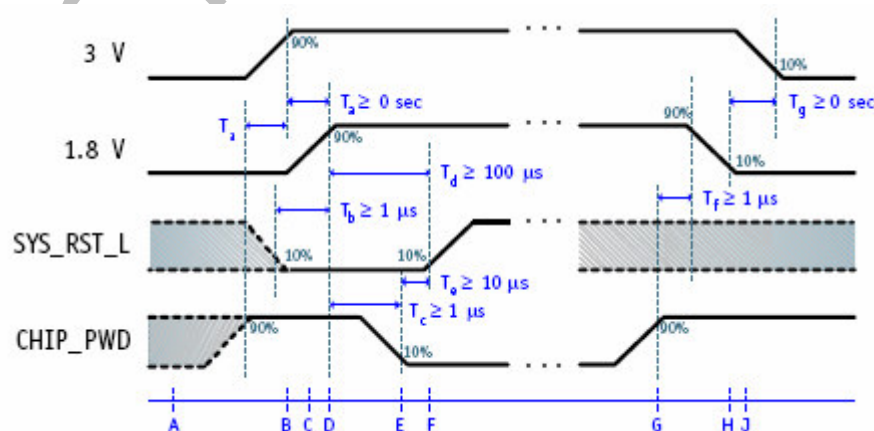
Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	25	MHz	100 pF $\geq C_L$ (7 cards)
t_{WL}	Clock low time	10	—	ns	100 pF $\geq C_L$ (7 cards)
t_{WH}	Clock high time	10	—	ns	100 pF $\geq C_L$ (7 cards)
t_{TLH}	Clock rise time	—	10	ns	100 pF $\geq C_L$ (10 cards)
t_{THL}	Clock fall time	—	10	ns	100 pF $\geq C_L$ (7 cards)
t_{ISU}	Input setup time	5	—	ns	25 pF $\geq C_L$ (1 card)
t_{IH}	Input hold time	5	—	ns	25 pF $\geq C_L$ (1 card)
$t_{O_DLY (min)}$	Output delay time during data transfer mode	0	14	ns	25 pF $\geq C_L$ (1 card)
$t_{O_DLY (max)}$	Output delay time during identification mode	0	50	ns	25 pF $\geq C_L$ (1 card)

External 32 KHz Input Clock Timing



Symbol	Description	Min	Typ	Max	Unit
CK1	Frequency	—	32.768	—	KHz
CK2	Fall time	—	—	100	ns
CK3	Rise time	—	—	100	ns
CK4	Duty cycle (high-to-low ratio)	30	—	70	%
CK5	Frequency stability	-50	—	50	ppm
CK6	Input high voltage	$V_{dd18} - 0.6$	—	$V_{dd18} + 0.3$	V
CK7	Input low voltage	-0.3	—	0.55	V

The power up/power down sequence for the AR6001(AR6031)GZ



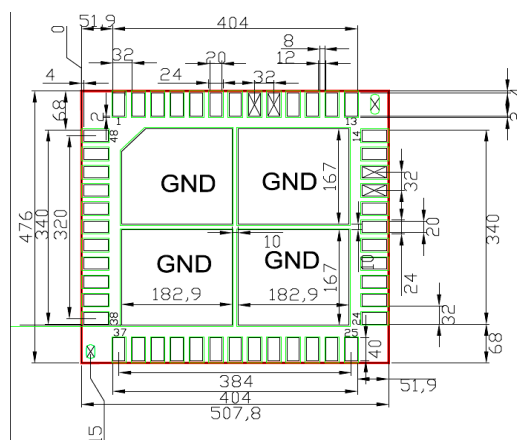
A	SYS_RST_L may be high or low; 3 V, 1.8 V, CHIP_PWD are low
B	3 V is high (90%) and CHIP_PWD is asserted simultaneous to 3 V
C	SYS_RST_L asserts at least T_b before 1.8 V is high, placing the AR6001GZ in reset
D ^[1]	1.8 V is high at least T_a after 3 V is high
E	CHIP_PWD de-asserts at least T_c after 1.8 V is high
F	SYS_RST_L de-asserts at least T_d after 1.8 V is high and at least T_e after CHIP_PWD de-asserts
G	CHIP_PWD asserts at least T_f before 1.8 V is powered down
H ^[1]	1.8 V is low at least T_g before 3 V is low
J	3 V is low

[1] T_a or T_g may be substituted by the condition where the 1.8 V supply is always no more than 0.3 V higher than the 3 V supply.

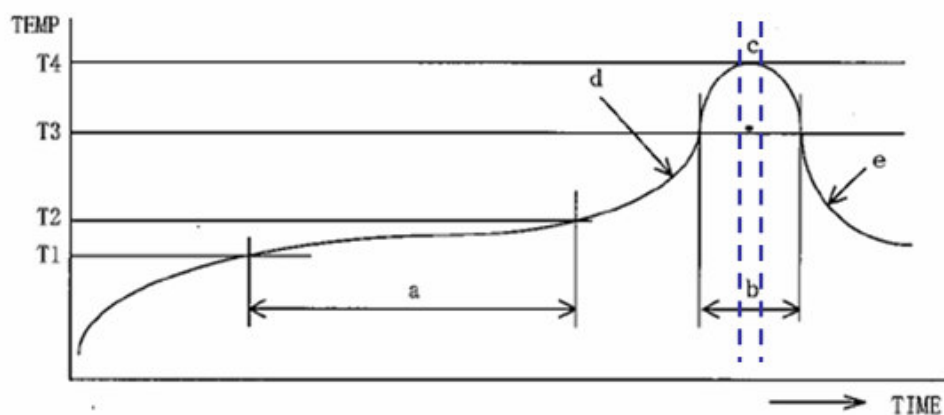
Layout Guideline

RF output (Pin-24)

1. RF traces are to be 50Ω and must not have sharp bends(90°) unless otherwise noted.
2. Via should be avoided in the RF traces.
3. Do not use any test points on RF trace or component.
4. Minimize lengths of RF traces
5. **GND pad must connect to main board ground to ensure RF performance.**



Re-flow Soldering Conditions (Reference)



(1) High temperature reflow-soldering conditions (No more than 2 flows allowed)

T1 : 150 , T2 : 180℃ , T3 : 230℃ , T4 : 260℃

a : Preheating 60 to 120 seconds

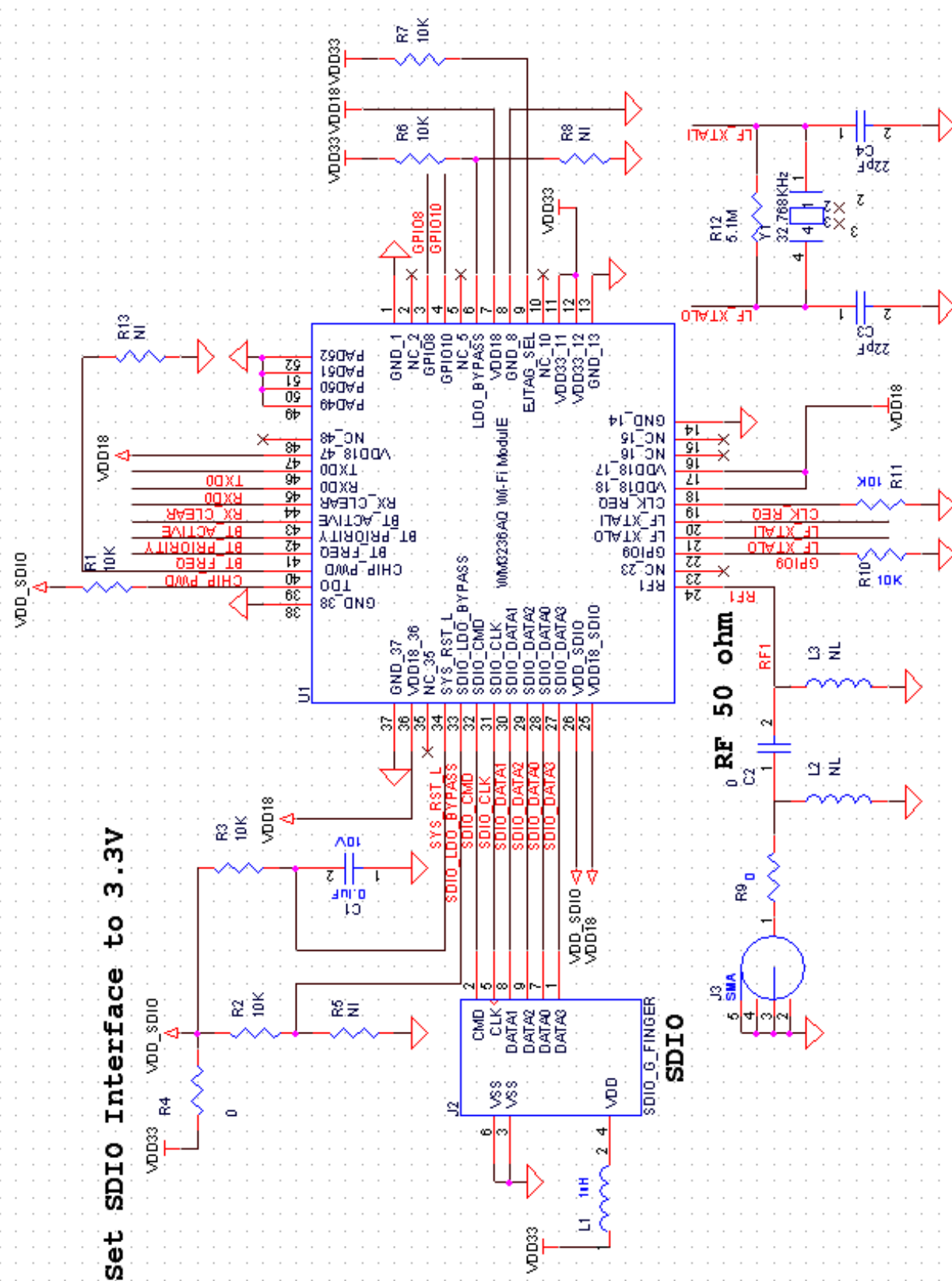
b : Heating 30 to 50 seconds

c : Peak temperature $260 \pm 5^\circ\text{C}$, 5 to 10 seconds

d : Temperature rising slope $10^\circ\text{C}/1 \text{ second}$, max.

e : Temperature falling slope $8^\circ\text{C}/1 \text{ second}$, max.

Application circuit



Application circuit appendix

LDO	LDO BYPASS	SDIO LDO BYPASS
Disable	HIGH	HIGH
Enable	LOW	LOW

When Internal LDO is disabled, system must supply 1.8V to VDD18 and VDD18_SDIO

ROM
R7 = 10K
R11 = 10K

FLASH
R7 = NI
R11 = 10K

VDD_SDIO (Pin-26) - Digital power supply for:
SDIO_CLK, SDIO_CMD,
SDIO_DATA_0, SDIO_DATA_1,
SDIO_DATA_2, SDIO_DATA_3,
SDIO_LDO_BYPASS, CLK_REQ, SYS_RST_L,
CHIP_PWD, TDO, GPIO9

WM3236AQ Product Specifications (TBD)

Physical	
Dimensions	12.9 mm x 12.1 mm x 1.25mm
Package	SiP QFN(LGA) Package
Operating Temperature	0 - 50 C
Storage Temperature	-20 - 70 C
Chipset Solution	
Chipset	Atheros AR6001 MAC/BB/RF/CPU + RF FEM
Host Interface	SDIO
Standards Conformance	IEEE 802.11b/g
Operating Voltage	3.3/1.8 V
Package	CSP
Baseband	
Modulations	DSSS (b), OFDM w/ BPSK, QPSK, 16QAM, 64QAM, CCK (g)
Media Access Technique	CSMA/CD
Radio	
Frequency Bands	2.412GHz – 2.484GHz (802.11b/g)
RF Transmit Output Power	14dBm (3.3V, 64QAM, -25dB EVM) (TBD)
Receive Sensitivity	-67dBm@54Mbps(TYP), -84dBm@11Mbps (TBD)
Data Throughput	
Throughput	17Mbps/16Mbps (TBD) -- x86 PC Linux Fedora Core 3 w/ PCI-SDIO card 7Mbps/5Mbps – Mio P350 PDA, WinMobile 5.0,SDIO (Platform depends)
Power Consumption	
Transmit, 15dBm	660mW (TYP)
Receive	450mW (TYP)
Sleep	<5mW (TYP)
Security Features	
Security	WEP 64/128, WPA (TKIP), WPA2 (802.11i)
Software	
Operating System	Linux 2.4/2.6, WinCE, Win Mobile 5.0, (Can be ported to other OS by contract)
Wireless Mode	AP-infrastructure, Ad-hoc
Utility	Configure wireless mode (AP-infrastructure, Ad-hoc) Configure security mode Manage security keys Select operating channel Set SSID, site survey, and profile manager View user configuration Receive signal quality and connection status

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