Glamo 3362 Command Queue

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Contents

1. Overview

1. The Command Queue has two parts, Soft Queue (SQ) and Hard Queue (HQ). Both of two queues are the FIFO to store the commands. The HQ means the data stores in the hardware circuit, it’s implemented by F.F. (Flip Flop). The data of SQ stores in the memory (SRAM), and the hardware controller will read the command from memory.
2. There are two modes of command queue, one is LFB Queue, and one is MMIO mode.
3. There are two types of command, one is single command, and one is burst command.
4. MMIO mode only loads single command, no burst command.
5. If MMIO mode is behind LFB mode, the drivers must wait queue (SQ & HQ) empty. Only when queue empty, queue mode can be switch.
6. Software driver must issue the command be written to LFB buffer on word (16 bits) boundary while updating the write pointer.

2. Register Definition

Register	I/O Address
Soft Queue Base Address Register 1	1600
Soft Queue Base Address Register 2	1602
Soft Queue Length Register	1604
Soft Queue Write Pointer Register 1	1606
Soft Queue Write Pointer Register	1608
Flip Index Register	160A
Command Queue Control Register	160C
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Soft Queue Base Address Register 1

Read/Write Port: 1600h

Default Value: 0000h

Field	Bits	Type	Description
SQBassAdr	15:0	RW	Soft Queue Base Address [15:0] The lower word of base linear address of soft queue in byte. *Limit:* The address range of soft queue is from 0 to 8M. *Limit:* It must align at word (16 bits) boundary, and the bit 0 is always zero for word boundary alignment.

Soft Queue Base Address Register 2

Read/Write Port: 1602h

Default Value: 0000h

Field	Bits	Type	Description
-	15:7	-	n/a
SQBassAdr	6:0	RW	Soft Queue Base Address [22:16] The higher word of base linear address of soft queue in byte. *Limit:* The address range of soft queue is from 0 to 8M.

Soft Queue Length Register

Read/Write Port: 1604h

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	n/a
SQLength	8:0	RW	Soft Queue Length [8:0] The length of Soft Queue in 1K bytes. *Limit:* The length of soft queue is from 1 to 512K. *Notes:* For example, if set the soft queue length is 0, the actual size of soft queue is 1K. If set the soft queue length is 3, the actual size of soft queue is (3+1)*1024=4096 bytes.

Soft Queue Write Pointer Register 1

Read/Write Port: 1606h

Default Value: 0000h

Field	Bits	Type	Description
SQWrPtr	15:0	RW	Soft Queue Write Pointer [15:0] The write pointer for Soft Queue. *Limit:* The write pointer of soft queue is from 0 to 512K. *Limit:* It must align at word boundary, and the bit 0 is always zero for word boundary alignment. *Notes:* Because the write pointer has 19 bits, there are two write requests to set it. To avoid setting the temporary value between two write requests, it should be write the bit [18:16] and [15:0] sequentially. Set the bit [18:16] to write the higher word of write pointer, and then set the bit [15:0] to update the hardware's write pointer.

Soft Queue Write Pointer Register 2

Read/Write Port: 1608h

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	n/a
SQWrPtr	2:0	RW	Soft Queue Write Pointer [18:16] The write pointer for Soft Queue.

			Limit: The write pointer of soft queue is from 0 to 512K.

Flip Index Register

Read/Write Port: 160Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	n/a
ISP Busy enable	2	RW	Force ISP Busy enable(A1ECO)
Flip Index	1:0	RW	Flip Index [1:0] *Notes:* when the decoder of command queue decodes which it is flip command, the command queue will puts the index number to the flip queue. *Notes:* when the mode of command buffer is soft queue buffer mode, the flip command should put in the soft queue instead of MMIO command. When the mode of command buffer is MMIO mode, the flip command is from MMIO command.

Command Queue Control Register

Read/Write Port: 160Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	n/a
TurboFlip	12	RW	Turbo Flip (see Appendix B, item 5) 0 Disable 1 Enable
FlipMode	11	RW	Flip Buffer Mode (see Appendix B, item 5) 0 Two buffers 1 Triple buffers
Interrupt	10:8	RW	Interrupt 000 wait 2D idle 001 wait 3D idle 010 wait HQ empty 011 wait SQ empty 100 wait 2D idle, 3D idle, HQ, and SQ empty Others no action
HQThreshold	7:4	RW	HQ threshold value [3:0] Maximum value is “1111”
CmdType	3	RW	Command Type (See Appendix A)

			0 Compact Commands 1 Command with header
EnAutoCorrect	2	RW	Enable Command Queue Auto-Correction Function. 0 Disable 1 Enable
CmdQMode	1	RW	Command Buffer Mode 0 Soft Queue Buffer Mode 1 MMIO Mode
CmdQSyncRst	0	RW	Command Queue Synchronous Reset Register 0 Normal Operation 1 Reset

Soft Queue Read Pointer Register 1

Read/Write Port: 160Eh

Default Value: 0000h

Field	Bits	Type	Description
SQRdPtr	15:0	RW	The read pointer for Soft Queue. *Limit:* The read pointer of soft queue is from 0 to 512K. *Limit:* It must align at word boundary, and the bit 0 is always zero for word boundary alignment. *Notes:* Because the read pointer has 19 bits, there are two read requests to get it. To avoid getting the temporary value between two read requests, it should be read the bit [15:0] and [18:16] sequentially. Read the bit [15:0] to latch the hardware read pointer, then read the bit [18:16] to get previous latched data.

Soft Queue Read Pointer Register 2

Read/Write Port: 1610h

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	n/a
SQRdPtr	2:0	RW	Soft Queue Read Pointer [18:16] The read pointer for Soft Queue. *Limit:* The read pointer of soft queue is from 0 to 512K.

Command Queue Status Register

Read/Write Port: 1612h

Default Value: 0000h

Field	Bits	Type	Description
-	15:7	-	n/a
ISP Busy	8	RW	ISP Busy 0 ISP idle 1 ISP busy
Capture Busy	7	RW	CAP Busy 0 CAP idle 1 CAP busy
FlipQEmpty	6	RW	Flip Q empty 0 queue not empty 1 queue empty
3DBusy	5	RW	3D Busy 0 3D idle 1 3D busy
2DBusy	4	RW	2D Busy 0 2D idle 1 2D busy
CmdQFail	3	RW	Command Queue Decode Fail 0 Fails occurs more than one time. 1 No Fails Occurs.
AllIdle	2	RW	2D idle, 3D idle, HQ, SQ and flip queue empty 0 Busy or Not Empty 1 Idle and Empty
HQEmpty	1	RW	H/W CQ Empty 0 Not Empty 1 Empty
SQEmpty	0	RW	S/W CQ Empty 0 Not Empty 1 Empty

Appendix A. Data Structure of Commands Types

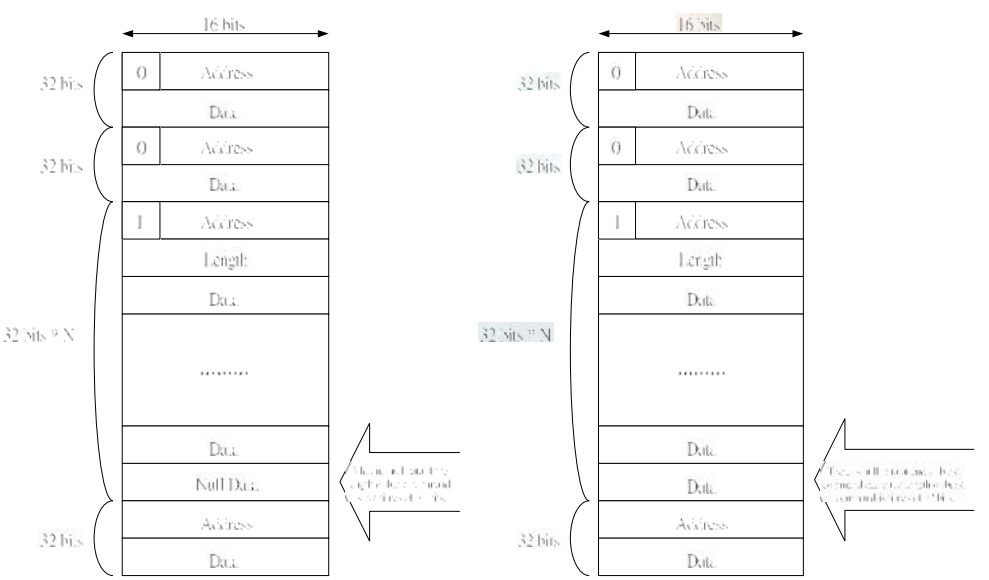
There are two types of command, one is compact command, and one is command with header. The compact command has no header for each sub-types of command. The command with header is as implied by the name, it has header definition for each sub-types of command.

Type 1: Compact Command

The compact command has two types of command, one is single command, and one is burst command. Both of two commands have one bit to indicate the command type. If the bit 15 of address field is 0, it is a single command. If the bit 15 is 1, it is a burst command. The address filed must align at double word (32 bits) boundary, so the burst command of total length must be the times of 32 bits. If the length of burst command is not times of 32 bits, the software driver must add one null data to the end of burst command.

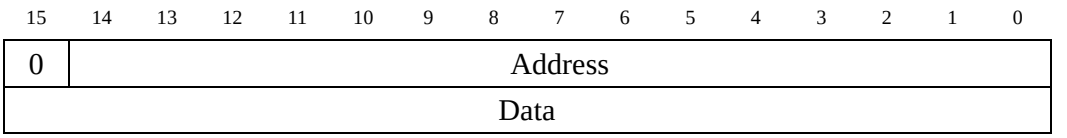
An Example:

By the following example, it adds one null data to the end of burst command.

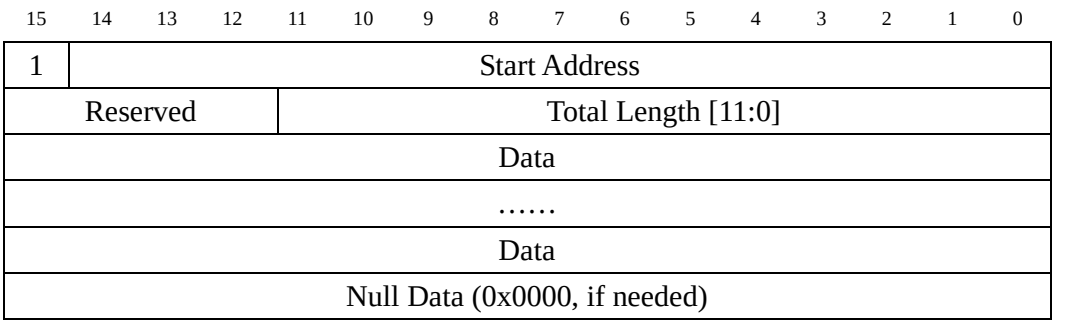


The definition of two commands type:

A. Single Command



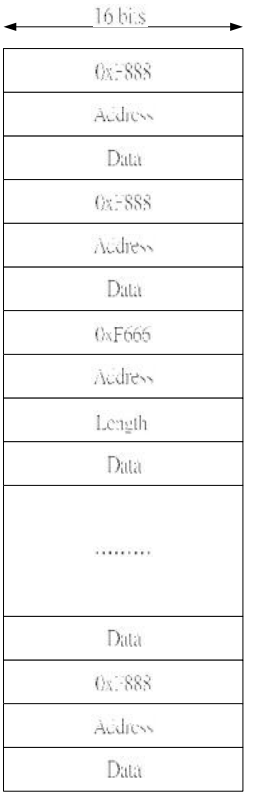
B. Burst Command



Type 2: Command with Header

The command with header also has two types of command, one is single command, and one is burst command. These two commands type has one 16 bits header to indicate commands type. For each filed of command (includes header, address, length, and data) must align at word boundary. It DOSE NOT need to add any null command at end of burst command.

An Example:



The definition of two commands types:

A. Single Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xF888 (Header)															
Address															
Data															

B. Burst Command

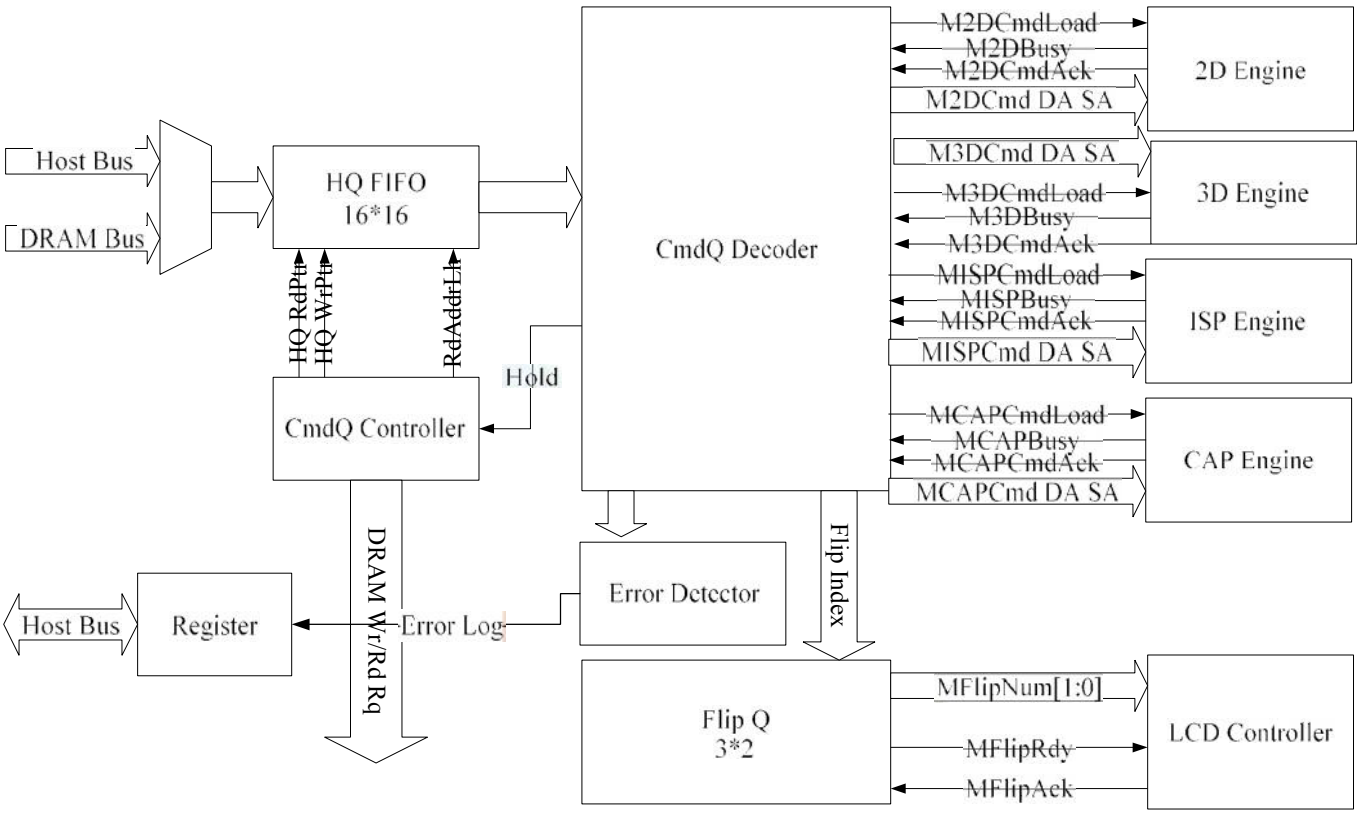
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xF666(Header)															
Start Address															
Reserved				Total Length [11:0]											
Data															
……															
Data															

Appendix B. Programming Notes

1. The definition of queue empty or full for software driver:
   A. Queue empty: if (Read_Pointer == Write_Pointer && HQ_Empty)
   B. Queue full: if (Read_Pointer == Write_Pointer + 1)
2. Software driver must issue the command be written to LFB buffer on word boundary while updating the write pointer.
3. Command Queue hold happens when:
   A. 2D Command Mode
      I. No acknowledgement when 2D Command is issued.
      II. 3D Engine Busy
      III. Flip Q Full
   B. 3D Command Mode
      I. 2D Engine Busy
      II. No acknowledgement when 3D Command is issued.
      III. Flip Q Full
4. Flip Queue hold happens when:
   A. 2D Engine Busy
   B. 3D Engine Busy
   C. Flip Q Full
5. Pseudo Code for Flip Q Full

```
If (TurboFlip == 1) {
   If (LengthOfFlipQueue == 3) {
      FlipQFull = 1;
   } else {
      FlipQFull = 0;
   }
} else {
   If (BufferModes == TwoBuffers && LengthOfFlipQueue == 1) {
      FlipQFull = 1;
   } else if (BufferModes == TripleBuffers && LengthOfFlipQueue == 2) {
      FlipQFull = 1;
   } else {
      FlipQFull = 0;
   }
}
```

6. Command Queue Architecture



7. Add Packet or Index Mode for 3D
   If the address is **FD00**, it's for 3D packet or index command. It's always in burst command.
8. The range of the total length in burst command mode is 11 down to 0.
9. To update write pointer of CQ, the driver should disable the gating clock of CQ's MCLK, and update the write pointer of CQ, the enable the gating clock of CQ's MCLK. (Add on 2004.04.22)
10. The *null command* is 0x0000 on the address filed on the P3362 or latter project, and the *null command* is any of read only MMIO address (eg. 0x173C) on the address filed on the P360.
11. Add dummy command "0x0000"

Appendix C. Software Patch

Modified P360 bugs. No needs to patch.