Glamo 3362

The Multimedia co-Processor for Mobile

Ver. 1.0

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Content

1 Product Overview

1.1 Introduction

As the speed of handheld devices increases with breathtaking pace, the mobile phone has become a vital necessity in our lives, improving and enhancing communication, while also providing a digital camera, game and video recorder. The Glamo 3362 is SMedia's latest mobile multimedia product that gives consumers a dizzying array of options to experience the digital world in all its glory. The Glamo 3362 supports today's most cutting edge multimedia functions including a 2D/3D graphic accelerator, MPEG-4 codec, JPEG codec and LCD controller. With SMedia's unique power management technology, battery life is effectively extended when running 2D/3D games and applications, and the digital camera and video recorder, making the Glamo 3362 chipset ideal choice for those demanding users who like to burn the midnight oil.

1.2 Overview

1.2.1 The High Performance Mobile GPU

The 3D hardware engine in Glamo 3362 is designed for the ultimate in mobile gaming performance, for users who need blistering gaming performance on the bus, train, beach, or anywhere else boredom strikes. Designed on the OpenGL ES 1.1, its performance reaches a smoking 1.54M triangles per second through SMedia's optimizing Transform and Lighting engine. With the capability of 8 lights simultaneously, 3 different lighting types and multiple textures in one cycle, the Glamo 3362 will give users a mind-glowing immersed 3D gaming experience that will make the most die hard gamers weep with joy. The 2D engine features a 50M filling rate per second and full functionality dealing with line, word and picture, making an unprecedented LCD monitor display, ideal for showing off embarrassing, shocking and hilarious photos of family and friends!

1.2.2 Powerful Image Processor

The Glamo 3362 boasts a 5M pixels digital photo resolution image processor. The MPEG-4 codec enables 30 frames per second in CIF resolution, providing an incredibly fluid and life-like image in the phone display. In Video Conference mode, Glamo 3362 can handle two differential images showing on one panel simultaneously. In addition, Glamo 3362 is able to support CIF resolution in video recording, allowing users to see each other with crystal clarity. Of course, the Glamo 3362 is fully compatible with H.263.

The Glamo 3362 supports CSTN and TFT LCD panels, allowing customer to choose the best solution for their particular market. As well, the display also can rotate 90/180/270 mirror mode and dual display mode, depending on user's needs.

1.2.3 Powerful MPEG-4 and JPEG Engine

The MPEG-4 engine in the Glamo 3362 gives users the ability to record/play video at any time, anywhere. Users can record a video clip in H.263 format and then transmit to their friends by MMS, or play received video clip. The MPEG-4 format can achieve higher compression ratio than H.263, so users can use their mobile phone as a digital video recorder to record high quality video (352x288 pixel, 30 fps) as long as they want, the only limitation is the storage space. The advanced rate-control algorithm and the intelligent mode decision algorithm can incredibly increase the visual quality of video while remaining the high compression ratio. The ultimate application of the Glamo 3362 MPEG-4 encoder and decoder engine is to support videophone, gives users and their friends to communicate with not only voice, but also video.

Using the JPEG encoder engine built on Glamo 3362, users can capture images with size over 5M pixels, compress to different quality according to their desire, and then store in the MMC/SD memory card or transmit to friends. With the ISP engine, the JPEG decoder can decode the JPEG file and then scale to any sizes on the fly.

1.2.4 On-chip Frame Buffer and Flexible Clock Scheme

The Glamo 3362 has built-in 16M bits on-chip frame buffer. It is useful for 2D and 3D application. It can support resolution up to 640x480 16bpp for double or triple buffers.

The Glamo 3362 has build-in a clock synthesizer to generate all internal clocks. The clock synthesizer can generate wide range of programmable frequencies. It can provide 1MHz to 90MHz flexible working frequency. The clock synthesizer accepts 32 KHz or 13 MHz reference clock input, which depends on the trapping value of CFG3. And system can even stop the reference clock after the PLL locked the target frequency and phase for power saving.

1.2.5 Optimizes Power Management

Because users often blame battery life of their mobile phones excessively during extreme gaming sessions and heated phone conversations, the Glamo 3362 adds many extra power-saving methods to extend battery life. In power-saving mode, the partial display extends battery life. Compared with software solutions, the Glamo 3362 hardware solution can reduce power consumption by at least 85% while still operating multimedia functions such as watching MPEG-4 videos, photo previewing, and playing 3D/2D games.

1.2.6 Rich Functionality in the Multimedia and Mobile Field

In order to satisfy various customers' demands, the Glamo 3362 can support all types of standard hardware and software specifications in the mobile phone industry. The Glamo 3362 is compatible with products such as CMOS, CCD, LCD, baseband processor or other components, and is well compatible with all products. SMedia not only satisfies all anticipated market demands, but also establishes precedents in mobile phone standards that will set the bar for mobile technologies higher, driving the industry to new heights of technological excellence.

1.3 Feature List

The following are the main features of the Glamo 3362:

Host Interface

- Supports 16 bits SRAM-like with variable latency host interface
- Supports addressing space up to 16 MB
- Supports four types of bus protocol
  - Type 1 direct addressing mode
  - Type 2 direct addressing mode
  - Type 3 iBurst (*Note 1) mode
  - Type 4 indirect addressing mode
- Supports LCD by-pass mode
- Memory read prefetch
- Supports interrupt
- Support burst mode
- Support frequency up to 75 MHz in burst mode

Display Interface

- 640x480 16/18 bpp (RGB565/RGB666) (*Note 2)
- Supports 6/9/16/18 bits RGB I/F and 8/9/16/18 bits CPU I/F
- Supports C-STN with frame buffer
- HW 90°/180°/270° rotate and mirror
- Supports TFT or TFD (with or without frame-buffer)
- Supports dual panels
- Supports three channel gamma correction
- Supports hardware cursor
- Supports partial display
- Supports by-pass mode
- Built-in power saving mode

- Support TV encoder interface

High Performance 2D Accelerator

- Fully compliant with the J2ME MIDP 2.0 2D requirement (Support J2ME/JSR-226 special rotation)
- Built-in an 1T pipelined 16bit BitBlt graphics engine
  - ROP3, rectangle fill, font expansion, line-drawing
  - Transparent BitBlt with source destination keys
  - Alpha blended BitBlt, clipping, stretch and shrink
  - Supports mirror/flip mode
  - Alpha Blending: Premultiply
  - AA text
  - Gradient fill
  - NTLine
  - Resolution: Max. 640x480
  - Supports HW 90°/180°/270° rotate
- Max. fill rate: 50 M pixels/sec.

High Performance 3D Accelerator

- Fully compliant with JSR-000184 mobile 3D graphics API for J2ME™
- Fully compliant with OpenGL ES v1.0 and 1.1
- Mobile D3D supported
- Max. 3D resolution: 511x511
- Built-in pipelined 3D primitive engine
  - Supports Geometry, lighting, clipping and texture transform
  - 8 active lights (point, directional and spot light) with spectacular and fog
  - Supports Back face culling and texture transform
  - Supports two side lighting
  - Supports linear, EXP and EXP2 vertex fog
  - Supports triangle, line and point primitive type
  - Supports primitive list, strip and fan input
  - Supports multi-stream for VBO

- Supports user clipping plane

- Built-in pipelined 3D setup engine
  - Supports float-point
  - Supports texture wrap correction
  - Supports polygon offset
- Built-in pipelined 3D graphics engine
  - Supports multiple texture up to two textures
  - Supports per pixel perspective corrected texture mapping
  - Supports MIP structure, MIPMAPLOD bias
  - Supports all of the filtering method (point, linear, bi-linear, NMN, NML, LMN, LML filtering)
  - Texture transparency, blending, wrapping, mirroring
  - Supports palette texture and 8/16 bits ARGB, AL texture
  - Supports rectangle texture
  - Supports non power two texture size
  - Supports Dot Product 3 Bump Mapping
  - Supports texture size up to 256x256
  - Supports flat and Gouraud shading
  - 16 bits Z-buffer, Z test and Z bias
  - 8 bits stencil buffer and stencil test
  - Supports vertex fog and pixel fog (linear, EXP and EXP2)
  - Supports alpha blending and spectacular effects
  - Supports point and line width
  - Supports dithering and ROP
- Supports Max. fill rate: 50 M pixels/sec
- Supports polygon rate: 1.54 M polygons/sec

MPEG–4 Engine

- Fully compliant with ISO/IEC 14496-2 (MPEG-4) video simple profile level 0, 1, 2, 3
- Fully compliant with ITU-T recommendation H.263 profile 0 level 10, 20, 30, 40
- H.263/MPEG-4 decode and encode

- Supports up to CIF 30 fps, 2 Mbps; VGA decoding up to 20fps (*Note 3)
- Supports constant bit rate (CBR) and variable bit rate (VBR)
- Advanced rate-control algorithm with HVS (human visual system) support
- Intelligent mode decision algorithm to increase coding quality
- Deblocking
- Downloadable Huffman table
- Decode non-interleave scan

JPEG Engine

- Fully compliant with Baseline JPEG standard ISO/IEC 10918
- JPEG decode and encode
- Low pass filter for noise reduction
- Supports encode and decode JPEG image larger than 5M pixel

Video Interface

- Supports up to 5M pixels CMOS/CCD sensor input (*Note 4)
- Supports Bayer pattern and YUV422 input format
- 10-bit interface
- Supports 90°/180°/270° rotate & mirror & flip (*Note 5)

Image Signal Processing

- Exposure Control
  - Default modes: Auto, Spot, Center-Weighted, Scenery, Portrait, and Night-Shoot
  - User defined mode: Programmable by the user
  - Configurable exposure table by varying Shutter Speed, Aperture, and Gain
- White balance control
  - Default Modes: Auto, Indoor, Fluorescent, Outdoor
  - User Define Mode: Programmable by the User
  - Configurable white balance table
- Focus Control

- Default modes: Auto
- User define mode: Programmable by User
- Configurable focus table

- Authentic 16x continuous digital zoom
- Night-shoot mode enhancement
- Image effects
  - Color filter effects: Red, Green, Blue, Cyan, Magenta, Yellow
  - Monochrome
  - Negative
  - Emboss
  - Solarization
- Lens shading correction
  - Configurable shading correction table
  - Four channel
- Bad-pixel removal
  - Configurable bad-pixel position table
- Gamma/Tone-Curve correction
  - Configurable Gamma/Tone-Curve table
- Color enhancement
  - Configurable color correction matrix
  - Supports hue adjustment
  - Supports saturation adjustment
  - Supports brightness adjustment
  - Supports contrast adjustment
- 2-D edge-enhancement
- Image and video scaling engine for scaling up and down
  - 4-Tap scaling filter for both preview and JPEG/MPEG
  - Proprietary 1-input-2-output scaling engine
  - Configurable filter coefficients
- Supports picture overlay

- Dither engine

MMC/SD Interface

- Fully compliant with MMCA v3.3
- Compliant with low-voltage support and 4 bits data of MMCA v4.0
- Compliant with SD

PLL Interface

- Supports two wide range clock frequency synthesizers, one from 1 MHz to 50 MHz and the other from 1MHz to 90 MHz.
- Accepts 32 KHz or 13 MHz optional reference clock input
- Supports power down mode to turn off PLL for power saving

Package

- 160-Ball 8 mm x 8 mm x 1.3 mm LFBGA.

Note:

1. iBurst proprietary interface support Infineon S-GOLD2 series baseband processor.
2. 8MB-stacked Glamo 3362 will be needed if you would like to adopt 640x480 panel.
3. VGA size MPEG4 CODEC can only be implemented on those models stacked with at least 4MB memory.
4. 16 Mb is set to be the default local memory size in Glamo 3362. Be aware of that if you want higher resolution of either image sensor or display device, you will need higher density of memory size.

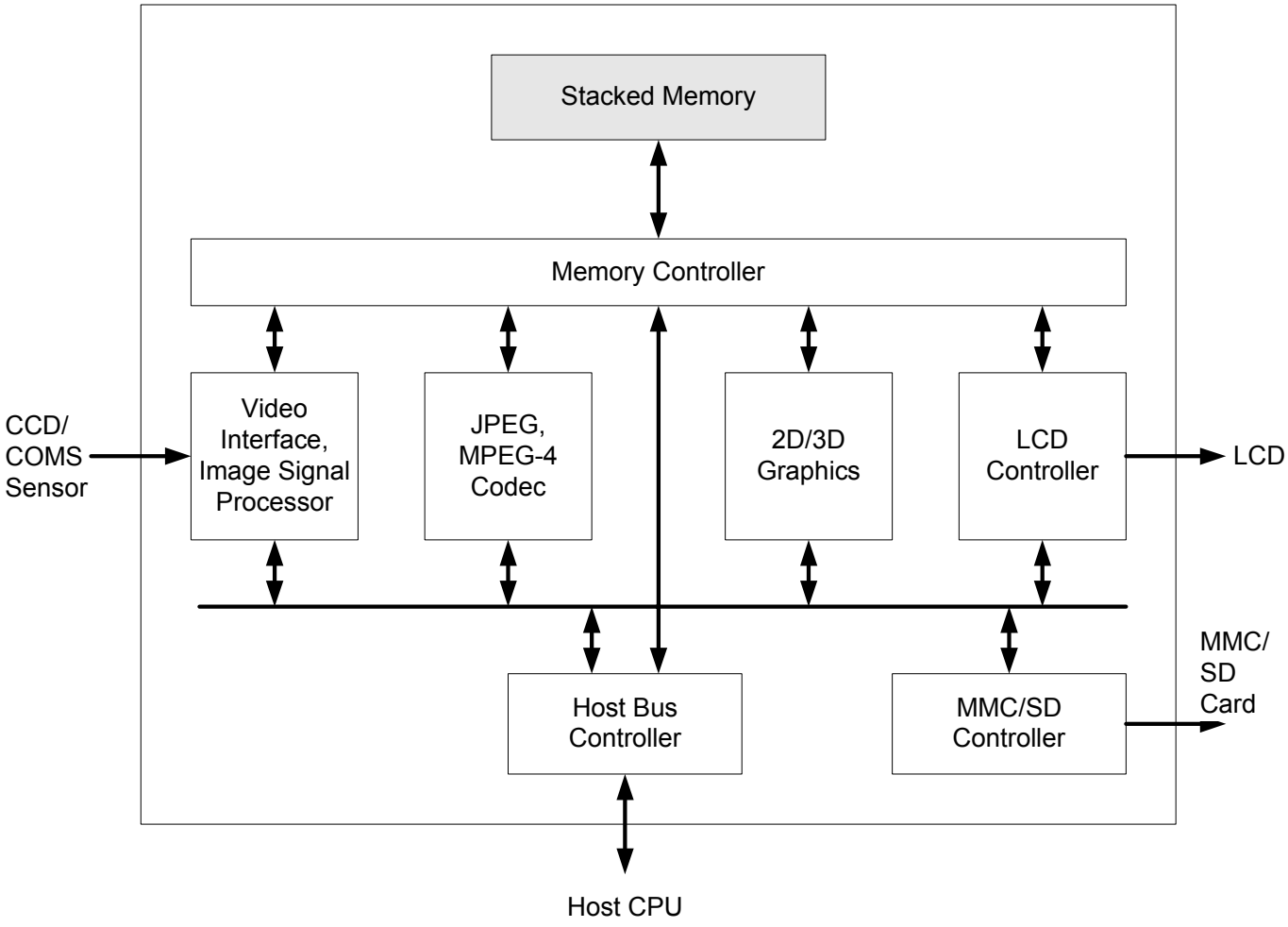
※ Maximum supporting resolution

	Bayer	***YUV***
2MB stacked	2M	<1M
4MB stacked	4M	2M
8MB stacked	5M	4M

5. In JPEG or MPEG mode, Glamo can support 180° & mirror & flip only.

1.4 Glamo 3362 Block Diagram

Figure 1.4-1 Glamo 3362 Block Diagram



2 Signal Descriptions

2.1 Introduction

This chapter describes and lists all of the Glamo 3362 pins. The sign (#) at the end of a signal indicates that the polarity of the signal is active-low. The pin types are classified as:

- P = power pin
- I = input pin
- O = output pin
- I/O = input/output pin

2.1.1 Internal Pull-Up Pins

The following pins are internally pulled up in the Glamo 3362:

- MMCCMD
- MMCDAT
- MMCDAT1
- MMCDAT2
- MMCDAT3

2.1.2 Default Value

The default value of pin is classified as:

- ‘I’ mark indicates this is input pin and the default value is depends on the input value.
- ‘O(0)’ mark indicates this is output pin and the default value is L.
- ‘O(1)’ mark indicates this is output pin and the default value is H.
- ‘O(U)’ mark indicates this is output pin and the default value is depends on the translated data
- ‘Highz’ mark indicates the pin with default no driving
- ‘Oper’ mark indicates this is IO pin and its’ I/O can be defined by system, the default value is depends on the system setting.

2.2 Host Interface

Host interface contains total 48 pins. Detail pin information is presented in Table 2.2-1.

Table 2.2-1 Host Interface Pin Descriptions

Ball Location	Pin Name	Type	Default (Reset)	Default (Sleep)	Power	Description
F3	HA1	I	-	-	HOVDD	Host interface address bus and allow up to 16MB addressable space.
F4	HA2	I	-	-	HOVDD	
F5	HA3	I	-	-	HOVDD	
G3	HA4	I	-	-	HOVDD	
G2	HA5	I	-	-	HOVDD	
H5	HA6	I	-	-	HOVDD	
H4	HA7	I	-	-	HOVDD	
H3	HA8	I	-	-	HOVDD	
H2	HA9	I	-	-	HOVDD	
H1	HA10	I	-	-	HOVDD	
J5	HA11	I	-	-	HOVDD	
J4	HA12	I	-	-	HOVDD	
J3	HA13	I	-	-	HOVDD	
J2	HA14	I	-	-	HOVDD	
J1	HA15	I	-	-	HOVDD	
K5	HA16	I	-	-	HOVDD	
K4	HA17	I	-	-	HOVDD	
K3	HA18	I	-	-	HOVDD	
K1	HA19	I	-	-	HOVDD	
L4	HA20	I/O	-	I/Oper	HOVDD	This pin can be programmed as GPIO0 when using type 4 indirect addressing mode.

L3	HA21	I/O	-	I/Oper	HOVDD	This pin can be programmed as GPIO1 when using type 4 indirect addressing mode.
L2	HA22	I/O	-	I/Oper	HOVDD	This pin can be programmed as GPIO2 when using type 4 indirect addressing mode.
L1	HA23	I/O	-	I/Oper	HOVDD	This pin can be programmed as GPIO3 when using type 4 indirect addressing mode.
B3	HD0	I/O	-	-	HOVDD	Host interface bi-directional data bus.
C3	HD1	I/O	-	-	HOVDD	
A2	HD2	I/O	-	-	HOVDD	
B2	HD3	I/O	-	-	HOVDD	
B1	HD4	I/O	-	-	HOVDD	
C1	HD5	I/O	-	-	HOVDD	
C2	HD6	I/O	-	-	HOVDD	
D1	HD7	I/O	-	-	HOVDD	
D3	HD8	I/O	-	-	HOVDD	
D4	HD9	I/O	-	-	HOVDD	
E1	HD10	I/O	-	-	HOVDD	
E2	HD11	I/O	-	-	HOVDD	
E3	HD12	I/O	-	-	HOVDD	
E4	HD13	I/O	-	-	HOVDD	
E5	HD14	I/O	-	-	HOVDD	
F1	HD15	I/O	-	-	HOVDD	
B5	HCS#	I	-	-	HOVDD	Chip select input
C5	HRD#	I	-	-	HOVDD	Read command input
D5	HWR#	I	-	-	HOVDD	Write command input
A4	HWAIT#	O	Highz	Highz	HOVDD	Wait cycle insertion. During a data transfer, HWAIT# is driven active to force the baseband to insert wait state. It is driven inactive to indicate the completion of a data transfer.
C4	HLB#	I	-	-	HOVDD	Byte enable input for lower data byte (HD[7:0])

A3	HUB#	I	-	-	HOVDD	Byte enable input for higher data byte (HD[15:8])
A5	INT#	O	Highz	Highz	HOVDD	Interrupt output
F2	HCLK	I	-	-	HOVDD	Host clock
B4	HADV#	I/O	-	I/Oper	HOVDD	Address/Data valid bit This pin can be programmed as GPIO19.

2.3 LCD Interface

There are two modes supported by LCD interface:

- Mode 0: CPU interface
- Mode 1: RGB interface

LCD interface contains total 28 pins. Detail pin information is presented in Table 2.3-1.

Table 2.3-1 LCD Interface Pin Descriptions

Ball Location	Pin Name	Type	Default (Reset)	Default (Sleep)	Power	Description
M8	LCS0#	I/O	O(1)	O(1)	LOVDD	Mode 0: Chip select output for LCD1 Mode 1: Serial interface enable This pin can be programmed as GPIO4.
H10	LCS1#	I/O	O(1)	O(1)	LOVDD	Mode 0: Chip select output for LCD2 Mode 1: No used This pin can be programmed as GPIO5.
N8	LDCLK	I/O	O(0)	O(0)	LOVDD	Mode 0: No used Mode 1: Clock output This pin can be programmed as GPIO6.
K9	LDE#	I/O	O(1)	O(1)	LOVDD	Mode 0: Read enable for 80CPU Read or Write enable for 68 CPU Mode 1: Data enable output This pin can be programmed as GPIO7.
N10	LD0	O	O(U)	O(U)	LOVDD	B[0] data output

L11	LD1	O	O(U)	O(U)	LOVDD	B[1] data output
M11	LD2	O	O(U)	O(U)	LOVDD	B[2] data output
N11	LD3	O	O(U)	O(U)	LOVDD	B[3] data output
M12	LD4	O	O(U)	O(U)	LOVDD	B[4] data output
N12	LD5	O	O(U)	O(U)	LOVDD	B[5] data output
M13	LD6	O	O(U)	O(U)	LOVDD	G[0] data output
L13	LD7	O	O(U)	O(U)	LOVDD	G[1] data output
L12	LD8	O	O(U)	O(U)	LOVDD	G[2] data output
K13	LD9	O	O(U)	O(U)	LOVDD	G[3] data output
K12	LD10	O	O(U)	O(U)	LOVDD	G[4] data output
K11	LD11	O	O(U)	O(U)	LOVDD	G[5] data output
J13	LD12	O	O(U)	O(U)	LOVDD	R[0] data output
J12	LD13	O	O(U)	O(U)	LOVDD	R[1] data output
J11	LD14	O	O(U)	O(U)	LOVDD	R[2] data output
J10	LD15	O	O(U)	O(U)	LOVDD	R[3] data output
J9	LD16	I/O	O(U)	O(U)	LOVDD	R[4] data output This pin can be programmed as GPIO8.
H11	LD17	I/O	O(U)	O(U)	LOVDD	R[5] data output This pin can be programmed as GPIO9.
L9	LHSYNC	O	O(1)	O(1)	LOVDD	Mode 0: Control register & memory space select Mode 1: Horizontal sync output
M9	LVSYNC	O	O(1)	O(1)	LOVDD	Mode 0: Data write output Mode 1: Vertical sync output
N9	LSCK	I/O	O(1)	O(1)	LOVDD	Mode 0: No used Mode 1: Serial interface clock This pin can be programmed as GPIO10.
L10	LSDA	I/O	O(0)	O(0)	LOVDD	Mode 0: No used Mode 1: Serial interface data input/output

						This pin can be programmed as GPIO11.
M10	LSA0	I/O	O(0)	O(0)	LOVDD	Mode 0: No used Mode 1: Serial interface A0 output This pin can be programmed as GPIO12.
H9	TVCLK	I	-	-	LOVDD	Clock input for TV encoder

2.4 Camera Interface

Camera interface contains total 18 pins. Detail pin information is presented in Table 2.3-2.

Table 2.3-2 Camera Interface Pin Descriptions

Ball Location	Pin Name	Type	Default (Reset)	Default (Sleep)	Power	Description
E13	PCLK	I	-	-	COVDD	Pixel clock from sensor
D11	SCLK	O	highz	highz	COVDD	Output clock to sensor
D12	CSEN	O	highz	highz	COVDD	Serial interface enable
D13	CSCL	O	highz	highz	COVDD	Serial interface clock
C12	CSDA	I/O	-	-	COVDD	Serial interface data input/output
E9	CSGPO0	I/O	O(0)	I/Oper	COVDD	Sensor data input D[0] Serial interface general purpose output This pin can be programmed as GPIO13.
D9	CSGPO1	I/O	O(0)	I/Oper	COVDD	Sensor data input D[1] Serial interface general purpose output This pin can be programmed as GPIO14.
C13	CHSYNC	I	-	-	COVDD	Horizontal sync signal
B12	CVSYNC	I	-	-	COVDD	Vertical sync signal
B13	CD0	I	-	-	COVDD	Sensor data input D[9:2]
A12	CD1	I	-	-	COVDD	
B11	CD2	I	-	-	COVDD	

A11	CD3	I	-	-	COVDD	
D10	CD4	I	-	-	COVDD	
C10	CD5	I	-	-	COVDD	
B10	CD6	I	-	-	COVDD	
A10	CD7	I	-	-	COVDD	
C9	FLCTL	I/O	O(0)	O(0)/Oper	COVDD	Flash light control output This pin can be programmed as GPIO15.

2.5 Dedicated GPIO

Dedicated GPIO contains total 16 pins. Detail pin information is presented in Table 2.3-4.

Table 2.3-4 DGPIO Pin Descriptions

Ball Location	Pin Name	Type	Default (Reset)	Default (Sleep)	Power	Description
N3	DGPIO0	I/O	-	Oper	UOVDD	DGPIO 0 in group A
N4	DGPIO1	I/O	-	Oper	UOVDD	DGPIO 1 in group A
L7	DGPIO2	I/O	-	Oper	UOVDD	DGPIO 2 in group A
M7	DGPIO3	I/O	-	Oper	UOVDD	DGPIO 3 in group A
K8	DGPIO4	I/O	-	Oper	LOVDD	DGPIO 4 in LCD group
L8	DGPIO5	I/O	-	Oper	LOVDD	DGPIO 5 in LCD group
F9	DGPIO6	I/O	-	Oper	COVDD	DGPIO 6 in Sensor group
F10	DGPIO7	I/O	-	Oper	COVDD	DGPIO 7 in Sensor group
E10	DGPIO8	I/O	-	Oper	COVDD	DGPIO 8 in Sensor group
E11	DGPIO9	I/O	-	Oper	COVDD	DGPIO 9 in Sensor group
E12	DGPIO10	I/O	-	Oper	COVDD	DGPIO 10 in Sensor group
B9	DGPIO11	I/O	-	Oper	COVDD	DGPIO 11 in Sensor group
A9	DGPIO12	I/O	-	Oper	COVDD	DGPIO 12 in Sensor group
D8	DGPIO13	I/O	-	Oper	COVDD	DGPIO 13 in Sensor group
C8	DGPIO14	I/O	-	Oper	COVDD	DGPIO 14 in Sensor group

B8	DGPIO15	I/O	-	Oper	COVDD	DGPIO 15 in Sensor group

2.6 Miscellaneous

It contains total 13 miscellaneous pins. Detail pin information is presented in Table 2.3-5.

Table 2.3-5 Miscellaneous Pin Descriptions

Ball Location	Pin Name	Type	Default (Reset)	Default (Sleep)	Power	Description
A6	OSCI	I	-	-	AOVDD	32KHz reference clock for PLL or digital clock input
D6	RST#	I	-	-	HOVDD	Chip asynchronous reset signal
C6	ENTEST	I	-	-	HOVDD	Test mode enables. This pin should be connected with GND in normal operation.
H12	MMCCLK	O	O(0)	O(0)	TOVDD	Multimedia card interface CLK signal output
G12	MMCCMD	I/O	O(1)	O(1)	TOVDD	Multimedia card interface CMD signal
G11	MMCDAT	I/O	-	-	TOVDD	Multimedia card interface DAT signal
F11	MMCDAT1	I/O	-	Oper	TOVDD	Multimedia card interface DAT signal This pin can be programmed as GPIO16.
F12	MMCDAT2	I/O	-	Oper	TOVDD	Multimedia card interface DAT signal This pin can be programmed as GPIO17.
F13	MMCDAT3	I/O	-	Oper	TOVDD	Multimedia card interface DAT signal This pin can be programmed as GPIO18.
M3	CFG0	I	-	-	HOVDD	Configuration trap [3:0]
M2	CFG1	I	-	-	HOVDD	
M1	CFG2	I	-	-	HOVDD	
N2	CFG3	I	-	-	HOVDD	

2.7 Power

It contains total 30 power pins. Detail pin information is presented in Table 2.3-6.

Table 2.3-6 Power Pin Descriptions

Ball Location	Pin Name	Type	Power	Description
A1, A7, A13, N1, N7, N13	MOVDD	P	-	1.8 V power for Memory interface
D2, K2	HOVDD	P	-	1.8/3.3 V IO power for Host interface
C11	COVDD	P	-	1.8/3.3 V IO power for Camera interface
K10	LOVDD	P	-	1.8/3.3 V IO power for LCD interface
H13	TOVDD	P	-	1.8/3.3 V IO power for MMC interface
D7, G4, G10, K7	IVDD	P	-	1.8 V core power
B7	AIVDD1	P	-	1.8 V power for PLL1
C7	AIVDD2	P	-	1.8 V power for PLL2
B6	AOVDD	P	-	1.8/3.3 V IO power for OSCI
L5	UOVDD	P	-	1.8/3.3 V IO power for GPIO group A
E6, E7, E8, G1, G5, G9, G13, J6, J7, J8	VSS	P	-	Ground for core
A8	AIVSS	P	-	Analog ground for PLL

2.8 Pin Assignment

Figure 2.4-1 Top-Down View of Glamo 3362

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	MOVDD	HD2	HUB#	HWAIT#	INT#	OSCI	MOVDD	AIVSS	DGPIO12	CD7	CD3	CD1	MOVDD
B	HD4	HD3	HD0	HADV#	HCS#	AOVDD	AIVDD1	DGPIO15	DGPIO11	CD6	CD2	CVSYNC	CD0
C	HD5	HD6	HD1	HLB#	HRD#	ENTEST	AIVDD2	DGPIO14	FLCTL	CD5	COVDD	CSDA	CHSYNC
D	HD7	HOVDD	HD8	HD9	HWR#	RST#	IVDD	DGPIO13	CSGPO1	CD4	SCLK	CSE#	CSCL
E	HD10	HD11	HD12	HD13	HD14	VSS	VSS	VSS	CSGPO0	DGPIO8	DGPIO9	DGPIO10	P C L K
F	HD15	HCLK	HA1	HA2	HA3				DGPIO6	DGPIO7	MMCDAT1	MMCDAT2	MMCDAT3
G	VSS	HA5	HA4	IVDD	VSS				VSS	IVDD	MMCDAT	MMCCMD	VSS
H	HA10	HA9	HA8	HA7	HA6				TVCLK	LCS1#	LD17	MMCLK	TOVDD
J	HA15	HA14	HA13	HA12	HA11	VSS	VSS	VSS	LD16	LD15	LD14	LD13	LD12
K	HA19	HOVDD	HA18	HA17	HA16	NC	IVDD	DGPIO4	LDE#	LOVDD	LD11	LD10	LD9
L	HA23	HA22	HA21	HA20	UOVDD	NC	DGPIO2	DGPIO5	LHSYNC	LSDA	LD1	LD8	LD7
M	CFG2	CFG1	CFG0	NC	NC	NC	DGPIO3	LCS0#	LVSYNC	LSA0	LD2	LD4	LD6
N	MOVDD	CFG3	DGPIO0	DGPIO1	NC	NC	MOVDD	LDCLK	LSCK	LD0	LD3	LD5	MOVDD

Total ball: 160 Signal ball: 130 Power ball: 30

3 Interface Descriptions

3.1 Host Interface

3.1.1 Introduction

Mobile phone baseband processors use asynchronous SRAM-like interface to communicate outside device. The outside devices include SRAM, FLASH and the multimedia chip. Most of the interface only support slave mode, that is, CPU driven mode. And some of the interface may support wait state insertion. Glamo 3362 provides an asynchronous SRAM-like interface to communicate with most baseband processors. For getting better data transfer rate, it also supports a proprietary synchronous interface - iBurst.

There are eight types of bus protocol supported by Glamo 3362 host interface. By trapping CFG[1:0] to decide the bus protocol of the host interface. Refer to Table 3.1.1-1.

Table 3.1.1-1 Host Bus Type Table

CFG1	CFG0	HADVN	HA10	HCLK	Host Bus Type Description
0	0	0	A10	0	Direct addressing 16-bit 80 type 1
0	0	1	A10	0	Direct addressing 16-bit 80 type 2
0	0	N/A	A10	1	Direct addressing 16-bit 68 type
1	0	ADV	0	0	Indirect addressing 16-bit 80 type
1	0	ADV	0	1	Indirect addressing 16-bit 68 type
1	0	ADV	1	0	Indirect addressing 8-bit 80 type
1	0	ADV	1	1	Indirect addressing 8-bit 68 type
1	1	ADVN	N/A	Interface Clock	Synchronous iBurst type

3.1.2 Direct Addressing Mode 16 bits 80 type 1 Interface

Figure 3.1.2-1 Direct Addressing Mode 16 bits 80 Type 1 Interface Implementation

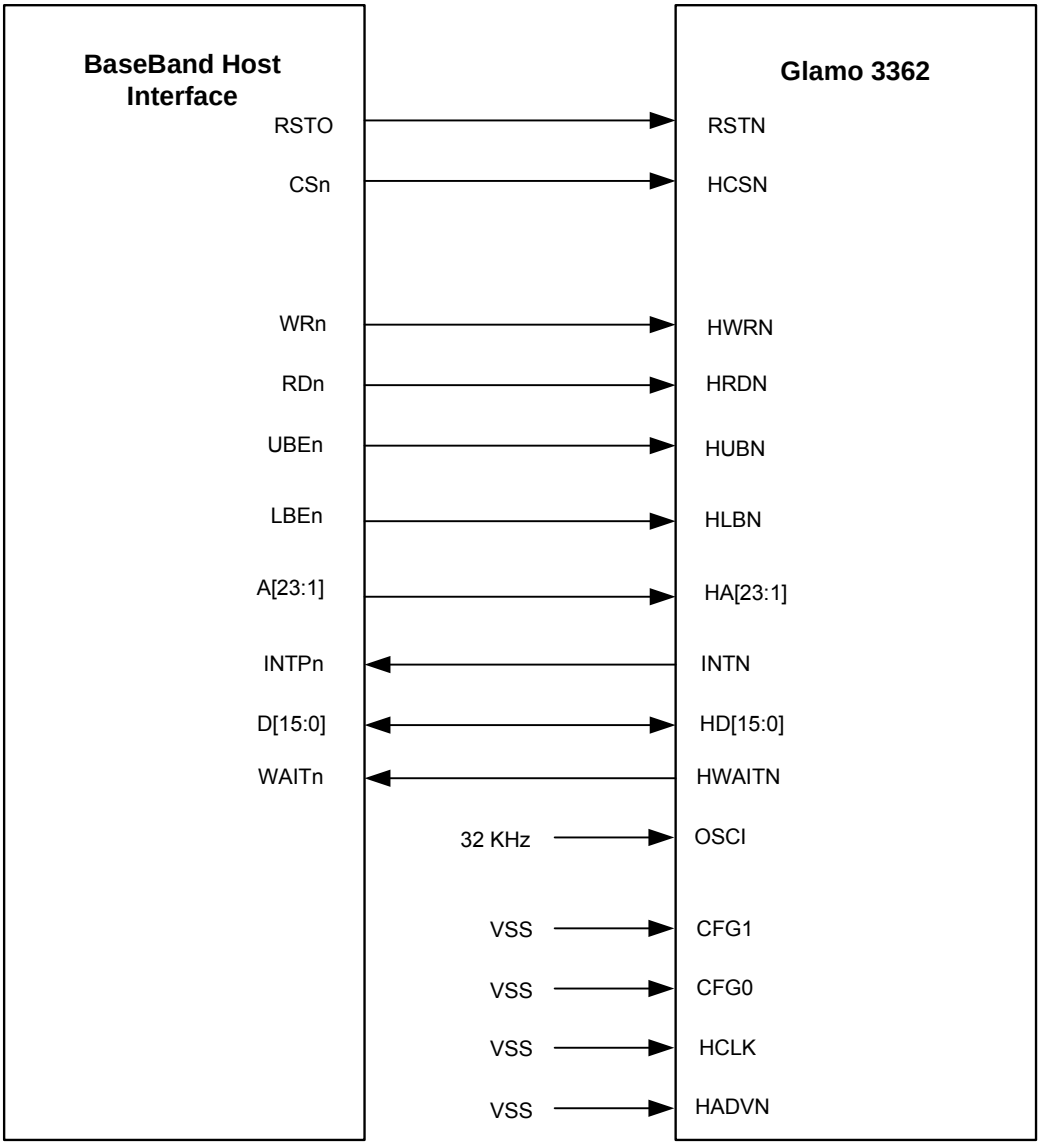


Figure 3.1.2-2 16 bits 80 Type 1 CPU Write Transaction

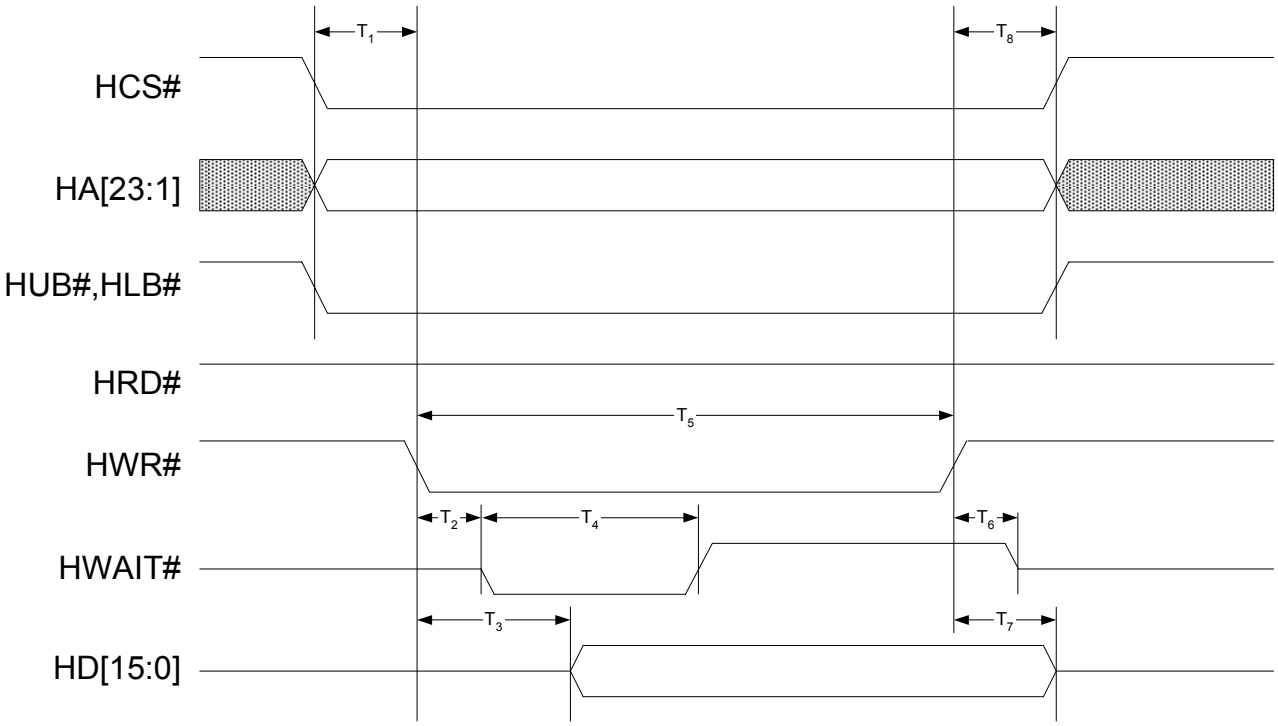


Figure 3.1.2-3 16 bits 80 Type 1 CPU Read Transaction

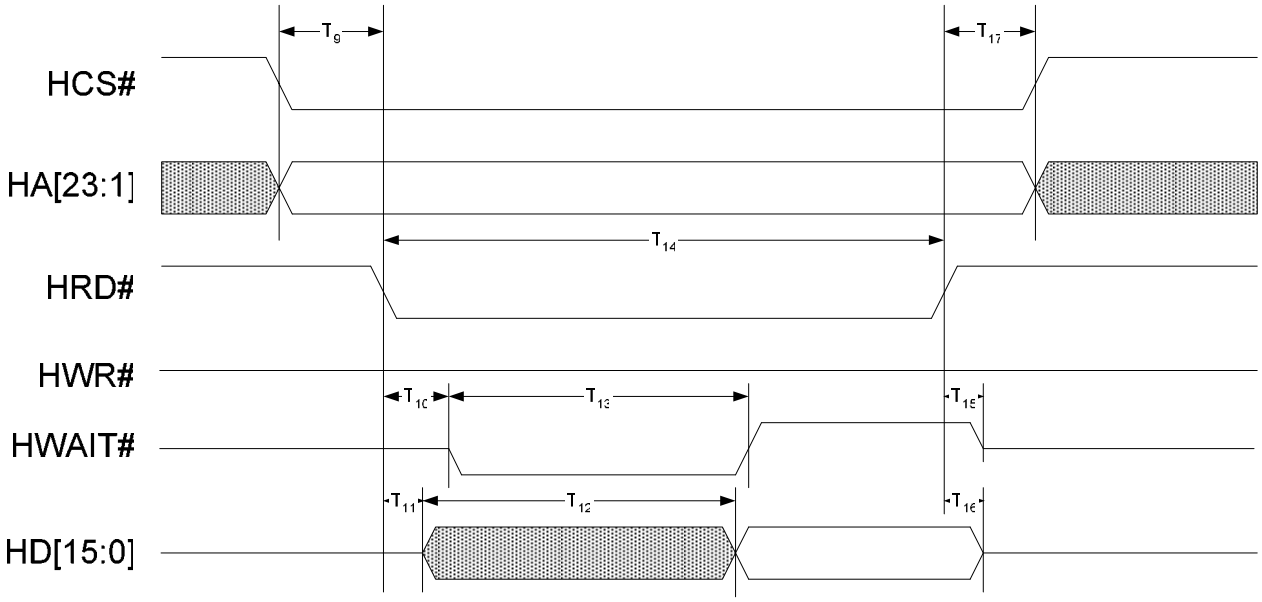


Table 3.1.2-1 Direct Addressing Mode 16 bits 80 Type 1 Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3	4	6.5	ns
T_7	Data hold time from write write rising edge	5			ns
T_8	Chip select, address and byte enable hold time from write rising edge	5			ns
T_9	Chip select, address and byte enable setup time from read falling edge	5			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4.0	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address and byte enable hold time from read rising edge	5			ns

Note:

1. See Table 3.1.2-2.

Table 3.1.2-2 Direct Addressing Mode 16 bits 80 Type 1 Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.3 Direct Addressing Mode 16 bits 80 type 2 Interface

Figure 3.1.3-1 Direct Addressing Mode 16 bits 80 Type 2 Interface Implementation

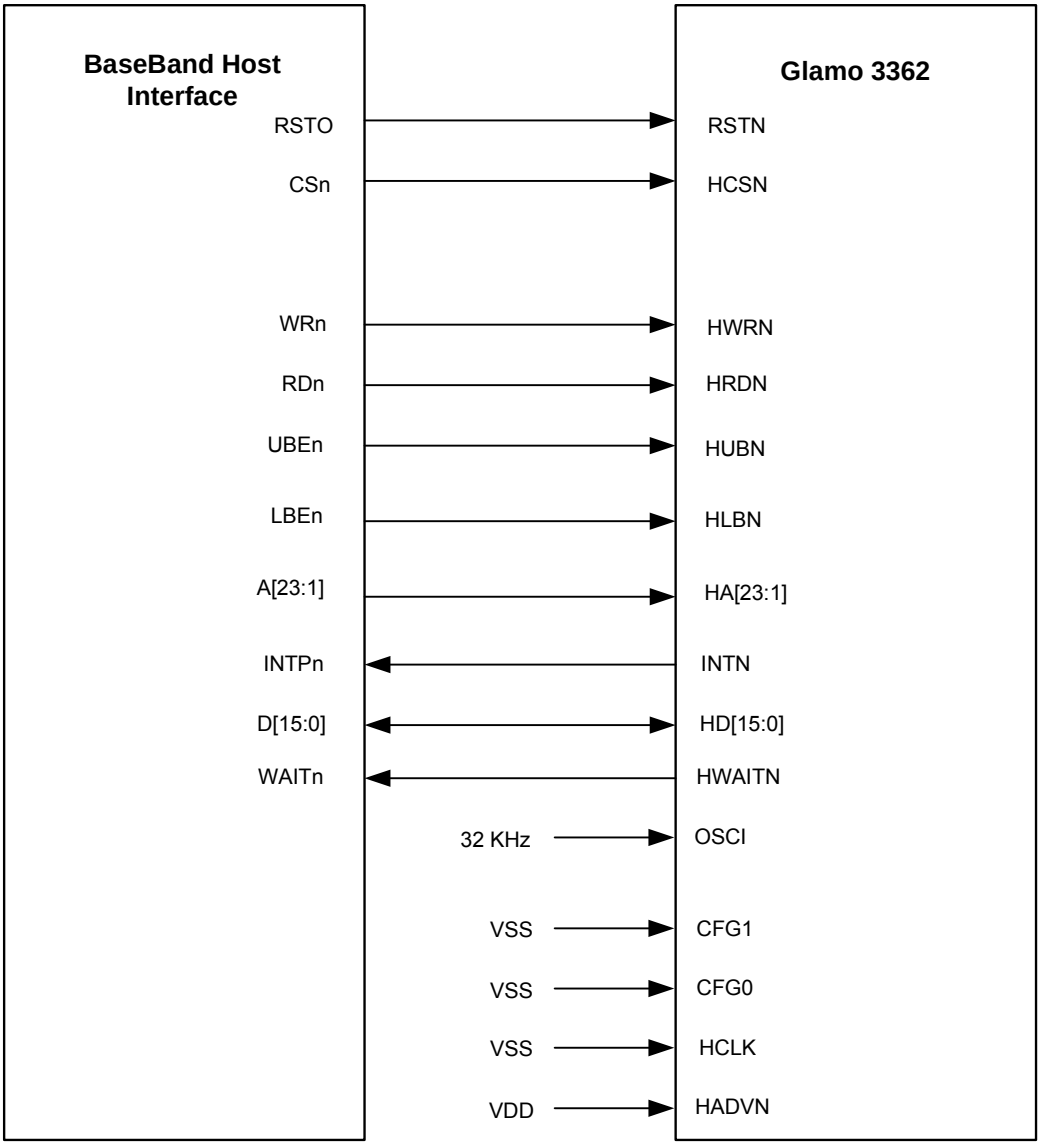


Figure 3.1.3-2 16 bits 80 Type 2 CPU Write Transaction

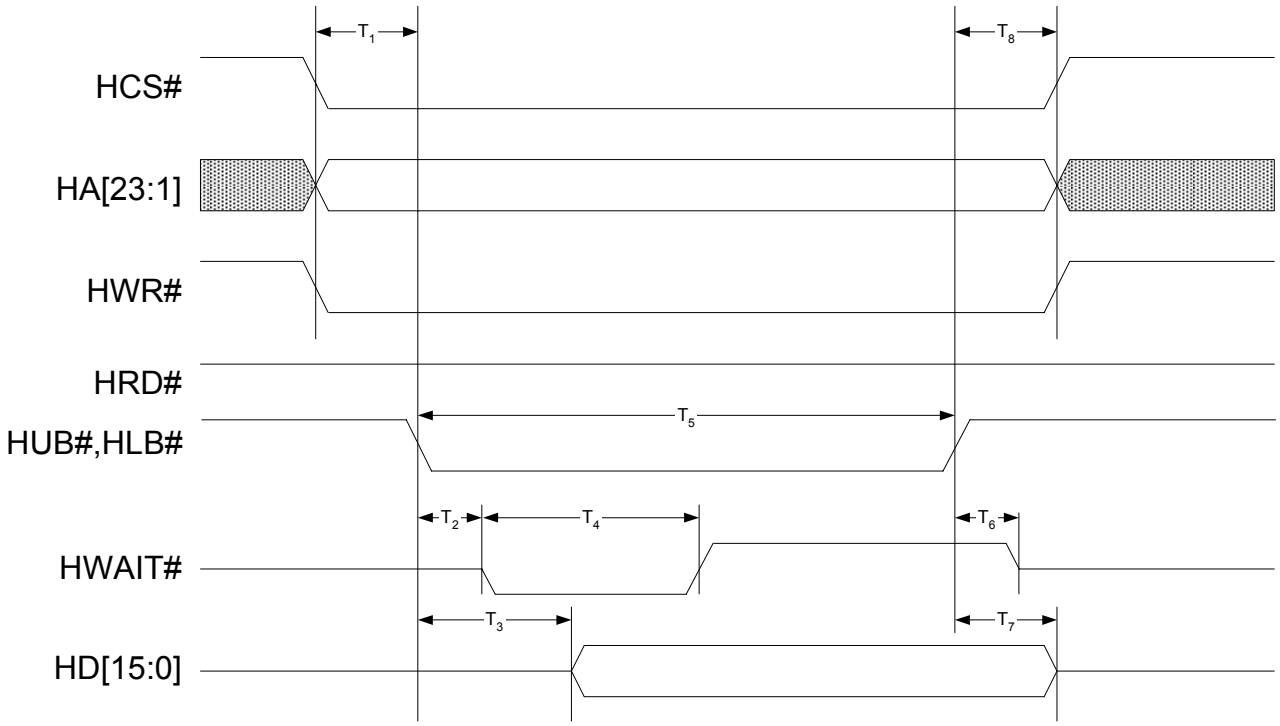


Figure 3.1.3-3 16 bits 80 Type 2 CPU Read Transaction

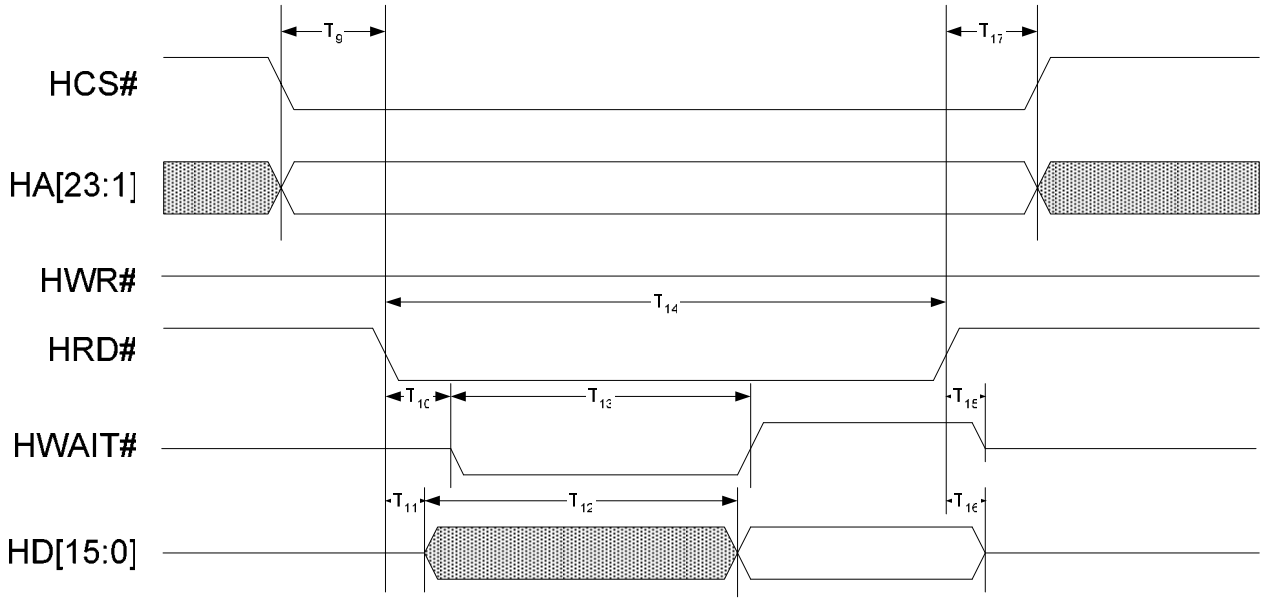


Table 3.1.3-1 Direct Addressing Mode 16 bits 80 Type 2 Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11.0	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3	4.0	6.5	ns
T_7	Data hold time from write write rising edge	5			ns
T_8	Chip select, address and byte enable hold time from write rising edge	5			ns
T_9	Chip select, address and byte enable setup time from read falling edge	5			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address and byte enable hold time from read rising edge	5			ns

Note:

1. See Table 3.1.3-2.

Table 3.1.3-2 Direct Addressing Mode 16 bits 80 Type 2 Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.4 Direct Addressing Mode 16 bits 68 Type Interface

Figure 3.1.4-1 Direct Addressing Mode 16 bits 68 Type Interface Implementation

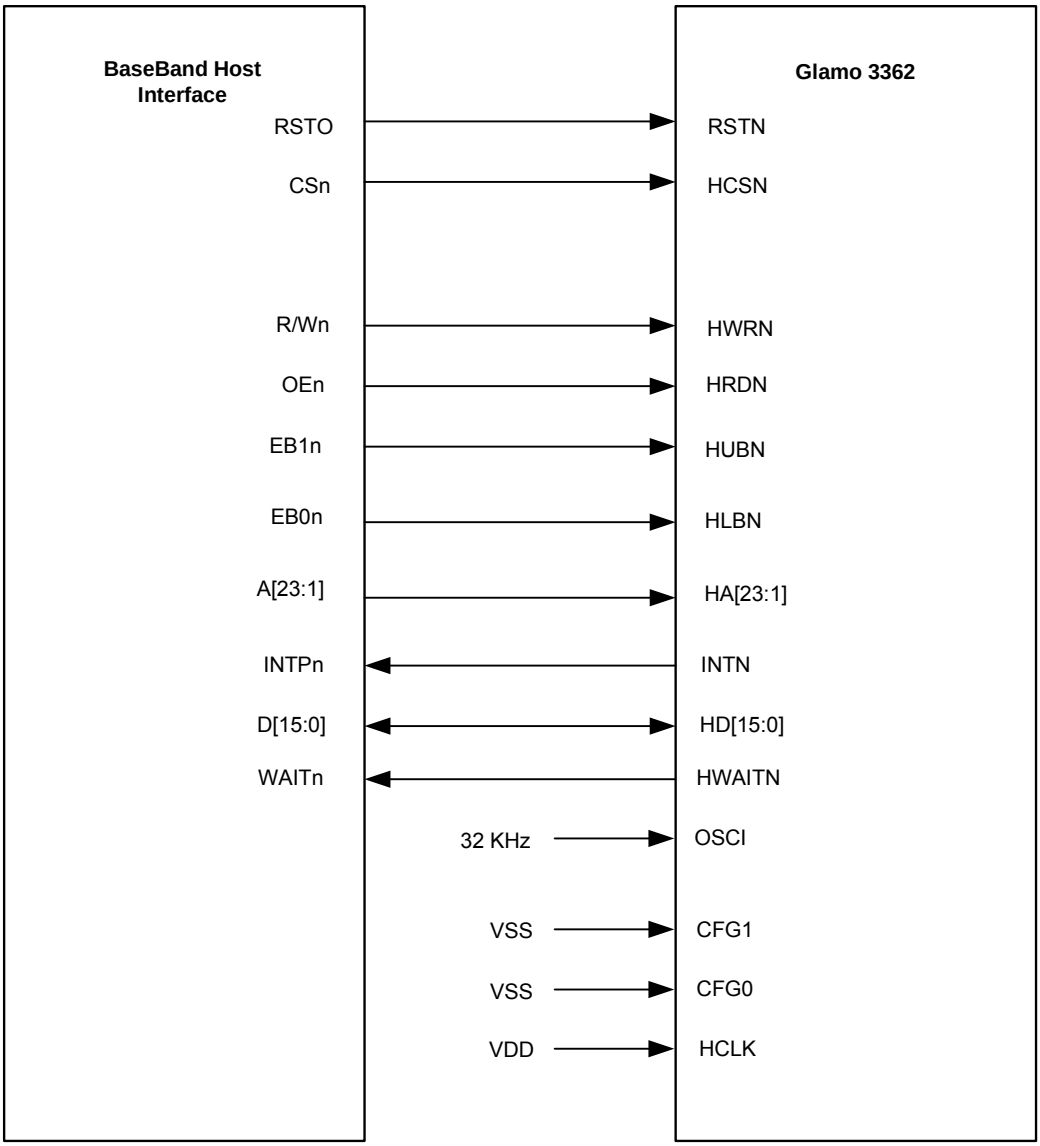


Figure 3.1.4-2 16 bits 68 Type CPU Write Transaction

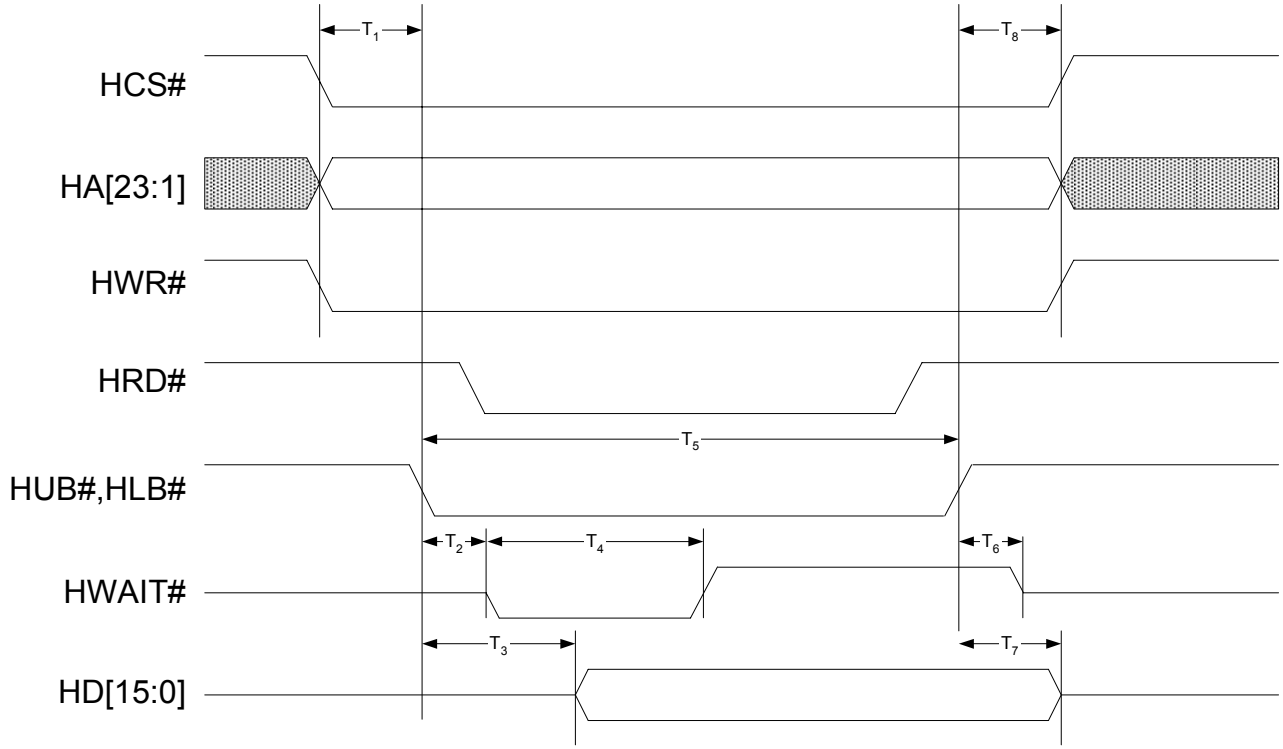


Figure 3.1.4-3 16 bits 68 Type CPU Read Transaction

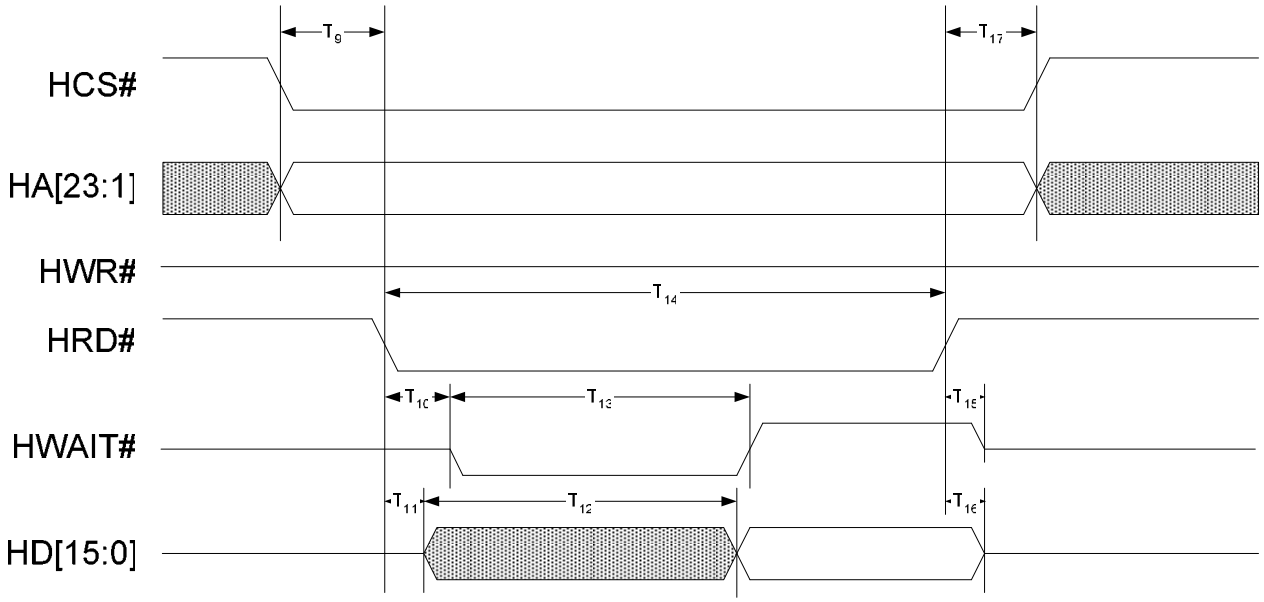


Table 3.1.4-1 Direct Addressing Mode 16 bits 68 Type Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11.0	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3.0	4.0	6.5	ns
T_7	Data hold time from write write rising edge	5			ns
T_8	Chip select, address and byte enable hold time from write rising edge	5			ns
T_9	Chip select, address and byte enable setup time from read falling edge	5			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address and byte enable hold time from read rising edge	5			ns

Note:

1. See Table 3.1.4-2.

Table 3.1.4-2 Direct Addressing Mode 16 bits 68 Type Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.5 Indirect Addressing Mode 16 bits 80 Type Interface

Figure 3.1.5-1 Indirect Addressing Mode 16 bits 80 Type Interface Implementation

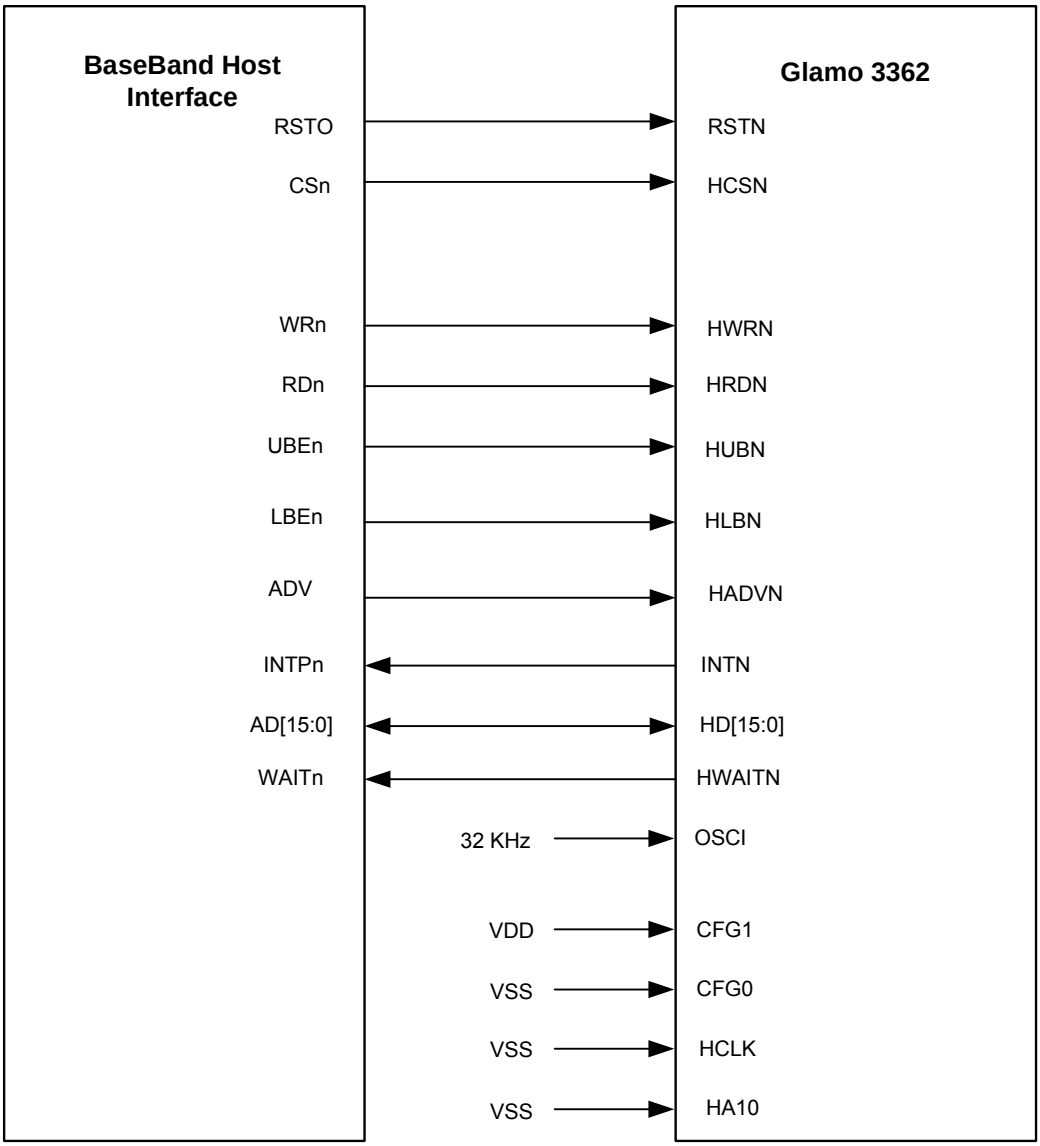


Figure 3.1.5-2 Indirect Addressing Mode 16 bits 80 Type Write Transaction

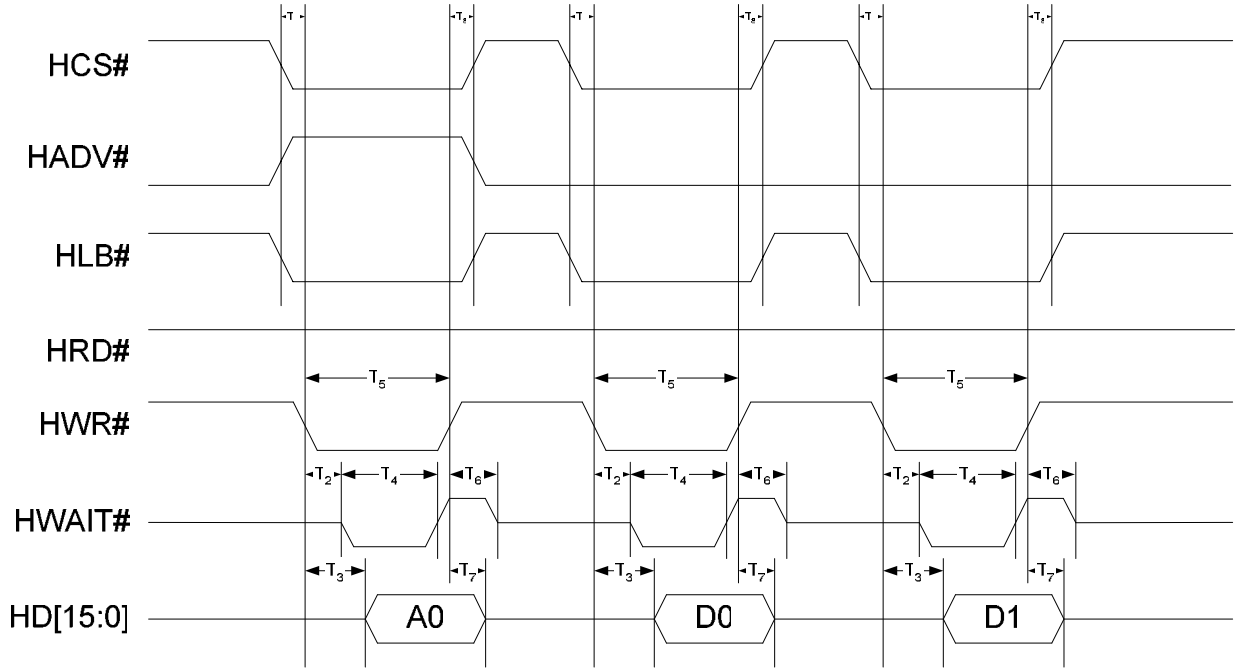


Figure 3.1.5-3 Indirect Addressing Mode 16 bits 80 Type Read Transaction

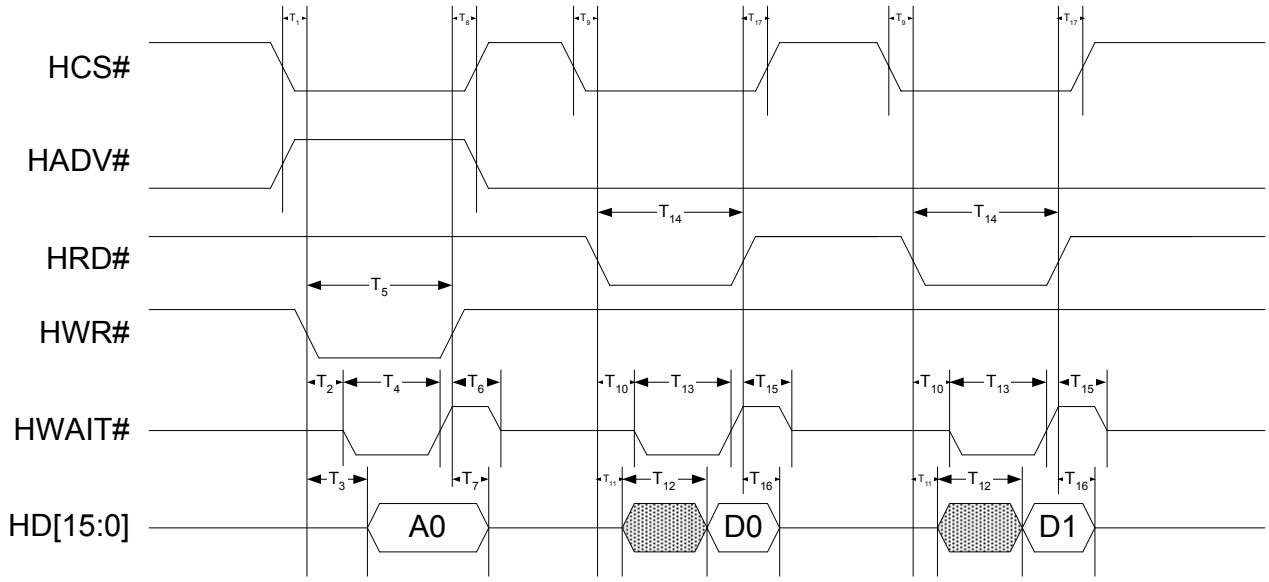


Table 3.1.5-1 Indirect Addressing Mode 16 bits 80 Type Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address valid and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11.0	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3.0	4.0	7.0	ns
T_7	Data hold time from write write rising edge	5			ns
T_8	Chip select, address valid and byte enable hold time from write rising edge	0			ns
T_9	Chip select, address valid and byte enable setup time from read falling edge	5			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4.0	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30.0			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address valid and byte enable hold time from read rising edge	0			ns

Note:

1. See Table 3.1.5-2.

Table 3.1.5-2 Indirect Addressing Mode 16 bits 68 Type Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.6 Indirect Addressing Mode 16 bits 68 Type Interface

Figure 3.1.6-1 Indirect Addressing Mode 16 bits 68 Type Interface Implementation

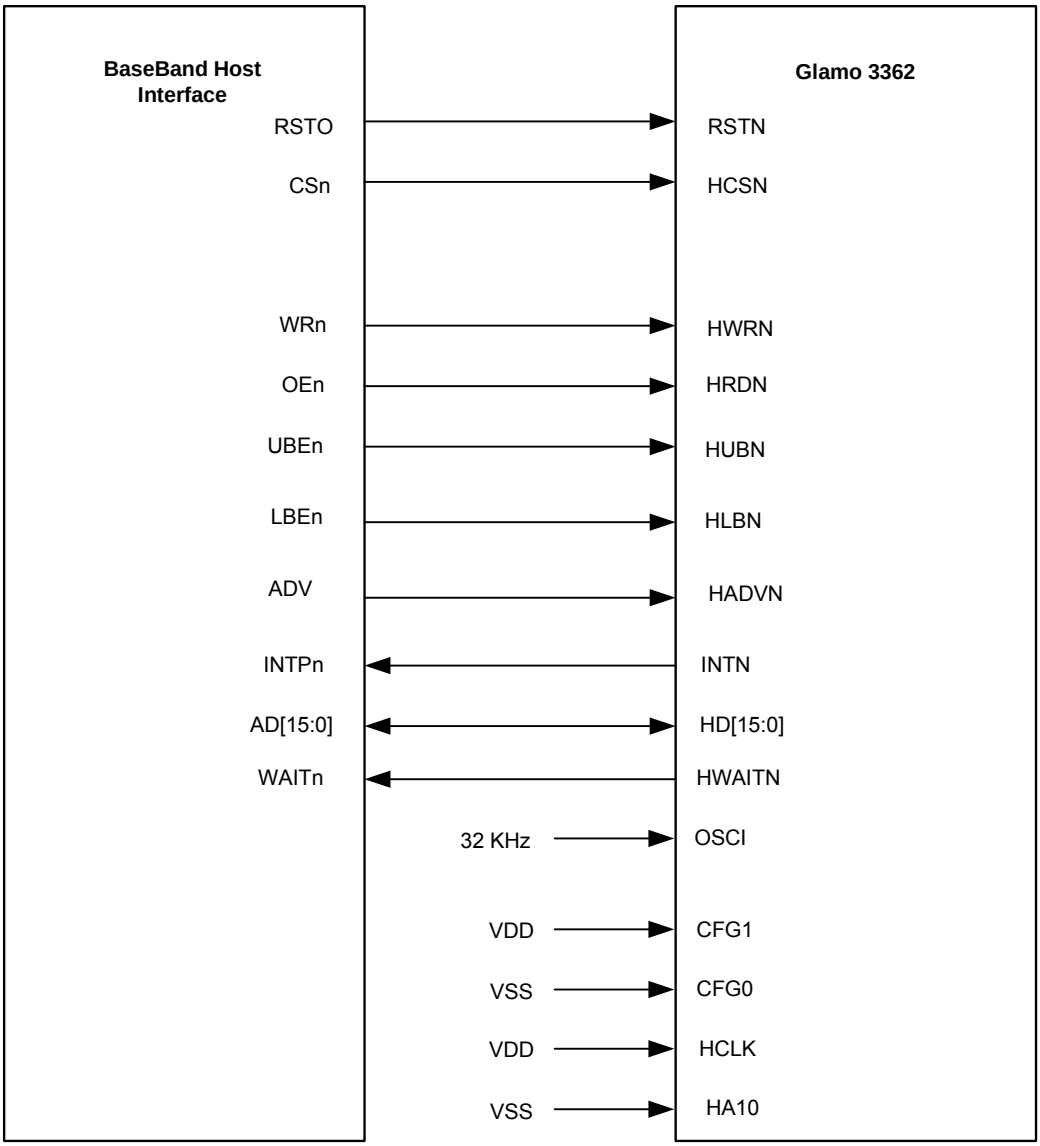


Figure 3.1.6-2 Indirect Addressing Mode 16 bits 68 Type Write Transaction

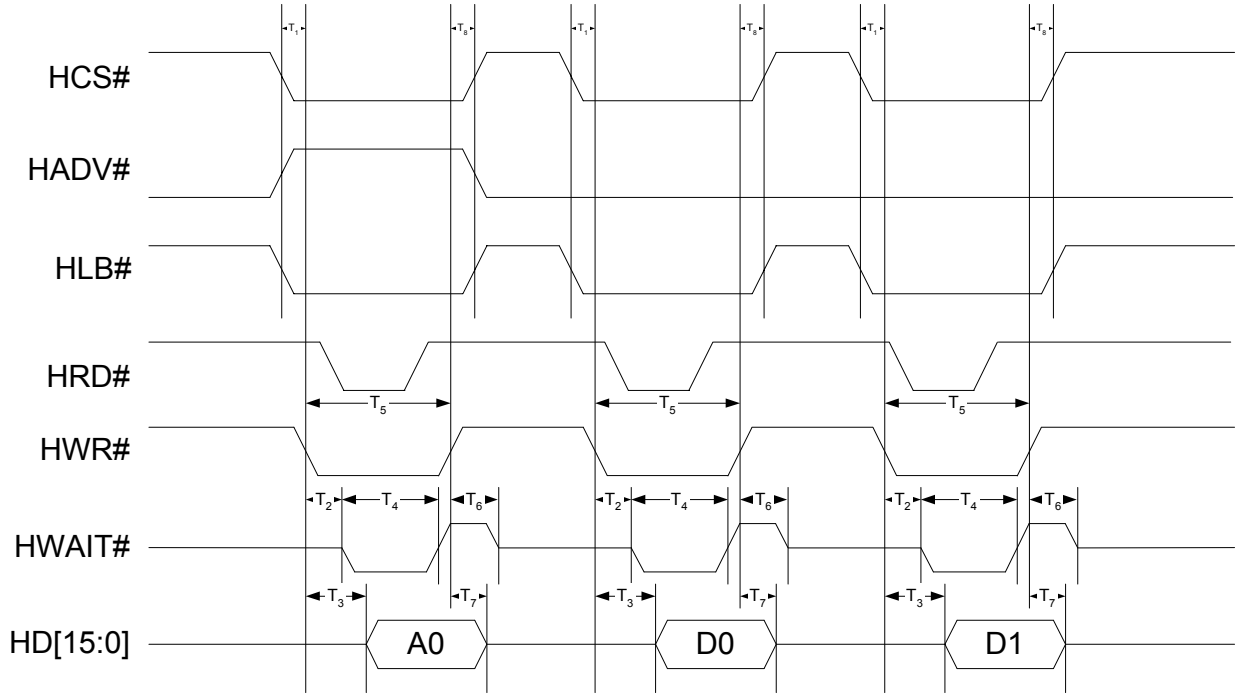


Figure 3.1.6-3 Indirect Addressing Mode 16 bits 68 Type Read Transaction

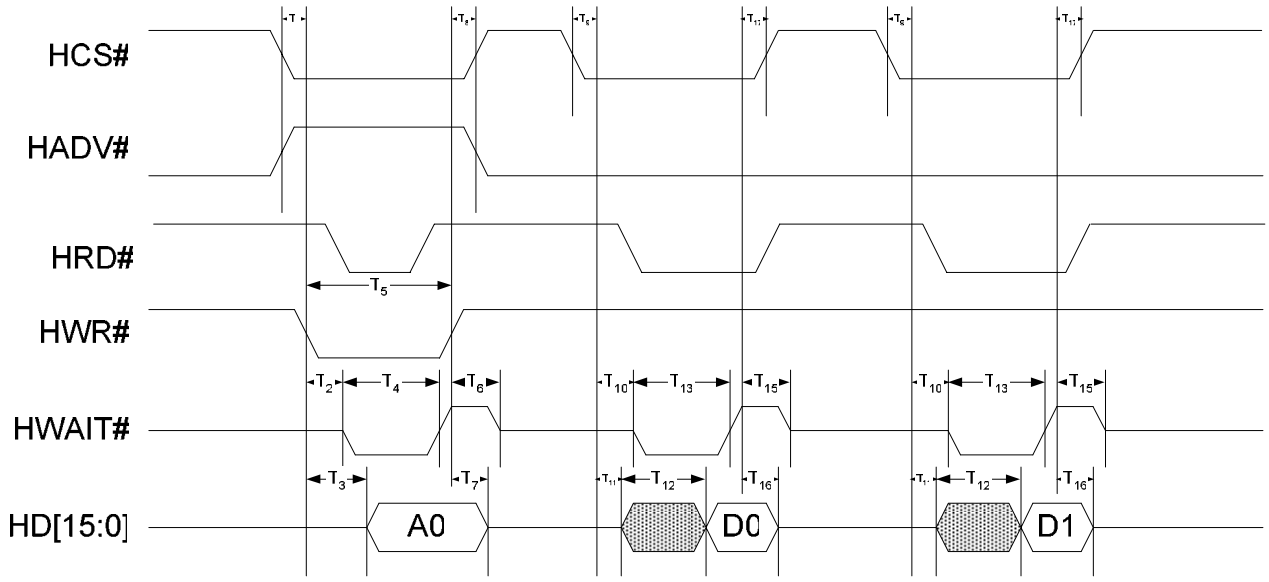


Table 3.1.6-1 Indirect Addressing Mode 16 bits 68 Type Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address valid and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11.0	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3.0	4.0	7.0	ns
T_7	Data hold time from write write rising edge	5			ns
T_8	Chip select, address valid and byte enable hold time from write rising edge	0			ns
T_9	Chip select, address valid and byte enable setup time from read falling edge	5			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4.0	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address valid and byte enable hold time from read rising edge	0			ns

Note:

1. See Table 3.1.6-2.

Table 3.1.6-2 Indirect Addressing Mode 16 bits 68 Type Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.7 Indirect Addressing Mode 8 bits 80 Type Interface

Figure 3.1.7-1 Indirect Addressing Mode 8 bits 80 Type Interface Implementation

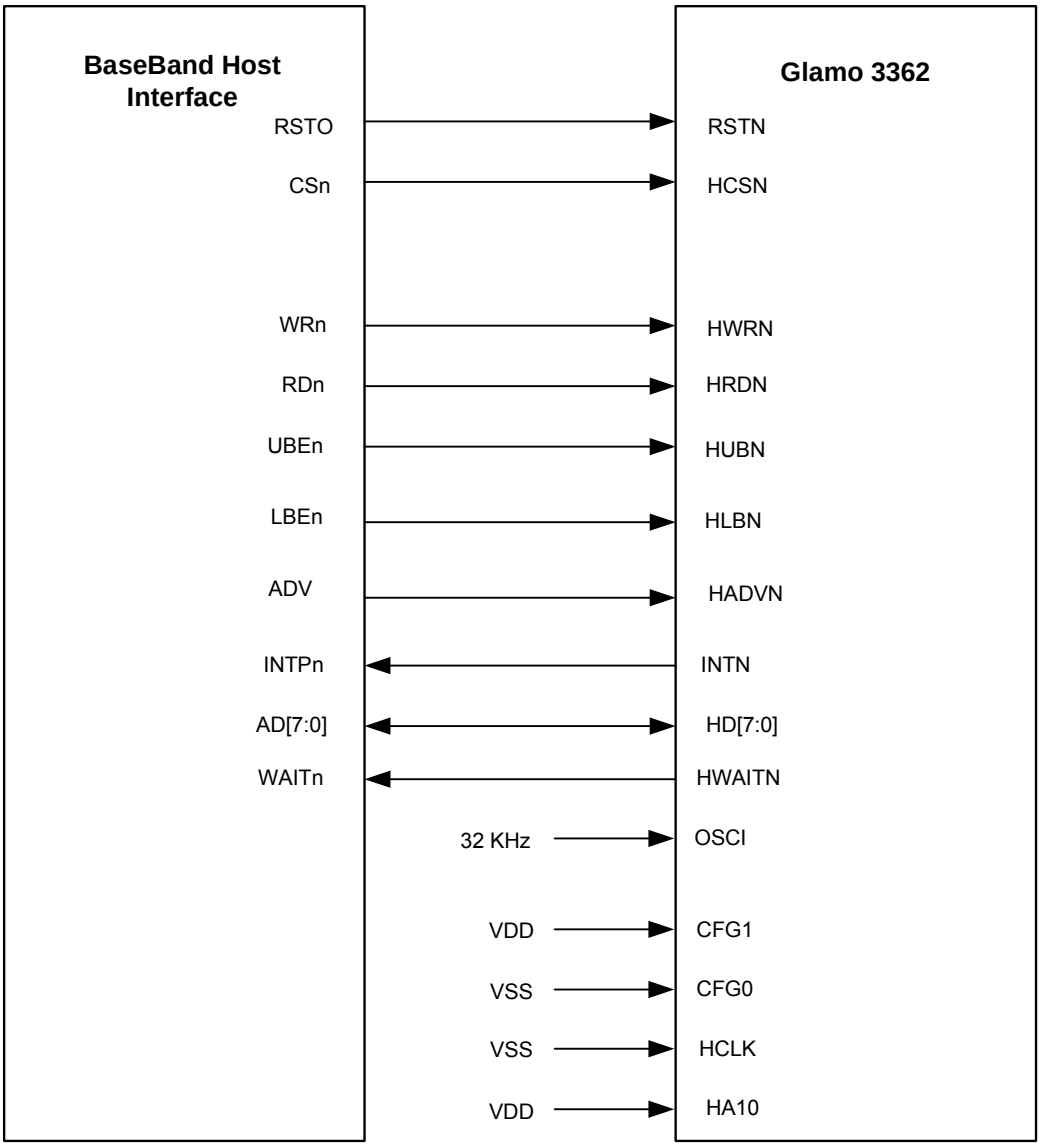


Figure 3.1.7-2 Indirect Addressing Mode 8 bits 80 Type Write Transaction

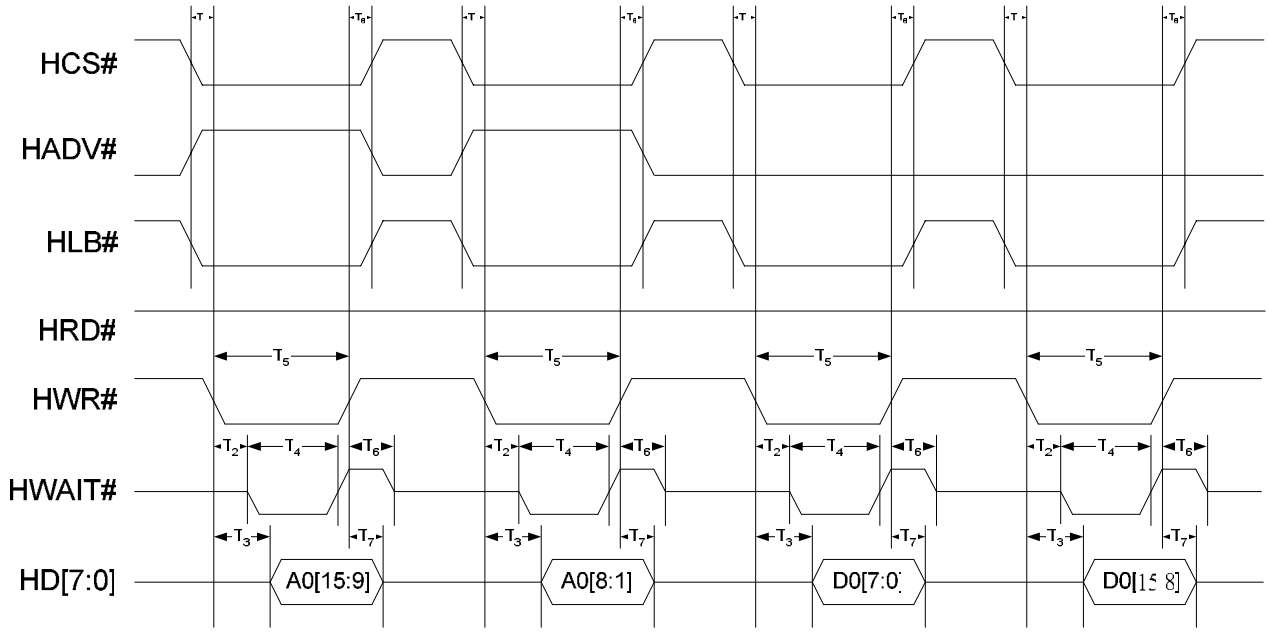
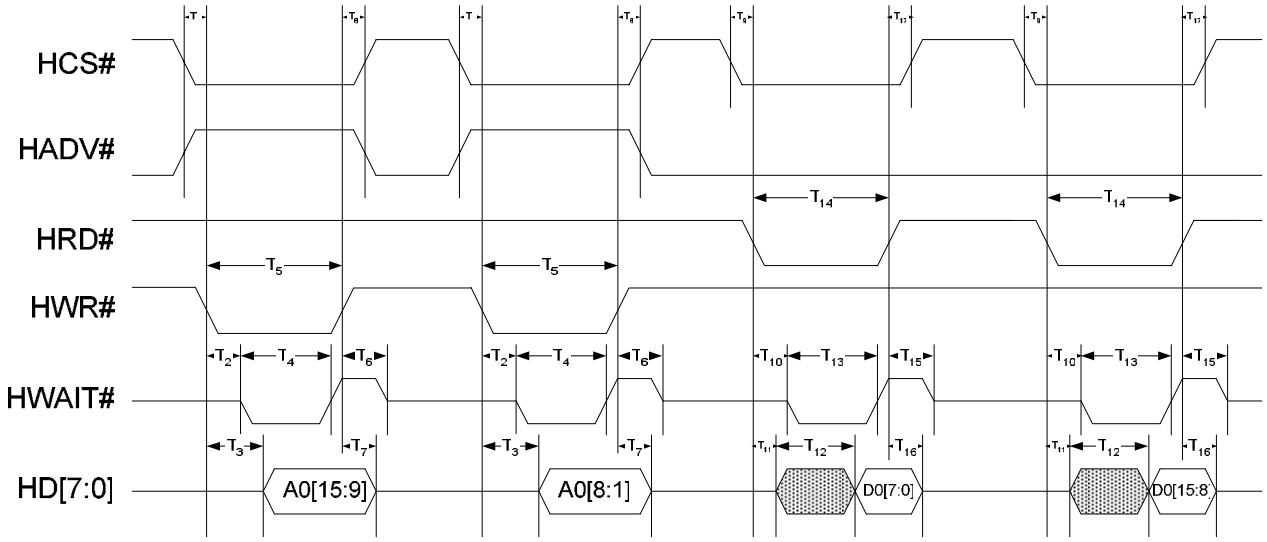


Figure 3.1.7-3 Indirect Addressing Mode



8 bits 80 Type Read Transaction

Table 3.1.7-1 Indirect Addressing Mode 8 bits 80 Type Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address valid and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11.5	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3.0	4.0	7.0	ns
T_7	Data hold time from write write rising edge	5			ns
T_8	Chip select, address valid and byte enable hold time from write rising edge	0			ns
T_9	Chip select, address valid and byte enable setup time from read falling edge	5			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4.0	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address valid and byte enable hold time from read rising edge	0			ns

Note:

1. See Table 3.1.7-2.

Table 3.1.7-2 Indirect Addressing Mode 8 bits 68 Type Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.8 Indirect Addressing Mode 8 bits 68 Type Interface

Figure 3.1.8-1 Indirect Addressing Mode 8 bits 68 Type Interface Implementation

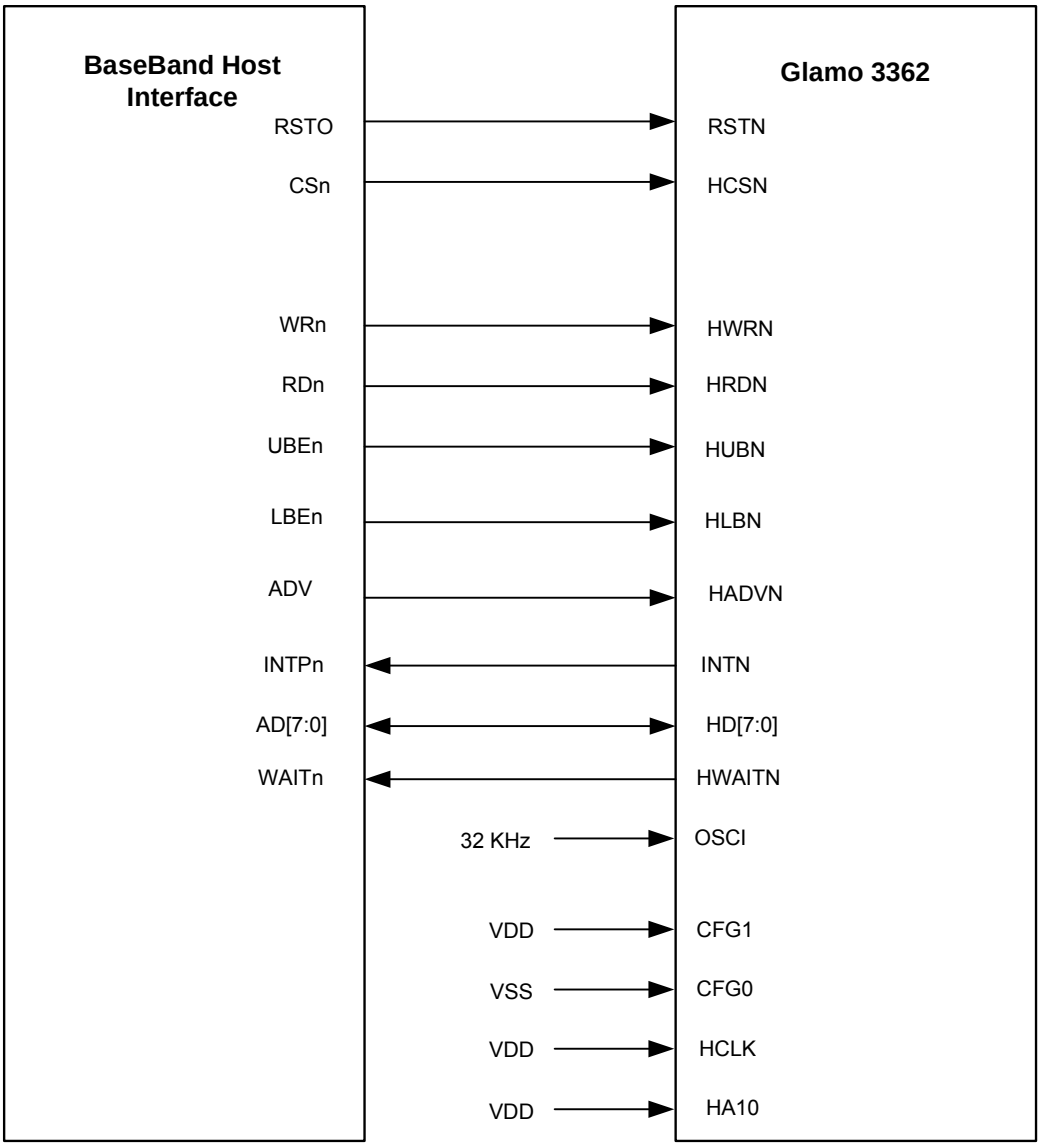


Figure 3.1.8-2 Indirect Addressing Mode 8 bits 68 Type Write Transaction

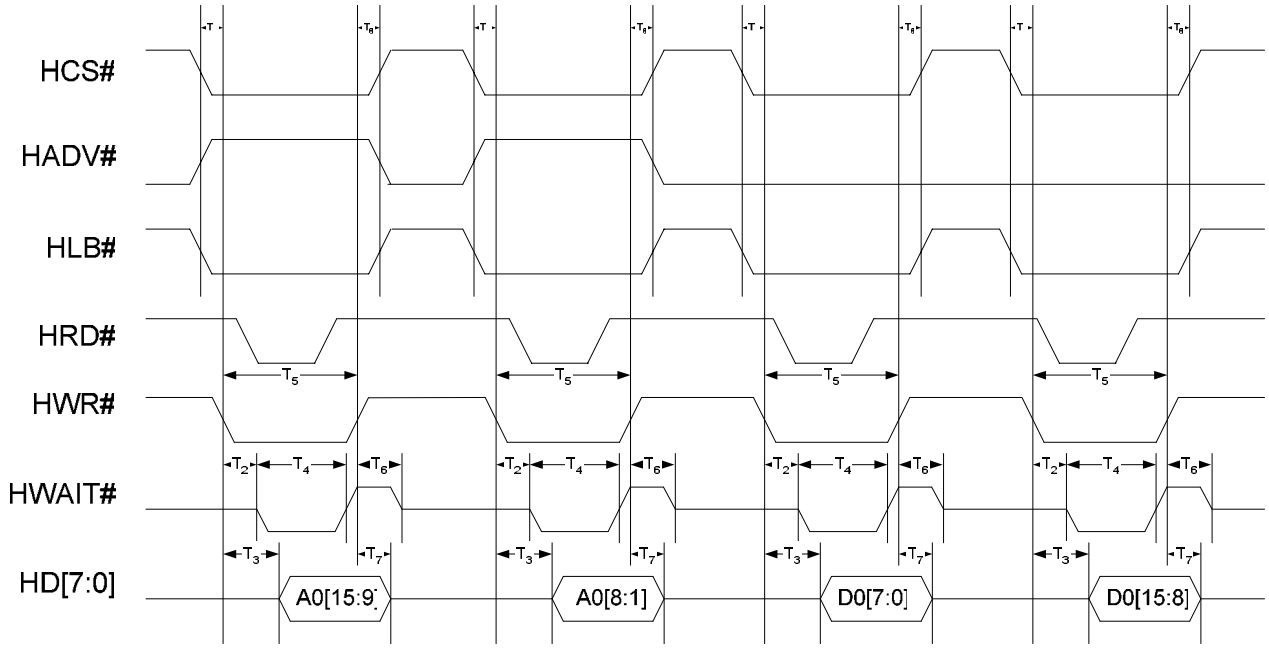


Figure 3.1.8-3 Indirect Addressing Mode 8 bits 68 Type Read Transaction

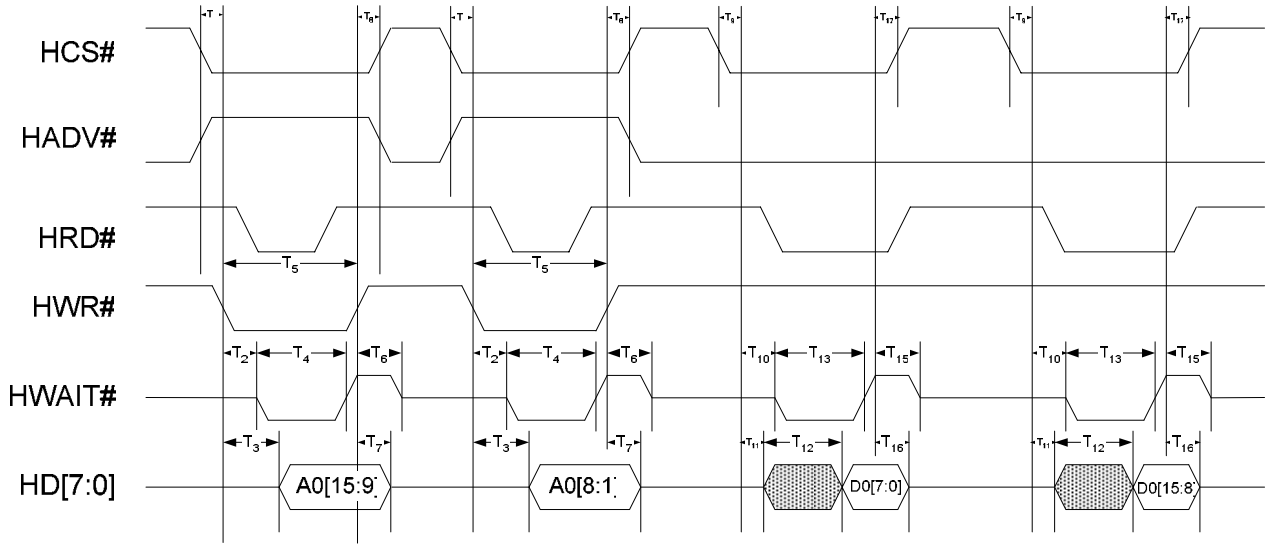


Table 3.1.8-1 Indirect Addressing Mode 8 bits 68 Type Interface Timing Table

Symbol	Parameter	Min	Typ	Max	Unit
T_1	Chip select, address valid and byte enable setup time from write falling edge	5			ns
T_2	Write falling edge to wait driven low	5.0	7.0	11.5	ns
T_3	Data delay from write falling edge			30	ns
T_4	Wait period during write cycle	(1)Note	(1)Note	(1)Note	
T_5	Write active period	30			ns
T_6	Write rising edge to wait high impedance	3.0	4.0	7.0	ns
T_7	Data hold time from write write rising edge	5.0			ns
T_8	Chip select, address valid and byte enable hold time from write rising edge	0			ns
T_9	Chip select, address valid and byte enable setup time from read falling edge	5.0			ns
T_{10}	Read falling edge to wait driven low	4.5	6.5	10.5	ns
T_{11}	Read falling edge to data driven	3.0	4.0	6.0	ns
T_{12}	Valid data period	(1)Note	(1)Note	(1)Note	-
T_{13}	Wait period during read cycle	(1)Note	(1)Note	(1)Note	-
T_{14}	Read active period	30			ns
T_{15}	Read rising edge to wait high impedance	3.0	3.5	6.5	ns
T_{16}	Data hold time from read rising edge	10.5	11.5	14.0	ns
T_{17}	Chip select, address valid and byte enable hold time from read rising edge	0			ns

Note:

1. See Table 3.1.8-2.

Table 3.1.8-2 Indirect Addressing Mode 8 bits 68 Type Interface Wait Period Table

Description	Min	Typ(2)	Max	Unit
Single Write to Registers		0	3(3)	T(1)
Single Read from Registers except ISP, JPEG, MPEG and 3D Registers		2	5(4)	T
Single Read from ISP Registers		3		T
Single Read from JPEG Registers		5		T
Single Read from MPEG Registers		5	7(5)	T
Single Read from 3D Registers		7		T
Consecutive(6) Write to Registers Penalty		1		T
Consecutive Read from Registers Penalty		1		T
Write to Registers after Read Penalty		1		T
Read from Registers after Write Penalty		3		T

Note:

1. T represents inner clock period.
2. Due to asynchronous timing, all above real timing should add the time from asynchronous asserted to inner clock latch edge.
3. Refer to 0x0200h[5:4] register in programming guide.
4. Refer to 0x0200h[7:6] register in programming guide.
5. Time for the first reading from MPEG registers.
6. It means read/write at the same time in 1T period.

3.1.9 Synchronous iBurst Interface

iBurst is a specific interface for synchronous transmission. By now, some baseband suppliers do plan to support it. The following is an example of Infineon's S-Gold2.

Figure 3.1.9-1 iBurst Interface Implementation

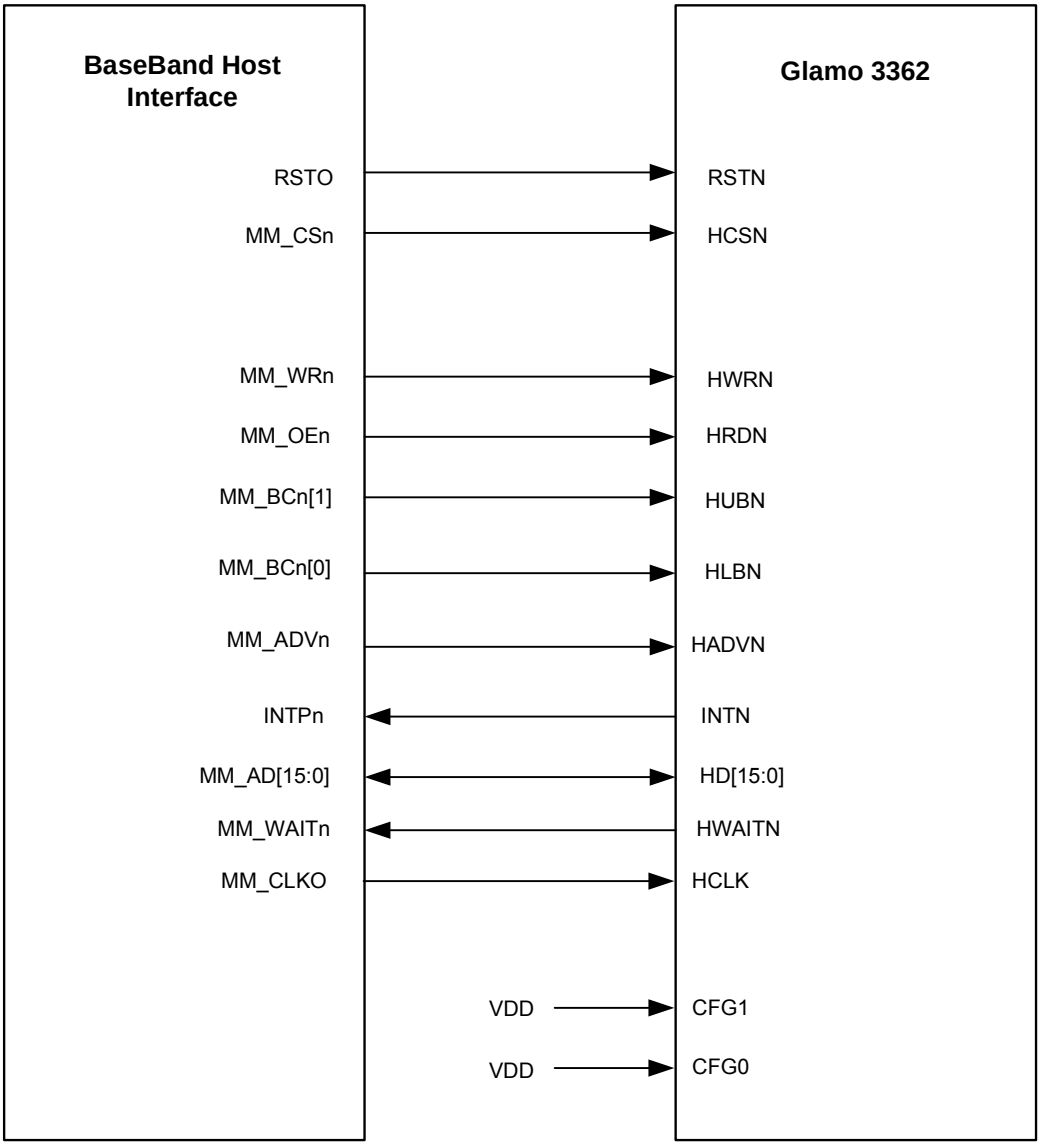

BaseBand Host Interface
Glamo 3362
RSTO
RSTN
MM_CSn
HCSN
MM_WRn
HWRN
MM_OEn
HRDN
MM_BCn[1]
HUBN
MM_BCn[0]
HLBN
MM_ADVn
HADVN
INTPn
INTN
MM_AD[15:0]
HD[15:0]
MM_WAITn
HWAITN
MM_CLKO
HCLK
VDD
CFG1
VDD
CFG0

Figure 3.1.9-2 iBurst Single Write Transaction with Wait_Ctrl =1 (High-Low Addressing Multiplex)

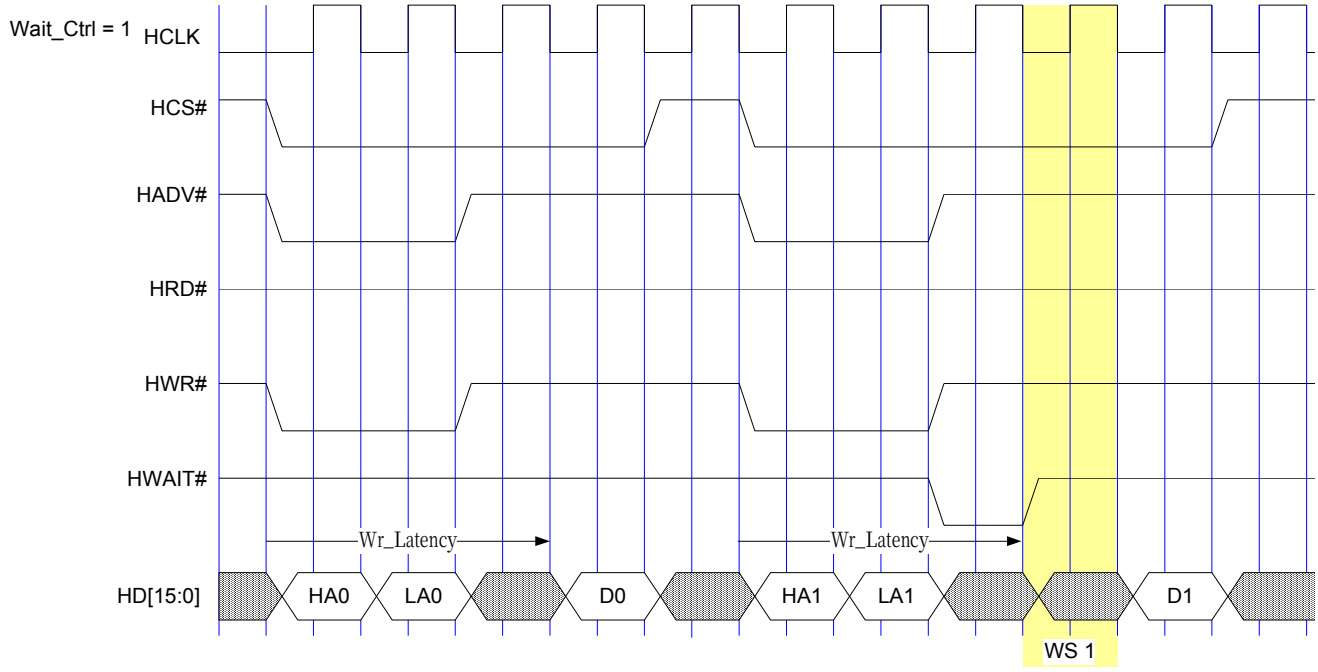


Figure 3.1.9-3 iBurst Single Write Transaction with Wait_Ctrl =0 (High-Low Addressing Multiplex)

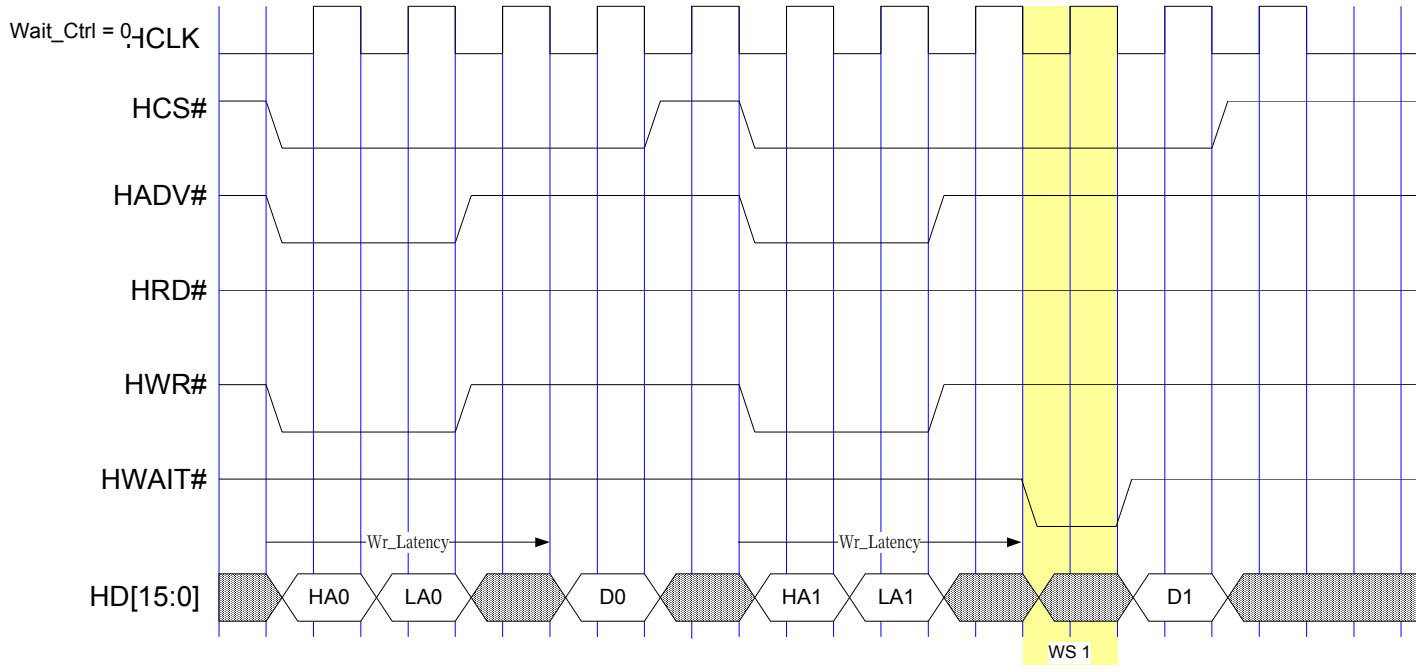


Figure 3.1.9-4 iBurst Burst Write Transaction with Wait_Ctrl =1 (High-Low Addressing Multiplex)

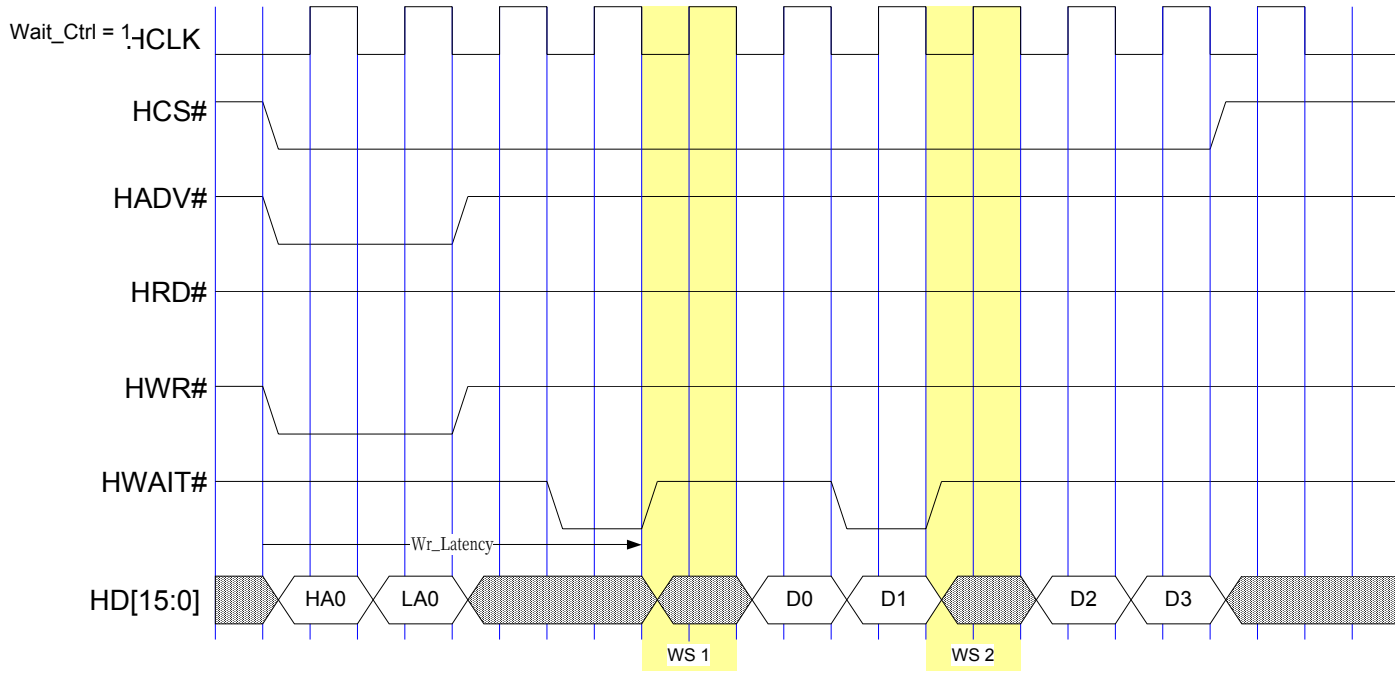


Figure 3.1.9-5 iBurst Burst Write Transaction with Wait_Ctrl =0 (High-Low Addressing Multiplex)

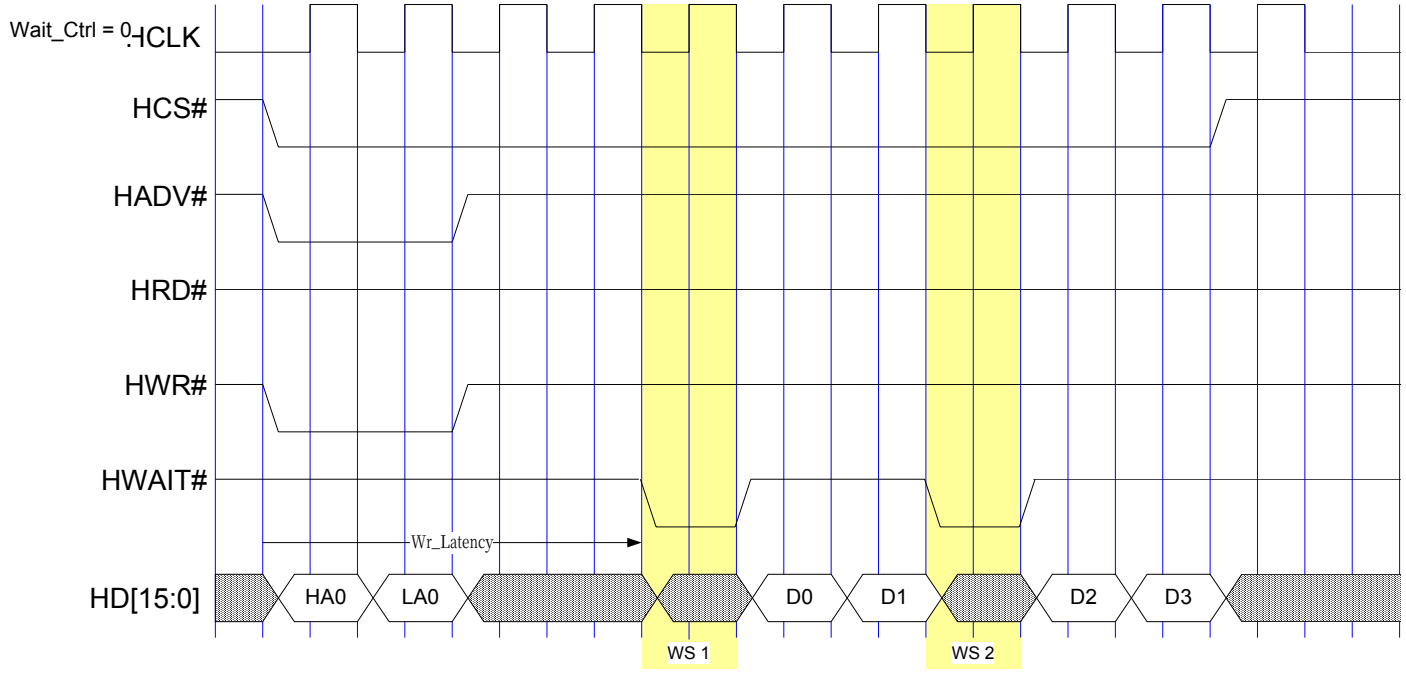


Figure 3.1.9-6 iBurst Single Read Transaction with Wait_Ctrl =1 (High-Low Addressing Multiplex)

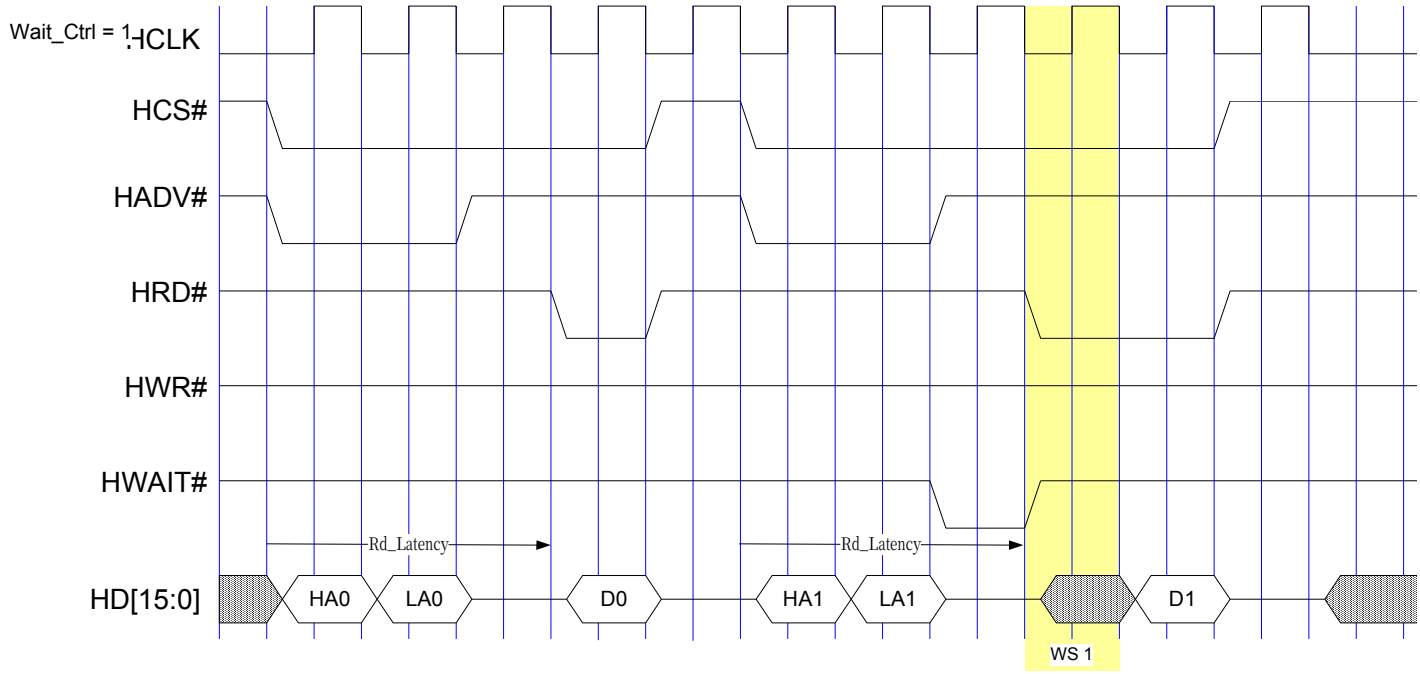


Figure 3.1.9-7 iBurst Single Read Transaction with Wait_Ctrl =0 (High-Low Addressing Multiplex)

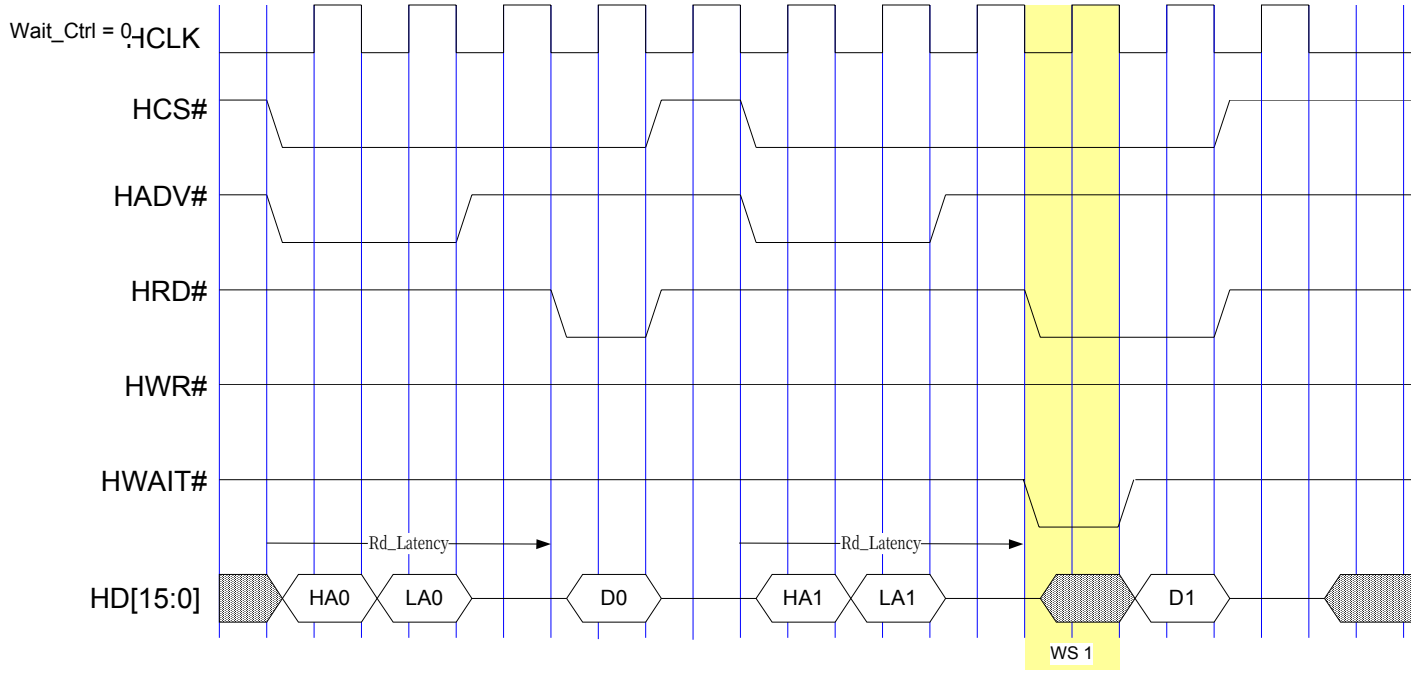


Figure 3.1.9-8 iBurst Burst Read Transaction with Wait_Ctrl =1 (High-Low Addressing Multiplex)

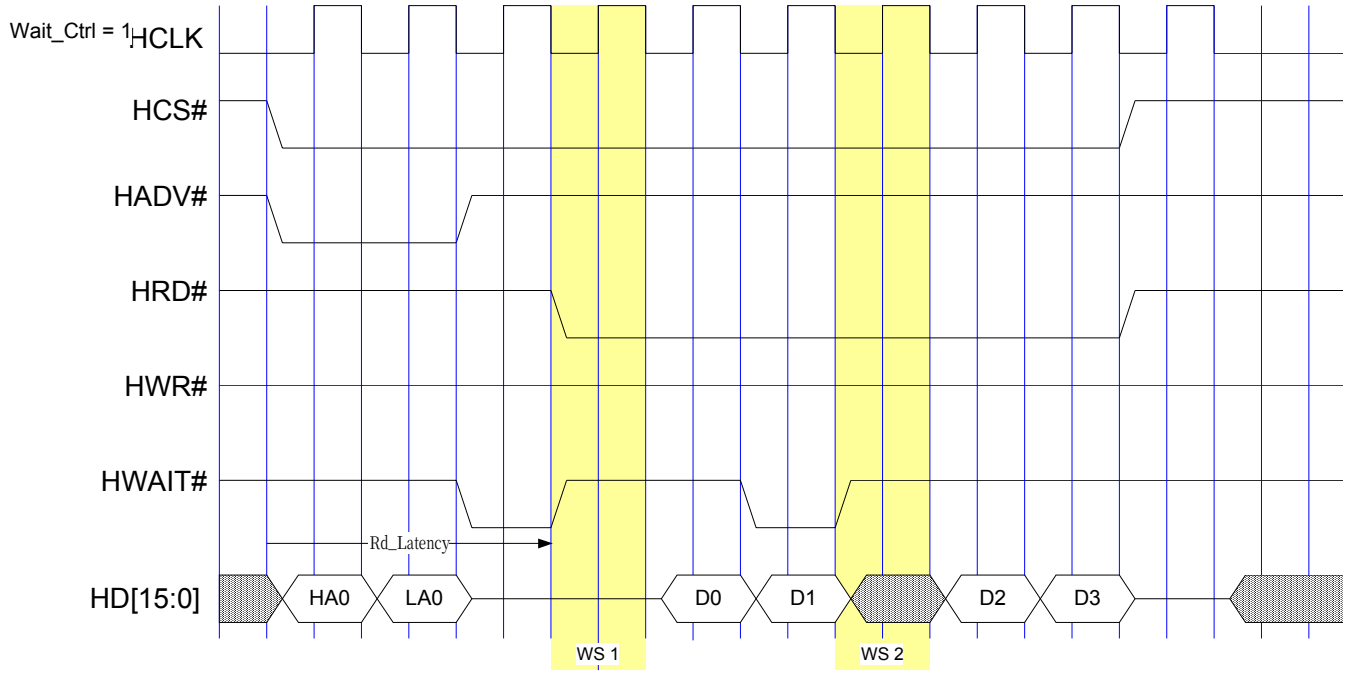


Figure 3.1.9-9 iBurst Burst Read Transaction with Wait_Ctrl =0 (High-Low Addressing Multiplex)

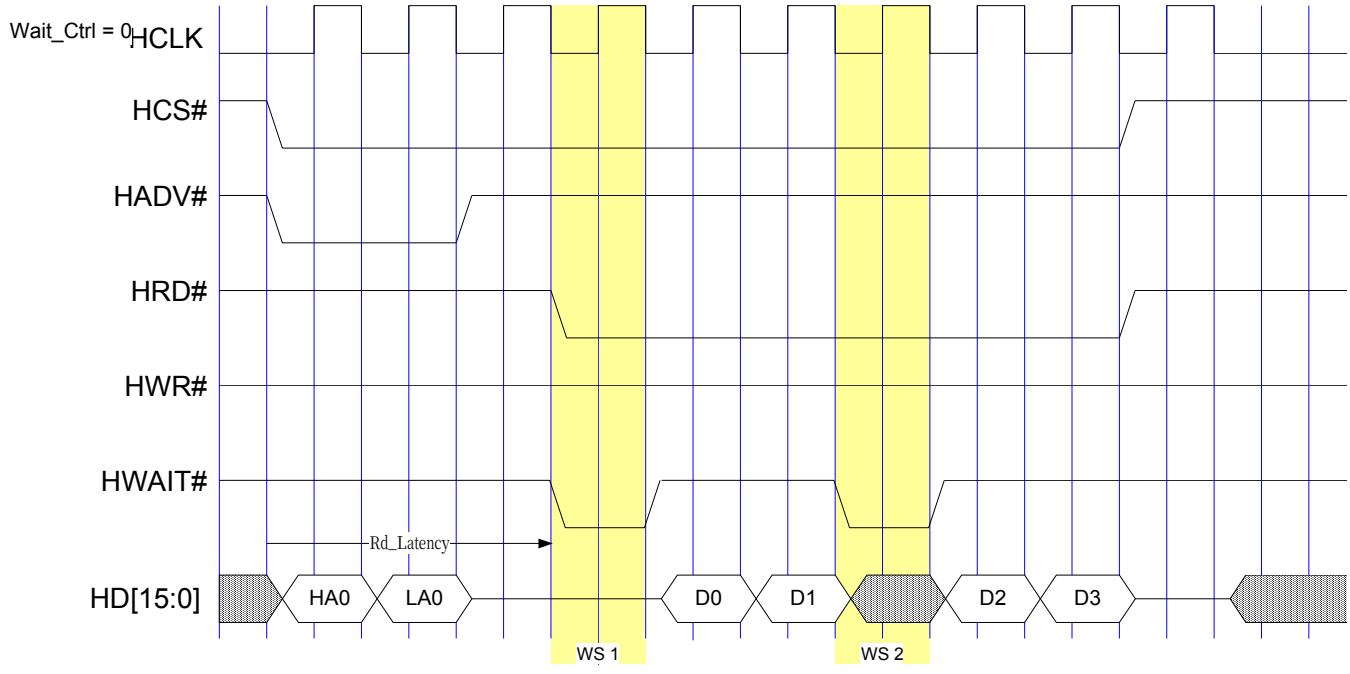


Table 3.1.9-1 iBurst Interface Read/Write Latency Table

Symbol	Parameter	Min	Typ	Max	Unit
Wr_Latency	Write latency cycle	0	4	15	T(1)
Rd_Latency	Read latency cycle	0	4	15	T

Note:

1. T represents one HCLK period from iBurst external clock.

3.2 LCD Interface

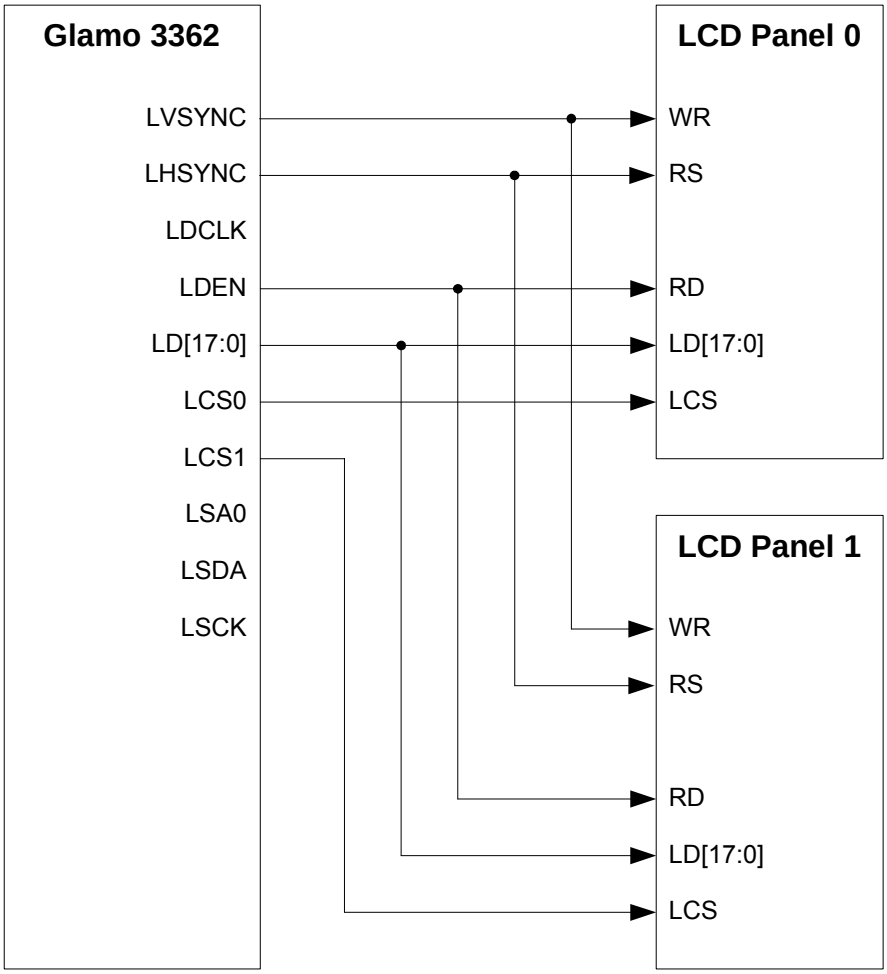
3.2.1 General Description

The Glamo 3362 supports 8/9/16/18 bits CPU interface, 6/9/16/18 bits RGB interface and by-pass mode. The Glamo 3362 supports both that with memory and that without memory LCD modules (LCM). The programmable interface timing is designed to fit most LCMs. The built-in power saving design is useful to increase the battery life.

3.2.2 80-Type CPU Interface

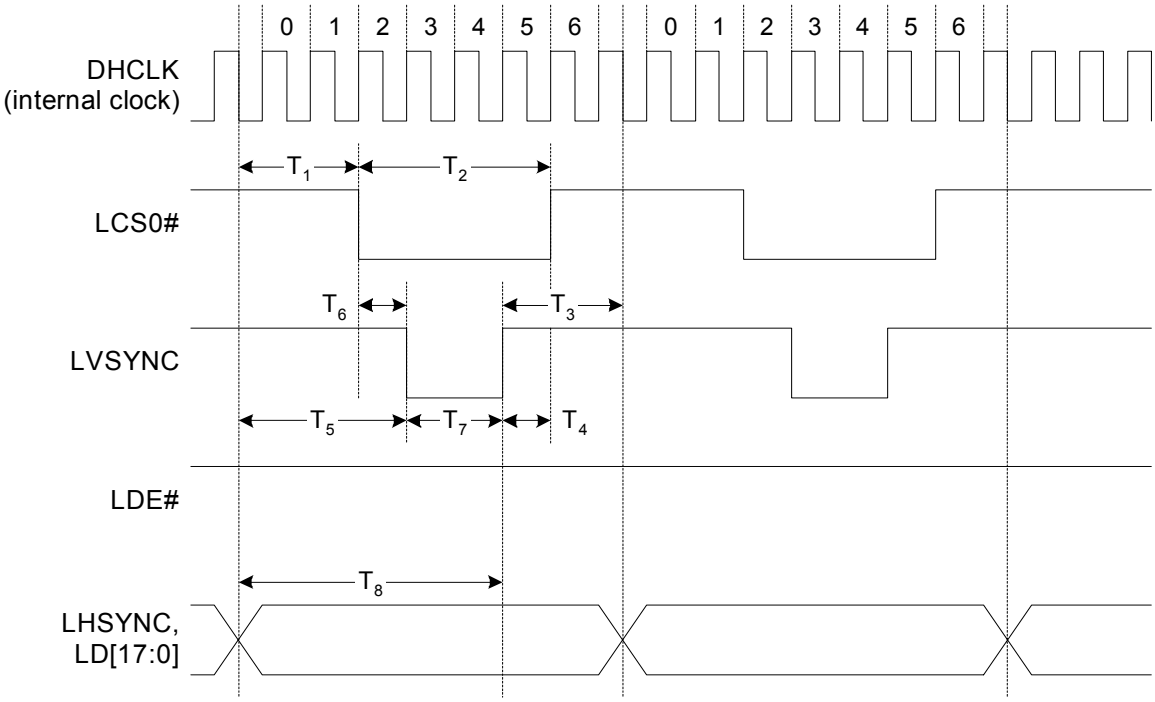
The figure below illustrates the implementation for interfacing the Glamo 3362 to an 80-type CPU interface LCM. Glamo 3362 can support dual display for this interface.

Figure 3.2.2-1 Connection of Glamo 3362 to 80-Type CPU Interface LCM



The timing for 80-type CPU interface is showed in the following figure. There is an internal clock DHCLK. By adjusting the timing parameters T_1 ~ T_8 which are relative to DHCLK, it can satisfy the timing requirement of LCD panels.

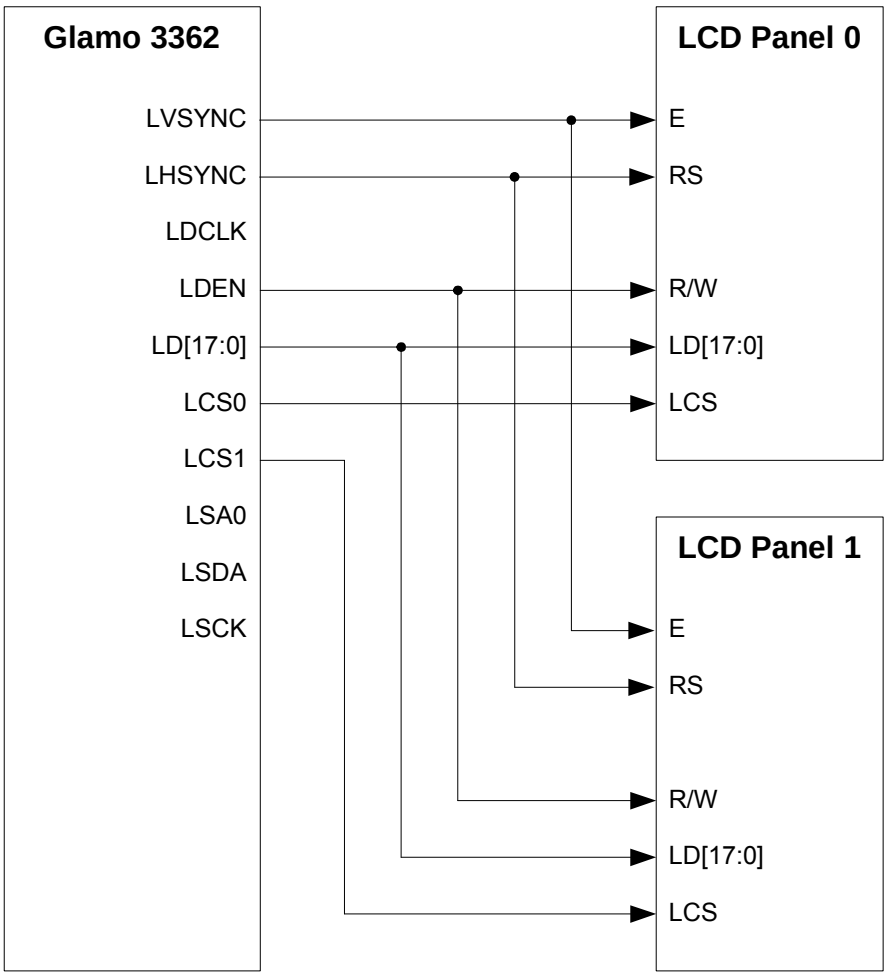
Figure 3.2.2-2 80-Type CPU Interface Timing



3.2.3 68-Type CPU Interface

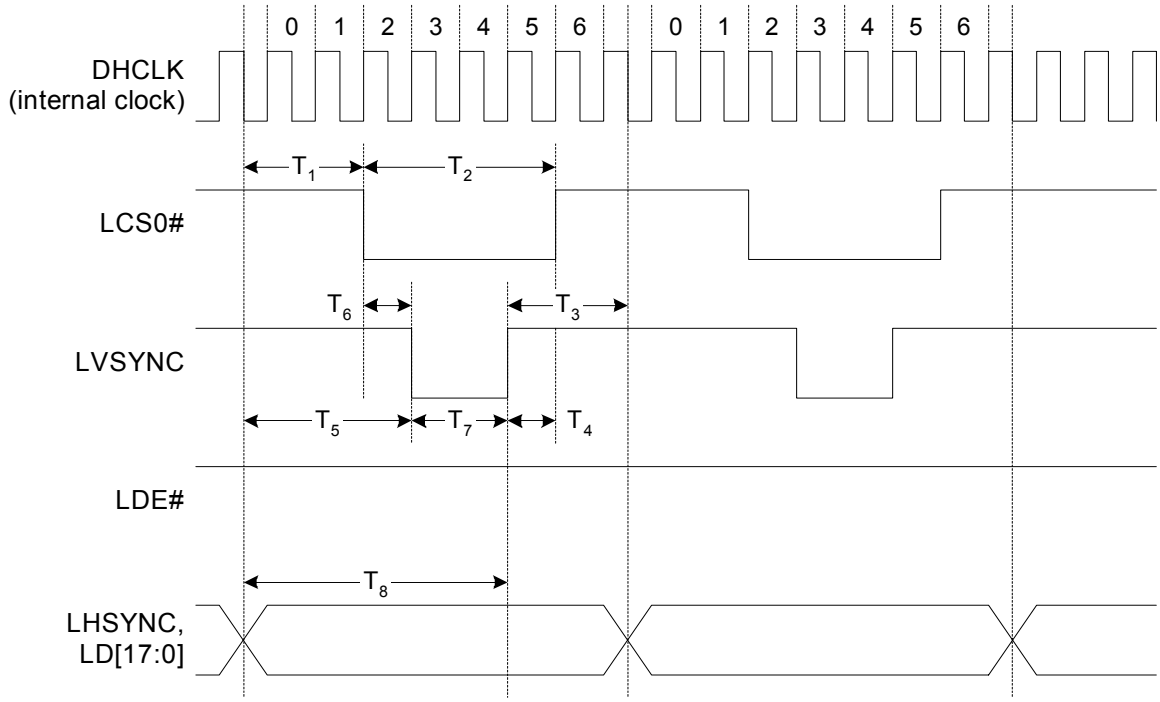
The figure below illustrates the implementation for interfacing the Glamo 3362 to a 68-type CPU interface LCM. Glamo 3362 can support dual display for this interface.

Figure 3.2.3-1 Connection of Glamo 3362 to 68-Type CPU Interface LCM



The timing for 68-type CPU interface is showed in the following figure. There is an internal clock DHCLK. By adjusting the timing parameters T_1 ~ T_8 which are relative to DHCLK, it can satisfy the timing requirement of LCD panels.

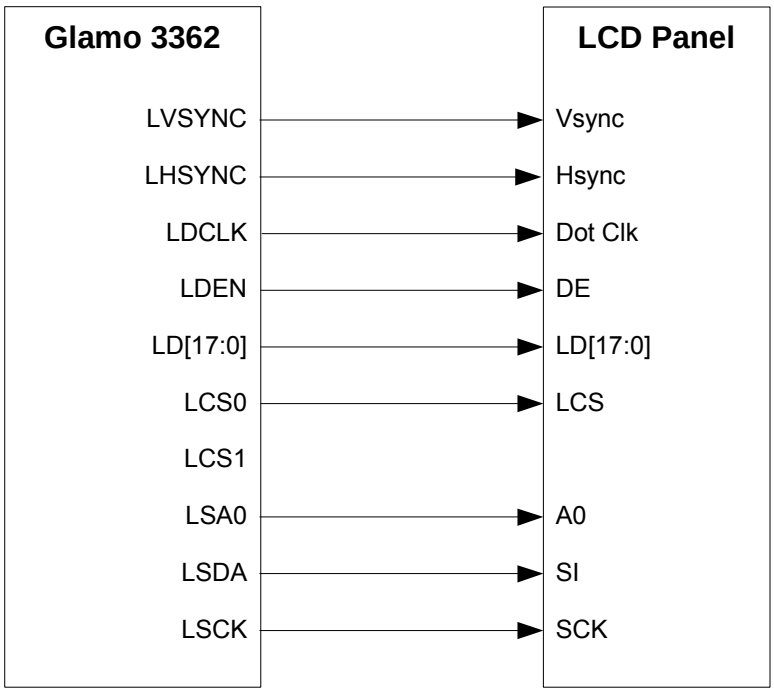
Figure 3.2.3-2 68-Type CPU Interface Timing



3.2.4 RGB with Serial Interface

The figure below illustrates the implementation for interfacing the Glamo 3362 to a RGB with serial interface LCM. Glamo 3362 only support one display for this interface

Figure 3.2.4-1 Connection of Glamo 3362 to RGB with Serial Interface LCM



Glamo 3362 supports 8/9/24 bits serial interface to send LCM command and uses 6/9/16/18 bits parallel RGB interface to send display data. The timing for RGB with serial interface is shown in the following figure.

Figure 3.2.4-2 RGB Timing (for Data)

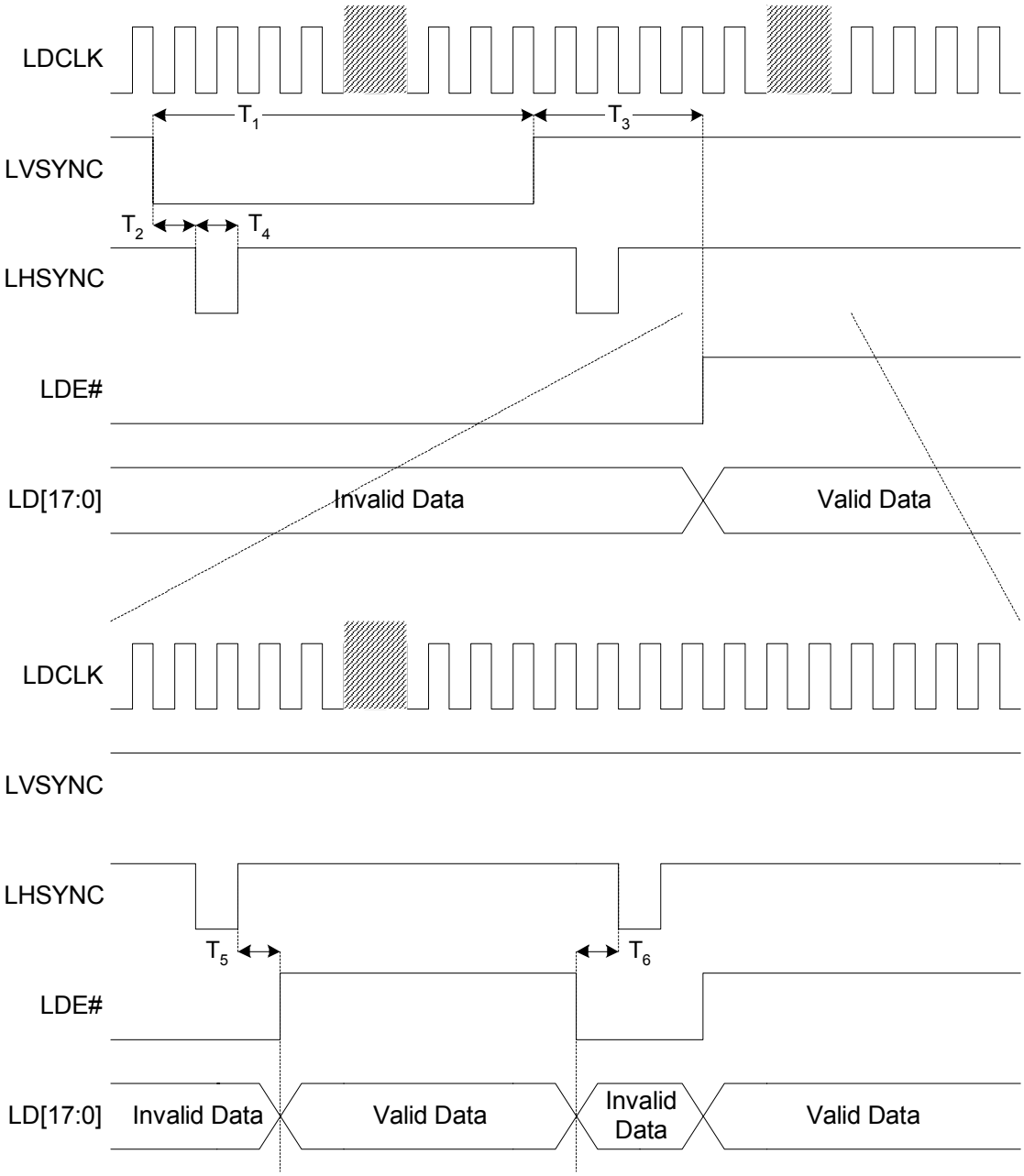
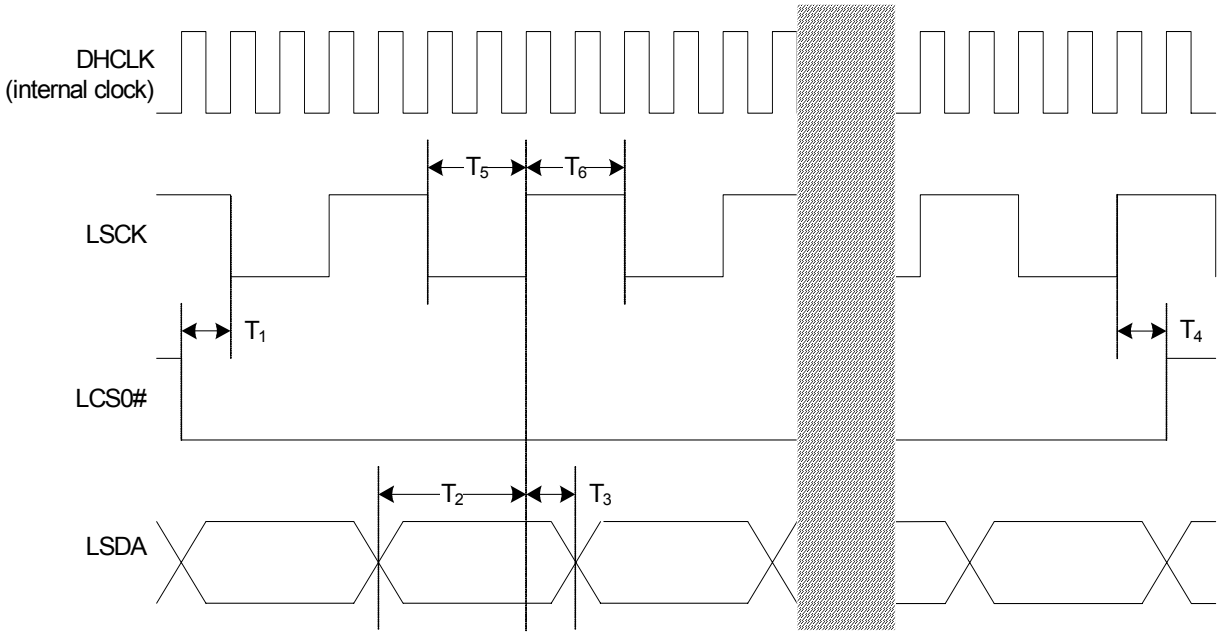


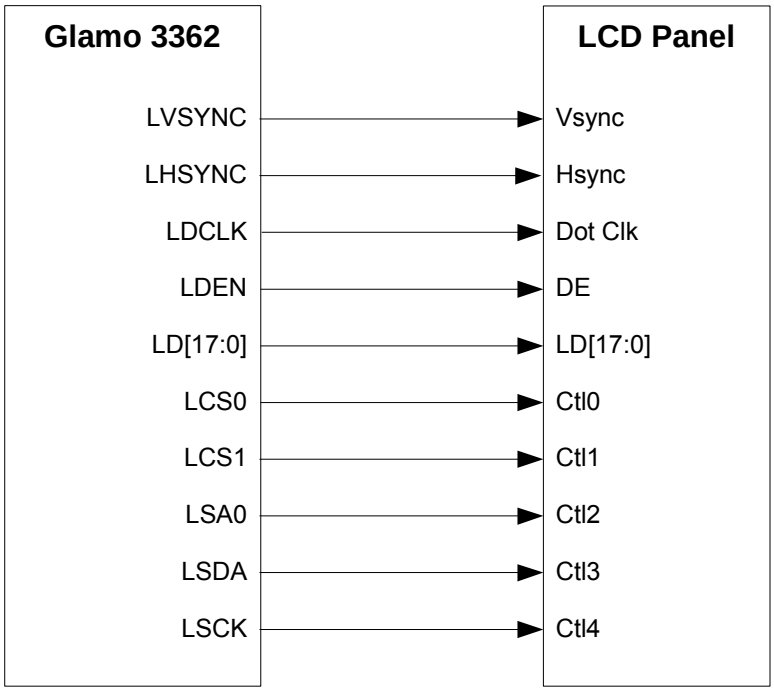
Figure 3.2.4-3 RGB with Serial Interface Timing (for Command)


DHCLK
(internal clock)
T5
T6
LSCK
T1
T4
LCS0#
T2
T3
LSDA

3.2.5 RGB with Direct Control Interface

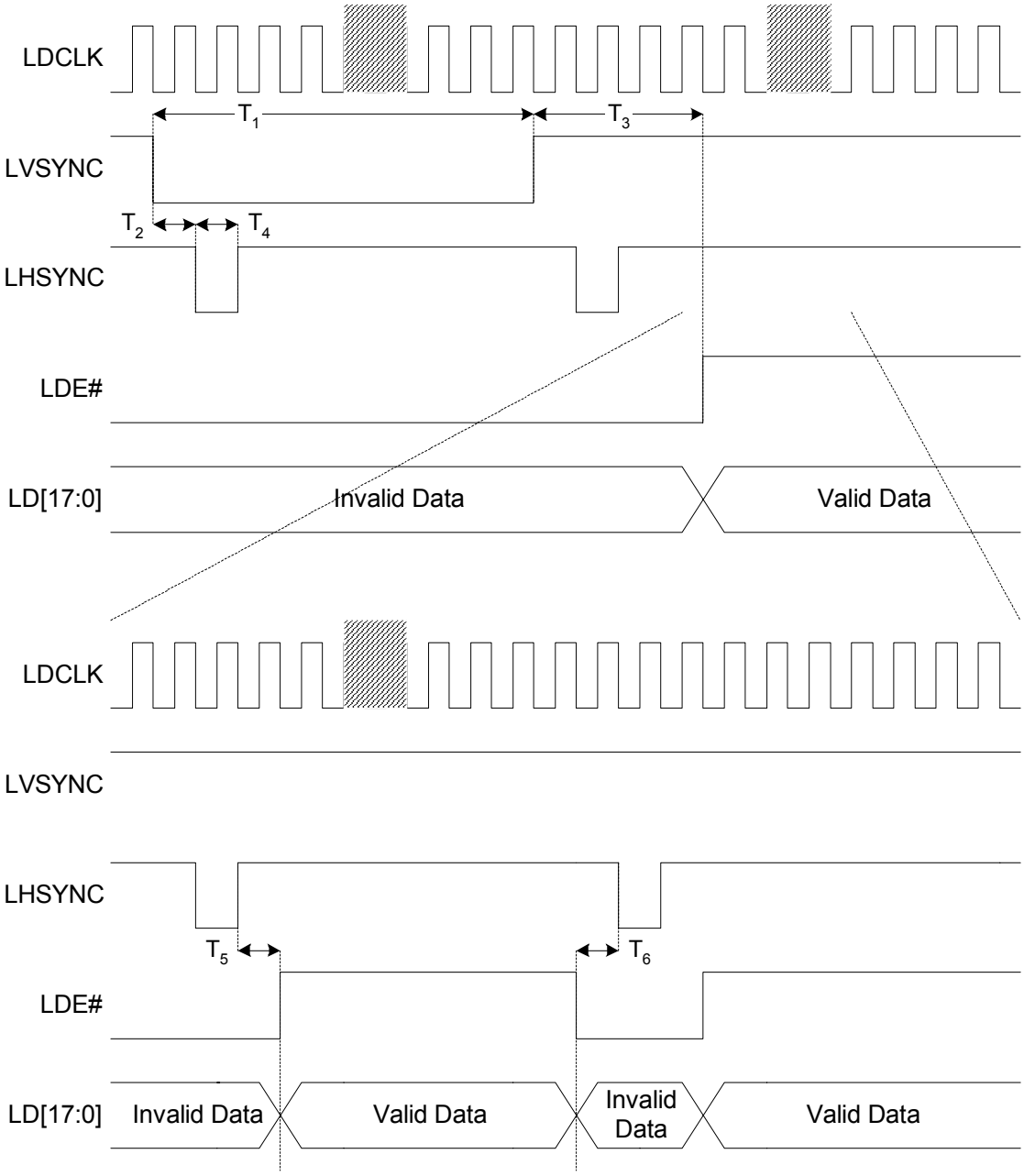
The figure below illustrates the implementation for interfacing the Glamo 3362 to a RGB with direct control interface LCM. Glamo 3362 only supports one display with this interface

Figure 3.2.5-1 Connection of Glamo 3362 to RGB with Direct Control Interface LCM



Some LCMs do not have any serial interface;, but only have parallel RGB interface. In this case, the un-used pins (LCS0#, LCS1#, LSA0, LSDA, LSCK) of the Glamo 3362 can be defined as GPIOs. The timing for RGB parallel interface is showed in the following figure.

Figure 3.2.5-2 RGB with Direct Control Interface Timing (for Data)


LDCLK
T1
T3
LVSYNC
T2
T4
LHSYNC
LDE#
LD[17:0]
Invalid Data
Valid Data
LDCLK
LVSYNC
LHSYNC
T5
T6
LDE#
LD[17:0]
Invalid Data
Valid Data
Invalid Data
Valid Data

3.2.6 By-Pass Mode Implementation

When turn on by-pass mode, some pins of the host interface will connect with the pins of LCD interface internally. In this mode, it supports 80-type CPU or 68-type CPU LCM.

Table 3.2.6-1 Mapping of Host Interface Pins to LCD Interface Pins for 80-Type CPU LCM

Host Interface Pin	LCD Interface Pin
HA1	LHSYNC
HD0	LD0
HD1	LD1
HD2	LD2
HD3	LD3
HD4	LD4
HD5	LD5
HD6	LD6
HD7	LD7
HD8	LD8
HD9	LD9
HD10	LD10
HD11	LD11
HD12	LD12
HD13	LD13
HD14	LD14
HD15	LD15
HCS#	LCS0#
HRD#	LDE#
HWR#	LVSYNC
HA2	LCS1#

Table 3.2.6-2 Mapping of Host Interface Pins to LCD Interface Pins for 68-Type CPU LCM

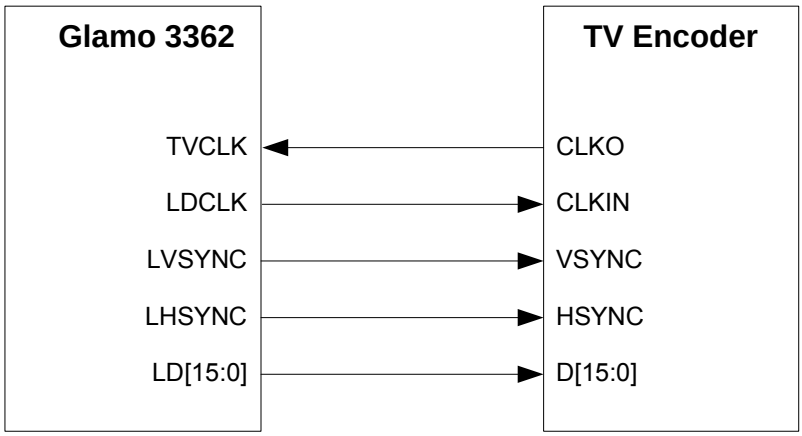
Host Interface Pin	LCD Interface Pin
HA1	LHSYNC
HD0	LD0
HD1	LD1
HD2	LD2
HD3	LD3
HD4	LD4
HD5	LD5
HD6	LD6
HD7	LD7
HD8	LD8
HD9	LD9
HD10	LD10
HD11	LD11
HD12	LD12
HD13	LD13
HD14	LD14
HD15	LD15
HCS#	LCS0#
HRD#	LDE#
HLB#	LVSYNC
HA2	LCS1#

3.2.7 TV encoder Implementation

Glamo 3362 can support TV encoder by LCD interface. Glamo 3362 connect to TV encoder can be configured as CPU mode or RGB mode, it is depends on the TV encoder. If the Glamo 3362 be configured as RGB mode, we recommend using pseudo master mode to connect TV encoder. In pseudo master mode, TV encoder output the Clock signal and input to Glamo 3362, then Glamo 3362 output RGB data, HSYNC, VSYNC signals to TV encode.

The figures below illustrate this implementation.

Figure 3.3.7-1 Connection of Glamo 3362 to TV Encoder



3.3 Video Interface

3.3.1 General Description

The Glamo 3362 provides a powerful video interface for most CCD/CMOS image sensors. It is designed to keep highly elasticity for users to communicate with most digital image sensors. There is a series interface that can be controlled by soft program to fit any series interface protocol. Besides, the Glamo 3362 provides a signal to control the external flashlight.

3.3.2 Video Interface Implementation

Video interface supports two modes for connecting sensor

- Mode1: When sensor provides a main clock input for sensor operation and a pixel clock out for latch pixel data, Glamo 3362 supports mode 1. (Such as Omnivision, Micron)
- Mode2: When sensor provides only one clock input for either sensor operation or latch pixel data, Glamo 3362 supports mode 2. (Such as Sony IU011)

Figure 3.3.2-1 Connection of Glamo 3362 to Sensor (Mode 1)

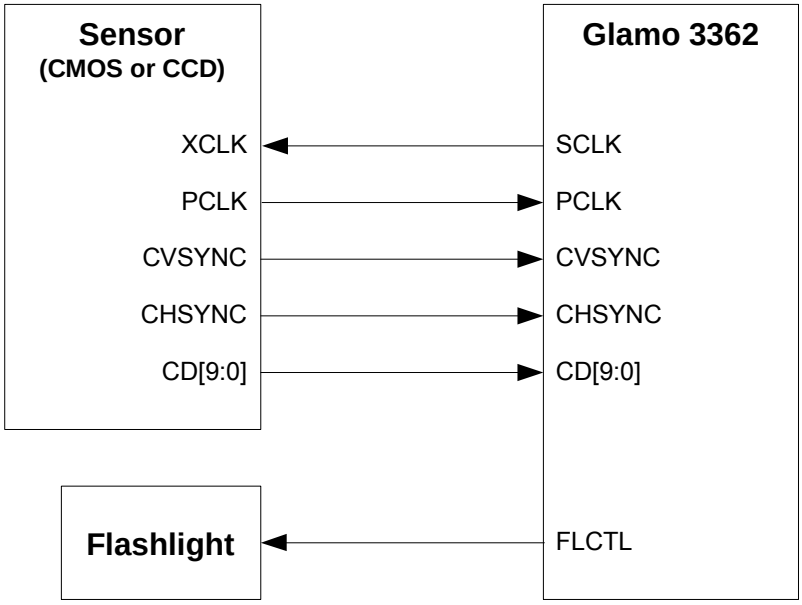
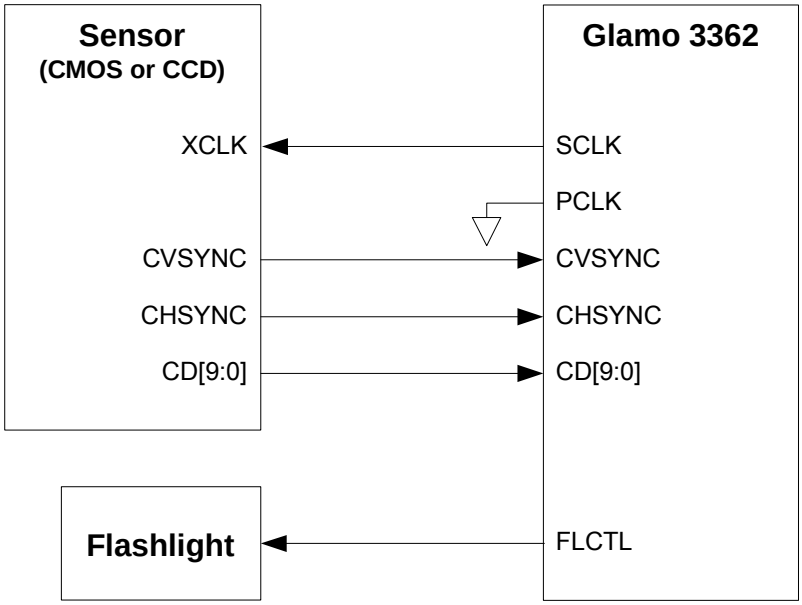


Figure 3.3.2-2 Connection of Glamo 3362 to Sensor (Mode 2)



3.3.3 Video Interface Timing Diagram

The video interface supports 4 input modes. The modes are positive CVSYNC with positive CHSYNC, positive CVSYNC with negative CHSYNC, negative CVSYNC with positive CHSYNC and negative CVSYNC with negative CHSYNC. The timing diagrams are showed as below.

Figure 3.3.3-1 Video Interface: Positive CVSYNC with Positive CHSYNC

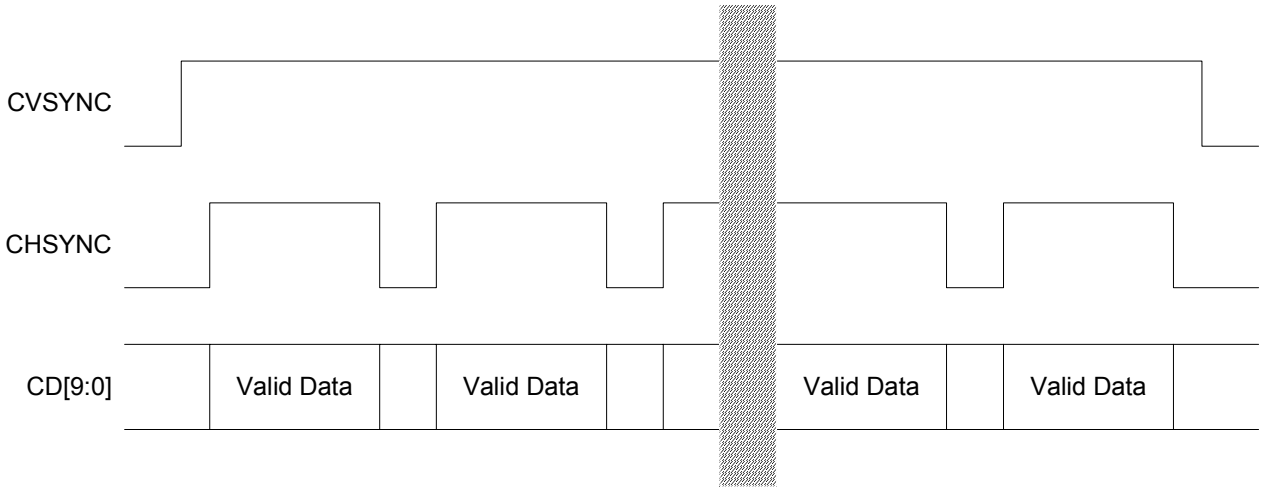


Figure 3.3.3-2 Video Interface: Positive CVSYNC with Negative CHSYNC

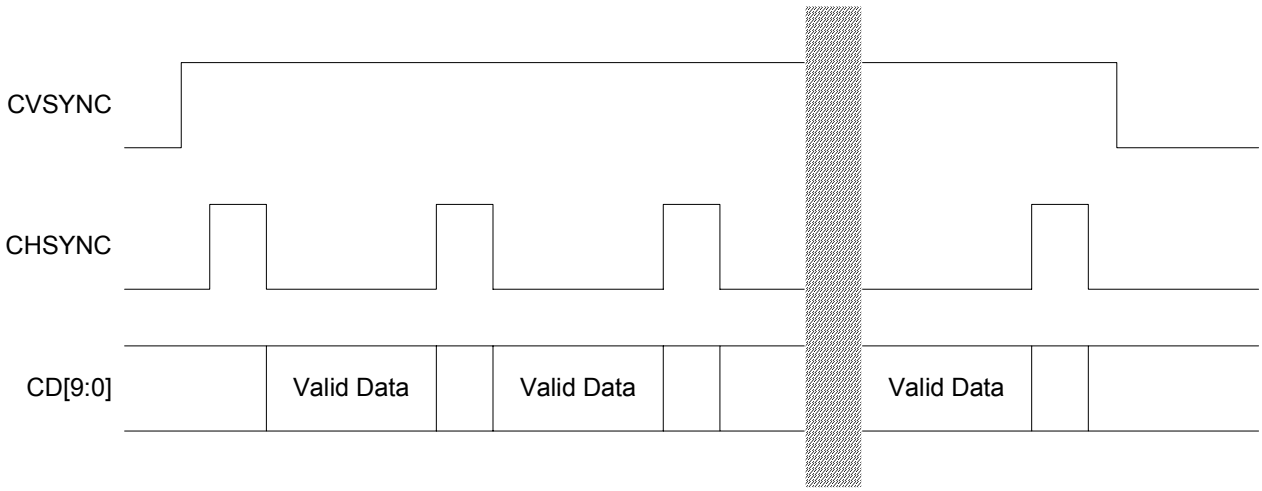


Figure 3.3.3-3 Video Interface: Negative CVSYNC with Positive CHSYNC

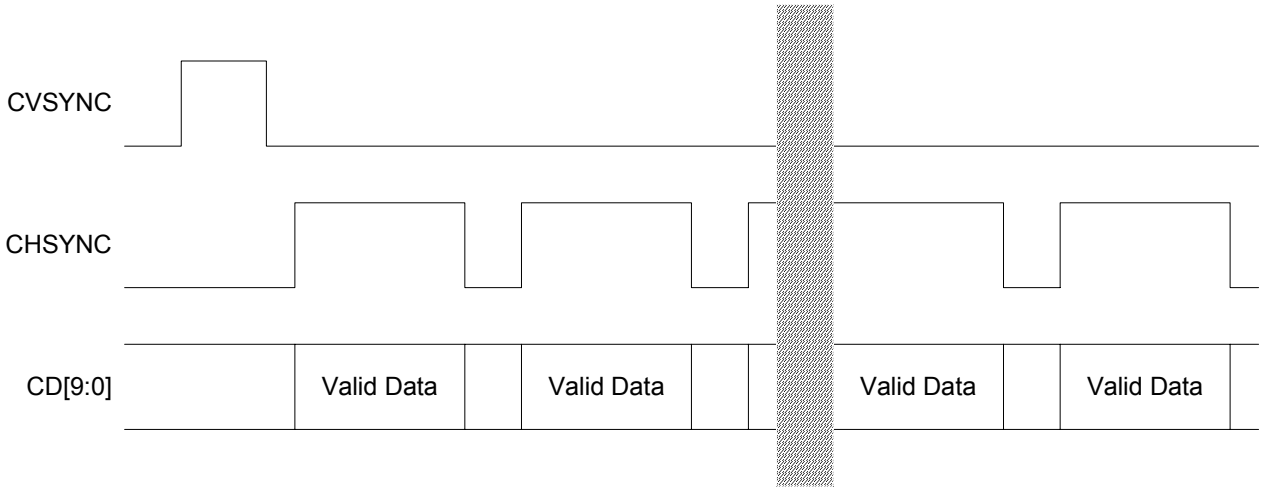
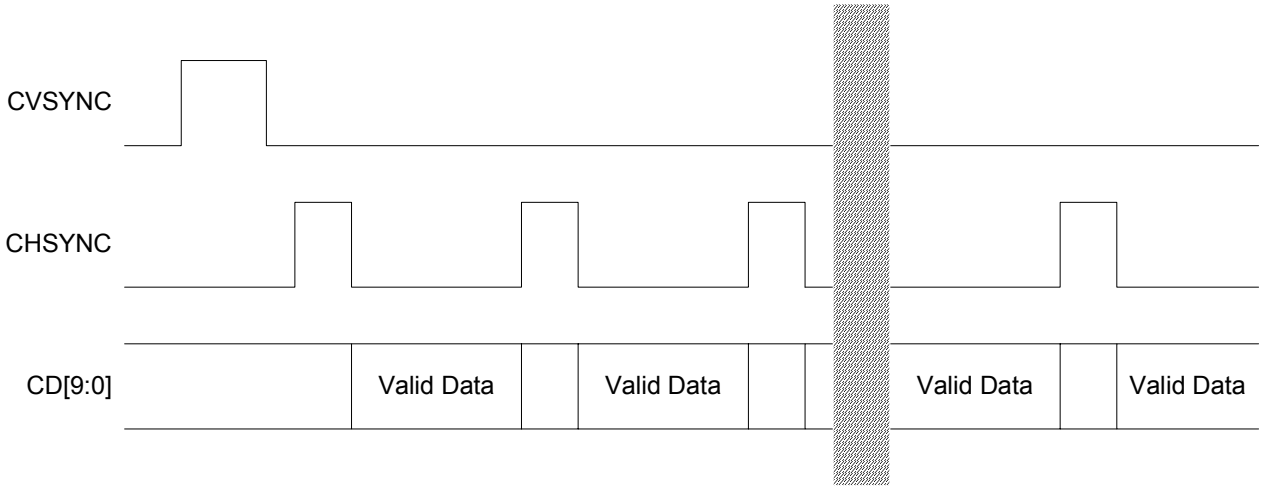
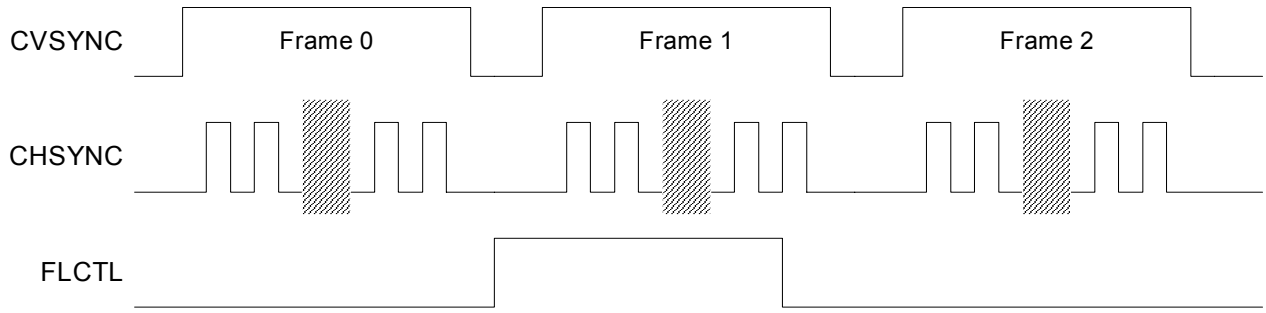


Figure 3.3.3-4 Video Interface: Negative CVSYNC with Negative CHSYNC



The video interface supports a programmable flashlight period. As below example, it can light the flash during frame 1 and take the frame 2 or latter.

Figure 3.3.3-5 Video Interface Flashlight Output



The timing diagram is showed in the Figure 4.2-4. The detail timing description is showed in the Table 4.2-2.

Figure 3.3.3-6 Video Capture Interface Timing Diagram

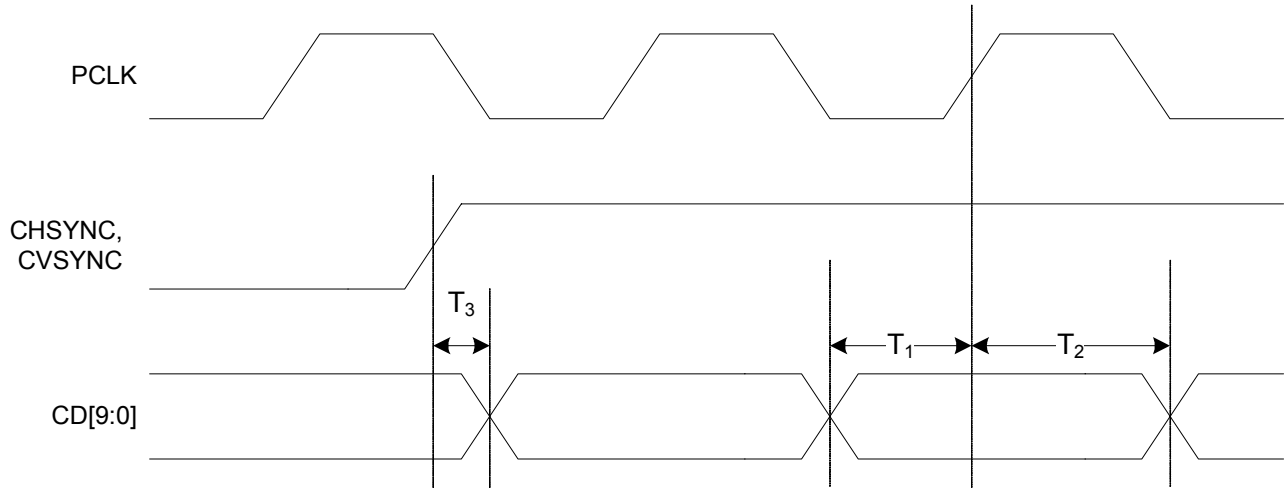


Table 3.3.3-1 Video Interface Timing Table

Symbol	Parameter	Min	Max	Unit
T_1	Pixel data setup time	8	-	ns
T_2	Pixel data hold time	2	-	ns
T_3	SYNC active time before pixel data	0	-	ns

3.4 MMC/SD Interface

3.4.1 General Description

The Glamo 3362 support MMC/SD card for user to storage the 3D games, JPEG image and MPEG-4 movies. It is convenient for user to put these data to the computer or download data from computer. The Glamo 3362 fully compliant with MMCA v3.3 and compliant with low-voltage support and 4 bits data of MMCA v4.0

3.4.2 MMC/SD Protocol

The Glamo 3362 supports both single and multiple block read/write. The figures below illustrate these basic MMC/SD protocol.

Figure 3.4.2-1 MMC/SD Command and Response Protocol

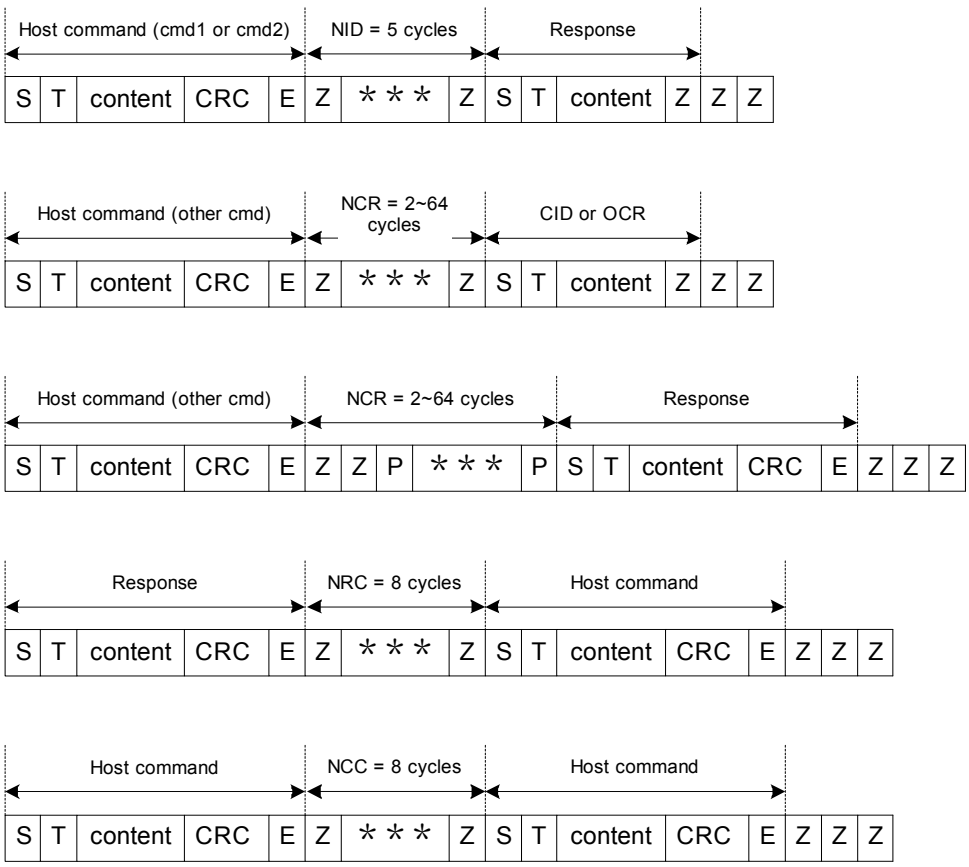


Figure 3.4.2-2 MMC/SD Single Block Read Protocol

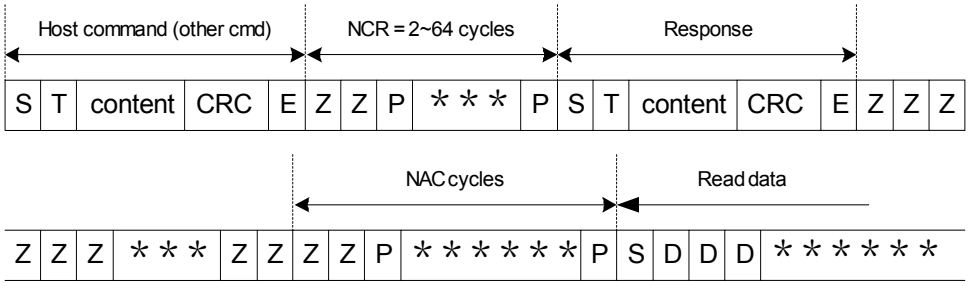


Figure 3.4.2-3 MMC/SD Multiple Block Read Protocol

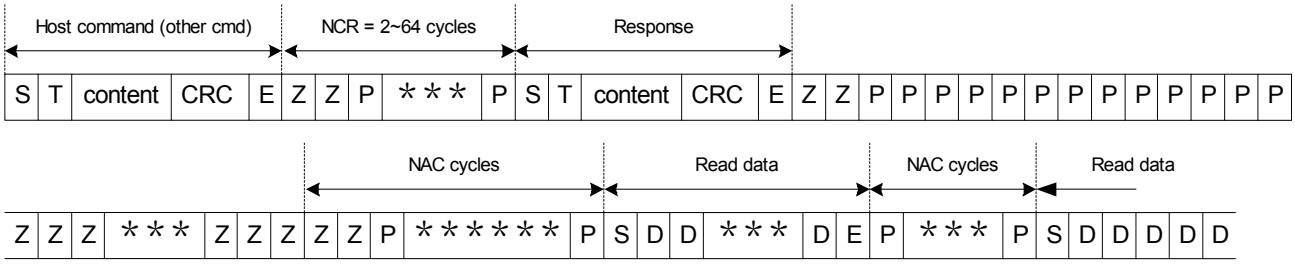


Figure 3.4.2-4 MMC/SD Single Block Write Protocol

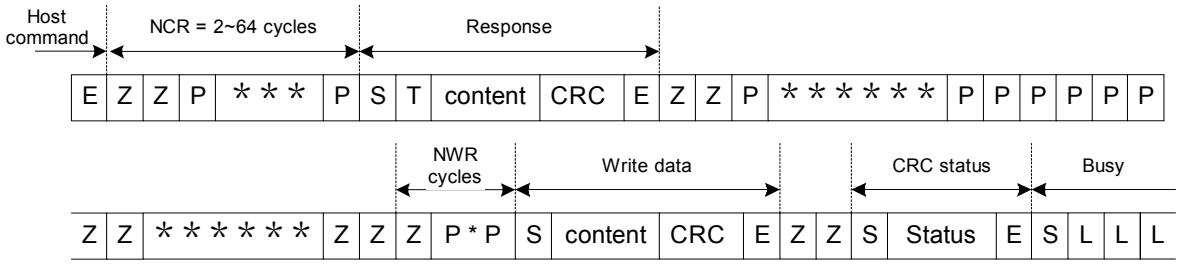
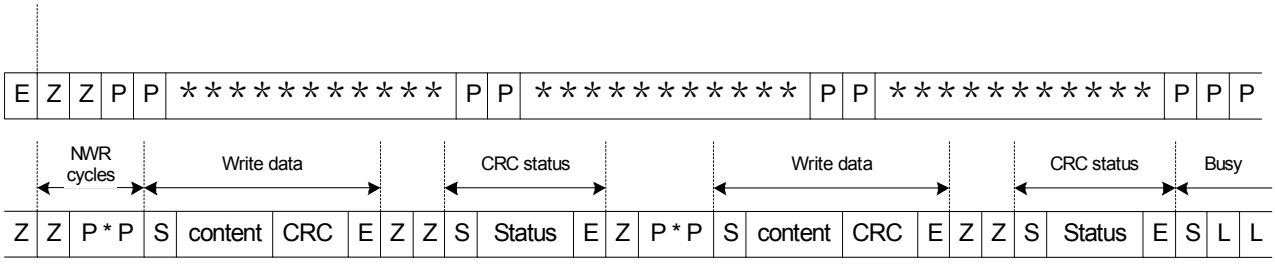


Figure 3.4.2-5 MMC/SD Multiple Block Write Protocol



3.4.3 MMC/SD Interface Timing Diagram

The MMC/SD Interface Timing diagram is showed in the Figure 4.3-6. The detail timing description is showed in the Table 4.3-1.

Figure 3.4.3-1 MMC/SD Interface Timing Diagram

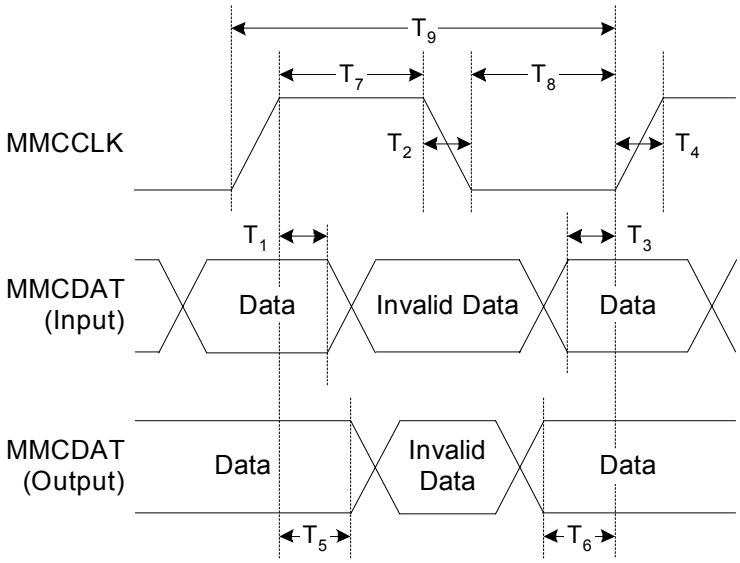


Table 3.4.3-1 MMC/SD Interface Timing Table

Symbol	Parameter	Min	Max	Unit
T_1	Input hold time	5	-	ns
T_2	Clock fall time	-	10	ns
T_3	Input set-up time	5	-	ns
T_4	Clock rise time	-	10	ns
T_5	Output hold time	3	-	ns
T_6	Output set-up time	3	-	ns
T_7	Clock high time	10	-	ns
T_8	Clock low time	10	-	ns
T_9	Clock cycle time	40	-	ns

3.5 PLL Interface

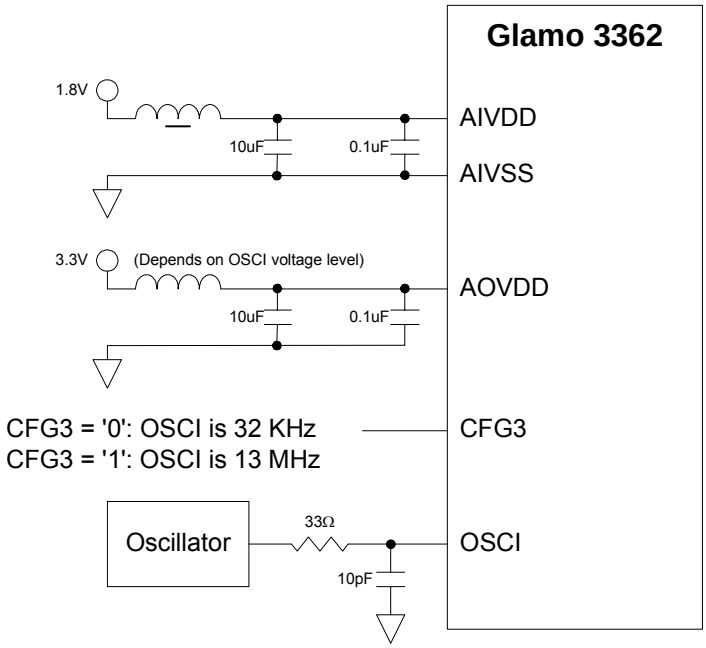
3.5.1 General Description

Glamo 3362 has two clock synthesizers to generate all of the internal clocks. The clock synthesizer can generate wide range of programmable frequencies, one is for up to 60MHz, and the other one is for up to 90MHz. The clock synthesizer accepts 32 KHz or 13 MHz reference clock input, which depends on the trapping value of CFG3. And system can even stop the reference clock after the PLL locked the target frequency and phase for power saving. The locking period is about 5ms. System can resend the reference clock and the PLL will automatically lock the target frequency and phase again. To meet the mobile application, the PLL contains the low power consumption, fast lock period, low clock jitter and flexible programming range features and automatically frequency and phase lock and relock scheme.

3.5.2 PLL Interface Implementation

The figure below illustrates the recommended implementation for PLL interface.

Figure 3.5.2-1 PLL Interface Implementation



3.6 General-Purpose I/O

3.6.1 General Description

The GPIO (general-purpose I/O) signals can be used to control and receive external devices or events. Glamo 3362 support 16 dedicated GPIO. For application flexibility, we divide these DGPIO into three group (group A, LCD and sensor Group). The voltage is set to be the same in the same group. In addition to the DGPIO, there are 21 GPIO pins that are shared with normal pins. Depending on physical usage, these normal pins can be programmed as GPIO pins. All of the GPIO pins are bi-directional; their directions are programmable by setting the internal registers.

3.6.2 GPIO Pins

The following table illustrates the mapping of GPIO pins.

Table 3.7.2-1 Mapping of GPIO Pins

GPIO Pin	Normal Pin
GPIO0	HA20
GPIO1	HA21

GPIO2	HA22
GPIO3	HA23
GPIO4	LCS0#
GPIO5	LCS1#
GPIO6	LDCLK
GPIO7	LDE#
GPIO8	LD16
GPIO9	LD17
GPIO10	LSCK
GPIO11	LSDA
GPIO12	LSA0
GPIO13	CSGPO0
GPIO14	CSGPO1
GPIO15	FLCTL
GPIO16	MMCDAT1
GPIO17	MMCDAT2
GPIO18	MMCDAT3
GPIO19	HADV#

Note: HA20, HA21, HA22, and HA23 can only be programmed as GPIO when using type 4 indirect addressing mode.

4 Electrical and Thermal Characteristics

4.1 Absolute Maximum Ratings

Table 4.1-1 Table of Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Core power (IVDD)	-0.3	2.0	V
Power for PLL (AIVDD)	-0.3	2.0	V
I/O power (AOVDD, COVDD, HOVDD, LOVDD, MOVDD, TOVDD)	-0.3	4.0	V
Input voltage	-0.3	OVDD+10%	V
Storage temperature	-40	125	^{0}C

NOTE: Violating these above may cause permanent damage on device. Functional operation of this device should be restricted to the conditions described under operating conditions.

4.2 Operating Conditions

Table 4.2-1 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD_{CORE}	Core power (IVDD)	1.7	1.8	1.9	V
VDD_{PLL}	Power for PLL (AIVDD)	1.7	1.8	1.9	V
MOVDD	Memory power	1.71	1.8	1.98	V
OVDD	I/O power (AOVDD, COVDD, HOVDD, LOVDD, MOVDD, TOVDD)	1.71	-	3.6	V
T_A	Operating ambient temperature	-25	-	85	^{0}C
T_J	Operating junction temperature	-25	-	100	^{0}C

4.3 DC Characteristics

Table 4.3-1 DC Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Output low voltage	Refer to I_{OL}	OVSS	OVSS+0.4	V
V_{OH}	Output high voltage	Refer to I_{OH}	OVDD-0.4	OVDD	V
I_{OH_S}	Output high current (with maximum driving strength)	OVDD=3.3V, V_{OH}=2.9V	3.03	5.58	mA
		OVDD=2.8V, V_{OH}=2.4V	2.77	5.37	mA
		OVDD=2.5V, V_{OH}=2.1V	2.57	5.17	mA
		OVDD=1.8V, V_{OH}=1.4V	1.91	4.34	mA
I_{OL_S}	Output low current (with maximum driving strength)	OVDD=3.3V, V_{OL}=0.4V	3.60	5.59	mA
		OVDD=2.8V, V_{OL}=0.4V	3.37	5.48	mA
		OVDD=2.5V, V_{OL}=0.4V	3.19	5.37	mA
		OVDD=1.8V, V_{OL}=0.4V	2.51	4.83	mA
I_{OH_W}	Output high current (with minimum driving strength)	OVDD=3.3V, V_{OH}=2.9V	1.20	2.23	mA
		OVDD=2.8V, V_{OH}=2.4V	1.11	2.14	mA
		OVDD=2.5V, V_{OH}=2.1V	1.03	2.07	mA
		OVDD=1.8V, V_{OH}=1.4V	0.76	1.74	mA

I_{OL_W}	Output low current (with minimum driving strength)	OVDD=3.3V, V_{OL}=0.4V	1.44	2.23	mA
		OVDD=2.8V, V_{OL}=0.4V	1.35	2.19	mA
		OVDD=2.5V, V_{OL}=0.4V	1.28	2.14	mA
		OVDD=1.8V, V_{OL}=0.4V	1.00	1.93	mA
I_{OZ}	Tristate leakage current		-	± 5	uA
V_{IL}	Input low voltage	OVDD=3.3V	-	1.35	V
		OVDD=2.8V	-	1.15	V
		OVDD=2.5V	-	1.00	V
		OVDD=1.8V	-	0.70	V
V_{IH}	Input high voltage	OVDD=3.3V	1.95	-	V
		OVDD=2.8V	1.65	-	V
		OVDD=2.5V	1.45	-	V
		OVDD=1.8V	1.05	-	V
I_{IN}	Input leakage current		-	± 1	uA
C_{IN}	Input capacitance		-	3	pF

4.4 AC Characteristics

4.4.1 Reset Timing

Figure 4.4-1 Reset Timing

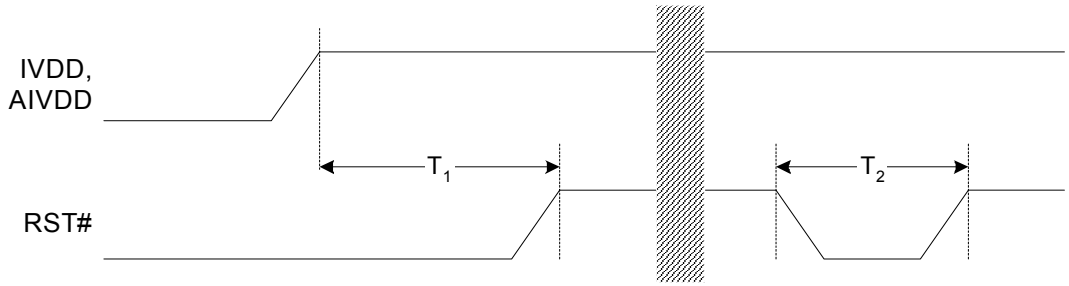


Table 5.4-1 Reset Timing Table

Symbol	Parameter	Min	Max	Unit
T_1	Power valid to reset inactive	1	-	ms
T_2	Minimum reset pulse width	1	-	us

Notes: When the reset process is finished, after 4 ms, you can access the registers.

4.4.2 Power Sequencing

All the I/O power and core power should be turned on or turn off as close as possible. If the power sources of Glamo 3362 can be turned on/off almost at the same time, there will be no specific sequencing requirements.

Figure 4.4.2-1 Power On/Off Sequencing

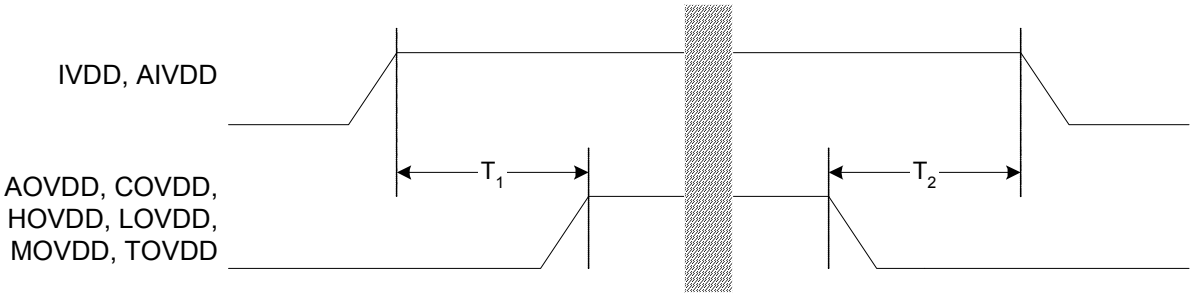
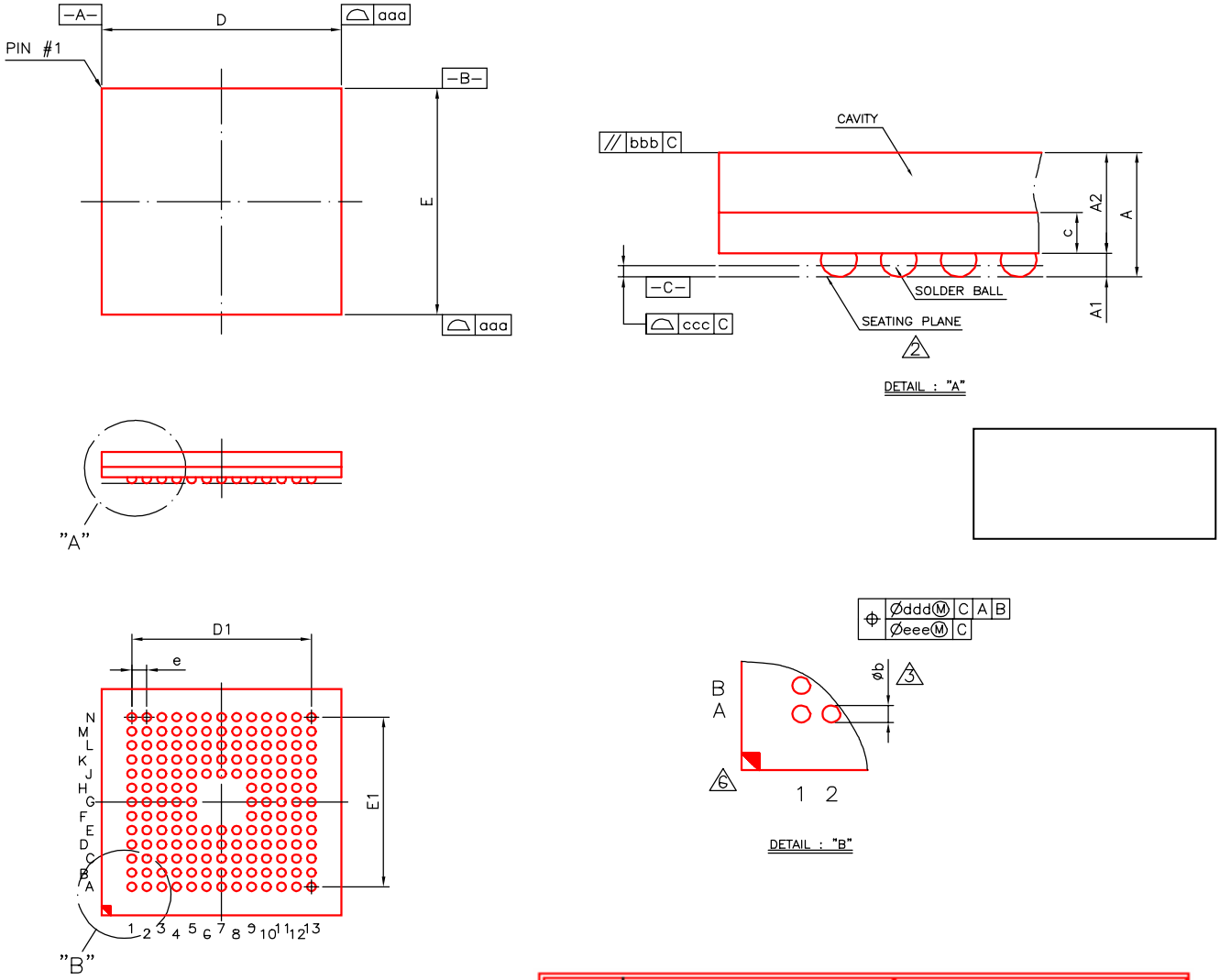


Table 4.4.2-1 Power On/Off Sequencing Table

Symbol	Parameter	Min	Max	Unit
T_1	Core power valid to IO power valid	0	1	us
T_2	IO power invalid to Core power invalid	0	1	us

5 Mechanical Dimension

Figure 5-1 Glamo 3362 8x8x1.3 160 Balls LFBGA Package (Unit: mm)



Bottom View

Top View

Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D1	---	6.00	---	---	0.236	---
E1	---	6.00	---	---	0.236	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
bbb		0.20			0.008	
ccc		0.10			0.004	
ddd		0.15			0.006	
eee		0.08			0.003	
MD/ME		13/13			13/13	

6 Memory

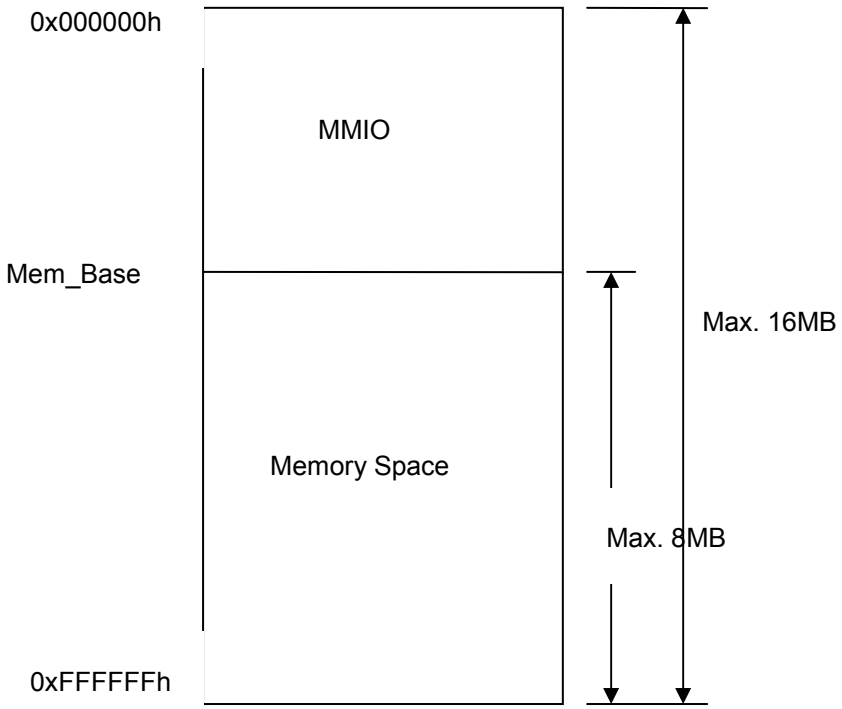
The memory is divided into two parts. One is mapping to the Glamo 3362 internal registers that we call it as Memory Map IO (MMIO) space. And the other is mapping to the stacked memory. The whole memory size is up to 16MBytes and the stacked memory size is maximum 8Mbytes. The physical memory size is depending on the stacked SDRAM or SRAM size.

The starting address of external memory is set on Mem_Base[23:1] which defined in Host Bus Controller Register 0x204h and 0x205h. For example, the default setting in the registers is 0x800000h. It means the starting address of stacked memory is 0x800000h. User can define the space by changing the Mem_Base setting.

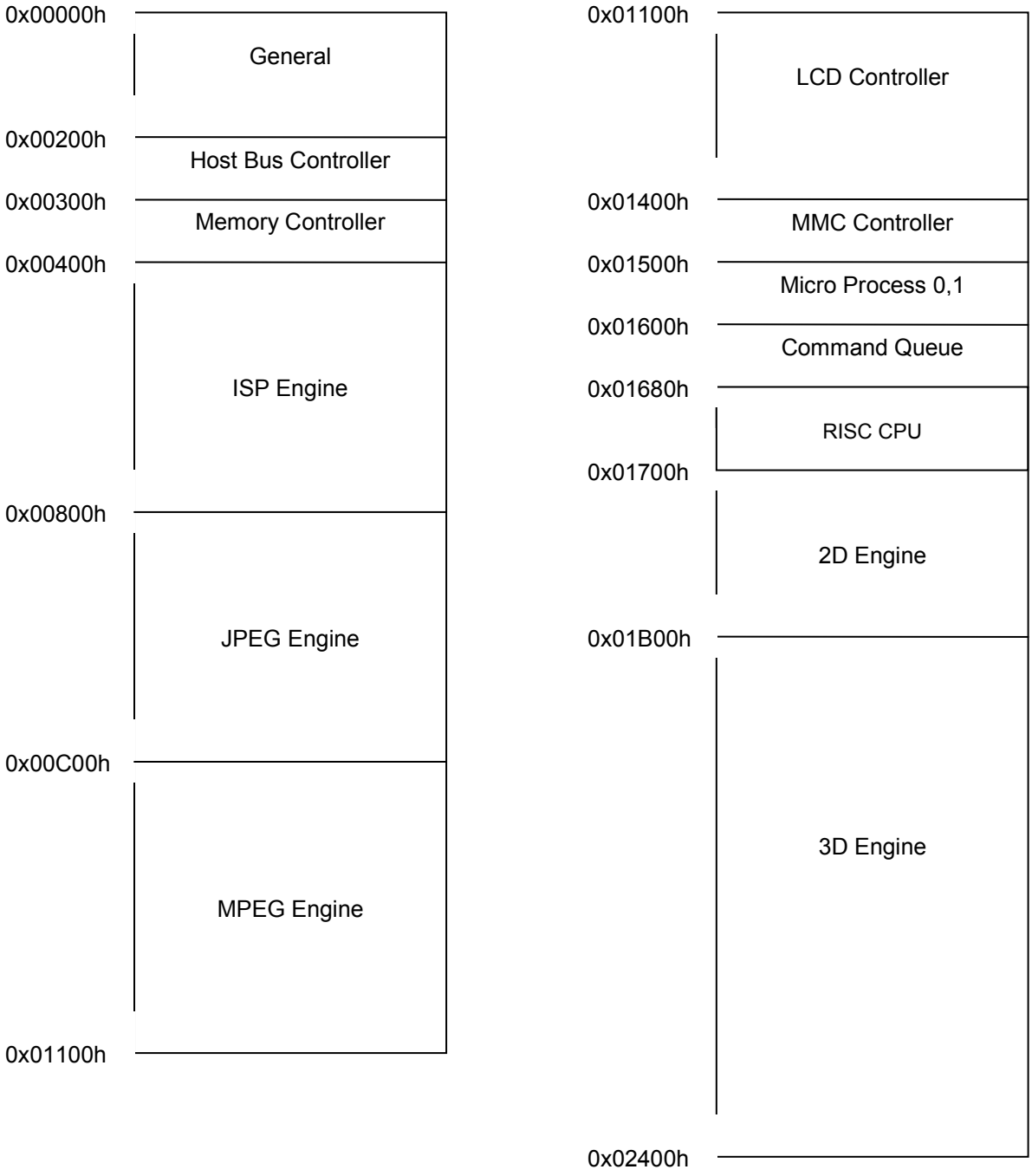
For example, if 2Mbytes SRAM is stacked and Mem_Base = 0x800000h. Then the actual memory space is from 0x800000h to 0x9FFFFFh.

Baseband CPU should set this memory space as non-cacheable space. Otherwise, it will lead to command delay action or data coherence error.

6.1 Memory Map

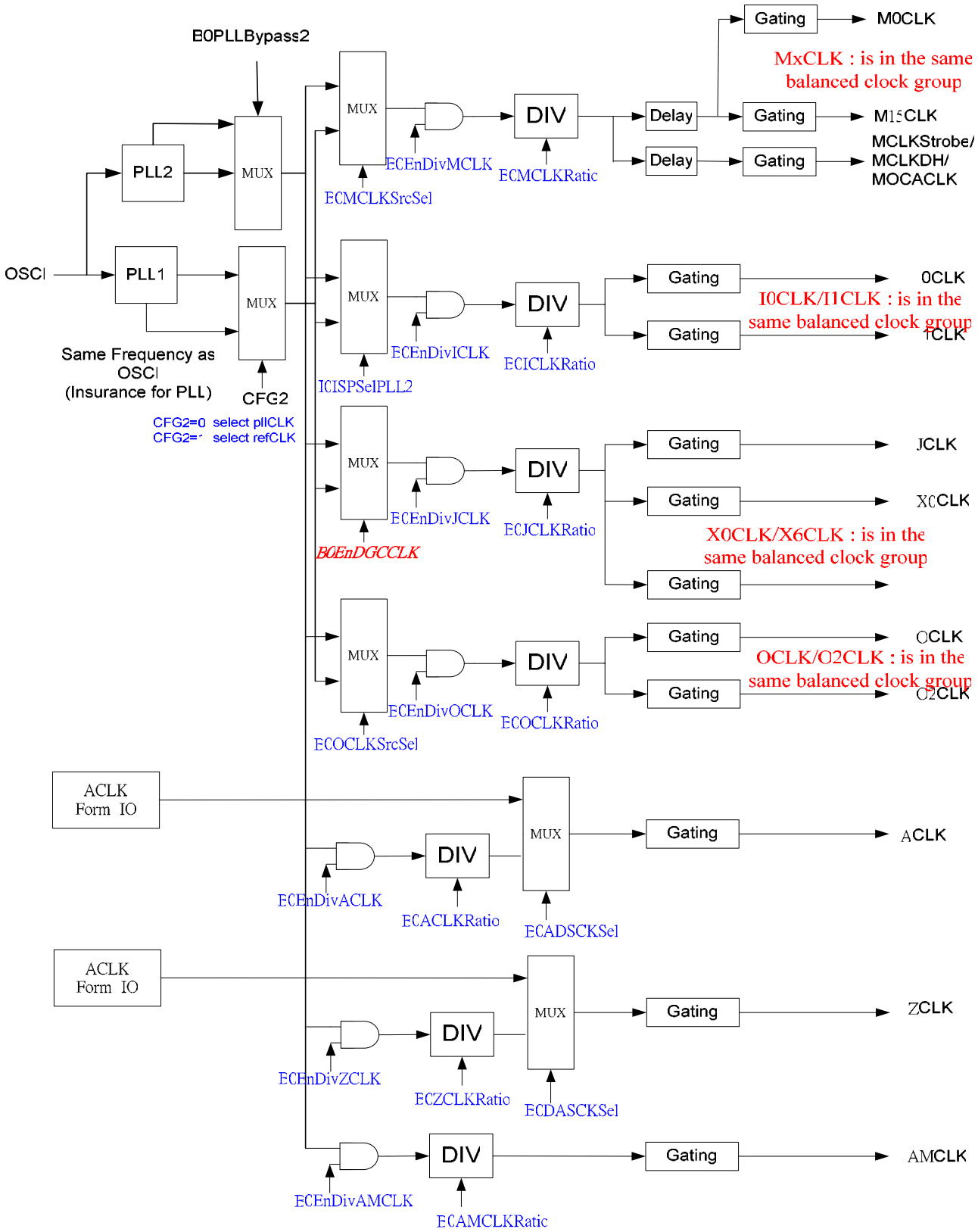


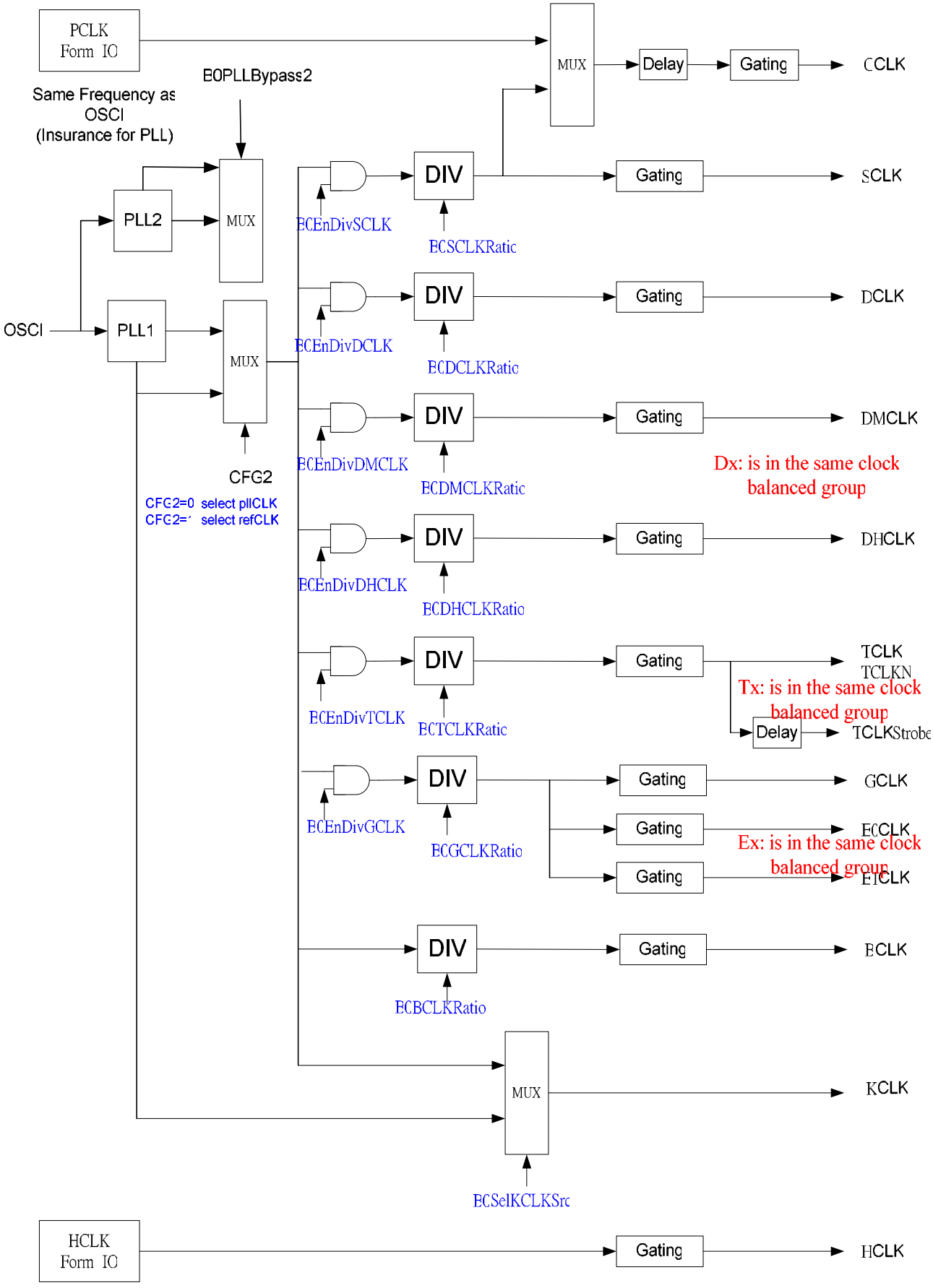
6.2 MMIO Map


0x00000h
General
0x00200h
Host Bus Controller
0x00300h
Memory Controller
0x00400h
ISP Engine
0x00800h
JPEG Engine
0x00C00h
MPEG Engine
0x01100h
0x01100h
LCD Controller
0x01400h
MMC Controller
0x01500h
Micro Process 0,1
0x01600h
Command Queue
0x01680h
RISC CPU
0x01700h
2D Engine
0x01B00h
3D Engine
0x02400h

7 Clocks

7.1 Clock Diagram




PCLK
Form IO
MUX
Delay
Gating
CCLK
E0PLLBypass2
Same Frequency as
OSCI
(Insurance for PLL)
PLL2
MUX
DIV
Gating
SCLK
ECEnDivSCLK
ECSCLKRatic
OSCI
PLL1
MUX
DIV
Gating
DCLK
ECEnDivDCLK
ECDCLKRatic
DIV
Gating
DMCLK
ECEnDivDMCLK
ECDMCLKRatic
Dx: is in the same clock
balanced group
CFG2
CFG2=0 select pllCLK
CFG2=' select refCLK
DIV
Gating
DHCLK
ECEnDivDHCLK
ECDHCLKRatio
DIV
Gating
TCLK
TCLKN
ECEnDivTCLK
ECTCLKRatic
Tx: is in the same clock
balanced group
Delay
TCLKStrobe
DIV
Gating
GCLK
ECEnDivGCLK
ECGCLKRatio
Gating
ECLK
Ex: is in the same clock
balanced group
Gating
EICLK
DIV
Gating
BCLK
ECBCLKRatio
MUX
KCLK
ECSelKCLKSrc
HCLK
Form IO
Gating
HCLK

7.2 Clocks

For power saving, each module has its own clock tree and can be Enable/Disable or divided frequency separately. In General Clock registers 0x0010h~0x0026h define the clock setting of each module.

Host Bus Clock (BCLK)

This clock is used for host bus controller and register banks of all internal modules. It can be divided using BCLK_Ratio. Turn on dynamic gating by En_DG_BCLK for power saving. This clock is always turn on, so there is no enable bit for it.

Image Processor 1 Clock (CCLK)

This clock is used for image signal processor 1. Its clock source is chose by Sel_CCLK_Src. One source is from external input clock PCLK, another source is from SCLK. The clock phase can be programmed by CCLK_Dly. Enable this clock by En_CCLK and turn on dynamic gating by En_DG_CCLK for power saving.

Image Processor 2 Clock (I1CLK)

This clock is used for image signal processor 2. Its clock source is chose by I0ISPSelPLL2. One source is from external input clock PLL1, another source is from PLL2. Set En_Div_ICLK for passing clock to the clock divider. It can be divided using ICLK_Ratio. Enable this clock by En_I1CLK and turn on dynamic gating by En_DG_I1CLK for power saving.

LCD Controller Clock 1 (DCLK)

This clock is used for LCD controller as the pixel clock. Set En_Div_DCLK for passing clock to the clock divider. It can be divided using DCLK_Ratio. Enable this clock by En_DCLK and turn on dynamic gating by En_DG_DCLK for power saving.

LCD Controller Clock 2 (DHCLK)

This clock is used for LCD controller. Set En_Div_DHCLK for passing clock to the clock divider. It can be divided using DHCLK_Ratio. Enable this clock by En_DHCLK. It does not have dynamic gating ability.

LCD Controller Clock 3 (DMCLK)

This clock is used for LCD controller. Set En_Div_DMCLK for passing clock to the clock divider. It can be divided using DMCLK_Ratio. Enable this clock by En_DMCLK and turn on dynamic gating by En_DG_DMCLK for power saving.

3D Engine Clock 1 (E0CLK)

This clock is used for 3D engine. It shares the same clock divider with E0CLK and GCLK. Set En_Div_GCLK for passing clock to the clock divider. It can be divided using GCLK_Ratio. Enable this clock by En_E0CLK and turn on dynamic gating by En_DG_E0CLK for power saving.

3D Engine Clock 2 (E1CLK)

This clock is used for 3D engine. It shares the same clock divider with E0CLK and GCLK. Set En_Div_GCLK for passing clock to the clock divider. It can be divided using GCLK_Ratio. Enable this clock by En_E1CLK and turn on dynamic gating by En_DG_E1CLK for power saving.

2D Engine Clock (GCLK)

This clock is used for 2D engine. It shares the same clock divider with E0CLK and E1CLK. Set

En_Div_GCLK for passing clock to the clock divider. It can be divided using GCLK_Ratio. Enable this clock by En_GCLK and turn on dynamic gating by En_DG_GCLK for power saving.

Host Bus Clock for iBurst Mode (HCLK)

This clock is used for host bus controller in iBurst mode. When CFG[1:0]=10, the CPU bus uses Type 3 iBurst mode. In this mode the clock comes from the pin HA2.

Micro Processor 1 Clock (I0CLK)

This clock is used for micro processor 0. Its clock source is chose by I0ISPSelPLL2. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with I0CLKand I1CLK. Set En_Div_ICLK for passing clock to the clock divider. It can be divided using ICLK_Ratio. Enable this clock by En_I0CLK and turn on dynamic gating by En_DG_I0CLK for power saving.

Micro Processor 2 Clock (X5CLK)

This clock is used for image signal processor 2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X5CLK and turn on dynamic gating by En_DG_X5CLK for power saving.

JPEG Engine Clock (JCLK)

This clock is used for JPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with I0CLK, I1CLK and X0CLK~X5CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_JCLK and turn on dynamic gating by En_DG_JCLK for power saving.

MPEG Engine Clock 1 (X0CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X0CLK and turn on dynamic gating by En_DG_X0CLK for power saving.

MPEG Engine Clock 2 (X1CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X1CLK and turn on dynamic gating by En_DG_X1CLK for power saving.

MPEG Engine Clock 3 (X2CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X2CLK and turn on dynamic gating by En_DG_X2CLK for power saving.

MPEG Engine Clock 4 (X3CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X3CLK and turn on dynamic gating by En_DG_X3CLK for power saving.

MPEG Engine Clock 5 (X4CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X4CLK and turn on dynamic gating by En_DG_X4CLK for power saving.

MPEG Engine Clock 6 (X5CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X5CLK and turn on dynamic gating by En_DG_X5CLK for power saving.

MPEG Engine Clock 7 (X6CLK)

This clock is used for MPEG engine. Its clock source is chose by B0EnDGCCLK. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with JCLK and X0CLK~X6CLK. Set En_Div_JCLK for passing clock to the clock divider. It can be divided using JCLK_Ratio. Enable this clock by En_X6CLK and turn on dynamic gating by En_DG_X6CLK for power saving.

System Timer Clock (KCLK)

This clock is for Accurate timer. This clock may come from two source, one is from external input clock OSCI and the other is from PLL. The clock source is chosed by Sel_KCLK_Src and enable this clock by En_KCLK.

Sensor Clock (SCLK)

This clock is used for sensor interface. Set En_Div_SCLK for passing clock to the clock divider. It can be divided using SCLK_Ratio. Enable this clock by En_SCLK. It does not have dynamic gating ability.

MMC Controller Clock (TCLK)

This clock is used for MMC controller. Set En_Div_TCLK for passing clock to the clock divider. It can be divided using TCLK_Ratio. Enable this clock by En_TCLK and turn on dynamic gating by En_DG_TCLK for power saving.

Memory Clock in Host Bus Controller (M0CLK)

This clock is used for host bus controller. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using

MCLK_Ratio. Enable this clock by En_M0CLK and turn on dynamic gating by En_DG_M0CLK for power saving.

Memory Clock in Memory Controller (M1CLK)

This clock is used for memory controller. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M1CLK and turn on dynamic gating by En_DG_M1CLK for power saving.

Memory Clock in ISP Engine (M2CLK)

This clock is used for image signal processor. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M2CLK and turn on dynamic gating by En_DG_M2CLK for power saving.

Memory Clock in JPEG Engine (M3CLK)

This clock is used for JPEG engine. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M3CLK and turn on dynamic gating by En_DG_M3CLK for power saving.

Memory Clock in MPEG Engine (M4CLK)

This clock is used for MPEG engine. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M4CLK and turn on dynamic gating by En_DG_M4CLK for power saving.

Memory Clock in LCD Controller (M5CLK)

This clock is used for LCD controller. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M5CLK and turn on dynamic gating by En_DG_M5CLK for power saving.

Memory Clock in Command Queue Controller (M6CLK)

This clock is used for command queue. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M6CLK and turn on dynamic gating by En_DG_M6CLK for power saving.

Memory Clock in 2D Engine (M7CLK)

This clock is used for 2D engine. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M7CLK and turn on dynamic gating by En_DG_M7CLK for power saving.

Memory Clock in 3D Engine (M8CLK)

This clock is used for 3D engine. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M8CLK and turn on dynamic gating by En_DG_M8CLK for power saving.

Memory Clock in MMC Engine (M9CLK)

This clock is used for MMC controller. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M9CLK and turn on dynamic gating by En_DG_M9CLK for power saving.

Memory Clock in Micro Processor 1 (M10CLK)

This clock is used for Micro Processor 1. Its clock source is chose by B0MCLKSrcSel. One source is from external input clock PLL1, another source is from PLL2. It shares the same clock divider with M0CLK~M15CLK. Set En_Div_MCLK for passing clock to the clock divider. It can be divided using MCLK_Ratio. Enable this clock by En_M10CLK and turn on dynamic gating by En_DG_M10CLK for power saving.

Memory Clock to Sample Write Data (MCLKDH)

This clock is used for adjusting the write data timing of the memory interface. The clock phase can be programmed by MCLKDH_Dly. Enable this clock by En_MCLKDH and turn on dynamic gating by En_DG_MCLKDH for power saving.

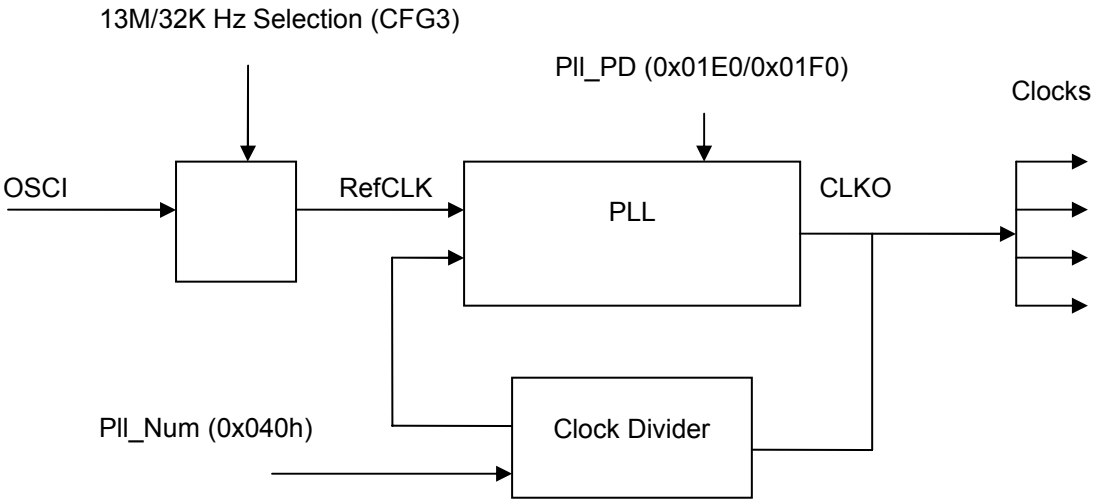
Memory Clock to Strobe Read Data (MCLKStrobe)

This clock is used for adjusting the read data timing of the memory interface. The clock phase can be programmed by MCLKStrobe_Dly. Enable this clock by En_MCLKStrobe and turn on dynamic gating by En_DG_MCLKStrobe for power saving.

Memory Clock to SDRAM (MOCACLK)

This clock is used for memory interface as the output clock to SDRAM. The clock phase can be programmed by MOCACLK_Dly. Enable this clock by En_MOCACLK.

7.3 Phase Lock Loop (PLL)



Glamo 3362 has two clock synthesizers to generate all of the internal clocks. The clock synthesizers can generate wide range of programmable frequencies. It can provide 1 MHz to 90 MHz flexible working frequency. The clock synthesizer accepts 32 KHz or 13 MHz reference clock input, which depends on the trapping value of CFG3 (0:32 KHz, 1:13 MHz). And system can even stop the reference clock after the PLL has locked the target frequency and phase for power saving. The period that system would need to lock the target frequency is about 5ms. System can resend the reference clock and the PLLs will automatically lock the target frequency and phase again. To meet the mobile application requirement, the PLLs have low power consumption, fast lock period, low clock jitter, flexible programming range, automatically frequency, phase lock and relock scheme. The frequency setting for PLL1 is defined in General register 0x0040h. In deep power saving mode, the PLL1 can be power down by setting the Pll_PD to 1 by writing 0x01E0h address with any data. And write 0x01F0h address to return to normal operation. The frequency setting for PLL2 is defined in General register 0x0044h. In deep power saving mode, the PLL2 can be power down by setting the Pll_PD2 to 1 by writing 0x044h D[13]. And disable 0x0044h D[13] to return to normal operation.

8 Power Management

For efficiency control the power consumption, to control the clock gating and divider is very important task for power management. The following table shows the suggestions of clock gating and divider for each operation mode. In addition to the dynamic clock gating control for each module, the Glamo 3362 embeds one hardware clock gating control.

	BCLK, M0CLK	CCLK, I0,I1CLK, M2CLK, M15CLK	DCLK, DHCLK, DMCLK, M5CLK	E0CLK, E1CLK, M6CLK, M8CLK	GCLK, M6CLK, M7CLK	JCLK, M3CLK	X0,X1,X2,X3,X5CLK+M4CLK	X0,X2,X4CLK+M4CLK	SCLK	TCLK, M9CLK	M1CLK	PLL	OCLK, M11~12CLK,ZCLK,AMCLK	OCLK, M13~14CLK,ACLK,AMCLK
HW Dynamic Clock Gating	V	-	-	V	V	-	V	V	-	-	V	-		
Deep Power Down Mode	-	-	-	-	-	-	-	-	-	-	-	-		
LCD Bypass Mode	-	-	-	-	-	-	-	-	-	-	-	-		
Standby Mode	-	-	-	-	-	-	-	-	-	-	-	-		
Partial Display Mode	V	-	V	-	-	-	-	-	-	-	-	V		
Full Static Display	V	-	V	-	-	-	-	-	-	-	V	V		
2D Application	V	-	V	-	V	-	-	-	-	-	V	V		
3D Application	V	-	V	V	-	-	-	-	-	-	V	V		
Preview Mode	V	V	V	-	-	-	-	-	V	-	V	V		
SnapShot Mode	V	V	V	-	-	V	-	-	V	-	V	V		
Video Recording Mode	V	V	V	-	-	-	V	-	V	-	V	V		
Image Viewing Mode	V	V	V	-	-	V	-	-	-	-	V	V		

Video Playback Mode	V	V	V	-	-	-	-	V	-	-	V	V
MMC/SD Access	V	-	V	-	-	-	-	-	-	V	V	V

Note:

1. HW Dynamic Clock Gating means Glamo 3362 supports dynamic clock gating architecture. Hardware module will monitor the engine status. If no new command is received and further staying in idle, the engine will automatically turn off the related clocks. But once any new command is received, the engine will enable the clock in next cycle and further enter normal operation.
2. In this table, we assume the non-memory LCD module is used and Glamo 3362 takes the LCD refresh task.
3. In deep power-down Mode, Glamo 3362 only consumes leakage current. After entering this mode, the data inside the stacked memory will not be guaranteed to keep well.
4. In Standby Mode, all the clocks and PLLs are turned off. After entering this mode, the data inside the stacked memory will be well kept.

9 Function Description

9.1 LCD Display

9.1.1 Display Data Format

Glamo 3362 supports kinds of data formats, and the LCD display related register is defined in LCD Register 0x1104h. Follow explains each data format.

6bits Mode RGB666 (RGB Interface Only)

Table 6bits Mode RGB666

Cycle	0	1	2	……..	3n	3n+1	3n+2
D5	$R_{0}5$	$G_{0}5$	$B_{0}5$		$R_{n}5$	$G_{n}5$	$B_{n}5$
D4	$R_{0}4$	$G_{0}4$	$B_{0}4$		$R_{n}4$	$G_{n}4$	$B_{n}4$
D3	$R_{0}3$	$G_{0}3$	$B_{0}3$		$R_{n}3$	$G_{n}3$	$B_{n}3$
D2	$R_{0}2$	$G_{0}2$	$B_{0}2$		$R_{n}2$	$G_{n}2$	$B_{n}2$
D1	$R_{0}1$	$G_{0}1$	$B_{0}1$		$R_{n}1$	$G_{n}1$	$B_{n}1$
D0	$R_{0}0$	$G_{0}0$	$B_{0}0$		$R_{n}0$	$G_{n}0$	$B_{n}0$

8bits Mode RGB332 (CPU Interface Only)

Table 8bits Mode RG332

Cycle	0	1	……..	n
D7	$R_{0}2$	$R_{1}2$		$R_{n}2$
D6	$R_{0}1$	$R_{1}1$		$R_{n}1$
D5	$R_{0}0$	$R_{1}0$		$R_{n}0$
D4	$G_{0}2$	$G_{1}2$		$G_{n}2$
D3	$G_{0}1$	$G_{1}1$		$G_{n}1$
D2	$G_{0}0$	$G_{1}0$		$G_{n}0$
D1	$B_{0}1$	$B_{1}1$		$B_{n}1$
D0	$B_{0}0$	$B_{1}0$		$B_{n}0$

8bits Mode RGB444 (CPU Interface Only)

Table 8bits Mode RGB444 (XR_GB)

Cycle	0	1	……..	2n	2n+1
D7	X	$G_{0}3$		X	$G_{n}3$
D6	X	$G_{0}2$		X	$G_{n}2$
D5	X	$G_{0}1$		X	$G_{n}1$
D4	X	$G_{0}0$		X	$G_{n}0$
D3	$R_{0}3$	$B_{0}3$		$R_{n}3$	$B_{n}3$
D2	$R_{0}2$	$B_{0}2$		$R_{n}2$	$B_{n}2$
D1	$R_{0}1$	$B_{0}1$		$R_{n}1$	$B_{n}1$
D0	$R_{0}0$	$B_{0}0$		$R_{n}0$	$B_{n}0$

Table 8bits Mode RGB444 (RX_GB)

Cycle	0	1	……..	2n	2n+1
D7	$R_{0}3$	$G_{0}3$		$R_{n}3$	$G_{n}3$
D6	$R_{0}2$	$G_{0}2$		$R_{n}2$	$G_{n}2$
D5	$R_{0}1$	$G_{0}1$		$R_{n}1$	$G_{n}1$
D4	$R_{0}0$	$G_{0}0$		$R_{n}0$	$G_{n}0$
D3	X	$B_{0}3$		X	$B_{n}3$
D2	X	$B_{0}2$		X	$B_{n}2$
D1	X	$B_{0}1$		X	$B_{n}1$
D0	X	$B_{0}0$		X	$B_{n}0$

Table 8bits Mode RGB444 (RG_BX)

Cycle	0	1	……..	2n	2n+1
D7	$R_{0}3$	$B_{0}3$		$R_{n}3$	$B_{n}3$
D6	$R_{0}2$	$B_{0}2$		$R_{n}2$	$B_{n}2$
D5	$R_{0}1$	$B_{0}1$		$R_{n}1$	$B_{n}1$

D4	$R_{0}0$	$B_{0}0$		$R_{n}0$	$B_{n}0$
D3	$G_{0}3$	X		$G_{n}3$	X
D2	$G_{0}2$	X		$G_{n}2$	X
D1	$G_{0}1$	X		$G_{n}1$	X
D0	$G_{0}0$	X		$G_{n}0$	X

Table 8bits Mode RGB444 (RG_XB)

Cycle	0	1	……..	2n	2n+1
D7	$R_{0}3$	X		$R_{n}3$	X
D6	$R_{0}2$	X		$R_{n}2$	X
D5	$R_{0}1$	X		$R_{n}1$	X
D4	$R_{0}0$	X		$R_{n}0$	X
D3	$G_{0}3$	$B_{0}3$		$G_{n}3$	$B_{n}3$
D2	$G_{0}2$	$B_{0}2$		$G_{n}2$	$B_{n}2$
D1	$G_{0}1$	$B_{0}1$		$G_{n}1$	$B_{n}1$
D0	$G_{0}0$	$B_{0}0$		$G_{n}0$	$B_{n}0$

Table 8bits Mode RGB444 (RG_BR_GB)

Cycle	0	1	2	……..	3n/2	3n/2+1	3n/2+2
D7	$R_{0}3$	$B_{0}3$	$G_{1}3$		$R_{n}3$	$B_{n}3$	$G_{n+1}3$
D6	$R_{0}2$	$B_{0}2$	$G_{1}2$		$R_{n}2$	$B_{n}2$	$G_{n+1}2$
D5	$R_{0}1$	$B_{0}1$	$G_{1}1$		$R_{n}1$	$B_{n}1$	$G_{n+1}1$
D4	$R_{0}0$	$B_{0}0$	$G_{1}0$		$R_{n}0$	$B_{n}0$	$G_{n+1}0$
D3	$G_{0}3$	$R_{1}3$	$B_{1}3$		$G_{n}3$	$R_{n+1}3$	$B_{n+1}3$
D2	$G_{0}2$	$R_{1}2$	$B_{1}2$		$G_{n}2$	$R_{n+1}2$	$B_{n+1}2$
D1	$G_{0}1$	$R_{1}1$	$B_{1}1$		$G_{n}1$	$R_{n+1}1$	$B_{n+1}1$
D0	$G_{0}0$	$R_{1}0$	$B_{1}0$		$G_{n}0$	$R_{n+1}0$	$B_{n+1}0$

8bits Mode RGB565 (CPU Interface Only)

Table 8bits Mode RGB565

Cycle	0	1	……..	2n	2n+1
D7	R_{05}	G_{02}		R_{n4}	G_{n2}
D6	R_{03}	G_{01}		R_{n3}	G_{n1}
D5	R_{02}	G_{00}		R_{n2}	G_{n0}
D4	R_{01}	B_{04}		R_{n1}	B_{n4}
D3	R_{00}	B_{03}		R_{n0}	B_{n3}
D2	G_{05}	B_{02}		G_{n5}	B_{n2}
D1	G_{04}	B_{01}		G_{n4}	B_{n1}
D0	G_{03}	B_{00}		G_{n3}	B_{n0}

8bits Mode RGB666 (CPU Interface Only)

Table 8bits Mode RGB666 (XR_XG_XB)

Cycle	0	1	2	……..	3n	3n+1	3n+2
D7	X	X	X	X	X	X	X
D8	X	X	X	X	X	X	X
D5	R_{05}	G_{05}	B_{05}		R_{n5}	G_{n5}	B_{n5}
D4	R_{04}	G_{04}	B_{04}		R_{n4}	G_{n4}	B_{n4}
D3	R_{03}	G_{03}	B_{03}		R_{n3}	G_{n3}	B_{n3}
D2	R_{02}	G_{02}	B_{02}		R_{n2}	G_{n2}	B_{n2}
D1	R_{01}	G_{01}	B_{01}		R_{n1}	G_{n1}	B_{n1}
D0	R_{00}	G_{00}	B_{00}		R_{n0}	G_{n0}	B_{n0}

Table 8bits Mode RGB666 (RX_GX_BX)

Cycle	0	1	2	……..	3n	3n+1	3n+2
D7	R_{05}	G_{05}	B_{05}		R_{n5}	G_{n5}	B_{n5}
D8	R_{04}	G_{04}	B_{04}		R_{n4}	G_{n4}	B_{n4}
D5	R_{03}	G_{03}	B_{03}		R_{n3}	G_{n3}	B_{n3}

D4	$R_{0}2$	$G_{0}2$	$B_{0}2$		$R_{n}2$	$G_{n}2$	$B_{n}2$
D3	$R_{0}1$	$G_{0}1$	$B_{0}1$		$R_{n}1$	$G_{n}1$	$B_{n}1$
D2	$R_{0}0$	$G_{0}0$	$B_{0}0$		$R_{n}0$	$G_{n}0$	$B_{n}0$
D1	X	X	X	X	X	X	X
D0	X	X	X	X	X	X	X

9bits Mode RGB666 (Both in CPU and RGB Interface)

Table 9bits Mode RGB666

Cycle	0	1	……..	2n	2n+1
D8	$R_{0}5$	$G_{0}2$		$R_{n}5$	$G_{n}2$
D7	$R_{0}4$	$G_{0}1$		$R_{n}4$	$G_{n}1$
D6	$R_{0}3$	$G_{0}0$		$R_{n}3$	$G_{n}0$
D5	$R_{0}2$	$B_{0}5$		$R_{n}2$	$B_{n}5$
D4	$R_{0}1$	$B_{0}4$		$R_{n}1$	$B_{n}4$
D3	$R_{0}0$	$B_{0}3$		$R_{n}0$	$B_{n}3$
D2	$G_{0}5$	$B_{0}2$		$G_{n}5$	$B_{n}2$
D1	$G_{0}4$	$B_{0}1$		$G_{n}4$	$B_{n}1$
D0	$G_{0}3$	$B_{0}0$		$G_{n}3$	$B_{n}0$

16bits Mode RGB565 (Both in CPU and RGB Interface)

Table 16bits Mode RGB565

Cycle	0	1	……..	n
D15	$R_{0}4$	$R_{1}4$		$R_{n}4$
D14	$R_{0}3$	$R_{1}3$		$R_{n}3$
D13	$R_{0}2$	$R_{1}2$		$R_{n}2$
D12	$R_{0}1$	$R_{1}1$		$R_{n}1$
D11	$R_{0}0$	$R_{1}0$		$R_{n}0$
D10	$G_{0}5$	$G_{1}5$		$G_{n}5$
D9	$G_{0}4$	$G_{1}4$		$G_{n}4$

D8	G_{03}	G_{13}		G_{n3}
D7	G_{02}	G_{12}		G_{n2}
D6	G_{01}	G_{11}		G_{n1}
D5	G_{00}	G_{10}		G_{n0}
D4	B_{04}	B_{14}		B_{n4}
D3	B_{03}	B_{13}		B_{n3}
D2	B_{02}	B_{12}		B_{n2}
D1	B_{01}	B_{11}		B_{n1}
D0	B_{00}	B_{10}		B_{n0}

16bits Mode RGB332 (CPU Interface Only)

Table 16bits Mode RGB332

Cycle	0	1	……..	n/2
D15	R_{02}	R_{22}		R_{n4}
D14	R_{01}	R_{21}		R_{n3}
D13	R_{00}	R_{20}		R_{n2}
D12	G_{02}	G_{22}		R_{n1}
D11	G_{01}	G_{21}		R_{n0}
D10	G_{00}	G_{20}		G_{n5}
D9	B_{01}	B_{21}		G_{n4}
D8	B_{00}	B_{20}		G_{n3}
D7	R_{12}	R_{32}		G_{n+12}
D6	R_{11}	R_{31}		G_{n+11}
D5	R_{10}	R_{30}		G_{n+10}
D4	G_{12}	G_{32}		B_{n+14}
D3	G_{11}	G_{31}		B_{n+13}
D2	G_{10}	G_{30}		B_{n+12}
D1	B_{11}	B_{31}		B_{n+11}
D0	B_{10}	B_{30}		B_{n+10}

16bits Mode RGB444 (CPU Interface Only)

Table 16bits Mode RGB444 (XRGB)

Cycle	0	1	……..	n
D15	X	X	X	X
D14	X	X	X	X
D13	X	X	X	X
D12	X	X	X	X
D11	R_{03}	R_{13}		R_{n3}
D10	R_{02}	R_{12}		R_{n2}
D9	R_{01}	R_{11}		R_{n1}
D8	R_{00}	R_{10}		R_{n0}
D7	G_{03}	G_{13}		G_{n3}
D6	G_{02}	G_{12}		G_{n2}
D5	G_{01}	G_{11}		G_{n1}
D4	G_{00}	G_{10}		G_{n0}
D3	B_{03}	B_{13}		B_{n3}
D2	B_{02}	B_{12}		B_{n2}
D1	B_{01}	B_{11}		B_{n1}
D0	B_{00}	B_{10}		B_{n0}

Table 16bits Mode RGB444 (RGBX)

Cycle	0	1	……..	n
D15	R_{03}	R_{13}		R_{n3}
D14	R_{02}	R_{12}		R_{n2}
D13	R_{01}	R_{11}		R_{n1}
D12	R_{00}	R_{10}		R_{n0}
D11	G_{03}	G_{13}		G_{n3}
D10	G_{02}	G_{12}		G_{n2}

D9	G_{01}	G_{11}		G_{n1}
D8	G_{00}	G_{10}		G_{n0}
D7	B_{03}	B_{13}		B_{n3}
D6	B_{02}	B_{12}		B_{n2}
D5	B_{01}	B_{11}		B_{n1}
D4	B_{00}	B_{10}		B_{n0}
D3	X	X	X	X
D2	X	X	X	X
D1	X	X	X	X
D0	X	X	X	X

18bits Mode RGB666 (Both in CPU and RGB Interface)

Table 18bits Mode RGB666

Cycle	0	1	……..	n
D17	R_{05}	R_{15}		R_{n5}
D16	R_{04}	R_{14}		R_{n4}
D15	R_{03}	R_{13}		R_{n3}
D14	R_{02}	R_{12}		R_{n2}
D13	R_{01}	R_{11}		R_{n1}
D12	R_{00}	R_{10}		R_{n0}
D11	G_{05}	G_{15}		G_{n5}
D10	G_{04}	G_{14}		G_{n4}
D9	G_{03}	G_{13}		G_{n3}
D8	G_{02}	G_{12}		G_{n2}
D7	G_{01}	G_{11}		G_{n1}
D6	G_{00}	G_{10}		G_{n0}
D5	B_{05}	B_{15}		B_{n5}
D4	B_{04}	B_{14}		B_{n4}
D3	B_{03}	B_{13}		B_{n3}

D2	B_{02}	B_{12}	B_{n2}
D1	B_{01}	B_{11}	B_{n1}
D0	B_{00}	B_{10}	B_{n0}

9.1.2 Full Display Mode

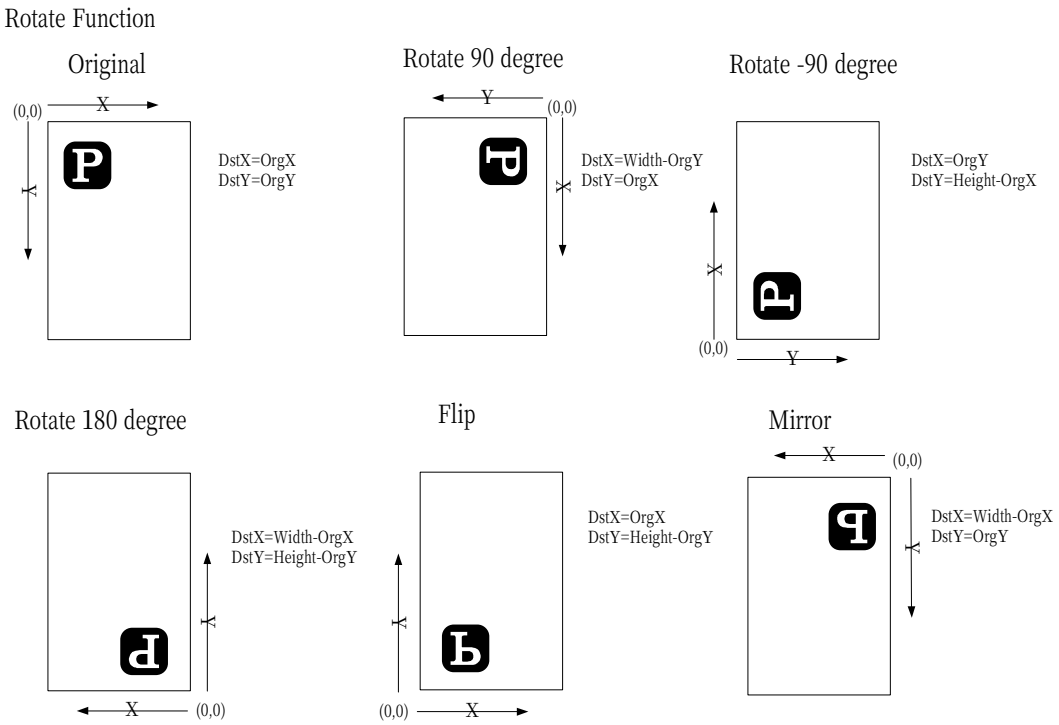
Glamo 3362 embeds display memory, LCD timing control and both CPU and RGB interface. Therefore Glamo 3362 can support both memory embedded LCM module and non-memory LCD module. The maximum display size is 640x480. The active period, front-porch, back-porch, retrace period are all programmable.

Refresh Rate

Only the video application or playing game needs to use full refresh rate for smooth motion display quality. But most of time, the LCD display is in static. While this happens, the display refresh rate can be reduced. With this, I/O power in the LCD interface and power consumption of the LCD module can be saved greatly. Glamo 3362 display controller refresh rate can be reduced to 10 Hz, even lower, by reducing the clock frequency of LCD controller module. Be noticed that the refresh rates supported by the LCD should be confirmed by the LCD vendor.

Rotation

Glamo 3362 LCD controller supports the following kinds of rotations.



Dithering

When viewing image of higher color depth on lower color depth LCD display, we tend to ignore low bits. This causes block effect on otherwise smooth surface of the image. Glamo 3362 provides special dithering architecture to eliminate this effect.

OSD

Glamo 3362 provides 2bits up to full screen size On Screen Display function. 2bits plain can define four operations:

00: Background color (defined in LCD Register 0x1164h)

10: Foreground color (defined in LCD Register 0x1160h)

01: Source color (or third color defined in LCD Register 0x1168h, if 0x1100h bit 6 set to 1)

11: Inverse source color

With this function, we can apply to pop-up menu on any plain, such as graphic or video.

Flipping

When motion video clip or graphic animation is shown on LCD, user can see the discomfort tearing image if there is only one frame displayed on the LCD. To solve this, Glamo 3362 implemented two display buffers, one is for LCD display and the other is for video or graphic engine drawing for the following frame. With that, we named the feature “flipping function”. When the following frame is well drawn, engine will issue a flip command to LCD controller. After receiving the flip command, LCD controller will not flip to the new frame until the vertical retracing starts. With this scheme, LCD display will always show the complete frame.

Gamma Correction

The character of each type of LCD panel may be different and with different gamma curve. Glamo 3362 supports fully programmable Gamma table to fine tune the display quality. The related registers are defined at LCD Register 0x1200h~0x125Fh.

9.1.3 Partial Display Mode

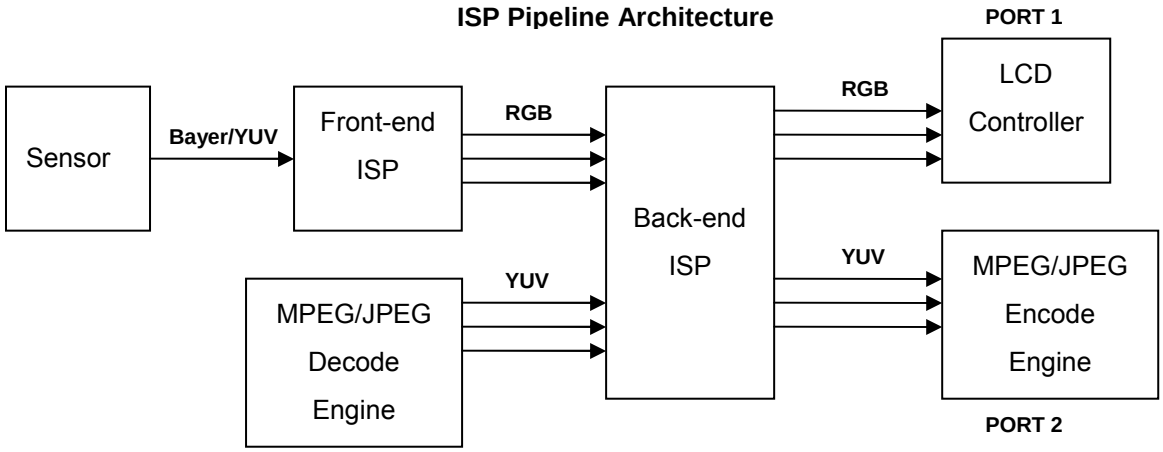
In full display mode, for display refresh, LCD controller in Glamo 3362 needs to read the frame buffer data from external memory periodically. The power consumption includes the memory operation power, the memory interface IO power, LCD controller power and the LCD IO power. Glamo 3362 supports one 128x64 pixels (2bits per pixel) internal SRAM for partial display. It will save the power consumption of memory operation and IO. The internal SRAM can be defined as any kind of dimension smaller than 128x64. For example, user can define the partial display screen as 256x32, 128x64, 64x128, and 32x256. The color of partial display uses the same definition as that of OSD function.

9.1.4 Bypass Mode

Glamo 3362 supports the LCD bypass mode. When this mode is enabled, baseband CPU will directly control the LCD panel and bypass Glamo 3362's LCD controller. Because it is hardware link from Host IO to LCD IO, Glamo 3362 can turn off all the clocks and PLL. At this moment, only Host IO and LCD IO consume power.

9.2 Image Signal Processor

The Image Signal Processor (ISP) is a hardware pipeline engine in Glamo 3362. It receives the sensor captured data or JPEG/MPEG decoding engine, doing the image processing and scaling and then output to the LCD monitor or JPEG/MPEG encoding engine. The input data format can be Bayer or YUV, and output format can be RGB for LCD and YUV for JPEG/MPEG engine. All the functions are controlled by the Capture Registers and ISP registers. Besides, there is s micro processor in Glamo 3362 to control the sensor programming and 3A (auto exposure, auto white balance and auto focus). That's to say, with Glamo 3362, baseband will just need to do handful things on DSC functions. The following diagram shows the pipeline architecture of ISP.



9.2.1 Sensor Programming

Each sensor needs to be configured before it can work properly, and most of sensors provide various modes for preview and snapshot. Additionally, based on various environment conditions, we need real-time change the sensor parameters, for example, the gain value for auto white balance control and exposure time for auto exposure control. Sensor contains one serial bus to program the internal registers. Glamo 3362 provides programmable micro processor scheme to handle these real-time control task. With this scheme, baseband CPU only needs to send commands or get the result without any extra loading, so system will be very easy to implement the DSC function into their mobile solution.

9.2.2 Front-End Image Processing

Front-End Image Processing module receives the data from Sensor and output to the back-end Image Processing module. The function of front-end ISP includes bad pixel removal, shading correction, black pixel

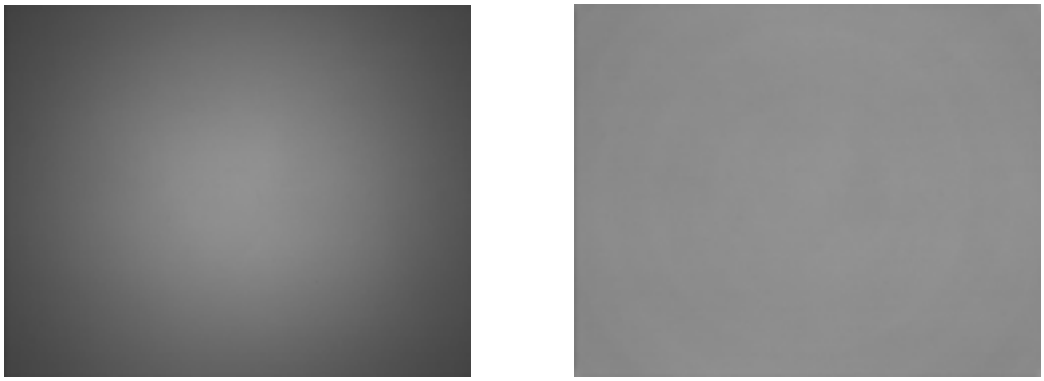
compensation, gain compensation, gamma Correction and Image Decimation.

Bad Pixel Removal

Every sensor may contain bad pixels. The bad pixels may be dark points or bright points, and it will let user feel discomfort because of the abruptly color noise. Glamo 3362 supports the bad pixel removal by recording the bad pixel location in advance and remove the bad pixels at run time. Glamo 3362 will use adjacent information to regenerate the defect pixel.

Lens Shading Correction

In mobile phone, because of the camera module's mechanism limitation, the lens size will be limited. Therefore the higher resolution the sensor is, the worse the lens distortion will be. Glamo 3362 supports hardware real-time lens shading compensation, and shading shape and shading location can be programmed. The related registers are defined in Video Capture registers 0x46Eh~0x497h.



Example of Shading Correction (a) before shading correction (b) after shading correction

Black Level Compensation

Each sensor may define an optically masked region for the black level compensation. It is because the sensor in the masked region may still contain a small value larger than 0. Therefore, the image acquired by the sensor needs to be compensated (subtracted) by the black level value first.

Gain Compensation

The spectrum sensitivities of Gr, R, Gb, B channels in a Bayer pattern image sensor vary depending on the ambient light sources. Hence, Glamo 3362 supports the gain compensation for each color channel to compensate the sensitivity differences.

Gamma Correction

Glamo 3362 supports a fully programmable gamma correction which allows users to define specific gamma curves. The gamma curves of Gr, R, Gb, and B channels can be defined independently.

Example of Gamma correction – (a) before gamma (b) after gamma correction

Image Decimation

In preview or video recording mode, the LCD or MPEG record size is much smaller than the sensor size. Glamo 3362 supports pre-step scaling down the image size. The function is useful for power saving, because it can reduce the data throughput of the ISP pipeline. If use simply drop line decimation algorithm, it may cause the jaggy edge and high frequency image. It will let user feels discomfort and raises the MPEG bits rate and also impact the video quality. Glamo 3362 support high quality 2-taps horizontal and 2-taps vertical decimation. It can improve the video quality display on LCD display and the MPEG encoding quality.

Image source

Example of Decimation - (a) Direct Drop (b) High quality decimation

9.2.3 Back-End Image Processing

Back-End Image Processing module receives data from Front-End Image Processing module (Encoding mode) or data from JPEG/MPEG decode engine (Playback mode) and output to the LCD controller and JPEG/MPEG encode engine. The functions of back-end Image Processing include Color Interpolation, Color Correction, Image Enhancement, Color space Transformation, 4-by-4 taps Continuous Scaling, Image Effects, Rotation and etc.. Back-End Image Processing module also collects the image statistic information for Auto Exposure, Auto White Balance and Auto Focus judgment.

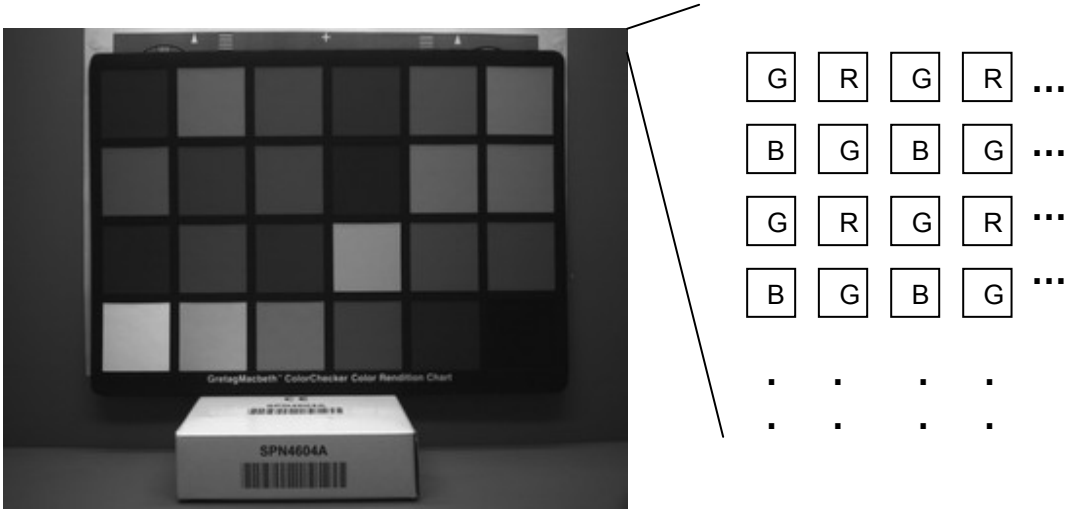
Auto Exposure/Auto White Balance/Auto Focus

Glamo 3362 provides the related statistic information to achieve the “3A” control. In order to reduce the baseband CPU loading, Glamo 3362 also builds in a micro processor to handle these tasks. So Glamo 3362 can achieve the “3A” control without baseband CPU involved. Auto Exposure is to dynamically changes the senor exposure time. Glamo 3362 ISP module provides the luminance statistic information every frame. Micro processor uses the information to change the exposure time of the sensor by programming the sensor registers. Auto White Balance is to dynamically change the gain value of the four-channel of raw data (Gr/R/Gb/B). Glamo 3362 provides the white area detection and white value statistic information every frame. Micro processor uses the information to change the gain value of the Gr, R, Gb, B channels on Glamo 3362 or sensor. Auto Focus is to dynamically change the focus-motor to focus on the target object. Glamo 3362 provides the Modulation Transfer Function (MTF) information every frame. Micro processor watches the changing MTF information of series frames and modifies the focus-motor value by GPIO pins.

Example of Auto white balance (a) before AWB (b) after AWB

Color Interpolation

For Bayer data format input, Glamo 3362 provides color interpolation architecture to generate from Gr, R, Gb, B channels per pixel per byte to RGB channel per pixel 3 bytes.



Example of Bayer data input

Example of after color interpolation

Color Correction

Various sensor types may contain various color sensitivity curves. It needs processes color correction to get the real color. Glamo 3362 provides fully programmable color correction matrix to fit various color correction matrix requests from various vendors. The color correction formula is as follows:

$$\begin{bmatrix} R_{DST} \\ G_{DST} \\ B_{DST} \end{bmatrix} = \begin{bmatrix} CC_{11} & CC_{12} & CC_{13} \\ CC_{21} & CC_{22} & CC_{23} \\ CC_{31} & CC_{32} & CC_{33} \end{bmatrix} \cdot \begin{bmatrix} R_{SRC} \\ G_{SRC} \\ B_{SRC} \end{bmatrix} + \begin{bmatrix} R_{Delta} \\ G_{Delta} \\ B_{Delta} \end{bmatrix}$$

Example of Color Correction – (a) before color correction (b) after color correction

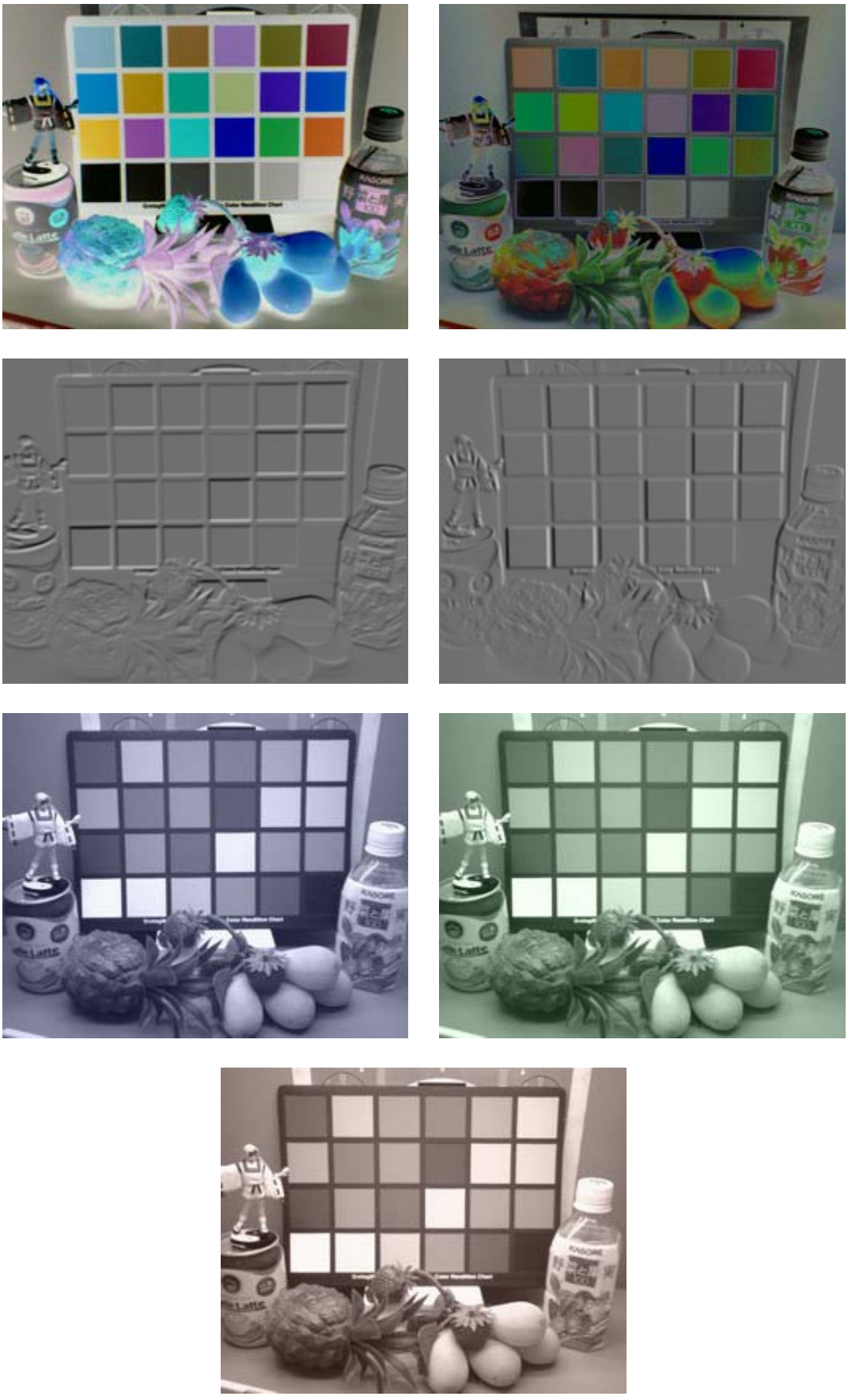
Hue/Saturation/Brightness/Contrast Image Enhancement

By using different color correction matrix, Glamo 3362 can support Hue/Saturation/Brightness/Contrast image enhancement and Black/White, solarization and a variety of color filter effects. All the effects can be applied to preview mode as well as JPEG image and MPEG video.

Exampe of Image Enhancement – (a) Origin (b) Brightness (c) Contrast (d) Hue (e) Saturation

Image Effects

Glamo 3362 provides hardware night shot compensation, negative picture, solarization, emboss and color filter effects. All the effects can be applied to preview mode as well as JPEG image and MPEG video.



Example of Image Effects – (a) Origin (b) Negative (c) Solarization (d) Emboss 1 (e) Emboss 2 (f) Color Filter with Blue (g) Color Filter with Green (h) Color Filter with Red

2D Edge Enhancement

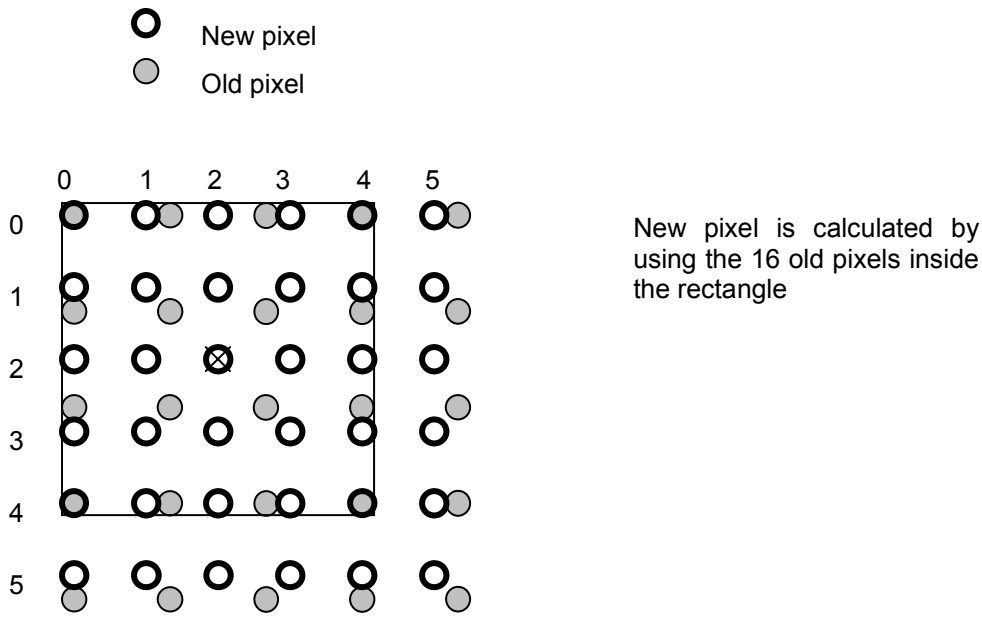
Glamo 3362 supports hardware 2D edge enhancement and the enhance strength can be programmed.

Example of 2D edge enhancement (a) without edge enhancement (b) with edge enhancement

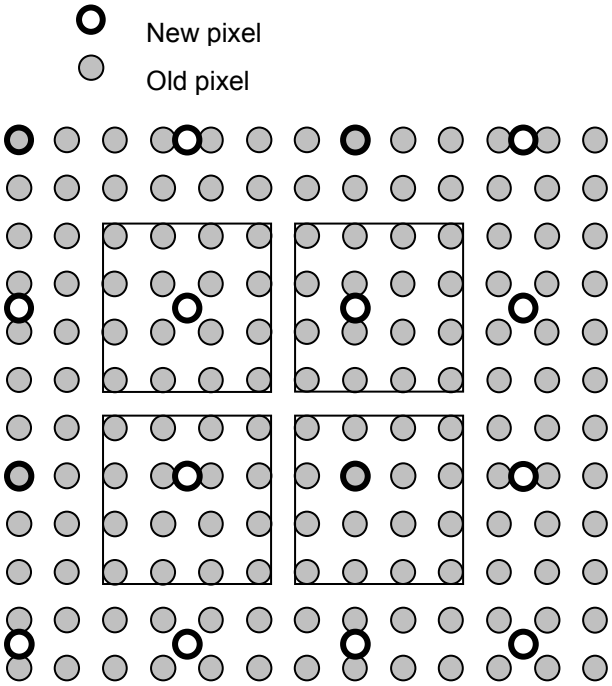
Continuous Image Scaling

Glamo 3362 supports 4-tap horizontal scaler and 4-tap vertical scaler to improve the image scaling quality. The image can be scaled up to 16X without discomfort block effect and can be scaled down to 16X without discomfort jaggy effect. Glamo 3362 also supports continuous image scaling. That is to say, customer can zoom in or zoom out to set the scene he would like to snap smoothly. The following case shows the 4-tap scaling methodology. All the weighted parameters are user programmable.

Example 1: 5/4 Scaling Up:



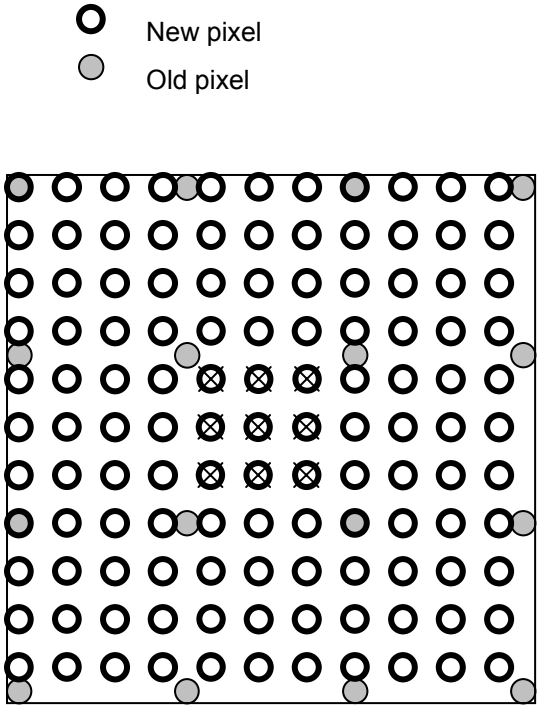
Example 2: 7/2 Scaling Down:



New pixel is calculated by using the 16 old pixels inside the rectangle

---

Example 3: 7/2 Scaling Up:



Marked new pixel are calculated by using the 16 old pixels inside the rectangle

---

Color Space Conversion

In video encoding mode or snapshot mode, ISP module provides RGB to YUV color space conversion in the data path. In video clip playback mode or photo browsing mode, ISP module provides YUV to RGB color space conversion. These conversions are 3x3 matrix operation. The parameter of the matrix is fully

programmable.

Rotation

Glamo 3362 supports two kinds of options for rotation. For display, that is, browsing video clips or images on the LCD monitor, Glamo 3362 supports +90, +180, -90, mirror and flip rotation options. For MPEG/JPEG file, Glamo 3362 supports +180, mirror, flip rotation options. The related register is defined in ISP register 0x0502h.

Frame Function

User may want to take pictures by using beautiful scene as his background or add flower frame around his picture. We call this application as frame function. Glamo 3362 supports frame function in snapshot. The background picture or frame image can be defined by user. Glamo 3362 uses overlay with color key technology to merge the picture that user took with pre-defined frame image. In the frame function mode, Glamo 3362 still can support continuous image scaling. That is, user can do continuous zoom in to take a picture.

Clipping

Glamo 3362 supports rectangle overlay to display the video or image on LCD monitor. User can define the rectangle size and position on the LCD by setting the clipping window. User also can define clipping inside or outside. With this function, video can be updated within this defined window without redrawing the original graphic outside the defined window.

9.2.4 ISP Operation Mode

According to the applications, ISP module supports the following operation modes:

Preview mode

In this mode, MPEG codec, JPEG codec are idle and the related clocks are off. The host controller is idle and related clock is off because micro processor take care all the auto exposure, auto white balance and auto focus jobs. The 2D/3D engines are idle and related clocks are off because of rectangle overlay, only video updated. Memory controller is enabled. LCD Controller is enabled. Micro processor is enabled. The initial sequence is as follows:

Turn on the related clocks

Program Sensor to preview mode.

Program the ISP registers for data input from sensor and output to LCD (port 1).

Program the video capture registers.

Enable micro processor.

Fire ISP module by setting 0x0502 bit0 to 1

Fire Video Capture module by setting 0x04c0 bit0 to 1

Snapshot mode

In this mode, JPEG encode will be enabled and the other settings will be similar to preview mode. The initial sequence is as follows:

Turn on the related clocks

Program Sensor to snapshot mode.

Program the JPEG encode registers.

Program the ISP registers for data input from sensor and output to LCD (port 1) and JPEG encoder (port 2).

Program the video capture registers.

Fire JPEG encoder module

Fire ISP module by setting 0x0502 bit0 to 1

Fire Video Capture module by setting 0x04c0 bit0 to 1

Video Recoding mode

In this mode, MPEG encode will be enable and Host Controller is enabled to read back the encoded bitstream. The other setting is similar to preview mode. The initial sequence is as follows:

Turn on the related clocks

Program Sensor to preview mode.

Program the MPEG encode registers.

Program the ISP registers for data input from sensor and output to LCD (port 1) and MPEG encoder (port 2).

Program the video capture registers.

Fire MPEG encoder module

Fire ISP module by setting 0x0502 bit0 to 1

Fire Video Capture module by setting 0x04c0 bit0 to 1

Photo browsing mode

In this mode, the JPEG Decoder, Memory Controller, LCD Controller and Host Controller are enabled.

Turn on the related clocks

Program the JPEG decode registers.

Program the ISP registers for data input from JPEG decoder and output to LCD (port 1).

Fire JPEG Decoder module

Fire ISP module by setting 0x0500 bit0 to 1

Video Playback mode

In this mode, the MPEG Decoder, Memory Controller, LCD Controller and Host Controller are enabled.

Turn on the related clocks

Program the MPEG decode registers.

Program the ISP registers for data input from MPEG decoder and output to LCD (port 1).

Fire MPEG Decoder module

Fire ISP module by setting 0x0500 bit0 to 1

Video Conference mode

Turn on the related clocks

Program Sensor to preview mode.

Enable Micro Processor.

Program the MPEG decode registers.

Program the MPEG encode registers.

Program the video capture registers.

Loop

Program the ISP registers for data input from sensor and output to LCD (port 1) and MPEG encoder (port 2).

Fire MPEG Encoder module

Fire ISP module by setting 0x0502 bit0 to 1

Fire Video Capture module by setting 0x04c0 bit1 to 1

Program the ISP registers for data input from MPEG decoder and output to LCD (port 1).

Fire MPEG Decoder module

Fire ISP module by setting 0x0500 bit0 to 1

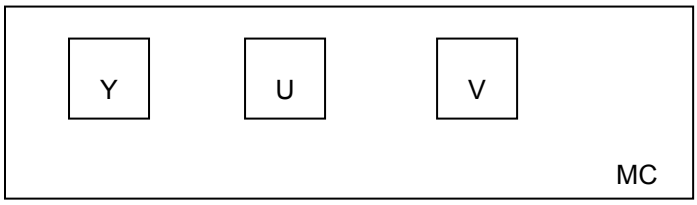
Go to Loop

9.3 JPEG Engine

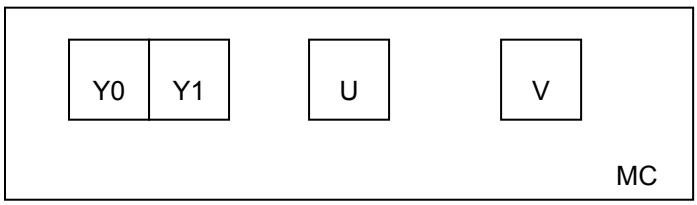
9.3.1 Support Formats

The Glamo 3362 JPEG codec is based on the JPEG baseline standard and the arithmetic accuracy satisfies the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The maximum image size is 5M pixels (2592x1944). The image that can be encoded/decoded must be the alignment of MCU base. The parameters of luminance and chrominance quantization table are fully programmable. The Huffman tables use the default tables that are suggested by specification. The decoding process supports YUV 4:4:4, 4:2:2, 4:1:1 and 4:2:0 with interleaved format, but the encoding process only supports YUV 4:2:2 interleaved format. The progressive mode is not supported, but sequential mode. The following diagram shows the definition of each formation.

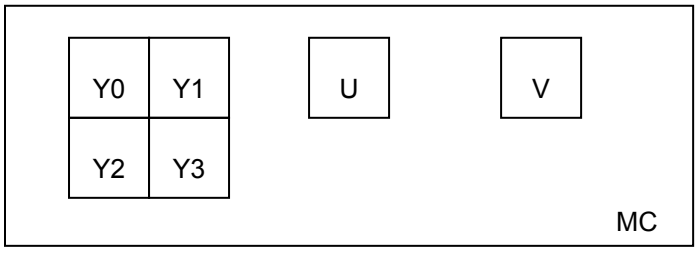
YUV 4:4:4 Format



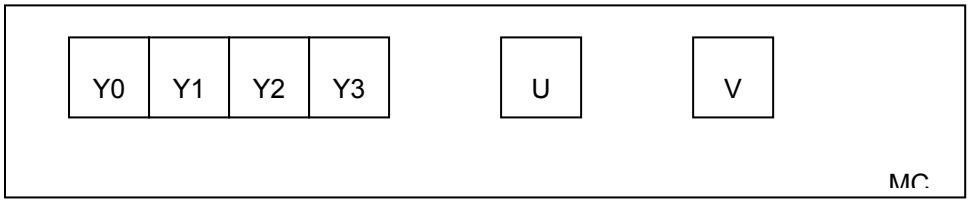
YUV 4:2:2 Format



YUV 4:2:0 Format



YUV 4:1:1 Format



9.3.2 Encode/Decode Time

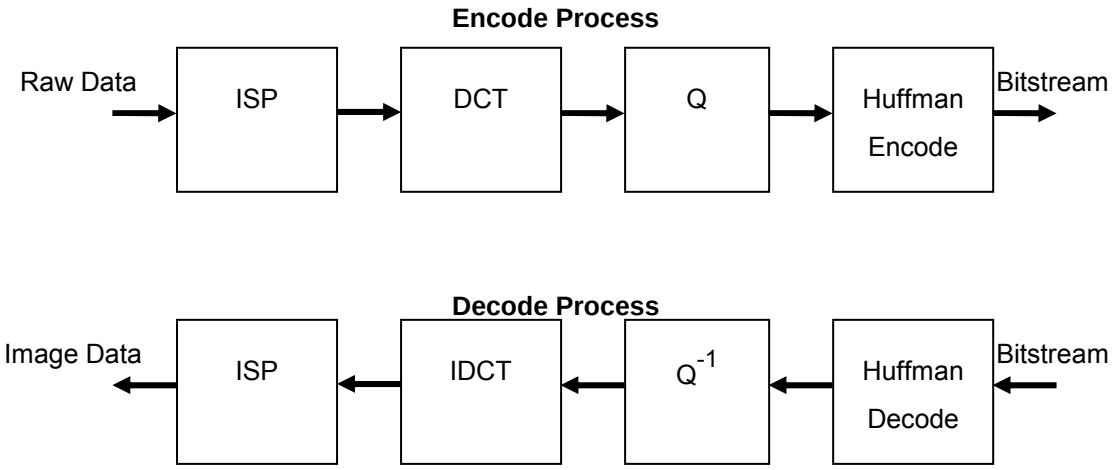
The encoding and decoding time of an image is about 70 clock cycle every block,. For example, when 1.3M-pixel(1280x1028) 4:2:2 format is processed under 33MHz frequency. The total numbers of block are 20480(Y) + 10240(U) + 10240(V) = 40960 blocks. The encode/decode time is about 0.08 second.

9.3.3 JPEG Engine Pipe Line Architecture

The following diagram shows the JPEG engine pipe line.

In encoding process, JPEG engine receives the image raw data from frame buffer and output the bit-stream to bit stream buffer. The handshaking with the ISP module is slice base, and can be triggered by hardware automatically. JPEG encoding engine also support software trigger mode. System puts the raw data from host interface to frame buffer and then driver will command JPEG engine to be triggered. JPEG encoding engine passes the raw data to DCT engine block, quantization block and then Huffman entropy encode block. All the flow is pipelined and controlled by hardware. The output bit-stream needs to add file header and marker to become JFIF or EXIF file format. The packaging job should be done by CPU.

In decoding process, JPEG engine receives the bit-stream from bit-stream buffer and output the constructed image to ISP module for further operations (scaling and rotation). The handshaking with the ISP module is slice-based and is triggered by software command. JPEG decode engine passes the bit-stream to Huffman entropy decode block, Dequantiaztion block and Inverse-DCT block. All the flow is pipelined and controlled by hardware.



9.3.4 Thumbnail Image

There are two ways to generate the thumbnail image. One is to use Port 1 of ISP module to output the RGB raw image as thumbnail image. With this method, the thumbnail image will be RGB 888 raw data format. The image size can be programmed by changing the scaling factors of Port 1 of ISP module. The other way is to use two passes to generate another small size image as thumbnail image. After the first pass is gone, we can change the scaling factors of ISP module and fire for JPEG encode again by software trigger command. With this method, the thumbnail image will be JPEG data format.

9.3.5 Engine Status Report

Glamo 3362 provides two schemes to inform baseband CPU the JPEG engine status. One is register flag. CPU is poling the JPEG Register 0xAB2 bit 0 or bit 1 to check the encoding or decoding task finished or not. The other is use interrupt to inform baseband CPU the JPEG engine status.

9.3.6 JPEG Encoding Process

The JPEG encoding process is as follows:

1. Initial the sensor and ISP module to snapshot mode.
2. Initial the JPEG encoding related register.
3. Fire ISP for snapshot
4. Interrupt signal to inform CPU for JPEG encoding ready
5. Check the JPEG engine status
6. Read back the encoded bitstream
7. Append the header and marker as JFIF or EXIF file format.

9.3.7 JPEG Decoding Process

The JPEG encoding process is as follows:

1. Initial ISP module to image viewing mode.
2. Initial the JPEG decoding related register.
3. Send bitstream to frame buffer for decoding
4. Fire ISP for decode mode
5. Interrupt signal to inform CPU for JPEG decoding ready
6. Check the JPEG engine status
7. Show the decoded image on the LCD display

9.4 MPEG Engine

9.4.1 Support Formats

The Glamo 3362 MPEG codec is based on the ISO/IEC 14496-2 (MPEG-4) simple profile standard. The maximum size can up to CIF (352x288) 30 fps or VGA (640x480) 12 fps. Glamo 3362 also supports the VOP

with short header (H.263). Glamo 3362 hardware decoder and encoder are fully pipelined architecture. It supports to VOP layer, the baseband only need to packaging the file header and AV synchronization for MPEG encoding and parsing the header for MPEG decoding.

9.4.2 MPEG Codec Architecture

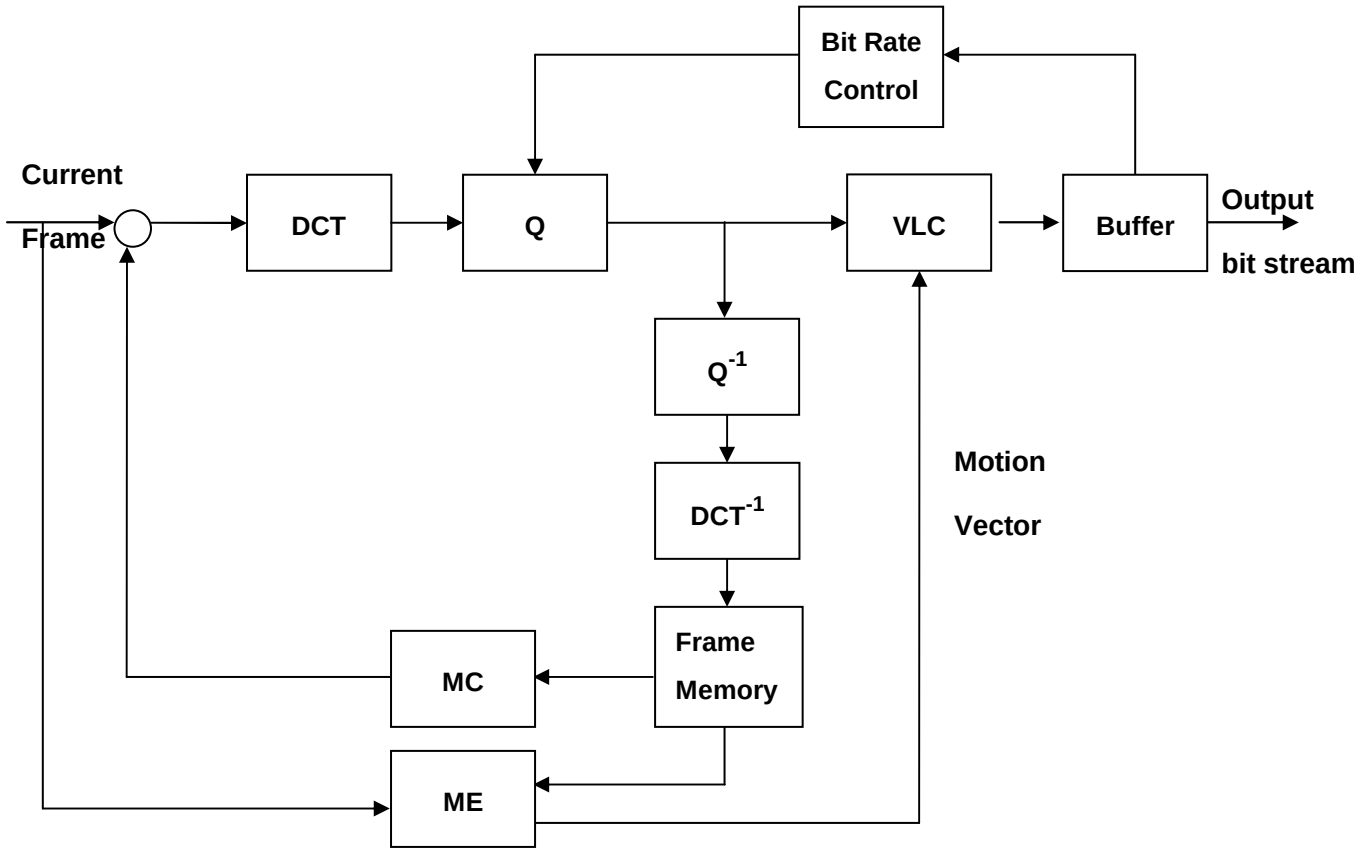
The following diagram shows the hardware architecture of MPEG encoder and MPEG decoder of Glamo 3362. They are all fully pipelined design and hardware flow control.

In MPEG decoder, the bit-stream sends to the VLD (Variable Length Decoding) block, Inverses Quantization block, inverses DCT transform and adds with data of motion compensation to generate the decoded MPEG video and then sends to the ISP and LCD module to display.

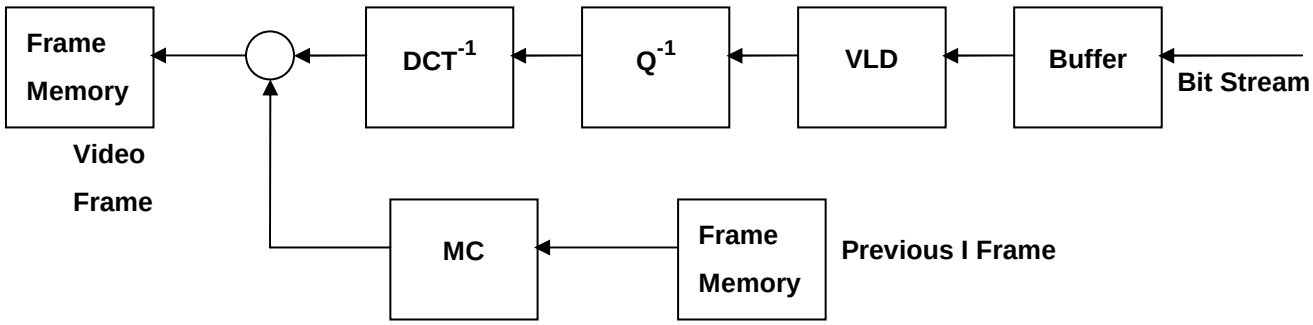
In MPEG encoder, there is one reconstructed path to generate the reconstructed video frame, and one motion estimation block to estimate the motion vector. The video frame subtracts the reconstructed video frame and sends to DCT block, Quantization block, Variable Length Coding and output the encoded bit-stream the bit-stream buffer.

The motion estimation of Glamo 3362 supports full search algorithm with ±16 search range in both X and Y direction. The resolution of motion vector is half-pixel. If the encoder is configured to encode MPEG-4 bitstream, the 4-MV (four motion vectors per macroblock) and unrestricted MV (motion vectors are allowed to point outside picture boundary) functions are also fully supported.

MPEG Encode Architecture



MPEG Decoder Architecture



Rate Control

Base on different applications, the rate control function of Glamo 3362 supports both CBR (constant bit rate) and VBR (variable bit rate) mode. For network transmission with constant bandwidth, the CBR mode can fulfill the allocated bandwidth with maximum quality. When recording video into local storage like flash card or hard disk, the VBR mode can adjust the bit-consumption rate according to the complexity variation of the incoming video, achieve a more uniform visual quality. The rate control function also includes a adaptive quantization scheme to support the HVS (human visual system). The quantization level of each macroblock is varied according to its visual complexity. With this scheme, the encoded video quality can be improved comparing to the video without rate control with same bit rate.

Handshaking with ISP

In the MPEG encoding mode, MPEG encoder receives the video data from ISP module with triple buffer scheme. The handshaking control is done by hardware, baseband CPU do not need to take the flow control efforts to reduce the CPU loading. Baseband CPU only needs to read back the encoded bit-stream and package the header of MPEG file format. In the MPEG decoding mode, MPEG decoder provided the decoded video data to ISP module every frame. And then software flips the video to LCD display according to the time stamp.

9.4.3 MPEG Encoding Process

The MPEG encoding process is as follows:

1. Initial the sensor and ISP module to video recording mode.
2. Initial the MPEG encoding related register.
3. Fire ISP for video recording.
4. Read back the encoded bitstream
5. Append the header and synchronous with audio bit-stream to became 3GPP file format.

9.4.4 MPEG Decoding Process

The MPEG decoding process is as follows:

8. Initial ISP module to video playback mode.
9. Initial the MPEG decoding related register.
10. De-multiplex the audio and video bit-streams
11. Send video bitstream to frame buffer for decoding
12. Fire ISP for MPEG decode mode
13. Show the decoded video on the LCD display

9.5 Micro Processor

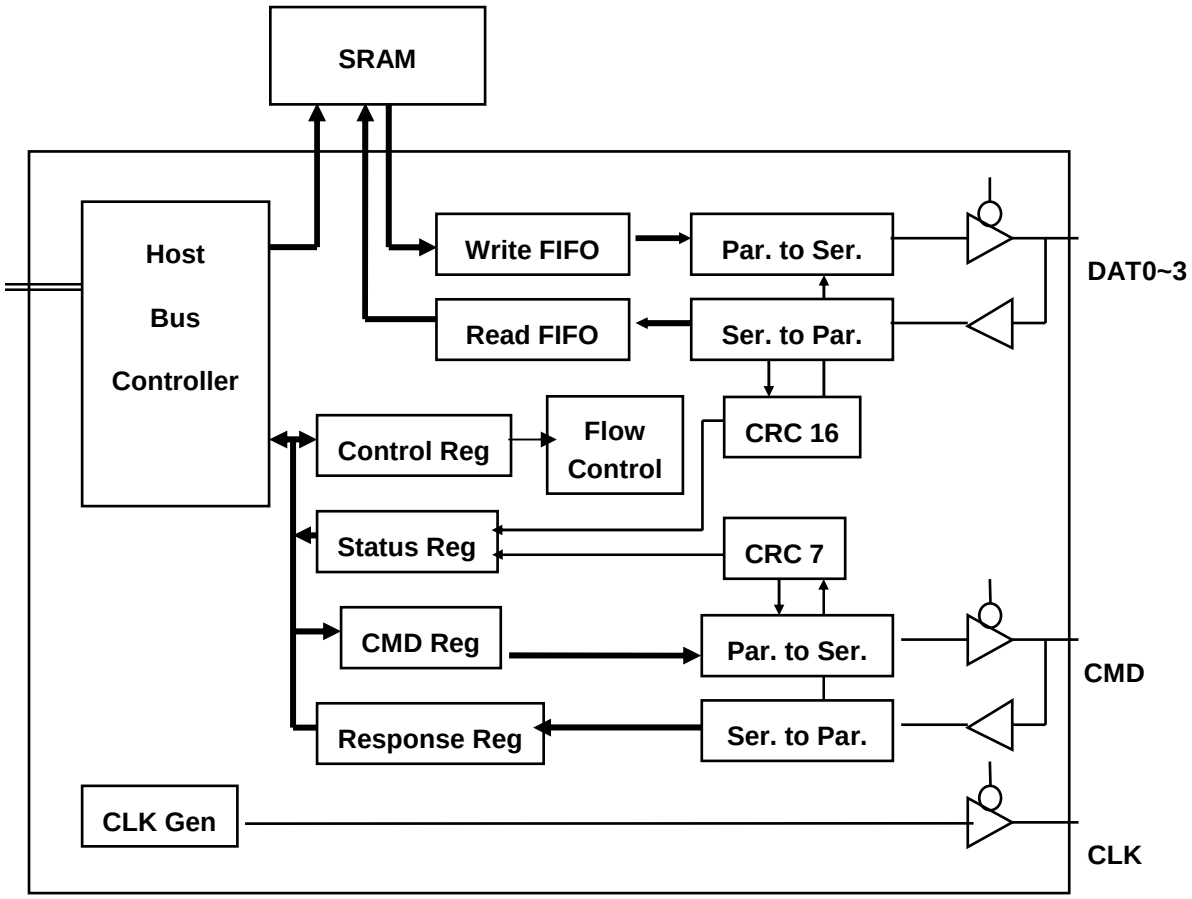
Glamo 3362 embeds two RISC processors for operational control. One is used for ISP function flow control and the other is used for rate control of MPEG encoding. Two processors can be worked independently. The purpose of the micro processors is to release the baseband CPU loading. When system process the camera function or video recording function, the baseband CPU is almost idle. Micro processor will take cares all the flow control and simple calculation efforts.

9.6 MMC/SD Controller

The Glamo 3362 support MMC/SD memory card and fully compliant with MMC 3.3 specification and compliant with low-voltage support of MMCA v4.0 and SD specification. The supported features as follows:

Support 4-bit DAT
Support variable clock rates : up to 50MHz supported
Support variable transfer block size
Support Single block READ/WRITE
Support open-ended Multiple block READ
Support Multiple block READ with pre-defined block count
Support Multiple block WRITE with pre-defined block count
Support Stream READ

9.6.1 Block Diagram



9.6.2 MMC/SD Read Process

1. Initialize the MMC/SD card
2. Prepare the read control information
3. Issue read CMD to CMD register
4. Wait response status from MMC/SD card.
5. Ready to receive data and save the received data back to SRAM
6. Check the CRC to make sure the data valid
7. Update the status register for CPU read back
8. CPU read back the data
9. Loop back to 3

9.6.3 MMC/SD Write Process

1. Initialize the MMC/SD card
2. Prepare the write control Information and write data into SRAM
3. Issue write CMD to CMD register
4. Wait response status
5. Send write data from SRAM to MMC DAT port block by block
6. Check the CRC/Busy status on DAT Line for valid write and wait programming complete
7. Loop Back to 5
8. Update the status register for write complete

9.7 2D Graphics Engine

Mobile Multimedia Processor (MMP) supports a powerful 2D graphics engine to enhance the performance. It only supports high color (16bpp) mode, and following functions:

1. BitBlt with ROP3
2. Color expansion
3. Transparent BitBlt with source and destination key
4. Line Drawing
5. Stretch
6. Alpha Blending, it supports constant alpha, ARGB8888, ARGB1555, and ARGB4444 source bitmap for per-pixel alpha value.

For each function, it can rotate by 90^{o}, -90^{o}, 180^{o}, flip and mirror the coordinate. The fill rate depends on the clock rate of 2D engine. For example, if the clock rate is 33MHz, the fill rate is 33M pixels per second.

9.7.1 ROP3

This section lists the ternary raster-operation codes used by the **BitBlt**, **Color Expansion**, and **Line Draw** functions. The line drawing function just supports ROP2 operation. It's same as ROP3 Boolean truth table but without Source components. The Pattern components comes from line style, the Destination components comes from destination bitmap. Ternary raster-operation codes define how hardware combines the bits in a source bitmap with the bits in the destination bitmap.

Each raster-operation code represents a Boolean operation in which the values of the pixels in the source, the selected brush, and the destination are combined. Following are the three operands used in these operations:

Operand	**Meaning**
D	Destination bitmap
P	Selected brush (also called pattern)
S	Source bitmap

Boolean operators used in these operations follow:

Operator	**Meaning**
a	Bitwise AND
n	Bitwise NOT (inverse)
o	Bitwise OR
x	Bitwise exclusive OR (XOR)

All Boolean operations are presented in reverse Polish notation. For example, the following operation replaces the values of the pixels in the destination bitmap with a combination of the pixel values of the source and brush:

PSo

The following operation combines the values of the pixels in the source and brush with the pixel values of the destination bitmap (there are alternative spellings of the same function, so although a particular spelling may not be in the list, an equivalent form would be):

DPSoo

For example, the operation indexes for the PSo and DPSoo operations are shown in the following list:

P	**S**	**D**	**PSo**	**DPSoo**
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1
Operation index:			FCh	FEh

In this case, PSo has the operation index FC (read from the bottom up); DPSoo has the operation index FE. These values define the location of the corresponding raster-operation codes, as shown in Table A.1, "Raster-Operation Codes." The PSo operation is in line 252 (FCh) of the table; DPSoo is in line 254 (FEh).

Table A.1 Raster-Operation Codes

Boolean function (hexadecimal)	**Boolean function in reverse Polish**	**Common name**
00	0	**BLACKNESS**
01	DPSoon	
02	DPSona	
03	PSon	
04	SDPona	
05	DPon	
06	PDSxnon	
07	PDSaon	

08	SDPnaa	
09	PDSxon	
0A	DPna	
0B	PSDnaon	
0C	SPna	
0D	PDSnaon	
0E	PDSonon	
0F	Pn	
10	PDSona	
11	DSon	**NOTSRCERASE**
12	SDPxnon	
13	SDPaon	
14	DPSxnon	
15	DPSaon	
16	PSDPSanaxx	
17	SSPxDSxaxn	
18	SPxPDxa	
19	SDPSanaxn	
1A	PDSPaox	
1B	SDPSxaxn	
1C	PSDPaox	
1D	DSPDxaxn	
1E	PDSox	
1F	PDSoan	
20	DPSnaa	
21	SDPxon	
22	DSna	
23	SPDnaon	
24	SPxDSxa	

25	PDSPanaxn	
26	SDPSaox	
27	SDPSxnox	
28	DPSxa	
29	PSDPSaoxxn	
2A	DPSana	
2B	SSPxPDxaxn	
2C	SPDSoax	
2D	PSDnox	
2E	PSDPxox	
2F	PSDnoan	
30	PSna	
31	SDPnaon	
32	SDPSoox	
33	Sn	**NOTSRCCOPY**
34	SPDSaox	
35	SPDSxnox	
36	SDPox	
37	SDPoan	
38	PSDPoax	
39	SPDnox	
3A	SPDSxox	
3B	SPDnoan	
3C	PSx	
3D	SPDSonox	
3E	SPDSnaox	
3F	PSan	
40	PSDnaa	
41	DPSxon	

42	SDxPDxa	
43	SPDSanaxn	
44	SDna	**SRCERASE**
45	DPSnaon	
46	DSPDaox	
47	PSDPxaxn	
48	SDPxa	
49	PDSPDaoxxn	
4A	DPSDoax	
4B	PDSnox	
4C	SDPana	
4D	SSPxDSxoxn	
4E	PDSPxox	
4F	PDSnoan	
50	PDna	
51	DSPnaon	
52	DPSDaox	
53	SPDSxaxn	
54	DPSonon	
55	Dn	**DSTINVERT**
56	DPSox	
57	DPSoan	
58	PDSPoax	
59	DPSnox	
5A	DPx	**PATINVERT**
5B	DPSDonox	
5C	DPSDxox	
5D	DPSnoan	
5E	DPSDnaox	

5F	DPan	
60	PDSxa	
61	DSPDSaoxxn	
62	DSPDoax	
63	SDPnox	
64	SDPSoax	
65	DSPnox	
66	DSx	**SRCINVERT**
67	SDPSonox	
68	DSPDSonoxxn	
69	PDSxxn	
6A	DPSax	
6B	PSDPSoaxxn	
6C	SDPax	
6D	PDSPDoaxxn	
6E	SDPSnoax	
6F	PDSxnan	
70	PDSana	
71	SSDxPDxaxn	
72	SDPSxox	
73	SDPnoan	
74	DSPDxox	
75	DSPnoan	
76	SDPSnaox	
77	DSan	
78	PDSax	
79	DSPDSoaxxn	
7A	DPSDnoax	
7B	SDPxnan	

7C	SPDSnoax	
7D	DPSxnan	
7E	SPxDSxo	
7F	DPSaan	
80	DPSaa	
81	SPxDSxon	
82	DPSxna	
83	SPDSnoaxn	
84	SDPxna	
85	PDSPnoaxn	
86	DSPDSoaxx	
87	PDSaxn	
88	DSa	**SRCAND**
89	SDPSnaoxn	
8A	DSPnoa	
8B	DSPDxoxn	
8C	SDPnoa	
8D	SDPSxoxn	
8E	SSDxPDxax	
8F	PDSanan	
90	PDSxna	
91	SDPSnoaxn	
92	DPSDPoaxx	
93	SPDaxn	
94	PSDPSoaxx	
95	DPSaxn	
96	DPSxx	
97	PSDPSonoxx	
98	SDPSonoxn	

99	DSxn	
9A	DPSnax	
9B	SDPSoaxn	
9C	SPDnax	
9D	DSPDoaxn	
9E	DSPDSaoxx	
9F	PDSxan	
A0	DPa	
A1	PDSPnaoxn	
A2	DPSnoa	
A3	DPSDxoxn	
A4	PDSPonoxn	
A5	PDxn	
A6	DSPnax	
A7	PDSPoaxn	
A8	DPSoa	
A9	DPSoxn	
AA	D	
AB	DPSono	
AC	SPDSxax	
AD	DPSDaoxn	
AE	DSPnao	
AF	DPno	
B0	PDSnoa	
B1	PDSPxoxn	
B2	SSPxDSxox	
B3	SDPanan	
B4	PSDnax	
B5	DPSDoaxn	

B6	DPSDPaoxx	
B7	SDPxan	
B8	PSDPxax	
B9	DSPDaoxn	
BA	DPSnao	
BB	DSno	**MERGEPAINT**
BC	SPDSanax	
BD	SDxPDxan	
BE	DPSxo	
BF	DPSano	
C0	PSa	**MERGECOPY**
C1	SPDSnaoxn	
C2	SPDSonoxn	
C3	PSxn	
C4	SPDnoa	
C5	SPDSxoxn	
C6	SDPnax	
C7	PSDPoaxn	
C8	SDPoa	
C9	SPDoxn	
CA	DPSDxax	
CB	SPDSaoxn	
CC	S	**SRCCOPY**
CD	SDPono	
CE	SDPnao	
CF	SPno	
D0	PSDnoa	
D1	PSDPxoxn	
D2	PDSnax	

D3	SPDSoaxn	
D4	SSPxPDxax	
D5	DPSanan	
D6	PSDPSaoxx	
D7	DPSxan	
D8	PDSPxax	
D9	SDPSaoxn	
DA	DPSDanax	
DB	SPxDSxan	
DC	SPDnao	
DD	SDno	
DE	SDPxo	
DF	SDPano	
E0	PDSoa	
E1	PDSoxn	
E2	DSPDxax	
E3	PSDPaoxn	
E4	SDPSxax	
E5	PDSPaoxn	
E6	SDPSanax	
E7	SPxPDxan	
E8	SSPxDSxax	
E9	DSPDSanaxxn	
EA	DPSao	
EB	DPSxno	
EC	SDPao	
ED	SDPxno	
EE	DSo	**SRCPAINT**
EF	SDPnoo	

F0	P	**PATCOPY**
F1	PDSono	
F2	PDSnao	
F3	PSno	
F4	PSDnao	
F5	PDno	
F6	PDSxo	
F7	PDSano	
F8	PDSao	
F9	PDSxno	
FA	DPo	
FB	DPSnoo	**PATPAINT**
FC	PSo	
FD	PSDnoo	
FE	DPSoo	
FF	1	**WHITENESS**

Line: ROP2

01	0	**BLACKNESS**
02	DPon	
03	DPna	
04	Pn	
05	PDna	
06	Dn	
07	DPx	
08	DPan	
09	Dpa	
0A	PDxn	
0B	D	
0C	DPno	

0D	P	
0E	PDno	
0F	DPo	
10	1	**WHITENESS**

9.7.2 BitBlt

Actually, BitBlt with ROP3 can represent all of the Bitblt functions. But most of them are never used. Here list some frequently used bitblt.

Rectangle Fill

Rectangle Fill is to fill the destination with solid color. The color is specified in the foreground color register. The fill size and position are also specified in registers. Rectangle Fill operation is the same as BitBlt with ROP3 and the code 0xF0. This function always used in fast clean the display screen

Pattern Copy

Pattern Copy is to fill the destination with 8x8 pattern. The pattern is specified in the pattern registers. The fill size and position are also specified in registers. The 8x8 pattern will be repeatedly tiled to the pre-defined rectangle. Pattern Copy operation is the same as BitBlt with ROP3 and the code 0xF0.

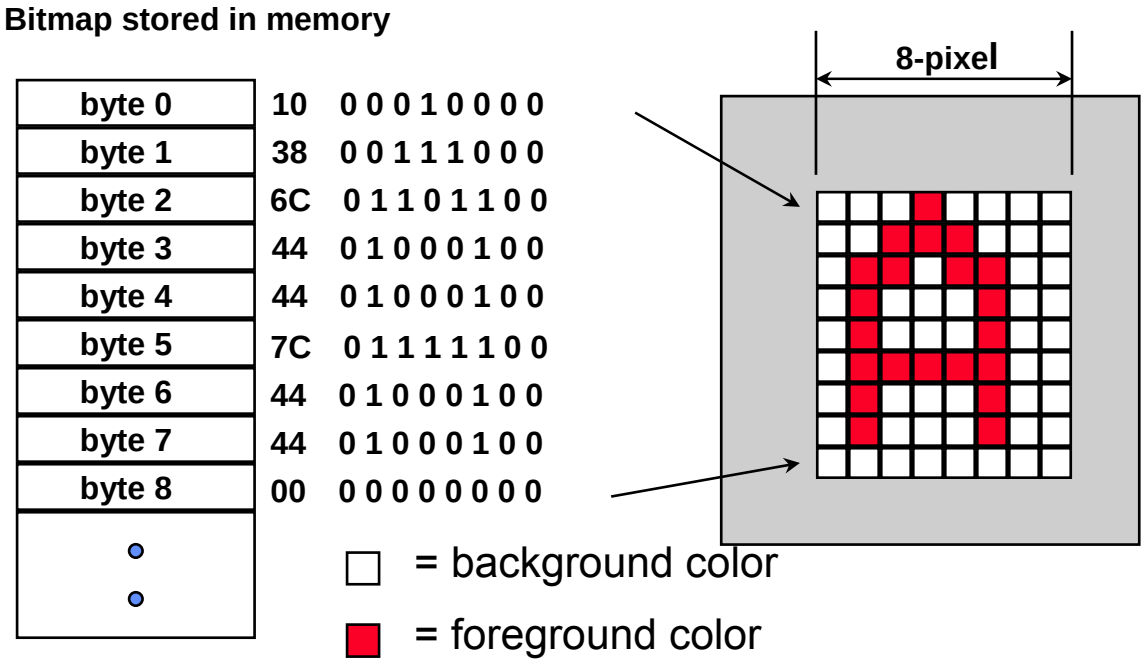
Source Copy

Source Copy is to copy a source rectangle to the destination. Source Copy operation is the same as BitBlt with ROP3 and the code 0xCC.

Because the fill rate is one pixel per cycle, when the clock frequency is 48MHz, Glamo 3362 can provide 48M pixels per second. For example, with VGA LCD display (640x480). Glamo 3362 2D engine can draw full screen more than one hundred times per second. The BitBlt function is always used in smoothly scrolling up and down or graphic animation.

9.7.3 Color Expansion

Color expansion also called font expansion. It used to expand a monochrome bitmap to color bitmap. With this function, user can save the font pattern size to 1 bit per pixel and run-time expanse to two colors font character. User can define his own font pattern with any size and use the color expansion function to expand to the display screen.



9.7.4 Transparent BitBlt

It copies a rectangular region of one bitmap into another, with some transparent pixels depends on the source and destination key. With this function user can perform the multi-layers of graphic overlay. Glamo 3362 provides 16 ROP.

ROP	Source	Destination	Read Destination
0000	Never	Always	No
0001	SRC key and DST key	Otherwise	Yes
0010	Not SRC key and DST key	Otherwise	Yes
0011	DST key	Otherwise	Yes
0100	SRC key and not DST key	Otherwise	Yes
0101	SRC key	Otherwise	No
0110	SRC key xor DST key	Otherwise	Yes
0111	SRC key or DST key	Otherwise	Yes
1000	Not SRC key and not DST key	Otherwise	Yes
1001	SRC key xnor DST key	Otherwise	Yes
1010	Not SRC key	Otherwise	No

1011	Not SRC key or DST key	Otherwise	Yes
1100	Not DST key	Otherwise	Yes
1101	SRC key or not DST key	Otherwise	Yes
1110	Not SRC key or not DST key	Otherwise	Yes
1111	Always	Never	No

The function is always used to merge one character's image into the background image for game application or animation.

9.7.5 Line Drawing

Glamo 3362 uses Bresenham's algorithm to draw a line. The drawing line could be either a solid line or a dashed line. The dashed line pattern can be defined in registers. The line color is define in foreground color register

9.7.6 Stretch

The stretch function is to scales up or down a rectangular region of one bitmap into another. The scaling factor of X axis and Y axis are independent. That is, user can scale up in X axis while scale down in Y axis. This function can be used in the display effect of pop-up menu and window creation or close.

9.7.7 Alpha Blending

Alpha blending means that you can copy a rectangular region of one bitmap into another. Glamo 3362 supports two kinds of alpha blending effects. One is constant alpha value. The formula is as follows:

Dst.R = (Src.R * Ac + (255 – Ac) * Dst.R) / 255

Dst.G = (Src.G * Ac + (255 – Ac) * Dst.G) / 255

Dst.B = (Src.B * Ac + (255 – Ac) * Dst.B) / 255

For constant alpha value, the color format of source supports ARGB8888, ARGB1555, ARGB4444 and RGB565. The color format of destination supports RGB565 and RGB555. Constant alpha value can be used in the display effect of fan-in and fan-out

The other is per-pixel alpha value in the source bitmap. source format The formula is as follows:

Dst.R = (Src.R * Src.A + (255 – Src.A) * Dst.R) / 255

Dst.G = (Src.G * Src.A + (255 – Src.A) * Dst.G) / 255

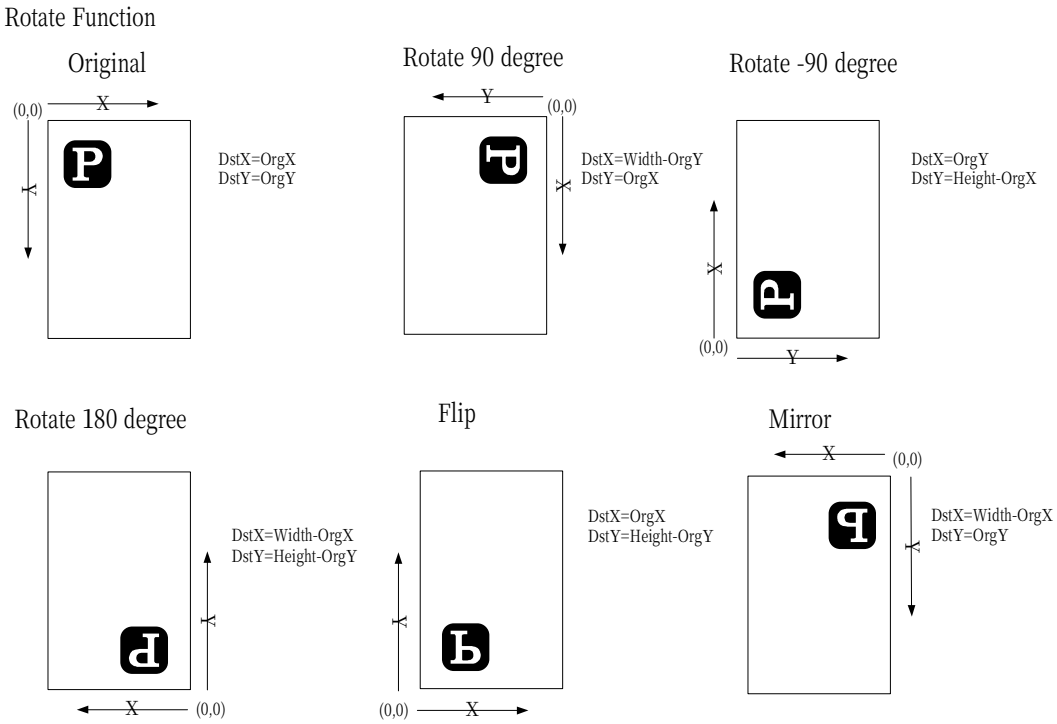
Dst.B = (Src.B * Src.A + (255 – Src.A) * Dst.B) / 255

For per-pixel alpha value, the color format of source supports ARGB8888, ARGB1555 and ARGB4444. The color format of destination supports RGB565 and RGB555. Per-pixel alpha value can be used in the display effect of merging two image and enhance the central part.

9.7.8 Rotation

Glamo 3362 2D engine supports five kinds of rotation, 90^0, -90^0, 180^0, Mirror, Flip

The definition of coordinate rotates as follows:

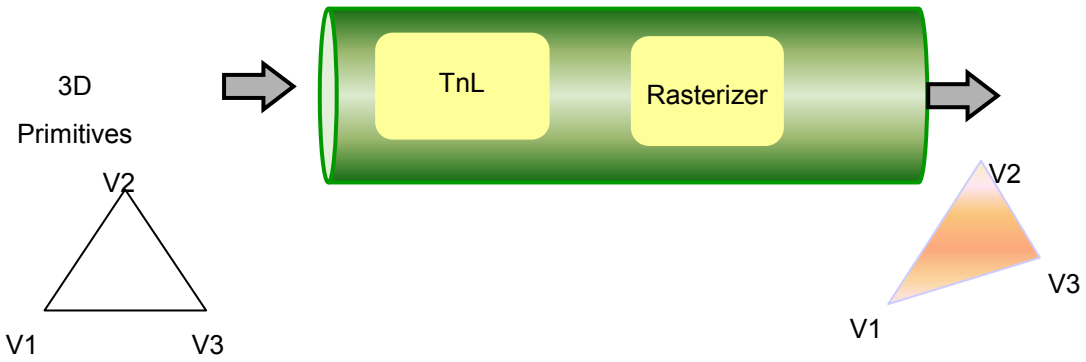


9.8 3D Graphics Engine

Glamo embeds 3D hardware accelerator which fully compliant with OpenGL ES v1.0, v1.1 and Mobile D3D, and max. 3D resolution is 511x511. Glamo supports wide range of data types (8-bit, 16-bit, 32-bit, fixed-point and floating-point) to reduce the computing load of processor. Glamo supports vertex buffering technology which can reduce the bus loading. Glamo supports all of 3D pipeline (Transform, cull, lighting, clipping, setup, and Rasterizer), it is very important in mobile application. Only the hardware accelerator can give the high quality and high performance 3D application in mobile device.

9.8.1 3D Engine Pipeline

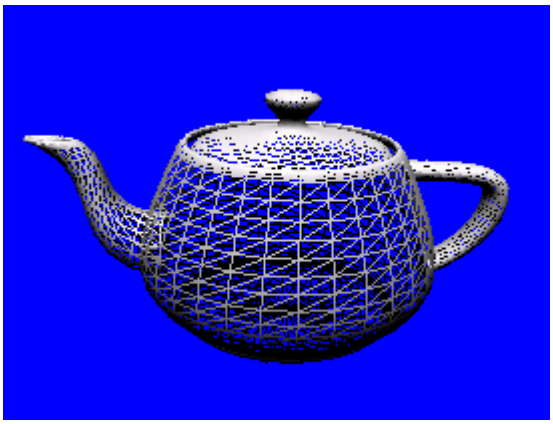
The following diagram shows the schematic diagram of the 3D accelerator. Commands are fed into the 3D engine on the left. The data formats of the commands are geometric primitives which described by vertices: points, line segments, and triangles. The first stage of 3D pipeline is vertices transform, lighting and clipped to a viewing volume. The second stage of 3D pipeline is rasterization the primitives. At this stage, the primitive will be converted to a two-dimensional image. Each pixel of this image contains color and depth information. Rasterizing a primitive consists of two parts. The first is to determine which pixels are occupied by the primitive. The second is assigning a depth value and color values to each pixel. The color value of pixels are determined by the shading operation, texture mapping, fog or alpha blending.



3D Pipeline Architecture

9.8.2 3D primitives

A 3D primitive is a collection of vertices to form a 3D object. The simplest primitive is 3D coordinate point set which is called a point list. Often, 3D primitives are polygons. The simplest polygon is a triangle. You can combine the triangles to form large, complex object. Following Figure shows a teapot triangle mesh.

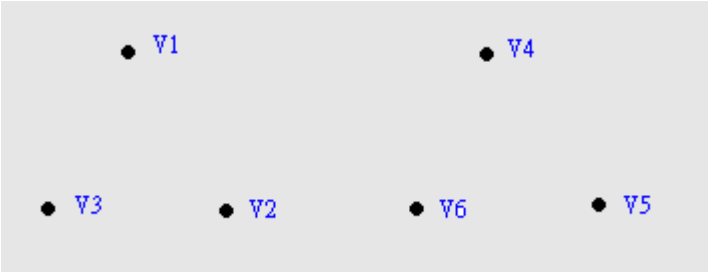


3D objects – teapot triangle mesh

Glamo can support following types of primitives.

Point lists

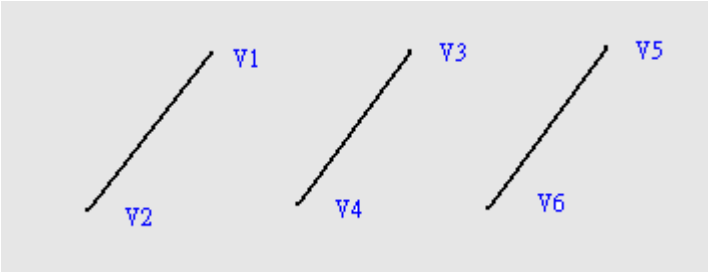
A point list is a collection of vertices that are rendered as isolated points. You can apply the materials, lights and textures to a point list. Following figure shows the rendered point list.



Example of point lists

Line Lists

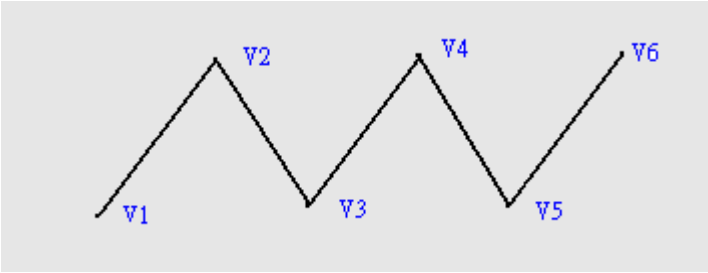
A line list is a list of isolated, straight line segments. You can apply materials, lights and textures to a line list. The colors in the material or texture appear only along the lines drawn, not at any point in between the lines. Following figure shows the rendered line list.



Example of line lists

Line Strips

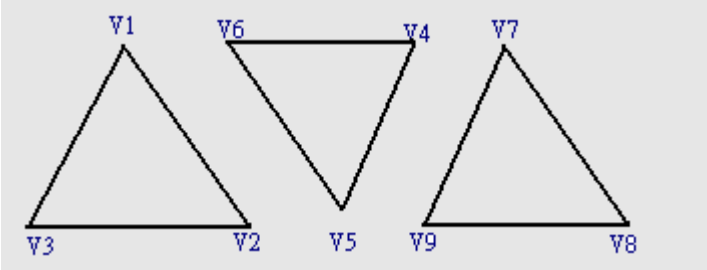
A line strip is a primitive which composed of connected line segments. Following figure shows the rendered Line Strips.



An example of line lists

Triangle Lists

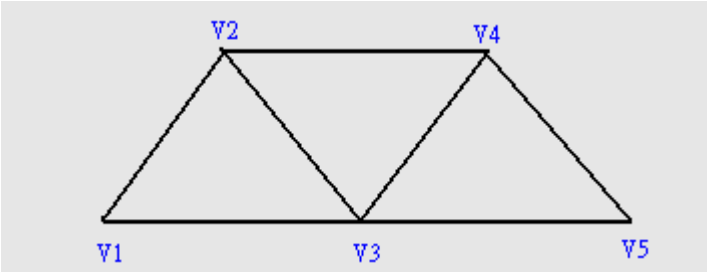
A triangle list is a list of isolated triangles. They may or may not be near each other. A triangle list must have at least three vertices and the total number of vertices must be divisibled by three. Following figure shows the rendered Triangle Lists.



An example of triangle lists

Triangle Strips

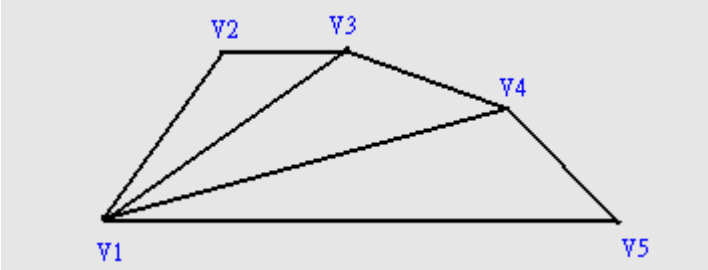
A triangle strip is a series of connected triangles. Because the triangles are connected, the application does not need to repeatedly specify all three vertices for each triangle. Most objects in 3D scenes are composed by triangle strips to reduce the vertices number and save memory sapce and improve processing time. Following figure shows the rendered Triangle Strips.



An example of triangle strips

Triangle Fans

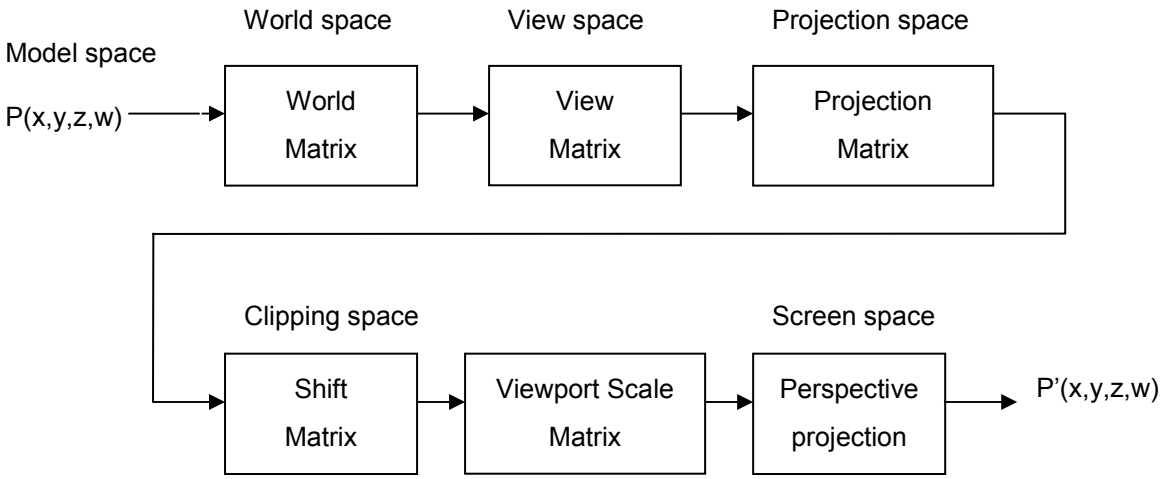
A triangle fan is similar to a triangle strip, excepting that all the triangles share one vertex. Following figure shows the rendered Triangle Fans.



An example of triangle fans

9.8.3 Transform

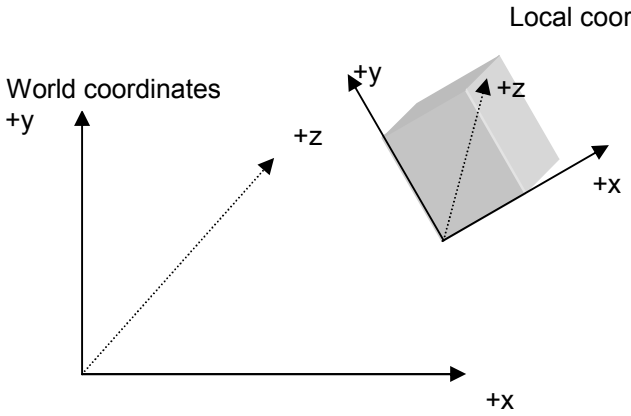
The transformation engine applies the world, view, and projection transformation and clips vertices to the view port. Following figure illustrates the transformation pipeline.



Transformation pipeline

World Space

The world transformation changes coordinates from model space to world space. The vertices are defined with respect to a common origin to all objects in the scene. World matrix includes the combination of translation, scaling and rotation operation. Following figure shows the relationship between the world coordinate system and a model's local coordinate system.



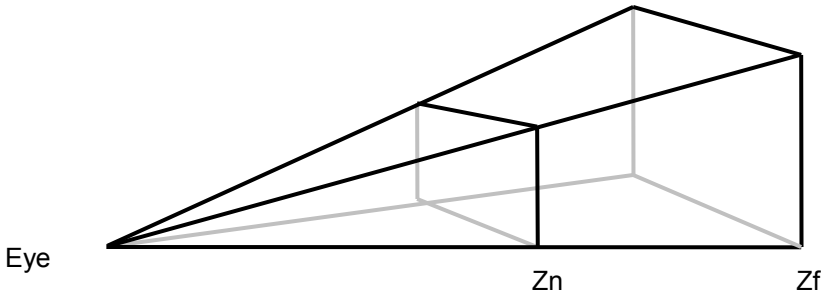
Relationship of world space and model's local space

View Space

View space is also known as camera space or eye space. The view transformation puts the viewer in world space and transforms vertices into view space. In view space, the viewer is at the origin and looks into the positive z-direction.

Projection space

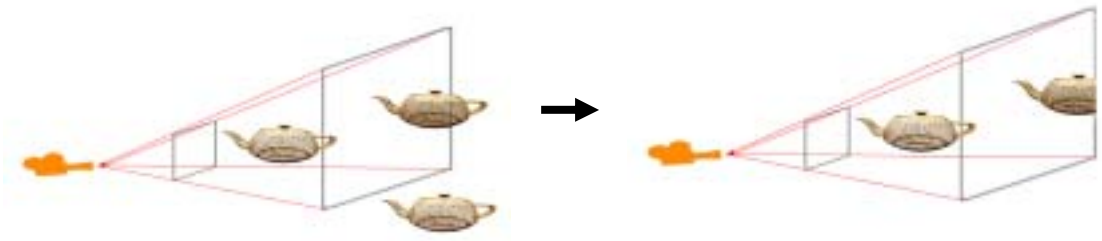
Projection space transform is to project the 3D view space onto a 2D space with depth. Projection space is a homogeneous space in which all vertices have x- and y-coordinates that range from –1.0 to 1.0, and a z-coordinate that ranges from 0.0 to 1.0. Following figure shows the view frustum. A viewing frustum is 3-D volume in a scene positioned relative to the view point. The shape of the volume affects how models are projected from view space onto the screen. The most common type of projection, a perspective projection, is responsible for making objects near the viewer appear bigger than objects in the distance.



View frustum

Clipping Volumes

D3DM and OpenGL ES define the clipping volume in clipping space. Any vertices that have an x, y, or z component outside these ranges are clipped. Following figure shows an example of clipping. After the clipping stage, we can use the view-port location and dimensions to scale the vertices to fit a rendered scene into the appropriate location on the target surface.



Example of clipping

Screen Space

After passing through the geometry pipeline, vertices have been transformed, clipped, and scaled to fit in the view-port on the render-target surface. After the perspective projection transform, we get the coordinate in screen space.

9.8.4 Lighting

Glamo support all the lighting type defined in D3DM and OpenGL ES (Point Light, Directional Light and Spot Light). Glamo can calculate all the Ambient Light, Diffuse Light, Specular Light and Emissive Light terms to determine the diffuse and specular color. Glamo supports up to 8 active light, and two side lighting in OpenGL.

Ambient

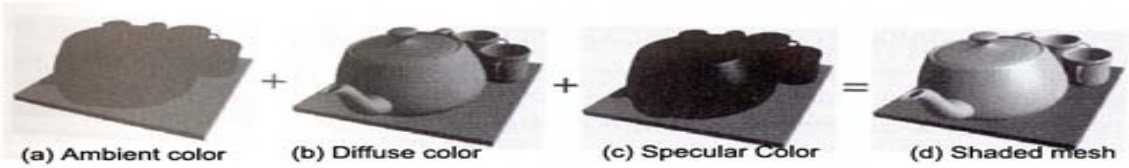
Ambient illumination is light that has been scattered by the environment, its direction is impossible to determine.

Diffuse

A diffuse light comes from one direction. Once it hits a surface, it is scattered equally in all directions. The diffuse color is decided not only by the diffuse color of the light and diffuse material of the object, but also by the surface normal and the light direction. However, the eye position will not affect the diffuse color.

Specular

Specular light comes from one direction, and it tends to bounce off the surface in a specific direction. It is decided not only by the specular color of the light and specular material of the object, but also by the surface normal, the light direction and the eye vector.

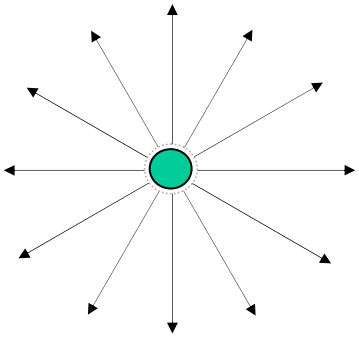


Light Type

Glamo support three light type: point light, directional light and spot light.

Point Light

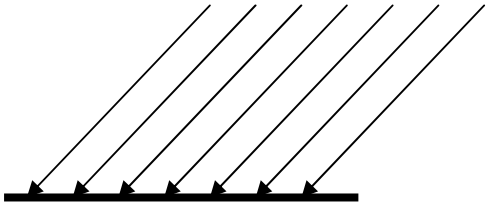
Point lights have to define color and position, but no single direction. The light illumination is equally in all directions. A good example of point light is a light bulb. Point light is affected by attenuation and range. Following figure shows an example of point light.



Example of point light

Directional Light

Directional lights have only color and direction, not position. All light generated by directional light travels through scene in the same direction. You can imagine a directional light as a light source at near infinite distance, such as the sun. Directional lights are not affected by attenuation or range. Following figure shows an example of directional light.

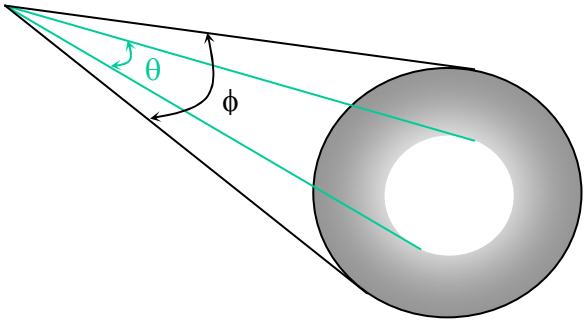


An example of direction light

Spot Lights

Spotlights have color, position, and direction in which they emit light. Spotlights are affected by falloff, attenuation, and range. Following figure shows the relationship between the value and how they can affect a spot light's inner

and outer cones of light. The “θ” value is the radian angle of the spotlight's inner cone, and the “Φ” value is the angle for the outer cone of light. The falloff value controls how light intensity decreases between the outer edge of the inner cone and the inner edge of the outer cone.



An example of spot light

9.8.5 Shading

Shading modes determine the intensity of color and lighting at any pixels on a polygon face. Glamo supports two shading modes: Flat shading and Gouraud shading.

Flat shading

In the flat shading mode, render using the color of the polygon material at its first vertex as the color for the entire polygon. 3D objects that are rendered with flat shading have visibly sharp edges between polygons if they are not coplanar. Following figure shows an example of flat shading.

An example of flat shading

Gouraud shading

In Gouraud shading mode, render all the pixels in the triangle using the color interpolation of three vertices color. Followin figure shows an example of Gouraud shading. Gouraud shading makes the surface of the object appear curved and smooth.

An example of Gouraud shading

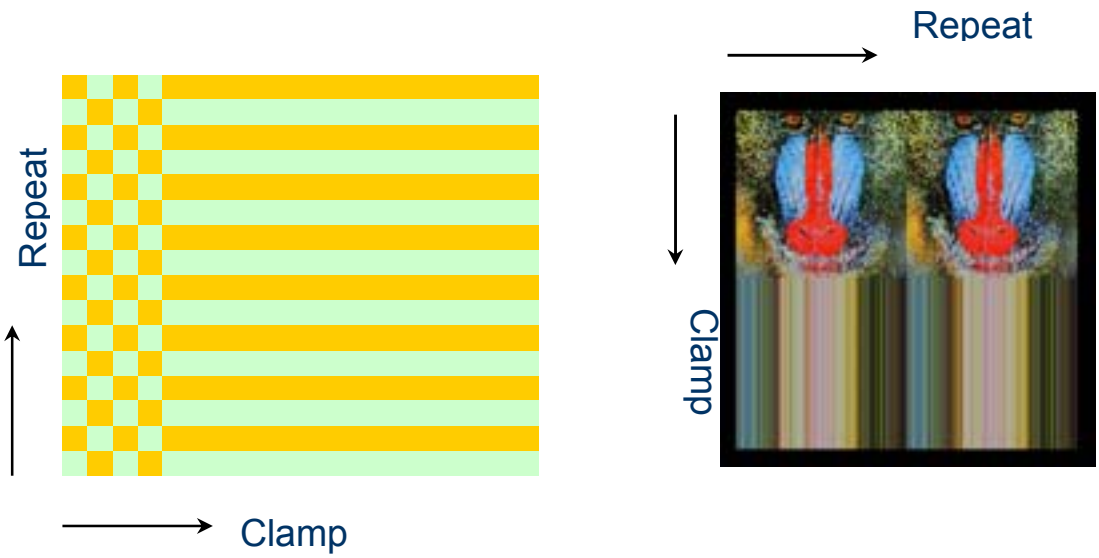
9.8.6 Textures Mapping

As we know texture mapping is a important technology in today's 3D game and 3D graphic, without texture mapping technology the world and model that are rendered would be far from realistic. Glamo supports an extensive texturing feature to provide developers easily accessing to advanced texturing techniques. Glamo supports maximum texture up to 256x256. Glamo also supports none-power-of-two texture and multiple textures. Following figure shows an example of texture mapping.

An example of texture mapping

Texture address mode

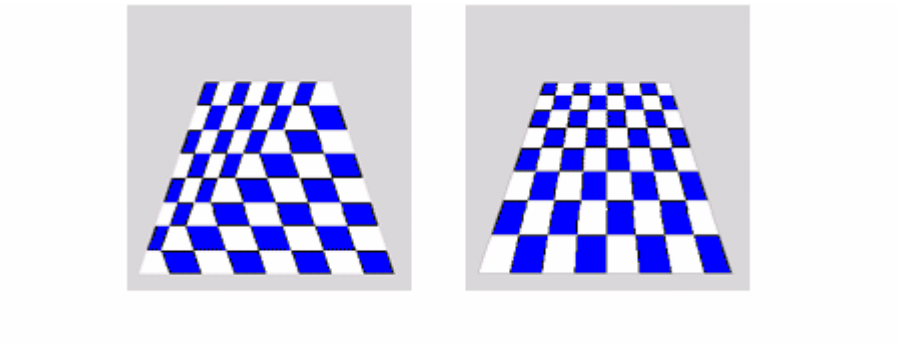
Typically, the texture coordinates that we assign to a vertex will be in the range of 0.0 to 1.0 inclusive. However, by assigning texture coordinates outside that range, we can create certain special texturing effects. We can control the texture coordinates that are outside the [0.0, 1.0] range by setting the texture addressing mode. Glamo supports all the addressing mode defined in D3DM and OpenGL ES (Repeat, Clamp, Mirror and Border). Following figure shows an example of texture address mode.



An example of texture address mode

Perspective Correction

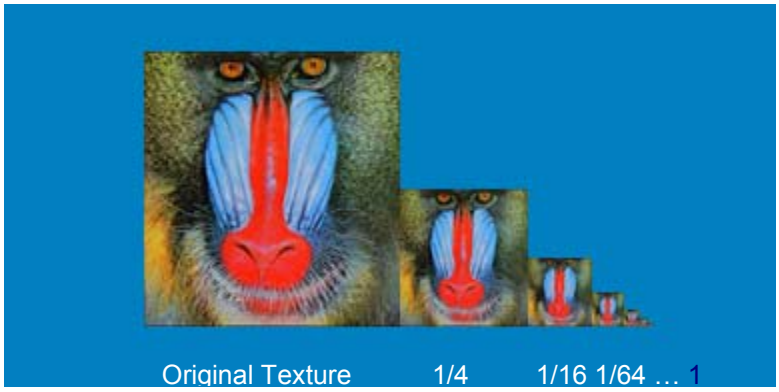
Without the perspective correction, the texture mapping will cause the incorrect in the 3D scene as shows in the following figure. Glamo supports per pixel perspective correction. Application can also enable or disable perspective correction. D3DM and OpenGL ES perspective correction are enabled by default.



Example of without perspective correction and with perspective correction

Texture MIPMAP

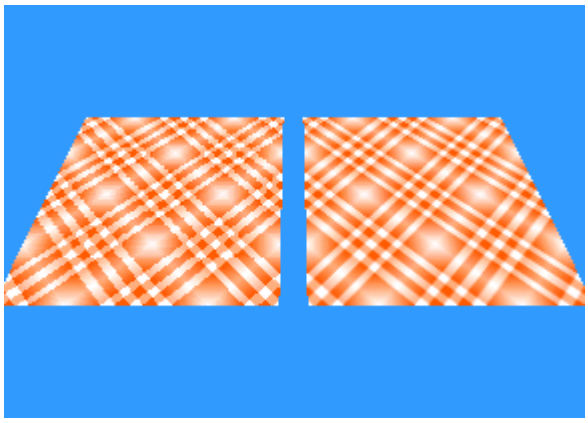
A mipmap is a sequence of textures, each of which is a progressively lower resolution representation of the same image. Mipmap textures are popularly used in 3D scenes to decrease the rendering time. They also improve the object realism. Glamo supports mipmap structure from 1x1 to 256x256. Following figure shows an example of mipmap texture.



An example of mipmap texture

Texture filtering

The pixels in the texture map are called texel. When a texture filter operation is performed, the texture can be magnified or minified. In other words, it is mapped onto a primitive image that is larger or smaller than itself. Magnification of a texture will cause that many pixels are mapped to one texel. The result is chunky appearance. Minification of a texture will cause that a single pixel is mapped to many texels. The result is blurry or aliased appearance. To resolve these problems, some blending of the texel colors must be filtered before mapping to the object. Glamo supports three types of texture filtering—linear filtering, nearest filtering and mipmap filtering. For mipmap filtering, Glamo can support NMN (Nearest-Mipmap-Nearest), NML (Nearest-Mipmap-Linear), LMN (Linear-Mipmap-Nearest), and LML (tri-linear) filtering. Following figure shows an example of texture filtering. The texture filter mode for left plane is nearest, the right plane is bi-linear. You can see the different between two planes.

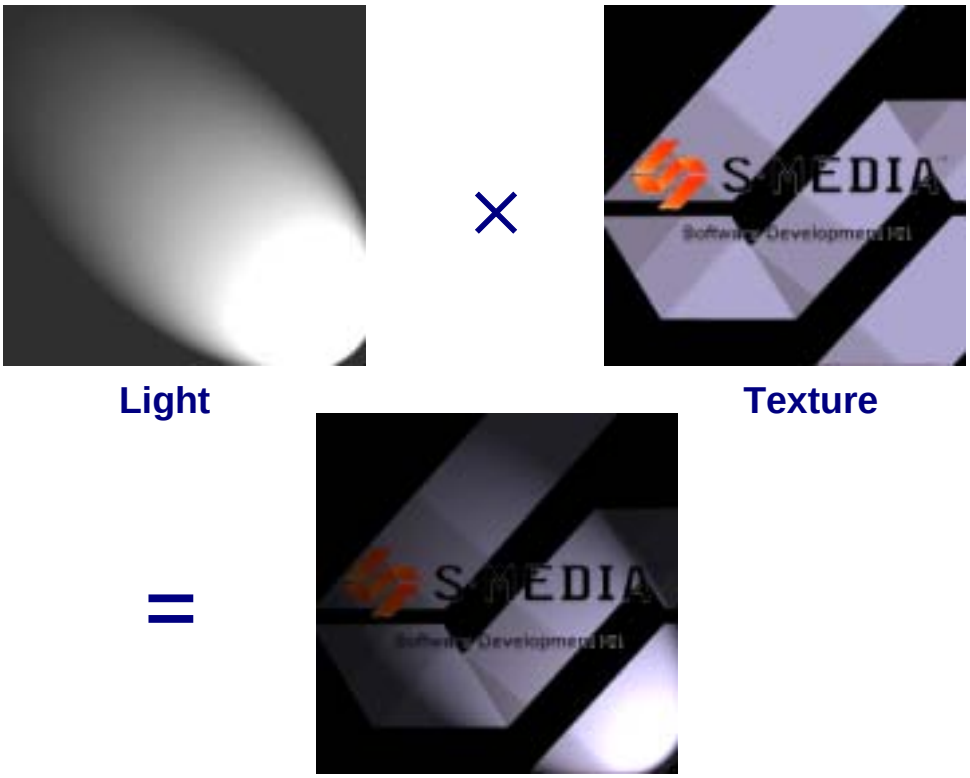


An example of texture filtering

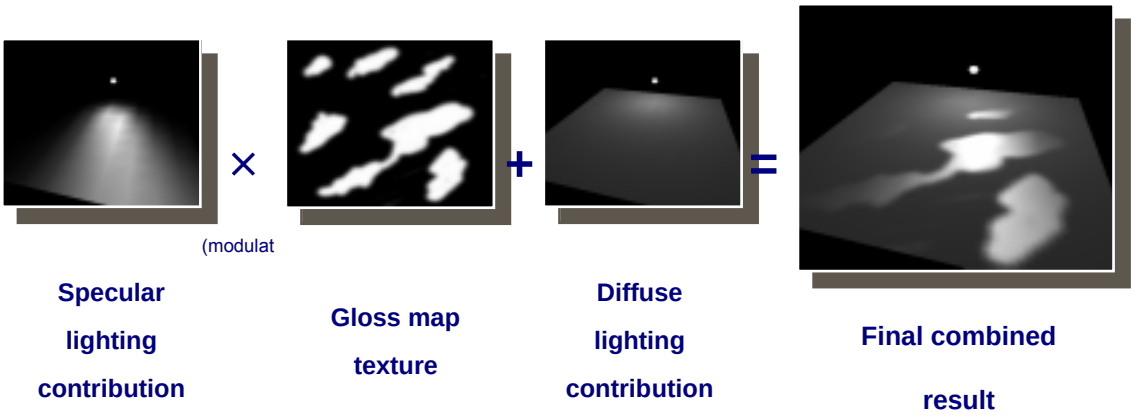
Texture Blending

D3DM and OpenGL ES can produce transparency effects by blending a texture with a primitive's color. It can also blends multiple textures onto a primitive. Glamo supports a texture combiner which can blend diffuse color,

specular color and multiple textures. Glamo can supports all the texture blending mode defined in D3DM and OpenGL ES. Following figure shows an example of multiple textures and example of texture blending.



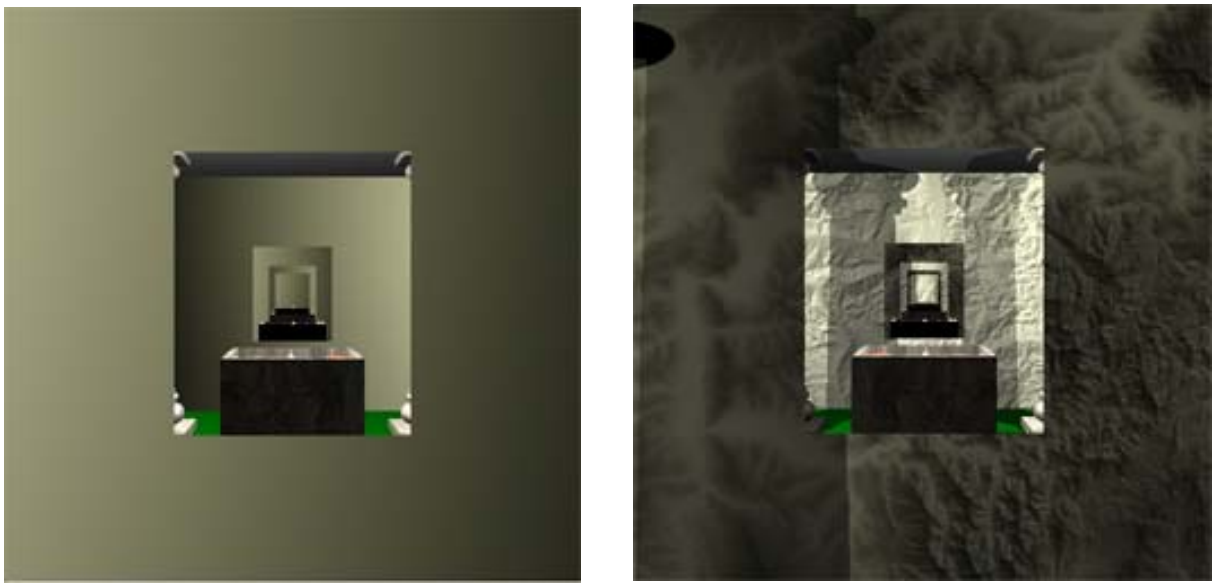
Example of multiple textures



Example of texture blending

Bump Mapping

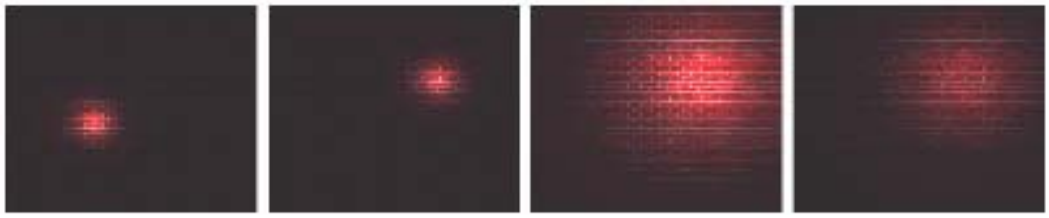
Bump mapping is a special form of specular or diffuse environment mapping that simulates the reflections of finely tessellated objects without requiring extremely high polygon counts. Bump mapping relies on blending multiple textures. Glamo supports multiple textures up to two and also have a programmable combiner can do such as dp3 or other operation. Following figure shows an example of bump mapping.



Example of bump mapping (a)without bumpmap (b) with bumpmap

Texture Transform

Glamo provides transform the texture coordinates of vertices by applying a 4×4 matrix. It is called the texture transform. The texture coordinate can be scaled, rotated, translated, projected, sheared or any bind of them. Texture coordinate transformations are useful to produce special effects without modifying the texture coordinates of existing geometry. You can use simple translation or rotation matrices to animate textures on an object. Following figure shows an example of texture transform.



Origina

Translate

Spotlight

Texture

Scale

Spotlight

Texture

Change Base

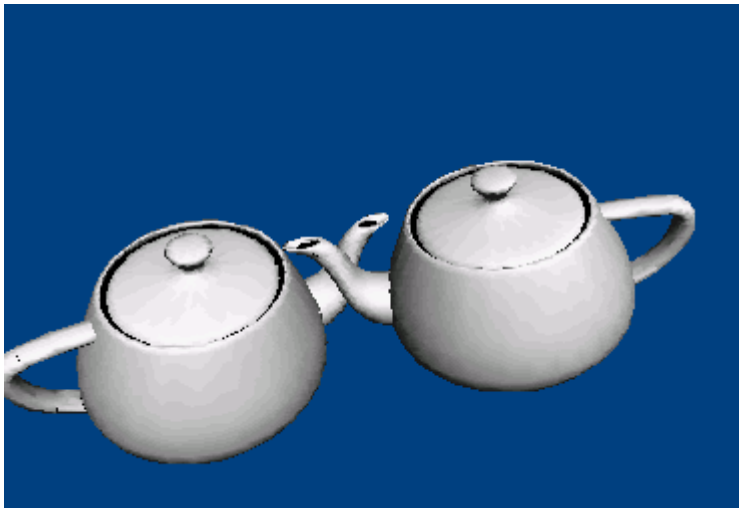
Polygon

Use texture matrix to perform spotlight texture coordinates transformations.

Example of texture transform

9.8.7 Z Buffer

Z buffer is a surface that stores depth information used in rending. When a 3D scene is rasterized with depth buffering enabled, each point on the rendering surface is tested. If the depth test is passed, means the new object is near to the viewer. Then the color can be updated to the target surface. The new depth value also can update to the Z buffer. Glamo supports the Z test and Z buffer. Glamo also supports polygon offset. Flolowing figure shows the result of two 3D objects with Z test.



The result of two 3D objects with z test.

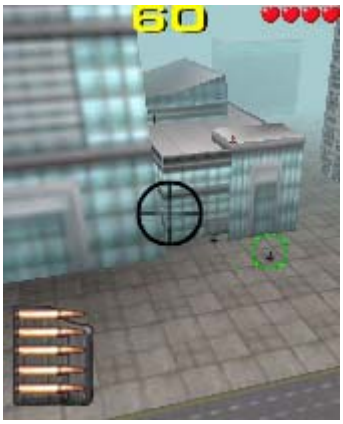
9.8.8 Stencil buffer

Applications use the stencil buffer to mask pixels on the image. The mask controls whether the pixel is drawn or not. Using stencil buffer can do some special effects. You can use the stencil buffer to composite 2D or 3D images onto a 3D scene. You also can do the special effects that are commonly used in movies, such as dissolves, swipes, and fades. For more abstract effects, such as outlining and silhouetting, you also can use stencil buffer to do it. Even the shadow effect also can be done by stencil buffer. Following figure shows an example of shadow which is done by stencil buffer.

Example of shadow

9.8.9 Fog

Adding fog to a 3D scene can enhance realism. Fog is implemented by blending the color of objects in a scene with a chosen fog color based on the depth of an object in a scene, or its distance from the viewpoint. Glamo provides two fog calculation, pixel fog and vertex fog. Pixel fog is implemented in the render pipeline and calculated the fog by pixel. Vertex fog is implemented in the light engine and calculated the fog by vertex and then, calculated each pixel fog value by shading. For different fog effect, Glamo supports the three kinds of fog types, linear, EXP and EXP2. Following figures shows a scene with fog effect.



The 3D scene with fog effect

9.8.10 Alpha Blending

Alpha blending is a combination of two colors with transparency effects in computer graphics. The alpha channel is additional bits that can present the level of translucency. The value of alpha in the color range from 0.0 to 1.0, where 0.0 represents a fully transparent, and 1.0 represents a fully opaque. Glamo fully supports all the blending modes define in the OpenGL ES and D3DM. Following figure shows an example of alpha blending.

Example of alpha blending

10 Registers

10.1 Register Mapping

Glamo 3362 registers are memory mapped. System accessing the address will directly map to the internal registers. The register space of each module is defined as following table.

Table 9-1 Glamo 3362 Register Mapping

Address	Function
0x000000h~0x0001FFh	General Register
0x000200h~0x0002FFh	Host Bus Controller Register
0x000300h~0x0003FFh	Memory Controller Register
0x000400h~0x0004FFh	Sensor Capture Controller Register
0x000500h~0x0007FFh	ISP Engine Register
0x000800h~0x000BFFh	JPEG Engine Register
0x000C00h~0x0010FFh	MPEG Engine Register
0x001100h~0x0014FFh	LCD Controller Register
0x001500h~0x00157Fh	Micro Processor 0 Register
0x001580h~0x0015FFh	Micro Processor 1 Register
0x001600h~0x00167Fh	Command Queue Register
0x001680h~0x0016FFh	RISC CPU Register
0x001700h~0x001AFFh	2D Engine Register
0x001B00h~0x0023FFh	3D Engine Register

10.2 Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results.

In the Type column of the register definition, the “R” means read only and “RW” means readable and writable. The Default Value means the initial value of the register after hardware reset.

10.3 Register Description

10.3.1 General Register

In General Register define the whole chip related setting which include the system configuration setting, hardware function enable bit, interrupt control, clock source control, software asynchronous reset of each module, PLL(Phase Lock Loop) control, GPIO control, and etc.

The following table defined the general register name and its address.

Address	Name
0x0000h	General Configuration Register 1
0x0002h	General Configuration Register 2
0x0004h	General Configuration Register 3
0x0006h	General Interrupt Register 1
0x0008h	General Interrupt Register 2
0x000Ah	General Interrupt Register 3
0x000Ch	General Interrupt Register 4
0x0010h	Host Clock Register
0x0012h	Memory Clock Register
0x0014h	LCD Clock Register
0x0016h	MMC Clock Register
0x0018h	ISP Clock Register
0x001Ah	JPEG Clock Register
0x001Ch	3D Clock Register
0x001Eh	2D Clock Register 8
0x0020h	Reserved
0x0022h	Reserved
0x0024h	MPEG Clock Register
0x0026h	Micro Processor Clock Register
0x0030h	General Clock Register 5-1
0x0032h	General Clock Register 5-2
0x0034h	General Clock Register 6
0x0036h	General Clock Register 7
0x0038h	General Clock Register 8
0x003Ah	General Clock Register 9
0x003Ch	General Clock Register 10
0x003Eh	General Clock Register 11
0x0040h	General PLL Register 1
0x0042h	General PLL Register 2

0x0044h	General PLL Register 3
0x0046h	General PLL Register 4
0x0048h	General PLL Register 5
0x0050h	General GPIO Register 1
0x0052h	General GPIO Register 2
0x0054h	General GPIO Register 3
0x0056h	General GPIO Register 4
0x0058h	General GPIO Register 5
0x005Ah	General GPIO Register 6
0x005Ch	General GPIO Register 7
0x005Eh	General GPIO Register 8
0x0060h	General GPIO Register 9
0x0062h	General GPIO Register 10
0x0070h	General DFT Register 1
0x0072h	General DFT Register 2
0x0074h	General DFT Register 3
0x0076h	General DFT Register 4
0x01E0h	General PLL Register 6
0x01F0h	General PLL Register 7

General Configuration Register 1

Read/Write Port: 0000h

Default Value: 0000h

Field	Bits	Type	Description
-	15:14	-	Reserved
Bypass_PLL	2	R	Clock source bypass PLL (bonding option from CFG2) 0: Clock source from PLL 1: Clock source bypass PLL but from OSCI input
Cpu_Bus_Type	1:0	R	CPU bus type selection (bonding option from CFG1 and CFG0) 00: Type 1 direct addressing mode 01: Type 2 direct addressing mode 10: Type 3 iBurst mode 11: Type 4 indirect addressing mode

General Configuration Register 2

Read/Write Port: 0002h

Default Value: 3650h

Field	Bits	Type	Description
Device_ID	15:0	R	Device ID

General Configuration Register 3

Read/Write Port: 0004h

Default Value: 0000h

Field	Bits	Type	Description
Revision_ID	15:0	R	Revision ID

General Interrupt Register 1

Read/Write Port: 0006h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
Interrupt_Select	9	RW	Select interrupt direction 0: Select interrupt to Base band 1: Select interrupt to RISC CPU
En_OR_Int	8	RW	Reserved for RISC interrupt enable 0: Disable 1: Enable
En_MMC_Int	7	RW	MMC interrupt enable 0: Disable 1: Enable
En_2D_Int	6	RW	2D interrupt enable 0: Disable 1: Enable
En_CQ_Int	5	RW	Command queue interrupt enable 0: Disable 1: Enable
En_P0_Int	4	RW	Micro processor 0 interrupt enable 0: Disable 1: Enable
En_P1_Int	3	RW	Micro processor 1 interrupt enable 0: Disable

			1: Enable
En_MPEG_Int	2	RW	MPEG interrupt enable 0: Disable 1: Enable
En_JPEG_Int	1	RW	JPEG interrupt enable 0: Disable 1: Enable
En_HBC_Int	0	RW	Host bus controller interrupt enable 0: Disable 1: Enable

General Interrupt Register 2

Read/Write Port: 0008h

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
Set_OR_Int	8	RW	Reserved for Set RISC CPU interrupt 0: No operation 1: Set interrupt
Set_MMC_Int	7	RW	Set MMC interrupt 0: No operation 1: Set interrupt
Set_2D_Int	6	RW	Set 2D interrupt 0: No operation 1: Set interrupt
Set_CQ_Int	5	RW	Set command queue interrupt 0: No operation 1: Set interrupt
Set_P0_Int	4	RW	Set Micro processor 0 interrupt 0: No operation 1: Set interrupt
Set_P1_Int	3	RW	Set Micro processor 1 interrupt 0: No operation 1: Set interrupt
Set_MPEG_Int	2	RW	Set MPEG interrupt 0: No operation 1: Set interrupt
Set_JPEG_Int	1	RW	Set JPEG interrupt 0: No operation

			1: Set interrupt
Set_HBC_Int	0	RW	Set host bus controller interrupt 0: No operation 1: Set interrupt

General Interrupt Register 3

Read/Write Port: 000Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
Clr_OR_Int	8	W	Reserved for Clear RISC CPU interrupt 0: No operation 1: Clear interrupt
Clr_MMC_Int	7	W	Clear MMC interrupt 0: No operation 1: Clear interrupt
Clr_2D_Int	6	W	Clear 2D interrupt 0: No operation 1: Clear interrupt
Clr_CQ_Int	5	W	Clear command queue interrupt 0: No operation 1: Clear interrupt
Clr_P0_Int	4	W	Clear Micro processor interrupt 0: No operation 1: Clear interrupt
Clr_P1_Int	3	W	Clear Micro processor 1 interrupt 0: No operation 1: Clear interrupt
Clr_MPEG_Int	2	W	Clear MPEG interrupt 0: No operation 1: Clear interrupt
Clr_JPEG_Int	1	W	Clear JPEG interrupt 0: No operation 1: Clear interrupt
Clr_HBC_Int	0	W	Clear host bus controller interrupt 0: No operation 1: Clear interrupt

General Interrupt Register 4

Read/Write Port: 000Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
RISC_Int	8	R	Reserved for RISC CPU interrupt status 0: No interrupt occurred 1: An interrupt occurred
MMC_Int	7	R	MMC interrupt status 0: No interrupt occurred 1: An interrupt occurred
2D_Int	6	R	2D interrupt status 0: No interrupt occurred 1: An interrupt occurred
CQ_Int	5	R	Command queue interrupt status 0: No interrupt occurred 1: An interrupt occurred
P0_Int	4	R	Micro processor 0 interrupt status 0: No interrupt occurred 1: An interrupt occurred
P1_Int	3	R	Micro processor 1 interrupt status 0: No interrupt occurred 1: An interrupt occurred
MPEG_Int	2	R	MPEG interrupt status 0: No interrupt occurred 1: An interrupt occurred
JPEG_Int	1	R	JPEG interrupt status 0: No interrupt occurred 1: An interrupt occurred
HBC_Int	0	R	Host bus controller interrupt status 0: No interrupt occurred 1: An interrupt occurred

Host Clock Register

Read/Write Port: 0010h

Default Value: 0000h

Field	Bits	Type	Description
	15:13	RW	Reserved

HBC_Rst	12	RW	Reset host bus controller 0: Normal operation 1: Reset
	11:4	RW	Reserved
En_M0CLK	3	RW	Enable M0CLK (memory clock in host bus controller) 0: Disable 1: Enable
En_DG_M0CLK	2	RW	Enable dynamic gating M0CLK 0: Disable 1: Enable
	1	RW	Reserved
En_DG_BCLK	0	RW	Enable dynamic gating BCLK 0: Disable 1: Enable

Memory Clock Register

Read/Write Port: 0012h

Default Value: 0000h

Field	Bits	Type	Description
	15:14	RW	Reserved
MOCA_Rst	13	RW	Reset MOCA-J 0: Normal operation 1: Reset
Mem_Rst	12	RW	Reset memory controller 0: Normal operation 1: Reset
	11:4	RW	Reserved
En_MOCACLK	3	RW	Enable MOCACLK (MOCA-J clock) 0: Disable 1: Enable
En_DG_MOCACLK	2	RW	Enable dynamic gating MOCACLK (MOCA-J clock) 0: Disable 1: Enable
En_M1CLK	1	RW	Enable M1CLK (memory clock in memory controller) 0: Disable 1: Enable
En_DG_M1CLK	0	RW	Enable dynamic gating M1CLK

			0: Disable 1: Enable

LCD Clock Register

Read/Write Port: 0014h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	RW	Reserved
LCD_Rst	12	RW	Reset LCD controller 0: Normal operation 1: Reset
-	11:8	RW	Reserved
En_M5CLK	7	RW	Enable M5CLK (memory clock in LCD controller) 0: Disable 1: Enable
En_DG_M5CLK	6	RW	Enable dynamic gating M5CLK 0: Disable 1: Enable
En_DHCLK	5	RW	Enable DHCLK (LCD controller high frequency clock) 0: Disable 1: Enable
Reserved for En_DG_ DHCLK	4	RW	Reserved
En_DMCLK	3	RW	Enable DMCLK (LCD controller middle frequency clock) 0: Disable 1: Enable
En_DG_DMCLK	2	RW	Enable dynamic gating DMCLK 0: Disable 1: Enable
En_DCLK	1	RW	Enable DCLK (LCD controller clock) 0: Disable 1: Enable
Reserved for En_DG_DCLK	0	RW	Enable dynamic gating DCLK 0: Disable 1: Enable

MMC Clock Register

Read/Write Port: 0016h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	RW	Reserved
MMC_Rst	12	RW	Reset MMC controller 0: Normal operation 1: Reset
-	11:4	RW	Reserved
En_M9CLK	3	RW	Enable M9CLK (memory clock in MMC controller) 0: Disable 1: Enable
En_DG_M9CLK	2	RW	Enable dynamic gating M9CLK 0: Disable 1: Enable
En_TCLK	1	RW	Enable TCLK (MMC controller clock) 0: Disable 1: Enable
En_DG_TCLK	0	RW	Enable dynamic gating TCLK 0: Disable 1: Enable

ISP Clock Register

Read/Write Port: 0018

Default Value: 0000h

Field	Bits	Type	Description
-	15:14	RW	Reserved
ISP2_Rst	13	RW	Reset image signal processor 2 0: Normal operation 1: Reset
ISP1_Rst	12	RW	Reset image signal processor 1 0: Normal operation 1: Reset
-	11:10	RW	Reserved
En_M15CLK	9	RW	Enable M15CLK (memory clock in image signal processor 1) 0: Disable (Capture Memory Clock) 1: Enable
En_DG_M15CLK	8	RW	Enable dynamic gating M15CLK 0: Disable 1: Enable
En_M2CLK	7	RW	Enable M2CLK (memory clock in image signal processor 2) 0: Disable

			1: Enable
En_DG_M2CLK	6	RW	Enable dynamic gating M2CLK 0: Disable 1: Enable
En_SCLK	5	RW	Enable SCLK (clock to sensor) 0: Disable 1: Enable
Reserved for En_DG_SCLK	4	RW	Reserved
En_CCLK	3	RW	Enable CCLK (image signal processor 1(Capture) clock) 0: Disable 1: Enable
En_DG_CCLK	2	RW	Enable dynamic gating CCLK 0: Disable 1: Enable
En_I1CLK	1	RW	Enable I1CLK (image signal processor 2 clock) 0: Disable 1: Enable
En_DG_I1CLK	0	RW	Enable dynamic gating I1CLK 0: Disable 1: Enable

JPEG Clock Register

Read/Write Port: 001A

Default Value: 0000h

Field	Bits	Type	Description
	15:13	RW	Reserved
JPEG_Rst	12	RW	Reset JPEG engine 0: Normal operation 1: Reset
	11:4	RW	Reserved
En_M3CLK	3	RW	Enable M3CLK (memory clock in JPEG engine) 0: Disable 1: Enable
En_DG_M3CLK	2	RW	Enable dynamic gating M3CLK 0: Disable 1: Enable
En_JCLK	1	RW	Enable JCLK (JPEG engine clock)

			0: Disable 1: Enable
En_DG_JCLK	0	RW	Enable dynamic gating JCLK 0: Disable 1: Enable

3D Clock Register

Read/Write Port: 001C

Default Value: 0000h

Field	Bits	Type	Description
	15:14	RW	Reserved
3D_Front_Rst	13	RW	Reset 3D front engine 0: Normal operation 1: Reset
3D_Back_Rst	12	RW	Reset 3D back engine 0: Normal operation 1: Reset
	11:6	RW	Reserved
En_M8CLK	5	RW	Enable M8CLK (memory clock in 3D engine) 0: Disable 1: Enable
En_DG_M8CLK	4	RW	Enable dynamic gating M8CLK 0: Disable 1: Enable
En_RCLK	3	RW	Enable RCLK (3D engine front clock) 0: Disable 1: Enable
En_DG_RCLK	2	RW	Enable dynamic gating RCLK 0: Disable 1: Enable
En_ECLK	1	RW	Enable ECLK (3D engine back clock) 0: Disable 1: Enable
En_DG_ECLK	0	RW	Enable dynamic gating ECLK 0: Disable 1: Enable

2D Clock Register

Read/Write Port: 001E

Default Value: 0000h

Field	Bits	Type	Description
	15:14	RW	Reserved
CQ_Rst	13	RW	Reset command queue 0: Normal operation 1: Reset
2D_Rst	12	RW	Reset 2D engine 0: Normal operation 1: Reset
	11:6	RW	Reserved
En_M6CLK	5	RW	Enable M6CLK (memory clock in command queue) 0: Disable 1: Enable
En_DG_M6CLK	4	RW	Enable dynamic gating M6CLK 0: Disable 1: Enable
En_M7CLK	3	RW	Enable M7CLK (memory clock in 2D engine) 0: Disable 1: Enable
En_DG_M7CLK	2	RW	Enable dynamic gating M7CLK 0: Disable 1: Enable
En_GCLK	1	RW	Enable GCLK (2D engine clock) 0: Disable 1: Enable
En_DG_GCLK	0	RW	Enable dynamic gating GCLK 0: Disable 1: Enable

MPEG Clock Register

Read/Write Port: 0024

Default Value: 0000h

Field	Bits	Type	Description
	15:14	RW	Reserved
MPEG_Dec_Rst	13	RW	Reset MPEG decoder 0: Normal operation 1: Reset
MPEG_Cod_Rst	12	RW	Reset MPEG encoder 0: Normal operation

			1: Reset
En_X6CLK	11	RW	Enable X6CLK (MPEG deblocking clock) 0: Disable 1: Enable
En_DG_X6CLK	10	RW	Enable dynamic gating X6CLK 0: Disable 1: Enable
En_X4CLK	9	RW	Enable X4CLK (MPEG decoder clock) 0: Disable 1: Enable
En_DG_X4CLK	8	RW	Enable dynamic gating X4CLK 0: Disable 1: Enable
En_X3CLK	7	RW	Enable X3CLK (MPEG decoder clock) 0: Disable 1: Enable
En_DG_X3CLK	6	RW	Enable dynamic gating X3CLK 0: Disable 1: Enable
En_X2CLK	5	RW	Enable X2CLK (MPEG decoder clock) 0: Disable 1: Enable
En_DG_X2CLK	4	RW	Enable dynamic gating X2CLK 0: Disable 1: Enable
En_X1CLK	3	RW	Enable X1CLK (MPEG encoder TC clock) 0: Disable 1: Enable
En_DG_X1CLK	2	RW	Enable dynamic gating X1CLK 0: Disable 1: Enable
En_X0CLK	1	RW	Enable X0CLK (MPEG encoder ME clock) 0: Disable 1: Enable
En_DG_X0CLK	0	RW	Enable dynamic gating X0CLK 0: Disable 1: Enable

Micro Processor Clock Register

Read/Write Port: 0026

Default Value: 0000h

Field	Bits	Type	Description
	15:13	RW	Reserved
B0I0_Rst	12	RW	Reset Micro Processor of ISP 0: Normal operation 1: Reset
	10:11	RW	Reserved
En_M10CLK	9	RW	Enable M10CLK (memory clock in Micro processor 0 (for ISP)) 0: Disable 1: Enable
En_DG_M10CLK	8	RW	Enable dynamic gating M10CLK 0: Disable 1: Enable
En_M4CLK	7	RW	Enable M4CLK (memory clock in MPEG and Micro processor 1) 0: Disable 1: Enable
En_DG_M4CLK	6	RW	Enable dynamic gating M4CLK 0: Disable 1: Enable
En_KCLK	5	RW	Enable KCLK (system clock for timer in micro processors) 0: Disable 1: Enable
	4	RW	Reserved
En_X5CLK	3	RW	Enable X5CLK (Micro processor 1 (for MPEG) clock) 0: Disable 1: Enable
En_DG_X5CLK	2	RW	Enable dynamic gating X5CLK 0: Disable 1: Enable
En_I0CLK	1	RW	Enable I0CLK (Micro processor 0 (for ISP) clock) 0: Disable 1: Enable
En_DG_I0CLK	0	RW	Enable dynamic gating I0CLK 0: Disable 1: Enable

General Clock Register 5_1

Read/Write Port: 0030h

Default Value: 1801h

Field	Bits	Type	Description
-	15	-	Reserved
Sel_KCLK_Src	14	RW	Select the clock source of KCLK 0: From OSCI input 1: From PLL
Sys_Timer_Rst	13	RW	Reset system timer 0: Normal operation 1: Reset
En_Sys_Timer	12	RW	Enable system timer 0: Disable 1: Enable
En_Sys_CLK	11	RW	Enable system clock 0: Disable 1: Enable
Clk_From_OSCI	10	RW	Select the clock source of all clock dividers 0: Clock source from PLL 1: Clock source bypass PLL but from OSCI input
Sel_CCLK_Src	9:8	RW	Select the clock source of CCLK 00: From PCLK 01: From PCLK but with opposite phase 10: From SCLK 11: From SCLK but with opposite phase
En_Div_TCLK	7	RW	Enable the divider for generating TCLK 0: Disable 1: Enable
En_Div_GCLK	6	RW	Enable the divider for generating GCLK, E0CLK and E1CLK 0: Disable 1: Enable
En_Div_DHCLK	5	RW	Enable the divider for generating DHCLK 0: Disable 1: Enable
En_Div_DMCLK	4	RW	Enable the divider for generating DMCLK 0: Disable 1: Enable
En_Div_DCLK	3	RW	Enable the divider for generating DCLK 0: Disable

			1: Enable
En_Div_JCLK	2	RW	Enable the divider for generating I0CLK, I1CLK, JCLK, X0CLK, X1CLK and ZCLK 0: Disable 1: Enable
En_Div_SCLK	1	RW	Enable the divider for generating SCLK and CCLK 0: Disable 1: Enable
En_Div_MCLK	0	RW	Enable the divider for generating M0CLK~M8CLK and MCLKStrobe 0: Disable 1: Enable

General Clock Register 5_2

Read/Write Port: 0032h

Default Value: 0000h

Field	Bits	Type	Description
-	15	-	Reserved
AMCLK_Ratio	14:8	RW	Reserved for AMCLK divide ratio 0000000: 1:1 0000001: 2:1 0000010: 3:1 …… 1111111: 128:1
	7:5	RW	Reserved
En_Div_ICLK	4	RW	Enable the divider for generating ICLK 0: Disable 1: Enable
En_Div_ZCLK	3	RW	Reserved for Enable the divider for generating ZCLK 0: Disable 1: Enable
En_Div_OCLK	2	RW	Reserved for Enable the divider for generating O1CLK, O2CLK 0: Disable 1: Enable
En_Div_AMCLK	1	RW	Reserved for Enable the divider for generating AMCLK 0: Disable 1: Enable
En_Div_ACLK	0	RW	Reserved for Enable the divider for generating ACLK 0: Disable

			1: Enable

General Clock Register 6

Read/Write Port: 0034h

Default Value: 8000h

Field	Bits	Type	Description
RF_CLKA_Dly	15:12	RW	Register file write pulse delay. 0000: delay 0.5 ns 0001: delay 1.0 ns …… 1111: delay 8.0 ns
-	11:10	-	Reserved
DHCLK_Ratio	9:8	RW	DHCLK divide ratio 00: 1:1 01: 2:1 10: 3:1 11: 4:1
GCLK_Ratio	7:6	RW	GCLK divide ratio 00: 1:1 01: 2:1 10: 3:1 11: 4:1
JCLK_Ratio	5:4	RW	JCLK divide ratio 00: 1:1 01: 2:1 10: 3:1 11: 4:1
MCLK_Ratio	3:2	RW	MCLK divide ratio 00: 1:1 01: 2:1 10: 3:1 11: 4:1
BCLK_Ratio	1:0	RW	BCLK divide ratio 00: 1:1 01: 2:1 10: 3:1 11: 4:1

General Clock Register 7

Read/Write Port: 0036h

Default Value: 0000h

Field	Bits	Type	Description
DMCLK_Ratio	15:8	RW	DMCLK divide ratio 00000000: 1:1 00000001: 2:1 00000010: 3:1 …… 11111111: 256:1
DCLK_Ratio	7:0	RW	DCLK divide ratio 00000000: 1:1 00000001: 2:1 00000010: 3:1 …… 11111111: 256:1

General Clock Register 8

Read/Write Port: 0038h

Default Value: 0000h

Field	Bits	Type	Description
SCLK_Ratio	15:8	RW	SCLK divide ratio 00000000: 1:1 00000001: 2:1 00000010: 3:1 …… 11111111: 256:1
TCLK_Ratio	7:0	RW	TCLK divide ratio 00000000: 1:1 00000001: 2:1 00000010: 3:1 …… 11111111: 256:1

General Clock Register 9

Read/Write Port: 003Ah

Default Value: 0000h

Field	Bits	Type	Description
CCLK_Dly	15:0	RW	CCLK delay. Four delay cells compose the delay chain. The

			delay cells are controlled by bit [3:0], [7:4], [11:8] and [15:12] separately. Each delay cell is: 0000: delay 0.5 ns 0001: delay 1.0 ns …… 1111: delay 8.0 ns

General Clock Register 10

Read/Write Port: 003Ch

Default Value: 0000h

Field	Bits	Type	Description
OCLK_Ratio	15:12	RW	Reserved for OCLK divide ratio 0000: 1:1 0001: 2:1 0010: 3:1 …… 1111: 16:1
ACLK_Ratio	11:0	RW	Reserved for ACLK divide ratio 000000000000: 1:1 000000000001: 2:1 000000000010: 3:1 …… 111111111111: 4096:1

General Clock Register 11

Read/Write Port: 003Eh

Default Value: 0000h

Field	Bits	Type	Description
ICLK_Ratio	15:11	RW	ICLK divide ratio 00000: 1:1 00001: 2:1 00010: 3:1 …… 11111: 32:1
	10	RW	Reserved
ZCLK_Ratio	9:0	RW	Reserved for ZCLK divide ratio 0000000000: 1:1 0000000001: 2:1 0000000010: 3:1

			…… 1111111111: 1024:1

General PLL Register 1

Read/Write Port: 0040h

Default Value: 0400h

Field	Bits	Type	Description
-	15:12	-	Reserved
Pll_Num1	11:0	RW	PLL1 numerator

General PLL Register 2

Read/Write Port: 0042h

Default Value: 0000h

Field	Bits	Type	Description
DCO_Gain1	15:0	R	DCO1 (Digital Controlled Oscillator) gain

General PLL Register 3

Read/Write Port: 0044h

Default Value: 0400h

Field	Bits	Type	Description
-	15:14	-	Reserved
Pll_PD2	13	RW	PLL2 Power down 0 : Normal operation 1 : Power down
Pll_Bypass2	12	RW	PLL2 By Pass mode 0 : Normal operation 1 : By Pass mode Enable
Pll_Num2	11:0	RW	PLL2 numerator

General PLL Register 4

Read/Write Port: 0046h

Default Value: 0000h

Field	Bits	Type	Description
DCO_Gain2	15:0	R	DCO2 (Digital Controlled Oscillator) gain

General PLL Register 5

Read/Write Port: 0048h

Default Value: 0000h

Field	Bits	Type	Description
-	15:2	-	Reserved
Pll_PhaseLock2	1	R	PLL2 Phase Lock
Pll_PhaseLock1	0	R	PLL1 Phase Lock

General GPIO Register 1

Read/Write Port: 0050h

Default Value: 000Fh

Field	Bits	Type	Description
Sel_GPIO_Pin	15:12	RW	Where GPIO[3:0] share with other pins: GPIO3 share with HA23 GPIO2 share with HA22 GPIO1 share with HA21 GPIO0 share with HA20 Turn on this bit to select GPIO[3:0] pin 0: Select normal pin 1: Select GPIO pin
GPIOI	11:8	R	The input data of GPIO[3:0]
GPIOO	7:4	RW	The output data of GPIO[3:0]
En_GPIO_ON	3:0	RW	Enable GPIO[3:0] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 2

Read/Write Port: 0052h

Default Value: 000Fh

Field	Bits	Type	Description
Sel_GPIO_Pin	15:12	RW	Where GPIO[7:4] share with other pins: GPIO7 share with LDE# GPIO6 share with LDCLK GPIO5 share with LCS1#

			GPIO4 share with LCS0# Turn on this bit to select GPIO[7:4] pin 0: Select normal pin 1: Select GPIO pin
GPIOI	11:8	R	The input data of GPIO[7:4]
GPIOO	7:4	RW	The output data of GPIO[7:4]
En_GPIO_ON	3:0	RW	Enable GPIO[7:4] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 3

Read/Write Port: 0054h

Default Value: 000Fh

Field	Bits	Type	Description
Sel_GPIO_Pin	15:12	RW	Where GPIO[11:8] share with other pins: GPIO11 share with LSDA GPIO10 share with LSCK GPIO9 share with LD17 GPIO8 share with LD16 Turn on this bit to select GPIO[11:8] pin 0: Select normal pin 1: Select GPIO pin
GPIOI	11:8	R	The input data of GPIO[11:8]
GPIOO	7:4	RW	The output data of GPIO[11:8]
En_GPIO_ON	3:0	RW	Enable GPIO[11:8] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 4

Read/Write Port: 0056h

Default Value: 000Fh

Field	Bits	Type	Description
Sel_GPIO_Pin	15:12	RW	Where GPIO[15:12] share with other pins: GPIO15 share with FLCTL GPIO14 share with CSGPO1

			GPIO13 share with CSGPO0 GPIO12 share with LSA0 Turn on this bit to select GPIO[15:12] pin 0: Select normal pin 1: Select GPIO pin
GPIOI	11:8	R	The input data of GPIO[15:12]
GPIOO	7:4	RW	The output data of GPIO[15:12]
En_GPIO_ON	3:0	RW	Enable GPIO[15:12] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 5

Read/Write Port: 0058h

Default Value: 000Fh

Field	Bits	Type	Description
Sel_GPIO_Pin	15:12	RW	Where GPIO[19:16] share with other pins: GPIO19 share with HADVN GPIO18 share with MMCDAT3 GPIO17 share with MMCDAT2 GPIO16 share with MMCDAT1 Turn on this bit to select GPIO[19:16] pin 0: Select normal pin 1: Select GPIO pin
GPIOI	11:8	R	The input data of GPIO[19:16]
GPIOO	7:4	RW	The output data of GPIO[19:16]
En_GPIO_ON	3:0	RW	Enable GPIO[19:16] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 7

Read/Write Port: 005Ch

Default Value: 000Fh

Field	Bits	Type	Description
-	15:12	RW	Reserved
DGPIOI	11:8	R	The input data of DGPIO[3:0]

DGPIOO	7:4	RW	The output data of DGPIO[3:0]
En_DGPIO_ON	3:0	RW	Enable DGPIO[3:0] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 8

Read/Write Port: 005Eh

Default Value: 000Fh

Field	Bits	Type	Description
-	15:12	RW	Reserved
DGPIOI	11:8	R	The input data of DGPIO[7:4]
DGPIOO	7:4	RW	The output data of DGPIO[7:4]
En_DGPIO_ON	3:0	RW	Enable DGPIO[7:4] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 9

Read/Write Port: 0060h

Default Value: 000Fh

Field	Bits	Type	Description
-	15:12	RW	Reserved
DGPIOI	11:8	R	The input data of DGPIO[11:8]
DGPIOO	7:4	RW	The output data of DGPIO[11:8]
En_DGPIO_ON	3:0	RW	Enable DGPIO[11:8] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General GPIO Register 10

Read/Write Port: 0062h

Default Value: 000Fh

Field	Bits	Type	Description
-	15:12	RW	Reserved
DGPIOI	11:8	R	The input data of DGPIO[15:12]

DGPIOO	7:4	RW	The output data of DGPIO[15:12]
En_DGPIO_ON	3:0	RW	Enable DGPIO[15:12] output mode, active low for each bit 0: Enable output mode 1: Disable output mode

General DFT Register 1

Read/Write Port: 0070h

Default Value: 0000h

Field	Bits	Type	Description
Debug_Sel	15:10	RW	Debug signal group selection for each module 000000: Group 0 001101: Group 1 …… 111111: Group 63
Probe_Sel	9:8	RW	Select 16-bit signals from 64-bit internal probe signals. 00: Select bit [15:0] from 64-bit internal probe signals 01: Select bit [31:16] from 64-bit internal probe signals 10: Select bit [47:32] from 64-bit internal probe signals 11: Select bit [63:48] from 64-bit internal probe signals When enable debug mode, these signals can be measured on the LCD pins: Bit0: LDCLK Bit1: LDE# Bit2: LD8 Bit3: LD9 Bit4: LD10 Bit5: LD11 Bit6: LD12 Bit7: LD13 Bit8: LD14 Bit9: LD15 Bit10: LD16 Bit11: LD17 Bit12: LCS1# Bit13: LSA0 Bit14: LSDA Bit15: LSCK

En_Debug_Mode	7	RW	Enable debug mode 0: Disable 1: Enable
En_Test_Fc_Rot	6	RW	Enable test function rotating automatically in debug mode 0: Disable 1: Enable
Test_Fc_Sel	5:2	RW	Test function selection in debug mode 0000: ProbeHost 0001: ProbeMem 0010: ProbeISP 0011: ProbeJPEG 0100: ProbeMPEG 0101: ProbeLCD 0110: ProbeMicroP0 0111: ProbeMicroP1 1000: ProbeCQ 1001: Probe2D 1010: Probe3D Others: ProbeMMC
-	1	-	Reserved
-	0	-	Reserved

General DFT Register 2

Read/Write Port: 0072h

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	Reserved
En_SRAMBIST	2	RW	Enable SRAM BIST 0: Disable 1: Enable
BIST_RstN	1	RW	Reset SRAM BIST 0: Normal operation 1: Reset
-	0	-	Reserved

General DFT Register 3

Read/Write Port: 0074h

Default Value: 0000h

Field	Bits	Type	Description

En_BISTALLDONE	15	R	SRAM BIST Test status
BISTDONE14	14	R	SRAM BIST14 Test status
BISTDONE13	13	R	SRAM BIST13 Test status
BISTDONE12	12	R	SRAM BIST12 Test status
BISTDONE11	11	R	SRAM BIST11 Test status
BISTDONE10	10	R	SRAM BIST10 Test status
BISTDONE9	9	R	SRAM BIST9 Test status
BISTDONE8	8	R	SRAM BIST8 Test status
BISTDONE7	7	R	SRAM BIST7 Test status
BISTDONE6	6	R	SRAM BIST6 Test status
BISTDONE5	5	R	SRAM BIST5 Test status
BISTDONE4	4	R	SRAM BIST4 Test status
BISTDONE3	3	R	SRAM BIST3 Test status
BISTDONE2	2	R	SRAM BIST2 Test status
BISTDONE1	1	R	SRAM BIST1 Test status
BISTDONE0	0	R	SRAM BIST0 Test status

General DFT Register 4

Read/Write Port: 0076h

Default Value: 0000h

Field	Bits	Type	Description
En_BISTALOAIL	15	R	SRAM BIST Test result

BISTFAIL14	14	R	SRAM BIST14 Test result
BISTFAIL13	13	R	SRAM BIST13 Test result
BISTFAIL12	12	R	SRAM BIST12 Test result
BISTFAIL11	11	R	SRAM BIST11 Test result
BISTFAIL10	10	R	SRAM BIST10 Test result
BISTFAIL9	9	R	SRAM BIST9 Test result
BISTFAIL8	8	R	SRAM BIST8 Test result
BISTFAIL7	7	R	SRAM BIST7 Test result
BISTFAIL6	6	R	SRAM BIST6 Test result
BISTFAIL5	5	R	SRAM BIST5 Test result
BISTFAIL4	4	R	SRAM BIST4 Test result
BISTFAIL3	3	R	SRAM BIST3 Test result
BISTFAIL2	2	R	SRAM BIST2 Test result
BISTFAIL1	1	R	SRAM BIST1 Test result
BISTFAIL0	0	R	SRAM BIST0 Test result

General PLL Register 5

Read/Write Port: 01E0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
Pll_PD	0	W	Power down PLL. Set the bit by setting write address = 0001E0h. Clear the bit by setting write address = 0001F0h. 0: Normal operation

			1: Power down

General PLL Register 6

Read/Write Port: 01F0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
Pll_PD	0	W	Power down PLL. Set the bit by setting write address = 0001E0h. Clear the bit by setting write address = 0001F0h. 0: Normal operation 1: Power down

10.3.2 Host Bus Controller Register

The following table define the Host Bus Controller registers name and its address.

Address	Name
0x0200h	Host Bus Controller Register 1
0x0202h	Host Bus Controller Register 2
0x0204h	Host Bus Controller Register 3
0x0206h	Host Bus Controller Register 4
0x0208h	Host Bus Controller Register 5
0x020Ah	Host Bus Controller Register 6
0x020Ch	Host Bus Controller Register 7
0x020Eh	Host Bus Controller Register 8
0x0210h	Host Bus Controller Register 9
0x0212h	Host Bus Controller Register 10
0x0214h	Host Bus Controller Register 11
0x0216h	Host Bus Controller Register 12
0x0218h	Host Bus Controller Register 13
0x02B0h	Host Bus Controller Register 14
0x02C0h	Host Bus Controller Register 15
0x02D0h	Host Bus Controller Register 16
0x02E0h	Host Bus Controller Register 17
0x02F0h	Host Bus Controller Register 18

Host Bus Controller Register 1

Read/Write Port: 0200h

Default Value: 0000h

Field	Bits	Type	Description
Bypass_LCD_Switch	15	RW	The control method to bypass LCD controller 0: Switch by address decoding (only for direct addressing mode) 1: Switch by GPIO8
Powerdown_PLL_Switch	14	RW	The control method to power down PLL 0: Switch by address decoding (only for direct addressing mode) 1: Switch by GPIO8
ISP_Commands_Select	13	RW	Image signal processor MMIO Write Selection 0: Write MMIO commands to ISP directly 1: Write MMIO commands to Command Queue
Sample_Cycle	12	RW	Asynchronous B.B Input signals asynchronous frequency transform sampling stage 0:no delay 1:delay 1 cycle
Host_IO_Drv	11:10	RW	Driving strength and resister setting for IO Buffer
CQ_Fire_Block	9	RW	Command Queue 0x1606h Fire blocking enable for SW can not polling to verify commands all writing to memory. 0: disable 1: enable
Int_Pol	8	RW	Interrupt polarity 0: Active low 1: Active high
RdCyc_Sample_Stage	7:6	RW	Input signals sampling stage when read cycle 00: no wait 01: wait 1 cycle 10: wait 2 cycles 11: wait 3 cycles
WrCyc_Sample_Stage	5:4	RW	Input signals sampling stage when write cycle 00: no wait 01: wait 1 cycle 10: wait 2 cycles 11: wait 3 cycles
	3	-	Reserved

Debug_Pin_Select	2:0	RW	7 sets debug signals

Host Bus Controller Register 2

Read/Write Port: 0202h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
En_3D_MMIO	10	RW	3D MMIO enable 0: Disable 1: Enable
En_2D_MMIO	9	RW	2D MMIO enable 0: Disable 1: Enable
En_OpenRISC_MMIO	8	RW	Reserved for Open RISC MMIO enable 0: Disable 1: Enable
En_CQ_MMIO	7	RW	Command queue MMIO enable 0: Disable 1: Enable
En_MicroP1_MMIO	6	RW	Micro processor #1 MMIO enable 0: Disable 1: Enable
En_MicroP0_MMIO	5	RW	Micro processor #0 MMIO enable 0: Disable 1: Enable
En_MMC_MMIO	4	RW	MMC MMIO enable 0: Disable 1: Enable
En_LCD_MMIO	3	RW	LCD MMIO enable 0: Disable 1: Enable
En_MPEG_MMIO	2	RW	MPEG MMIO enable 0: Disable 1: Enable
En_JPEG_MMIO	1	RW	JPEG MMIO enable 0: Disable 1: Enable

Host Bus Controller Register 3

Read/Write Port: 0204h

Default Value: 0000h

Field	Bits	Type	Description
Mem_Base	15:1	RW	Memory base address bit [15:1]. For direct addressing mode, it is the base address of linear frame buffer. The frame buffer size is up to 8 Mbytes.
-	0	-	Reserved

Host Bus Controller Register 4

Read/Write Port: 0206h

Default Value: 0080h

Field	Bits	Type	Description
-	15:7	-	Reserved
Mem_Base	7:0	RW	Memory base address bit [23:16]. For direct addressing mode, it is the base address of linear frame buffer. The frame buffer size is up to 8 Mbytes. For indirect addressing mode, it is the base address of one segment. Each segment size is 64 Kbytes.

Host Bus Controller Register 5

Read/Write Port: 0208h

Default Value: 0344h

Field	Bits	Type	Description
Burst_Length	15:14	RW	Burst length amount. For S-GOLD2 00: 1 word 01: 4 words 10: 8 words 11: continuous
-	13:10	-	Reserved
Wait_Ctrl	9	RW	Wait Control For S-GOLD2 0: Dynamic wait state evaluated at the same time when the data becomes invalid. 1: Dynamic wait state evaluated one cycle in advance before the data becomes invalid.
En_Access_MMIO	8	RW	Enable read MMIO space when pre-read memory mechanism is enabled. 0: disable 1: enable

Rd_Latency	7:4	RW	Read latency time For S-GOLD2 0000: 0 cycle 0001: 1 cycle …… 1110: 14 cycles 1111: 15 cycles
Wr_Latency	3:0	RW	Write latency time For S-GOLD2 0000: 0 cycle 0001: 1 cycle …… 1110: 14 cycles 1111: 15 cycles

Host Bus Controller Register 6

Read/Write Port: 020Ah

Default Value: 0600h

Field	Bits	Type	Description
-	15:12	-	Reserved
PreRd_DataBack_Amt {B0PRdBackAmt}	11:9	RW	As data was back up to this parameter, Re-Read Request (Tri-RE) will start till read back buffer full. Initial=”011” (4 words). 000: 1 word 001: 2 words ….. 111: 8 words
PreRdMem_Burst_Length {B0PRdBurstLength}	8:0	RW	Pre-Read memory burst length. We support 2~512 word read continuously. 00000000:disable 00000001:2 words 00000010:3 words …… 11111111:512 words

Host Bus Controller Register 7

Read/Write Port: 020Ch

Default Value: 0000h

Field	Bits	Type	Description
PreRdMem_Addr	15:1	RW	Pre-Read Memory address bit [15:1]. For direct addressing mode, it just keeps first for the followed

			020Eh address to start burst read. For indirect addressing mode, this field can be neglected.
-	0	-	Reserved

Host Bus Controller Register 8

Read/Write Port: 020Eh

Default Value: 0000h

Field	Bits	Type	Description
En_PreRd_Mem	15	W	Enable Pre-Read mechanism 0: disable 1: enable
-	14:7	-	Reserved
PreRdMem_Addr {B0PRdMemAddr}	6:0	RW	Pre-Read memory address bit [22:16]. When baseband command writes to this register, burst read memory mechanism will start by setting B0EnPRdMem

Host Bus Controller Register 9

Read/Write Port: 0210h

Default Value: 0000h

Field	Bits	Type	Description
MOCA_Base	15:1	RW	MOCA base address bit [15:1]. MOCA is addressing between 64KB and 128KB. Also it is programmable. Default Value: 0x010000(64KB)
-	0	-	Reserved

Host Bus Controller Register 10

Read/Write Port: 0212h

Default Value: 0001h

Field	Bits	Type	Description
-	15:8	-	Reserved
MOCA_Base	7:0	RW	MOCA base address bit [23:16].

Host Bus Controller Register 11

Read/Write Port: 0214h

Default Value: 0000h

Field	Bits	Type	Description
BB_Idle_Cnt {B0BBIdleCnt}	15:14	RW	BaseBand Idle cycles 00: 32 cycles

			01: 64 cycles 10: 128 cycles 11: 256 cycles
	13:8	-	Reserved
Wr_Mem_Acc_Lth {B0AccLength}	7:6	RW	Ready to Write memory FIFO when up to accumulation length 00: 1 word 01: 2 words 10: 4 words 11: 8 words
Wr_Mem_Acc_Dur {B0AccDur}	5:4	RW	Ready to write memory FIFO accumulation duration while not up to accumulation length 00: 1 cycle 01: 8 cycles 10: 16 cycles 11: 32 cycles

Host Bus Controller Register 12

Read/Write Port: 0216h

Default Value: 400Eh

Field	Bits	Type	Description
BIOWAITON _Delay {B0IOWAITONDly}	15:12	RW	delay cell JDLY4B08X4A control bits for BIOWAITON 0000: delay 0.5 ns 0001: delay 1.0 ns …… 1111: delay 8.0 ns
BEnIOWAITON _Delay {B0IOEnWAITONDly}	11:8	RW	delay cell JDLY4B08X4A control bits for BEnIOWAITON 0000: delay 0.5 ns 0001: delay 1.0 ns …… 1111: delay 8.0 ns
BEnIODON_Delay {B0IOEnDONDly}	7:0	RW	2 stages delay cell JDLY4B08X4A control bits for BEnIODON 00001110: delay 8.0ns 00001111: delay 8.5ns …… 11111111: delay 16.0 ns

Host Bus Controller Register 13

Read/Write Port: 0218h

Default Value: 0000h

Field	Bits	Type	Description
-	15:8	-	Reserved
Mem_Read_Empty	7	R	Memory read FIFO empty 0: not empty 1: empty
Mem_Write_Empty	6	R	Memory write FIFO empty 0: not empty 1: empty
Mem_Read_Back	5	R	Memory read back status 0: no return. 1: return.
Mem_Read_Full	4	R	Memory read FIFO full 0: not full 1: full
Mem_Write_Full	3	R	Memory write FIFO full 0: not full 1: full
MMIO_Read	2	R	MMIO read no ack 0: ack 1: no ack

Host Bus Controller Register 14

Read/Write Port: 02B0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
WriteMMIO_FIFO_Flush	0	W	When baseband write address = 02B0h, MMIO FIFO should flush all write commands before read except 0x0218h

Host Bus Controller Register 15

Read/Write Port: 02C0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
Wait_Polarity {B0WaitPol}	0	W	Wait Polarity. Set the bit by setting write address = 0002C0h. Clear the bit by setting write address = 0002D0h. 0: active low 1: active high

Host Bus Controller Register 16

Read/Write Port: 02D0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
Wait_Polarity	0	W	Wait Polarity. Set the bit 1 by setting write address = 0002C0h. Set the bit 0 by setting write address = 0002D0h. 0: active low 1: active high

Host Bus Controller Register 17

Read/Write Port: 02E0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
Bypass_LCD	0	W	Bypass LCD controller. Set the bit by setting write address = 0002E0h. Clear the bit by setting write address = 0002F0h. 0: Normal operation 1: Bypass LCD controller

Host Bus Controller Register 18

Read/Write Port: 02F0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
Bypass_LCD	0	W	Bypass LCD controller. Set the bit by setting write address = 0002E0h. Clear the bit by setting write address = 0002F0h. 0: Normal operation 1: Bypass LCD controller

10.3.3 Memory Controller Register

Reserved

10.3.4 LCD Controller Register

The following table define the LCD Controller registers name and its address.

Address	Name
0x1100h	Enable and Mode Setting Register 1
0x1102h	Enable and Mode Setting Register 2
0x1104h	Enable and Mode Setting Register 3
0x1106h	Display Width Register
0x1108h	Display Height Register
0x110Ah	Polarity Setting Register
0x110Ch	Display Base Address Register 1
0x110Eh	Display Base Address Register 2
0x1110h	Display Base Address Register 3
0x1112h	Display Base Address Register 4
0x1114h	Display Base Address Register 5
0x1116h	Display Base Address Register 6
0x1118h	Display Pitch Register
0x111Ch	Horizontal Total Register
0x1120h	Horizontal Retrace Start Register
0x1124h	Horizontal Retrace End Register
0x1128h	Horizontal Display Start Register
0x112Ch	Horizontal Display End Register
0x1130h	Vertical Total Register
0x1134h	Vertical Retrace Start Register
0x1138h	Vertical Retrace End Register
0x113Ch	Vertical Display Start Register
0x1140h	Vertical Display End Register
0x1144h	LCD POL Register
0x1146h	LCD Data Start Register
0x1148h	Frame Rate Control Register
0x114Ah	Data Command Header Register
0x114Ch	LCD SP Start Register
0x114Eh	LCD SP End Register
0x1150h	HW Cursor Base Address Register 1
0x1152h	HW Cursor Base Address Register 2
0x1154h	HW Cursor Pitch Register
0x1156h	HW Cursor X Size Register
0x1158h	HW Cursor Y Size Register
0x115Ah	HW Cursor X Position Register
0x115Ch	HW Cursor Y Position Register

0x115Eh	HW Cursor Preset Register
0x1160h	HW Cursor Foreground Color Register
0x1164h	HW Cursor Background Color Register
0x1168h	HW Cursor Destination Color Register
0x1180h	Status Register 1
0x1182h	Status Register 2
0x1184h	Status Register 3
0x1186h	Status Register 4
0x11A0h	Command Register 1
0x11A2h	Command Register 2
0x11B0h	Waveform Delay Control Register 1
0x11B2h	Waveform Delay Control Register 2
0x1200h	Gamma Correction Register
0x1210h	Gamma R Entry Register 1
0x1212h	Gamma R Entry Register 2
0x1214h	Gamma R Entry Register 3
0x1216h	Gamma R Entry Register 4
0x1218h	Gamma R Entry Register 5
0x1230h	Gamma G Entry Register 1
0x1232h	Gamma G Entry Register 2
0x1234h	Gamma G Entry Register 3
0x1236h	Gamma G Entry Register 4
0x1238h	Gamma G Entry Register 5
0x1250h	Gamma B Entry Register 1
0x1252h	Gamma B Entry Register 2
0x1254h	Gamma B Entry Register 3
0x1256h	Gamma B Entry Register 4
0x1258h	Gamma B Entry Register 5
0x1260h	SRAM Driving Register 1
0x1262h	SRAM Driving Register 2
0x1264h	SRAM Driving Register 3

Enable and Mode Setting Register 1

Read/Write Port: 1100h

Default Value: 0000h

Field	Bits	Type	Description
DGenRot	15	RW	Enable LCD display rotation mode 0 : Normal Display 1 : Rotation Enable(used with 1106h DGDRotMode[15:13])

DGenHwCurs	14	RW	Enable Hardware Cursor 0: Hardware Cursor Disable 1: Hardware Cursor Enable
DGenDither	13	RW	Enable dither function 0: RGB444 or RGB332 Dither Disable 1: RGB444 or RGB332 Dither Enable
DGenGamma	12	RW	Enable Gamma correction 0: Gamma Correction Disable 1: Gamma Correction Enable
DGenHsyncFlip	11	RW	Enable Hsync Flip 0: Vertical Retrace Flip (flip when current frame finish) 1: Horizontal Retrace Flip (flip when current line finish)
DGVsynPLTY	10	RW	Vsync or LCD IF : STV polarity 0: Vsync Low active 1: Vsync High active
DGHsynPLTY	9	RW	Hsync or LCD IF : STH polarity 0: Hsync Low active 1: Hsync High active
DGenBBcont	8	RW	Enable TVCLK in from IO 0: use self DCLK for LCD clock 1: use TVCLK from IO for LCD clock
DGenParDis	7	RW	Enable Partial Display 0: Partial Display Disable 1: Partial Display Enable
DGenHCurDefDst	6	RW	Enable Hardware Cursor use default Destination color For hardware cursor Destination color selection, we can use color from frame buffer or from default color(setting in 1168h DGHCuSDstColor) 0: Hardware cursor destination color from frame buffer 1: Hardware cursor destination color from 1168h DGHCuSDstColor
DGParDisMode	5	RW	Partial Display Mode We use hardware cursor size for partial display range, DGparDisMode define the out of the display range how the hardware do it. 0: Only send the partial display range to LCD 1: Send all the display range to LCD, but send RGB=0,0,0 to LCD when in the out of partial display range.
DGenSerCmdDirC	4	RW	Reserved

DGLCDSelct	3	RW	LCD selection 0: for LCD1 1: for LCD2
DGHWFlip	2	RW	Hardware flip Enable Hardware flip is used for 3D engine Software Flip is used for Video flip(used with 1102h DgenVideoFlip) and driver flip(driver can use 11a2h to change frame buffer) 0: Use software Flip 1: Hardware Flip Enable
DGPRTMode	1	RW	Partial Display PRT Mode In partial display mode, controller will generate a PRT signal for some special panel(sony 515), and DGPRTMode will cause PRT signal to cover Hsync and Vsync or just partial display range 1102h DGLSDAfromPTR and DGLDENfromPTR will decision which IO pin to output PRT signal. 0: include Hvsync and Vsync 1: no include Hvsync and Vsync
DGenPowSave	0	RW	CPU I/F Power Saving mode Enable When power saving mode is enabled, controller will not send the frame data, if the current frame is not changed. 1102h DGenSingleFr (if single frame buffer is used, controller will check if someone update frame buffer. If double buffer is used, controller will check if frame buffer number is updated.) 0: CPU I/F Power Saving mode disable 1: CPU I/F Power Saving mode Enable

Enable and Mode Setting Register 2

Read/Write Port: 1102h

Default Value: 0000h

Field	Bits	Type	Description
DgenVideoFlip	15	RW	Video Flip enable When DgenVideoFlip is enabled, controller will receive flip from ISP module to change frame buffer number. Otherwise, controller will use the same frame buffer with ISP. 0: Video Flip disable 1: Video Flip enable

DGLSDAfromPTR	14	RW	LSDA form PTR enable(used with 1100h DGPRTMode) Output PRT signal from LSDA(IO pin) 0: LSDA in normal mode 1: LSDA from PTR
DGLDENfromPTR	13	RW	LDEN form PTR enable(used with 1100h DGPRTMode) Output PRT signal from LDEN(IO pin) 0: LDEN in normal mode 1: LDEN from PTR
DGDHCLKoff	12	RW	Change to No DHCLK circuit for DHCLK off When CPU interface is used, controller needs DHCLK to generate CS and WR cycle. When RGB interface is used, controller can set DGDHCLKoff to 1, and close DHCLK 0: Normal case 1: Change to No DHCLK circuit , DHCLK can off
DGenStandBy	11	RW	Stand by and Partial Display Mode Enable Change controller to standby mode(controller read data from internal sram(data is wrote with 1260h 1262h)).(it can be turn on, only when controller is IDLE 1182h DGLCDIdle) 0: Normal Mode 1: Stand By Mode Enable
DGCS1PLTY[2:0]	10:8	RW	CPU Interface CS1 or LCD IF : XDON Polarity For setting CS1's polarity. When 000 or 001 is used, user can use 11b0 to adjust CS1's cycle. When 010 or 011 is used, CS1 cycle will be the DCLK' cycle. When 100 or 101 is used, user force CS1 to low or high. 000: CS1 Pulse width Low active (raising edge trigger) 001: CS1 Pulse width High active (falling edge trigger) 010: CS1 1T width Low active 011: CS1 1T width High active 100: CS1 force Low 101: CS1 force high
-	7	-	Reserved
DGenInvSerIn	6	RW	Serial Interface inverse data sequence Enable 0: MSB to LSB 1: LSB to MSB
DGenSingleFr	5	RW	single Frame Buffer Enable

			for setting frame buffer's number 0: Double Buffer or Triple buffer 1: Single buffer Enable
DGenFrCon	4	RW	Frame rate control Enable When using 3D engine, use DGenFrCon to enable frame rate control. (used with 1148h) 0: No Frame rate control 1: Frame rate control Enable
DGOutPosMode	3	RW	Output data position Mode when the output bits < The real bus width ex. Real bus width is D15~D0 0: align D15~D0 to MM365 pin LD15~LD0 1: align D15~D0 to MM365 pin LD17~LD2 0: Align LSB 1: Align MSB
DGNoUseBDef	2	RW	Output data No use bits default value When real bus width is D15 ~D0, 0: D17 and D16 will set to 0 1: D17 and D16 will set to 1 0: Output 0 for no use bits 1: Output 1 for no use bits
DGCmdPerdMode	1	RW	Data Command Period Mode For CPU interface, it will be added to the beginning of the frame. Used with 114Ah DGCmdHeader 0: One command per frame 1: One command per line
DGenCRC	0	RW	CRC Check Enable For debug and testing 0: No CRC Check 1: CRC Check Enable

Enable and Mode Setting Register 3

Read/Write Port: 1104h

Default Value: 0000h

Field	Bits	Type	Description
DGCsrcformat[1:0]	15:14	RW	LCD Color source Data Format

			00 : RGB565 01 : ARGB1555 10 : ARGB4444 11 : Reserved
-	13	-	Reserved
DGLCDDisMode[12:0]	12:0	RW	LCD Display mode setting 10 xxx xxxx xxxx : LCD interface 01 xxx xxxx xxxx : RGB Interface 00 xxx xxxx xxxx : CPU interface xx 000 xxxx xxxx : RGB 332 xx 001 xxxx xxxx : RGB 444 xx 010 xxxx xxxx : RGB 565 xx 011 xxxx xxxx : RGB 666 xx xxx 0000 xxxx : 6 bits interface xx xxx 0001 xxxx : 8 bits interface xx xxx 0010 xxxx : 9 bits interface xx xxx 0011 xxxx : 16 bits interface xx xxx 0100 xxxx : 18bits interface xx xxx xxxx 0000 : control Mode setting | xx xxx xxxx 1111 : control Mode setting CPU Interface Mode setting : 00 000 0001 0000 : CPU, RGB332, 8 bits, 1P1T(RGB) 00 001 0001 0000 : CPU, RGB444, 8 bits, 1P2T(XR_GB) 00 001 0001 0001 : CPU, RGB444, 8 bits, 1P2T(RX_GB) 00 001 0001 0010 : CPU, RGB444, 8 bits, 1P2T(RG_BX) 00 001 0001 0011 : CPU, RGB444, 8 bits, 1P2T(RG_XB) 00 001 0001 0100 : CPU, RGB444, 8 bits, 2P3T(RG_BR_GB) 00 010 0001 0000 : CPU, RGB565, 8 bits, 1P2T(RG3_G3B) 00 011 0001 0000 : CPU, RGB666, 8 bits, 1P3T(XR_XG_XB) 00 011 0001 0001 : CPU, RGB666, 8 bits, 1P3T(RX_GX_BX) 00 011 0010 0000 : CPU, RGB666, 9 bits, 1P2T(XG3_G3B) 00 000 0011 0000 : CPU, RGB332, 16 bits, 2P1T(RGBRGB) 00 001 0011 0000 : CPU, RGB444, 16 bits, 1P1T(XRGB) 00 001 0011 0001 : CPU, RGB444, 16 bits, 1P1T(RGBX) 00 010 0011 0000 : CPU, RGB565, 16 bits, 1P1T(RGB) 00 011 0011 0000 : CPU, RGB666, 16 bits, 2P3T(XRG_XBR_XGB)

			00 011 0011 0001 : CPU, RGB666, 16 bits, 2P3T(RGX_BRX_GBX) 00 000 0100 0000 : CPU, RGB332, 18 bits, 2P1T(XRGBRGB) 00 000 0100 0001 : CPU, RGB332, 18 bits, 2P1T(RGBRGBX) 00 001 0100 0000 : CPU, RGB444, 18 bits, 1P1T(XRGB) 00 001 0100 0001 : CPU, RGB444, 18 bits, 1P1T(RGBX) 00 010 0100 0000 : CPU, RGB565, 18 bits, 1P1T(XRGB) 00 010 0100 0001 : CPU, RGB565, 18 bits, 1P1T(RGBX) 00 011 0100 0000 : CPU, RGB666, 18 bits, 1P1T(RGB) RGB Interface Mode setting : 01 011 0000 0000 : RGB, RGB666, 6 bits, 1P3T(R_G_B) 01 011 0010 0000 : RGB, RGB666, 9 bits, 1P2T(RG3_G3B) 01 010 0011 0000 : RGB, RGB565, 16 bits, 1P1T(RGB) 01 011 0100 0000 : RGB, RGB666, 18 bits, 1P1T(RGB) LCD Interface Mode Setting : 10 010 0011 0000 : LCD, RGB565, 16 bits, 1P1T(RGB) 10 011 0100 0000 : LCD, RGB666, 18 bits, 1P1T(RGB)

Display Width Register

Read/Write Port: 1106h

Default Value: 0000h

Field	Bits	Type	Description
DGDRotMode[2:0]	15:13	RW	LCD Rotation display Mode (rotation is active only when 1100h DGenRot is enabled 000 : No Rotation 001 : 180 010 : Mirror 011 : Flip 100 : 90 101 : -90 others : Reserved
-	12:10	-	Reserved
DGDisWidth[9:0]	9:0	RW	LCD display width

Display Height Register

Read/Write Port: 1108h

Default Value: 0000h

Field	Bits	Type	Description
DGDCPUType[1:0]	15:14	RW	LCD CPU Type for CPU Interface 0x: 80 Type CPU 10: 68 Type CPR with CS latch data 11: 68 Type CPR with RW latch data
-	12:10	-	Reserved
DGDisHeigh	9:0	RW	LCD display Height

Polarity Setting Register

Read/Write Port: 110Ah

Default Value: 0000h

Field	Bits	Type	Description
DGDEnOLTY	15:14	RW	RGB Interface Deable or LCD IF : LD Polarity DE for RGB interface 00: DEnable Low active 01: DEnable High active 10: DEnable Force Low 11: DEnable Force High
DGXRESPLTY	13:12	RW	CPU Interface XRES or LCD IF : FG Polarity For CPU interface to infer the current access is command or data using RS(MM365 LHsync pin). 00: low is for data 01: high is for data 10: Force RS(MM365 LHsync pin) Low 11: Force RS(MM365 LHsync pin) High
DGDCLKPLTY	11	RW	RGB Interface DCLK or LCD IF : FS Polarity 0: DCLK Rising Edge Latch data 1: DCLK Falling Edge Latch data
DGCS0PLTY	10:8	RW	CPU Interface CS0 or LCD IF : XDOFF Polarity For setting CS0's polarity. When 000 or 001 is used, user can use 11b0 to adjust CS0's cycle. When 010 or 011 is used, CS0 cycle will be the DCLK' cycle. When 100 or 101 is used, user force CS0 to low or high. 000: CS0 Pulse width Low active (raising edge trigger) 001: CS0 Pulse width High active (falling edge trigger)

			010: CS0 1T width Low active 011: CS0 1T width High active 100: CS0 force Low 101: CS0 force high
DGA0PLTY	7	RW	RGB Serial Interface A0 or LCD IF : SP Polarity For serial interface to infer the current access is command or data 0: A0 Low for data 1: A0 high for data
DGRWPLTY	6:4	RW	CPU Interface RW Polarity For setting WR's polarity. When 000 or 001 is used, user can use 11b2 to adjust WR's cycle. When 010 or 011 is used, WR cycle will be the DCLK' cycle. When 100 or 101 is used, user force WR to low or high. 000: RW Pulse width Low active (raising edge trigger) 001: RW Pulse width High active (falling edge trigger) 010: RW 1T width Low active 011: RW 1T width High active 100: RW force Low 101: RW force high
DGSerialDType	3:2	RW	Serial Interface Data Type 00: 8 bits Data 01: 9 bits Data 10: 24 bits Data 11: Reserved
DGSCLKPLTY	1	RW	RGB Interface SCLK Polarity For serial interface SCLK's polarity 0: SCLK Rising Edge Latch data 1: SCLK Falling Edge Latch data
-	0	-	Reserved

Display A Base Address Register 1

Read/Write Port: 110Ch

Default Value: 0000h

Field	Bits	Type	Description
DGDBASA	15:0	RW	Display A Base Address [15:0] (Bit 0 should always equal to 0)

Display A Base Address Register 2

Read/Write Port: 110Eh

Default Value: 0000h

Field	Bits	Type	Description
DGReqThrehd	15:14	RW	SRAM Request threshold (FIFO remain length). To adjust Controller's behavior about accessing memory. It can tune memory access performance 00 : remain 1 stage and then Request 01 : remain 2 stage and then Request 10 : remain 4 stage and then Request 11 : remain 8 stage and then Request
-	13:7	-	Reserved
DGDBASA	6:0	RW	Display A Base Address [22:16]

Display B Base Address Register 1

Read/Write Port: 1110h

Default Value: 0000h

Field	Bits	Type	Description
DGDBASB	15:0	RW	Display B Base Address [15:0] (Bit 0 should always equal to 0)

Display B Base Address Register 2

Read/Write Port: 1112h

Default Value: 0000h

Field	Bits	Type	Description
-	15:7	-	Reserved
DGDBASB	6:0	RW	Display B Base Address [22:16]

Display C Base Address Register 1

Read/Write Port: 1114h

Default Value: 0000h

Field	Bits	Type	Description
DGDBASC	15:0	RW	Display C Base Address [15:0] (Bit 0 should always equal to 0)

Display C Base Address Register 2

Read/Write Port: 1116h

Default Value: 0000h

Field	Bits	Type	Description
-	15:7	-	Reserved
DGDBASC	6:0	RW	Display C Base Address [22:16]

Display Pitch Register

Read/Write Port: 1118h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
DGDPITCH	10:0	-	Display pitch [10:0] (Bit 0 should always equal to 0)

Reserved Register

Read/Write Port: 111Ah

Default Value: 0000h

Horizontal Total Register

Read/Write Port: 111Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHTotal	9:0	RW	Display Horizontal Total [9:0] For RGB interface, Hsync total period.

Reserved Register

Read/Write Port: 111Eh

Default Value: 0000h

Horizontal Retrace Start Register

Read/Write Port: 1120h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHRst	9:0	RW	Display Horizontal Retrace or STH Start [9:0] For RGB interface, Hsync Retrace starts.

Reserved Register

Read/Write Port: 1122h

Default Value: 0000h

Horizontal Retrace End Register

Read/Write Port: 1124h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHRend	9:0	RW	Display Horizontal Retrace or STH End [9:0] For RGB interface, Hsync Retrace End

Reserved Register

Read/Write Port: 1126h

Default Value: 0000h

Horizontal Display Start Register

Read/Write Port: 1128h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHDRst	9:0	RW	Display Horizontal Display or LD Start [9:0] For RGB interface, Hsync Data valid start.

Reserved Register

Read/Write Port: 112Ah

Default Value: 0000h

Horizontal Display End Register

Read/Write Port: 112Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHDRend	9:0	RW	Display Horizontal Display or LD End [9:0] For RGB interface, Hsync Data valid End

Reserved Register

Read/Write Port: 112Eh

Default Value: 0000h

Vertical Total Register

Read/Write Port: 1130h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGVTotal	9:0	RW	Display Vertical Total [9:0] For RGB interface, Vsync total period

Reserved Register

Read/Write Port: 1132h

Default Value: 0000h

Vertical Retrace Start Register

Read/Write Port: 1134h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGVRst	9:0	RW	Display Vertical Retrace or STV Start [9:0] For RGB interface, Vsync retrace start

Reserved Register

Read/Write Port: 1136h

Default Value: 0000h

Vertical Retrace End Register

Read/Write Port: 1138h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGVRend	9:0	RW	Display Vertical Retrace or STV End [9:0] For RGB interface, Vsync retrace end

Reserved Register

Read/Write Port: 113Ah

Default Value: 0000h

Vertical Display Start Register

Read/Write Port: 113Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGVDRst	9:0	RW	Display Vertical Display or FG Start [9:0] For RGB interface, Vsync valid line start

Reserved Register

Read/Write Port: 113Eh

Default Value: 0000h

Vertical Display End Register

Read/Write Port: 1140h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGVDRend	9:0	RW	Display Vertical Display or FG End [9:0] For RGB interface, Vsync valid line end

Reserved Register

Read/Write Port: 1142h

Default Value: 0000h

LCD POL Register

Read/Write Port: 1144h

Default Value: 0000h

Field	Bits	Type	Description
DGXONWFr	15:12	RW	LCD Interface: The Waiting frame number for Display ON
-	11:9	-	Reserved
DGPOLst	8:0	RW	LCD Interface POL start [8:0]

LCD Data Start Register

Read/Write Port: 1146h

Default Value: 0000h

Field	Bits	Type	Description
DGXOFFWFr	15:12	RW	LCD Interface: The Waiting frame number for Display Off

-	11:9	-	Reserved
DGDATAst	8:0	RW	LCD Interface Data start [8:0]

Frame Rate Control Register

Read/Write Port: 1148h

Default Value: 0000h

Field	Bits	Type	Description
DGFrRate	15:9	RW	LCD Frame rate For 3D engine frame rate control
DGFrConCnt	8:0	RW	LCD Frame rate control counter [8:0] counter unit : 8 lines For 3D engine frame rate control

Data Command Header Register

Read/Write Port: 114Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
DGCmdHeader	8:0	RW	Data Command Header [8:0] For CPU interface, it will be added to the beginning of the frame. 8 or 9 bits depends on input command

LCD SP Start Register

Read/Write Port: 114Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
DGSPst	8:0	RW	LCD Interface SP start [8:0]

LCD SP End Register

Read/Write Port: 114Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
DGSPst	8:0	RW	LCD Interface SP End [8:0]

HW Cursor Base Address Register 1

Read/Write Port: 1150h

Default Value: 0000h

Field	Bits	Type	Description
DGHCuSBAS	15:0	-	Hardware Cursor Base Address [15:0] Bit 0 should always equal to 0

HW Cursor Base Address Register 2

Read/Write Port: 1152h

Default Value: 0000h

Field	Bits	Type	Description
DGDebugSel	15:13	RW	Debug signal Selection For debug
-	12:7	-	Reserved
DGHCuSBAS	6:0	RW	Hardware Cursor Base Address [22:16]

HW Cursor Pitch Register

Read/Write Port: 1154h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
DGHCuSPitch	10:0	-	Hardware cursor pitch [10:0] (Bit 0 should always equal to 0)

HW Cursor X Size Register

Read/Write Port: 1156h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHCuSXsize	9:0	-	Hardware cursor X size [9:0]

HW Cursor Y Size Register

Read/Write Port: 1158h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHCuSYsize	9:0	-	Hardware cursor Y size [9:0]

			Reference to above Hardware Cursor introduction

HW Cursor X Position Register

Read/Write Port: 115Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHCuSXpos	9:0	-	Hardware cursor X position [9:0] Reference to above Hardware Cursor introduction

HW Cursor Y Position Register

Read/Write Port: 115Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
DGHCuSYpos	9:0	-	Hardware cursor Y position [9:0] Reference to above Hardware Cursor introduction

HW Cursor Preset Register

Read/Write Port: 115Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGHCuSXpreset	12:8	RW	Hardware cursor X preset [4:0] Reference to above Hardware Cursor introduction
-	7:5	-	Reserved
DGHCuSYpreset	4:0	RW	Hardware cursor Y preset [4:0] Reference to above Hardware Cursor introduction

HW Cursor Foreground Color Register

Read/Write Port: 1160h

Default Value: 0000h

Field	Bits	Type	Description
DGHCuSFColor	15:0	RW	Hardware cursor foreground Color, RGB565 When using hardware cursor, controller will use DGHCuSFColor as output pixel color when Hardware Cursor data is 01

Reserved Register

Read/Write Port: 1162h

Default Value: 0000h

HW Cursor Background Color Register

Read/Write Port: 1164h

Default Value: 0000h

Field	Bits	Type	Description
DGHCuSBackColor	15:0	RW	Hardware cursor background Color, RGB565 When using hardware cursor, controller will use DGHCuSBackColor as output pixel color when Hardware Cursor data is 00

Reserved Register

Read/Write Port: 1166h

Default Value: 0000h

HW Cursor Destination Color Register

Read/Write Port: 1168h

Default Value: 0000h

Field	Bits	Type	Description
DGHCuSDstColor	15:0	RW	Hardware cursor default destination Color,RGB565 When using hardware cursor and 1100h DGenHCurDefDst is enabled, controller will use DGHCuSDstColor as output pixel color when Hardware Cursor data is 10

Reserved Register

Read/Write Port: 116Ah ~ 117Fh

Default Value: 0000h

Status Register 1

Read/Write Port: 1180h

Default Value: 0000h

Field	Bits	Type	Description
DGCMdQempty	15	R	Command queue Empty For checking if command sent to controller is finished. 0 : Not Empty 1 : Empty

DGCMDMode	14	R	Command Mode Read Back It can send command to LCD panel only when controller is in command mode
DGFlipCnt	13:12	R	Display Flip Counter [1:0] It infers which frame buffer is displayed by controller.
-	11:9	-	Reserved
DGHCnt	8:0	R	Display Horizontal Counter [8:0] It infers which Horizontal pixel is displayed

Status Register 2

Read/Write Port: 1182h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGLCDIdle	12	R	LCD Idle
-	11:9	-	Reserved
DGVCnt	8:0	R	Display Vertical counter [8:0] It infers which line is displayed

Status Register 3

Read/Write Port: 1184h

Default Value: 0000h

Field	Bits	Type	Description
-	15	-	Reserved
DGFrDataCRCflag	14:8	R	Frame data CRC check flag [6:0] For debug and testing.
-	7	-	Reserved
DGHSDataCRCflag	6:0	R	Hardware cursor data CRC check flag [6:0] For debug and testing.

Status Register 4

Read/Write Port: 1186h

Default Value: 0000h

Field	Bits	Type	Description
-	15:7	-	Reserved
DGOutDataCRCflag	6:0	R	Output data CRC check flag [6:0] For debug and testing.

Reserved Register

Read/Write Port: 1188h ~ 119Fh

Default Value: 0000h

Command Register 1

Read/Write Port: 11A0h

Default Value: 0000h

Field	Bits	Type	Description
EGComdType	15:14	RW	Command Type 00: LCD display fire & command fire 01: Parallel command mode 10: Serial command mode 10: Serial command direct control mode
DGComdPos	13:12	RW	Command Position 00: first Bytes 01: 2nd Bytes 10: 3rd Bytes 11: Reserved
DGComdFire	11	RW	Command Fire 0: Command No fire 1: Command Fire (Start send to LCD)
DGComdEnable	10	RW	Command Enable Indicate current access is command or data. 0: indicate the data is Non command 1: indicate the data is command
DGComdDW	9	RW	Command Data Width 0: Data width is 8 Bits 1: Data width is 9 Bits
DGComdData	8:0	RW	Command Data [8:0]

Command Register 2

Read/Write Port: 11A2h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
EGSWFlipMode	4	RW	Sofware Flip Mode When user flip frame buffer, if EGSWFlipMode is set to 1,

			controller will change to the buffer without care the current frame is finish or not. If EGSWFlipMode is set to 0, controller will check 1100h DGHsynPLTY to decide wait line finish or frame finish. 0 : wait Sync (Vsync or Hsync) 1 : No wait sync (Vsync or Hsync)
-	3:2	-	Reserved
EGSWFlipNum	1:0	RW	Sofware Flip Number User can use EGSWFlipNum to ask controller to change to the frame buffer. 00 : Surface A 01 : Surface B 10 : Surface C 11 : Reserved

Reserved Register

Read/Write Port: 11A4h ~ 11AFh

Default Value: 0000h

Waveform Delay Control Register 1

Read/Write Port: 11B0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:14	-	Reserved
DGCSStCnt	13:8	RW	CS waveform programming : Start counter [5:0] Adjust CS's cycle.
-	7:6	-	Reserved
DGCSEndCnt	5:0	RW	CS waveform programming : End counter [5:0] Adjust CS's cycle.

Waveform Delay Control Register 2

Read/Write Port: 11B2h

Default Value: 0000h

Field	Bits	Type	Description
-	15:14	-	Reserved
DGRWStCnt	13:8	RW	RW waveform programming : Start counter [5:0] Adjust WR's cycle.
-	7:6	-	Reserved

DGRWEndCnt	5:0	RW	RW waveform programming : End counter [5:0] Adjust WR's cycle.

Reserved Register

Read/Write Port: 11B4h ~ 11FFh

Default Value: 0000h

Gamma Correction Register

Read/Write Port: 1200h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
DGGamBVrang	5:4	RW	Gamma correction : B channel Range 00 : B channel gamma value > 1 01 : B channel gamma value = 1 10 : B channel gamma value < 1 11 : Reserved
DGGamGVrang	3:2	RW	Gamma correction : G channel Range 00 : G channel gamma value > 1 01 : G channel gamma value = 1 10 : G channel gamma value < 1 11 : Reserved
DGGamRVrang	1:0	RW	Gamma correction : R channel Range 00 : R channel gamma value > 1 01 : R channel gamma value = 1 10 : R channel gamma value < 1 11 : Reserved

Reserved Register

Read/Write Port: 1202h ~ 120Fh

Default Value: 0000h

Gamma R Entry Register 1

Read/Write Port: 1210h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamR1Entry	12:8	RW	R channel Gamma value [4:0] for Entry1

-	7:5	-	Reserved
DGGamR0Entry	4:0	RW	R channel Gamma value [4:0] for Entry0

Gamma R Entry Register 2

Read/Write Port: 1212h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamR3Entry	12:8	RW	R channel Gamma value [4:0] for Entry3
-	7:5	-	Reserved
DGGamR2Entry	4:0	RW	R channel Gamma value [4:0] for Entry2

Gamma R Entry Register 3

Read/Write Port: 1214h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamR5Entry	12:8	RW	R channel Gamma value [4:0] for Entry5
-	7:5	-	Reserved
DGGamR4Entry	4:0	RW	R channel Gamma value [4:0] for Entry4

Gamma R Entry Register 4

Read/Write Port: 1216h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamR7Entry	12:8	RW	R channel Gamma value [4:0] for Entry7
-	7:5	-	Reserved
DGGamR6Entry	4:0	RW	R channel Gamma value [4:0] for Entry6

Gamma R Entry Register 5

Read/Write Port: 1218h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved

DGGamR8Entry	4:0	RW	R channel Gamma value [4:0] for Entry8

Reserved Register

Read/Write Port: 121Ah ~ 122Fh

Default Value: 0000h

Gamma G Entry Register 1

Read/Write Port: 1230h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamG1Entry	12:8	RW	G channel Gamma value [4:0] for Entry1
-	7:5	-	Reserved
DGGamG0Entry	4:0	RW	G channel Gamma value [4:0] for Entry0

Gamma G Entry Register 2

Read/Write Port: 1232h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamG3Entry	12:8	RW	G channel Gamma value [4:0] for Entry3
-	7:5	-	Reserved
DGGamG2Entry	4:0	RW	G channel Gamma value [4:0] for Entry2

Gamma G Entry Register 3

Read/Write Port: 1234h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamG5Entry	12:8	RW	G channel Gamma value [4:0] for Entry5
-	7:5	-	Reserved
DGGamG4Entry	4:0	RW	G channel Gamma value [4:0] for Entry4

Gamma G Entry Register 4

Read/Write Port: 1236h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamG7Entry	12:8	RW	G channel Gamma value [4:0] for Entry7
-	7:5	-	Reserved
DGGamG6Entry	4:0	RW	G channel Gamma value [4:0] for Entry6

Gamma G Entry Register 5

Read/Write Port: 1238h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
DGGamG8Entry	4:0	RW	G channel Gamma value [4:0] for Entry8

Reserved Register

Read/Write Port: 123Ah ~ 124Fh

Default Value: 0000h

Gamma B Entry Register 1

Read/Write Port: 1250h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamB1Entry	12:8	RW	B channel Gamma value [4:0] for Entry1
-	7:5	-	Reserved
DGGamB0Entry	4:0	RW	B channel Gamma value [4:0] for Entry0

Gamma B Entry Register 2

Read/Write Port: 1252h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamB3Entry	12:8	RW	B channel Gamma value [4:0] for Entry3
-	7:5	-	Reserved
DGGamB2Entry	4:0	RW	B channel Gamma value [4:0] for Entry2

Gamma B Entry Register 3

Read/Write Port: 1254h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamB5Entry	12:8	RW	B channel Gamma value [4:0] for Entry5
-	7:5	-	Reserved
DGGamB4Entry	4:0	RW	B channel Gamma value [4:0] for Entry4

Gamma B Entry Register 4

Read/Write Port: 1256h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
DGGamB7Entry	12:8	RW	B channel Gamma value [4:0] for Entry7
-	7:5	-	Reserved
DGGamB6Entry	4:0	RW	B channel Gamma value [4:0] for Entry6

Gamma B Entry Register 5

Read/Write Port: 1258h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
DGGamB8Entry	4:0	RW	B channel Gamma value [4:0] for Entry8

Reserved Register

Read/Write Port: 125Ah ~ 125Fh

Default Value: 0000h

SRAM Driving Register 1

Read/Write Port: 1260h

Default Value: 0000h

Field	Bits	Type	Description
DGRFAddrMode	15:14	RW	RF Write Address Mode When standby mode is enabled, user can use host to write controller's internal sram to fill display data. DGRFAddrMode will set the display size. 00 : 256 x 32

			01 : 128 x 64 10 : 64 x 128 11 : 32 x 256
BOLCDIODrv	13:12	RW	LCD IO Driver strength 00 : default 01 : x 2 10 : x 4 11 : x 8
-	11:8	-	Reserved
DGRFXpos	7:0	RW	RF Write Address [7:0] : X Position The position X that user wants to fill data.

SRAM Driving Register 2

Read/Write Port: 1262h

Default Value: 0000h

Field	Bits	Type	Description
-	15:8	-	Reserved
DGRFYpos	7:0	RW	RF Write Address [7:0] : Y Position The position Y that user want to fill data.

SRAM Driving Register 3

Read/Write Port: 1264h

Default Value: 0000h

Field	Bits	Type	Description
DGRFData	15:0	RW	RF Write Address [15:0] : Data The data that user want to fill in DGRFXpos and DGRFYpos.

10.3.5 MMC/SD Controller Register

Command Format Register 1

(1404h 1402h 1400h is the MMC command format 48bits)

Read/Write Port: 1400h

Default Value: 0000h

Field	Bits	Type	Description
MCGCmdArg	15:8	RW	Command format : Command argument[7:0]
MCGCmdCRC	7:1	RW	Command format : Command CRC[6:0]
MCGCmdEndbit	0	RW	Command format : Command End bit

Command Format Register 2

Read/Write Port: 1402h

Default Value: 0000h

Field	Bits	Type	Description
MCGCmdArg	15:0	RW	Command format : Command argument[23:8]

Command Format Register 3

Read/Write Port: 1404h

Default Value: 0000h

Field	Bits	Type	Description
MCGCmdStBit	15	RW	Command format : start bit
MCGCmdTransBit	14	RW	Command format : transmission bit
MCGCmdIndex	13:8	RW	Command format : Command Index [5:0]
MCGCmdArg	7:0	RW	Command format : Command argument[31:24]

Command Fire Register

When controller receive this register, controller will send 1404 1402 1400(48 bits) to MMC card and according the setting in 1406h to decide whether receive, send data or wait response.

Read/Write Port: 1406h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
MCGCmdCnt	12	RW	MMC Command Counter To set the label of the command. When the controller finish the command 1420h MCGRBSCmdCnt will be changed to this label, and user will understand the command is finished.
-	11	-	Reserved
MCGCmdResType	10:8	RW	MMC Command Response Type The response type is the same with MMC's protocol 000: R1 001: R1b 010: R2 011: R3 100: R4

			101: R5
MCGCmdType	7:6	RW	MMC Command Type 00: Broadcast commands, no response 01: Broadcast command, with response 10 : Addressed command no data transfer on DAT 11: Addressed command with data transfer on DAT
-	5:4	-	Reserved
MCGCmdClass	3:0	RW	MMC Command Class 0000: Stream Read 0001: Single Block Read 0010: Multiple Block Read with STOP 0011: Multiple Block Read No STOP 0100: **Reserved** for Stream Write 0101: Single Block Write 0110: **Reserved** for Multiple Block Write with STOP 0111: Multiple Block Write No STOP 1000: STOP Command 1001: Cancel On Running Command 1010: Basic Command

Reserved Register

Read/Write Port: 1408h ~ 140Fh

Default Value: 0000h

Command Response Register

Read/Write Port: 1410h ~ 141Fh

Default Value: 0000h

For R2

Field	Bits	Type	Description
MCGCRCID	127:1	RW	MMC Command Response CID or CSD
MCGCREndBit	0		MMC Command Response End Bit

For R1, R3, R4, R5

Field	Bits	Type	Description
MCGCRCID	127:48	RW	Reserved
MCGCRStBit	47		MMC Command Response Start Bit
MCGCRTransBit	46		MMC Command Response Transmission Bit

MCGCRCmdIndex	45:40		MMC Command Response Command Index [5:0]
MCGCRStatus	39:8		MMC Command Response Status [31:0]
MCGCRCRC	7:1		MMC Command Response CRC [6:0]
MCGCREndBit	0		MMC Command Response End Bit

Read Back Status Register 1

Read/Write Port: 1420h

Default Value: 0000h

Field	Bits	Type	Description
MCGRBSCmdCnt	15	R	MMC Read Back Status Command Counter
MCGRBSMCIdle	14	R	MMC Read Back StatusMMC Idle
-	13:10	R	Reserved
MCGRBSCmdRRdy	9	R	MMC Read Back Status Response Ready 0 : Command Response Not Ready 1 : Command Response Ready
MCGRBSDATRdy	8	R	MMC Read Back Status Data Ready 0 : Data Not Ready 1 : Data Ready
-	7:6	-	Reserved
MCGRBSNoResTout	5	R	MMC Read Back Status No Response Time Out 0 : No any No Response Time out Error 1 : No Response Time out Error
MCGRBSNoDATTout	4	R	MMC Read Back Status No Data Time Out 0 : No any No Data Time out Error 1 : No Data Time out Error
-	3	-	Reserved
MCGRBSWrCRCErr	2	R	MMC Read Back Status Block Write CRC Error 0 : No any Block Write CRC check Error 1 : Block Write CRC check Error
MCGRBSRdCRCErr	1	R	MMC Read Back Status Block Read CRC Error 0 : No any Block Read CRC check Error 1 : Block Read CRC check Error
MCGRBSAlgnErr	0	R	MMC Read Back Status Stream Read No Byte alignment Error) Now is no used. 0 : No any Byte Align Error 1 : Stream Read byte Align Error

Read Back Status Register 2

Read/Write Port: 1422h

Default Value: 0000h

Field	Bits	Type	Description
MCGRBSBlkCnt	15:0	R	MMC R/W Finish Data Block Counter [15:0]

Read Back Status Register 3

Read/Write Port: 1424h

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
MCGRBSBlkLen	11:0	R	MMC R/W Finish Data Block Length [11:0]

Reserved Register

Read/Write Port: 1426h ~ 142Fh

Default Value: 0000h

MMC Basic Register

Read/Write Port: 1430h

Default Value: 0000h

Field	Bits	Type	Description
MCGTCLKNStrobeDly	15:8	RW	TCLK delay. Two delay cells compose the delay chain. The delay cells are controlled by bit [11:8] and [15:12] separately. Each delay cell is: 0000: delay 0.5 ns 0001: delay 1.0 ns …… 1111: delay 8.0 ns
MCGIODrv	7:6	RW	MMC IO driving strength 00: minimum strength 01: low strength 10: high strength 11: maximum strength
MCGCMD75k	5	RW	MMC CMD Pull high enable

			0: CMD No 75k pull high 1: CMD 75k pull high
MCGDAT75k	4	RW	MMC DAT0~3 Pull high enable 0: DAT0~3 No 75k pull high 1: DAT0~3 75k pull high
MCGen4BitBus	3	RW	MMC 4 bits bus enable 0 : disable 1: enable
MCGenPushPull	2	RW	Used to enable MMC stop clock when MMC is waiting for memory access and can not receive data or send data 0 : disable 1 : enable
MCGenIntRupCon	1	RW	MMC enable Interrupt Control When MMC controller finish data access, MMC controller will pull up the interrupt. 0 : MMC disable Interrupt control 1 : MMC Enable Interrupt control
MCGdisCRC	0	RW	MMC disable CRC check 0 : MMC enable CRC check 1 : MMC disable CRC check

Reserved Register

Read/Write Port: 1432h

Default Value: 0000h

Data Read Base Address Register 1

Read/Write Port: 1434h

Default Value: 0000h

Field	Bits	Type	Description
MCGRdBAS	15:0	RW	Data Read Base Address [15:0] (Bit 0 should always equal to 0)

Data Read Base Address Register 2

Read/Write Port: 1436h

Default Value: 0000h

Field	Bits	Type	Description

-	15:7	-	Reserved
MCGRdBAS	6:0	RW	Data Read Base Address [22:16]

Data Write Base Address Register 1

Read/Write Port: 1438h

Default Value: 0000h

Field	Bits	Type	Description
MCGWrBAS	15:0	RW	Data Write Base Address [15:0] (Bit 0 should always equal to 0)

Data Write Base Address Register 2

Read/Write Port: 143Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:7	-	Reserved
MCGWrBAS	6:0	RW	Data Write Base Address [22:16]

Data Block Counter Register

Read/Write Port: 143Ch

Default Value: 0000h

Field	Bits	Type	Description
MCGRWBlkCnt	15:0	RW	MMC R/W Data Block Counter

Data Block Length Register

Read/Write Port: 143Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
MCGRWBlkLen	11:0	RW	MMC R/W Data Block Length

MMC Time Out Counter Register

Read/Write Port: 1440h

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
MCGTimoutCnt	11:0	RW	MMC Time out Counter [11:0] MMC Time out Counter = MCGTimoutCnt x 16 MMCLK

10.3.6 Video Capture Register

Capture Testing Register

Read/Write Port: 0400h

Default Value: 0000h

Field	Bits	Type	Description
CGPixDataSize	15:8	R/W	Test data size for n x n (255x255) max.
CGTestMode	7:6	R/W	Test mode for fix data in.
CGTestDataIn	5	R/W	Test mode enables.
CGMWrBufLV	4:0	R/W	Write buffer efficiency setting

Capture Enable Register 1

Read/Write Port: 0402h

Default Value: 0000h

Field	Bits	Type	Description
CGBay10Bin	15	R/W	Enable 10 bits raw data in.
CGEnPreviewTurbo	14	R/W	Preview turbo mode enables. Generally, Capture and ISP module will delay 1 frame. When this bit enable, Capture and ISP module will process the same frame with delay some scan lines. It will improve the delay time between real image and LCD display.
CGBlkENB	13	R/W	Enable black level compensation. 0: Disable 1: Enable
CGSticENB	12	R/W	Enable statistic. 0: Disable 1: Enable
Reserved	11:10	-	Reserved
CGBlkNumPower	9:5	R/W	Power 2 number for black pixel sum. .
CGNumPower	4:0	R/W	Power 2 number for statistic image sum.

Note: HW circuit sum all the black pixels value and image pixels value with 27bits counter. Capture module shift left CGBlkNumPower bits for black pixels sum and send 8bits of the result to uP for further average calculation. Capture module shift left CGNumPower bits for image pixels sum and send 8bits of the result to uP for further average calculation.

Capture Enable Register 2

Read/Write Port: 0404h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:14	-	Reserved
CGShadENB	13	R/W	Enable Shading correction. 0: Disable 1: Enable
CGGamENB	12	R/W	Enable Gamma correction 0: Disable 1: Enable
CGBadPixENB	11	RW	Enable Bad pixel compenstation. 0: Disable 1: Enable
CGRotate	10	RW	Enable frame rotate write to memory with 180 degree 0: Disable 1: Enable
CGFlashENB	9	RW	Enable flashlight signal. 0: Disable 1: Enable
CGSnapShot	8	R/W	Snapshot mode or preview mode. 0: Preview 1: Snapshot
CGFlashFrmCunt	7:4	R/W	Frame count after CGSnapShot bit set. After this frame count, flashlight counter of 0x4A6 and 0x4A8 register begin to work.
CGSnapFrmCunt	3:0	R/W	Frame count after CGSnapShot bit set After this frane count, capture module enable frame snapshot.

Capture Enable Register 3

Read/Write Port: 0406h

Default Value: 0000h

Field	Bits	Type	Description
CGRunJudgeSelW	15	RW	Enable frame window (frame size of sensor output is non-change) and registers synchronize for continue digital zoom in.
Reserved	14	-	Reserved
ENCSLKENSCLKON	13	RW	Enable output tri-state of SCLK, CSCL and COEN
CGYUVTransf	12	RW	Enable UV component of YUV input transfer the range from -128~127 to the range 0~255. 0: Disable

			1: Enable
CGVScalDn	11:10	RW	Enable 1'st vertical decimation. 00: Disable 01: 1/2 10: 1/4 11: 1/8
CGHScalDn	9:8	RW	Enable 1'st horizontal decimation. 00: Disable 01: 1/2 10: 1/4 11: 1/8
CGFrmScalDn	7:4	RW	Enable preview mode scale down the throughput. Drop one frame for every n frames.
CGHsyncInv	3	RW	Invert the Hsync signal.
CGVsyncInv	2	RW	Invert the Vsync signal.
CGDmENB	1	RW	Enable decimation. Quality scale frame size to 1/4 0: Disable 1: Enable
CGPatMode	0	RW	Input data mode. 0: Bayer (Row data) 1: YUV (UYVY sequence)

Capture Enable Register 4

Read/Write Port: 0408h

Default Value: 0000h

Field	Bits	Type	Description
CGRunJudge	15	RW	Enable frame size (frame size of sensor output is changed) and registers synchronize for continue digital zoom in.
CGPipeStall	14	RW	Capture pipe stall enable When this bit set, all the capture pip line will stall. It is used before setting new registers.
CGUVExchange	13	RW	Reorder YUV input for "VYUY".
CGMEMRingENB	12	RW	Enable memory re-use for snapshot.
Reserved	11:0	-	Reserved

Capture Ring Register

Read/Write Port: 040Ah

Default Value: 0000h

Field	Bits	Type	Description

-	15:13	-	Reserved
CGRingHeight	12:0	R/W	Row number of snapshot ring(co-operate with 0408[12]).

Capture Horizontal Start Register

Read/Write Port: 040Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGHDS	12:0	R/W	Horizontal data start. Scan line counts after the rising edge of Hsync from sensor. And capture module begin to record the image data

Capture Horizontal End Register

Read/Write Port: 040Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGHDE	12:0	R/W	Horizontal data end. Scan line counts after the rising edge of Hsync from sensor. And capture module stop to record the image data

Capture Vertical Start Register

Read/Write Port: 0410h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGVDS	12:0	R/W	Vertical data start. Scan line counts after the rising edge of Vsync from sensor. And capture module begin to record the image data

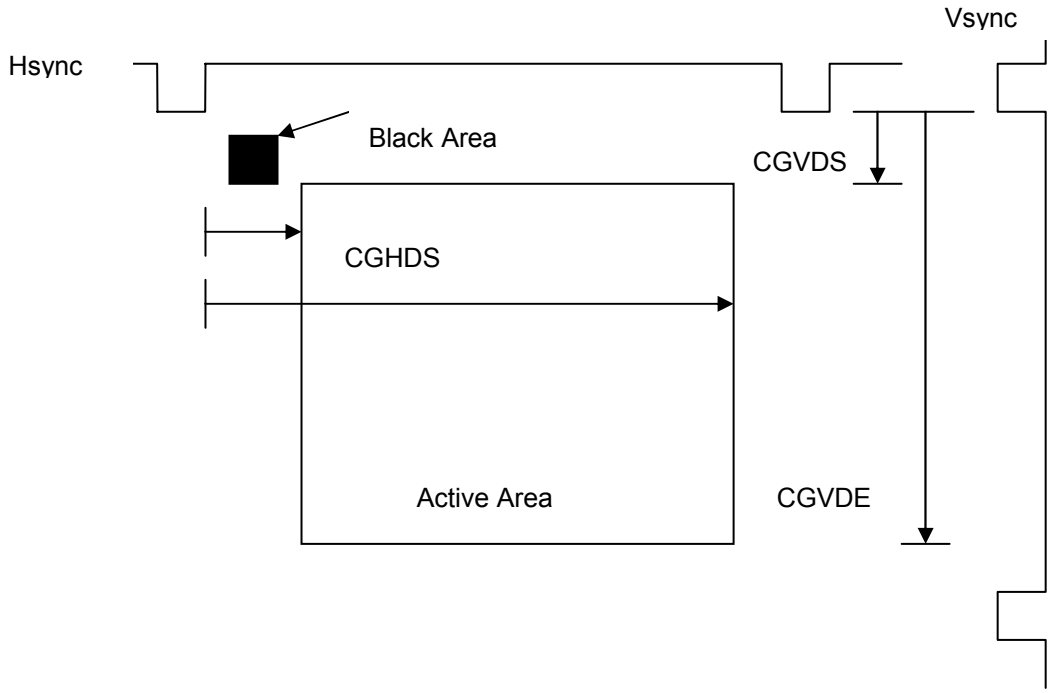
Capture Vertical End Register

Read/Write Port: 0412h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGVDE	12:0	R/W	Vertical data end. Scan line counts after the rising edge of Vsync from sensor. And capture module stop to record the image data

Note:



Capture Horizontal Black Start Register

Read/Write Port: 0414h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGBlkHDS	12:0	R/W	Horizontal black level data start. CCLK clock counts after the rising edge of Hsync from sensor. And Capture module begins to record the black area.

Capture Horizontal Black End Register

Read/Write Port: 0416h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGBlkHDE	12:0	R/W	Horizontal black level data end. CCLK clock counts after the rising edge of Hsync from sensor. And capture module stop to record the black area.

Capture Vertical Black Start Register

Read/Write Port: 0418h

Default Value: 0000h

Field	Bits	Type	Description

-	15:13	-	Reserved
CGBlkVDS	12:0	R/W	Vertical black level data start. Scan line counts after the rising edge of Vsync from sensor. And capture module begin to record the black area

Capture Vertical Black End Register

Read/Write Port: 041Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGBlkVDE	12:0	R/W	Vertical black level data end. Scan line counts after the rising edge of Vsync from sensor. And capture module stop to record the black data.

Note. Capture module uses the area defined by the parameters of CGBlkHDS, CGBlkHDE, CGBlkVDS and CGBlkVDE for black level compensation. The value of black level is the average of the image data in this area. (CGBlkHDE-CGBlkHDS) and (CGBlkVDE-CGBlkHDS) shall be power of 2

Capture Base Address Register 1

Read/Write Port: 041Ch

Default Value: 0000h

Field	Bits	Type	Description
CGFrmBaseAdr0	15:0	R/W	Base address of frame buffer 0. LSB Base address of frame buffer 0 for store the capture image data.

Capture Base Address Register 2

Read/Write Port: 041Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
CGFrmBaseAdr0	5:0	R/W	Base address of frame buffer 0. MSB Base address of frame buffer 0 for store the capture image data.

Capture Base Address Register 3

Read/Write Port: 0420h

Default Value: 0000h

Field	Bits	Type	Description
CGFrmBaseAdr1	15:0	R/W	Base address of frame buffer 1.

			LSB Base address of frame buffer 1 for store the capture image data.

Capture Base Address Register 4

Read/Write Port: 0422h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
CGFrmBaseAdr1	5:0	R/W	Base address of frame buffer 1. MSB Base address of frame buffer 1 for store the capture image data.

Note: The Capture module use double buffer scheme to communicate with ISP module. That is Capture module is saving the data into frame 0 while ISP is processing frame 1. This is for pipe line processing.

Capture Pitch Register

Read/Write Port: 0424h

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
CGPitch	11:0	R/W	SRAM store pitch. Set the pitch with CGPitch = (CGHDE-CGHDS+1)/2

Bad Pixel Base Address Register 1

Read/Write Port: 0426h

Default Value: 0000h

Field	Bits	Type	Description
CGBadPixBaseAdr	15:0	R/W	Bad pixel Base address. LSB Base address to store bad pixel data.

Bad Pixel Base Address Register 2

Read/Write Port: 0428h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
CGBadPixBaseAdr	5:0	R/W	Bad pixel base address. LSB Base address to store bad pixel data.

Note: The data save in the base address is X1, Y1, X2, Y2,…..Xn, Yn, 0xFFFF, 0xFFFF. X and Y parameters are word (2 Bytes). It means that there are n bad pixels recorded with their X, Y position. After the last bad pixel, shall

add two 0xFFFF to represent the end of the data structure. Capture module uses this parameter to identify the position of bad pixel and use the average of contiguous pixels to replace the bad pixel.

Capture Timing Control Register 1

Read/Write Port: 042Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGWrValidVS	12:0	R/W	Start time line of Valid Command interval to micro-p.

Capture Timing Control Register 2

Read/Write Port: 042Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGWrValidVE	12:0	R/W	End time-line of Valid Command interval to micro-p.

Note: Please check the 0x468h register for time-line definition. Use the time-line scheme, we can get the accurate time after Vsync falling edge. Hsync count can not be used because the Hsync will be various according to resolution of sensor setting.

Capture Timer Register1

Read/Write Port: 042Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGFlashCntS	12:0	R/W	Start time-line of flashlight signal becomes high.

Capture Timer Register 2

Read/Write Port: 0430h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
CGFlashCntE	12:0	R/W	End time-line of flashlight signal becomes low.

Note: Please check the 0x468h register for time-line definition. Use the time-line scheme, we can get the accurate time after Vsync falling edge. Hsync count can not be used because the Hsync will be various according to resolution of sensor setting.

Capture Timer Register 1

Read/Write Port: 0432h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:13	RW	Reserved
CGLinePeriod	12:0	RW	CCLK counter per time-line.

Note: The time-line counter use the falling edge of Vsync to start counting. This scheme wants to provide a real and accurate timer.

Capture Offset Register 1

Read/Write Port: 0434h

Default Value: 0000h

Field	Bits	Type	Description
CGROffSet	15:8	R/W	Offset of R component.
CGBOffSet	7:0	R/W	Offset of B component.

Capture Offset Register 2

Read/Write Port: 0436h

Default Value: 0000h

Field	Bits	Type	Description
CGG0OffSet	15:8	R/W	Offset of G0 component.
CGG1OffSet	7:0	R/W	Offset of G1 component.

Capture Gain Register 1

Read/Write Port: 0438h

Default Value: 0000h

Field	Bits	Type	Description
CGRgain	15:8	R/W	Gain of Red. Red gain for gain compensation. The format is 2.6
CGBgain	7:0	R/W	Gain of blue. Blue gain for gain compensation. The format is 2.6

Capture Gain Register 2

Read/Write Port: 043Ah

Default Value: 0000h

Field	Bits	Type	Description
CGG0gain	15:8	R/W	Gain of green0. Green0gain for gain compensation. The format is 2.6
CGG1gain	7:0	R/W	Gain of green1. Green1gain for gain compensation. The format is 2.6

Gamma_R Correction Register 1

Read/Write Port: 043Ch

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4RX	11:9	R/W	Color Red gamma function entry for delta X.
CGGammaLUT3RX	8:6	R/W	Color Red gamma function entry for delta X.
CGGammaLUT2RX	5:3	R/W	Color Red gamma function entry for delta X.
CGGammaLUT1RX	2:0	R/W	Color Red gamma function entry for delta X.

Gamma_R Correction Register 2

Read/Write Port: 043Eh

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT8RX	11:9	R/W	Color Red gamma function entry for delta X.
CGGammaLUT7RX	8:6	R/W	Color Red gamma function entry for delta X.
CGGammaLUT6RX	5:3	R/W	Color Red gamma function entry for delta X.
CGGammaLUT5RX	2:0	R/W	Color Red gamma function entry for delta X.

Note: CGGammaLUT?RX = 000 : deltaX = 8

= 001 : deltaX = 16

= 010 : deltaX = 32

= 011 : deltaX = 64

= 100 : deltaX = 128

= 101 : deltaX = 256

Gamma_R Correction Register 3

Read/Write Port: 0440h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT0RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 4

Read/Write Port: 0442h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT1RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 5

Read/Write Port: 0444h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT2RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 6

Read/Write Port: 0446h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT3RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 7

Read/Write Port: 0448h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 8

Read/Write Port: 044Ah

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT5RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 9

Read/Write Port: 044Ch

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT6RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 10

Read/Write Port: 044Eh

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT7RY	9:0	R/W	Color Red gamma function entry for Y.

Gamma_R Correction Register 11

Read/Write Port: 0450h

Default Value: 0000h

Field	Bits	Type	Description

CGGammaLUT8RY	9:0	R/W	Color Red gamma function entry for Y.

Reserved

Read/Write Port: 0452h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Reserved

Read/Write Port: 0454h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Gamma_G0 Correction Register 1

Read/Write Port: 0456h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4G0X	11:9	R/W	Color Green0 gamma function entry for delta X.
CGGammaLUT3G0X	8:6	R/W	Color Green0 gamma function entry for delta X.
CGGammaLUT2G0X	5:3	R/W	Color Green0 gamma function entry for delta X.
CGGammaLUT1G0X	2:0	R/W	Color Green0 gamma function entry for delta X.

Gamma_G0 Correction Register 2

Read/Write Port: 0458h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT8G0X	11:9	R/W	Color Green0 gamma function entry for delta X.
CGGammaLUT7G0X	8:6	R/W	Color Green0 gamma function entry for delta X.
CGGammaLUT6G0X	5:3	R/W	Color Green0 gamma function entry for delta X.
CGGammaLUT5G0X	2:0	R/W	Color Green0 gamma function entry for delta X.

Gamma_G0 Correction Register 3

Read/Write Port: 045Ah

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT0G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 4

Read/Write Port: 045Ch

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT1G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 5

Read/Write Port: 045Eh

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT2G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 6

Read/Write Port: 0460h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT3G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 7

Read/Write Port: 0462h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 8

Read/Write Port: 0464h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT5G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 9

Read/Write Port: 0466h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT6G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 10

Read/Write Port: 0468h

Default Value: 0000h

Field	Bits	Type	Description

CGGammaLUT7G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Gamma_G0 Correction Register 11

Read/Write Port: 046Ah

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT8G0Y	9:0	R/W	Color Green0 gamma function entry for Y.

Reserved

Read/Write Port: 046Ch

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Reserved

Read/Write Port: 046Eh

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Gamma_G1 Correction Register 1

Read/Write Port: 0470h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4G1X	11:9	R/W	Color Green1 gamma function entry for delta X.
CGGammaLUT3G1X	8:6	R/W	Color Green1 gamma function entry for delta X.
CGGammaLUT2G1X	5:3	R/W	Color Green1 gamma function entry for delta X.
CGGammaLUT1G1X	2:0	R/W	Color Green1 gamma function entry for delta X.

Gamma_G1 Correction Register 2

Read/Write Port: 0472h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT8G1X	11:9	R/W	Color Green1 gamma function entry for delta X.
CGGammaLUT7G1X	8:6	R/W	Color Green1 gamma function entry for delta X.
CGGammaLUT6G1X	5:3	R/W	Color Green1 gamma function entry for delta X.
CGGammaLUT5G1X	2:0	R/W	Color Green1 gamma function entry for delta X.

Gamma_G1 Correction Register 3

Read/Write Port: 0474h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT0G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 4

Read/Write Port: 0476h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT1G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 5

Read/Write Port: 0478h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT2G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 6

Read/Write Port: 047Ah

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT3G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 7

Read/Write Port: 047Ch

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 8

Read/Write Port: 047Eh

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT5G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 9

Read/Write Port: 0480h

Default Value: 0000h

Field	Bits	Type	Description

CGGammaLUT6G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 10

Read/Write Port: 0482h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT7G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Gamma_G1 Correction Register 11

Read/Write Port: 0484h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT8G1Y	9:0	R/W	Color Green1 gamma function entry for Y.

Reserved

Read/Write Port: 0486h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Reserved

Read/Write Port: 0488h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Gamma_B Correction Register 1

Read/Write Port: 048Ah

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4BX	11:9	R/W	Color Blue gamma function entry for delta X.
CGGammaLUT3BX	8:6	R/W	Color Blue gamma function entry for delta X.
CGGammaLUT2BX	5:3	R/W	Color Blue gamma function entry for delta X.
CGGammaLUT1BX	2:0	R/W	Color Blue gamma function entry for delta X.

Gamma_B Correction Register 2

Read/Write Port: 048Ch

Default Value: 0000h

Field	Bits	Type	Description

CGGammaLUT8BX	11:9	R/W	Color Blue gamma function entry for delta X.
CGGammaLUT7BX	8:6	R/W	Color Blue gamma function entry for delta X.
CGGammaLUT6BX	5:3	R/W	Color Blue gamma function entry for delta X.
CGGammaLUT5BX	2:0	R/W	Color Blue gamma function entry for delta X.

Gamma_B Correction Register 3

Read/Write Port: 048Eh

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT0BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 4

Read/Write Port: 0490h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT1BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 5

Read/Write Port: 0492h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT2BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 6

Read/Write Port: 0494h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT3BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 7

Read/Write Port: 0496h

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT4BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 8

Read/Write Port: 0498h

Default Value: 0000h

Field	Bits	Type	Description

CGGammaLUT5BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 9

Read/Write Port: 049Ah

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT6BY	9:0	R/W	Color Blue gamma function entry for Y.

Gamma_B Correction Register 10

Read/Write Port: 049Ch

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT7BY	9:0	R/W	Color Blue gamma function entry for Y.

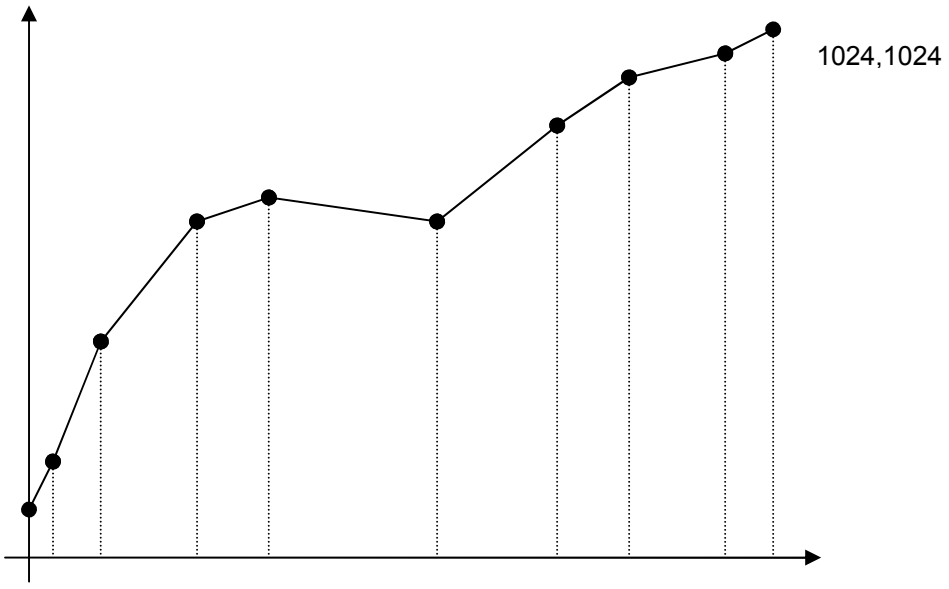
Gamma_B Correction Register 11

Read/Write Port: 049Eh

Default Value: 0000h

Field	Bits	Type	Description
CGGammaLUT8BY	9:0	R/W	Color Blue gamma function entry for Y.

Note: With these parameters, users can customize their own gamma curve. R, B and B gamma curves can be different.



Reserved

Read/Write Port: 04A0h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Reserved

Read/Write Port: 04A2h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:0	-	Reserved

Shading Correction Register 1

Read/Write Port: 04A4h

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
CGShadCenX	11:0	R/W	Center coordinate X of shading correction.

Shading Correction Register 2

Read/Write Port: 04A6h

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
CGShadCenY	11:0	R/W	Center coordinate Y of shading correction.

Shading Correction Register 3

Read/Write Port: 04A8h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15	-	Reserved
CGShadStep3	14:12	RW	Pixels involved in of one step of shading correction step3. “000”: 1 “001”:8 “010”:16 “011”:32 “100”:64 “101”:128 others:256
Reserved	11	RW	Enable Gamma correction 0: Disable 1: Enable
CGShadStep2	10:8	RW	Pixels involved in of one step of shading correction step2. “000”: 1 “001”:8 “010”:16 “011”:32 “100”:64 “101”:128 others:256

Reserved	7	RW	Enable frame rotate write to memory. 0: Disable 1: Enable
CGShadStep1	6:4	RW	Pixels involved in of one step of shading correction step1. “000”: 1 “001”:8 “010”:16 “011”:32 “100”:64 “101”:128 others:256
Reserved	3	R/W	Snapshot mode or preview mode. 0: Preview 1: Snapshot
CGShadStep0	2:0	R/W	Pixels involved in of one step of shading correction step0. “000”: 1 “001”:8 “010”:16 “011”:32 “100”:64 “101”:128 others:256

Shading Correction Register 4

Read/Write Port: 04AAh

Default Value: 0000h

Field	Bits	Type	Description
CGShadSection3	15:12	RW	Section of Shading correction.
CGShadSection2	11:8	RW	Section of Shading correction.
CGShadSection1	7:4	RW	Section of Shading correction.
CGShadSection0	3:0	RW	Section of Shading correction.

Shading Correction Register 5

Read/Write Port: 04ACh

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
CGShadR0	10:0	RW	Radius section setting of shading correction

Shading Correction Register 6

Read/Write Port: 04AEh

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
CGShadR1	10:0	RW	Radius section setting of shading correction

Shading Correction Register 7

Read/Write Port: 04B0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
CGShadR2	10:0	RW	Radius section setting of shading correction

Shading Correction Register 8

Read/Write Port: 04B2h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
CGShadR3	10:0	RW	Radius section setting of shading correction

Shading Correction Register 9

Read/Write Port: 04B4h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
CGShadRmax	10:0	RW	Maximum radius of frame for shading correction

Shading Correction Register 10

Read/Write Port: 04B6h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadG0Gain5A[9:8]	11:10	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain4A[9:8]	9:8	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain3A[9:8]	7:6	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain2A[9:8]	5:4	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain1A[9:8]	3:2	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain0A[9:8]	1:0	RW	MSB of Gain for Green_0 shading correction.

Shading Correction Register 11

Read/Write Port: 04B8h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadG0Gain11A[9:8]	11:10	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain10A[9:8]	9:8	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain9A[9:8]	7:6	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain8A[9:8]	5:4	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain7A[9:8]	3:2	RW	MSB of Gain for Green_0 shading correction.
CGShadG0Gain6A[9:8]	1:0	RW	MSB of Gain for Green_0 shading correction.

Shading Correction Register 12

Read/Write Port: 04BAh

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadG1Gain5A[9:8]	11:10	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain4A[9:8]	9:8	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain3A[9:8]	7:6	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain2A[9:8]	5:4	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain1A[9:8]	3:2	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain0A[9:8]	1:0	RW	MSB of Gain for Green_1 shading correction.

Shading Correction Register 13

Read/Write Port: 04BCh

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadG1Gain11A[9:8]	11:10	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain10A[9:8]	9:8	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain9A[9:8]	7:6	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain8A[9:8]	5:4	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain7A[9:8]	3:2	RW	MSB of Gain for Green_1 shading correction.
CGShadG1Gain6A[9:8]	1:0	RW	MSB of Gain for Green_1 shading correction.

Shading Correction Register 14

Read/Write Port: 04BEh

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain0A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.

CGShadG0Gain0A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 15

Read/Write Port: 04C0h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain1A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain1A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 16

Read/Write Port: 04C2h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain2A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain2A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 17

Read/Write Port: 04C4h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain3A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain3A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 18

Read/Write Port: 04C6h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain4A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain4A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 19

Read/Write Port: 04C8h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain5A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain5A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 20

Read/Write Port: 04CAh

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain6A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain6A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 21

Read/Write Port: 04CCh

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain7A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain7A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Read/Write Port: 04CEh

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain8A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain8A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 22

Read/Write Port: 04D0h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain9A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain9A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 23

Read/Write Port: 04C2h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain10A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain10A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 24

Read/Write Port: 04D4h

Default Value: 0000h

Field	Bits	Type	Description
CGShadG1Gain11A[7:0]	15:8	RW	LSB of Gain for Green_1 shading correction.
CGShadG0Gain11A[7:0]	7:0	RW	LSB of Gain for Green_0 shading correction.

Shading Correction Register 25

Read/Write Port: 04D6h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadRGain5A[9:8]	11:10	RW	MSB of Gain for Red shading correction.
CGShadRGain4A[9:8]	9:8	RW	MSB of Gain for Red shading correction.
CGShadRGain3A[9:8]	7:6	RW	MSB of Gain for Red shading correction.
CGShadRGain2A[9:8]	5:4	RW	MSB of Gain for Red shading correction.
CGShadRGain1A[9:8]	3:2	RW	MSB of Gain for Red shading correction.
CGShadRGain0A[9:8]	1:0	RW	MSB of Gain for Red shading correction.

Shading Correction Register 26

Read/Write Port: 04D8h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadRGain11A[9:8]	11:10	RW	MSB of Gain for Red shading correction.
CGShadRGain10A[9:8]	9:8	RW	MSB of Gain for Red shading correction.
CGShadRGain9A[9:8]	7:6	RW	MSB of Gain for Red shading correction.
CGShadRGain8A[9:8]	5:4	RW	MSB of Gain for Red shading correction.
CGShadRGain7A[9:8]	3:2	RW	MSB of Gain for Red shading correction.
CGShadRGain6A[9:8]	1:0	RW	MSB of Gain for Red shading correction.

Shading Correction Register 27

Read/Write Port: 04DAh

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadBGain5A[9:8]	11:10	RW	MSB of Gain for Blue shading correction.
CGShadBGain4A[9:8]	9:8	RW	MSB of Gain for Blue shading correction.
CGShadBGain3A[9:8]	7:6	RW	MSB of Gain for Blue shading correction.
CGShadBGain2A[9:8]	5:4	RW	MSB of Gain for Blue shading correction.
CGShadBGain1A[9:8]	3:2	RW	MSB of Gain for Blue shading correction.
CGShadBGain0A[9:8]	1:0	RW	MSB of Gain for Blue shading correction.

Shading Correction Register 28

Read/Write Port: 04DCh

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:12	-	Reserved
CGShadBGain11A[9:8]	11:10	RW	MSB of Gain for Blue shading correction.
CGShadBGain10A[9:8]	9:8	RW	MSB of Gain for Blue shading correction.
CGShadBGain9A[9:8]	7:6	RW	MSB of Gain for Blue shading correction.
CGShadBGain8A[9:8]	5:4	RW	MSB of Gain for Blue shading correction.
CGShadBGain7A[9:8]	3:2	RW	MSB of Gain for Blue shading correction.
CGShadBGain6A[9:8]	1:0	RW	MSB of Gain for Blue shading correction.

Shading Correction Register 29

Read/Write Port: 04DEh

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain0A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain0A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 30

Read/Write Port: 04E0h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain1A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain1A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 31

Read/Write Port: 04E2h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain2A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain2A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 32

Read/Write Port: 04E4h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain3A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain3A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 33

Read/Write Port: 04E6h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain4A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain4A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 34

Read/Write Port: 04E8h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain5A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain5A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 35

Read/Write Port: 04EAh

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain6A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain6A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 36

Read/Write Port: 04ECh

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain7A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain7A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 37

Read/Write Port: 04EEh

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain8A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain8A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 38

Read/Write Port: 04F0h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain9A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.

CGShadRGain9A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 39

Read/Write Port: 04F2h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain10A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain10A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Shading Correction Register 40

Read/Write Port: 04F4h

Default Value: 0000h

Field	Bits	Type	Description
CGShadBGain11A[7:0]	15:8	RW	LSB of Gain for Blue shading correction.
CGShadRGain11A[7:0]	7:0	RW	LSB of Gain for Red shading correction.

Note: For shading register setting, please reference to C-Model of Shading Algorithm by W.K. Lin.

Capture IO Driving Register

Read/Write Port: 04F6h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:10	-	Reserved
B0ISPIODrv	5:4	RW	For SCLK IO pad driving strength. 00: lowest driving strength 01: lower driving strength 10: higher driving strength 11: highest driving strength
Reserved	3:0	-	Reserved

Capture Debug Register

Read/Write Port: 04F8h

Default Value: 0000h

Field	Bits	Type	Description
-	15:4	-	Reserved
CGDebugSel	3:0	RW	Debug signal

Capture enable Register

Read/Write Port: 04FAh

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
CGWakeUp	0	RW	Enable the ISP Capture module. 0: Disable Capture module 1: Enable Capture module When change any registers of Capture in command queue mode, be remember set the CGWakeUp at the end of queue sequence.

10.3.7 Image Signal Processor Register

ISP Enable Register 1

Read/Write Port: 0500h

Default Value: 0000h

Field	Bits	Type	Description
I1EnDi565	15	R/W	(I1-- for encoder, and I2-- for decoder) Enable RGB565 dither output 0: Disable 1: Enable
I1EnDi444	14	R/W	Enable RGB444 dither output 0: Disable 1: Enable
I1EnDither	13	R/W	Enable Dither output (for LCD) 0: Disable 1: Enable
I1EnRGB888	12	R/W	Enable RGB888 output (for thumbnail picture) 0: Disable 1: Enable
I1EnStat	11	R/W	Enable Statistic function 0: Disable 1: Enable
I1EnCCFun	10	R/W	Enable Color Correction function 0: Disable 1: Enable
I1EnYUV420	9	R/W	Enable YUV420 mode input 0: Disable: 422

			1: Enable: 420
I1EnCIYUV	8	R/W	Enable YUV format input in color interpolation function 0: Disable 1: Enable
I1PlaneMode	7	R/W	Enable plane mode input 0: Disable 1: Enable
I0YUVPack	6	R/W	Enable YUV packed mode input 0: Disable 1: Enable
I0BayerFormat	5:4	R/W	Starting component in top-left size when Bayer pattern input 00: GR/BG 01: RG/GB 10: BG/GR 11: GB/RG
I0BayerSrc	3	R/W	Enable Bayer source input 0: Disable 1: Enable
I0VideoConf	2	R/W	Enable Video conference mode 0: Disable 1: Enable
I0SrcFmCap	1	R/W	Enable Capture fire ISP mode 0: Disable 1: Enable
IDrvFireISP	0	R/W	Enable driver fire ISP mode 0: Disable 1: Enable

ISP Enable Register 2

Read/Write Port: 0502h

Default Value: 0000h

Field	Bits	Type	Description
I1RdRotDir	15:13	R/W	ISP read rotate direction for MPEG/JPEG 000: 0 degree 001: reserved 010: reserved 011: 180 degree 100: mirror 101: flip

			Others: reserved
I1WrRotDir	12:10	R/W	ISP write rotate direction for LCD 000: 0 degree 001: +90 degree 010: 270 degree 011: 180 degree 100: mirror 101: flip Others: reserved
I0SrcRing	9	R/W	Enable Data from Capture with memory ring mode. 0: Disable 1: Enable
I1OutYUV420	8	R/W	Enable YUV420 output 0: Disable: 422 1: Enable: 420
I1EmBoss	7	R/W	Enable Emboss image effect function 0: Disable 1: Enable
I1EnEdgePro	6	R/W	Enable edge enhancement 0: Disable 1: Enable
I1EnSolat	5	R/W	Enable Solat image effect 0: Disable 1: Enable
I1EnNegative	4	R/W	Enable Negative image effect 0: Disable 1: Enable
I1EnInvMul	3	R/W	Enable Inverse Multiply effect 0: Disable 1: Enable
I1EnFrameFun2	2	R/W	Enable YUV output with frame function 0: Disable 1: Enable
I1EnFrameFun1	1	R/W	Enable LCD output with frame function 0: Disable 1: Enable
I1EnFrameFun	0	R/W	Enable Frame function 0: Disable 1: Enable

ISP Enable Register 3

Read/Write Port: 0504h

Default Value: 0000h

Field	Bits	Type	Description
I2EnDi565	15	R/W	(I1-- for encoder, and I2-- for decoder) Enable RGB565 dither output 0: Disable 1: Enable
I2EnDi444	14	R/W	Enable RGB444 dither output 0: Disable 1: Enable
I2EnDither	13	R/W	Enable Dither output (for LCD) 0: Disable 1: Enable
I2EnRGB888	12	R/W	Enable RGB888 output (for thumbnail picture) 0: Disable 1: Enable
I2EnStat	11	R/W	Enable Statistic function 0: Disable 1: Enable
I2EnCCFun	10	R/W	Enable Color Correction function 0: Disable 1: Enable
I2EnYUV420	9	R/W	Enable YUV420 mode input 0: Disable: 422 1: Enable: 420
I2EnCIYUV	8	R/W	Enable YUV format input in color interpolation function 0: Disable 1: Enable
I2PlaneMode	7	R/W	Enable plane mode input 0: Disable 1: Enable
I0EnScaleimprv	6	R/W	Enable Scaling improve mode 0: Disable 1: Enable
Reserved	5	-	Reserved
I0MWrBufLv[4:0]	4:0	R/W	Write buffer efficiency.

ISP Enable Register 4

Read/Write Port: 0506h

Default Value: 0000h

Field	Bits	Type	Description
I2RdRotDir	15:13	R/W	ISP read rotate direction for MPEG/JPEG 000: 0 degree 001: reserved 010: reserved 011: 180 degree 100: mirror 101: flip Others: reserved
I2WrRotDir	12:10	R/W	ISP write rotate direction for LCD 000: 0 degree 001: +90 degree 010: 270 degree 011: 180 degree 100: mirror 101: flip Others: reserved
I0ParaHold	9	R/W	Enable Command Hold. 0: Disable 1: Enable
I2OutYUV420	8	R/W	Enable YUV420 output 0: Disable: 422 1: Enable: 420
I2EmBoss	7	R/W	Enable Emboss image effect function 0: Disable 1: Enable
I2EnEdgePro	6	R/W	Enable edge enhancement 0: Disable 1: Enable
I2EnSolat	5	R/W	Enable Solat image effect 0: Disable 1: Enable
I2EnNegative	4	R/W	Enable Negative image effect 0: Disable 1: Enable
I2EnInvMul	3	R/W	Enable Inverse Multiply effect

			0: Disable 1: Enable
I2EnFrameFun2	2	R/W	Enable YUV output with frame function 0: Disable 1: Enable
I2EnFrameFun1	1	R/W	Enable LCD output with frame function 0: Disable 1: Enable
I2EnFrameFun	0	R/W	Enable Frame function 0: Disable 1: Enable

ISP Base Address Register 1

Read/Write Port: 0508h

Default Value: 0000h

Field	Bits	Type	Description
I1CI1YStAdr0	15:0	R/W	Encoder Color interpolation Y start address (15:0) of #0

ISP Base Address Register 2

Read/Write Port: 0508h

Default Value: 0000h

Field	Bits	Type	Description
I1CI1YStAdr0	15:0	R/W	Encoder Color interpolation Y start address (15:0) of #0

Note: In Capture input mode, Glamo 3362 provide HW double buffers scheme. This address will be the same as Capture write address CGFrmBaseAdr0 (0x410, 0x412). For example, it will be the bayer address or YUV packed address. In MPEG/JPEG decode mode, it will be the Y start address of plane mode and there is only frame 0 used. It is because that the SW ISP fire is used in MPEG/JPEG decode mode. SW controls the double/triple buffer issue.

ISP Base Address Register 3

Read/Write Port: 050Ch

Default Value: 0000h

Field	Bits	Type	Description
I1CI1YStAdr1	15:0	R/W	Encoder Color interpolation Y start address (15:0) of #1

ISP Base Address Register 4

Read/Write Port: 050Eh

Default Value: 0000h

Field	Bits	Type	Description
I1CI1YStAdr1	6:0	R/W	Encoder Color interpolation Y start address (22:16) of #1

Note: In YUV plane input mode, the address of U start address and there is only frame 0 used. It is because that the SW ISP fire is used in MPEG/JPEG decode mode. SW controls the double/triple buffer issue. In capture mode, this register is reserved.

ISP Base Address Register 5

Read/Write Port: 0510h

Default Value: 0000h

Field	Bits	Type	Description
I0DecYStAdr0	15:0	R/W	Decoder Data of Color interpolation Y start address (15:0) of #0

ISP Base Address Register 6

Read/Write Port: 0512h

Default Value: 0000h

Field	Bits	Type	Description
I0DecYStAdr0	6:0	R/W	Decoder Data of Color interpolation Y start address (22:16) of #0

Note: In YUV plane input mode, the address of V start address and there is only frame 0 used. It is because that the SW ISP fire is used in MPEG/JPEG decode mode. SW controls the double/triple buffer issue. In capture mode, this register is reserved.

ISP Base Address Register 7

Read/Write Port: 0514h

Default Value: 0000h

Field	Bits	Type	Description
I0DecUStAdr0	15:0	R/W	Decoder Data of Color interpolation U start address (15:0) of #0

ISP Base Address Register 8

Read/Write Port: 0516h

Default Value: 0000h

Field	Bits	Type	Description
I0DecUStAdr0	6:0	R/W	Decoder Data of Color interpolation U start address (22:16) of #0

Note: In Capture input mode, Glamo 3362 provide HW double buffers scheme. This address will be the same as Capture write address CGFrmBaseAdr1 (0x414, 0x416). For example, it will be the bayer address or YUV packed address. In JPEG/MPEG decode mode, this register is reserved. So there is no need the U, V address for frame 1.

ISP Base Address Register 9

Read/Write Port: 0518h

Default Value: 0000h

Field	Bits	Type	Description
I0DecVStAdr0	15:0	R/W	Decoder Data of Color interpolation V start address (15:0) of #0

ISP Base Address Register 10

Read/Write Port: 051Ah

Default Value: 0000h

Field	Bits	Type	Description
I0DecVStAdr0	6:0	R/W	Decoder Data of Color interpolation V start address (22:16) of #0

ISP Source Segment Height Register

Read/Write Port: 051Ch

Default Value: 0000h

Field	Bits	Type	Description
I0CapSgHeight	12:0	R/W	Memory height of memory ring mode. (I0SrcRing must be set)

ISP Pitch Register 1

Read/Write Port: 051Eh

Default Value: 0000h

Field	Bits	Type	Description
I1CI1YPitch	12:0	R/W	Encoder Color interpolation pitch (12:0)

ISP Source Height Register

Read/Write Port: 0520h

Default Value: 0000h

Field	Bits	Type	Description
I1CIFrmHeight	12:0	R/W	Image signal process input height (12:0)

ISP Source Height Register

Read/Write Port: 0522h

Default Value: 0000h

Field	Bits	Type	Description
I1CIFrmWidth	12:0	R/W	Image signal process input width (12:0)

ISP Pitch Register 2

Read/Write Port: 0524h

Default Value: 0000h

Field	Bits	Type	Description
I0DecYPitch	12:0	R/W	Decoder Data of Color Y interpolation pitch (12:0)

ISP Pitch Register 3

Read/Write Port: 0526h

Default Value: 0000h

Field	Bits	Type	Description
I0DecUVPitch	6:0	R/W	Decoder Data of Color UV interpolation pitch (12:0)

ISP Source Height Register

Read/Write Port: 0528h

Default Value: 0000h

Field	Bits	Type	Description
I0DecFrmHeight	12:0	R/W	Decoder data input height (12:0)

ISP Decode Width Register

Read/Write Port: 052Ah

Default Value: 0000h

Field	Bits	Type	Description
I0DecFrmWidth	12:0	R/W	Decoder data input width (12:0)

ISP OnFLY Mode Register 1

Read/Write Port: 052Ch

Default Value: 0000h

Field	Bits	Type	Description
I0SrcBlockY	15:8	R/W	Y(6.2) Points jump per Block for OnFly mode.
I0SrcBlockX	7:0	R/W	X(6.2) Points jump per Block for OnFly mode.

ISP OnFLY Mode Register 2

Read/Write Port: 052Eh

Default Value: 0000h

Field	Bits	Type	Description
I0SrcBlockHeight	14:8	R/W	OnFly mode parameters.
I0SrcBlockWidth	6:0	R/W	OnFly mode parameters.

ISP OnFLY Mode Register 3

Read/Write Port: 0530h

Default Value: 0000h

Field	Bits	Type	Description
I0JPEGOutBlkY	13:8	R/W	OnFly mode parameters.
I0JPEGOutBlkX	5:0	R/W	OnFly mode parameters.

ISP OnFLY Mode Register 4

Read/Write Port: 0532h

Default Value: 0000h

Field	Bits	Type	Description
I0P1FifoFullCnt	15:8	R/W	OnFly mode parameters.
I0P2InLength	5:0	R/W	OnFly mode parameters.

ISP OnFLY Mode Register 5

Read/Write Port: 0534h

Default Value: 0000h

Field	Bits	Type	Description
I0P1FifoDateCnt	15:6	R/W	OnFly mode parameters.
I0P2InHeight	5:0	R/W	OnFly mode parameters.

Reserved Register

Read/Write Port: 0536h ~ 053Bh

Default Value: 0000h

ISP Statistic Register 1

Read/Write Port: 053Ch

Default Value: 0000h

Field	Bits	Type	Description
I0StatWrStAdr0	15:0	R/W	Statistic write start address (15:0) of #0

ISP Statistic Register 2

Read/Write Port: 053Eh

Default Value: 0000h

Field	Bits	Type	Description
I0StatWrStAdr0	6:0	R/W	Statistic write start address (22:16) of #0

ISP Statistic Register 3

Read/Write Port: 0540h

Default Value: 0000h

Field	Bits	Type	Description
I0StatWrStAdr1	15:0	R/W	Statistic write start address (15:0) of #0

ISP Statistic Register 4

Read/Write Port: 0542h

Default Value: 0000h

Field	Bits	Type	Description
I0StatWrStAdr1	6:0	R/W	Statistic write start address (22:16) of #0

Note: Glamo 3362 use double buffer for statistic function to avoid reading the old statistic data while updating the new statistic data.

ISP Statistic Register 5

Read/Write Port: 0544h

Default Value: 0000h

Field	Bits	Type	Description
I0StatYTop	7:0	R/W	Statistic Y component upper bound value (7:0) Define the white pixel value upper bound. If the pixel exceed this value will bypass the pixel.

ISP Statistic Register 6

Read/Write Port: 0546h

Default Value: 0000h

Field	Bits	Type	Description
I0statW1Bnd0	14:8	R/W	Statistic Color width 1 value (6:0) for statistic set 0
I0StatYBnd0	7:0	R/W	Statistic Y component lower bound value (7:0) for statistic set 0

ISP Statistic Register 7

Read/Write Port: 0548h

Default Value: 0000h

Field	Bits	Type	Description
I0statDYBnd0	13:8	R/W	Statistic Color shift Y direction value (5:0) for statistic set 0
I0statW2Bnd0	4:0	R/W	Statistic Color width 2 value (4:0) for statistic set 0

ISP Statistic Register 8

Read/Write Port: 054Ah

Default Value: 0000h

Field	Bits	Type	Description
I0StatYBnd1	15:8	R/W	Statistic Y component lower bound value (7:0) for statistic set 1
I0statDXBnd0	5:0	R/W	Statistic Color shift X direction value (5:0) for statistic set 0

ISP Statistic Register 9

Read/Write Port: 054Ch

Default Value: 0000h

Field	Bits	Type	Description
I0statW2Bnd1	12:8	R/W	Statistic Color width 2 value (4:0) for statistic set 1
I0statW1Bnd1	6:0	R/W	Statistic Color width 1 value (6:0) for statistic set 1

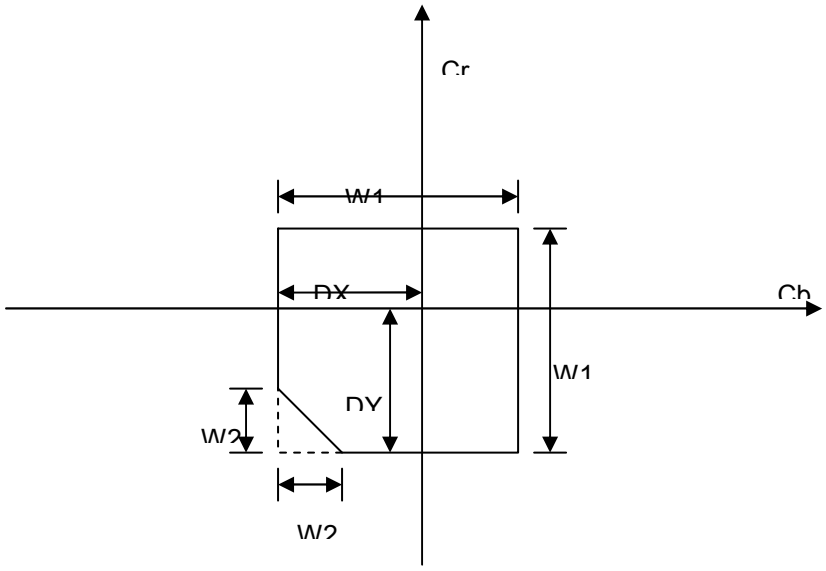
ISP Statistic Register 10

Read/Write Port: 054Eh

Default Value: 0000h

Field	Bits	Type	Description
I0StatDXBnd1	13:8	R/W	Statistic Color shift X direction value (5:0) for statistic set 1
I0StatDYBnd1	5:0	R/W	Statistic Color shift Y direction value (5:0) for statistic set 1

Note: Statistic engine define 2 statistic sets to calculate the “white value”. The parameters are defined as follows:



Color Space Conversion Register 1

Read/Write Port: 0550h

Default Value: 0000h

Field	Bits	Type	Description
I0CIYUV11	9:0	R/W	Color interpolation matrix parameter (1,1)

Color Space Conversion Register 2

Read/Write Port: 0552h

Default Value: 0000h

Field	Bits	Type	Description
I0CIYUV21	9:0	R/W	Color interpolation matrix parameter (2,1)

Color Space Conversion Register 3

Read/Write Port: 0554h

Default Value: 0000h

Field	Bits	Type	Description
I0CIYUV21	9:0	R/W	Color interpolation matrix parameter (2,1)

Color Space Conversion Register 4

Read/Write Port: 0556h

Default Value: 0000h

Field	Bits	Type	Description
I0CIYUV33	9:0	R/W	Color interpolation matrix parameter (3,3)

Color Space Conversion Register 5

Read/Write Port: 0558h

Default Value: 0000h

Field	Bits	Type	Description
I0CIConstR	15:8	R/W	Color interpolation constant R
I0CIConstG	7:0	R/W	Color interpolation constant G

Color Space Conversion Register 6

Read/Write Port: 055Ah

Default Value: 0000h

Field	Bits	Type	Description
I0CIConstB	7:0	R/W	Color interpolation constant B

Note: The color space conversion of YUV to RGB equation as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} CI_{11} & CI_{12} & CI_{13} \\ CI_{21} & CI_{22} & CI_{23} \\ CI_{31} & CI_{32} & CI_{33} \end{bmatrix} \cdot \begin{bmatrix} Y \\ U \\ V \end{bmatrix} + \begin{bmatrix} R_{Const} \\ G_{Const} \\ B_{Const} \end{bmatrix}$$

Color Correction Register 1

Read/Write Port: 055Ch

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB11	12:0	R/W	Color correction matrix (1,1) (S4.8)

Color Correction Register 2

Read/Write Port: 055Eh

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB12	12:0	R/W	Color correction matrix (1,2) (S4.8)

Color Correction Register 3

Read/Write Port: 0560h

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB13	12:0	R/W	Color correction matrix 13(S4.8)

Color Correction Register 4

Read/Write Port: 0562h

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB21	12:0	R/W	Color correction matrix 21(S4.8)

Color Correction Register 5

Read/Write Port: 0564h

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB22	12:0	R/W	Color correction matrix 22(S4.8)

Color Correction Register 6

Read/Write Port: 0566h

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB23	12:0	R/W	Color correction matrix 23(S4.8)

Color Correction Register 7

Read/Write Port: 0568h

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB31	12:0	R/W	Color correction matrix 11(S4.8)

Color Correction Register 8

Read/Write Port: 056Ah

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB32	12:0	R/W	Color correction matrix 32(S4.8)

Color Correction Register 9

Read/Write Port: 056Ch

Default Value: 0000h

Field	Bits	Type	Description
I0TCCRGB33	12:0	R/W	Color correction matrix 33(S4.8)

Color Correction Register 10

Read/Write Port: 056Eh

Default Value: 0000h

Field	Bits	Type	Description
I0CCDeltaR	7:0	R/W	Color correction Delta R component (S7.0)

Color Correction Register 11

Read/Write Port: 0570h

Default Value: 0000h

Field	Bits	Type	Description
I0CCDeltaG	7:0	R/W	Color correction Delta G component (S7.0)

Color Correction Register 12

Read/Write Port: 0572h

Default Value: 0000h

Field	Bits	Type	Description
I0CCDeltaB	7:0	R/W	Color correction Delta B component (S7.0)

Note: The color correction equation as follows:

$$\begin{bmatrix} R_{DST} \\ G_{DST} \\ B_{DST} \end{bmatrix} = \begin{bmatrix} CC_{11} & CC_{12} & CC_{13} \\ CC_{21} & CC_{22} & CC_{23} \\ CC_{31} & CC_{32} & CC_{33} \end{bmatrix} \cdot \begin{bmatrix} R_{SRC} \\ G_{SRC} \\ B_{SRC} \end{bmatrix} + \begin{bmatrix} R_{Delta} \\ G_{Delta} \\ B_{Delta} \end{bmatrix}$$

Image Effect Register 1

Read/Write Port: 0574h

Default Value: 0000h

Field	Bits	Type	Description
I0EmBossStg	7:6	R/W	Emboss function setting, bit7: sign, bit6: pixel

			00: up direction with 1 pixel 01: up direction with 2 pixels 10: down direction with 1 pixel 11: down direction with 2 pixels
I0EdgeStg	5:4	R/W	Edge enhancement stage (3: Max; 0: min)
I0InvMulK0	3:0	R/W	Inverse multiply K0 (0.4 fromat)

Note:

Emboss equation:

DST[y][x] = 127 + sign*(SRC[y][x] - SRC[y+pixel][x+pixel])

Edge enhancement equation:

DST[y][x] = SRC[y][x] + IEdgeStg*(8 * SRC[y][x] –
(SRC[y-1][y-1] + SRC[y-1][x] + SRC[y-1][x+1] +
SRC[y][x-1] + SRC[y][x+1] + SRC[y+1][x-1] +
SRC[y+1][y]+SRC[y+1][x+1])) / 32);

Inverse multiply are used in night shot mode and its equation is:

DST[y][x] = 255*K0 – (255 – SRC[y][x]*K0)^2

Image Scaling Register 1

Read/Write Port: 0576h

Default Value: 0000h

Field	Bits	Type	Description
I0Scale1HCI	15:0	R/W	Saling factor in H direction of port 1 (5.11 format)

Image Scaling Register 2

Read/Write Port: 0578h

Default Value: 0000h

Field	Bits	Type	Description
I0Scale1VCI	15:0	R/W	Scaling factor in V direction of port 1 (5.11 format)

Image Scaling Register 3

Read/Write Port: 057Ah

Default Value: 0000h

Field	Bits	Type	Description
I0Scale2HCI	15:0	R/W	Saling factor in H direction of port 2 (5.11 format)

Image Scaling Register 4

Read/Write Port: 057Ch

Default Value: 0000h

Field	Bits	Type	Description

I0Scale2VCI	15:0	R/W	Scaling factor in V direction of port 2 (5.11 format)

Note: HCI and VCI is the incremental factor for scaling step in horizontal and vertical direction. Following show the case of scaling factor larger than 1 and smaller than 1.

Image Scaling Register 5

Read/Write Port: 057Eh

Default Value: 0000h

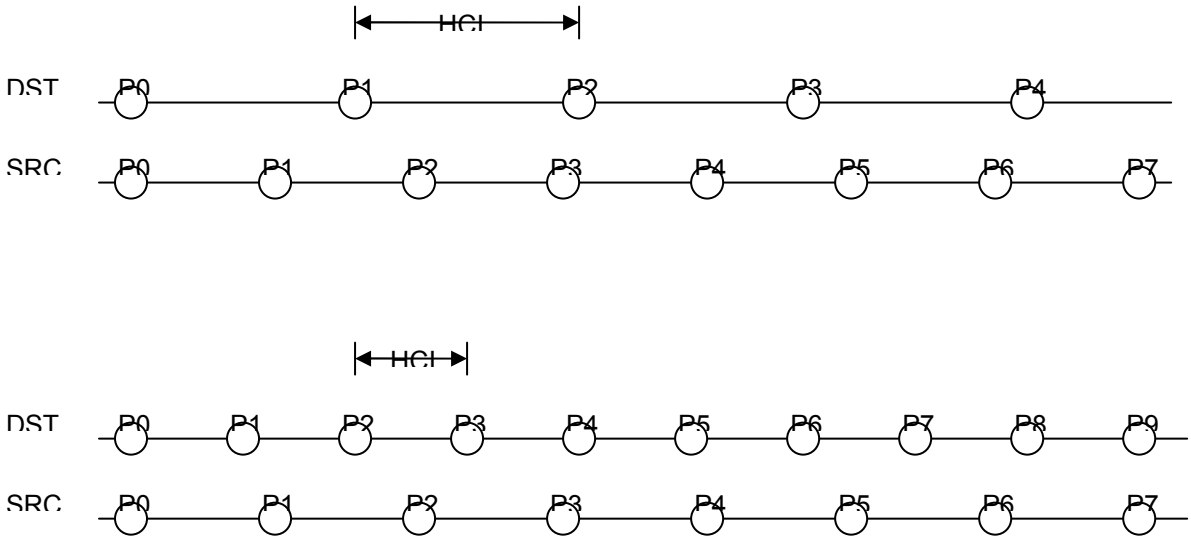
Field	Bits	Type	Description
I0Scale3HCI	15:0	R/W	Saling factor in H direction of decoder (5.11 format)

Image Scaling Register 6

Read/Write Port: 0580h

Default Value: 0000h

Field	Bits	Type	Description
I0Scale3VCI	15:0	R/W	Scaling factor in V direction of decoder (5.11 format)



ISP Turbo Register

Read/Write Port: 0582h

Default Value: 0000h

Field	Bits	Type	Description
I0EnEncoderFast	13	R/W	Enable Encode faster than the preview when videoconference mode 0: Disable 1: Enable
I0EnPViewFast	12	R/W	Enable preview faster than the mpeg encoder when

			videoconference mode 0: Disable 1: Enable
I0PreViewFCnt	11:9	R/W	When the I0EnEncoderFast = '1' or I0EnPViewFast = '1', this counter show the drop frame number between preview/mpeg encoder 000: Encoder rate same as preview 001: Slower(depend on the enable bit) drop one frame in each 2 frames 010: Slower drop one frame in each 3 frames … 111: Slower drop one frame in each 7 frames
I0EnPViewTurbo	8	R/W	Enable preview turbo mode 0: Disable 1: Enable Generally, Capture and ISP module will delay 1 frame. When this bit enable, Capture and ISP module will process the same frame with delay some scan lines. It will improve the delay time between real image and LCD display.
I0PrePViewSliNum	7:0	R/W	The 32-line number of the capture image saved brfore ISP start processing the image. Used in perview turbo mode.

Image Enable Register 3

Read/Write Port: 0584h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:5	R/W	Reserved
I1EnDualBuf1	4	R/W	Enable double buffer output for port 1 0: disable (only single buffer) 1: enable
I1EnClipOut1	3	R/W	Enable clipping of outside region for port 1 0: clipping of inside region 1: clipping of outside region
I1EnClipOn1	2	R/W	Enable clipping function for port 1 0: disable 1: enable
I1EnScale1	1	R/W	Enable scale for port 1 0: Disable (Bypass the 4-by-4 scaling engine) 1: Enable (Scale the image according to the scaling factor)

I1EnOutput1	0	R/W	Enable output for port 1 0: Disable (Bypass the port1 image processing) 1: Enable

ISP Output Port 1 Base Address Register 1

Read/Write Port: 0586h

Default Value: 0000h

Field	Bits	Type	Description
I1O0StWrAddr	15:0	R/W	Output start address (15:0) of frame 0 for port 1

ISP Output Port 1 Base Address Register 2

Read/Write Port: 0588h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:7	R/W	Reserved
I1O0StWrAddr	6:0	R/W	Output start address (22:16) of frame 0 for port 1

ISP Output Port 1 Base Address Register 3

Read/Write Port: 058Ah

Default Value: 0000h

Field	Bits	Type	Description
I1O1StWrAddr	15:0	R/W	Output start address (15:0) of frame 1 for port 1

ISP Output Port 1 Base Address Register 4

Read/Write Port: 058Ch

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:7	R/W	Reserved
I1O1StWrAddr	6:0	R/W	Output start address (22:16) of frame 1 for port 1

Note: ISP output port 1 is output to LCD display. To achieve tearing free, Glamo 3362 support double buffer flip for LCD display.

ISP Output Port 1 Width Register

Read/Write Port: 058Eh

Default Value: 0000h

Field	Bits	Type	Description
I1O1FrmWidth	11:0	R/W	Output width of port 1

ISP Output Register Port 1 Height

Read/Write Port: 0590h

Default Value: 0000h

Field	Bits	Type	Description
I1O1FrmHeight	11:0	R/W	Output height of port 1

ISP Output Port 1 Pitch Register

Read/Write Port: 0592h

Default Value: 0000h

Field	Bits	Type	Description
I1O1Pitch	11:0	R/W	Output pitch of port 1

ISP Output Port 1 Clipping Register 1

Read/Write Port: 0594h

Default Value: 0000h

Field	Bits	Type	Description
I1ClipLeft1	11:0	R/W	Output clipping left of port 1

ISP Output Port 1 Clipping Register 2

Read/Write Port: 0596h

Default Value: 0000h

Field	Bits	Type	Description
I1ClipRight1	11:0	R/W	Output clipping right of port 1

ISP Output Port 1 Clipping Register 3

Read/Write Port: 0598h

Default Value: 0000h

Field	Bits	Type	Description
I1ClipTop1	11:0	R/W	Output clipping top of port 1

ISP Output Port 1 Clipping Register 4

Read/Write Port: 059Ah

Default Value: 0000h

Field	Bits	Type	Description
I1ClipBot1	11:0	R/W	Output clipping bottom of port 1

Note: Clipping function only be supported in port 1, because only the LCD display need to use clipping.

ISP Output Port 1 For decode Enable Register 1

Read/Write Port: 059Ch

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:5	R/W	Reserved
I2EnDualBuf1	4	R/W	Enable double buffer output for port 1 0: disable (only single buffer) 1: enable
I2EnClipOut1	4	R/W	Enable clipping of outside region for port 1 0: clipping of inside region 1: clipping of outside region
I2EnClipOn1	3	R/W	Enable clipping function for port 1 0: disable 1: enable
I2EnClipOn1	2	R/W	Enable scale for port 1 0: Disable (Bypass the 4-by-4 scaling engine) 1: Enable (Scale the image according to the scaling factor)
I0EnUVEdge	1	R/W	Enable uv edge enhancement for JPEG 0: Disable 1: Enable
I2EnOutput1	0	R/W	Enable output for port 1 0: Disable (Bypass the port1 image processing) 1: Enable

ISP Output Port 1 For decode Base Address Register 1

Read/Write Port: 059Eh

Default Value: 0000h

Field	Bits	Type	Description
I1ODec0StWrAddr	15:0	R/W	Output start address (15:0) of frame 0 for port 1

ISP Output Port 1 For decode Base Address Register 2

Read/Write Port: 05A0h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:7	R/W	Reserved
I1ODec0StWrAddr	6:0	R/W	Output start address (22:16) of frame 0 for port 1

ISP Output Port 1 For decode Base Address Register 3

Read/Write Port: 05A2h

Default Value: 0000h

Field	Bits	Type	Description
I1ODec1StWrAddr	15:0	R/W	Output start address (15:0) of frame 1 for port 1

ISP Output Port 1 For decode Base Address Register 4

Read/Write Port: 05A4h

Default Value: 0000h

Field	Bits	Type	Description
Reserved	15:7	R/W	Reserved
I1ODec1StWrAddr	6:0	R/W	Output start address (22:16) of frame 1 for port 1

Note: ISP output port 1 is output to LCD display. To achieve tearing free, Glamo 3362 support double buffer flip for LCD display.

ISP Output Port 1 For decode Width Register

Read/Write Port: 05A6h

Default Value: 0000h

Field	Bits	Type	Description
I1ODecFrmWidth	11:0	R/W	Output width of port 1

ISP Output Port 1 For decode Height

Read/Write Port: 05A8h

Default Value: 0000h

Field	Bits	Type	Description
I1ODecFrmHeight	11:0	R/W	Output height of port 1

ISP Output Port 1 For decode Pitch Register

Read/Write Port: 05AAh

Default Value: 0000h

Field	Bits	Type	Description
I1ODecPitch	11:0	R/W	Output pitch of port 1

ISP Output Port 1 For decode Clipping Register 1

Read/Write Port: 05ACh

Default Value: 0000h

Field	Bits	Type	Description
I0DecClipLeft1	11:0	R/W	Output clipping left of port 1

ISP Output Port 1 For decode Clipping Register 2

Read/Write Port: 05AEh

Default Value: 0000h

Field	Bits	Type	Description
I0DecClipRight1	11:0	R/W	Output clipping right of port 1

ISP Output Port 1 For decode Clipping Register 3

Read/Write Port: 05B0h

Default Value: 0000h

Field	Bits	Type	Description
I0DecClipTop1	11:0	R/W	Output clipping top of port 1

ISP Output Port 1 For decode Clipping Register 4

Read/Write Port: 05B2h

Default Value: 0000h

Field	Bits	Type	Description
I0DecClipBot1	11:0	R/W	Output clipping bottom of port 1

Note: Clipping function only be supported in port 1, because only the LCD display need to use clipping.

ISP Enable Register 4

Read/Write Port: 05B4h

Default Value: 0000h

Field	Bits	Type	Description
I0TotalSliNum	15:8	R/W	Total JPEG-slice number can be buffered in memory.
I0EnDecode	7	R/W	Enable ISP process for MPEG/JPEG decode
I0EnEncoder	6	R/W	Enable ISP process for MPEG/JPEG encode
I0EnMPEG	5	R/W	Enable ISP process for MPEG
I0EnJPEG	4	R/W	Enable ISP process for JPEG
Reserved	3:2	R/W	Reserved
I0EnScale2	1	R/W	Enable scale engine for port 2 0: Disable (Bypass the 4-by-4 scaling engine) 1: Enable (Scale the image according to the scaling factor)
I0EnOutput2	0	R/W	Enable output for port 2 0: Disable (Bypass the port1 image processing) 1: Enable

Note: For MPEG encode, ISP module use 3 frame buffers to handshake with MPEG engine. For JPEG encode, ISP module use Slice buffer to handshake with JPEG engine. ITotalSliNum define the total slice number of this buffer. This is a ring scheme and use read write point to control the slice number.

ISP Output Port 2 Base Address Register 1

Read/Write Port: 05B6h

Default Value: 0000h

Field	Bits	Type	Description
I0O2YStWrAddr	15:0	R/W	Output Y start address (15:0) of frame 0 for port 2

ISP Output Port 2 Base Address Register 2

Read/Write Port: 05B8h

Default Value: 0000h

Field	Bits	Type	Description
I0O2YStWrAddr	6:0	R/W	Output Y start address (22:16) of frame 0 for port 2

ISP Output Port 2 Base Address Register 3

Read/Write Port: 05BAh

Default Value: 0000h

Field	Bits	Type	Description
I0O2UStWrAddr	15:0	R/W	Output U start address (15:0) of frame 0 for port 2

ISP Output Port 2 Base Address Register 4

Read/Write Port: 05BCh

Default Value: 0000h

Field	Bits	Type	Description
I0O2UStWrAddr	6:0	R/W	Output U start address (22:16) of frame 0 for port 2

ISP Output Port 2 Base Address Register 5

Read/Write Port: 05BEh

Default Value: 0000h

Field	Bits	Type	Description
I0O2VStWrAddr	15:0	R/W	Output V start address (15:0) of frame 0 for port 2

ISP Output Port 2 Base Address Register 6

Read/Write Port: 05C0h

Default Value: 0000h

Field	Bits	Type	Description
I0O2VStWrAddr	6:0	R/W	Output V start address (22:16) of frame 0 for port 2

ISP Output Port 2 Base Address Register 7

Read/Write Port: 05C2h

Default Value: 0000h

Field	Bits	Type	Description
I0O2Y1StWrAddr	15:0	R/W	Output Y start address (15:0) of frame 1 for port 2

ISP Output Port 2 Base Address Register 8

Read/Write Port: 05C4h

Default Value: 0000h

Field	Bits	Type	Description
I0O2Y1StWrAddr	6:0	R/W	Output Y start address (22:16) of frame 1 for port 2

ISP Output Port 2 Base Address Register 9

Read/Write Port: 05C6h

Default Value: 0000h

Field	Bits	Type	Description
I0O2U1StWrAddr	15:0	R/W	Output U start address (15:0) of frame 1 for port 2

ISP Output Port 2 Base Address Register 10

Read/Write Port: 05C8h

Default Value: 0000h

Field	Bits	Type	Description
I0O2U1StWrAddr	6:0	R/W	Output U start address (22:16) of frame 1 for port 2

ISP Output Port 2 Base Address Register 11

Read/Write Port: 05CAh

Default Value: 0000h

Field	Bits	Type	Description
I0O2V1StWrAddr	15:0	R/W	Output V start address (15:0) of frame 1 for port 2

ISP Output Port 2 Base Address Register 12

Read/Write Port: 05CCh

Default Value: 0000h

Field	Bits	Type	Description
I0O2V1StWrAddr	6:0	R/W	Output V start address (22:16) of frame 1 for port 2

ISP Output Port 2 Base Address Register 13

Read/Write Port: 05CEh

Default Value: 0000h

Field	Bits	Type	Description
I0O2Y2StWrAddr	15:0	R/W	Output Y start address (15:0) of frame 2 for port 2

ISP Output Port 2 Base Address Register 14

Read/Write Port: 05D0h

Default Value: 0000h

Field	Bits	Type	Description
I0O2Y2StWrAddr	6:0	R/W	Output Y start address (22:16) of frame 2 for port 2

ISP Output Port 2 Base Address Register 15

Read/Write Port: 05D2h

Default Value: 0000h

Field	Bits	Type	Description
I0O2U2StWrAddr	15:0	R/W	Output U start address (15:0) of frame 2 for port 2

ISP Output Port 2 Base Address Register 16

Read/Write Port: 05D4h

Default Value: 0000h

Field	Bits	Type	Description
I0O2U2StWrAddr	6:0	R/W	Output U start address (22:16) of frame 2 for port 2

ISP Output Port 2 Base Address Register 17

Read/Write Port: 05D6h

Default Value: 0000h

Field	Bits	Type	Description
I0O2V2StWrAddr	15:0	R/W	Output V start address (15:0) of frame 2 for port 2

ISP Output Port 2 Base Address Register 18

Read/Write Port: 05D8h

Default Value: 0000h

Field	Bits	Type	Description
I0O2V2StWrAddr	6:0	R/W	Output V start address (22:16) of frame 2 for port 2

Note: Port 2 is ISP output for MPEG/JPEG encode engine. ISP module use triple buffer to handshake with MPEG encode engine. The sequence is controlled by HW and the sequence is 0, 1, 2, 0, 1, 2…. ISP module use one buffer to handshake with JPEG encode engine. That is buffer 0.

ISP Output Port 2 Width Register 1

Read/Write Port: 05DAh

Default Value: 0000h

Field	Bits	Type	Description
I0O2FrmWidth	11:0	R/W	Output width of port 2

ISP Output Port 2 Height Register 2

Read/Write Port: 05DCh

Default Value: 0000h

Field	Bits	Type	Description
I0O2FrmHeight	11:0	R/W	Output Height of port 2

ISP Output Port 2 Pitch Register 1

Read/Write Port: 05DEh

Default Value: 0000h

Field	Bits	Type	Description
I0O2YPitch	11:0	R/W	Output Y pitch of port 2

ISP Output Port Pitch Register 2

Read/Write Port: 05E0h

Default Value: 0000h

Field	Bits	Type	Description
I0O2UVPitch	11:0	R/W	Output UV pitch of port 2

ISP Frame Function Register 1

Read/Write Port: 05E2h

Default Value: 0000h

Field	Bits	Type	Description
IFrameGKey	15:8	R/W	Frame function G component Key value
IFrameRKey	7:0	R/W	Frame function R component Key value

ISP Frame Function Register 2

Read/Write Port: 05E4h

Default Value: 0000h

Field	Bits	Type	Description
IFrameBKey	7:0	R/W	Frame function B component Key value

ISP Frame Function Register 3

Read/Write Port: 05E6h

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunStAdr	15:0	R/W	Frame function start address (15:0)

ISP Frame Function Register 4

Read/Write Port: 05E8h

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunStAdr	6:0	R/W	Frame function start address (22:16)

Note: Frame function is that one image from ISP module can overlay on a graphic with color key. So the graphic image of width, height, base address and color key value shall be defined. Frame function effect can be enabled in

port 1 or port 2.

ISP Frame Function Register 5

Read/Write Port: 05EAh

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunStX	11:0	R/W	Start coordinate X of the frame function

ISP Frame Function Register 6

Read/Write Port: 05ECh

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunStY	11:0	R/W	Start coordinate Y of the frame function

ISP Frame Function Register 7

Read/Write Port: 05EEh

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunWidth	11:0	R/W	Width of the frame function

ISP Frame Function Register 8

Read/Write Port: 05F0h

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunHeight	11:0	R/W	Height of the frame function

ISP Frame Function Register 9

Read/Write Port: 05F2h

Default Value: 0000h

Field	Bits	Type	Description
I0FrmFunPitch	11:0	R/W	Pitch of the frame function

ISP Frame Function Register 10

Read/Write Port: 05F4h

Default Value: 0000h

Field	Bits	Type	Description

I0FrmFunBlkY	14:8	R/W	Block Y of the frame function (6:0)
I0FrmFunBlkX	6:0	R/W	Block X of the frame function (6:0)

ISP RGB to YUV Register 1

Read/Write Port: 05F6h

Default Value: 0000h

Field	Bits	Type	Description
I0OUTYUV12	15:8	R/W	RGB to YUV matrix 12 of port 2
I0OUTYUV11	7:0	R/W	RGB to YUV matrix 11 of port 2

ISP RGB to YUV Register 2

Read/Write Port: 05F8h

Default Value: 0000h

Field	Bits	Type	Description
I0OUTYUV21	15:8	R/W	RGB to YUV matrix 21 of port 2
I0OUTYUV13	7:0	R/W	RGB to YUV matrix 13 of port 2

ISP RGB to YUV Register 3

Read/Write Port: 05FAh

Default Value: 0000h

Field	Bits	Type	Description
I0OUTYUV23	15:8	R/W	RGB to YUV matrix 23 of port 2
I0OUTYUV22	7:0	R/W	RGB to YUV matrix 22 of port 2

ISP RGB to YUV Register4

Read/Write Port: 05FCh

Default Value: 0000h

Field	Bits	Type	Description
I0OUTYUV32	15:8	R/W	RGB to YUV matrix 32 of port 2
I0OUTYUV31	7:0	R/W	RGB to YUV matrix 31 of port 2

ISP RGB to YUV Register5

Read/Write Port: 05FEh

Default Value: 0000h

Field	Bits	Type	Description
I0OUTYUV33	7:0	R/W	RGB to YUV matrix 33 of port 2

Note: RGB to YUV equation:

$$\begin{bmatrix} Y_{DST} \\ U_{DST} \\ V_{DST} \end{bmatrix} = \begin{bmatrix} CO_{11} & CO_{12} & CO_{13} \\ CO_{21} & CO_{22} & CO_{23} \\ CO_{31} & CO_{32} & CO_{33} \end{bmatrix} \cdot \begin{bmatrix} R_{SRC} \\ G_{SRC} \\ B_{SRC} \end{bmatrix}$$

ISP HandShaking Register

Read/Write Port: 0600h

Default Value: 0000h

Field	Bits	Type	Description
I0SliOutNum	15:8	R/W	Slice number of each ISP block will produce. ISliOutNum define the slice threshold number to avoid overflow of the ITotalSliNum.
I0SolarValue	7:0	R/W	Solar image effect judge value

Note: Solar image effect equation:

DST[y][x] = (SRC[y][x] > ISolarValue) ? (255 - SRC[y][x]) : SRC[y][x]

Reserved Register

Read/Write Port: 0602h ~ 060Bh

Default Value: 0000h

ISP Scaling Factor Register 1~80

Read/Write Port: 060Ch ~ 0683h

Default Value: 0000h

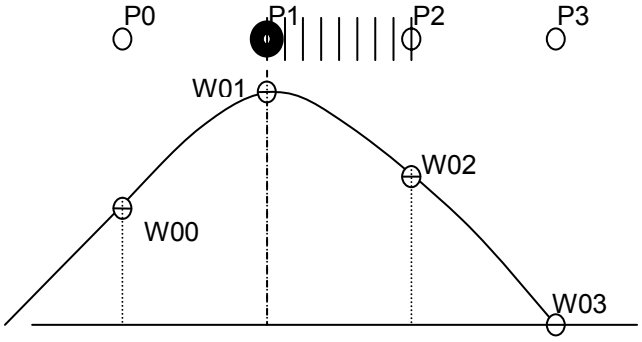
Field	Bits	Type	Description
I1Scale1WX00	7:0	R/W	Scale 1 H direction factor00 (S1.6 format)
I1Scale1WX01	7:0	R/W	Scale 1 H direction factor01 (S1.6 format)
I1Scale1WX02	7:0	R/W	Scale 1 H direction factor02 (S1.6 format)
I1Scale1WX03	7:0	R/W	Scale 1 H direction factor03 (S1.6 format)
I1Scale1WX10	7:0	R/W	Scale 1 H direction factor10 (S1.6 format)
I1Scale1WX11	7:0	R/W	Scale 1 H direction factor11 (S1.6 format)
I1Scale1WX12	7:0	R/W	Scale 1 H direction factor12 (S1.6 format)
I1Scale1WX13	7:0	R/W	Scale 1 H direction factor13 (S1.6 format)
I1Scale1WX20	7:0	R/W	Scale 1 H direction factor20 (S1.6 format)
I1Scale1WX21	7:0	R/W	Scale 1 H direction factor21 (S1.6 format)
I1Scale1WX22	7:0	R/W	Scale 1 H direction factor22 (S1.6 format)
I1Scale1WX23	7:0	R/W	Scale 1 H direction factor23 (S1.6 format)
I1Scale1WX30	7:0	R/W	Scale 1 H direction factor30 (S1.6 format)
I1Scale1WX31	7:0	R/W	Scale 1 H direction factor31 (S1.6 format)
I1Scale1WX32	7:0	R/W	Scale 1 H direction factor32 (S1.6 format)

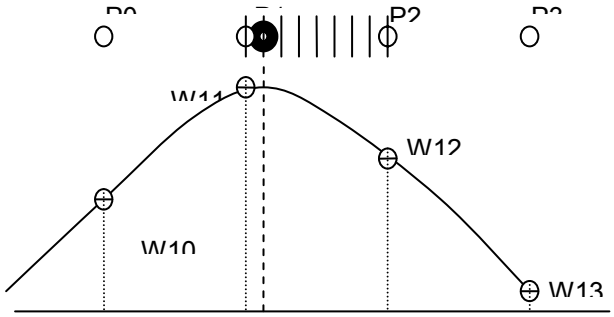
I1Scale1WX33	7:0	R/W	Scale 1 H direction factor33 (S1.6 format)
I1Scale1WX40	7:0	R/W	Scale 1 H direction factor40 (S1.6 format)
I1Scale1WX41	7:0	R/W	Scale 1 H direction factor41 (S1.6 format)
I1Scale1WX42	7:0	R/W	Scale 1 H direction factor42 (S1.6 format)
I1Scale1WX43	7:0	R/W	Scale 1 H direction factor43 (S1.6 format)
I1Scale1WY00	7:0	R/W	Scale 1 V direction factor00 (S1.6 format)
I1Scale1WY01	7:0	R/W	Scale 1 V direction factor01 (S1.6 format)
I1Scale1WY02	7:0	R/W	Scale 1 V direction factor02 (S1.6 format)
I1Scale1WY03	7:0	R/W	Scale 1 V direction factor03 (S1.6 format)
I1Scale1WY10	7:0	R/W	Scale 1 V direction factor10 (S1.6 format)
I1Scale1WY11	7:0	R/W	Scale 1 V direction factor11 (S1.6 format)
I1Scale1WY12	7:0	R/W	Scale 1 V direction factor12 (S1.6 format)
I1Scale1WY13	7:0	R/W	Scale 1 V direction factor13 (S1.6 format)
I1Scale1WY20	7:0	R/W	Scale 1 V direction factor20 (S1.6 format)
I1Scale1WY21	7:0	R/W	Scale 1 V direction factor21 (S1.6 format)
I1Scale1WY22	7:0	R/W	Scale 1 V direction factor22 (S1.6 format)
I1Scale1WY23	7:0	R/W	Scale 1 V direction factor23 (S1.6 format)
I1Scale1WY30	7:0	R/W	Scale 1 V direction factor30 (S1.6 format)
I1Scale1WY31	7:0	R/W	Scale 1 V direction factor31 (S1.6 format)
I1Scale1WY32	7:0	R/W	Scale 1 V direction factor32 (S1.6 format)
I1Scale1WY33	7:0	R/W	Scale 1 V direction factor33 (S1.6 format)
I1Scale1WY40	7:0	R/W	Scale 1 V direction factor40 (S1.6 format)
I1Scale1WY41	7:0	R/W	Scale 1 V direction factor41 (S1.6 format)
I1Scale1WY42	7:0	R/W	Scale 1 V direction factor42 (S1.6 format)
I1Scale1WY43	7:0	R/W	Scale 1 V direction factor43 (S1.6 format)
I0Scale2WX00	7:0	R/W	Scale 2 H direction factor00 (S1.6 format)
I0Scale2WX01	7:0	R/W	Scale 2 H direction factor01 (S1.6 format)
I0Scale2WX02	7:0	R/W	Scale 2 H direction factor02 (S1.6 format)
I0Scale2WX03	7:0	R/W	Scale 2 H direction factor03 (S1.6 format)
I0Scale2WX10	7:0	R/W	Scale 2 H direction factor10 (S1.6 format)
I0Scale2WX11	7:0	R/W	Scale 2 H direction factor11 (S1.6 format)
I0Scale2WX12	7:0	R/W	Scale 2 H direction factor12 (S1.6 format)
I0Scale2WX13	7:0	R/W	Scale 2 H direction factor13 (S1.6 format)
I0Scale2WX20	7:0	R/W	Scale 2 H direction factor20 (S1.6 format)
I0Scale2WX21	7:0	R/W	Scale 2 H direction factor21 (S1.6 format)
I0Scale2WX22	7:0	R/W	Scale 2 H direction factor22 (S1.6 format)
I0Scale2WX23	7:0	R/W	Scale 2 H direction factor23 (S1.6 format)
I0Scale2WX30	7:0	R/W	Scale 2 H direction factor30 (S1.6 format)

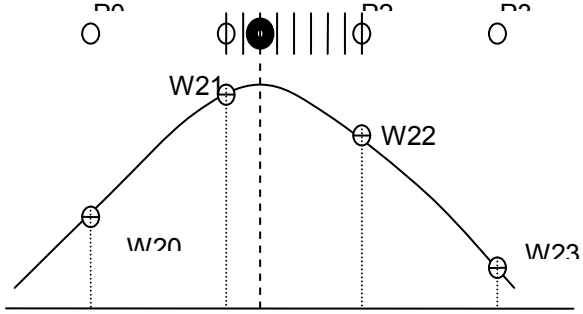
I0Scale2WX31	7:0	R/W	Scale 2 H direction factor31 (S1.6 format)
I0Scale2WX32	7:0	R/W	Scale 2 H direction factor32 (S1.6 format)
I0Scale2WX33	7:0	R/W	Scale 2 H direction factor33 (S1.6 format)
I0Scale2WX40	7:0	R/W	Scale 2 H direction factor40 (S1.6 format)
I0Scale2WX41	7:0	R/W	Scale 2 H direction factor41 (S1.6 format)
I0Scale2WX42	7:0	R/W	Scale 2 H direction factor42 (S1.6 format)
I0Scale2WX43	7:0	R/W	Scale 2 H direction factor43 (S1.6 format)
I0Scale2WY00	7:0	R/W	Scale 2 V direction factor00 (S1.6 format)
I0Scale2WY01	7:0	R/W	Scale 2 V direction factor01 (S1.6 format)
I0Scale2WY02	7:0	R/W	Scale 2 V direction factor02 (S1.6 format)
I0Scale2WY03	7:0	R/W	Scale 2 V direction factor03 (S1.6 format)
I0Scale2WY10	7:0	R/W	Scale 2 V direction factor10 (S1.6 format)
I0Scale2WY11	7:0	R/W	Scale 2 V direction factor11 (S1.6 format)
I0Scale2WY12	7:0	R/W	Scale 2 V direction factor12 (S1.6 format)
I0Scale2WY13	7:0	R/W	Scale 2 V direction factor13 (S1.6 format)
I0Scale2WY20	7:0	R/W	Scale 2 V direction factor20 (S1.6 format)
I0Scale2WY21	7:0	R/W	Scale 2 V direction factor21 (S1.6 format)
I0Scale2WY22	7:0	R/W	Scale 2 V direction factor22 (S1.6 format)
I0Scale2WY23	7:0	R/W	Scale 2 V direction factor23 (S1.6 format)
I0Scale2WY30	7:0	R/W	Scale 2 V direction factor30 (S1.6 format)
I0Scale2WY31	7:0	R/W	Scale 2 V direction factor31 (S1.6 format)
I0Scale2WY32	7:0	R/W	Scale 2 V direction factor32 (S1.6 format)
I0Scale2WY33	7:0	R/W	Scale 2 V direction factor33 (S1.6 format)
I0Scale2WY40	7:0	R/W	Scale 2 V direction factor40 (S1.6 format)
I0Scale2WY41	7:0	R/W	Scale 2 V direction factor41 (S1.6 format)
I0Scale2WY42	7:0	R/W	Scale 2 V direction factor42 (S1.6 format)
I0Scale2WY43	7:0	R/W	Scale 2 V direction factor43 (S1.6 format)
I1Scale3WX00	7:0	R/W	Scale 3 H direction factor00 (S1.6 format)
I1Scale3WX01	7:0	R/W	Scale 3 H direction factor01 (S1.6 format)
I1Scale3WX02	7:0	R/W	Scale 3 H direction factor02 (S1.6 format)
I1Scale3WX03	7:0	R/W	Scale 3 H direction factor03 (S1.6 format)
I1Scale3WX10	7:0	R/W	Scale 3 H direction factor10 (S1.6 format)
I1Scale3WX11	7:0	R/W	Scale 3 H direction factor11 (S1.6 format)
I1Scale3WX12	7:0	R/W	Scale 3 H direction factor12 (S1.6 format)
I1Scale3WX13	7:0	R/W	Scale 3 H direction factor13 (S1.6 format)
I1Scale3WX20	7:0	R/W	Scale 3 H direction factor20 (S1.6 format)
I1Scale3WX21	7:0	R/W	Scale 3 H direction factor21 (S1.6 format)
I1Scale3WX22	7:0	R/W	Scale 3 H direction factor22 (S1.6 format)

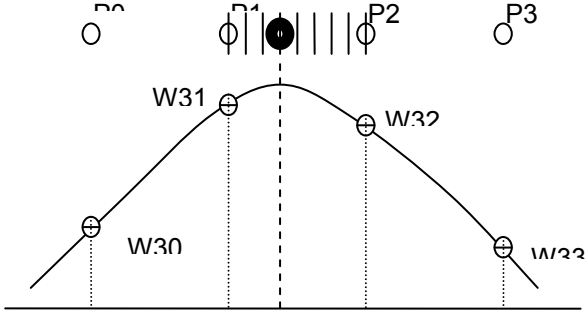
I1Scale3WX23	7:0	R/W	Scale 3 H direction factor23 (S1.6 format)
I1Scale3WX30	7:0	R/W	Scale 3 H direction factor30 (S1.6 format)
I1Scale3WX31	7:0	R/W	Scale 3 H direction factor31 (S1.6 format)
I1Scale3WX32	7:0	R/W	Scale 3 H direction factor32 (S1.6 format)
I1Scale3WX33	7:0	R/W	Scale 3 H direction factor33 (S1.6 format)
I1Scale3WX40	7:0	R/W	Scale 3 H direction factor40 (S1.6 format)
I1Scale3WX41	7:0	R/W	Scale 3 H direction factor41 (S1.6 format)
I1Scale3WX42	7:0	R/W	Scale 3 H direction factor42 (S1.6 format)
I1Scale3WX43	7:0	R/W	Scale 3 H direction factor43 (S1.6 format)
I1Scale3WY00	7:0	R/W	Scale 3 V direction factor00 (S1.6 format)
I1Scale3WY01	7:0	R/W	Scale 3 V direction factor01 (S1.6 format)
I1Scale3WY02	7:0	R/W	Scale 3 V direction factor02 (S1.6 format)
I1Scale3WY03	7:0	R/W	Scale 3 V direction factor03 (S1.6 format)
I1Scale3WY10	7:0	R/W	Scale 3 V direction factor10 (S1.6 format)
I1Scale3WY11	7:0	R/W	Scale 3 V direction factor11 (S1.6 format)
I1Scale3WY12	7:0	R/W	Scale 3 V direction factor12 (S1.6 format)
I1Scale3WY13	7:0	R/W	Scale 3 V direction factor13 (S1.6 format)
I1Scale3WY20	7:0	R/W	Scale 3 V direction factor20 (S1.6 format)
I1Scale3WY21	7:0	R/W	Scale 3 V direction factor21 (S1.6 format)
I1Scale3WY22	7:0	R/W	Scale 3 V direction factor22 (S1.6 format)
I1Scale3WY23	7:0	R/W	Scale 3 V direction factor23 (S1.6 format)
I1Scale3WY30	7:0	R/W	Scale 3 V direction factor30 (S1.6 format)
I1Scale3WY31	7:0	R/W	Scale 3 V direction factor31 (S1.6 format)
I1Scale3WY32	7:0	R/W	Scale 3 V direction factor32 (S1.6 format)
I1Scale3WY33	7:0	R/W	Scale 3 V direction factor33 (S1.6 format)
I1Scale3WY40	7:0	R/W	Scale 3 V direction factor40 (S1.6 format)
I1Scale3WY41	7:0	R/W	Scale 3 V direction factor41 (S1.6 format)
I1Scale3WY42	7:0	R/W	Scale 3 V direction factor42 (S1.6 format)
I1Scale3WY43	7:0	R/W	Scale 3 V direction factor43 (S1.6 format)

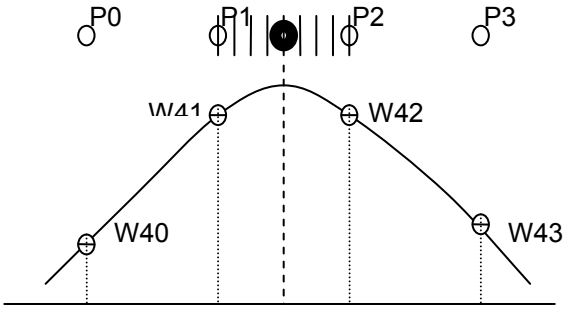
Note: MMP365 support 4-tape horizontal and 4-tape vertical scaling engine. The 4-tape coefficients of horizontal and vertical can be programmed independently. There are 8 scaling steps between contiguous pixel. That is, there are 8 different weighted points can be generated between two contiguous pixel. Port 1 and Port 2 use different scaling factor. So we shall general the weight table as defined in 0x5EAh~0x6E8h. Check the following diagram for weight coefficient description.

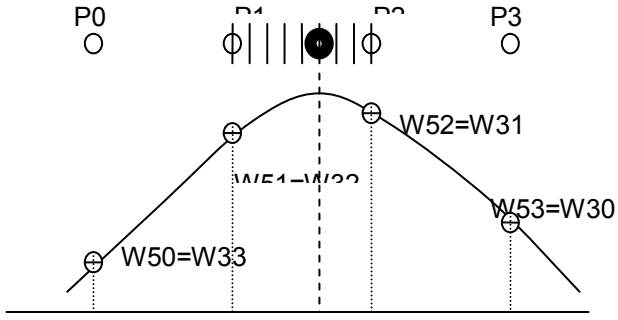


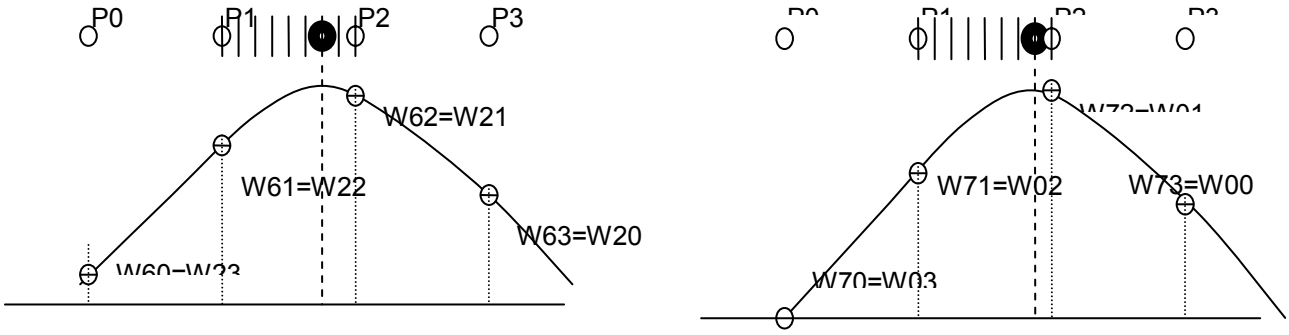












ISP Status Register

Read Port: 0684h

Default Value:

Field	Bits	Type	Description
ISP status	0	R	0: idle, 1: busy

10.3.8 JPEG Engine Register

JPEG Codec Control Register

Read/Write Port: 0A00h

Default Value: 0000h

Field	Bits	Type	Description
	15:14		Reserved
UVLowPassMode	13	RW	0: Turn off 1: Turn on
YLowPassMode	12	RW	0: Turn off 1: Turn on
ACTabSel	11	RW	Decoding process and non-interleave mode only 0: Luminance 1: Chrominance
DCTabSel	10	RW	Decoding process and non-interleave mode only 0: Luminance 1: Chrominance
QuantTabSel	9	RW	Decoding process and non-interleave mode only 0: Luminance 1: Chrominance

DeComponent	8:7	RW	Decoding process and non-interleave mode only 00: Y Component 01: U Component 10: V Component
NonInterMode	6	RW	Decoding process only 0: Interleave mode 1: Non-interleave mode
ISPOnFlyMode	5	RW	Encoding process only. And when the flag set 1, Edge Enhancement Mode flag must set 1. 0 : Data read from SRAM 1 : Data read from Buffer between ISP and JPEG
EdgeEnhanceMode	4	RW	0: Turn off 1: Turn on
EncTrigMode	3	RW	Encoding Trigger Mode 0 : Trigger by ISP 1 : Trigger by Command This flag is valid only when encoding mode. When trigger by ISP, hardware controls the flow automatically. When trigger by Command, software controls the flow.
ColorFormat	2:1	RW	Color Format 00 : YUV 4:4:4 01 : YUV 4:2:2 10 : YUV 4:2:0 11 : YUV 4:1:1 Decoding process supports 4:2:2, 4:2:0, 4:4:4 and 4:1:1. Encoding process supports 4:2:2.
OpMode	0	RW	Operation Mode 0: Encoding process 1: Decoding process

DRI Setting Register

Read/Write Port: 0A02h

Default Value: 0000h

Field	Bits	Type	Description
RstMCUNum	15:0	RW	Specifies the number of MCU in the restart interval. When set all zero, it means no RST marker insertion. Ex. If there are 16 MCU in the interval, S/W should set 0x10 to the register.

JPEG Interrupt Control Register

Read/Write Port: 0A04h

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	RW	Reserved
	8	RW	Valid Data Occupancy Threshold Interrupt Enable 0 : Disable 1 : Enable
	7	RW	Bitstream Buffer Full Interrupt Enable 0 : Disable 1 : Enable
	6	RW	Bitstream Buffer Empty Interrupt Enable 0 : Disable 1 : Enable
	5	RW	Line Buffer Full Interrupt Enable 0 : Disable 1 : Enable
	4	RW	Line Buffer Empty Interrupt Enable 0 : Disable 1 : Enable
	3	RW	Maximum encoded size violation Interrupt Enable 0 : Disable 1 : Enable
	2	RW	Decode Error Interrupt Enable 0 : Disable 1 : Enable
	1	RW	JPEG Encode Complete Interrupt Enable 0 : Disable 1 : Enable
	0	RW	JPEG Decode Complete Interrupt Enable 0 : Disable 1 : Enable

MCU Width of Y Component Register

Read/Write Port: 0A06h

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
MCUWidth	8:0	RW	The MCU width [8:0] of Y component

			Ex. 4:2:2 1280x1024 image size MCU width is 1280/16 = 80 Ex. 4:4:4 1280x1024 image size MCU width is 1280/8 = 160 Ex. 4:2:0 1280x1024 image size MCU width is 1280/16 = 80 Ex. 4:1:1 1280x1024 image size MCU width is 1280/32 = 40

MCU Height of Y Component Register

Read/Write Port: 0A08h

Default Value: 0000h

Field	Bits	Type	Description
-	15:8	-	Reserved
MCUHeight	7:0	RW	The MCU height [7:0] of Y component Ex. 4:2:2 1280x1024 image size MCU height is 1024/8 = 128 Ex. 4:4:4 1280x1024 image size MCU height is 1024/8 = 128 Ex. 4:2:0 1280x1024 image size MCU height is 1024/16 = 64 Ex. 4:1:1 1280x1024 image size MCU height is 10240/8 = 128

Base Address of Y Component Register 1

Read/Write Port: 0A0Ah

Default Value: 0000h

Field	Bits	Type	Description
YBaseAdr	15:0	RW	Base Address [15:0] of Y Component The twenty-two bits of line buffer address in 16-bit unit can address up to 8M bytes SRAM. For Encode and ISP trigger mode, ISP will put the Y slice data in this buffer. For Encode and Command trigger mode, S/W will put the Y slice data in this buffer. For Decode mode, JPEG Codec will put the decoded Y frame in this buffer.

Base Address of Y Component Register 2

Read/Write Port: 0A0Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
YBaseAdr	5:0	RW	Base Address [21:16] of Y Component

Base Address of U Component Register 1

Read/Write Port: 0A0Eh

Default Value: 0000h

Field	Bits	Type	Description
UBaseAdr	15:0	RW	Base Address [15:0] of U Component The twenty-two bits of line buffer address in 16-bit unit can address up to 8M bytes SRAM. For Decode mode, JPEG Codec will put the decoded U frame in this buffer.

Base Address of U Component Register 2

Read/Write Port: 0A10h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
UBaseAdr	5:0	RW	Base Address [21:16] of U Component

Base Address of V Component Register 1

Read/Write Port: 0A12h

Default Value: 0000h

Field	Bits	Type	Description
VBaseAdr	15:0	RW	Base Address [15:0] of V Component The twenty-two bits of line buffer address in 16-bit unit can address up to 8M bytes SRAM. For Decode mode, JPEG Codec will put the decoded V frame in this buffer.

Base Address of V Component Register 2

Read/Write Port: 0A14h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
VBaseAdr	5:0	RW	Base Address [21:16] of V Component

Line Buffer Number Register

Read/Write Port: 0A16h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
SliceNum	4:0	RW	The Number of Line Buffer [4:0] in Slice Unit Slice Unit means 8 x frame width. Ex. 1280 x 1024 encoded frame has (1024/8) slice. Maximum number is 16 slices. The number of U, V components slices is SliceNum / 2. And U, V slice is 8 x (frame_width/2)

Y Pitch Register

Read/Write Port: 0A18h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
YPitch	10:0	RW	Pitch [10:0] of Y Component Line Buffer in 16-bits Unit

U,V Pitch Register

Read/Write Port: 0A1Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
YPitch	10:0	RW	Pitch [10:0] of U,V Component Line Buffer in 16-bits Unit

Write Buffer Register

Read/Write Port: 0A1Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
WrSlicNum	4:0	RW	The Write Number for Line Buffer in Slice Unit When encoding process and command trigger mode, S/W should set the write number and take care the full condition. Other mode is for Read Only.

Base Address of Bit Stream Register 1

Read/Write Port: 0A1Eh

Default Value: 0000h

Field	Bits	Type	Description

StreamBaseAdr	15:0	RW	Base Address [15:0] of Bit Stream The twenty-two bits of line buffer address in 16-bit unit can address up to 8M bytes SRAM. For Encode mode, S/W will get the JPEG encoded bitstream from this buffer. For Decode mode, S/W will put the encoded bitstream to this buffer.

Base Address of Bit Stream Register 2

Read/Write Port: 0A20h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
StreamBaseAdr	5:0	RW	Base Address [21:16] of Bit Stream

Bit Stream Size Register 1

Read/Write Port: 0A22h

Default Value: 0000h

Field	Bits	Type	Description
StreamSize	15:0	RW	Bitstream Buffer Size [15:0] Maximum buffer size is up to 512 K words.

Bit Stream Size Register 2

Read/Write Port: 0A24h

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
	9:8	RW	Valid Data Occupancy Threshold 00 : the valid data more than 1/16 Bistream Buffer size 01 : the valid data more than 1/8 Bistream Buffer size 10 : the valid data more than 1/4 Bistream Buffer size 11 : the valid data more than 1/2 Bistream Buffer size
-	7:3	-	Reserved
StreamSize	2:0	RW	Bitstream Buffer Size [18:16]

Bit Stream R/W Data Size Register 1

Read/Write Port: 0A26h

Default Value: 0000h

Field	Bits	Type	Description

StreamDataSize	15:0	RW	Bitstream Buffer Read/Write Data Size [15:0] in 16-bit Unit When encoding process, S/W should set the size of moving from the buffer. When decoding process, S/W should set the size of moving to the buffer.

Bit Stream R/W Data Size Register 2

Read/Write Port: 0A28h

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	Reserved
StreamDataSize	2:0	RW	Bitstream Buffer Read/Write Data Size [18:16] in 16-bit Unit

Edge Enhancement Threshold 1

Read/Write Port: 0A2Ah

Default Value: 0000h

Field	Bits	Type	Description
LPWeight	14:10	RW	Lowpass Weight
EdgeEnhTh1	9:0	RW	Default is 60

Edge Enhancement Threshold 2

Read/Write Port: 0A2Ch

Default Value: 0000h

Field	Bits	Type	Description
EdgeEnhWeight	15:11	RW	Default is 8
EdgeEnhTh2	10:0	RW	Default is 80

Luminance Q Table Register 1

Read/Write Port: 0A2Eh

Default Value: 0000h

Field	Bits	Type	Description
LQTable1	15:8	RW	Luminance Quantization Table of Pixel 1 in zig-zag order
LQTable0	7:0	RW	Luminance Quantization Table of Pixel 0 in zig-zag order

Luminance Q Table Register 2~31

Read/Write Port: 0A30h ~ 0A6Dh

Default Value: 0000h

LQTable2 ~ LQTable 63

Chrominance Q Table Register 1

Read/Write Port: 0A6Eh

Default Value: 0000h

Field	Bits	Type	Description
CQTable1	15:8	RW	Chrominance Quantization Table of Pixel 1 in zig-zag order
CQTable0	7:0	RW	Chrominance Quantization Table of Pixel 0 in zig-zag order

Chrominance Q Table Register 2~31

Read/Write Port: 0A70h ~ 0AADh

Default Value: 0000h

CQTable2 ~ CQTable 63

JPEG Codec Fire Register

Read/Write Port: 0AAEh

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
CmdFire	8	RW	Start to Encode or Decode Set 1 to Fire Encode or Decode
-	7:1	-	Reserved
SWRst	0	RW	**S/W Reset** Set '1' to reset the JPEG internal engine

JPEG Engine Status Register

Read/Write Port: 0AB0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
JPEGStatus	4:1	R	Engine Status
OpMode	0	RW	Operation Mode 1 : Encode mode 0 : Decode mode

JPEG Interrupt Status Register

Read/Write Port: 0AB2h

Default Value: 0000h

Field	Bits	Type	Description

-	15:9	-	Reserved
DataThreshold	8	RW	Valid Data Occupancy Threshold (R/W) For Read, 1 : Valid Data exceeds threshold. 0 : Valid Data doesn't exceed threshold. For Write, 1 : clear the flag. 0 : no affect.
BitstreamBufFull	7	R	Bitstream Buffer Full Flag For Encode, 1: Bistream buffer is full and inform S/W to move the bitstream. 0 : Normal condition. For Decode - Debug only.
BitstreamBufEmpty	6	R	Bitstream Buffer Empty Flag For Encode - Debug only. For Decode, 1 : Inform S/W no data in buffer and can send the data for decoding.
LineBufFull	5	R	Line Buffer Full Flag Debug only.
LineBufEmpty	4	R	Line Buffer Empty Flag For Encode and ISP trigger mode, Debug only, report the line buffer status. When this bit is 1, maybe ISP is too slow or line buffer size is too small. For Encode and Command trigger mode, 1 : Inform S/W can send the data to line buffer. 0 : Normal condition. For Decode, Debug only, can check the performance for ISP and Decoder power.
ViolateEncSize	3	RW	Maximum encode size violation Flag For Read, '1' : current total encoded bitstream size violate the user defined maximum size. '0' : not exceed the maximum size. For Write, Set '1' to continue to decode.

			Set '0' to stop to decode.
DecError	2	RW	Decode Error Flag For Read, '1' : Decode error '0' : Decode not error For Write, Set '1' to continue to decode. Set '0' to stop to decode.
EncComp	1	R	JPEG Encode Complete Flag For Read, '1' : JPEG encode complete. '0' : JPEG encode not complete.
DecComp	0	R	JPEG Decode Complete Flag For Read, '1' : JPEG decode complete. '0' : JPEG decode not complete.

Line Buffer Control Register

Read/Write Port: 0AB4h

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	Reserved
EncDataLast	2	RW	Last Encode Data Flag Only when encoding process and command trigger mode is valid. After copy the last data to line buffer, S/W should set the flag to inform H/W the slice is the last encode data.
LBWrEnd	1	RW	Line Buffer Write End Flag (R/W) Only when encoding process and command trigger mode is valid. For Write, After each time copy the last data to line buffer, S/W should set the flag to inform H/W. The flag should set after REG[12] For Read, '0' : H/W already receives the S/W previous update. '1' : H/W doesn't receives the S/W previous update.

LBReset	0	RW	Line Buffer Reset Flag Reset the line buffer read/write pointer.

Valid Line Buffer Register

Read/Write Port: 0AB6h

Default Value: 0000h

Field	Bits	Type	Description
-	15:5	-	Reserved
	4:0	R	When encoding process, S/W can move the size (REG[9] - REG[23]) data to the line buffer.

Bitstream Buffer Control Register

Read/Write Port: 0AB8h

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	Reserved
BitsDataLast	2	R	Last Bitstream Data Flag Only when encoding process and command trigger mode is valid. After copy the last bitstream data to the bitstream buffer, S/W should set the flag to inform H/W.
BitsWrEnd	1	RW	Bitstream Buffer Write End Flag For Write, After each time copy or read the last data to the bitstream buffer, S/W should set the flag to inform H/W. The flag should set after REG[15] For Read, '0' : H/W already receives the S/W previous update. '1' : H/W doesn't receives the S/W previous update.
BitsBufReset	0	R	Bitstream Buffer Reset Flag Reset the line buffer read/write pointer.

Bitstream Buffer Valid Register 1

Read/Write Port: 0ABAh

Default Value: 0000h

Field	Bits	Type	Description
BitsValid	15:0	R	Bitstream Buffer Valid Data Size [15:0] in 16-bits Unit When encoding process, S/W can move the size (REG[25])

			from the bitstream buffer. When decoding process, S/W can move the size (REG[14] - REG[25]) data to the bitstream buffer.

Bitstream Buffer Valid Register 1

Read/Write Port: 0ABAh

Default Value: 0000h

Field	Bits	Type	Description
-	15:3	-	Reserved
BitsValid	2:0	R	Bitstream Buffer Valid Data Size [18:16] in 16-bits Unit

The Number of Huffman Codes of Each Length

Read Port: 0ABEh

Default Value: 0000h

Field	Bits	Type	Description
-	15:14	-	Reserved
DC/AC Talbe	13	R	'0' : DC '1' : AC
Luminance/Chrominance Table	12	R	'0' : Luminance '1' : Chrominance
Huffman Codes of Length i indicator	11:8	R	When set each table, first need to set 0 to reset.
The Number of Huffman Codes of Length i	7:0	R	Please reference T.81 page 40

The DC Value Associated with Each Huffman Code

Read Port: 0AC0h

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
Luminance/Chrominance Table	11	R	'0' : Luminance '1' : Chrominance
Huffman Codes of Length i indicator	10:8	R	When set each table, first need to set 0 to reset.
The Value Associated with Huffman Codes of Length i	7:0	R	Please reference T.81 page 40 Need to send two value simultaneously.

The AC Luminance Value Associated with Each Huffman Code

Read Port: 0AC2h

Default Value: 0000h

Field	Bits	Type	Description
Encode: The Value Associated with Huffman Codes of Length i Decode: Huffman Codes of Length i indicator	15:8	R	Please reference T.81 page 40. Need to send two value simultaneously
Encode: Huffman Codes of Length i indicator Decode: The Value Associated with Huffman Codes of Length i	7:0	R	Please reference T.81 page 40 Need to send two value simultaneously.

The AC Chrominance Value Associated with Each Huffman Code

Read Port: 0AC2h

Default Value: 0000h

Field	Bits	Type	Description
Encode: The Value Associated with Huffman Codes of Length i Decode: Huffman Codes of Length i indicator	15:8	R	Please reference T.81 page 40. Need to send two value simultaneously
Encode: Huffman Codes of Length i indicator Decode: The Value Associated with Huffman Codes of Length i	7:0	R	Please reference T.81 page 40 Need to send two value simultaneously.

10.3.9 MPEG-4 Engine Register

Y Frame Base Address of Encode Buffer 0 Register 1

Read/Write Port: 0C00h

Default Value: 0000h

Field	Bits	Type	Description
EncY0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0.

			Notice: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Encode Buffer 0 Register 2

Read/Write Port: 0C02h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncY0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Frame in 16-bits Unit

U Frame Base Address of Encode Buffer 0 Register 1

Read/Write Port: 0C04h

Default Value: 0000h

Field	Bits	Type	Description
EncU0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Encode Buffer 0 Register 2

Read/Write Port: 0C06h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncU0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Frame in 16-bits Unit

V Frame Base Address of Encode Buffer 0 Register 1

Read/Write Port: 0C08h

Default Value: 0000h

Field	Bits	Type	Description
EncV0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Encode Buffer 0 Register 2

Read/Write Port: 0C0Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncV0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Frame in 16-bits Unit

Notice : When command trigger mode, Only Buffer 0 is valid and Buffer 1 and 2 are not valid. The Buffer 0 is

current original frame.

Y Frame Base Address of Encode Buffer 1 Register 1

Read/Write Port: 0C0Ch

Default Value: 0000h

Field	Bits	Type	Description
EncY1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Encode Buffer 1 Register 2

Read/Write Port: 0C0Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncY1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Frame in 16-bits Unit

U Frame Base Address of Encode Buffer 1 Register 1

Read/Write Port: 0C10h

Default Value: 0000h

Field	Bits	Type	Description
EncU1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Encode Buffer 1 Register 2

Read/Write Port: 0C12h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncU1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Frame in 16-bits Unit

V Frame Base Address of Encode Buffer 1 Register 1

Read/Write Port: 0C14h

Default Value: 0000h

Field	Bits	Type	Description
EncV1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Encode Buffer 1 Register 2

Read/Write Port: 0C16h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncV1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Frame in 16-bits Unit

Y Frame Base Address of Encode Buffer 2 Register 1

Read/Write Port: 0C18h

Default Value: 0000h

Field	Bits	Type	Description
EncY2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Encode Buffer 2 Register 2

Read/Write Port: 0C1Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncY2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for Y Frame in 16-bits Unit

U Frame Base Address of Encode Buffer 2 Register 1

Read/Write Port: 0C1Ch

Default Value: 0000h

Field	Bits	Type	Description
EncU2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Encode Buffer 2 Register 2

Read/Write Port: 0C1Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncU2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for U Frame in 16-bits Unit

V Frame Base Address of Encode Buffer 2 Register 1

Read/Write Port: 0C20h

Default Value: 0000h

Field	Bits	Type	Description
EncV2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Encode Buffer 2 Register 2

Read/Write Port: 0C22h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncV2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for V Frame in 16-bits Unit

Y Reconstructed Frame Base Address of Buffer 0 Register 1

Read/Write Port: 0C24h

Default Value: 0000h

Field	Bits	Type	Description
YR0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Reconstructed Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Reconstructed Frame Base Address of Buffer 0 Register 2

Read/Write Port: 0C26h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
YR0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Reconstructed Frame in 16-bits Unit

U Reconstructed Frame Base Address of Buffer 0 Register 1

Read/Write Port: 0C28h

Default Value: 0000h

Field	Bits	Type	Description
UR0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for U Reconstructed Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Reconstructed Frame Base Address of Buffer 0 Register 2

Read/Write Port: 0C2Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
UR0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Reconstructed Frame in 16-bits Unit

V Reconstructed Frame Base Address of Buffer 0 Register 1

Read/Write Port: 0C2Ch

Default Value: 0000h

Field	Bits	Type	Description
VR0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Reconstructed Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Reconstructed Frame Base Address of Buffer 0 Register 2

Read/Write Port: 0C2Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
VR0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Reconstructed Frame in 16-bits Unit

Notice : When command trigger mode, the Reconstructed frame of Buffer 0 is forward reference frame.

Y Reconstructed Frame Base Address of Buffer 1 Register 1

Read/Write Port: 0C30h

Default Value: 0000h

Field	Bits	Type	Description
YR1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Reconstructed Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Reconstructed Frame Base Address of Buffer 1 Register 2

Read/Write Port: 0C32h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
YR1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Reconstructed Frame in 16-bits Unit

U Reconstructed Frame Base Address of Buffer 1 Register 1

Read/Write Port: 0C34h

Default Value: 0000h

Field	Bits	Type	Description
UR1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for U Reconstructed Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Reconstructed Frame Base Address of Buffer 1 Register 2

Read/Write Port: 0C36h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
UR1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Reconstructed Frame in 16-bits Unit

V Reconstructed Frame Base Address of Buffer 1 Register 1

Read/Write Port: 0C38h

Default Value: 0000h

Field	Bits	Type	Description
VR1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Reconstructed Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Reconstructed Frame Base Address of Buffer 1 Register 2

Read/Write Port: 0C3Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
VR1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Reconstructed Frame in 16-bits Unit

Notice : When command trigger mode, the Restructured Frame of Buffer 1 is reconstructed frame.

DC Prediction Buffer Base Address Register 1

Read/Write Port: 0C3Ch

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Temporal Buffer Base Address [15:0] of DC Prediction in 16-bits Unit Temporal storage base linear address for DC prediction. *Notice*: The size of buffer is (Frame_Width / 16) * 48 bits

DC Prediction Buffer Base Address Register 2

Read/Write Port: 0C3Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	Temporal Buffer Base Address [21:16] of DC Prediction in 16-bits Unit

AC Prediction Buffer Base Address Register 1

Read/Write Port: 0C40h

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Temporal Buffer Base Address [15:0] of AC Prediction in 16-bits Unit Temporal storage base linear address for AC prediction. *Notice*: The size of buffer is (Frame_Width / 16) * 96 bits

AC Prediction Buffer Base Address Register 2

Read/Write Port: 0C42h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	Temporal Buffer Base Address [21:16] of AC Prediction in 16-bits Unit

VLC Buffer Base Address Register 1

Read/Write Port: 0C44h

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	VLC Buffer Base Address [15:0] in 16-bits Unit

VLC Buffer Base Address Register 2

Read/Write Port: 0C46h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	VLC Buffer Base Address [21:16] in 16-bits Unit

VLC Buffer Length Register

Read/Write Port: 0C48h

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	VLC Buffer Length [15:0] in 16-bits Unit *Limitation*: The maximum length is less and not equal to 64K words.

Header Buffer Base Address Register 1

Read/Write Port: 0C4Ah

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Header Buffer Base Address [15:0] in 16-bits Unit Each frame header is 64 bits. *Notice*: The size is 64 x 32 bits.

Header Buffer Base Address Register 2

Read/Write Port: 0C4Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	Header Buffer Base Address [21:16] in 16-bits Unit

Encode Frame Width Register

Read/Write Port: 0C4Eh

Default Value: 0000h

Field	Bits	Type	Description
EncYPitch	15:7	RW	Encode Y Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
EncFrameWidth	5:0	RW	Frame Width [5:0] in 128-bits Unit The frame width must be times of 16.

Encode Frame Height Register

Read/Write Port: 0C50h

Default Value: 0000h

Field	Bits	Type	Description
EncUVPitch	15:7	RW	Encode UV Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
EncFrameHeight	5:0	RW	Frame Height [5:0] in 128-bits Unit The frame height must be times of 16.

VOP Time Code Register

Read/Write Port: 0C52h

Default Value: 0000h

Field	Bits	Type	Description
VOPIncRes	15:0	RW	VOP Time Increment Resolution of Time Code Information [15:0] This is a 16-bit unsigned integer that indicates the number of evenly spaced subintervals, called ticks, within one modulo time. One modulo time represents the fixed interval of one second. The value zero is forbidden.

Fixed VOP Time Code Register

Read/Write Port: 0C54h

Default Value: 0000h

Field	Bits	Type	Description
FixVOPIncRes	15:0	RW	Fixed VOP Time Increment of Time Code Information [15:0] This value represents the number of ticks between two successive VOPs in the display order. The length of a tick is given by vop_time_increment_resolution. It can take a value in the range between 0 and VOPIncRes.

Encoding Parameter Register 1

Read/Write Port: 0C56h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
TCodeBitNum	12:8	RW	**Encode Time Code Bit Number** The number of bits representing the value is calculated as the minimum number of unsigned integer bits required to represent the above range.
-	7:5	-	Reserved
SrcFormat	4:2	RW	**Source format** Only valid for short header is turn on. 000 : Reserved 001 : sub-QCIF (128 x 96) 010 : QCIF (176x144) 011 : CIF (352x288) 100 : 4CIF (704x576) 100 ~111 are forbidden.
EnACPred	1	RW	**AC_pred_enable** Always set to 0.
EnShortHead	0	RW	**Short header** When this flag set to 1, the encoded bitstream is compatiable with H.263.

Encoding Parameter Register 2

Read/Write Port: 0C58h

Default Value: 0000h

Field	Bits	Type	Description
	15:7	RW	Key Frame Period Period between key frames (I frame).
	6	RW	SubPixel Enable Only for debug. Normal condition the flag is always turn on.
	5	RW	4MV Enable When short header is set, this flag must be 0.
	4	RW	Restricted MV Enable When short header is set, this flag must be 1.
	3:1	RW	Intra dc vlc thr 000: Use Intra DC VLC for entire VOP 001: Switch to Intra AC VLC at running Qp >=13 010: Switch to Intra AC VLC at running Qp >=15 011: Switch to Intra AC VLC at running Qp >=17

			100: Switch to Intra AC VLC at running Qp >=19 101: Switch to Intra AC VLC at running Qp >=21 110: Switch to Intra AC VLC at running Qp >=23 111: Use Intra AC VLC for entire VOP When short header is set, the value must be 0.
	0	RW	MQ trigger mode '0' : MicroP will do rate control and calculate mquant value to Codec. '1' : Send by Drivers. The mquant value is given by Command Register.

Encoding Parameter Register 3

Read/Write Port: 0C5Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
	11:0	RW	Intra mode tolerance Defalut value is 512.

Encoding Parameter Register 4

Read/Write Port: 0C5Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
	11:0	RW	4MV mode tolerance Defalut value is 129.

Encoding Parameter Register 5

Read/Write Port: 0C5Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
	11:0	RW	Zero MV tolerance Defalut value is 129.

Safe Register 1

Read/Write Port: 0C60h

Default Value: 0000h

Field	Bits	Type	Description
-	15	RW	**VGA Size Flag** Decode Only When the decoding size is larger than 640x480, the flag must set to 1.
	14:11	RW	**Macroblock Bit Number** Decode Only Ex. 48 x 48 => 9 MB => 4 bits 352 x 288 => 396 MB => 9 bits
	10:5	RW	**Skip Frame Number** Encode Only. When Command mode, (a). MPEG 4 mode and each frame reset Ex. Reg[0c50] = 30, Reg[0c52] = 1, Frmae0 => set 0, Frmae1 => set 1, Frmae2 => set 2, ……. Frmae30 => set 30, Frame31 => set 1, …….. (b). MPEG 4 mode and without each frame reset Ex. Reg[0c50] = 30, Reg[0c52] = 1, Frmae0 => set 0, Frmae1 => set 1, Frmae2 => set 1 ……. Frmae30 => set 1, Frame31 => set 1, …….. (c). H.263 mode and don't care reset Ex. Reg[0c50] = 30, Reg[0c52] = 1, Frmae0 => set 0, Frmae1 => set 1, Frmae2 => set 2, ……. Frmae30 => set 30, Frame31 => set 1, …….. When ISP trigger mode, Must set for the first frame. Most case set to zero.
	4:0	RW	**GOB Incremental Number** Encode Only.

			Defalut value is 1

Safe Register 2

Read/Write Port: 0C62h

Default Value: 0000h

Field	Bits	Type	Description
	15:4	RW	**BMaxMBLen** Maximum bits of one MB Default value is 1800
	3:0	RW	**Debug Info Selection** 0000 : Arbiter 0001 : ME0 0010 : ME1 0011 : VLC 0100 : TC0

Safe Register 3

Read/Write Port: 0C64h

Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
	10:8	RW	Gate Clock Safe Register B(0) => X1CLK (ME), B(1) => X2CLK (TC), B(2) => X3CLK (VLC), 0 : only frame level 1 : MB level
-	7:2	-	Reserved
	1:0	RW	ISP Buf Number The number between ISP and MPEG. Defalut is 3

Interrupt Control Register

Read/Write Port: 0C66h

Default Value: 0000h

Field	Bits	Type	Description
-	15:4	-	Reserved
	3	RW	Header Buffer Full Interrupt Enable '0' : Disable

			'1' : Enable
	2	RW	VLC Buffer Full Interrupt Enable '0' : Disable '1' : Enable
	1	RW	MPEG Encode Sequence Complete Interrupt Enable '0' : Disable '1' : Enable
	0	RW	MPEG Encode Frame Complete Interrupt Enable '0' : Disable '1' : Enable

Encode Control Register

Read/Write Port: 0C68h

Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
	0	RW	Clear Header Buffer Flag '1' : When S/W finish to get the header information, should set the flag to clear the header buffer flag. '0' : not affect

VLC Read Data Size Register

Read/Write Port: 0C6Ah

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	VLC Buffer Read Data Size [15:0] in 16-bits Unit

Fire Command Register

Read/Write Port: 0C6Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
	8	RW	Pitcture type Current frame encode picture type. Only command trigger mode is valid.
	7:3	RW	Mquant value Value is 1 ~31. Only Mquant trigger mode is set to 1.
	2	RW	Force refresh key frame

			0 : Normal mode 1 : Force to update I frame and re-accumulate refresh counter. Engine maybe delay one or two frame. Only ISP trigger mode is valid
	1:0	RW	Trigger Mode 00: Encoding Trigger by ISP 01: Encoding Trigger by Command 10: Stop encoding 11: Reversed

Y Frame Base Address of Decode Buffer 0 Register 1

Read/Write Port: 0C6Eh

Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Decode Buffer 0 Register 2

Read/Write Port: 0C70h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Frame in 16-bits Unit

U Frame Base Address of Decode Buffer 0 Register 1

Read/Write Port: 0C72h

Default Value: 0000h

Field	Bits	Type	Description
U0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Decode Buffer 0 Register 2

Read/Write Port: 0C74h

Default Value: 0000h

Field	Bits	Type	Description

-	15:6	-	Reserved
U0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Frame in 16-bits Unit

V Frame Base Address of Decode Buffer 0 Register 1

Read/Write Port: 0C76h

Default Value: 0000h

Field	Bits	Type	Description
V0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Decode Buffer 0 Register 2

Read/Write Port: 0C78h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Frame in 16-bits Unit

Y Frame Base Address of Decode Buffer 1 Register 1

Read/Write Port: 0C7Ah

Default Value: 0000h

Field	Bits	Type	Description
Y1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Decode Buffer 1 Register 2

Read/Write Port: 0C7Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Frame in 16-bits Unit

U Frame Base Address of Decode Buffer 1 Register 1

Read/Write Port: 0C7Eh

Default Value: 0000h

Field	Bits	Type	Description
U1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1.

			Notice: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Decode Buffer 1 Register 2

Read/Write Port: 0C80h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Frame in 16-bits Unit

V Frame Base Address of Decode Buffer 1 Register 1

Read/Write Port: 0C82h

Default Value: 0000h

Field	Bits	Type	Description
V1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Decode Buffer 1 Register 2

Read/Write Port: 0C84h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Frame in 16-bits Unit

Y Frame Base Address of Decode Buffer 2 Register 1

Read/Write Port: 0C86h

Default Value: 0000h

Field	Bits	Type	Description
Y2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Decode Buffer 2 Register 2

Read/Write Port: 0C88h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for Y Frame in 16-bits Unit

U Frame Base Address of Decode Buffer 2 Register 1

Read/Write Port: 0C8Ah

Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Decode Buffer 2 Register 2

Read/Write Port: 0C8Ch

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for U Frame in 16-bits Unit

V Frame Base Address of Decode Buffer 2 Register 1

Read/Write Port: 0C8Eh

Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Decode Buffer 2 Register 2

Read/Write Port: 0C90h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for V Frame in 16-bits Unit

Decode Frame Width Register

Read/Write Port: 0C92h

Default Value: 0000h

Field	Bits	Type	Description
DecYPitch	15:7	RW	Decode Y Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
DecFrameWidth	5:0	RW	Frame Width [5:0] in 128-bits Unit The frame width must be times of 16.

Decode Frame Height Register

Read/Write Port: 0C94h

Default Value: 0000h

Field	Bits	Type	Description
DecUVPitch	15:7	RW	Decode UV Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
DecFrameHeight	5:0	RW	Frame Height [5:0] in 128-bits Unit The frame height must be times of 16.

Special function Register

Read/Write Port: 0C96h

Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
	12:8	RW	Decode Time Code Bit Number The number of bits representing the value is calculated as the minimum number of unsigned integer bits required to represent the above range.
-	7	-	Reserved
	6	W	MPEG Half Rate Flag '0' : Disable '1' : Enable Write Only.
	5	W	MPEG Skip One Frame '0' : No Affect '1' : skip one frame Write Only.
	4	W	MPEG Add One Frame '0' : No Affect '1' : add one frame Write Only.
-	3	RW	Deblocking filter turn on flag '0' : On '1' : Off
	2	RW	MPEG Decode Short Header '0' : Disable '1' : Enable
	1	RW	MPEG Capture Write Interrupt Enable

			'0' : Disable '1' : Enable
	0	RW	MPEG Decode Complete Interrupt Enable '0' : Disable '1' : Enable

Command and Data Buffer Start Address Register 1

Read/Write Port: 0C98h

Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Command and Data Buffer Start Address[15:0] S/W will prepare the decoded data in the data buffer. This is also fire command. When S/W finish to set the register, H/W will start to issue request to get the data.

Command and Data Buffer Start Address Register 2

Read/Write Port: 0C9Ah

Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
			Frame Buffer Selector This flag is used to identify which one frame buffer had been selected to decode. *Notice* : S/W should set the REG[0E2E]and REG[0E30] sequentially.
-	7:6	-	Reserved
	5:0	RW	Command and Data Buffer Start Address[21:16] S/W will prepare the decoded data in the data buffer. This is also fire command. When S/W finish to set the register, H/W will start to issue request to get the data.

Y Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0C9Ch

Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Deblocking Buffer 0 Register 2

Read/Write Port: 0C9Eh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Frame in 16-bits Unit

U Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0CA0h

Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer0 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Deblocking Buffer 0 Register 2

Read/Write Port: 0CA2h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Frame in 16-bits Unit

V Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0CA4h

Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Deblocking Buffer 0 Register 2

Read/Write Port: 0CA6h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Frame in 16-bits Unit

Y Frame Base Address of Deblocking Buffer 1 Register 1

Read/Write Port: 0CA8h

Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Deblocking Buffer 1 Register 2

Read/Write Port: 0CAAh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Frame in 16-bits Unit

U Frame Base Address of Deblocking Buffer 1 Register 1

Read/Write Port: 0CACh

Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer1 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Deblocking Buffer 1 Register 2

Read/Write Port: 0CAEh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Frame in 16-bits Unit

V Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0CB0h

Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Deblocking Buffer 1 Register 2

Read/Write Port: 0CB2h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Frame in 16-bits Unit

Y Frame Base Address of Deblocking Buffer 2 Register 1

Read/Write Port: 0CB4h

Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Deblocking Buffer 2 Register 2

Read/Write Port: 0CB6h

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for Y Frame in 16-bits Unit

U Frame Base Address of Deblocking Buffer 2 Register 1

Read/Write Port: 0CB8h

Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer2 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Deblocking Buffer 2 Register 2

Read/Write Port: 0CBAh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for U Frame in 16-bits Unit

V Frame Base Address of Deblocking Buffer 2 Register 1

Read/Write Port: 0CBCh

Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for V Frame in 16-bits Unit

			V Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Deblocking Buffer 2 Register 2

Read/Write Port: 0CBEh

Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for V Frame in 16-bits Unit

Deblocking Process Thresholds Setting Register

Read/Write Port: 0CC0h

Default Value: 0602h

Field	Bits	Type	Description
-	15:12	-	Reserved
DBThresholdB	11:8	RW	Deblocking threshold B
DBThresholdA	7:0	RW	Deblocking threshold A

VLC Buffer Valid Size Register

Read/Write Port: 0CC2h

Default Value: 0000h

Field	Bits	Type	Description
VLCBufValid	15:0	RW	Indicate how much valid data in VLC Buffer.

Encode Status Register 0

Read/Write Port: 0CC4h

Default Value: 0000h

Field	Bits	Type	Description
-	15:14	-	Reserved
	13	R	MPEG Half Rate Flag
	12	R	MPEG Skip One Frame
	11	R	MPEG Add One Frame
	10	R	Capture In Status '1' : One Frame In
	9:4	R	Valid Header Number The number of header is valid to read.
	3	R	Header Buffer Full Flag '0' : Not full

			'1' : Full
	2	R	VLC Buffer Full Flag '0' : Not full '1' : Full
	1	R	MPEG Encode Sequence Complete Flag '0' : Busy '1' : End
	0	R	MPEG Encode Frame Complete Flag '0' : Busy '1' : End

Encode Status Register 1

Read/Write Port: 0CC6h

Default Value: 0000h

Field	Bits	Type	Description
	15	R	Re-Construct Req
	14	R	VLD Stall
	13	R	Decode Zero Block
	12	R	Decoder Block End in Q
	11	R	Decode Write Enable in Q
	10	R	VLD Scan Direction
	9	R	TC Idle
	8	R	DC AC Prediction Rdy
	7	R	Block End
	6	R	Q to Mquant Ack
	5	R	AC Rdy
	4	R	DC Rdy
	3	R	DCT Rdy
	2	R	TC MC RF Valid
	1	R	TC Cur RF Valid
	0	R	ME Rdy

Decode Status Register

Read/Write Port: 0CC8h

Default Value: 0000h

Field	Bits	Type	Description
	15:14	R	Debug Info Encoder FSM Stauts

	13	R	MPEG Decode Engine Status '0' : Idle '1' : Busy
	12	R	Fire Queue Empty '0' : Empty '1' : Full
	11:10	R	Current Frame Buffer Indicator Indicate current decoding frame buffer
	9:6	R	Current Frame Decode Error Flag "0000" : No Error Others : Error
	5:4	R	Finished Frame Buffer Indicator Indicate which frame buffer has finished to decode
	3:0	R	Finished Frame Decode Error Flag "0000" : No Error Others : Error

Decode Read Back Register 0

Read/Write Port: 0CCAh

Default Value: 0000h

Field	Bits	Type	Description
	15	R	Decode Status (0)
	14:12	R	VLC OUT FSM
	11:8	R	VLC TOP FSM
	7:4	R	MBD FSM
	3	R	VLCOverFlow
	2	R	VLCStall
	1	R	UsedBitsRdy
	0	R	FrmSumRdy

Decode Read Back Register 1

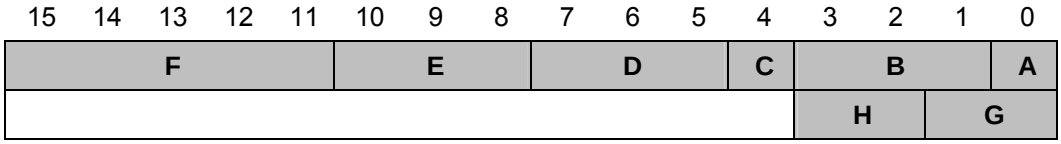
Read/Write Port: 0CCCh

Default Value: 0000h

Field	Bits	Type	Description
	15	R	DeStatus(1)
	14:11	R	ME Top FSM Status
	10:8	R	Ref FSM Status
	7:6	R	Org FSM Status

	5	R	Mask Rdy
	4	R	ME Rdy
	3:0	R	VLD Status

VOP_Header Data Format for Decoding Process



A. vop_coding_type

0 : I frame, 1 : P frame

B. vop_r_size[2:0]

vop_r_size = vop_fcode_forward - 1

C. vop_rounding_type

D. vop_start_bits[2:0]

indicate H/W should discard bit counts to decode

E. intra_dc_vlc_thr[2:0]

F. vop_quant[4:0]

G. vop_forward_buf[1:0]

forward reference buffer selector

H. vop_current_buf[1:0]

current decoding buffer selector

Decoding Data sent to H/W

VOP Header Data

Data

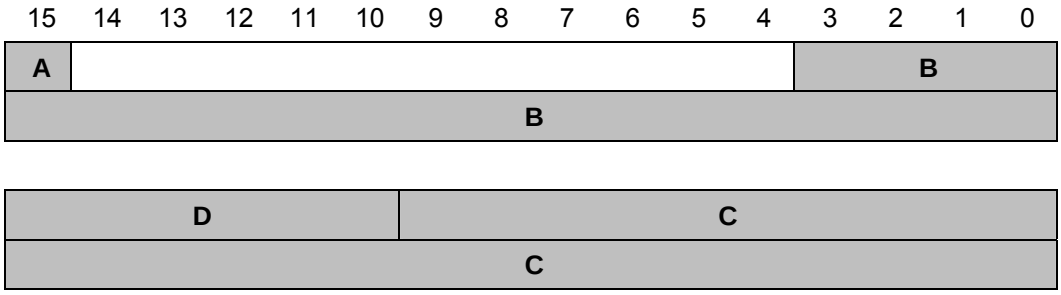
: :

: :

Data

VOP End Data (0x000001B6)

Encoding Header Data Format



A. Discard Frame

1: This frame should be discard.

B. Total Frame Bits

C. Time Code for AV sync

D. Skip Frame Number