Glamo3365 MPEG4 Engine

Released

Rev. 1.0

June 22, 2005

MPEG Engine

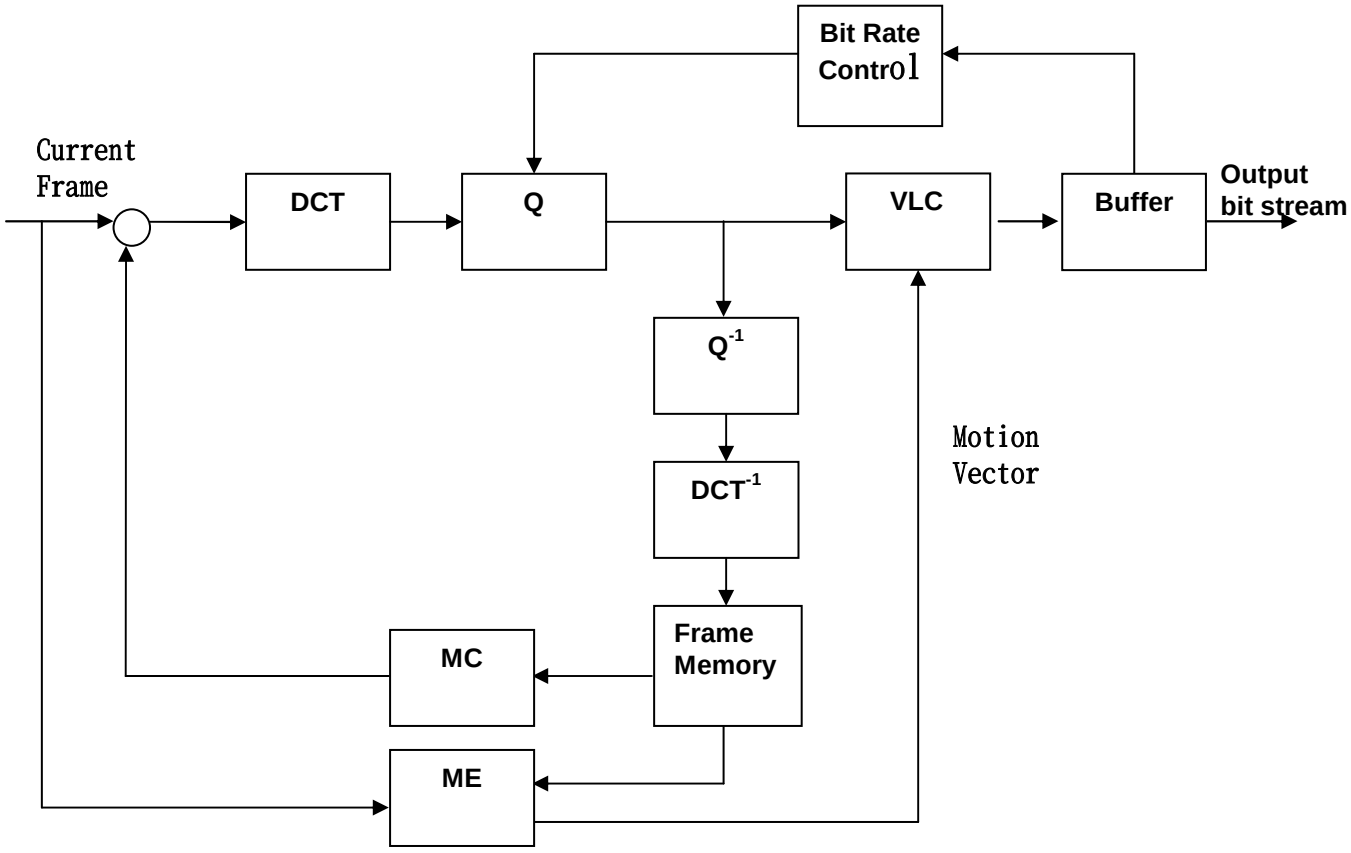
Support Formats

The Glamo3365 MPEG codec is based on the ISO/IEC 14496-2 (MPEG-4) simple profile standard. The maximum size can up to CIF (352x288) 30 fps. Glamo3365 also supports the VOP with short header (H.263). Glamo3365 hardware decoder and encoder are fully pipelined architecture. It supports to VOP layer, the baseband only need to packaging the file header and AV synchronization for MPEG encoding and parsing the header for MPEG decoding.

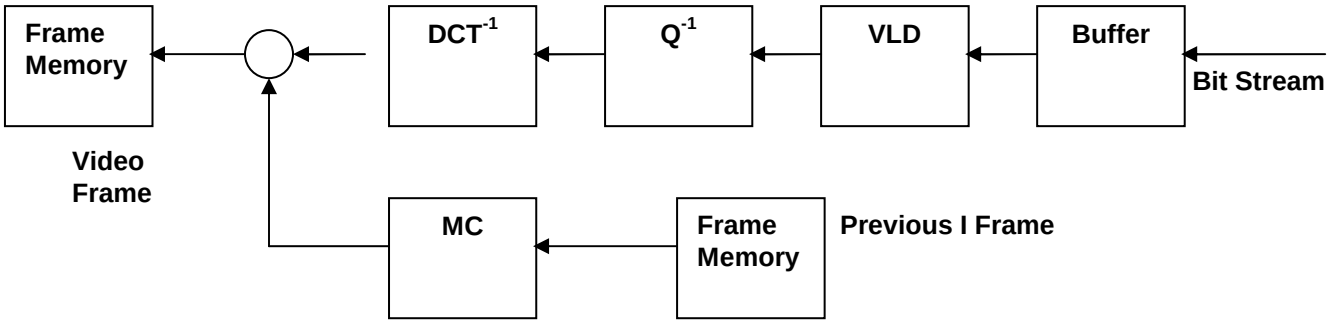
MPEG Codec Architecture

The motion estimation of Glamo3365 supports full search algorithm with ±16 search range in both X and Y direction. The resolution of motion vector is half-pixel. Glamo3365 supports both CBR (constant bit rate) and VBR (variable bit rate). Glamo3365 also provides a hardware rate control scheme. The bit rate can be dynamically changed according to the complexity of the frame scene. With this scheme, the encoded video quality can be improved comparing to the video without rate control with same bit rate.

MPEG Encode Architecture



MPEG Decoder Architecture:



Handshaking with ISP

In the MPEG encoding mode, MPEG encoder receives the video data from ISP module with triple buffer scheme. The handshaking control is done by hardware, baseband CPU do not need to take the flow control efforts to reduce the CPU loading. Baseband CPU only need to read back the encoded bit-stream and package the header of MPEG file format. In the MPEG decoding mode, MPEG decoder provided the decoded video datat to ISP module every frame. And then software flips the video to LCD display according to the time stamp.

Audio/Video Synchronization

Glamo3365 provides a hardware audio/video synchronization scheme to let the baseband CPU handles the AV sync task very easy.

Deblocking filter for post-processing

The MPEG standard divides video to 8x8 blocks and transforms each block by DCT. After DCT transformation, the transformed coefficients are quantized and then entropy coded. According to the different bit rates requirement, the codec adjusts the quantization step. When at the high bit rate, the codec preserves more low and high frequency coefficients. However, at the lower bit rate, most high frequency are discard and the relationship between adjacent blocks is loss. This block-based approach leads to noticeable blocking artifact, that is artificial discontinuities appearing between the block boundaries. The Deblocking filter can be used to help reduce the appearance of block like artifacts that appear in highly compressed video streams.

3GPP File Format

Glamo3365 also provides the sample code of 3GPP file format packaging and parsing.

MPEG Encoding Process

The MPEG encoding process is as follows:

1. Initial the sensor and ISP module to video recording mode.
2. Initial the MPEG encoding related register.
3. Fire ISP for video recording.
4. Read back the encoded bitstream
5. Append the header and synchronous with audio bit-stream to became 3GPP file format.

MPEG Decoding Process

The MPEG decoding process is as follows:

2. Initial ISP module to video playback mode.
3. Initial the MPEG decoding related register.
4. De-multiplex the audio and video bit-streams
5. Send video bitstream to frame buffer for decoding
6. Fire ISP for mpeg decode mode
7. Show the decoded video on the LCD display

Register Defination

Y Frame Base Address of Encode Buffer 0 Register 1

Read/Write Port: 0C00h
Default Value: 0000h

Field	Bits	Type	Description
EncY0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Encode Buffer 0 Register 2

Read/Write Port: 0C02h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncY0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Frame in 16-bits Unit

U Frame Base Address of Encode Buffer 0 Register 1

Read/Write Port: 0C04h
Default Value: 0000h

Field	Bits	Type	Description
EncU0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Encode Buffer 0 Register 2

Read/Write Port: 0C06h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncU0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Frame in 16-bits Unit

V Frame Base Address of Encode Buffer 0 Register 1

Read/Write Port: 0C08h
Default Value: 0000h

Field	Bits	Type	Description
EncV0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Encode Buffer 0 Register 2

Read/Write Port: 0C0Ah
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncV0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Frame in 16-bits Unit

Notice : When command trigger mode, Only Buffer 0 is valid and Buffer 1 and 2 are not valid. The Buffer 0 is current original frame.

Y Frame Base Address of Encode Buffer 1 Register 1

Read/Write Port: 0C0Ch
Default Value: 0000h

Field	Bits	Type	Description
EncY1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Encode Buffer 1 Register 2

Read/Write Port: 0C0Eh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncY1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Frame in 16-bits Unit

U Frame Base Address of Encode Buffer 1 Register 1

Read/Write Port: 0C10h
Default Value: 0000h

Field	Bits	Type	Description
EncU1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Encode Buffer 1 Register 2

Read/Write Port: 0C12h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncU1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Frame in 16-bits Unit

V Frame Base Address of Encode Buffer 1 Register 1

Read/Write Port: 0C14h
Default Value: 0000h

Field	Bits	Type	Description
EncV1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Encode Buffer 1 Register 2

Read/Write Port: 0C16h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncV1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Frame in 16-bits Unit

Y Frame Base Address of Encode Buffer 2 Register 1

Read/Write Port: 0C18h
Default Value: 0000h

Field	Bits	Type	Description
EncY2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Encode Buffer 2 Register 2

Read/Write Port: 0C1Ah
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncY2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for Y Frame in 16-bits Unit

U Frame Base Address of Encode Buffer 2 Register 1

Read/Write Port: 0C1Ch
Default Value: 0000h

Field	Bits	Type	Description
EncU2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Encode Buffer 2 Register 2

Read/Write Port: 0C1Eh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncU2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for U Frame in 16-bits Unit

V Frame Base Address of Encode Buffer 2 Register 1

Read/Write Port: 0C20h
Default Value: 0000h

Field	Bits	Type	Description
EncV2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Encode Buffer 2 Register 2

Read/Write Port: 0C22h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
EncV2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for V Frame in 16-bits Unit

Y Reconstructed Frame Base Address of Buffer 0 Register 1

Read/Write Port: 0C24h
Default Value: 0000h

Field	Bits	Type	Description
YR0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Reconstructed Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Reconstructed Frame Base Address of Buffer 0 Register 2

Read/Write Port: 0C26h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
YR0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Reconstructed Frame in 16-bits Unit

U Reconstructed Frame Base Address of Buffer 0 Register 1

Read/Write Port: 0C28h
Default Value: 0000h

Field	Bits	Type	Description
UR0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for U Reconstructed Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Reconstructed Frame Base Address of Buffer 0 Register 2

Read/Write Port: 0C2Ah
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
UR0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Reconstructed Frame in 16-bits Unit

V Reconstructed Frame Base Address of Buffer 0 Register 1

Read/Write Port: 0C2Ch
Default Value: 0000h

Field	Bits	Type	Description
VR0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Reconstructed Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Reconstructed Frame Base Address of Buffer 0 Register 2

Read/Write Port: 0C2Eh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
VR0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Reconstructed Frame in 16-bits Unit

Notice : When command trigger mode, the Reconstructed frame of Buffer 0 is forward reference frame.

Y Reconstructed Frame Base Address of Buffer 1 Register 1

Read/Write Port: 0C30h
Default Value: 0000h

Field	Bits	Type	Description
YR1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Reconstructed Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Reconstructed Frame Base Address of Buffer 1 Register 2

Read/Write Port: 0C32h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
YR1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Reconstructed Frame in 16-bits Unit

U Reconstructed Frame Base Address of Buffer 1 Register 1

Read/Write Port: 0C34h
Default Value: 0000h

Field	Bits	Type	Description
UR1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for U Reconstructed Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Reconstructed Frame Base Address of Buffer 1 Register 2

Read/Write Port: 0C36h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
UR1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Reconstructed Frame in 16-bits Unit

V Reconstructed Frame Base Address of Buffer 1 Register 1

Read/Write Port: 0C38h
Default Value: 0000h

Field	Bits	Type	Description
VR1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Reconstructed Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Reconstructed Frame Base Address of Buffer 1 Register 2

Read/Write Port: 0C3Ah
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
VR1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Reconstructed Frame in 16-bits Unit

Notice : When command trigger mode, the Restructured Frame of Buffer 1 is reconstructed frame.

DC Prediction Buffer Base Address Register 1

Read/Write Port: 0C3Ch
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Temporal Buffer Base Address [15:0] of DC Prediction in 16-bits Unit Temporal storage base linear address for DC prediction. *Notice*: The size of buffer is (Frame_Width / 16) * 48 bits

DC Prediction Buffer Base Address Register 2

Read/Write Port: 0C3Eh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	Temporal Buffer Base Address [21:16] of DC Prediction in 16-bits Unit

AC Prediction Buffer Base Address Register 1

Read/Write Port: 0C40h
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Temporal Buffer Base Address [15:0] of AC Prediction in 16-bits Unit Temporal storage base linear address for AC prediction. *Notice*: The size of buffer is (Frame_Width / 16) * 96 bits

AC Prediction Buffer Base Address Register 2

Read/Write Port: 0C42h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	Temporal Buffer Base Address [21:16] of AC Prediction in 16-bits Unit

VLC Buffer Base Address Register 1

Read/Write Port: 0C44h
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	VLC Buffer Base Address [15:0] in 16-bits Unit

VLC Buffer Base Address Register 2

Read/Write Port: 0C46h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	VLC Buffer Base Address [21:16] in 16-bits Unit

VLC Buffer Length Register

Read/Write Port: 0C48h
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	VLC Buffer Length [15:0] in 16-bits Unit *Limitation*: The maximum length is less and not equal to 64K words.

Header Buffer Base Address Register 1

Read/Write Port: 0C4Ah
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Header Buffer Base Address [15:0] in 16-bits Unit Each frame header is 64 bits. *Notice*: The size is 64 x 32 bits.

Header Buffer Base Address Register 2

Read/Write Port: 0C4Ch
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
	5:0	RW	Header Buffer Base Address [21:16] in 16-bits Unit

Encode Frame Width Register

Read/Write Port: 0C4Eh
Default Value: 0000h

Field	Bits	Type	Description
EncYPitch	15:7	RW	Encode Y Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
EncFrameWidth	5:0	RW	Frame Width [5:0] in 128-bits Unit The frame width must be times of 16.

Encode Frame Height Register

Read/Write Port: 0C50h
Default Value: 0000h

Field	Bits	Type	Description
EncUVPitch	15:7	RW	Encode UV Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
EncFrameHeight	5:0	RW	Frame Height [5:0] in 128-bits Unit The frame height must be times of 16.

VOP Time Code Register

Read/Write Port: 0C52h
Default Value: 0000h

Field	Bits	Type	Description
VOPIncRes	15:0	RW	VOP Time Increment Resolution of Time Code Information [15:0] This is a 16-bit unsigned integer that indicates the number of evenly spaced subintervals, called ticks, within one modulo time. One modulo time represents the fixed interval of one second. The value zero is forbidden.

Fixed VOP Time Code Register

Read/Write Port: 0C54h
Default Value: 0000h

Field	Bits	Type	Description
FixVOPIncRes	15:0	RW	Fixed VOP Time Increment of Time Code Information [15:0] This value represents the number of ticks between two successive VOPs in the display order. The length of a tick is given by vop_time_increment_resolution. It can take a value in the range between 0 and VOPIncRes.

Encoding Parameter Register 1

Read/Write Port: 0C56h
Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
TCodeBitNum	12:8	RW	**Encode Time Code Bit Number** The number of bits representing the value is calculated as the minimum number of unsigned integer bits required to represent the above range.
-	7:5	-	Reserved
SrcFormat	4:2	RW	**Source format**

			Only valid for short header is turn on. 000 : Reserved 001 : sub-QCIF (128 x 96) 010 : QCIF (176x144) 011 : CIF (352x288) 100 : 4CIF (704x576) 100 ~111 are forbidden.
EnACPred	1	RW	**AC_pred_enable** Always set to 0.
EnShortHead	0	RW	**Short header** When this flag set to 1, the encoded bitstream is compatiable with H.263.

Encoding Parameter Register 2

Read/Write Port: 0C58h
Default Value: 0000h

Field	Bits	Type	Description
	15:7	RW	Key Frame Period Period between key frames (I frame).
	6	RW	SubPixel Enable Only for debug. Normal condition the flag is always turn on.
	5	RW	4MV Enable When short header is set, this flag must be 0.
	4	RW	Restricted MV Enable When short header is set, this flag must be 1.
	3:1	RW	Intra dc vlc thr 000: Use Intra DC VLC for entire VOP 001: Switch to Intra AC VLC at running Qp >=13 010: Switch to Intra AC VLC at running Qp >=15 011: Switch to Intra AC VLC at running Qp >=17 100: Switch to Intra AC VLC at running Qp >=19 101: Switch to Intra AC VLC at running Qp >=21 110: Switch to Intra AC VLC at running Qp >=23 111: Use Intra AC VLC for entire VOP When short header is set, the value must be 0.
	0	RW	MQ trigger mode '0' : MicroP will do rate control and calculate mquant value to Codec. '1' : Send by Drivers. The mquant value is given by Command Register.

Encoding Parameter Register 3

Read/Write Port: 0C5Ah
Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
	11:0	RW	Intra mode tolerance Defalut value is 512.

Encoding Parameter Register 4

Read/Write Port: 0C5Ch
Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved

	11:0	RW	4MV mode tolerance Defalut value is 129.

Encoding Parameter Register 5

Read/Write Port: 0C5Eh
Default Value: 0000h

Field	Bits	Type	Description
-	15:12	-	Reserved
	11:0	RW	Zero MV tolerance Defalut value is 129.

Safe Register 1

Read/Write Port: 0C60h
Default Value: 0000h

Field	Bits	Type	Description
-	15	RW	**VGA Size Flag** Decode Only When the decoding size is larger than 640x480, the flag must set to 1.
	14:11	RW	**Macroblock Bit Number** Decode Only Ex. 48 x 48 => 9 MB => 4 bits 352 x 288 => 396 MB => 9 bits
	10:5	RW	**Skip Frame Number** Encode Only. When Command mode, (a). MPEG 4 mode and each frame reset Ex. Reg[0c50] = 30, Reg[0c52] = 1, Frmae0 => set 0, Frmae1 => set 1, Frmae2 => set 2, ……. Frmae30 => set 30, Frame31 => set 1, …….. (b). MPEG 4 mode and without each frame reset Ex. Reg[0c50] = 30, Reg[0c52] = 1, Frmae0 => set 0, Frmae1 => set 1, Frmae2 => set 1 ……. Frmae30 => set 1, Frame31 => set 1, …….. (c). H.263 mode and don't care reset Ex. Reg[0c50] = 30, Reg[0c52] = 1, Frmae0 => set 0, Frmae1 => set 1, Frmae2 => set 2, ……. Frmae30 => set 30, Frame31 => set 1, …….. When ISP trigger mode,

			Must set for the first frame. Most case set to zero.
	4:0	RW	**GOB Incremental Number** Encode Only. Defalut value is 1

Safe Register 2

Read/Write Port: 0C62h
Default Value: 0000h

Field	Bits	Type	Description
	15:4	RW	**BMaxMBLen** Maximum bits of one MB Default value is 1800
	3:0	RW	**Debug Info Selection** 0000 : Arbiter 0001 : ME0 0010 : ME1 0011 : VLC 0100 : TC0

Safe Register 3

Read/Write Port: 0C64h
Default Value: 0000h

Field	Bits	Type	Description
-	15:11	-	Reserved
	10:8	RW	Gate Clock Safe Register B(0) => X1CLK (ME), B(1) => X2CLK (TC), B(2) => X3CLK (VLC), 0 : only frame level 1 : MB level
-	7:2	-	Reserved
	1:0	RW	ISP Buf Number The number between ISP and MPEG. Defalut is 3

Interrupt Control Register

Read/Write Port: 0C66h
Default Value: 0000h

Field	Bits	Type	Description
-	15:4	-	Reserved
	3	RW	Header Buffer Full Interrupt Enable '0' : Disable '1' : Enable
	2	RW	VLC Buffer Full Interrupt Enable '0' : Disable '1' : Enable
	1	RW	MPEG Encode Sequence Complete Interrupt Enable '0' : Disable '1' : Enable
	0	RW	MPEG Encode Frame Complete Interrupt Enable '0' : Disable '1' : Enable

Encode Control Register

Read/Write Port: 0C68h
Default Value: 0000h

Field	Bits	Type	Description
-	15:1	-	Reserved
	0	RW	Clear Header Buffer Flag '1' : When S/W finish to get the header information, should set the flag to clear the header buffer flag. '0' : not affect

VLC Read Data Size Register

Read/Write Port: 0C6Ah
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	VLC Buffer Read Data Size [15:0] in 16-bits Unit

Fire Command Register

Read/Write Port: 0C6Ch
Default Value: 0000h

Field	Bits	Type	Description
-	15:9	-	Reserved
	8	RW	Pitcture type Current frame encode picture type. Only command trigger mode is valid.
	7:3	RW	Mquant value Value is 1 ~31. Only Mquant trigger mode is set to 1.
	2	RW	Force refresh key frame 0 : Normal mode 1 : Force to update I frame and re-accumulate refresh counter. Engine maybe delay one or two frame. Only ISP trigger mode is valid
	1:0	RW	Trigger Mode 00: Encoding Trigger by ISP 01: Encoding Trigger by Command 10: Stop encoding 11: Reversed

Y Frame Base Address of Decode Buffer 0 Register 1

Read/Write Port: 0C6Eh
Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Decode Buffer 0 Register 2

Read/Write Port: 0C70h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved

Y0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Frame in 16-bits Unit

U Frame Base Address of Decode Buffer 0 Register 1

Read/Write Port: 0C72h
Default Value: 0000h

Field	Bits	Type	Description
U0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Decode Buffer 0 Register 2

Read/Write Port: 0C74h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Frame in 16-bits Unit

V Frame Base Address of Decode Buffer 0 Register 1

Read/Write Port: 0C76h
Default Value: 0000h

Field	Bits	Type	Description
V0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Decode Buffer 0 Register 2

Read/Write Port: 0C78h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V0BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Frame in 16-bits Unit

Y Frame Base Address of Decode Buffer 1 Register 1

Read/Write Port: 0C7Ah
Default Value: 0000h

Field	Bits	Type	Description
Y1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Decode Buffer 1 Register 2

Read/Write Port: 0C7Ch
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Frame in 16-bits Unit

U Frame Base Address of Decode Buffer 1 Register 1

Read/Write Port: 0C7Eh
Default Value: 0000h

Field	Bits	Type	Description
U1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for U Frame in 16-bits Unit

			U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Decode Buffer 1 Register 2

Read/Write Port: 0C80h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Frame in 16-bits Unit

V Frame Base Address of Decode Buffer 1 Register 1

Read/Write Port: 0C82h
Default Value: 0000h

Field	Bits	Type	Description
V1BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Decode Buffer 1 Register 2

Read/Write Port: 0C84h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V1BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Frame in 16-bits Unit

Y Frame Base Address of Decode Buffer 2 Register 1

Read/Write Port: 0C86h
Default Value: 0000h

Field	Bits	Type	Description
Y2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Decode Buffer 2 Register 2

Read/Write Port: 0C88h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for Y Frame in 16-bits Unit

U Frame Base Address of Decode Buffer 2 Register 1

Read/Write Port: 0C8Ah
Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Decode Buffer 2 Register 2

Read/Write Port: 0C8Ch
Default Value: 0000h

Field	Bits	Type	Description

-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for U Frame in 16-bits Unit

V Frame Base Address of Decode Buffer 2 Register 1

Read/Write Port: 0C8Eh
Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Decode Buffer 2 Register 2

Read/Write Port: 0C90h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for V Frame in 16-bits Unit

Decode Frame Width Register

Read/Write Port: 0C92h
Default Value: 0000h

Field	Bits	Type	Description
DecYPitch	15:7	RW	Decode Y Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
DecFrameWidth	5:0	RW	Frame Width [5:0] in 128-bits Unit The frame width must be times of 16.

Decode Frame Height Register

Read/Write Port: 0C94h
Default Value: 0000h

Field	Bits	Type	Description
DecUVPitch	15:7	RW	Decode UV Pitch [8:0] in16 bits Unite.
-	6	-	Reserved
DecFrameHeight	5:0	RW	Frame Height [5:0] in 128-bits Unit The frame height must be times of 16.

Special function Register

Read/Write Port: 0C96h
Default Value: 0000h

Field	Bits	Type	Description
-	15:13	-	Reserved
	12:8	RW	Decode Time Code Bit Number The number of bits representing the value is calculated as the minimum number of unsigned integer bits required to represent the above range.
-	7	-	Reserved
	6	W	MPEG Half Rate Flag '0' : Disable '1' : Enable Write Only.

	5	W	MPEG Skip One Frame '0' : No Affect '1' : skip one frame Write Only.
	4	W	MPEG Add One Frame '0' : No Affect '1' : add one frame Write Only.
-	3	RW	Deblocking filter turn on flag '0' : On '1' : Off
	2	RW	MPEG Decode Short Header '0' : Disable '1' : Enable
	1	RW	MPEG Capture Write Interrupt Enable '0' : Disable '1' : Enable
	0	RW	MPEG Decode Complete Interrupt Enable '0' : Disable '1' : Enable

Command and Data Buffer Start Address Register 1

Read/Write Port: 0C98h
Default Value: 0000h

Field	Bits	Type	Description
	15:0	RW	Command and Data Buffer Start Address[15:0] S/W will prepare the decoded data in the data buffer. This is also fire command. When S/W finish to set the register, H/W will start to issue request to get the data.

Command and Data Buffer Start Address Register 2

Read/Write Port: 0C9Ah
Default Value: 0000h

Field	Bits	Type	Description
-	15:10	-	Reserved
			Frame Buffer Selector This flag is used to identify which one frame buffer had been selected to decode. *Notice* : S/W should set the REG[0E2E]and REG[0E30] sequentially.
-	7:6	-	Reserved
	5:0	RW	Command and Data Buffer Start Address[21:16] S/W will prepare the decoded data in the data buffer. This is also fire command. When S/W finish to set the register, H/W will start to issue request to get the data.

Y Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0C9Ch
Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Deblocking Buffer 0 Register 2

Read/Write Port: 0C9Eh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for Y Frame in 16-bits Unit

U Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0CA0h
Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer0 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Deblocking Buffer 0 Register 2

Read/Write Port: 0CA2h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for U Frame in 16-bits Unit

V Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0CA4h
Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 0 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 0. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Deblocking Buffer 0 Register 2

Read/Write Port: 0CA6h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 0 for V Frame in 16-bits Unit

Y Frame Base Address of Deblocking Buffer 1 Register 1

Read/Write Port: 0CA8h
Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Deblocking Buffer 1 Register 2

Read/Write Port: 0CAAh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for Y Frame in 16-bits Unit

U Frame Base Address of Deblocking Buffer 1 Register 1

Read/Write Port: 0CACh
Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer1 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Deblocking Buffer 1 Register 2

Read/Write Port: 0CAEh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for U Frame in 16-bits Unit

V Frame Base Address of Deblocking Buffer 0 Register 1

Read/Write Port: 0CB0h
Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 1 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 1. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Deblocking Buffer 1 Register 2

Read/Write Port: 0CB2h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 1 for V Frame in 16-bits Unit

Y Frame Base Address of Deblocking Buffer 2 Register 1

Read/Write Port: 0CB4h
Default Value: 0000h

Field	Bits	Type	Description
Y0BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for Y Frame in 16-bits Unit Y Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height

Y Frame Base Address of Deblocking Buffer 2 Register 2

Read/Write Port: 0CB6h
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
Y2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for Y Frame in 16-bits Unit

U Frame Base Address of Deblocking Buffer 2 Register 1

Read/Write Port: 0CB8h
Default Value: 0000h

Field	Bits	Type	Description
U2BaseAdr	15:0	RW	Base Address [15:0] of Buffer2 for U Frame in 16-bits Unit U Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

U Frame Base Address of Deblocking Buffer 2 Register 2

Read/Write Port: 0CBAh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
U2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for U Frame in 16-bits Unit

V Frame Base Address of Deblocking Buffer 2 Register 1

Read/Write Port: 0CBCh
Default Value: 0000h

Field	Bits	Type	Description
V2BaseAdr	15:0	RW	Base Address [15:0] of Buffer 2 for V Frame in 16-bits Unit V Frame's base liner address for encoding buffer 2. *Notice*: The size of buffer is Frame_Pitch * Frame_Height / 4

V Frame Base Address of Deblocking Buffer 2 Register 2

Read/Write Port: 0CBEh
Default Value: 0000h

Field	Bits	Type	Description
-	15:6	-	Reserved
V2BaseAdr	5:0	RW	Base Address [21:16] of Buffer 2 for V Frame in 16-bits Unit

Deblocking Process Thresholds Setting Register

Read/Write Port: 0CC0h
Default Value: 0602h

Field	Bits	Type	Description
-	15:12	-	Reserved
DBThresholdB	11:8	RW	Deblocking threshold B
DBThresholdA	7:0	RW	Deblocking threshold A

VLC Buffer Valid Size Register

Read/Write Port: 0CC2h
Default Value: 0000h

Field	Bits	Type	Description
VLCBufValid	15:0	RW	Indicate how much valid data in VLC Buffer.

Encode Status Register 0

Read/Write Port: 0CC4h
Default Value: 0000h

Field	Bits	Type	Description
-	15:14	-	Reserved
	13	R	MPEG Half Rate Flag
	12	R	MPEG Skip One Frame
	11	R	MPEG Add One Frame
	10	R	Capture In Status '1' : One Frame In
	9:4	R	Valid Header Number The number of header is valid to read.
	3	R	Header Buffer Full Flag '0' : Not full '1' : Full

	2	R	VLC Buffer Full Flag '0' : Not full '1' : Full
	1	R	MPEG Encode Sequence Complete Flag '0' : Busy '1' : End
	0	R	MPEG Encode Frame Complete Flag '0' : Busy '1' : End

Encode Status Register 1

Read/Write Port: 0CC6h
Default Value: 0000h

Field	Bits	Type	Description
	15	R	Re-Construct Req
	14	R	VLD Stall
	13	R	Decode Zero Block
	12	R	Decoder Block End in Q
	11	R	Decode Write Enable in Q
	10	R	VLD Scan Direction
	9	R	TC Idle
	8	R	DC AC Prediction Rdy
	7	R	Block End
	6	R	Q to Mquant Ack
	5	R	AC Rdy
	4	R	DC Rdy
	3	R	DCT Rdy
	2	R	TC MC RF Valid
	1	R	TC Cur RF Valid
	0	R	ME Rdy

Decode Status Register

Read/Write Port: 0CC8h
Default Value: 0000h

Field	Bits	Type	Description
	15:14	R	Debug Info Encoder FSM Stauts
	13	R	MPEG Decode Engine Status '0' : Idle '1' : Busy
	12	R	Fire Queue Empty '0' : Empty '1' : Full
	11:10	R	Current Frame Buffer Indicator Indicate current decoding frame buffer
	9:6	R	Current Frame Decode Error Flag "0000" : No Error Others : Error
	5:4	R	Finished Frame Buffer Indicator

			Indicate which frame buffer has finished to decode
	3:0	R	Finished Frame Decode Error Flag "0000" : No Error Others : Error

Decode Read Back Register 0

Read/Write Port: 0CCAh
Default Value: 0000h

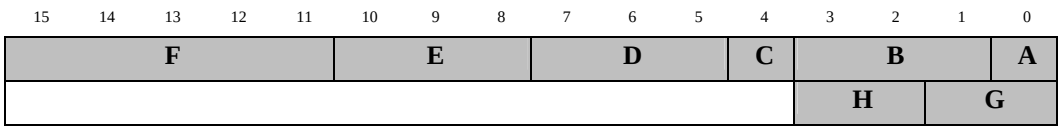
Field	Bits	Type	Description
	15	R	Decode Status (0)
	14:12	R	VLC OUT FSM
	11:8	R	VLC TOP FSM
	7:4	R	MBD FSM
	3	R	VLCOverFlow
	2	R	VLCStall
	1	R	UsedBitsRdy
	0	R	FrmSumRdy

Decode Read Back Register 1

Read/Write Port: 0CCCh
Default Value: 0000h

Field	Bits	Type	Description
	15	R	DeStatus(1)
	14:11	R	ME Top FSM Status
	10:8	R	Ref FSM Status
	7:6	R	Org FSM Status
	5	R	Mask Rdy
	4	R	ME Rdy
	3:0	R	VLD Status

VOP_Header Data Format for Decoding Process



A. vop_coding_type
0 : I frame, 1 : P frame

B. vop_r_size[2:0]
vop_r_size = vop_fcode_forward - 1

C. vop_rounding_type

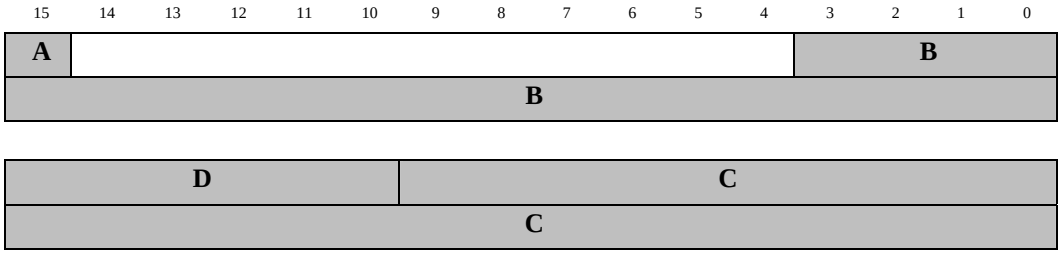
D. vop_start_bits[2:0]
indicate H/W should discard bit counts to decode

E. intra_dc_vlc_thr[2:0]
F. vop_quant[4:0]
G. vop_forward_buf[1:0]
forward reference buffer selector
H. vop_current_buf[1:0]
current decoding buffer selector

Decoding Data sent to H/W

VOP Header Data
Data
: :
: :
Data
VOP End Data (0x000001B6)

Encoding Header Data Format



A. Discard Frame
1 : This frame should be discard.
B. Total Frame Bits

C. Time Code for AV sync

D. Skip Frame Number