BT-AN-0052 (BRF63xx Voice and Audio Configuration, Rev 0.4)

Bluetooth Applications department

ABSTRACT

This document describes the capabilities of the BRF63xx voice and FM audio systems. It describes the different audio formats supported by the BRF63xx and how to interface with them using the PCM bus. It also describes voice over HCI and some issues regarding eSCO links.

CONTENTS

Revision Control

Author Name	Description	Rev.	Date
Anthony Levine	2.1: Added use with profiles HFP1.5 and A2DP, eSCO use in scatternet. 2.3: FM over BT	0.4	11 Jan 2007
Anthony Levine	11.3.1: Clarified throughput calculation	0.2	15 Dec 2005
Anthony Levine	Document creation	0.1	30 May 2005

1 Audio Codec (PCM) interface

1.1 Overview

The Codec interface is a fully dedicated programmable serial port that provides the logic to interface to several kinds of PCM or I2S codecs. The interface supports:

- Two voice channels
- Master / slave modes
- u-Law, A-Law, Linear and Transparent coding schemes
- Variable length frames and frame sync duty cycles
- Variable data size, position and bit order.
- PCM bus sharing
- High rate PCM interface for EDR.
- Various voice formats (standard PCM, I2S, UDI) and a wide variety of Codecs.

1.2 PCM hardware interface

The PCM interface is a 4-wire interface. It contains the following lines:

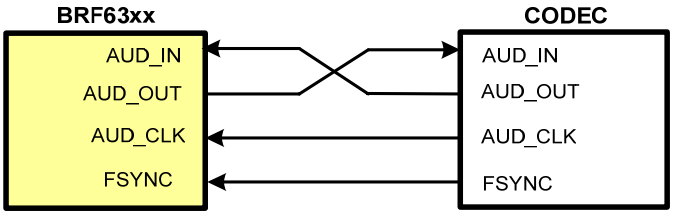


Figure 1. PCM interface (BRF63xx as slave)

AUD_IN	-	Input
AUD_OUT	-	Output
AUD_CLK	-	Configurable direction (input or output)
FSYNC	-	Configurable direction (input or output)

The Bluetooth device can be either the master of the interface where it generates the clock and the frame-sync signals, or slave where it receives these two signals. i.e. Clock and frame-sync can act as inputs or outputs.

Configuration is done by HCI_VS_Write_Codec_Configuration_Island3.

(For all VS information, see BT-SW-0031 (BRF6350 Vendor Specific commands)).

After reset or power up, the PCM interface is set to slave by default with all PD's active.

1.2.1 AUD_CLK

For slave mode, clock input frequencies of up to 16 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.

For master mode, the BRF63xx can generate any clock frequency between 64 - 4,096 KHz, with 1ppm accuracy. Clocks are generated from the fast clock and will be synchronous to it.

EDR support affects the maximum PCM clock rate. The maximum data rate will be achieved when using 3-EV5 packets. The maximum rate of one asymmetric 3-EV5 channel is 1.154MHz (= one 3-EV5 packet every 3 frames). The maximum rate of two asymmetric 3-EV5 channels is 1.382MHz (= two 3-EV5 packets every 5 frames).
Therefore in order to support 2 channels, the clock rate needs to be at least 1.382MHz.

1.2.2 AUD_OUT

The Data Out line is configured as Hi-Z output between data words. Data Out can also be set for permanent Hi-Z, irrespective of data out. This allows BRF63xx to act as a bus slave in a multi-device PCM bus.

1.2.3 FSYNC

For both master and slave modes, the interface supports:

- Fsync periods from 1 to 65535 times the Audio Clock period, in 1 clock increments.
- Fsync duty cycles of 1 to 65535 times the Audio Clock period, in 1 clock increments. A value of 0x0000 sets for 50% duty cycle (e.g. required by I2S interface)

1.2.4 Clock-edge operation

The Codec interface of the BRF63xx can work on rising or falling edge of the clock. It also has the ability to sample the frame sync and the data at inversed polarity.

The following diagram shows operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame sync signal is updated by the codec on the falling clock edge and therefore shall be sampled by the BRF63xx on the next rising clock. The data from the codec will be driven from the falling edge and therefore sampled by the BRF63xx on the clock falling edge.

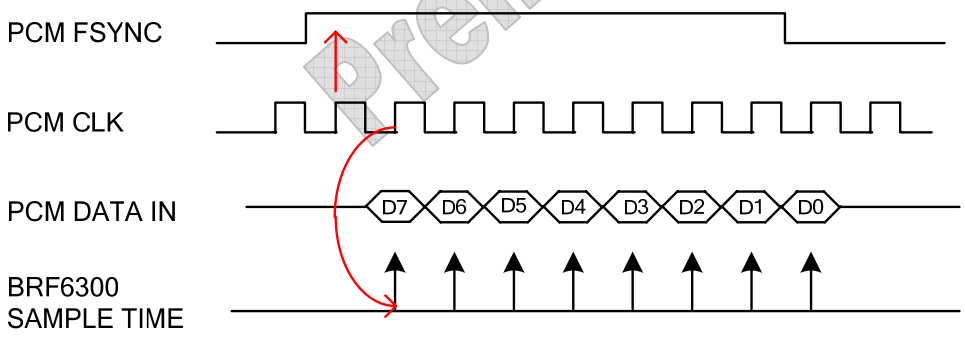


Figure 2. Negative clock edge PCM operation

1.2.5 Data bits configuration

1.2.5.1 Size

The data length can be set from 8 to 640 bits, per channel. Up to two channels are possible and data length can be set independently for each channel.
Data in and data out do not necessarily have to be the same size.

1.2.5.2 Order

There are codecs in which the bit-order is inversed, i.e. LSB is first. The BRF63xx Codec interface supports both MSB first and LSB first.
The bits order of data in and data out can be configured independently.
The order for each channel is separately configurable.

1.2.5.3 Position / offset

There are codecs in which the input and output data do not have the same timing – for example PCM3008, a stereo audio codec of TI.
In general, the data position within a frame is configurable in with 1 clock (bit) resolution and can be set independently for each channel, relative to the beginning edge of the frame sync signal.

1.2.5.4 HCI vendor specific commands

The following VS commands are used to set up the codec interface:

- HCI_VS_write_codec_config_Island3
- HCI_VS_write_codec_config_enhanced_Island3

See BT-SW-0031 - BRF6300 Vendor Specific Commands

1.3 Two channel PCM bus Example

In the following figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame.

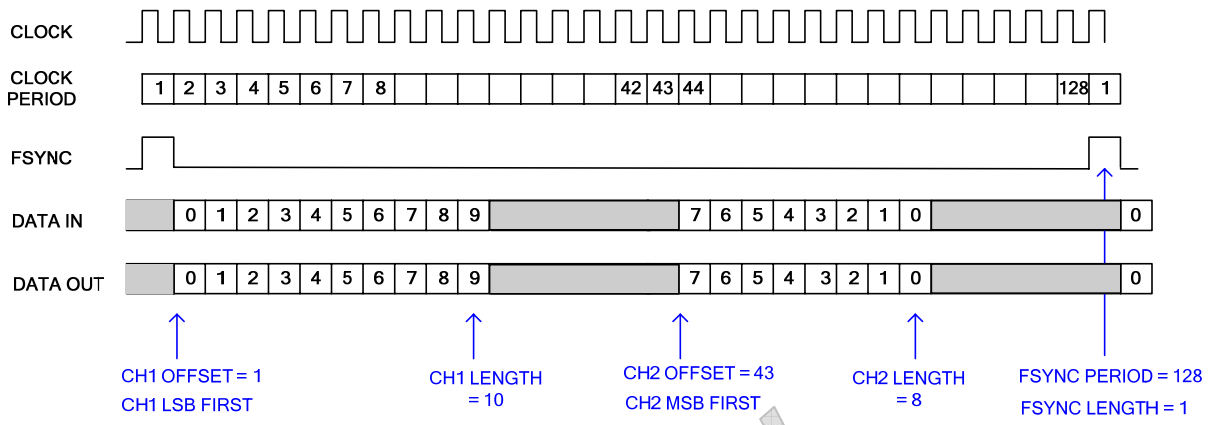


Figure 3. Two channel PCM bus timing

HCI_VS_Write_Codec_Configuration_Island3 setup:

- PCM clock rate 0x0800 (2.048 MHz)
- PCM clock direction 0x01 (BRF63xx is slave)
- Frame sync frequency 0x03E80 (16 KHz)
- Frame sync duty cycle 0x0001 (high for 1 period of PCM clock)
- Frame sync edge 0x00 (rising edge)
- Frame sync polarity 0x00 (active high)
- Reserved 0x00
- CH1 data out size 0x000A (10 bits)
- CH1 data out offset 0x0001 (1 clock from rising edge of fsync)
- CH1 data out edge 0xFF (data out driven at clock rising edge)
- CH1 data in size 0x000A (10 bits)
- CH1 data in offset 0x0001 (1 clock from rising edge of fsync)
- CH1 data in edge 0xFF (data out driven at clock rising edge)
- Reserved 0x00
- CH2 data out size 0x0008 (8 bits)
- CH2 data out offset 0x002C (44 clocks from rising edge of fsync)
- CH2 data out edge 0xFF (data out driven at clock rising edge)
- CH2 data in size 0x0008 (8 bits)
- CH2 data in offset 0x002C (44 clocks from rising edge of fsync)
- CH2 data in edge 0xFF (data out driven at clock rising edge)

- Reserved 0x00

HCI_VS_Write_Codec_Configuration_Enhanced_Island3 setup:

- PCM clock shutdown 0x00 (disabled)
- PCM clock start 0x0000 (N/A)
- PCM clock stop 0x0000 (N/A)
- Reserved 0x00
- CH1 data in order 0x01 (LSB first)
- CH1 data out order 0x01 (LSB first)
- CH1 data out mode 0x02 (Hi-Z when idle)
- CH1 data out duplication 0x00 (Retransmit last sample for missing data)
- CH1 tx_dup_valve 0x00000000 (N/A)
- CH1 data quant 0x00 (Use bit mode if < 24 bits)
- Reserved 0x00
- CH2 data in order 0x00 (MSB first)
- CH2 data out order 0x00 (MSB first)
- CH2 data out mode 0x02 (Hi-Z when idle)
- CH2 data out duplication 0x00 (Retransmit last sample for missing data)
- CH2 tx_dup_valve 0x00000000 (N/A)
- CH2 data quant 0x00 (Use bit mode if < 24 bits)
- Reserved 0x00

1.4 Frame Idle Period

The Codec interface has the capability for frame idle periods, where the PCM clock can “take a break” and become ‘0’ at the end of the PCM frame, i.e. after all data has been transferred. This feature is configured by HCI_VS_Write_Codec_Config_Enhanced, mentioned above. The BRF63xx supports frame idle periods both as master and slave of the PCM bus. When BRF63xx is the master of the interface, the frame idle period is configurable.

There are two configurable parameters:

- Clk_Idle_Start - Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock will become ‘0’.
- Clk_Idle_End – Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

e.g. For PCM clock rate = 1MHz, frame sync period = 10 KHz, Clk_Idle_Start = 60, Clk_Idle_End = 90:

Between each 2 frame syncs there will be 70 clock cycles (instead of 100). The clock idle period will start 60 clock cycles after the beginning of the frame and will last 90-60=30 clock cycles. This means that the idle period will end 100-90=10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.

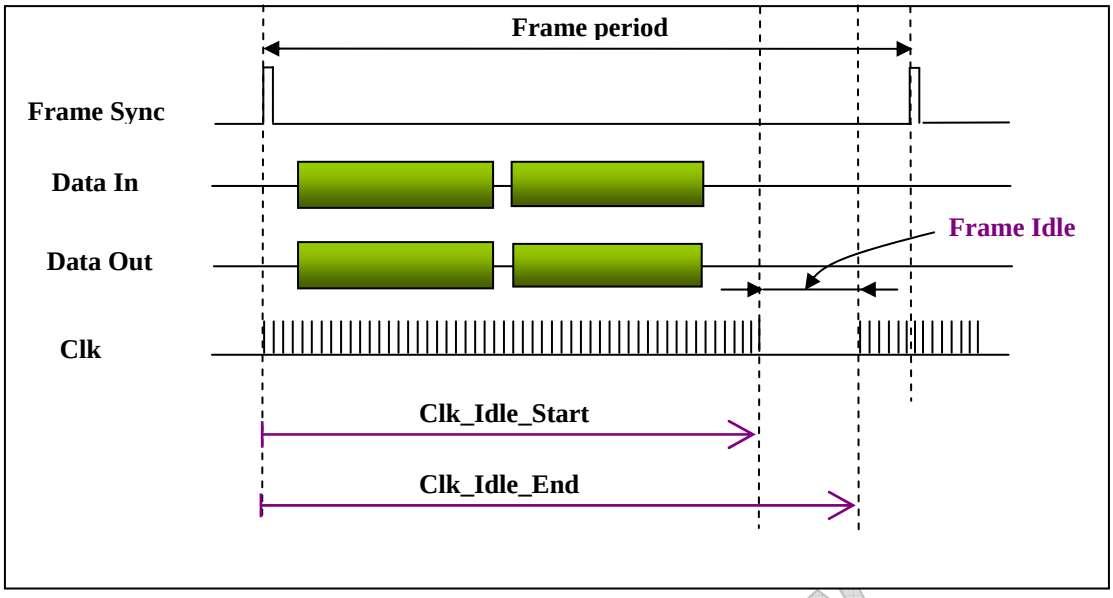


Figure 4. Frame Idle Period

1.4.1 Behavior with no input clock

As an improvement over the BRF6150 and in addition to the above, the BRF63xx (as slave) features a flexible recovery mechanism when the clock stops unexpectedly during a SCO/eSCO link. Little impact will be noticeable on the voice channel.

1.5 PCM Bus Sharing

The BRF63xx supports multi device configuration, in which there are several devices on the PCM bus.

The pin AUD_OUT can be configured to High impedance when it is not in use (i.e. between data words).
Combining this mode and setting the PCM interface to Slave mode (AUD_CLK and AUD_FSYNC are Inputs), allows sharing the same codec for both Bluetooth and other applications. When the BRF63xx is not used, the codec interface is configured as described above and other devices can be active on the PCM bus.

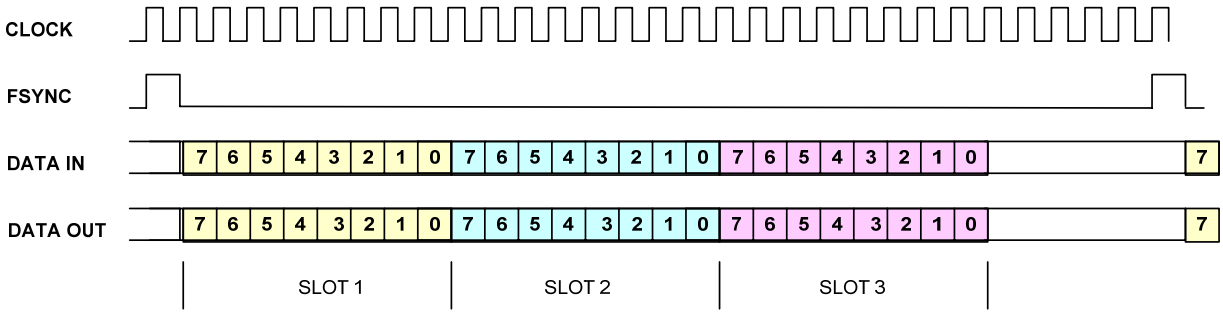


Figure 5. PCM bus sharing

1.6 RF link/PCM clock mismatch handling

The BRF63xx receives audio data from external codec or similar on the PCM interface and transmits these over Bluetooth 2.4GHz RF channels. Similarly, the BRF63xx receives audio data via Bluetooth 2.4GHz RF channels and transmits these to external codec via the PCM interface. These input and output data rates will not usually be the same, and therefore an audio data overflow or underflow can occur.

1.6.1 Overflow

The BRF63xx receives RF voice packets and writes these to the Codec interface. If the BRF63xx receives data faster than the Codec I/F output allows, an overflow will occur. In this case, the BRF63xx has two possible behavior modes: 'allow overflow' and 'don't allow overflow'.

A similar situation occurs when the BRF63xx receives data packets via the codec interface, faster than the BT RF link is able to transmit.

- If overflow is allowed, the BRF63xx will continue receiving data and will overwrite any data not yet sent to the Codec.
- If overflow is not allowed, RF voice packets received when buffer is full, will be discarded.

1.6.2 Underflow

Underflow will occur if output to the Codec interface occurs at a higher rate than the BRF63xx receives new data over the air. i.e. The PCM output buffer will be empty.

- In this case, the configured duplication data will be output to the PCM bus.

Underflow can also occur if Codec interface input rate is lower than the BT RF transmitting rate.

- In this case, the last PCM sample will be re-sent over the air.

1.6.3 Bluetooth clock and PCM clock synchronization.

Even when the BT and PCM data are well matched to avoid the problems or overflow and underflow above, there still exists a potential problem of data loss due to long-term clock drift between the BT clock and the PCM clock. This synchronization issue exists in any voice connection that uses the Codec interface. However, it is most critical for UDI support.

The BRF63xx solves this problem by the following: When the BRF63xx is the PCM bus master, it will automatically synchronize the PCM clock to the BT clock.

Note: Bluetooth clock is the Bluetooth timing clock provided by the Bluetooth piconet master and should not be confused with the BRF63xx Fref input.

There are 4 possible master-slave combinations. The BRF63xx can guarantee clock synchronization only when it is PCM master. When it is PCM slave and BT master, the PCM clock can not be relied on to meet BT accuracy specifications or to be continuous. In the case of the BRF63xx being the BT slave and the PCM slave, it has no control over either clock.

This is shown in the following table:

BT clock	PCM clock	Result
Master	Master	Synchronized
Master	Slave	Not synchronized
Slave	Master	Synchronized
Slave	Slave	Not synchronized

1.7 PCM Loop back

The PCM loop back feature allows performing loop back on the PCM bus. The loop back is done through buffers only and is used to test the connectivity on the PCB.
All the codec interface parameters, set by the HCI_VS_Write_Codec_Configuration_Island3 command, need to be set prior starting the PCM loop back.
The PCM loop back is enabled using HCI_VS_Set_PCM_Loopback_Enable. However, the loopback delay must first be configured using the following HCI_VS command:

PCM loop back is enabled using the command:
HCI_VS_Set_PCM_Loopback_Configuration_Island3.

1.8 Improved algorithm for lost packets

The BRF63xx features an improved algorithm for improving voice quality when received voice data packets go missing. There are two options:

- Repeat the last sample – possible only for sample sizes up to 24 bits. For sample sizes >24 bits, the last byte is repeated.

- Repeat a configurable sample of 8-24 bits (depends on the real sample size), in order to simulate silence (or anything else) in the PCM bus. The configured sample will be written in a specific register for each channel.

The choice between those two options is configurable separately for each channel using the HCI_VS_Write_Codec_Configuration_Enhanced_Island3.

This feature is further enhanced using the following new HCI_VS command: HCI_VS_enable_EPLC

2 Voice formats

The voice setting parameter as specified in the BT specification, controls the various settings for voice connections. The voice setting parameter controls the following configuration for voice connections: Input Coding, Air coding format, input data format, Input sample size, and linear PCM parameter. The formats used on the PCM interface and RF air coding, need not necessarily be the same.

The settings apply to all voice connections and can not be set for individual voice connections.

The standard HCI_Write_Voice_Setting command is used to write the values for the voice setting configuration parameter (see description in the Bluetooth spec version1.2 sections 6.12, 7. 3.29 and 7.3.30).

The BRF63xx Codec interface can use one of four audio coding patterns:

- Law (8-bit)
- μ-Law (8-bit)
- Linear (8 or 16-bit)
- Transparent

Command Parameters

Value	Description
00XXXXXXX	Input Coding: Linear
01XXXXXXX	Input Coding: μ-law Input Coding
10XXXXXXX	Input Coding: A-law Input Coding
11XXXXXXX	Reserved for Future Use
XX00XXXXX	Input Data Format: 1's complement
XX01XXXXX	Input Data Format: 2's complement
XX10XXXXX	Input Data Format: Sign-Magnitude
XX11XXXXX	Reserved for Future Use
XXXX0XXXX	Input Sample Size: 8 bit (only for Liner PCM)
XXXX1XXXX	Input Sample Size: 16 bit (only for Liner PCM)
XXXXXnnnXX	Linear_PCM_Bit_Pos: # bit positions that MSB of sample is away from starting at MSB (only for Liner PCM)

XXXXXXXX00	Air Coding Format: CVSD
XXXXXXXX01	Air Coding Format: µ-law
XXXXXXXX10	Air Coding Format: A-law
XXXXXXXX11	Reserved

Table 1. Voice setting parameters

2.1 Using SCO/eSCO links in the BRF63xx

2.1.1 Basic eSCO negotiation

In general eSCO packet types are negotiated by the host BT profiles. However, if all packets are enabled in the HCI_Setup_Synchronous_Connection command and there are no other link constraints, BRF63xx default selection will be the following:

- All packet types available: 2-EV3, Desco = 0, Tesco = 12, Wesco = 2, payload = 60 bytes.
- All packet types, except EDR: EV4, Desco = 0, Tesco = 10, Wesco = 0, payload = 50 bytes.

In both cases throughput = 64Kbps.

2.1.2 Scatternet with SCO/eSCO

The BRF63xx can handle 2 simultaneous SCO (or eSCO) channels on the same or different piconets, with packet type of HV3, EVx, 2-EVx, 3-EVx. If two eSCO channels are used, they must have the same BW configuration.

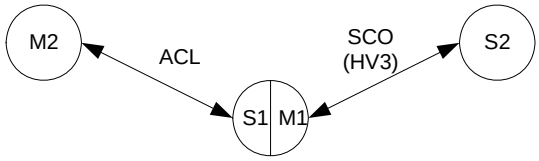
During the voice channel establishment, the highest possible interval between the voice packets is used before accepting/changing of the voice packet type.

Switching between the two networks is done automatically when needed. Various hooks are given to the firmware in order to avoid collisions between the two channels. This can be achieved by changing the (e)SCO parameters “on the fly”, according to the networks drifting rate, offset etc, resulting in optimal QoS and link management.

i.e. BRF63xx will automatically change (e)SCO slot positions if it sees potential problems between two piconets due to clock drift.

2.1.3 Combined SCO/eSCO and ACL links

The voice link will usually be given highest priority except for the following scenario:



A master (M1) has voice connection with a slave (S2) with interval of 3 frames (HV3 packets). A second master (M2) connects to the first master (M1 now S1) and establishes an ACL link. M2 will ACK the ACL data from S1 in a different frame to the one it received the ACL data in. If S1/M1 will not listen to M2 in that frame, S1 will NACK the packet to M2 in the next transmission.
In order to avoid an endless loop of NACK's from S1 to M2, S1 must listen in consecutive frames to receive the ACK from M2. Since there are no two consecutive frames between the SCO frames in this case, S1/M1 will need to overrun on the SCO frames to S2.
The scheduler priority of S1/M1 for the S1-M2 link, will remain higher than the M1-S2 voice for one more frame, in order to receive M2's acknowledgement.

For quick transactions, such as sending a business card between phones, the effect on voice quality will be very small. The host may manage this distortion by putting the device in Sniff mode and have voice interference in the Sniff intervals only. It is important to remember that the priorities can change “on the fly” and are fully flexible, in order to enable the firmware to achieve the best link management possible.

Because of above issues, it is recommended to use eSCO rather than SCO whenever possible for a Scatternet scenario. Because of eSCO's ability to allow greater spacing between packets and its retransmission capability, it will not have the limitations seen for SCO.

2.1.4 Support for Hands Free Profile 1.5 (HFP1.5)

BRF63xx provides full support for HFP 1.5, as specified in the specification.

HFP1.5 requires support for EV3 + 1 retransmission as a minimum for devices that do not support EDR packets (e.g. 2-EV3). This will normally not be allowed for a scatternet slave as there are insufficient slots to accommodate ACL links for the scatternet as well as EV3 + 1 retransmission.

The BRF63xx makes special provision for this by "stealing" slots from the eSCO link in order to allow the ACL links to coexist.

The HFP1.5 profile can act both as master or slave. Due to power consumption optimization it is preferred that the handset will act as slave when connected to a headset and as master when connected to a car kit. This will allow the headset to set up the lowest power ACL link, and the car kit (where power is plentiful) to be controlled by the headset.

2.1.5 Support for A2DP profile

The Advanced Audio Distribution Profile (A2DP) is usually used to connect to high quality headphones. The term “advanced audio”, therefore, should be distinguished from “Bluetooth audio”, which indicates distribution of narrow band voice on SCO channels. A typical use case is the streaming of music content from a stereo music player to headphones or speakers.

A2DP streams are guaranteed asynchronous links with demand for high bandwidth and low latency. A2DP devices are agnostic to device role, M/S. However, it is preferred that the source device will be the master since this is controlling the data steam, but both configurations are supported. It is assumed that the receiving device has a buffer of at least 100ms (required by AVRCP profile) and therefore the stream can handle peek latency of 100ms.

Parameters Set	Low quality Mode	High Quality Mode 1	High Quality Mode 2
Incoming Traffic	Control packets	Control packets	Control Packets
Outgoing Traffic	Guaranteed service 333bytes every 13.3ms 48 kHz, bitpool 28, subband 8, block size 16, mono, 5 SBC frames per packet	Guaranteed service 667bytes every 16ms 48 kHz, bitpool 48, subband 8, block size 16, joint stereo, 6 SBC frames per packet	Guaranteed service 181bytes every 5.3ms 48 kHz, bitpool 38, subband 8, block size 16, joint stereo, 2 SBC frames per packet

Table 2. A2DP Asynchronous Link

A HCI link with 500Kbps and 3mS latency is sufficient for the High quality mode 1 above.
i.e. The role of the BRF63xx is to receive/send A2DP data from/to a BT A2DP source over an ACL link and to stream this to the host - supporting the required throughput and latency.

2.2 Voice over HCI (VoHCI)

In addition to the codec interface, the BRF63xx also supports transfer of voice channels over the HCI interface. In this case (and unlike when using the PCM interface), the application is running a synchronous link through the HCI and all control is performed by the BRF63xx firmware. i.e. the data rate matching between the host and the air, buffer management and the total latency.

Main features:

- Supports all SCO/eSCO packet types and all data rates.
- All air modes supported: Transparent, CVSD, μLaw, aLaw.
- Flow control support in both directions

- Support 2 channels combinations – both Codec and VoHCI simultaneously. i.e. Each channel can be configured separately to Codec or HCI
- Local Loopback is available.

Constraints:
- When using H5 transport layer, the Voice over HCI is not supported.

2.2.1 Creating a Synchronous link over HCI

HCI_VS_Write_SCO_Configuration

The command HCI_VS_Write_SCO_Configuration allows the host to configure the following parameters of the voice channels:

Audio type: Codec interface/ Host interface (HCI)

HCI TX buffer size – allows the host to determine the BRF63xx transmission buffer length.

Max latency – determines the maximum amount of data (in Bytes) allowed in the TX buffer before it is flushed. This directly affects the latency of the channel. This parameter is applicable only if flow control is disabled. If flow control is enabled, then the host must regulate the data flow to keep the latency within limits.

Accept packet with bad CRC – determines whether to accept packets received with bad CRC. In eSCO with retransmission, it will not disable retransmission - packet will be accepted only after all retransmissions have failed.

SCO connection parameters and the flow control.

Return values:
- Status.
- HCI TX buffer size.
- Number of TX buffers.

The TX buffer minimum size is 30 bytes and there has to be at least 2 buffers.
The number of buffers is simply the number of buffers that will fit into the max latency given.

Notice that if the max latency value is not a multiple of the buffer size then it will be truncated accordingly. Therefore to prevent uncertainty, the host is encouraged to use max latency that is a multiple of the buffer size.

2.2.2 Flow Control

The flow control is implemented in both directions. Since there are separate RX and TX buffers for each channel, the host has to handle the flow control separately for each channel.

Host → Controller

Unlike ACL data, the flow control in this direction is not mandated by the BT specification, however it is highly recommended to be used for guaranteed synchronization

- HCI_Write_SCO_ Flow_Control_Enable: Used to enable / disable flow control of SCO/eSCO data
- HCI_Read_Buffer_Size: If flow control is enabled, Host must issue the command before it sends any data to the Controller.
- In case a packet is totally or partly flushed, a "data buffer overflow" event is sent to the Host
- Host has to manage flow control independently for each channel. Therefore, the SCO connection handle needs to be considered. See the BT specification for more detail.

Controller → Host

- HCI_Host_Buffer_Size: The host uses this command to notify the controller of its SCO buffer pool.
- HCI_Set_Host_Controller_To_Host_Flow_Control: The host uses this command to enable/disable flow control in this direction. See the BT specification for more detail.

Host has the control over the buffer size that the device will use and whether the synchronous connection is with the host or with the codec.

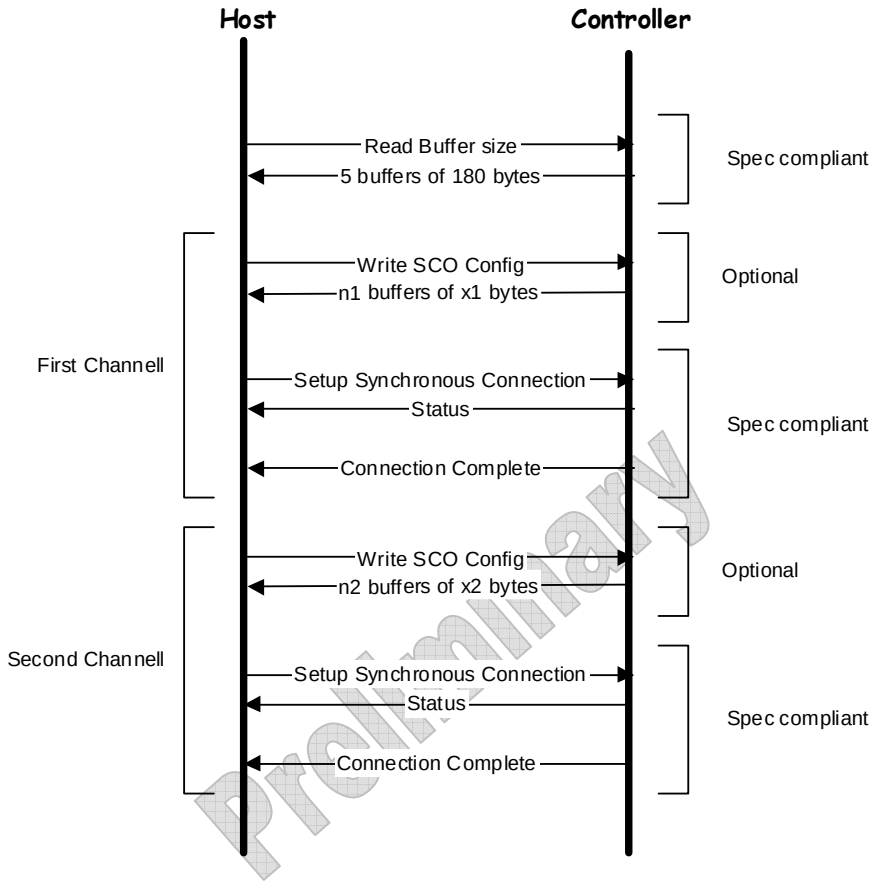


Figure 6. Synchronous connection creation procedure

2.2.3 Special considerations for voice over HCI

2.2.3.1 Performance

There are several factors to consider when evaluating the performance of VoHCI:

- Latency – The duration starting when sending a packet from one side until the other side receives it. It includes the UART delay, processing delay, air delay and buffer delay. It does not include the time that the host waits for flow control before sending the packet.
- Flow control affect on the BW – ability to reach full BW between the host and the device.
- Performance in high data rate.
- Idle time.
- Concurrent ACL and voice data.

A rough estimation for the latency is the number of BB (baseband) packets in the SCO buffer multiplied by the T_esco. Therefore, the bigger the SCO buffer, the larger the latency.

2.3 FM over BT

FM I2S audio can be directed to the BT module. The BT module sees this as an alternative PCM interface and can assign a eSCO channel to this. e.g. FM audio to a remote headset supporting only 64kbps (mono) voice stream. This use case assumes an HFP headset enabling the transfer of the FM similar to system tones or gaming tones transferred to the headset.

See command HCIPP_FM_SET_AUDIO_PATH in document BT-SW-0031 - BRF6350 HCI Vendor Specific Commands.

Note that if this is specified, the BT external PCM bus with not be available (all pins Hi-Z).

3 Application examples

The special features of BRF63xx such as clock synchronization and optimum packet size determination, enables the device to support two other Codec interfaces, which can be used for both voice and music transports.:

- Inter-IC Sound (I2S)
- UDI

These interfaces have different timing and data format requirements to the standard PCM codec interface described above.

3.1 Inter-IC Sound (I2S)

The BRF63xx can be configured as a Inter-IC Sound (I2S) serial interface to a I2S Codec device. I2S is a serial bus designed for digital audio devices and technologies such as compact disc (CD) players, digital sound processors, and digital TV (DTV) sound.

The I2S bus consists of three serial bus lines: a line with two time-division multiplexing data channels (SD), a word select line (WS), and a continuous serial clock line (SCK). The BRF63xx implements this using its standard PCM lines, with FSYNC = WS, DATA_IN/OUT = SD and CLOCK = SCK. The BRF63xx can act as an I2S master (provides WS and SCK), or as an I2S slave (receives WS and SCK).

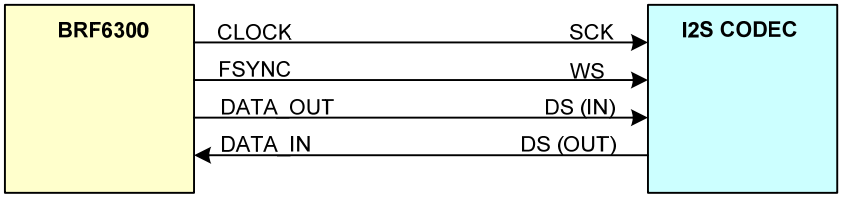


Figure 7. BRF63xx as I2S Master

The I2S link is implemented as a time division multiplexed (TDM) slot based serial interface, which is used to transfer audio data and command/status to or from the Codec device. In this mode, the BRF63xx audio Codec interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 (WS low) is used for the left channel audio data and time slot 1 (WS high) for the right channel audio data.

The I2S interface handles the audio data separately from the clock signals. By separating the data and clock signals, time-related errors that cause jitter do not occur, thereby eliminating the need for anti-jitter devices.

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock, word-select signal and data. In complex systems however, there may be several transmitters and receivers, which makes it difficult to define the master. In such systems, there is usually a system master controlling digital audio data-flow between the various ICs. Transmitters have to generate data under the control of an external clock, and so act as slaves.

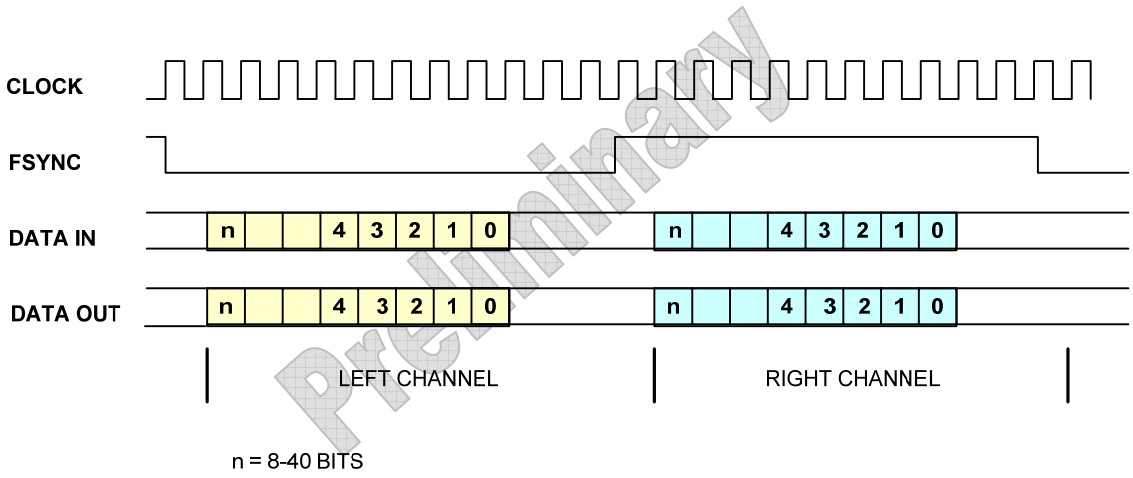


Figure 8. I2S signal format

In order to work in I2S configuration, SCL (IO2) is used for clock and SDA (IO3) for data. For more details see BRF63xx IO Configuration document. Also, in order to configure the correct timing, Fsync should have a duty cycle of 50%. Use HVI_VS_Write_Codec_Configuration_Island3.

HCI_VS_Write_Codec_Configuration_Island2 setting for I2S interface example:

- PCM clock rate – 0xC00 (3072 KHz)
- PCM clock direction – 0x0 (BRF63xx is Master)
- Frame sync frequency – 0x01 (8 KHz)
- Frame sync duty cycle – 0x05 (50% duty cycle)
- Frame sync direction – 0x0 (BRF63xx is Master)
- CH#1 data size – 0x10 (16 bit)
- CH#1 data offset – 0x00 (PCM clock cycle between the rising of frame sync and the first data bit.)

- CH#1 padding start – 0xFF (no padding)
- CH#1 padding value – 0x0

HCI_VS_Write_I2C_Register setting example:

- Slave ID – 0x1a (codec 2)
- PVT clock - 0 (pre scale clock divider factor)
- Working frequency – 0x0190 (400 khz)
- Sub address – 0x1e (an internal register address)
- Data length – 0x01 (1 byte)
- Data – "00" (one byte of data which is 00)

3.2 UDI

The UDI profile defines the protocols and procedures that are used by devices implementing UDI for the 3G mobile phone systems. e.g. device with Bluetooth connection to a 3G Handset, communicating via videophone over a 3G network. Up to 2 channels of UDI data can be supported. The data will be transferred via the Codec interface using transparent mode and will be sent out using eSCO EV4 Bluetooth packets (EV5 is also selectable).

3.2.1 UDI over Bluetooth Characteristics

The 3G UDI characteristics are:

- UDI frame size = 10ms.
- Clock rate = 3.84MHz (usually).
- UDI packet size = 86 bytes.
- Data rate = 64 or 384 Kbps

Each 3G UDI packet consists of 80 data bytes and 6 header bytes. Only the UDI data (80 bytes) is transferred via the PCM bus. The host receives the 3G UDI packets, including header and data, and then sends the data only to the BRF63xx device via PCM. I.e, the BRF63xx gets the data only and transmits the data only, over the air.

The UDI data can be transferred via PCM using any bus configuration that will supply a data rate of 64 kbps.

UDI RF data is transferred using eSCO EV4 packets every 12 BT frames = 120 bytes every 15 msec = 64 Kbps. There may be up to 2 UDI channels.

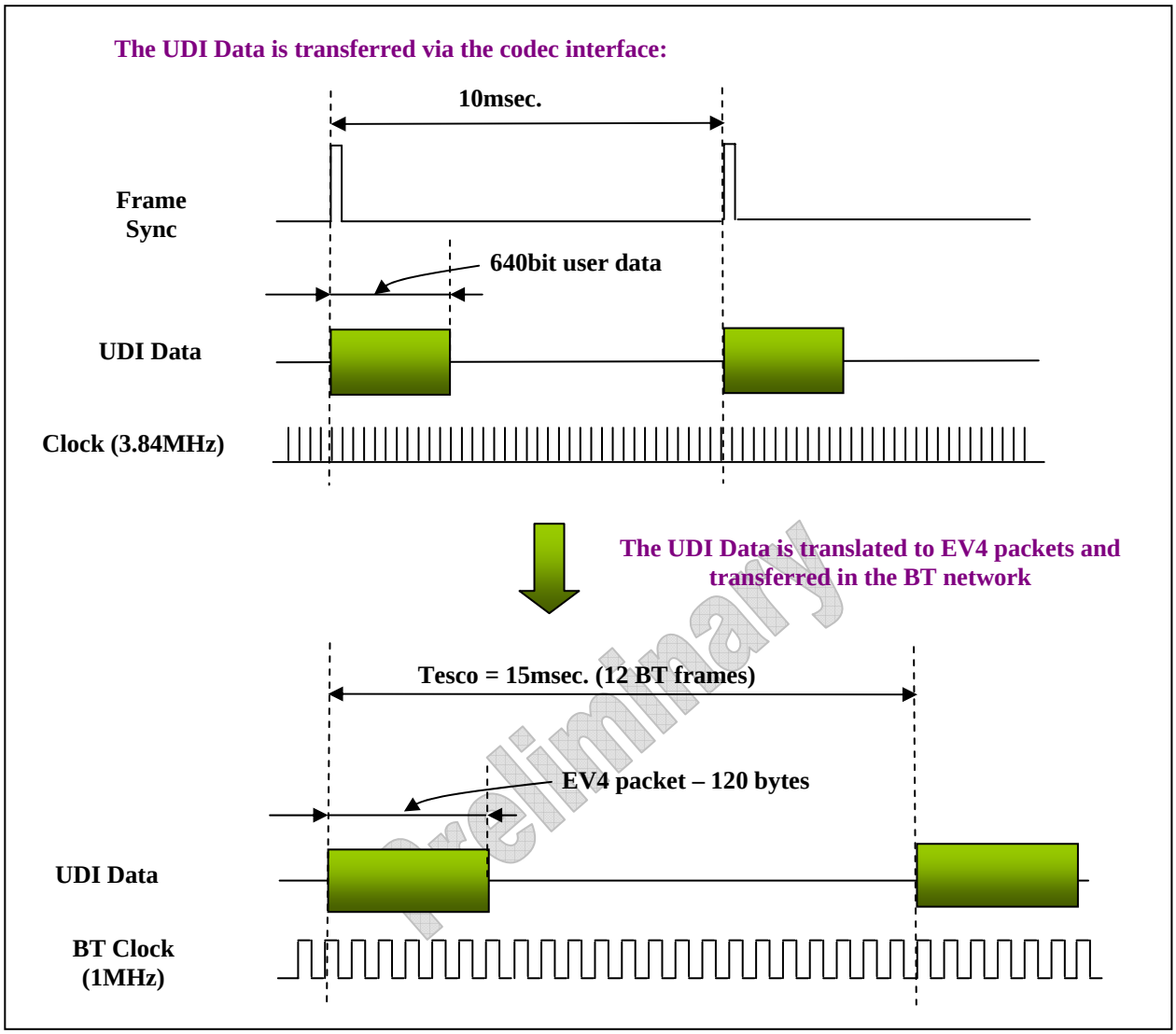


Figure 9. Examples of transferring UDI data

3.2.2 UDI Support Requirements

To support the UDI profile, the BRF63xx has the following abilities:

Support clock rate of 3.84MHz as input and as output.

Note:
According to the UDI spec, the frequency accuracy of the PCM clock must be under 100ppm and the latency in the BT part should be under 50msec. The BRF63xx supports these requirements.

3.3 Stereo music and MP3 support

3.3.1 Stereo

xxxIf SCO/eSCO BT channel is supplied from 1 PCM channel, then the only option is mono (or dual mono if you got 2 speakers) supplied by the mono Codec.

If SCO/eSCO BT channels are supplied from 2 PCM channels, then I2S configuration (described above) can be used to provide stereo music over 1 voice link.

BT 1.2 maximum rate is EV5 (TX 180 bytes over 3 slots + 1 slot RX).
i.e.: (180 * 8) / (3 * 625us + 625us) = 576 Kbps

Max stereo rate (assuming 16 bits per sample) would therefore be:
576kbps / 16bits / 2 chan = 18 Ksample/s.

With 3-EV5 EDR packets, this can be tripled to 54 Ksample/s.

These numbers are the maximum theoretical configuration that occupies the entire bandwidth. In real life, we must leave open slots for Scan, AFH classification, Signaling packets (LMP's) etc. So a more calculation is to leave 1 free frame for every eSCO packets (2 frames):

(180 * 8) / (3 * 625usec + 625usec + 1250usec) = 384kbps

Note that the PCM interface has Linear/CVSD digital filtering mechanism which limits the PCM to an audio frequency response bandwidth of 3.4KHz. To obtain the high sample/s data rate required by stereo music, transparent air mode must be used instead of the usually used CVSD. See BT specification HCI_Setup_Synchronous connection.

3.3.2 MP3

MP3 music can be transmitted as encoded (compressed) or decoded (uncompressed):

Transmitting decoded mp3 simply requires a very high rate eSCO channel.

Transmitting encoded mp3 requires a high data rate ACL channel and an MP3 decoder on the receiving side.

MP3 has 2 sample rate groups:
- 11.025, 22.05, 44.1 Ksample/sec
- 12k, 24, 48 Ksample/sec

Sample rate X number of bits/sample = channel rate:

e.g. 24 Ksample/s * 16 bits = 384 Kbps

e.g. 2 channels of 48 Ksample/s with 32 bits/sample
= Channel rate of 1536Kbps of decoded MP3
= Channel rate of 512Kbps of encoded MP3

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