BRF6300 Stacked RAM Programming Application Note

Revision Control

Revision 0.1

Abstract

This document describes the BRF6300 stacked RAM device and the method used to load it with the firmware.

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1. Introduction

The BRF6300 ROM device is available in the standard Microstar Junior BGA package for mass production quantities. A stacked RAM device in the same size is also available for the product development stage only, and is not available in high volumes. Its main use is to enable customers to update the BRF6300 firmware code during the development phase of the device, thus enabling them to get the advantage of testing the latest BRF6300 firmware releases as they become available, and before it is available on the ROM device.

In order to support the Enhanced Data Rate (EDR), the internal BRF6300 ARM processor is working with a high speed clock, which also affects the memory interface access time.

Since a Stacked Flash is not a valid solution due to the access time requirements, the stacked memory solution is based on a stacked RAM which enables 0 Wait State operation. The stacked RAM size is 512 KByte.

The Stacked RAM device has the same footprint as the production ROM device (4.5x4.5mm, 0.5 mm pitch) and holds sufficient RAM memory to upload the standard ROM code into it.

The differences from the standard ROM device are in the height (1.3mm in contrast to 0.8mm) and RF performance (slightly degraded in the stacked RAM), but do not result in any change in the assembly requirements.

2. Documents Reference

Document Description	Reference Number	Revision Number
BRF6300 product Preview	BT-DS-0023	Rev 0.2
BRF6300 Package Information	BT-AN-0046	Rev 0.1

Table 1: Documents reference

2.1 Power supply requirements

The stacked RAM voltage is supplied from the same source supplying the BRF6300 VDD_IO (1.8V).

The voltage to the stacked RAM should be supplied at all times, even during deep sleep and shutdown mode in order to ensure a valid storage of the downloaded code; this will eliminate the need for the code download sequence each time shutdown or deep sleep modes are used, so the code download sequence will be performed only once at power up.

This is achieved by supplying the stacked RAM from VDD_IO.

Whenever the voltage supply to the Stacked RAM is removed, a new code downloading procedure is required.

2.2 Stacked RAM Downloading Sequence

As mentioned earlier, since the stacked device is RAM based, a downloading sequence of the firmware is required at every power up.

The downloading sequence is performed via the HCI transport layer.

A typical Stacked RAM downloading sequence consists of the following steps:

1. Wakeup in ROM state (default).
2. Download the firmware to the stacked RAM via the HCI interface (in the same manner as a regular init script).

Now that the Stacked RAM is already loaded, the firmware detects it automatically and starts to run from the Stacked RAM.

There are two methods of downloading the firmware to the Stacked RAM through the HCI interface:

1. The system host is downloading the firmware
2. Using a PC application

In the case of downloading the firmware by the system host, the BRF6300 wakes up from the ROM at power up and the host downloads the firmware to the Stacked RAM via the HCI interface in the same manner of sending a regular init script.

This script contains a set of vendor specific commands that will load the firmware to the Stacked RAM.

When the downloading is completed, the BRF6300 starts to run automatically from the Stacked RAM and is ready to use.

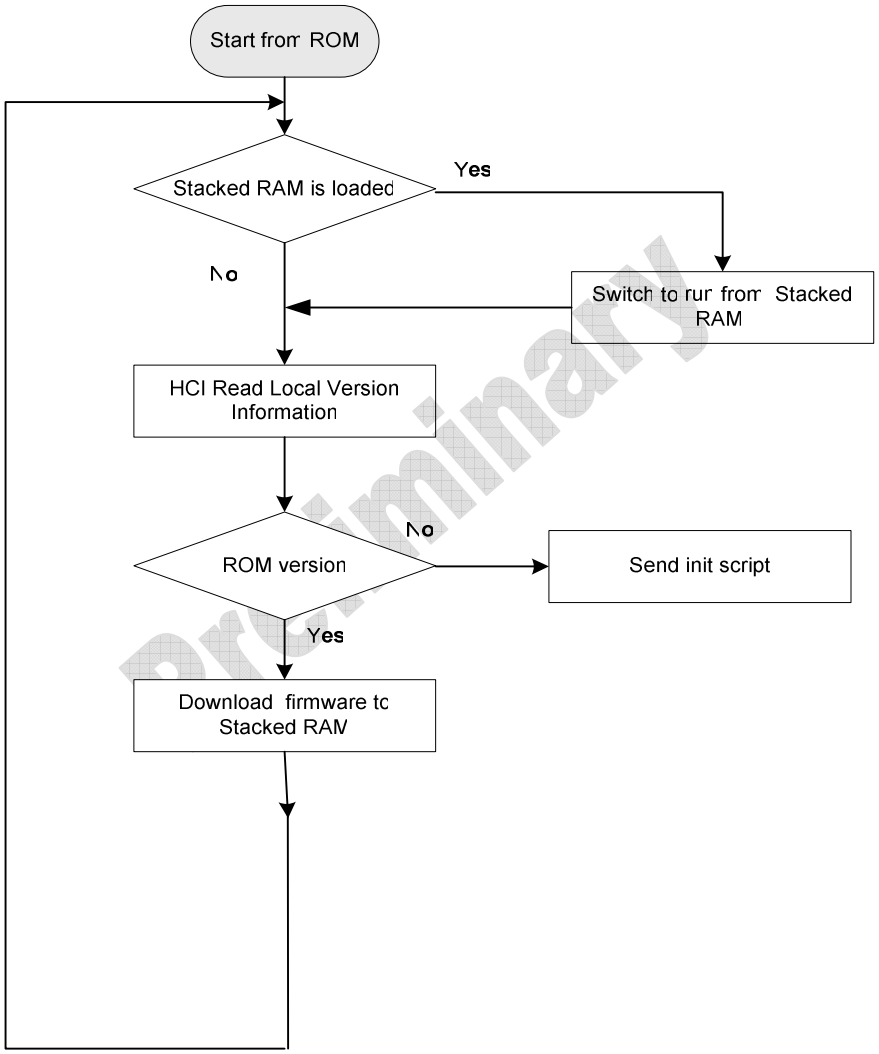
The host also needs to send its regular init script after every nSHUT_DOWN release, used for setting the system specific parameters like UART baud rate, codec configuration, etc., which is a different script than the script containing the firmware itself used for downloading the stacked RAM.

The regular init script, however, can be added to the firmware script and can be used as one script runs after every shut down.

Another option, in order to distinguish between these two script, is that the host can send after every nSHUT_DOWN release the HCI_Read_Local_Version_Information command and according the returned value of the LMP Subversion parameter it can decide if it is a ROM version (1.0.21) and a downloaded is needed or it is a Stacked RAM version (2.0.15 or above) and no download is needed and the regular init script need to be sent.

If the Stacked RAM needs to be erased, shutting down the power of the BRF6300 will erase the RAM and on the next power up the device will start running from the ROM.

The following diagram describes the process of downloading the firmware to the Stacked RAM and sending the regular init script separately:

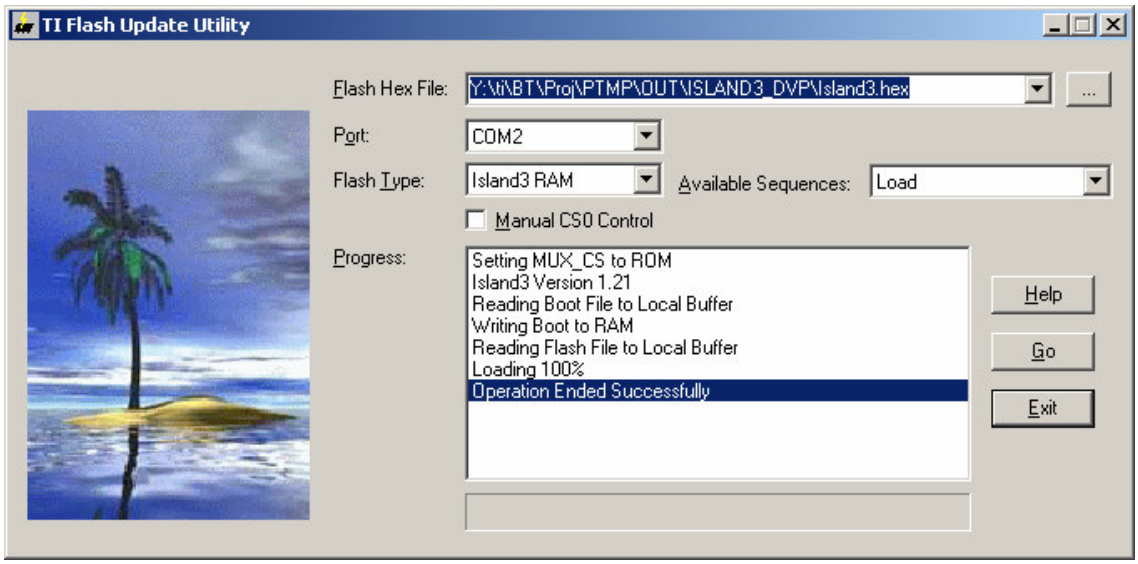


2.3 Stacked RAM Programming

As mentioned earlier, the downloading is done via the UART interface and the Flash update utility PC application. The UART interface consists of four lines: RX, TX, RTS and CTS, all four lines must be used to program the flash.

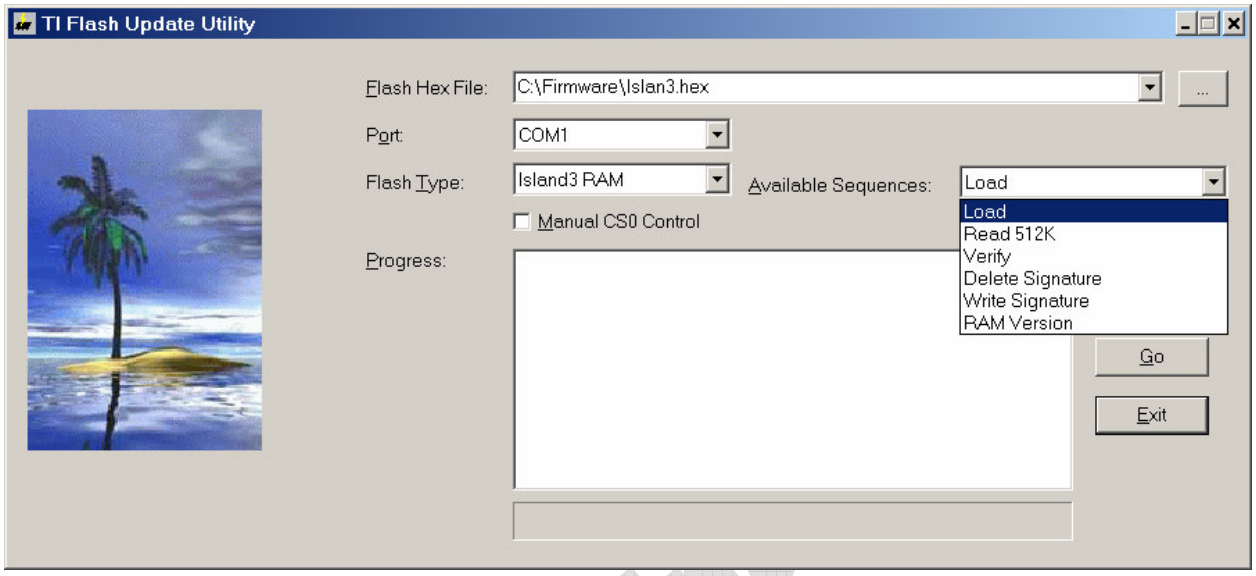
Note: The voltage levels of the PC must be modified by a level shifter (not provided by Texas Instruments) to allow it to work with the CMOS levels required by the stacked RAM device (1.8V typically).

- In the 'Flash Hex File' drop down menu selects the hex file to program
- In the 'Port' drop down menu selects the desired PC COM port
- In the 'Flash Type' drop down menu selects Island3 RAM
- In the 'Available Sequences' selects Load
- Press "GO"



The 'Progress' menu will display the status of the operation.

"Operation ended successfully" indicates successful completion of the downloading process; reset the board to start up with the new firmware loaded in the stacked RAM.



The 'Available Sequences' drop down menu has the following options:

- Load – load the firmware to the RAM
- Read 512K – read the content of the RAM
- Verify – verify that the content of the RAM matches to what was downloaded to it
- Delete Signature – erase the Stacked RAM
- Write Signature – for internal use
- RAM Version – read the firmware version loaded in the RAM

2.4 Stacked RAM Package

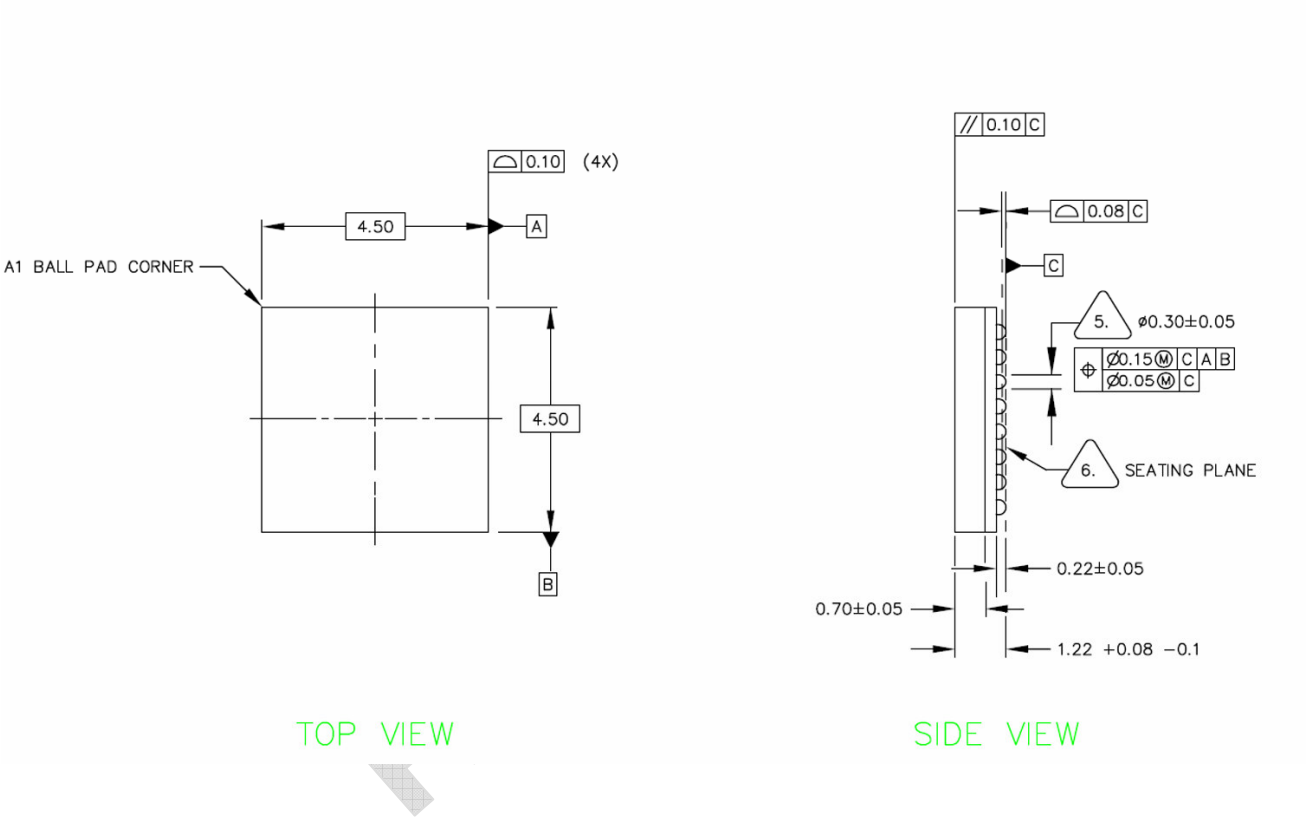


Figure 1: Stacked RAM package top and side view

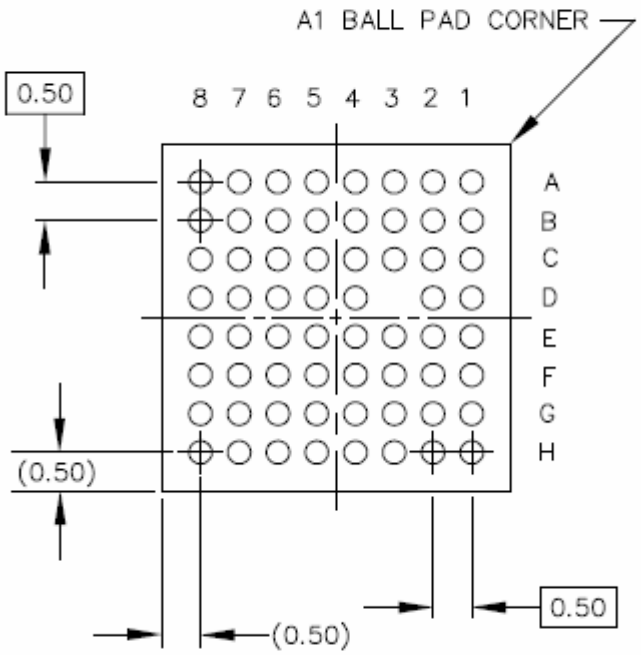


Figure 2: Stacked RAM package bottom view

2.5 Assembly

The stacked RAM device is assembled using the same profile as the standard device.
See the reflow profile below:

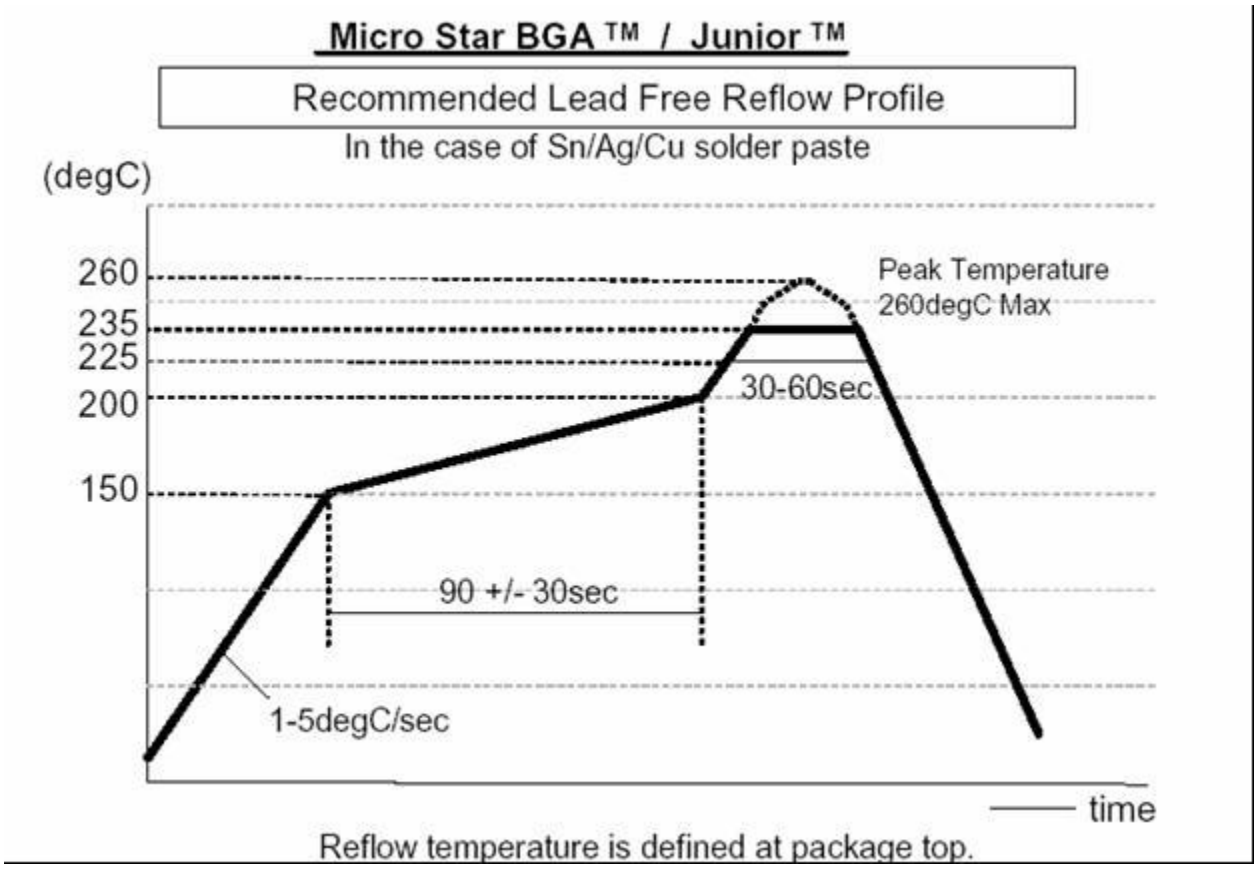


Figure 3: Stacked RAM reflow profile

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