Application Report
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SPI Host-Controller Interface

Bluetooth Applications Group

ABSTRACT

This document describes the Serial Peripheral Interface (SPI™) Host-Controller interface (HCI) for the BRF63xx from Texas Instruments. Specifically, it discusses the following information:

- Supported features
- Shared SPI bus mode

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1 Overview

The BRF63xx provides a TI Bluetooth® SPI (BTSPI) transport layer, in addition to the uinversal asynchronous receiver/transmitter (UART) and the secure digital input/output (SDIO) interfaces. The SPI interface provides high-speed data transfer capability with low power consumption for mobile electronic devices. The SPI bus is used as interface between a host and several different TI devices (including WLAN, Bluetooth and DTV). The SPI bus was designed to operate on a point-to-multipoint basis by providing a separate, active-low chip select ($\overline{CS}$) per device.

2 Supported BTSPI Features

BTSPI supports the following features:

- Incorporates a deep-sleep protocol
- Transport layer H4
- Point-to-multipoint
- Supports Bluetooth (BT) basic, EDR2 and EDR3 data rates
- Maximum supported clock rate = 13MHz
- BRF63xx is always SPI Slave, host is always SPI Master

3 BRF63xx Pinouts for HCI Transport Layer

The BRF63xx supports three transport layers that are multiplexed on the same I/O pins listed in Table 1.

Table 1. Transport Layer Pinout Multiplexing(1)

	UART	SDIO (1-bit)	SPI
CLK (I)	—	CLK (I)	CLK (I)
RX (B)	RX (PU, I)	CMD (B)	DI (I)
CTS (I)	CTS (PU, I)	IRQ (O)	$\overline{CS}$ (PU, I)
RTS (B)	RTS (PU, O)	IRQ (O)	IRQ (O)
TX (B)	TX (PU, O)	DATA (B)	DO (O)

(1) **Key:** I = Input; O = Output; **PU = ???; B = ???**

4 BTSPI Interface Description

In order to facilitate a broad implementation, the protocol is half duplex and does not require simultaneous operation of data OUT (DO) and data IN (DI). All TI communication devices are slaves in this protocol, and all transactions are initiated by the host, as SPI Master. The clock rate for each one of the connected devices may be different and configured per device.

Figure 1 illustrates the SPI interface signals; Table 2 describes the SPI interface signals.

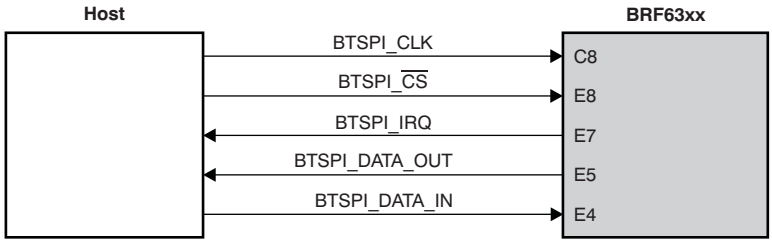


Figure 1. SPI Interface Signals

Table 2. SPI Interface Signals Description

Port Name	I/O	Description
BTSPI_CLK	I	Clock (0MHz to 13MHz) from host to slave
BTSPI_DI	I	Data from host to slave
BTSPI_CS	I	$\overline{CS}$ signal from host to slave
BTSPI_IRQ	O	Interrupt from slave to host
BTSPI_ DO	O	Data from slave to host

During reset, all outputs are in high-impedance mode and all pull-up resistors are pulled up.

4.1 $\overline{CS}$ and Bus Sharing Operation

The $\overline{CS}$ line selects a specific device on the shared SPI bus. $\overline{CS}$ is asserted at the beginning of an SPI transaction and de-asserted when the transaction completes; $\overline{CS}$ must not be de-asserted during the transaction.

Bus sharing by multiple devices is implemented by asserting one $\overline{CS}$ signal at a time and performing transactions with a specific device Device multiplexing is performed on a transaction basis rather than on a byte or word basis.

4.2 Sleep Protocol

In order to optimize power consumption, the BRF63xx device toggles between an active state and a low-power mode (deep sleep).

When operating in low power mode, the device deactivates most of its logic and is not capable of full-speed transactions with the host. The host must wake up the device when the BRF63xx is in sleep mode.

The wake-up protocol is based on assertion of $\overline{CS}$. The BT device performs its wake-up procedure and responds by asserting the IRQ line. $\overline{CS}$ must be asserted for a minimum time of 31µs in order for a BRF63xx device in sleep mode to recognize the signal.

Note: If a BRF63xx device is in sleep mode, any transactions (read or write) should not be started until the IRQ line is asserted.

The SPI driver within the host does not have to be aware of the sleep state of the device. It is the responsibility of the BT stack to report to the SPI driver what state is the device is in.

This procedure is also utilized as a method for flow control. The BT stack always signals the SPI driver that the device is in sleep mode. In response to a $\overline{CS}$ assertion, the BRF63xx device asserts the IRQ line only when it has enough free buffer space to receive a transaction.

Note: The delay from $\overline{CS}$ assertion to the IRQ line assertion may vary, depending on the actual state of the BRF63xx device and the delay in system clock activation. The delay does not exceed 2ms under worst-case conditions in order to prevent bus blocking. In normal operation, the delay until IRQ line assertion is significantly shorter, and polling of the IRQ line may be beneficial.

4.2.1 Enabling the BTSPI Deep Sleep Protocol

Deep Sleep operation is disabled at at power-up by default. In order to enable the BRF Deep Sleep feature and make the Deep Sleep protocol active, the host must first send an **HCI_VS_Sleep_Mode_Configurations** command:

```
Send_HCI_VS_Sleep_Mode_Configurations 0xFD0C, 1, 1, 0x06, 0xFF, 0xFF, 0xFF, 0, 100
Wait_HCI_Command_Complete_VS_Sleep_Mode_Configurations_Event 5000, any,
HCI_VS_Sleep_Mode_Configurations, 0x00
```

Refer to Section 9 for a detailed description of this command.

5 BTSPI Transactions

Note: The first command to be sent to the BRF63xx requires special consideration. Refer to Section 8 for more details.

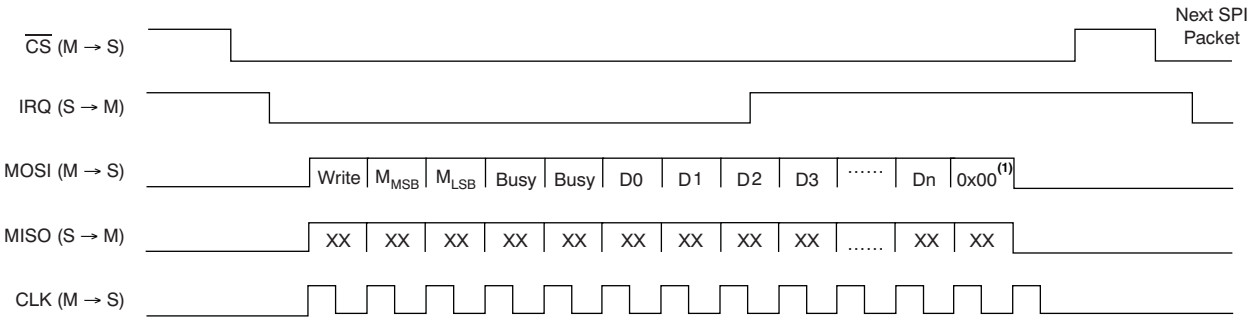
5.1 Write/Read Transactions

5.1.1 16-Bit Alignment

All data sent or received over the BT SPI interface are 16-bit aligned.

5.1.2 Write Operation—Host to BRF63xx Data Transfer

Figure 2 shows the BTSPI write transaction timing.



(1) Padding byte for 16-bit alignment, if required.

Figure 2. BTSPI Write Transaction

SPI Header:

MOSI	=	BRF63xx Data In
MISO	=	BRF63xx Data Out
Write	=	Opcode for write is 0x01
M_{MSB}, M_{LSB}	=	16-bit data payload length (including alignment byte)
Busy	=	Busy byte (0x00)

SPI Payload (equal to the HCI command + padding byte):

D0 …Dn = 0x00 (depending of number of bytes in SPI payload)

XX = Should be ignored by master

In order for the total SPI packet (that is, the SPI transaction) to be 16-bit aligned, the HCI command must be padded with an additional 0x00 byte if the HCI packet is even size. Refer to Table 3 for more information.

Table 3. BT SPI Read/Write Transaction—16-bit Alignment

SPI Header	SPI Paylod (HCI Command)	Padding Byte
5 bytes	Odd	None
5 bytes	Even	0x00

The host must assert $\overline{CS}$ (that is, drive the signal to low) before sending data on the DI line.

After completing its wake-up sequence, the BT device asserts the IRQ line to inform the host that it is ready.(1)

If the Bluetooth device is awake, the IRQ line is asserted immediately (within ≤250ns). When the BT device detects the HCI packet header, it de-asserts its IRQ line. When the host completes the SPI transaction, it must de-assert its $\overline{CS}$ line.

Note: The host can wake up the Bluetooth device by generating a pulse on the $\overline{CS}$ line or performing a write transaction.

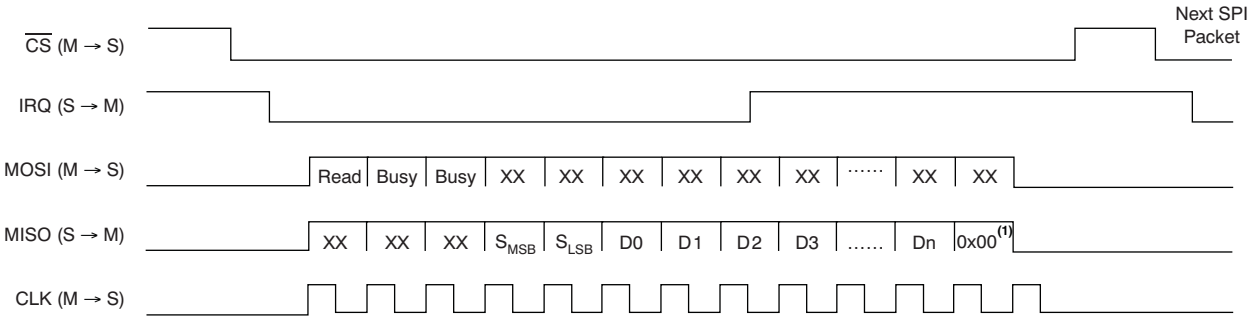
The write transaction is performed according to the following parameters:

- A complete HCI packet must be included within every SPI transaction. However, the HCI header and HCI payload may be sent in different SPI transactions.
- The number of bytes for each SPI transaction will always be even.
- The padding byte is added at the end of the HCI packet, but is not reflected in the HCI header length parameter (H4 packet length ignores this byte).
- The BRF63xx will ignore the additional byte.

(1) The wake-up sequence period depends on whether or not the external fast clock is available; the external fast clock is configurable by the HCI_VS_Fast_Clock_Configuration command. Refer to the *BRF6350 HCI Vendor-Specific Command* document (SWRU115).

5.1.3 Read Operation—BRF63xx to Host Data Transfer

Figure 3 shows the BTSPI read transaction timing.



(1) Padding byte for 16-bit alignment, if required.

Figure 3. BTSPI Read Transaction

SPI Header:

Read	=	Opcode for write is 0x03
S_{MSB}, S_{LSB}	=	16-bit data payload length (including alignment byte)
Busy	=	Busy byte (0x00)

SPI Payload (equal to the HCI command + padding byte):

D(0) … D(n)	=	0x00 (depending of number of bytes in SPI payload)

In order for the total SPI packet (that is, the SPI transaction) to be 16-bit aligned, the HCI event sent from the BT device is padded with an additional 0x00 byte (if required). Refer to Table 3 for more information.

The BT device signals to the host its desire to transfer data by asserting the IRQ line. The host asserts $\overline{CS}$ and performs a read transaction. Upon completing the read transaction, the host must de-assert $\overline{CS}$. The Bluetooth device then de-asserts its IRQ line immediately as a response (within ≤250ns).

Note: The host should be set to trigger on high to low edge.

The read transaction is performed according to the following parameters:

- A single BTSPI read transaction includes a full HCI packet.
- The number of bytes for each SPI transaction will always be even.
- The padded byte is added at the end of the HCI packet, but is not reflected in the HCI header length parameter (H4 packet length ignores this byte).
- The host should read a full SPI packet (including the alignment byte) according to the SPI packet length (S_{MSB} and S_{LSB}).
- **The host must ignore the additional byte according to the HCI packet length.**

Refer to Appendix B for the BTSPI read and write timing diagrams.

6 Clock Polarity

The polarity of the clock used by the SPI protocol can be switched by initiating a vendor-specific command, **HCI_VS_TI_SPI_Configuration**, through the SPI interface (refer to Appendix A for a detailed description of this command).

The switching command must be sent using the default clock polarity as described in Figure B-1 and Figure B-2, but the polarity can be switched for subsequent transactions..

7 Shared SPI Bus Mode

This section describes the TI solution for a system in which the SPI host controller interfaces with both Bluetooth (BRF63xx) and WLAN (WL1251) devices.

The topology includes one SPI master and an SPI bus shared by several slaves. The bus topology has a single master (Host) and multiple slaves (WLAN and Bluetooth devices). The following lines are common to all SPI devices in the system:

- CLK
- Data IN
- Data OUT—when this line is shared between the different devices, it must be set to tri-state when $\overline{CS}$ is de-asserted via the vendor-specific command, **HCI_VS_TI_SPI_Configuration** (refer to Section 9)

Figure 4 illustrates the shared SPI bus architecture.

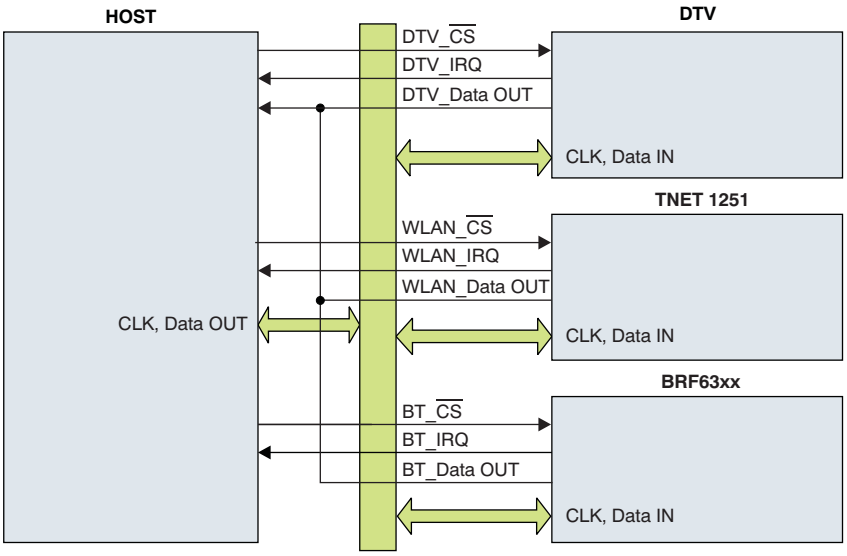


Figure 4. Shared SPI Bus Topology

8 Initialization Commands for BTSPI

In order for the BRF63xx to operate using BTSPI protocol, the following commands must be sent to the device. These commands must be sent in the specified order:

1. When working in non-shared mode:
```
Send_HCI_VS_TI_SPI_Configuration 0xFD41, 0, 1, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0
Wait_HCI_Command_Complete_VS_TI_SPI_Configuration_Event 5000, any,
HCI_VS_TI_SPI_Configuration, 0x00
```

   When working in shared mode:
```
Send_HCI_VS_TI_SPI_Configuration 0xFD41, 0, 1, 0, 1, 0, 1, 0, 0, 0, 0, 0, 0, 0
Wait_HCI_Command_Complete_VS_TI_SPI_Configuration_Event 5000, any,
HCI_VS_TI_SPI_Configuration, 0x00
```

   Whether working in shared or non-shared mode, this command must be the first command sent to the BRF63xx (even before the initialization script). Refer to Appendix A for a HEX dump example of this command.

> **CAUTION**
>
> The normal SPI host write sequence is $\overline{CS}$ low (host → BRF63xx device), followed by IRQ low (BRF63xx device → host), indicating that the BRF63xx device is ready to accept data. However, after power-up, IRQ goes low automatically to indicate that device power up is complete—it is the same line as RTS.
>
> Therefore, for the first command only, the host cannot rely on the IRQ line going low. The host must wait for a delay of more than 50µs before sending the SPI packet.
>
> In addition, during this command the BRF63xx device performs its internal processing to switch to the required SPI mode. This processing requires an additional small amount of time. Therefore, for the first command only, a short delay is required after the first four bytes and before the following 21 bytes. This delay must also be greater than 50µs.

2. Enabling the deep-sleep protocol:
```
Send_HCI_VS_Sleep_Mode_Configurations 0xFD0C, 1, 1, 0x06, 0xFF, 0xFF, 0xFF, 0, 100
Wait_HCI_Command_Complete_VS_Sleep_Mode_Configurations_Event 5000, any,
HCI_VS_Sleep_Mode_Configurations, 0x00
```
3. All the commands of the most recent initialization script
4. Other platform-related commands

9 Related Commands

The following vendor-specific commands are used for SPI mode. For additional details, refer to the application notes *BRF6350 HCI Vendor-Specific Command* (SWRU115) and *BRF6300 Vendor-Specific Commands* (BT-SW-0030).

- HCI_VS_Sleep_Mode_Configurations
- HCI_VS_TI_SPI_Configuration

10 References

Table 4 lists some of the reference documents that are recommended to the user for additional information.

Table 4. Reference Documents

Document	Reference
BRF63xx Product Review Rev 0.41	BT-DS-0023
BRF6300 Vendor-Specific Commands	BT-SW-0030
BRF6350 Vendor-Specific Commands	SWRU115

Appendix A Sample Commands Hex Dump

HCI_VS_TI_SPI_Configuration Command (non-shared mode):

01 00 15 00 00 01 41 fd 11 00 01 00 00 00 01 00 00 00 00 00 00 00 00 00 00

The first five bytes (in **bold**) are the SPI header. The last 21 bytes are the HCI_VS_SPI_Configuration command bytes.

Command Complete for VS TI SPI:

03 00 00 00 09 00 0E 04 01 05 FD 41 00

Read BD address:

01 00 05 00 00 00 09 01 00 10

Command Complete of read BD address:

03 00 00 00 0f 00 0E 04 01 0A 10 09 61 00 69 67 47 69 97 -

Write Scan Enable:

01 00 07 00 00 00 1A 01 01 0C 03 00

Command Complete Event for write scan enable:

03 00 00 00 09 00 0E 04 01 04 0c 1A 00

Read Scan Enable:

01 00 05 00 00 00 19 01 00 0C

Command Complete for Read Scan Enable:

03 00 00 00 09 00 0E 04 01 05 0c 19 03 00

Max slots 5 event:

03 00 00 00 07 00 1b 04 01 03 05 00

Appendix B Timing Information

Figure B-1 and Figure B-2 show the BTSPI write and read timing sequence, respectively. Table B-1 defines the BTSPI read/write timing parameters.

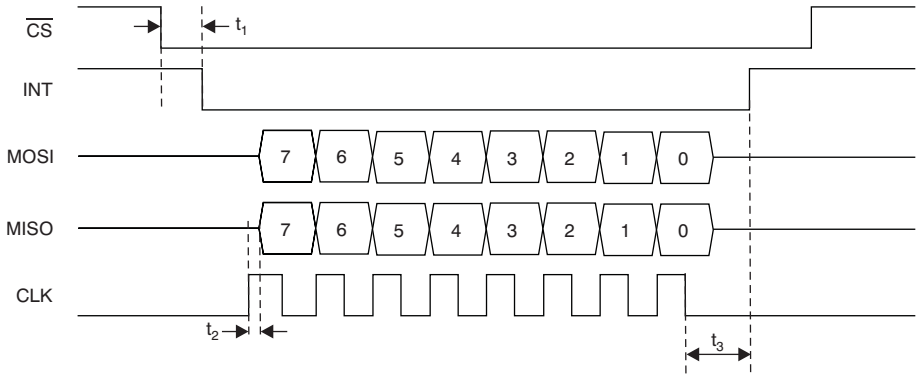


Figure B-1. BTSPI Write Timing

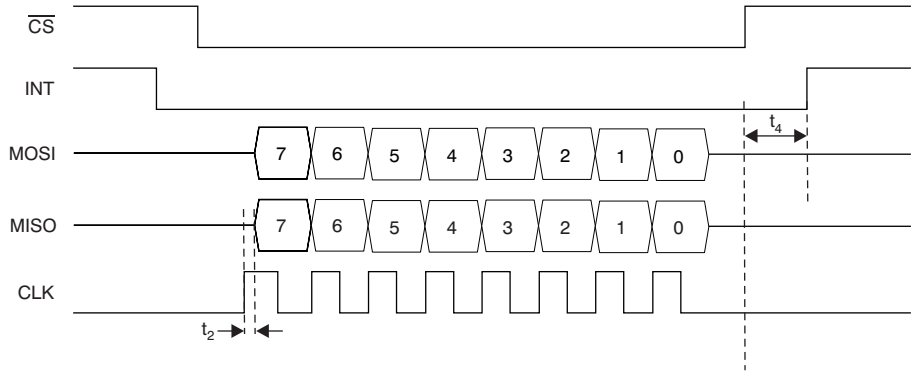


Figure B-2. BTSPI Read Timing

Table B-1. BTSPI Read/Write Timing

Time	Result (Typ)
t_1	142ns
t_2	11ns
t_3	1170ns
t_4	135ns

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