BRF6300 Starter-Kit

User Manual

Revision 0.1

July 6, 2005

BT-UM-0048

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1. Introduction

The Starter Kit provides both a demonstration platform and a development environment for a variety of Bluetooth™ products.

The Starter Kit allows users to easily develop their application using the Bluetooth™ protocol and allows the integration of Bluetooth™ functionality with various host applications.
The Starter Kit contains all the necessary tools to enable easy development and is designed in a manner that provides easy migration to final product.

The Starter Kit Hardware consists of 2 boards:

- BTM – Bluetooth™ Module
- GIB – Generic Interface Board

1.1. Bluetooth™ Module (BTM)

The BTM holds the TI BRF6300 single chip along with a BALUN, matching network, decoupling capacitors, BT antenna, SMA connector for RF testing and an RF switch to choose between antenna and SMA. There are several BTM versions:

Bluetooth™ Module I (BTM - I) – Bluetooth™ Module based on the BRF6300 chip in 4.5x4.5 package. This is a general-purpose BT module

Bluetooth™ Module II (BTM - II) – future

1.2. Generic Interface Board (GIB)

This board holds the Bluetooth™ Module (BTM) and provides it with needed power and clocks. It contains all peripherals needed to communicate with the BRF6300 as well as providing a platform for measurement of power consumption.
The main interfaces are:

- RS232 or USB HCI port for connecting to a PC host
- RS232 or USB debug trace port for capturing BRF6300 baseband traces using a PC host
- Host connectors for interfacing to a host board
- Mono / Stereo CODECs with mono / stereo headset jack and Line IN / Line Out jack.
- BTM connectors and interface
- Current measurement interface
- IO pull up / pull down selection jumpers

1.3. Working Configurations

The GIB provides extensive flexibility for supporting different work configuration needs, via on-board peripherals and support for different BT modules.

The default power (3.3V) for VDD_IN provided by the GIB can be changed by changing resistor values on board (see 7.2).

External host interface supports host I/O voltage equal to or less than the BTM voltage,with no changes required to board. Level shifters on the GIB achieve this.

BTM signals can be directed either to the host interface connectors or to the GIB (to RS232 converters, CODEC etc.). For flexibility, signals are divided into 4 groups, where each group can be routed independently to either Host connector or GIB (see 7.8 jumper list).

1.4. Hardware requirements

Item	Comments	Quantity
Host PC running: Windows 2000 or XPe.		1
Serial cable (RS232)	Included in package.	1
Headset	Included in package.	1
DC-adaptor.	Included in package.	1
Main AC cable to the DC-adaptor.	Standard AC appliance connector. Not included in package	1

Table 1: Hardware Requirements

2. Terms & Abbreviations

Abbreviation /Term	Meaning / Explanation
BALUN	Balanced to Unbalanced
BPF	Band Pass Filter
BT	Bluetooth™
BTM	Bluetooth™ Module
CFG	Configuration
FW	Firmware
GIB	Generic Interface Board
GPIO	General Purpose I/O
HCI	Host Controller Interface
Host Application	User application connected to the board through the host connector, or HCI interface.
Host PC	A PC connected to the Starter Kit via the serial port or USB (HCI)
HW	Hardware
LED	Light-Emitting Diode
NC	Not Connected or Not assembled.
PCM	Pulse Code Modulation
PPM	Parts Per Million
PTMP	Point To Multi Point
PTP	Point To Point
RF	Radio Frequency
ROM	Read Only Memory
SK	Starter Kit
SBTM	Supper BTM – future (not implemented) BTM with extended footprint
TCXO	Temperature Compensated Crystal Oscillator
VC-TCXO	Voltage Controlled Temperature Compensated Crystal Oscillator

Table 2: Terms and Abbreviations

3. Documents Reference

Document Description	Reference Number	Revision Number
BRF6300 product Specification	BT-SM-0037	Rev 0.2
HCI commander user manual	BT-UM-0029	Rev 0.2

Table 3: Documents reference

4. System description

4.1. Block diagram

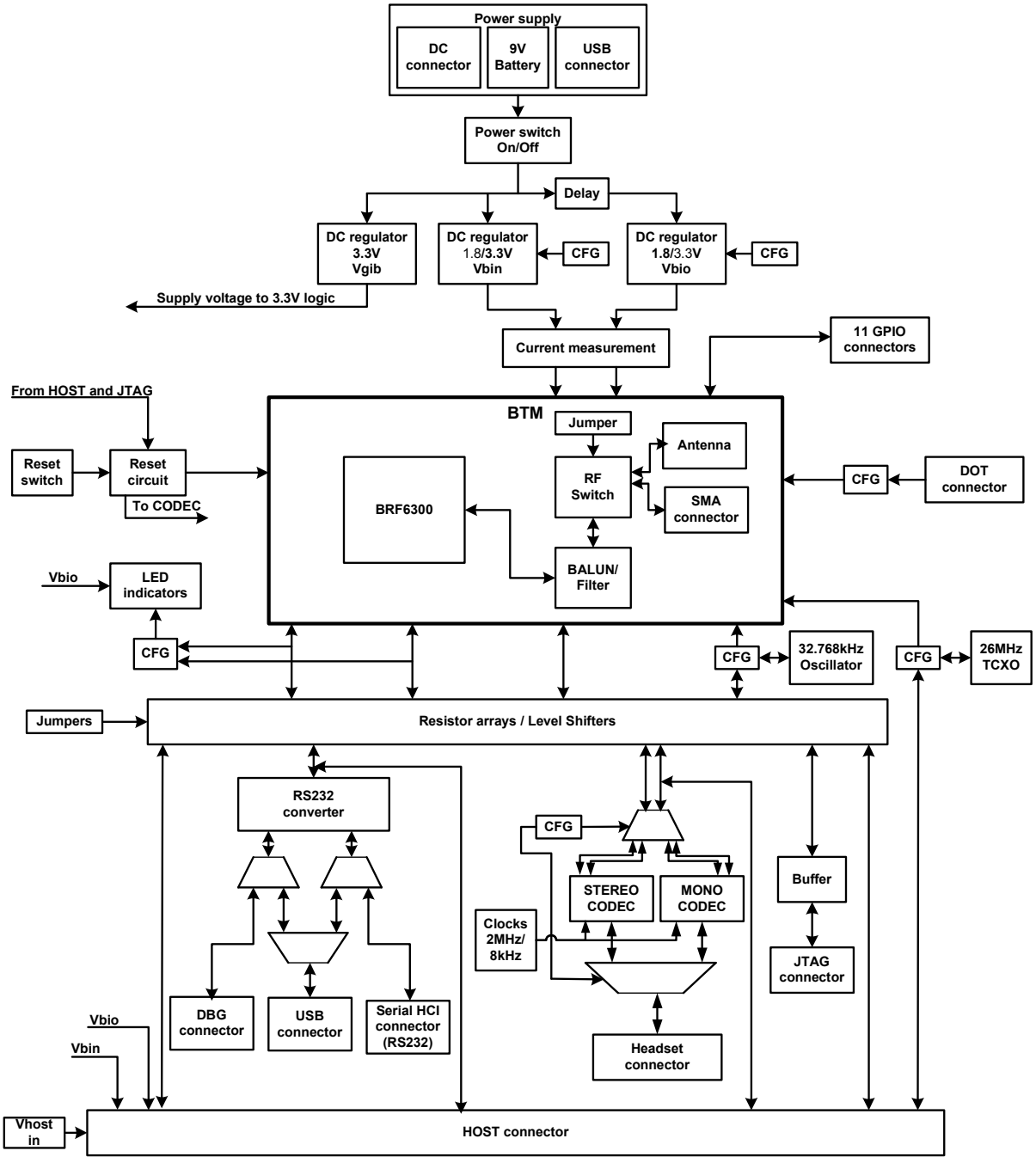


Figure 1: Starter Kit block diagram

4.2. Generic Interface Board (GIB)

This section will describe the different parts of the GIB, which is the mother board for the BTM plug-in module.

4.2.1. Voice interfaces

4.2.1.1. Mono CODEC

TWL1103 - 3V Linear (default), A-Law, μ-Law CODEC with an I^2C control interface (slave to the BRF6300).

HCI Commander has built-in init script to setup the BRF6300 to work with the CODEC default parameters. If any other application is used, the BRF6300 must be configured accordingly using HCI_VS_Write_CODEC_Config_Island3.

4.2.1.2. Stereo CODEC

TLV320AIC23 I2S compatible stereo codec with an I^2C control interface, stereo headphone and Line OUT capability as well as stereo MIC IN and Line IN capability. This CODEC is supplied with its own master clock of 12.288MHz from a dedicated crystal oscillator. It is capable of operating in both Master and Slave modes.

4.2.1.3. CODEC Clocks (2.048MHz / 8kHz)

The BRF6300 can perform as either a PCM master or slave. When setting the BRF6300 to operate as a PCM slave, an on board clock circuit can be used for providing the PCM clocks. A 4.096MHz oscillator divided by 2 generates a PCM clock of 2.048MHz with a 50% duty cycle. Another division by 256 creates Frame Sync of 8KHz. Routing of these clocks to the CODECs is done is done by changing a set of resistors (see 7.4).

4.2.2. RS232 interfaces

4.2.2.1. HCI RS232 Interface (J13)

MAX3245 provides conversion of 3.3V and RS232 levels. It provides:

- Com port connection to a PC Host (RX and TX)
- HW flow control (CTS/RTS)
- Power management control (DTR/DSR)

4.2.2.2. Debug RS232 Interface (J14)

MAX3245 provides conversion of 3.3V and RS232 levels. It provides:

- Com port connection to PC based Logger utility.

4.2.3. Clocks

4.2.3.1. 26MHz TCXO

20 PPM Fast clock to the BTM provided from a VC-TCXO.

There is an option to provide this clock to the BTM from the Host connector by changing a resistor configuration (see 7.4).

There is also an option to provide this via a SMA connector - selected by JP16.

4.2.3.2. 32.768 kHz oscillator

250 PPM slow clock to the BTM provided by an on board oscillator circuit.

There is an option to provide the clock to the BTM from the Host connector (see 7.4).

4.2.4. DC regulators

Three low-dropout adjustable on-board voltage regulators (TPS7101Q) provide 3 separate voltages:

- Vgib - Peripheral voltage for GIB onboard peripherals like CODEC and RS232 converters etc. (default 3.3V)
- Vbin – BRF6300 core voltage supply
- Vbio – BRF6300 IO voltage supply

Supply to these regulators is provided from the power jack or on-board 9V battery connector, or via USB connector J16.

Vbin can also be supplied from an external unregulated source to emulate direct battery connection. This is done by removing 3-4 and 5-6 jumpers on J4 (to isolate the on-board regulator output from the BTM) and connecting external unregulated source to pin 4 or 6 of J4.

4.2.5. Level shifter

MAX3378E – 9 low voltage, bi-directional level translators for supporting 1.8/3.3V mixed voltage system. This allows interfacing of the BTM IO to the host IO, with different voltage levels on each side. An option exists for bypassing each level shifter using a 0R resistor array.

Note: If no host suplly is provided, 3.3V is automatically supplied as Vhost. In addition, the level shifters' outputs to the BTM and host connectors can be tri-stated via jumpers.

4.2.6. Indication LEDs

Two indications LED's are mounted on the GIB in order to give some information on the Starter Kit status:

- **Blue Green LED (D5) -** indicates power is applied to the board
- **Blue LED (D4) –** controlled by the BTM RTS_HCI signal and indicates that the BRF6300 is up and ready (when RTS_HCI goes low)

4.2.7. Host Interface

The GIB provides an interface for connecting the BRF6300 BTM to a host board via a set of Host connectors. All the BTM signals are routed to the Host connectors via level shifters. This allows direct drive of the BTM from the customer application board. If no level shifting is needed, the level shifters can be bypassed using 0R resistor banks.

4.2.8. GPIO connectors

There are eleven GPIO connectors located on the GIB serving as a pull-up / pull-down area for BRF6300 IO signals (see 6.12 for additional details)

Connector type: Header 1x3 (JP3, JP4, JP5, JP6, JP8, JP10, JP11, JP12, JP13, JP14, JP15)

4.2.9. Debug RS232 DB9 connector (J14)

Used for logging BRF6300 Baseband messages. J14 provides access to the BRF6300 baseband traces at RS232 levels for interfacing to a PC com port.

4.2.10. RS232 converter connector (J15)

J15 provides the ability to convert external RS232 level signals to logic levels and vice versa, using spare I/O on a MAX3245.(see 6.11 for additional details)

4.2.11. JTAG connector (J17)

Allows for TI internal SW debugging and testing.

Connector type: Header7x2

4.3. Bluetooth Module (BTM)

The BTM contains an onboard antenna for ease of use of the Starter Kit as a Bluetooth™ device. It also provides an RF interface to the BRF6300 via an SMA connector (J1). The SMA connector allows for easy hookup to RF measuring instruments for full RF evaluation.

Selection between SMA and Antenna can be achieved using J2 (closed by default, meaning on board antenna is connected).

A set of resistors RNR1 and RNR2 can be populated appropriately to bypass the RF switch and connect the RF signal applied at the SMA connector directly to the BALUN. This allows avoiding the insertion loss introduced by the additional path when going through the RF switch. By default, RNR1 and RNR2 are configured to use the RF switch in the path.

The insertion loss introduced by the RF switch is ~0.8 dB at 2.5GHz.

4.4. Board layout

4.4.1. GIB layout

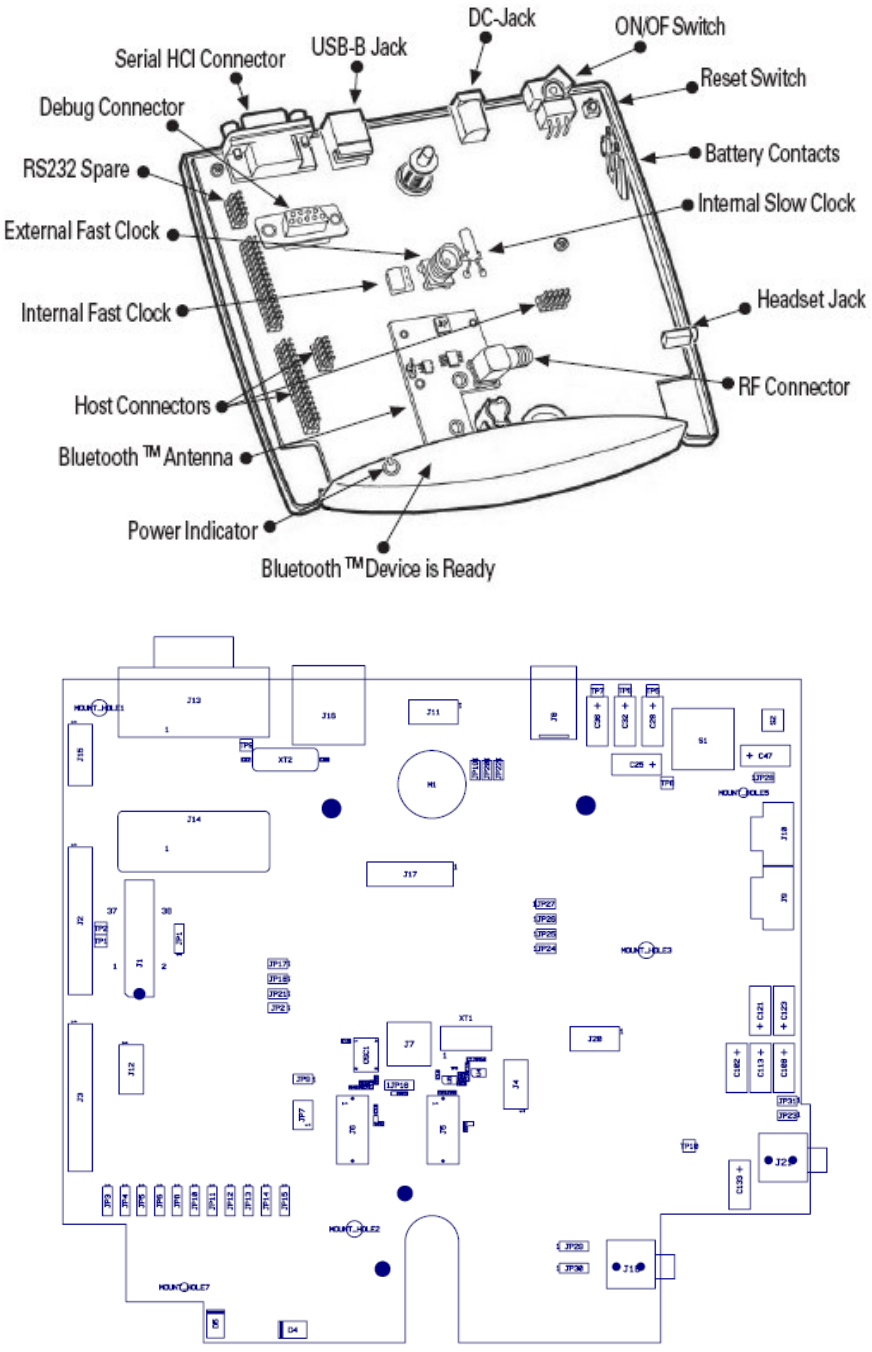


Figure 2: GIB layout

4.4.2. BTM – I layout and description

Illustration only. This board's layout may change from time to time. Please refer to the respective schematics portion of the CD for the updated placement.

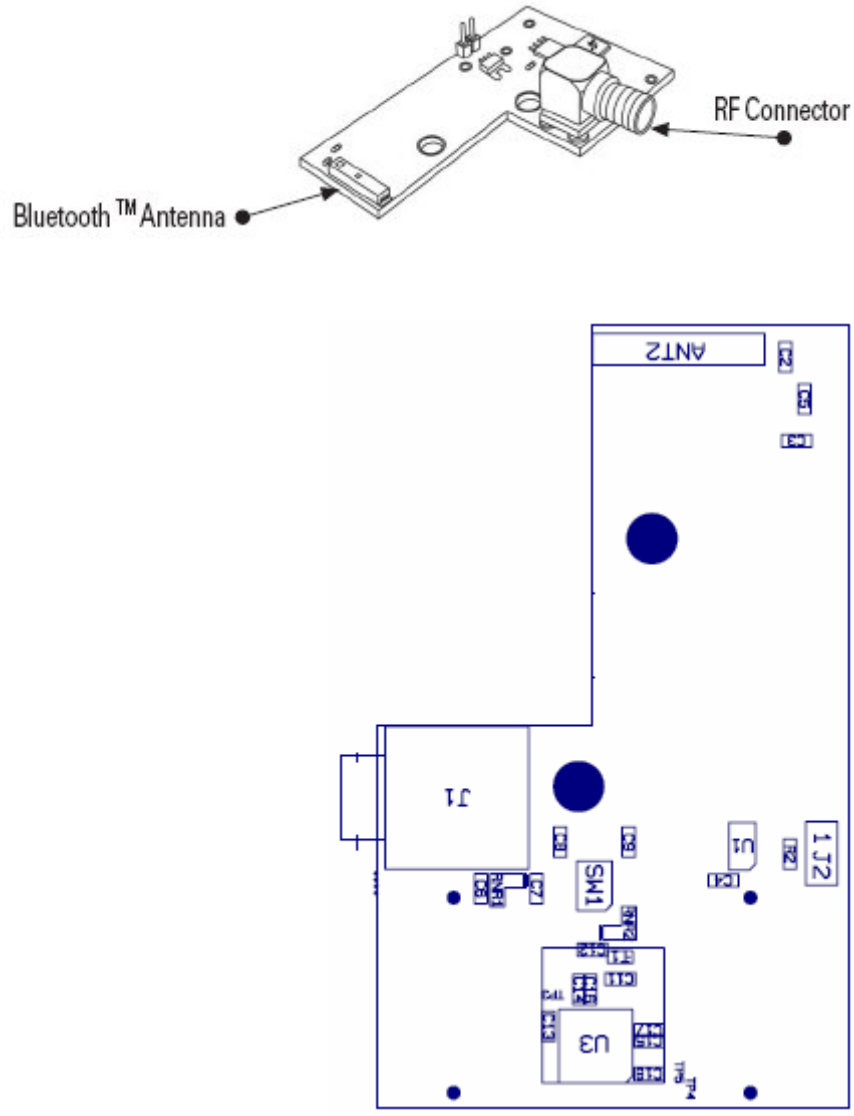


Figure 3: BTM-I layout

5. Getting started

The following is required to activate the Starter Kit platform:

5.1. Installing the software package

The CD included in the package contains:

- Documentation
- Schematics and placement
- Firmware
- Scripts (for the HCI commander tool)
- Setup.exe for the PC tools

Please refer to the Readme.txt on the CD root directory for the detailed structure of the CD.
Install the package from the CD to obtain the TI PC tools (HCI Commander and Flash Update Utility).
After installation, the TI tools as well as their User Manuals should be available at:
C:\Program Files\Texas Instruments\Bluetooth Tools
An HCI Commander icon should appear on the Quick Launch bar as well.

The HCI Commander is a user-friendly tool which allows Bluetooth inquiring for remote devices, connecting, creating voice links, etc. It also provides a simple way for sending scripts for different dedicated operations (like putting a device in test mode).

When new scripts are available, they need to be copied to the location of the HCI Commander application (should be in "C:\Program Files\Texas Instruments\Bluetooth Tools\ ").

The Flash Update Utility allows updating the BRF6300 Firmware via the HCI UART connection (BRF6300 stacked ram or external ram modules only).

To use these tools, refer to the User Manuals included.

5.2. Preparing the Starter Kit for use

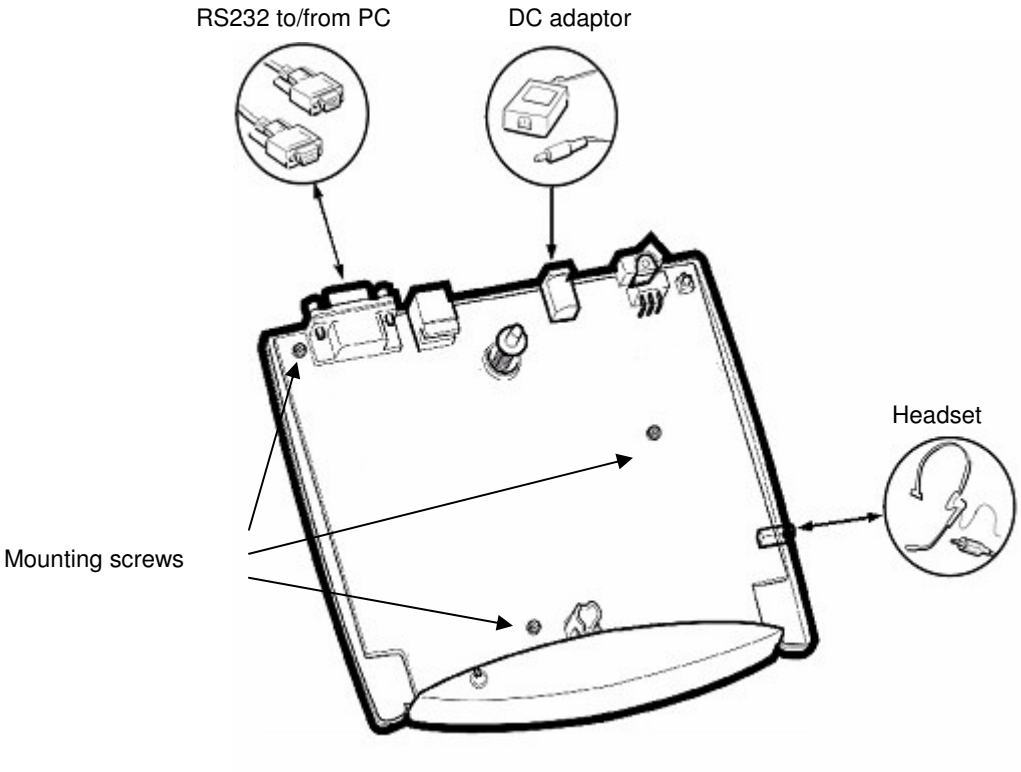


Figure 4: Cable inserts description

- Configure the jumpers for using either the USB or RS232 port for HCI connection with PC. Connect appropriate connector from starter kit to PC.
- Apply power to the Starter Kit
- Connect the headset.
- Run the HCI Commander tool and select the correct port (COM or USB) for communication with the starter kit.
- Using the tool, Inquire for other devices and connect to them (easily done with another TI Starter Kit run by an HCI Commander)

6. Connectors & Interfaces

6.1. BTM/GIB interface (J5 and J6 on GIB)

The BTM mounts on the GIB using two connectors – J5 and J6. All signals at the two connectors are labeled on the GIB schematic with a *_btm* to distinguish them.

Signal name	J5/J6 pin #	Direction	Description
PCM (CODEC) interface			
AUD_IN	JP5-10	GIB → BTM	CODEC audio data input
AUD_OUT	JP5-6	GIB ← BTM	CODEC audio data output
AUD_FSYNC	JP5-4	GIB ↔ BTM	CODEC frame synchronization control
AUD_CLK	JP5-8	GIB ↔ BTM	CODEC transmit/receive clock
HCI RS232 interface			
HCI_RX	JP5-11	GIB → BTM	HCI Data Receive
HCI_ TX	JP5-13	GIB ← BTM	HCI Data Transmit
HCI_ CTS	JP5-9	GIB → BTM	HCI Clear-To-Send
HCI_ RTS	JP5-7	GIB ← BTM	HCI Request-To-Send
Debug RS232 interface			
TX_DBG_UART	JP5-3	GIB ← BTM	Debug Data Transmit
Clocks and Reset			
SLOW_CLK_IN	JP5-17	GIB → BTM	32kHz Clock input
XTALP_FAST_CLK_IN	JP6-10	GIB → BTM	Fast oscillator in
NSHUT_DOWN	JP6-16	GIB → BTM	Active low reset/shutdown input
General I/O			
CLK_MODE_SEL	JP5-18	GIB → BTM	Clock Request Active high/low select
IO0-ETX_CLK_REQ_OUT	JP5-26	GIB ← BTM	GPIO0 / external clock request out
IO15-EXT_CLK_REQ_IN	JP5-25	GIB ↔ BTM	GPIO15 / external clock request in
IO17-SCL	JP5-29	GIB ↔ BTM	GPIO17 / I^2C Clk
IO3-SDA	JP5-27	GIB ↔ BTM	GPIO3 / I^2C Data
IO4	JP5-12	GIB ↔ BTM	GPIO4
IO1	JP5-16	GIB ↔ BTM	GPIO1
IO7	JP5-5	GIB → BTM	GPIO7
IO14	JP6-3	GIB ↔ BTM	GPIO14
IO5	JP6-5	GIB ↔ BTM	GPIO5
IO2	JP5-14	GIB ↔ BTM	GPIO2
IO16	JP6-4	GIB ↔ BTM	GPIO16
JTAG interface			
TDI	JP6-9	GIB → BTM	JTAG Test Data In
TMS	JP5-24	GIB → BTM	JTAG Test Mode
TCK	JP6-18	GIB → BTM	JTAG Test Clock
TDO	JP5-23	GIB ← BTM	JTAG Test Data Output

Power			
VDD_DAC	JP6-7		Internal DAC supply voltage
VDD_IN	JP5-31,33,35,37 JP6-32,34,36,38		Internal power supply
VDD_IO	JP5-28,30,32,34,36,38 JP6-27,29,31,33,35,37		Power supply for IO buffers
GND	JP5-1,2,19,20,21,22,39,40 JP6-1,2,19,20,21,22,23,24,25,26,39,40		Digital ground

Table 4: BTM/GIB interface

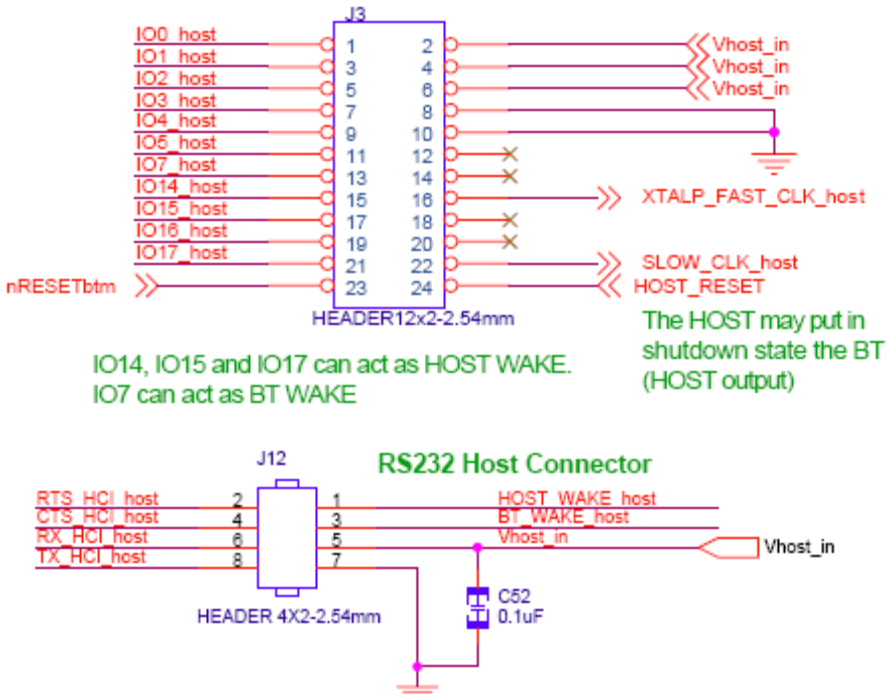
6.2. Host connector (J3, J12 and J20)

The Host interface is divided into three signal groups – HCI (J12), Audio/ I^2C (J20) and IO (J3). These three connectors located on the GIB include all options for interfacing to a host board. All signals at the three connectors are labeled on the GIB schematic with a *_host* to distinguish them. The host interface signals are level shifted to the host supply voltage that can be applied at one or many places on the GIB including the connectors J3/J12/J20.

J20			
Pin no	**Signal name**	**Direction**	**Description**
5	AUD_IN	Host → BTM	CODEC Audio Data Input
3	AUD_OUT	Host ← BTM	CODEC Audio Data Output
4	AUD_CLK	Host ↔ BTM	CODEC transmit/receive clock
6	AUD_FSYNC	Host ↔ BTM	CODEC frame synchronization control
2	IO17-SCL	Host ↔ BTM	GPIO17 / I^2C Clk
1	IO3-SDA	Host ↔ BTM	GPIO3 / I^2C Data
8	GND		Ground
7	Vhost_in	Host → BTM	Power supply from host
J12			
Pin no	**Signal name**	**Direction**	**Description**
6	RX_HCI	Host → BTM	HCI RS232 Data Receive
8	TX_HCI	Host ← BTM	HCI RS232 Data Transmit
2	RTS_HCI	Host ← BTM	HCI RS232 Request-To-Send
4	CTS_HCI	Host → BTM	HCI RS232 Clear-To-Send
1	HOST_WAKE	Host ← BTM	Host wakeup signal to host
3	BT_WAKE	Host → BTM	BT wakeup signal from host
5	Vhost_in	Host → BTM	Power supply from host
7	GND		Ground
J3			
Pin no	**Signal name**	**Direction**	**Description**

16	HOST_XTALP_FAST_CLK	Host ↔ BTM	Fast clockoscillator in/out
8, 10	GND		Ground
2, 4, 6	Vhost_in	Host → BTM	Power supply from host
12, 14, 18, 20	NC		Not connected
22	HOST_SLOW_CLK	Host ↔ BTM	32.768kHz Clock in/out
23	IO0-ETX_CLK_REQ_OUT	Host ↔ BTM	GPIO0 / external clock request out
24	HOST_RESET	Host → BTM	Reset from the Host (to shut down the BTM)
1	IO0	Host ↔ BTM	GPIO2 / I^2C Clk
3	IO1	Host ↔ BTM	GPIO1 / external clock request in
5	IO2	Host ↔ BTM	GPIO4 / NEMU0
7	IO3	Host ↔ BTM	GPIO3
9	IO4	Host ↔ BTM	GPIO4
11	IO5	Host ↔ BTM	GPIO5
13	IO7	Host ↔ BTM	GPIO7
15	IO14	Host ↔ BTM	GPIO14
17	IO15	Host ↔ BTM	GPIO15
19	IO16	Host ↔ BTM	GPIO16
21	IO17	Host ↔ GIB	GPIO17
23	NRESET_btm	Host ← BTM	Iindication to the HOST that BTM is in shut down state

Table 5: Host connectors



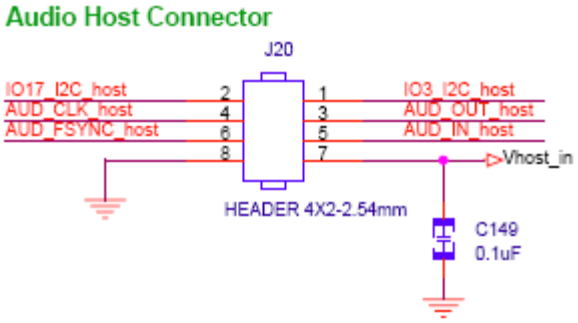


Figure 6; Host Connectors – J3/J12/J20

6.3. Headset jack (J21)

The headset jack J21 is a 6-pin jack that can be used with either a mono or stereo headset, depending on the configuration set on the GIB by JP23.

JP23	Description
Closed	Mono CODEC selected and MONO headset signals available for configuration on headset jack using J31
Open	Stereo CODEC selected and STEREO headset signals available for configuration on headset jack using J31

Table 6: Mono/Stereo CODEC selection

Additionally, depending on the setting of JP31, the signals that connect to J21 can be changed in either mode. This allows for two configurations each, for a mono or a stereo headset.

JP31 = OPEN	Config: Mono1/Stereo1	
J21 Pin #	**Signal Connected**	**Notes**
1 (&2) (shorted)	Headset_Right	For mono headset, this is NC
3 (&4) (shorted)	MIC_in	Same for mono or stereo
5	Headset_Left	For mono headset, this is Headset_out
6	GND	Ground

JP31 = CLOSED	Config: Mono2/Stereo2	
J21 Pin #	**Signal Connected**	**Notes**
1 (&2) (shorted)	Headset_Left	For mono headset, this is Headset_out
3 (&4) (shorted)	MIC_in	Same for mono or stereo
5	GND	Ground
6	Headset_Right	For mono headset, this is NC

Table 7: Headset jack signal configuration

6.4. Line IN / Line OUT jack (J18)

The stereo Line IN / Line OUT jack is a 6-pin jack that can be used as either Line IN or Line OUT, but not both simultaneously. This function is only available when using the stereo CODEC. The configuration can be set using JP29 and JP30. Please note that JP29 and JP30 should have the same settings (any other configuration is invalid).

JP29 & JP30 both closed on 1-2	Config: LINE IN	
J18 Pin #	**Signal Connected**	**Notes**
2, 3, 5	NC	Pins 1-4 are not connected
4	LIN	Left channel Line IN
1	RIN	Rt channel Line IN
6	GND	Ground
JP29 & JP30 both closed on 2-3	**Config: LINE OUT**	
J21 Pin #	**Signal Connected**	**Notes**
2, 3, 5	NC	Pins 1-4 are not connected
4	LOUT	Left channel Line OUT
1	ROUT	Rt channel Line OUT
6	GND	Ground

Table 8: Line jack signal configuration

6.5. JTAG connector (J17)

Pin no	Signal name	Direction	Description
1	TMS	JTAG → GIB	JTAG Test Mode Signal
2	JTAG_RST	JTAG → GIB	JTAG reset to FBTM
3	TDI	JTAG → GIB	JTAG Test Data In
4	GND		Ground
5	Vgib		3.3V DC
6	NC		Not assembled
7	TDO	JTAG ← GIB	JTAG Test Data Output
8	GND		Ground
9	TCK_gib		JTAG Test Clock after buffer
10	GND		Ground
11	TCK		JTAG Test Clock
12	GND		Ground
13	NC		Not connect
14	NC		Not connect

Table 9: JTAG connector

6.6. HCI RS232 connector (J13)

Pin no	Signal name	I/O	Comment
1	NC		EIA-RS232C levels
2	TXD_HCI_RS232	Out	
3	RXD_HCI_RS232	In	
4	DSR_HCI_RS232 (BT_Wakeup)	In	
5	GND		

6	DTR_HCI_RS232 (Host_Wakeup)	Out	
7	CTS_HCI_RS232	In	
8	RTS_HCI_RS232	Out	
9	NC		

Table 10: HCI RS232 connector

6.7. Debug RS232 connector (J14)

Pin no	Signal name	I/O	Comment
1	NC		EIA-RS232C levels
2	TXD_DEBUG	Out	
3	NC	In	
4	NC	In	
5	GND		
6	NC	Out	
7	NC	In	
8	NC	Out	
9	NC		

Table 11: Debug RS232 connector

6.8. DC jack (J8)

Pin	Signal name	Voltage range	Min current	Comment
1	V_IN	6-9V	300mA	
2	GND			Ground

Table 12: DC connector

6.9. USB connector (J16)

Pin no	Signal name	Comment
1	V_USB	5V (supplied when connected to a USB host)
2	USB_D_N	D- USB signal
3	USB_D_P	D+ USB signal
4	GND	Ground

Table 13: USB connector

6.10. Battery connector (J9, J10)

Connector	Signal name	Comment
J9	V_BAT	9V (supplied when 9V battery is attached)
J10	GND	Ground

Table 14: Battery connector

6.11. RS232 Converter connector (J15)

Pin no	Signal name	Comment
1	RS232_IN_1	RS232 level signal in 1
2	RS232_OUT_1	RS232 level signal out 1
3	RS232_IN_2	RS232 level signal in 2
4	RS232_OUT_2	RS232 level signal out 2
5	LOGIC_OUT_2	Vgib level signal out 2
6	LOGIC_IN_2	Vgib level signal in 2
7	LOGIC_OUT_1	Vgib level signal out 1
8	LOGIC_IN_1	Vgib level signal in 1
9	GND	Ground
10	GND	Ground

Table 15: Spare RS232 connector

6.12. GPIO Jumpers

Connector	Pin no	Signal name	Description
JP3	1	Vbio	Power supply for BTM IO
	2	IO0-ETX_CLK_REQ_OUT	GPIO0 / external clock request out
	3	GND	Ground
JP4	1	Vbio	Power supply for BTM IO
	2	IO1	GPIO1
	3	GND	Ground
JP5	1	Vbio	Power supply for BTM IO
	2	IO2	GPIO2
	3	GND	Ground
J6	1	Vbio	Power supply for BTM IO
	2	IO3-SDA	GPIO3 / I^2C Data
	3	GND	Ground
J8	1	Vbio	Power supply for BTM IO
	2	IO4	GPIO4
	3	GND	Ground
J10	1	Vbio	Power supply for BTM IO
	2	IO5	GPIO5
	3	GND	Ground
J11	1	Vbio	Power supply for BTM IO
	2	IO7	GPIO7
	3	GND	Ground
J12	1	Vbio	Power supply for BTM IO
	2	IO14	GPIO14
	3	GND	Ground
J13	1	Vbio	Power supply for BTM IO
	2	IO15-EXT_CLK_REQ_IN	GPIO15 / external clock request in
	3	GND	Ground
J14	1	Vbio	Power supply for BTM IO
	2	IO16	GPIO16
	3	GND	Ground
J15	1	Vbio	Power supply for BTM IO
	2	IO17-SCL	GPIO17 / I^2C Clk
	3	GND	Ground

Table 16: GPIO jumpers

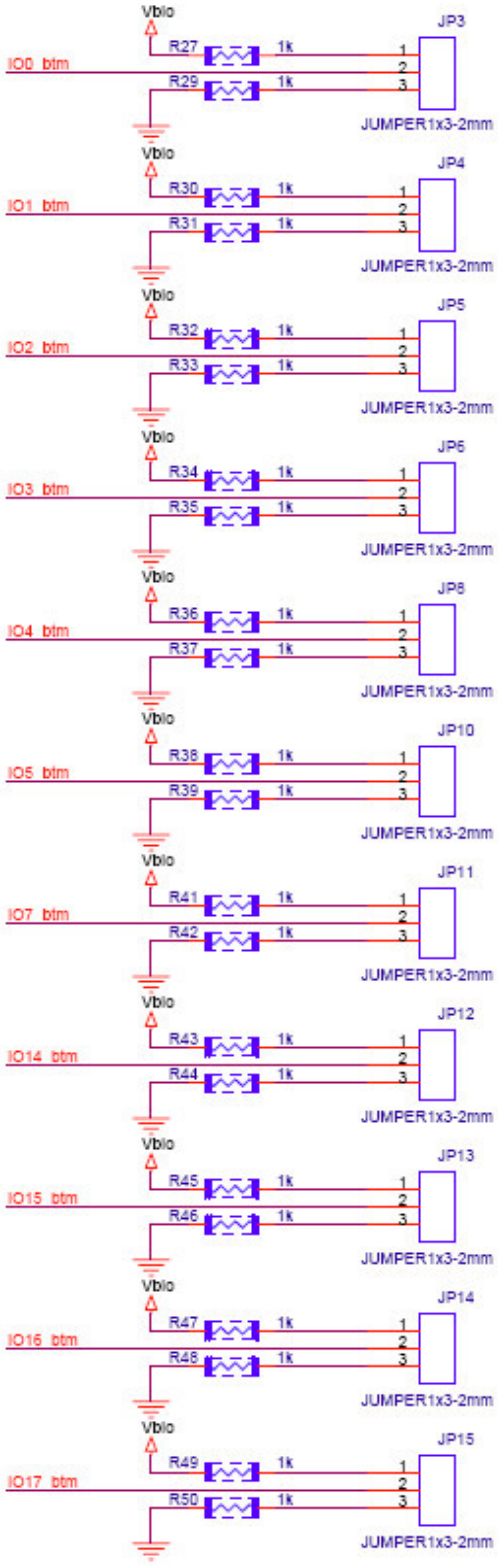


Figure 7: GPIO Jumpers

6.13. Power connector (J11)

Pin name	Signal name	Comments
1	Vdcb	Power supply source voltage
2	Vbio	BTM IO supply voltage
3	Vgib	GIB supply voltage
4	Vhost	Voltage to level shifters on host interfaces (if no Vhost_in, Vgib is used by default).
5	Vfast	Fast clock oscillator power supply
6	Vhost_in	Power supplied by Host board
7	Vbin	BTM core supply voltage
8	GND	Ground

Table 17: Power Connector

6.14. Test Points

Test Point name	Test Point no	Comments
GIB		
FPGA_IO_5	TP1	FPGA IO 5 signal on J1 (DOT interface connector)
FPGA_IO_6	TP2	FPGA IO 6 signal on J1 (DOT interface connector)
SLOW_CLK	TP3	32.768 kHz slow clock (or inverted slow clock)
Vgib	TP5	GIB supply voltage
Vbin	TP6	BTM core supply voltage
Vbio	TP7	BTM IO supply voltage
nRESET	TP8	Active low reset for BTM
CLKOUT	TP9	USB to RS232 converter (U29) clock output
CLKOUT_TEST	TP10	Stereo CODEC clock (U39) output
BTM		
ANATEST1	TP3	IF test
ANATEST2	TP4	IF test
PMTST	TP5	Power Management test

Table 18: Test Points

6.15. DOT interface connectors

The DOT interface connectors J1 and J2 are reserved for TI use only - not intended for customer use. Additionally, JP1 is reserved for use with J1 and J2.

7. System Configuration

7.1. Power Supply

The Starter Kit requires external power supply of 6-9V with a minimum of 300mA current supply. The power supply is included in the SK package; however the AC cable (which is country specific) is not. Any "PC like" power cable will do.

Number	Type	Polarity	Description
J8	DC jack	Center: + Sleeve: -	6-9V, minimum 300mA external supply common for DC adaptors.

Table 19: Power supply (J8)

7.2. Power Supply Configuration

Power configuration is preset and does not need to be changed unless there is a specific need to interface to a host board with a specific voltage level. The following information is for reference only on how power supply options are set for the GIB. It is, however, recommend that power supply settings not be changed.

The following power rails are available on the Starter kit:

- Vgib – Default Voltage for all devices on the GIB
- Vbin – BRF6300 core voltage
- Vbio – BRF6300 IO voltage
- Vfast – Voltage for the Fast Clock Oscillator (Vfast = Vgib)
- Vdcb – Power supply source voltage (DC in or USB or 9V battery)
- Vhost – Power supply for level shifters when connecting to a host board (default is Vhost=Vgib)

Power configuration			Description
Default configuration	Vgib	3.3V	Regulated power supply from DC-jack, USB connector or from on board battery. For information refer to GIB schematic Power page.
	Vbin	3.3V	
	Vbio	1.8V	

Table 20: Power configuration

The table below shows the required resistor values for different GIB voltage levels.

Vbin/Vbio				
	R73/R81	R77/R85	R76/R83	R78/R86
1.6V	6.8k	18k	N.C.	N.C.
1.8V	10k	18k	N.C.	N.C.
2.0V	10k	18k	68k	8.2k
2.7V	10k	18k	0	13k
3.0V	10k	18k	0	10k
3.3V	10k	18k	0	8.2k
3.6V	10k	18k	0	6.8k

Table 21: Voltage levels configuration

R70 and R75 can be used to redirect Vgib, Vbin and Vbio, if required..

7.3. Indicator LED Configuration

There are two LEDs on the starter kit GIB.

The Green LED indicates power is applied to the GIB. The Blue LED default control is the BTM signal RTS_HCI. When connected to the RTS_HCI (default), The Blue LED turns on after power up to indicate that the BRF6300 FW is up and ready.

7.4. Clock Source Configuration

The BRF6300 chip requires two clocks – Fast clock (12MHz – 40MHz) and slow clock (32.768 kHz). The fast clock can be selected by changing jumpers or resistors on the GIB. Default setting is done by jumper.

The mono CODEC TWL1103 requires two clocks – PCMCLK (2.048MHz, AUD_CLK, PCM data clock) and PCMSYN (8 kHz, AUD_FSYNC, PCM frame synchronization). The clock source for the CODEC can be selected by changing configuration resistors on the GIB.

The stereo CODEC TLV320AIC23 requires three clock signals – MCLK (12.288MHz, crystal oscillator) and BCLK (2.048MHz, AUD_CLK, PCM data clock) and frame sync – LRCIN/LRCOUT (8 kHz, AUD_FSYNC, Left / Right Channel select)

The different configurations are described in the following table:

Clock configuration	Description		
Clocks for BRF6300			
Clocks provided to the HOST	Slow clock	Supplied from an on-board crystal oscillator (32.768kHz) assembled on the GIB (XT1). Assemble R51 (0R).	
	Fast clock	Supplied from an on-board VC-TCXO (26MHz) (OSC1) assembled on the GIB. Assemble R57 (0R).	
		Supplied from an external signal generator on SMA connector J7. Remove C18 and assemble R57. Close JP16:1-3.	
Clocks provided to the BTM	Slow clock	Supplied from crystal oscillator (32.768kHz) (XT1) assembled on the GIB **(Default)**.	
		Remove R53, add R51 (0R).	Supply clock via the Host connector J3:22 (SLOW_CLK_host).
	Fast clock 12-40MHz	Supplied from VC-TCXO (26MHz) assembled on the GIB (OSC1) **(Default)**. Close JP16:1-2.	
		Remove C18, assemble R57. Close JP16:1-2.	Supply clock via the Host connector J3:16 (HOST_XTALP_FAST_CLK).
		Close JP16:2-3.	Supply clock from an external signal generator on SMA connector J7.
Clocks for CODEC TWL1103			
BRF6300 CODEC I/F is Master (Default – set by the HCI Commander init script)	PCMCLK	Supplied by the BRF6300. BTM signal AUD_CLK.	
	PCMSYNC	Supplied by the BRF6300. BTM signal AUD_FSYNC.	

BRF6300 CODEC I/F is Slave	PCMCLK	Connect R165	Supplied from the 2.048MHz clock signal generated on board the GIB. This clock signal also supplies the BRF6300 with the audio clock. BTM signal AUD_CLK.
	PCMSYNC	Connect R167	Supplied from the 8kHz clock signal generated on board the GIB. This clock signal also supplies the BRF6300 with the audio frame sync. BTM signal AUD_FSYNC.
Clocks for CODEC TLV320AIC23			
BRF6300 CODEC I/F is Master (Default – set by the HCI Commander init script)	MCLK	Supplied from an on-board crystal oscillator (12.288MHz) (OSC2) assembled on the GIB.	
	BCLK	Supplied by the BRF6300. BTM signal AUD_CLK.	
	LRCIN/LRCOUT	Supplied by the BRF6300. BTM signal AUD_FSYNC.	
BRF6300 CODEC I/F is Slave	MCLK	Supplied from crystal oscillator (12.288MHz) (OSC2) assembled on the GIB.	
	BCLK	Internally generated by the TLV320AIC23. This clock signal also supplies the BRF6300 with the audio clock. BTM signal AUD_CLK **(default)**. Configure CODEC as master.	
		Connect R165. Configure CODEC as slave.	Supplied from the 2.048MHz clock signal generated on board the GIB. This clock signal also supplies the BRF6300 with the audio clock. BTM signal AUD_CLK.
	LRCIN/LRCOUT	Internally generated by the TLV320AIC23. This signal also supplies the BRF6300 with the audio frame sync. BTM signal AUD_FSYNC **(default)**. Configure CODEC as master.	
		Connect R167. Configure CODEC as slave.	Supplied from the 8kHz clock signal generated on board the GIB. This clock signal also supplies the BRF6300 with the frame sync. BTM signal AUD_FSYNC.

Table 22: Clock configuration

NOTE: The appropriate selection for Mono or Stereo CODEC must be made to ensure clock availability to a particular CODEC. See Table 6 in section 6.3.

7.5. Voice Configuration

Both the mono and the stereo CODECs are set to work with the default power-on settings. For configuring and/or changing the CODEC default settings, an I^2C interface is available on each CODEC. The I^2C interface is connected to the host and BTM I^2C signals.

BRF6300 chip is capable of supporting two simultaneous voice channels (using the I2S format). The stereo CODEC can be used to demonstrate this capability.

Refer to Table 6, Table 7 and Table 8 for details on selecting a particular CODEC. Default selections are: Mono CODEC and LINE IN for Line jack.

7.6. HCI and TX_DBG configuration (USB or RS232) for GIB

The GIB provides USB and RS232 interfaces for use with a PC for both the HCI communication and the TX_DBG signal of the baseband traces. The settings on JP19, JP 20 and JP22 configure how the relevant GIB signals are brought out to the different connectors – J13 (dedicated RS232 connector for HCI signals), J14 (dedicated RS232 connector for TX_DBG) and J16 (USB connector for HCI signals or TX_DBG signal - only one at one time).

Below table lists all the different combinations possible. “N/A” indicates signals not available on any connector.

JP19	JP20	JP22	GIB HCI signals (RTS, CTS, TX, RX)	GIB TX_DBG signal
Open	Open	Open	J13	J14
Open	Open	Close	J13	N/A
Open	Close	Open	J16	J14
Open	Close	Close	J16	N/A
Close	Open	Open	J13	J14
Close	Open	Close	J13	J16
Close	Close	Open	N/A	J14
Close	Close	Close	N/A	J16

Table 23: USB or RS232 select for HCI and TX_DBG on GIB

7.7. Default Jumper Configurations

The following table describes the default configuration for all jumpers. The jumpers are on the GIB unless noted otherwise.

Function	Pins	Default jumper configuration (relevant only when working with the level shifters)
BTM current measurements (J4)	1 – 2 (Vbio)	Connected
	3 – 4 (Vbin)	Connected
	5 – 6 (shunt)	Connected
	7 – 8 (Vgib)	Not connected
Host IO connection to BTM on connector J3 (JP2)	1 – 2 Connection disabled	JP2 connected
Host HCI connection to BTM on connector J12 (JP21)	1 – 2 Connection disabled	JP21 connected
Host audio connection to BTM on connector J20 (JP27)	1 – 2 Connection disabled	JP27 connected
Host I^2C connection to BTM on connector J20 (JP24)	1 – 2 Connection disabled	JP24 connected
CODEC audio connection to BTM (JP26)	1 – 2 Connection enabled	JP26 not connected
CODEC I^2C connection to BTM (JP25)	1 – 2 Connection enabled	JP25 not connected
USB and RS232 HCI connection to BTM on connectors J16 and J13, respectively (JP17)	1 – 2 Connection enabled	JP17 not connected

TX_DBG and JTAG connection to BTM on connectors J14 and J17, respectively (JP18)	1 – 2 Connection enabled	JP18 not connected	
IO select for BT_WAKE signal (JP9)	1 – 2 (IO7) Connection disabled	JP9 not connected	
IO select for HOST_WAKE signal (JP7)	1 – 2 (IO14)	Not connected	
	3 – 4 (IO15)	Not connected	
	5 – 6 (IO17)	Not connected	
Fast clock source Select (JP16)	1 – 2 (26MHz from GIB)	**Connected**	
	2 – 3 (Ext via SMA)	Not connected	
Mono / Stereo CODEC select (JP23)	1 – 2 (Mono)	**Connected**	
Headset Jack configuration select (JP31)	1 – 2 (Mono2)	Not Connected (see Table 7 in section 6.3)	
Left Line IN / Line OUT configuration select (JP29)	1 – 2 (Left Line IN)	**Connected** Note: JP29 and JP30 settings MUST always be the set to the same position.	
Right Line IN / Line OUT configuration select (JP30)	1 – 2 (Right Line IN)	**Connected** Note: JP29 and JP30 settings MUST always be the same	
Antenna select (J2 on BTM)	1 – 2 (Antenna)	**Connected**	
USB/RS232 configuration select for HCI and TX_DBG on GIB	JP19: 1 – 2	Not connected	GIB HCI signals are available on the RS232 connector J13 and TX_DBG signal is available on the RS232 connector J14
	JP20: 1 – 2	Not connected	
	JP22: 1 – 2	Not connected	

Table 24: Default Jumper configurations

The GIB has provision to bypass the level shifters by using the 0R resistor arrays. The bypass resistors are not populated by default and should be populated when a particular level shifter needs to be bypassed. Please refer to the GIB schematics.

7.8. HOST Configuration

The Host connectors provide an interface for communication between the BRF6300 and a customer application board.

7.8.1. Host Power supply configuration

By default, the host interface signals from the BTM are level shifted to Vgib.The customer application board can be operated at its own supply level. If this is different from Vgib, to allow the BTM signals to be level shifted to this voltage level, the host board should supply Vhost_in to the GIB at one of the following.

J11:6 or J12:5 or J20:7

7.8.2. Host connection to BTM

The Host connection to BTM is provided by grouping signals of a particular type on different connectors. Each of these connectors can be individually enabled or disabled as stated in the following table.

Jumper	Function	Position select	Description
JP2	Host IO connection to BTM on connector J3	Close	Disable
		Open	Enable
JP21	Host HCI connection to BTM on connector J12	Close	Disable
		Open	Enable
JP27	Host audio connection to BTM on connector J20	Close	Disable
		Open	Enable
JP24	Host I^2C connection to BTM on connector J20	Close	Disable
		Open	Enable

Table 25: HOST jumper configuration

7.8.3. Host clock supply configuration

See section 7.4 for information about how to supply the Fast clock and the slow clock from the Host interface.

7.9. JTAG Configuration

Before the JTAG interface can be used, it must be enabled. See Table below.

Jumper	Pins	Jumper configuration
JP18	Open (default)	Enable JTAG and TX_DBG connection to BTM
	Close	Disable JTAG and TX_DBG connection to BTM.

Table 26: Enabling JTAG operation

7.10. RF Configuration

The BRF6300 RF output to antenna can either be via an SMA connector or via the onboard antenna – both of which are on the BTM. The “Antenna Select” Jumper (J2 on BTM board) is set connected by default, selecting on-board antenna operation. To select the SMA connector path, the jumper must be removed (see Table below).

Function	Pins	Jumper configuration
Antenna select (J2)	On-board antenna	**Connected**
	SMA connector	**Not connected**

Table 27: RF configuration

Note: RF path on the BTM can be routed to bypass the RF switch to reduce losses to the SMA RF connector. See 4.3 for more information.

8. PC Tools

8.1. Firmware Update

Starter kits with a stacked-RAM BRF6300 BTM allow the user to update the BRF6300 firmware. Updated code can be downloaded to the stacked RAM via the HCI RS232 interface, USB interface or JTAG.

For detailed information on updating FW please see “BT-UM-00xx (RAM Update Utility User Manual, Rev 0.2)”.

8.2. HCI Commander

The HCI Commander is a PC host utility that can be used for quick setup of BT connections and can also be used for testing purposes. The HCI main features are:

- Demonstration of BT RF link activities: ACL links, Voice link, Text Chat.
- Sending HCI commands and receiving HCI events from the BT device.
- Ability to edit scripts of HCI commands using a special language and send it to the target.
- Full Point-to-Multipoint support for all features.
- Monitor data on HCI RS-232 port or USB port.

For more information regarding the HCI Commander, please refer to the “HCI commander user manual”.

9. Measurements

9.1. RF measurements using a Bluetooth™ Tester

A. Remove the Antenna Selection jumper (J2 on BTM board) for working with the SMA connector.
B. Connect the Bluetooth™ tester to the SMA connector using an RF cable
C. Connect the PC to the Starter Kit device using an RS232 cable (included in package) or a USB cable.
D. Run the HCI Commander.
E. If using the COM port, make sure the COM port is properly set up (the default should be 115.2K baud, 8 bit, no parity, HW flow control)
F. Initiate the device using the "Initiate Device" button. This operation initiates the BRF6300 and enables Inquiry scan and Page scan so that it is discoverable
G. Press the "Enter test Mode" button
H. Perform Inquiry from the Tester
I. Page the BRF6300 from the Tester
J. The connection is now established!

Note: When measuring RF performance, see 4.3 for RF board loss information.

9.2. Power Consumption Measurement

The BRF6300 starter kit has provision to measure both the core and IO current of the BRF6300. This is done using jumper **J4**.

Core current

Two types of current consumption measurements can be made for the **BRF6300 core**:

1. Current consumption for **long lasting modes** (like constant Tx or Deep Sleep): This can be done using an ammeter

- Remove the jumper between **J4:3** and **J4:4** (Vbin).
- Measure the current with an ammeter between **J4:3** and **J4:4**

2. Current consumption for **fast changing signals** (like page scan, inquiry scan, etc.): This can be done with an oscilloscope by measuring the voltage drop across a 1-ohm shunt resistor (R28):

- Remove the jumper between **J4:3** and **J4:4** (Vbin)
- Connect a jumper between **J4:5** and **J4:6** (connects a 1 ohm shunt resistor)
- Measure with an differential oscilloscope between **J4:3** and **J4:4**
- 1mV on the scale implies 1mA of current consumption

IO current

To measure the current drawn by the BRF6300 **IO** ring:

- Remove the jumper between **J4:1** and **J4:2** (Vbio)
- Measure the current with the ammeter between **J4:1** and **J4:2**

Note: The SK is not optimized for BRF6300 IO current measurements.

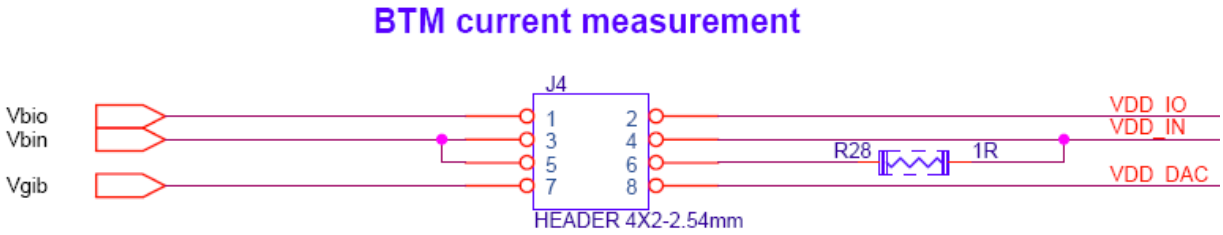


Figure 8: BTM Current Measurement jumpers

Important Notice - Intended use

This product is for demonstration or development purposes only, and has not been qualified for compliance with the Bluetooth™ specifications.

The intended use of the product and applicable accessories are:

Short range Bluetoothä radio development.

Bluetoothä function development.

Bluetoothä interface development.

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