BRF6300 and BRF6150 Differences Application Note

Revision Control

Revision 0.4 → Revision 0.5

- 2.3 Hardware Architecture – update BRF6150 voice buffering capability
- 4.3, 4.4, 4.5 – changed C7 to NC for the BRF6300

Revision 0.31 → Revision 0.4

- 2.5 Added software changes required from host
- 3.1 & 3.2 C2 and B3 pin correction for the BRF6150
- 4.4 & 4.5 BRF6300 designs corrected for C2 and B3 connections

Revision 0.2 → Revision 0.31

- 2.3 Hardware Architecture – update patch trap entries number
- 2.5 Software – WLAN coexistence, correct SG2.0 to 4 wires (was I2C)
- Sections 3 and 4 - Change signal name from CLK_REQ_SEL to CLK_MODE_SEL
- 3.1, 3.2, 4.3, 4.4 and 4.5 – update terminal name and description of F4 from VSSA to VSS_HVM

Revision 0.1 → Revision 0.2

- 2.2 Power Management – correct minimum input voltage from 1.76V to 1.7V.
- 2.3 Hardware Architecture – update Shared antenna with WALN
- 3.1 Terminal changes and 3.2 – update VDD_DAC and PA_CTRL location
- Add chapters 4.4 and 4.5

Abstract

This document describes the main differences, in term of features, system capabilities and implementation between the BRF6300 single chip Bluetooth device and its predecessor, the BRF6150.

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Table of Content

1. Introduction

The BRF6300 has been designed to be pin-compatible with the BRF6150 TI single chip Bluetooth device. Certain pins, however, have been given additional functionality in the BRF6300. This document describes these differences and how they may affect migration from BRF6150 to BRF6300 designs.

2. Features description

The following sections describe detailed comparison between the BRF6300 and the BRF6150, in the following areas: package and size, power management, hardware architecture, RF and software.

2.1 Package and Size

Both devices are available in a 4.5X4.5 mm MicroStar Junior BGA pb-free package (63 terminals) with 0.5mm ball pitch.

Subject	BRF6300	BRF6150	Notes
Technology	90 nm	130 nm	
Package size (mm)	**ROM** – 4.5X4.5X0.8 **Stacked RAM** (BGA package only) – 4.5X4.5X1.3 **WSP** 3.23X3.23X0.5, 0.4mm pitch Availability is TBD.	**ROM** – 4.5X4.5X0.8 **Stacked Flash** - 4.5X4.5X1.3	
Number of external components	6 + balun/filter (optional matching network)	7 + balun/filter (optional matching network)	Reduced number of power management terminals. All external capacitors are of one type with common value and small package
Total solution area	45 mm2 (MicroStar BGA) 35 mm2 (WSP)	< 50 mm2	
Number of terminals	63 (MicroStar BGA) 48 (WSP)	63	
Package type	Microstar BGA ZSL Lead-Free WSP	Microstar BGA ZSL Lead-Free	Complies with the latest environmental requirements
Memory for firmware upgrade	Stacked RAM Pin to pin compatible to the ROM device, same layout	Stacked Flash Pin to pin compatible to the ROM device, same layout	Early integration of new firmware releases in form factor product. Reduced risk and improved development schedule

2.2 Power Management

Subject	BRF6300	BRF6150	Notes
Architecture			Low voltage and high voltage regions – certain regions such as the BB can operate at lower voltages than the DRP and therefore consume less power. The scheme alone saves approximately 2mA. The quiescent current while in deep sleep (low power consumption) mode is reduced by using a lower power supply level to the core.
On chip LDOs	Yes Extended voltage range 1.7 – 5.4	Yes	Enables use of one power source, increased noise immunity. LDO improvement in the 6300: soft start and short circuit protection One reference design for all power supply configurations in the 6300: battery or external regulator
Direct connection to battery	Yes	Yes	Eliminate the need for external regulator, the 6300 has one reference design for all power supply configurations
Power On Reset	Internal Power On Reset	Internal Power On Reset	No need for hard reset, reset is performed internally after power up; no need for external reset circuit
Shut Down mode	Yes	Yes	A mode of complete shut down – power is still connected, but the device is disabled and consumes only 5 uA; easy disabling of Bluetooth. This input can be used to reset the BRF6300.
VDD_IO range	1.425 – 1.98V	1.65 – 3.6V	

2.3 Hardware Architecture

Subject	BRF6300	BRF6150	Notes
Voice channels	2	2	
Voice interface	Enhanced flexible voice interface and data format – McBSP	Flexible voice interface and data format – McBSP	Full flexibility of data bits order, sampling and positioning for variety codecs support High data rate with voice
Voice interface – maximum clock range	Master – 4.096 MHZ Slave – 16 MHz	Master – 3.072 MHZ Slave – 15 MHz	
Voice buffering noise (Synchronizes the PCM clock to the BT clock in case the BT is slave and the codec is master)	Yes	No The clocks are synchronized only in master - master mode.	Avoids losing samples due to clock mismatch between the remote BT device and the PCM host.
Lost voice packets handling	Yes	Limited	Improved algorithm for handling packets loss: duplicate the last sample or configurable sample size
UDI support	Yes	Yes	Support also clock synchronization
Host controller interface Four wire UART (H4) Three wire UART (H5) SDIO Automatic transport detection	 4 Mbps Yes Up to 25MHz clock rate, 1 bit, slave, V1.0 specification, 1.8V Yes	 3 Mbps Yes No Yes	Additional interfaces
Clock sharing	Yes	Yes, not including shut down mode	Improved clock sharing, supported during shut down mode and active low/high configurable
Digital trimming of the fast clock initial offset	±150 ppm	±50 ppm	Digital initial compensation of up to ±150 ppm of the fast clock source (including the ±20 ppm drift defined in the spec), allows the use of a low cost oscillator or crystal.
Number of general purpose IO pins	11	9	In addition to these 11 GPIOs, any unused signal can be used as a GPIO (Audio, UART, etc)
Class 1	Yes	Yes	Improved class 1 interface – dedicated analog power control signal and per handle per packet control for dynamic switching. API will ease the adaptation of the firmware to different types of PA
Shared antenna with WLAN	Yes	Yes	The effect of the RF_SHUTDOWN signal is slightly different between the BRF6300 and the BRF6150

Patch trap entries	24	12	Expanded software update facility
Terminals pull resistor	Single pull polarity is supported - either pull up or pull down	Possible to select to each GPIO either pull up or pull down	

2.4 RF

Subject	BRF6300	BRF6150	Notes
Digital RF architecture	Improved Digital RF architecture	Yes	Improved RF performance
Receiver (Sensitivity, blocking, co-channel)	1. Receiver chain performance was optimized to have 5dB better sensitivity threshold (reduced Noise Figure and Improved ADC-Dynamic Range). 2. A new RX Demodulator included to support EDR modulation 3. LNA input bandwidth has been narrowed to increase blocking performance 4. All clock domain was optimized to reduce leakages and to increase blocking performance 5. IFA pole location has been optimized for co-channel performance		
Transmitter	1. New Digital-TX block was added to support EDR modulation with a “Polar-Modulation” architecture, which gives best spectral- purify with low current consumption EDR. 2. The higher bit rate required by EDR increases the power consumption of the transmitter. The DRP therefore uses the full Digital TX EDR transmissions and has a lower-power, pass-through mode of operation for GFSK transmissions. This is accomplished by a unique method of giving the transmitter advance indication of EDR packets in order to allow the necessary ramp-up period.		
EDR (2,3 Mbps)	Yes	No	
Typical sensitivity	-90	-85	
Temperature sensing algorithm	Improved algorithm	Basic algorithm	“On chip” high resolution temperature sensor ensures performance stability over temperature

2.5 Software

Subject	BRF6300	BRF6150	Notes
Bluetooth spec 1.1 and 1.2	Yes	Yes	
Bluetooth 2.0 + EDR and 2005 Core release	Yes	No	Full support of 2.0 + EDR Future support for Bluetooth 2005 core release (only software upgrade when Bluetooth specification will be available)
Multiple IAC's	Yes	No	Identification capability of up to three IAC Simultaneously for faster and power saving inquiries
Channel classification	Yes	Yes	Faster classification, less "wasted" bandwidth
Low power scan	Yes	No	Reduce power consumption by 3 during Page and Inquiry scan
SNR measurements for a better channel quality assessment	Yes	No	Enhance the AFH algorithm Packet size to use per channel (the noisier the channel, the smaller the packet)
Low power mode mechanism	HCILL and H5	HCILL and H5	
WLAN coexistence	Soft Gemini 1.0, 1.1, and 2.0.	Soft Gemini 1.0 and 1.1	Enhanced WLAN co-existence algorithm (SG2.0 with 4 wires). Utilizes both AFH and Soft Gemini (time domain) coexistence, for best Bluetooth/WLAN interoperability in cellular phones

From a host point of view, very few changes are required when moving from BRF6150 to BRf6300:

- Same data transfer and sleep protocols
- No change required in the HOST to activate EDR in the BRF6300 firmware level
- New init file is needed to handle changes in the vendor specific commands e.g. new codec configuration parameters
- Improved buffer size to support the EDR rates. Old configuration is supported for BT 1.2 (GFSK)
- Improve HCI commands flow control for better robustness

3. BRF6150 to BRF6300 board design migration

In order to allow easy migration of platforms using the BRF6150 device to the BRF6300 device, the BRF6300 ROM version is pin compatible to the BRF6150 ROM version. However, the compatibility is limited to different board assembly and configuration.

This section describes the required board changes when replacing the BRF6150 with the BRF6300 and the limitations on this migration.

3.1 Terminal changes between the BRF6150 and BRF6300

The following table describes all the terminals that have a different functionality between the BRF6150 and BRF6300.

Ball	BRF6300	BRF6150	Comment
A1	IO16	BGAP_I	BGAP_I functionality is multiplexed with BGAP_V, additional GPIO was added.
A6,C4	IO4, IO5 have pull down during shut down	IO4, IO5 have pull up during shut down	These IOs are used for the WLAN interface and required pull down during shut down (also improve the current leakage)
C2	VDD_DAC	VDD_IN_ANA	The previous VDD_IN supply voltage is now used as the input voltage for the internal DAC (should be connected to 3.3V max), the output of the DAC controls the external class1 analog PA. For Class 2 devices it can be grounded (preferably) or connected to 3V or less.
B7	IO2	IO2/SCL	The SCL functionality moved to IO17
B3	PA_CTRL	VDD_IO_SF	This pin must be left N.C. - as would be the case if BRF6150 ROM device was used. Otherwise output to external PA control.
C6	IO1	IO1//EXT_CLK_REQ_IN	EXT_CLK_REQ_IN moved to IO15
D6	CLK_MODE_SEL	JTAG_SEL	Added function for clock request scheme. Should be high for internal clock sharing scheme and low for wired OR/no clock sharing scheme (see the BRF6300 product preview for details).
F7	IO15/EXT_CLK_REQ_IN	IO15	EXT_CLK_REQ_IN moved to IO15
G4	IO17/SCL	TL_LDO_OUT	Re-arrangement of internal LDOs, additional GPIO was added
G6	PMTST	KA_OUT	Re-arrangement of internal LDOs, reserved for power management tests (for TI internal use)
H5	F_LDO_OUT	BB_LDO_OUT	Re-arrangement of internal LDOs
H6	NC	VBAT	In the BRF6300, these two terminals are shortened internally. This enables a direct replacement with the BRF6150 VBAT designs.
G5	NC	VLDO_OUT	
H8	NC	VDD_IO_SF	

F4	VSS_HVM	VSSA	VSS_HVM terminal need to be connected directly to the internal ground plane and not to terminals F3, G1 and G2 as in the BRF6150.

These changes in the terminal functions introduce the following limitations:

- I2C is not compatible; this feature can be supported only with layout changes.
- Analog class 1 external PA is not compatible; this feature can be supported only with layout changes.
- BRF6300 enhanced clock sharing options are not compatible; this feature can be supported only with layout changes.

Additional limitation:

- The BRF6300 VDD_IO support 1.8V only (BRF6150 is up to 3.6V)
- External crystal connection - changed from Colpitts to Pierce, Not “reference design compatible” due to change of circuitry architecture; this does not affect external fast clock configuration.

3.2 Required design changes

The following table describes in details all the required changes when replacing the BRF6150 with the BRF6300.

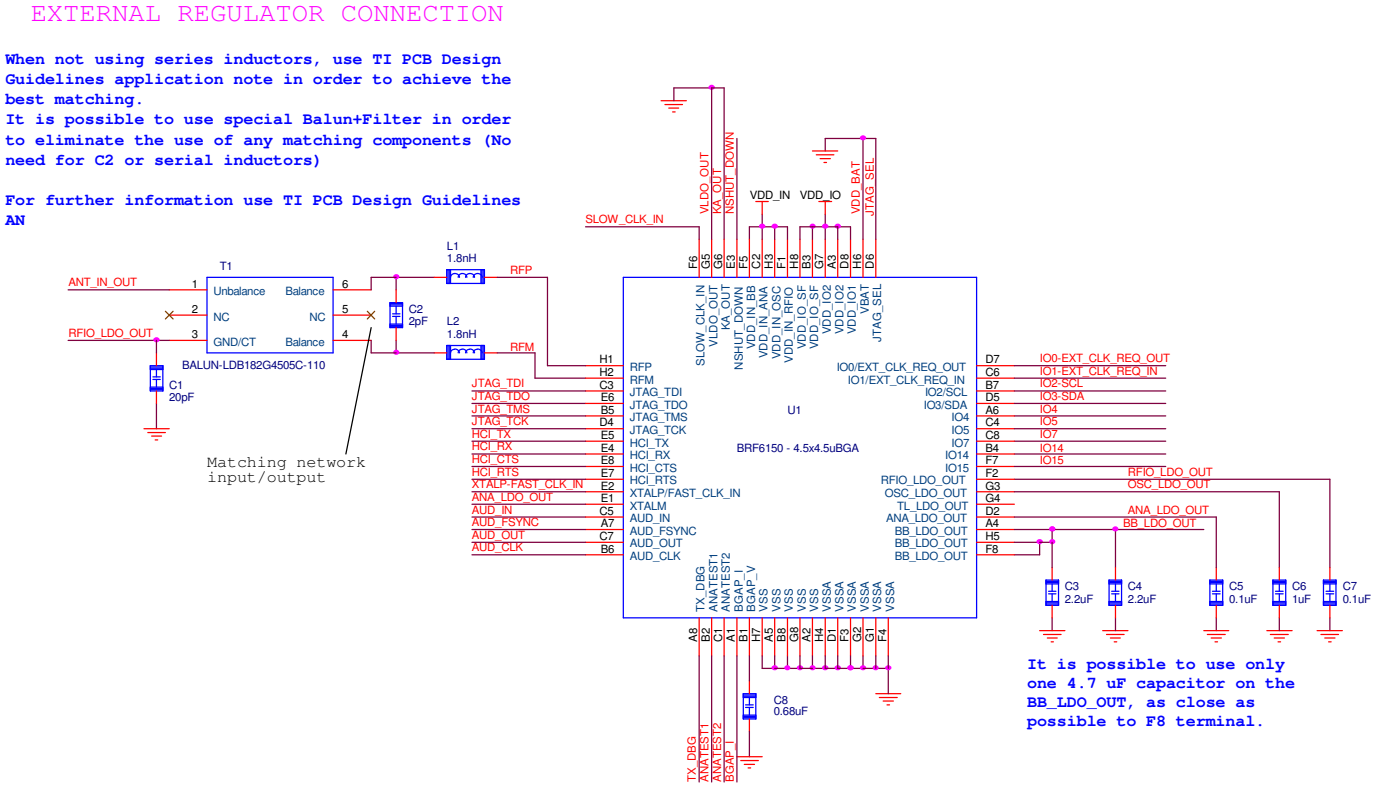
Ball	BRF6300	BRF6150	Required Changes for BRF6300 assembly (on board)	Remarks
Baseband				
B7	IO2	IO2/SCL	Connect SCL to IO17 instead to IO2 (if using I2C), GSM Synchronization signal can be on IO2 (only for 6300 assembly)	Required only if I2C feature is used, otherwise no change is required
C6	IO1	IO1/EXT_CLK_REQ_IN	Connect the external clock request to IO15 instead of IO1	Required only if EXT_CLK_REQ_IN feature is used, otherwise no change is required
F7	IO15/EXT_CLK_REQ_IN	IO15	Connect external clock request to IO15 if used	Required only if EXT_CLK_REQ_IN feature is used, otherwise no change is required
D6	CLK_MODE _SEL	JTAG_SEL	JTAG_SEL default value for the BRF6150 is low. For the BRF6300, this terminal is used to select the clock sharing scheme	If using the internal clock sharing feature, this terminal should be high, otherwise low.
E6	JTAG_TDO(+)	JTAG_TDO	During power up, this terminal is set to input. External pull up required only if JTAG debugging is	Indicates that ARM JTAG is selected (replaces the JTAG_SEL

			needed.	functionality)
DRP				
G6	PMTST	KA_OUT	Test pin for power management. Can be connected to BB_LDO_OUT or GND if not used (as it is for the BRF 6150).	No change is required
G4	IO17/SCL	TL_LDO_OUT	If I2C is used, must be connected to SCL. Otherwise can be left not connected as for the BRF6150	Required only if I2C feature is used or there is a need to use IO17, otherwise no change is required
H5	FLDO_OUT	BB_LDO_OUT	For the BRF6150, all three BB_LDO_OUT are connected externally. For the BRF6300 this terminal shouldn't be connected to the other two BB_LDO_OUT terminals and it has its own capacitor	For the BRF6300, leaving this terminal connected to BB_LDO_OUT results in extra 2 mA in the current consumption (in this case one capacitor is required)
H8	Not Used	VDD_IO_SF		Can be left connected to 3V, as in the BRF6150
C2	VDD_DAC	VDD_IN_ANA	VDD_DAC supports 1.65 - 3.6V	For external analog PA No assembly or layout change is required
B3	PA_CTRL	VDD_IO_SF	DAC output, used for class 1analog PA, wakes up in High-Z	No assembly or layout change is required if not using class 1 analog PA
D2	ANA_OUT	ANA_OUT	The short to XTALM (as on the BRF6150) is supported but not recommended. Results in small (TBD uA) additional current.	
A1	IO16	BGAP_I	BGAP_I is for testing purpose only and can be not connected in BRF6150 designs.	No change is needed in case there is no need for IO16
B1	BGAP_V/I	BGAP_V	Remove the capacitor used for the BRF6150	

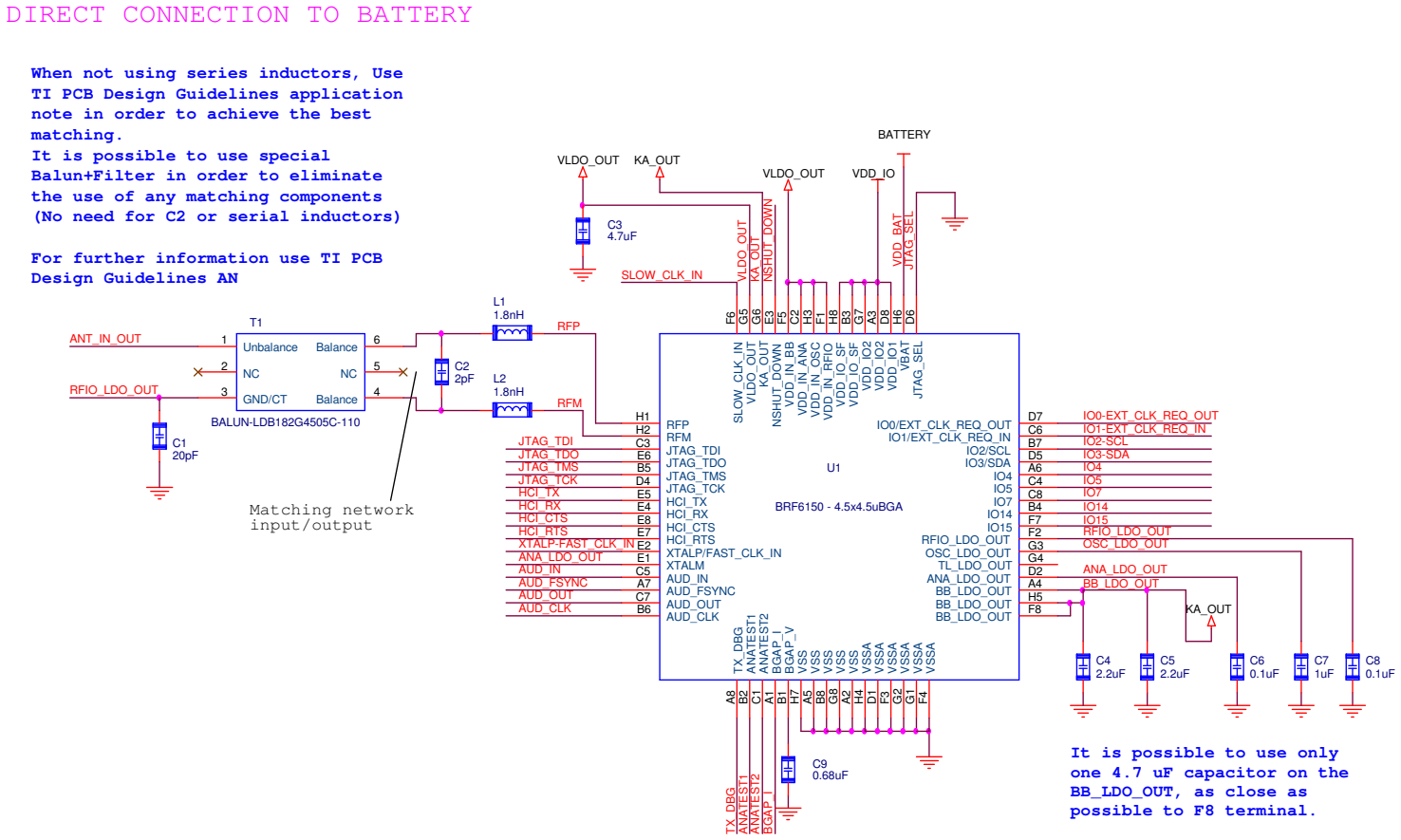
H1, H2	RFP, RFM	RFP, RFM	The BRF6300 matching network consists of a serial 0.8nH, achieved by the board traces, and 1.8pF capacitor in parallel.	The BRF6150 matching network consists of two serial inductors (1.8nH) and a parallel capacitor (2 pF). If using the board traces inductance, 2.2 nH is required with a 2.7 pF capacitor.
F4	VSS_HVM	VSSA		In the BRF6150 this terminal was connected to other VSSA terminals (G1, G2 and F3), which were connected to the internal ground plane. In the BRF6300 this terminal shouldn't be connected to the VSSA terminals but rather directly to the internal ground plane.

4. Reference design

4.1 BRF6150 external regulator connection



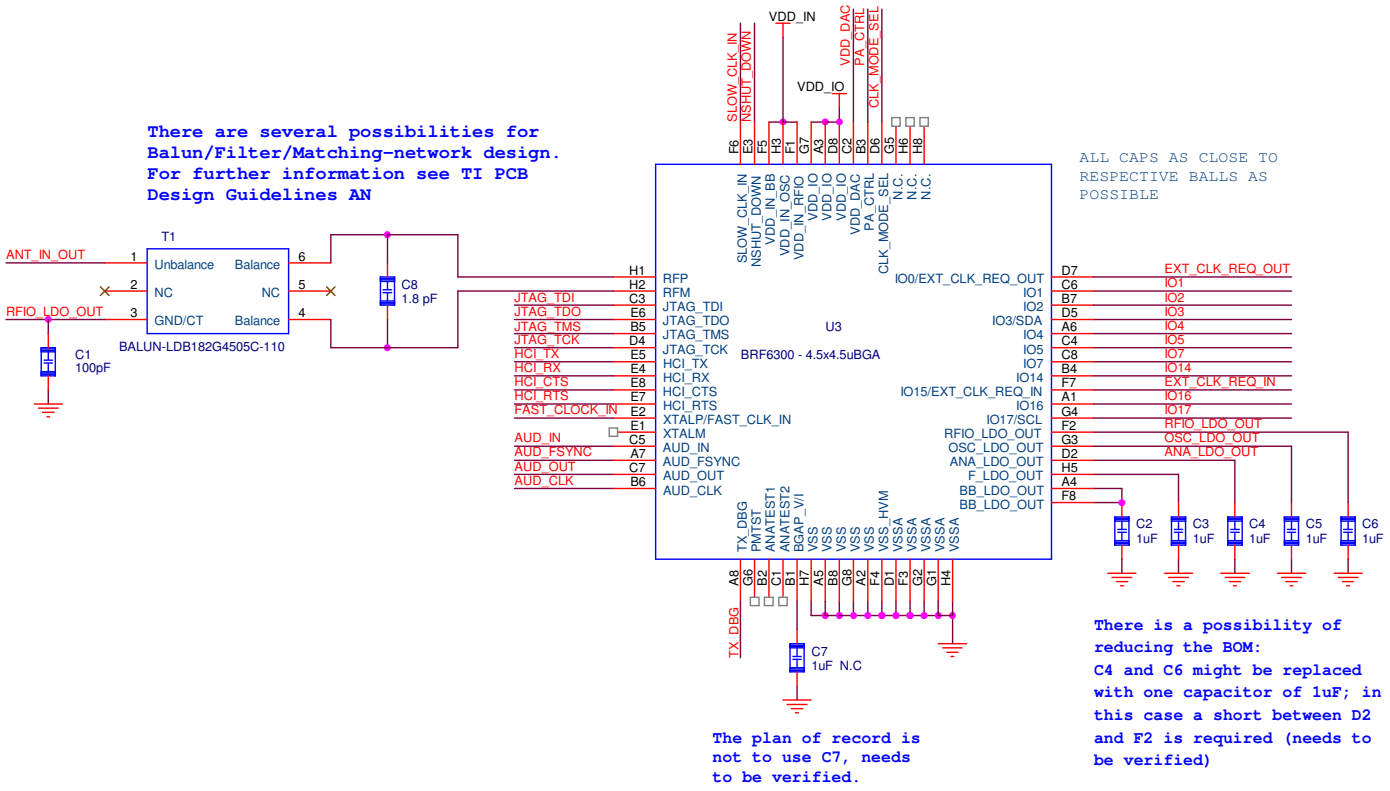
4.2 BRF6150 direct battery connection



4.3 BRF6300

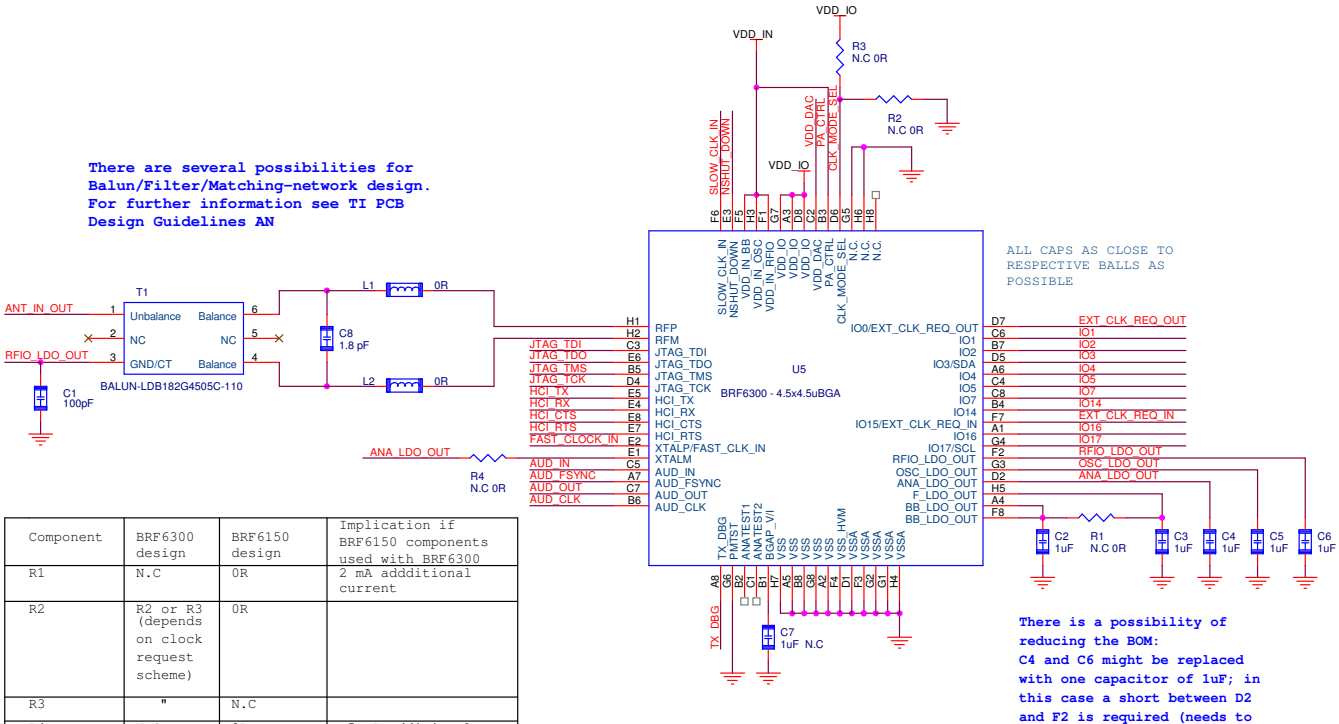
As described earlier, the BRF6300 supports a single reference design for both external regulator and direct battery connection.

Please note that this schematic is still preliminary.



4.4 BRF6150 with External Regulator to BRF6300 migration

The following schematic describes the provisions required for a design based on the BRF6150 connected to an external regulator and planned to be replaced with the BRF6300.

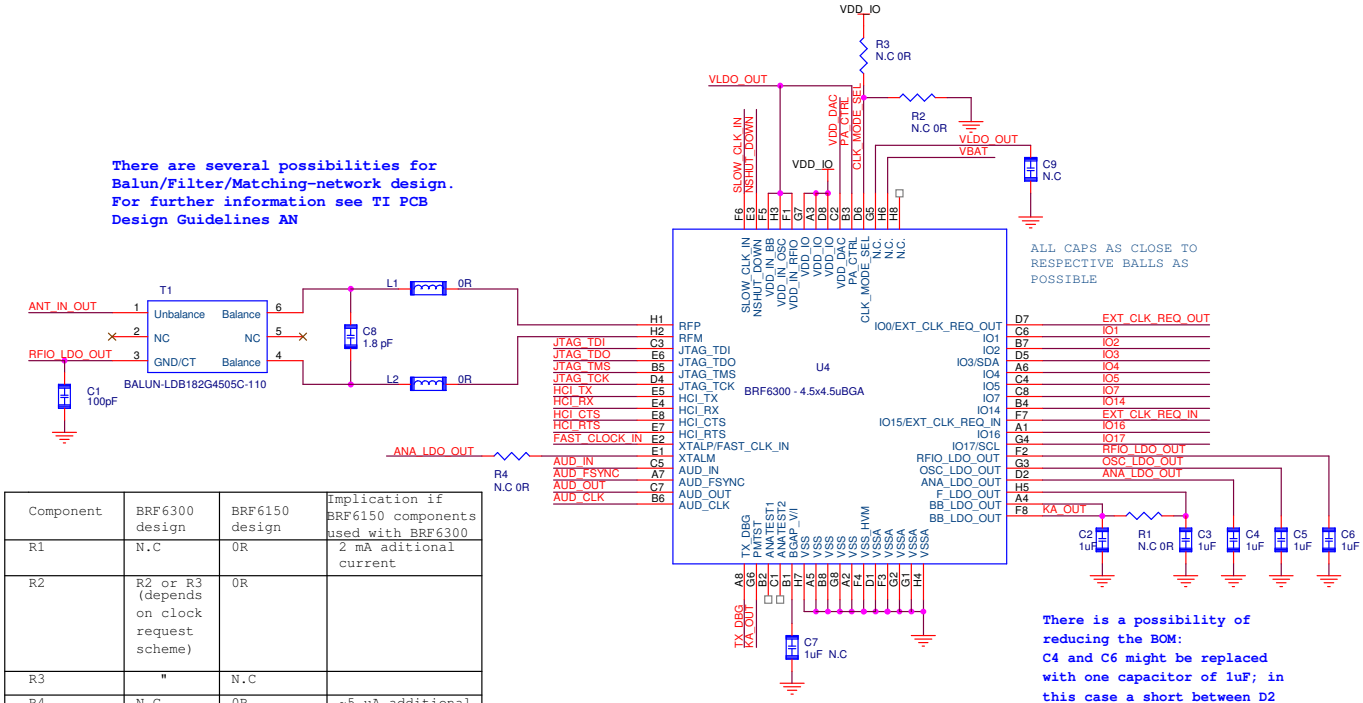


Component	BRF6300 design	BRF6150 design	Implication if BRF6150 components used with BRF6300
R1	N.C	0R	2 mA addditional current
R2	R2 or R3 (depends on clock request scheme)	0R	
R3	"	N.C	
R4	N.C	0R	~5 uA additional current
C2, C3	1 uF	2.2 uF 0603	
C4, C6	1 uF	0.1 uF	
C7	N.C	0.68 uF	
L1, L2	0R 0201	1.8 nH	Incorrect RF matching

Notes:
1. In the BRF6300, ball G6 (PMTST) is in high-Z and can be left connected to GND, as in the BRF6150 design
2. In the BRF6300, balls G5 and H6 are shortened internally, and can be left connected to GND, as in the BRF6150 design

4.5 BRF6150 with VBAT to BRF6300 migration

The following schematic describes the provisions required for a design based on the BRF6150 connected to VBAT and planned to be replaced with the BRF6300.



Component	BRF6300 design	BRF6150 design	Implication if BRF6150 components used with BRF6300
R1	N.C	0R	2 mA aditional current
R2	R2 or R3 (depends on clock request scheme)	0R	
R3	"	N.C	
R4	N.C	0R	~5 uA additional current
C2, C3	1 uF	2.2 uF 0603	
C4, C6	1 uF	0.1 uF	
C7	N.C	0.68 uF	
C9	N.C	4.7uF	
L1, L2	0R 0201	1.8 nH	Incorrect RF matching

Notes:
1. In the BRF6300, ball G6 (PMTST) is in high-Z and can be left connected to BB_LDO_OUT, as in the BRF6150 design
2. In the BRF6300, balls G5 and H6 are shortened internally, so VBAT can be applied to H6 as in the BRF6150 design

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