Application Report
SWRA132–February 2007

BRF63xx Voice and Audio Configuration

Bluetooth Applications Group

ABSTRACT

This document discusses the capabilities of the BRF63xx voice and FM audio systems. It describes the different audio formats supported by the BRF63xx and how to interface with them using the pulse-code modulation (PCM) bus. It also reviews voice over HCI (VoHCI) protocol and some issues regarding extended Synchronous Connection Oriented Channels (eSCO) links.

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1 Audio Codec (PCM) Interface

1.1 Overview

The codec interface is a fully-dedicated, programmable serial port that provides the logic necessary to interface with several kinds of PCM or I²S™ codecs. The interface supports the following features:

- Two voice channels
- Master/slave modes
- µLaw, A-Law, Linear and Transparent coding schemes
- Variable length frames and frame-sync duty cycles
- Variable data size, position and bit order
- PCM bus sharing
- High-rate PCM interface for Enhanced Data Rate (EDR)
- Various voice formats (standard PCM, I²S, Unrestricted Digital Information [UDI] profile) and a wide variety of codecs

1.2 PCM Hardware Interface

The PCM interface is a 4-wire interface, as illustrated in Figure 1.

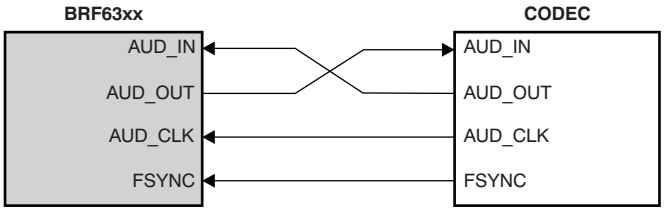

Figure 1. PCM Interface (BRF63xx As Slave)

It contains the following lines:

- **AUD_IN**: Input
- **AUD_OUT**: Output
- **AUD_CLK**: Configurable direction (input or output)
- **FSYNC**: Configurable direction (input or output)

The Bluetooth® (BT) device can be either the master of the interface where it generates the clock and the frame-sync signals, or the slave, where it receives these two signals; in other words, clock and frame-sync can act as inputs or outputs.

The HCI_VS_Write_Codec_Configuration_Island3 command configures the PCM interface. (For all vendor-specific information, see SWRU115, *BRF6350 Vendor-Specific Commands*).

After reset or power up, the PCM interface is set as the slave by default, with all pulldowns (PDs) active.

1.2.1 AUD_CLK

Slave mode supports clock input frequencies of up to 16MHz. At clock rates above 12MHz, the maximum data burst size is 32 bits.

In master mode, the BRF63xx can generate any clock frequency between 64kHz–4,096kHz, with 1ppm accuracy. Clocks are generated from the fast clock and are synchronous to it.

EDR support affects the maximum PCM clock rate. The maximum data rate will be achieved when using 3-EV5 packets. The maximum rate of one asymmetric 3-EV5 channel is 1.154MHz (equal to one 3-EV5 packet every three frames). The maximum rate of two asymmetric 3-EV5 channels is 1.382MHz (equal to two 3-EV5 packets every five frames). Therefore, in order to support two channels, the clock rate must be at least 1.382MHz.

1.2.2 AUD_OUT

The Data Out line is configured as *Hi-Z* output between data words. Data Out can also be set for permanent Hi-Z, regardless of data output. This configuration allows the BRF63xx to act as a bus slave in a multi-device PCM bus.

1.2.3 FSYNC

For both master and slave modes, the interface supports these specifications:

- FSYNC periods from 1 to 65535 times the Audio Clock period, in one-clock increments
- FSYNC duty cycles of 1 to 65535 times the Audio Clock period, in one-clock increments. A value of 0x0000 sets the mode to 50% duty cycle (for example, as required by the I^2S interface protocol).

1.2.4 Clock-Edge Operation

The codec interface of the BRF63xx can work on either the rising or the falling edge of the clock. It also has the ability to sample the frame-sync and the data at inverse polarity.

Figure 2 shows the operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame-sync signal is updated by the codec on the falling clock edge, and therefore is sampled by the BRF63xx on the next rising clock. Data from the codec are driven from the falling edge and therefore sampled by the BRF63xx on the clock falling edge.

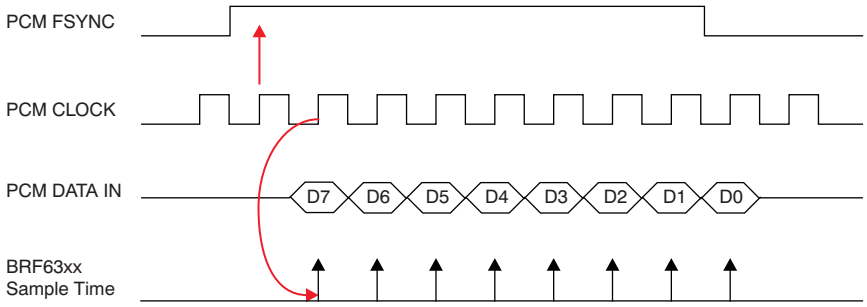

Figure 2. Negative Clock Edge PCM Operation

1.2.5 Data Bits Configuration

1.2.5.1 Size

Data length can be set from 8 bits to 640 bits per channel. Up to two channels are possible; data length can be set independently for each channel.

Data in and data out do not necessarily have to be the same size.

1.2.5.2 Order

Some codecs have a reversed bit-order (that is, LSB first). The BRF63xx codec interface supports both MSB first and LSB first bit orders.

The bit order of data in and data out can be configured independently; additionally, the order for each channel is separately configurable.

1.2.5.3 Position/Offset

Some codecs are configured so that the input and output data do not have the same timing—for example, the PCM3008, a TI stereo audio codec.

In general, data position within a frame is configurable within one clock (bit) resolution and can be set independently for each channel, relative to the beginning edge of the frame-sync signal.

1.2.5.4 HCI Vendor-Specific Commands

The following vendor-specific commands are used to configure the codec interface:

- HCI_VS_write_codec_config_Island3
- HCI_VS_write_codec_config_enhanced_Island3

See SWRU115, *BRF6350 Vendor-Specific Commands*, for additional information.

1.3 Two-Channel PCM Bus Example

In Figure 3, a two-channel PCM bus is shown where each channel has a different word size and arbitrary position in the bus frame.

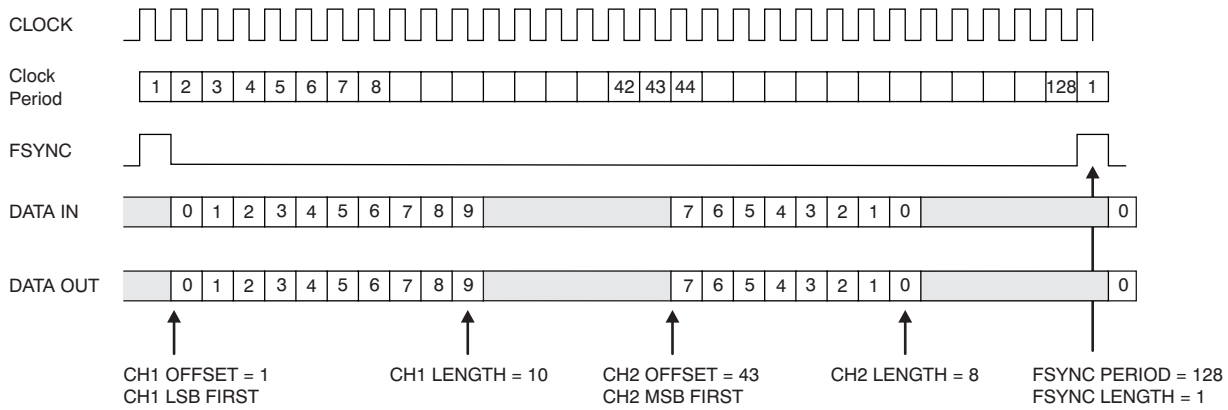

Figure 3. Two-Channel PCM Bus Timing

The structure for each vendor-specific command is shown below.

HCI_VS_Write_Codec_Configuration_Island3 setup:

PCM clock rate	0x0800	(2.048MHz)
PCM clock direction	0x01	(BRF63xx is slave)
Frame-sync frequency	0x03E80	(16kHz)
Frame-sync duty cycle	0x0001	(High for 1 period of PCM clock)
Frame-sync edge	0x00	(Rising edge)
Frame-sync polarity	0x00	(Active high)
Reserved	0x00	
CH1 data out size	0x000A	(10-bits)
CH1 data out offset	0x0001	(One clock from rising edge of fsync)
CH1 data out edge	0xFF	(Data out driven at clock rising edge)
CH1 data in size	0x000A	(10-bits)
CH1 data in offset	0x0001	(One clock from rising edge of fsync)

CH1 data in edge	0xFF	(Data out driven at clock rising edge)
Reserved	0x00	
CH2 data out size	0x0008	(8-bits)
CH2 data out offset	0x002C	(44 clocks from rising edge of fsync)
CH2 data out edge	0xFF	(Data out driven at clock rising edge)
CH2 data in size	0x0008	(8-bits)
CH2 data in offset	0x002C	(44 clocks from rising edge of fsync)
CH2 data in edge	0xFF	(Data out driven at clock rising edge)
Reserved	0x00	

HCI_VS_Write_Codec_Configuration_Enhanced_Island3 setup:

PCM clock shutdown	0x00	(Disabled)
PCM clock start	0x0000	(N/A)
PCM clock stop	0x0000	(N/A)
Reserved	0x00	
CH1 data in order	0x01	(LSB first)
CH1 data out order	0x01	(LSB first)
CH1 data out mode	0x02	(Hi-Z when idle)
CH1 data out duplication	0x00	(Retransmit last sample for missing data)
CH1 tx_dup_valve	0x00000000	(N/A)
CH1 data quant	0x00	(Use bit mode if < 24 bits)
Reserved	0x00	
CH2 data in order	0x00	(MSB first)
CH2 data out order	0x00	(MSB first)
CH2 data out mode	0x02	(Hi-Z when idle)
CH2 data out duplication	0x00	(Retransmit last sample for missing data)
CH2 tx_dup_valve	0x00000000	(N/A)
CH2 data quant	0x00	(Use bit mode if < 24 bits)
Reserved	0x00	

1.4 Frame Idle Period

The codec interface has the capability for frame idle periods, where the PCM clock can go inactive and become '0' at the end of the PCM frame (after all data have been transferred). This feature is configured by HCI_VS_Write_Codec_Config_Enhanced_Island3 (described above). The BRF63xx supports frame idle periods both as master and slave of the PCM bus. When BRF63xx is the master of the interface, the frame idle period is configurable.

There are two configurable parameters:

- **Clk_Idle_Start**: Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock will become ‘0’.
- **Clk_Idle_End**: Indicates the time from the beginning of the frame until the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period. For example:

For PCM clock rate = 1MHz and frame-sync period = 10kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90

Between each two frame-sync periods, there will be 70 clock cycles (instead of 100). The clock idle period will start 60 clock cycles after the beginning of the frame and will last (90 – 60) = 30 clock cycles.

This means that the idle period will end (100 – 90) = 10 clock cycles before the end of the frame. The data transmission must end before the beginning of the idle period, as shown in Figure 4.

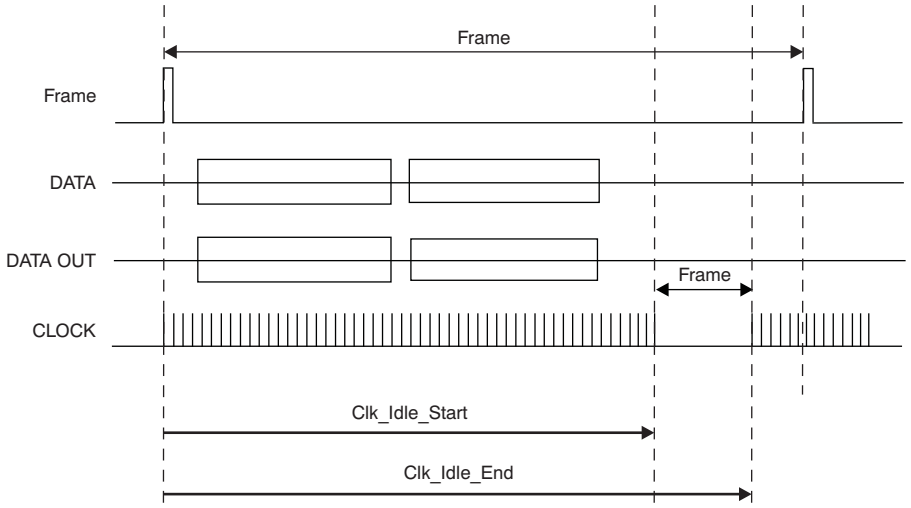

Figure 4. Frame Idle Period

1.4.1 Behavior with No Input Clock

As an enhancement to the BRF6150 plattform, and in addition to the features discussed, the BRF63xx (as a slave) features a flexible recovery mechanism when the clock stops unexpectedly during a SCO/eSCO link. The voice channel experiences very little impact when this process executes.

1.5 PCM Bus Sharing

The BRF63xx supports multiple device configuration, when there are several devices on the PCM bus simultaneously; see Figure 5.

The pin AUD_OUT can be configured to a high impedance state when it is not in use (that is, between data words). Combining this mode and setting the PCM interface to Slave mode (both AUD_CLK and AUD_FSYNC are inputs) allows sharing the same codec for both BTand other applications. When the BRF63xx is not used, the codec interface is configured as described earlier, and other devices can be active on the PCM bus.

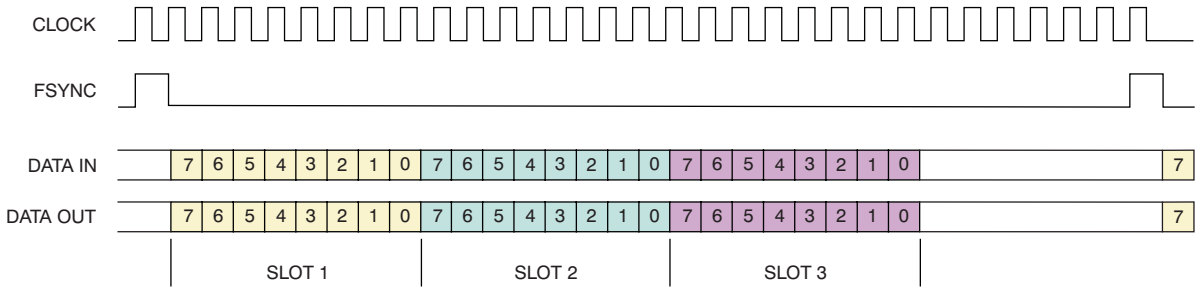

Figure 5. PCM Bus Sharing

1.6 RF Link/PCM Clock Mismatch Handling

The BRF63xx receives audio data from an external codec (or similar device) on the PCM interface and transmits the data over BT 2.4GHz radio frequency (RF) channels. In the same way, the BRF63xx receives audio data via BT 2.4GHz RF channels and transmits the data to an external codec via the PCM interface. These input and output data rates are not usually the same, and therefore audio data overflow or underflow can occur.

1.6.1 Overflow

The BRF63xx receives RF voice packets and writes the data to the codec interface. If the BRF63xx receives data faster than the codec I/F output allows, an overflow occurs. In this case, the BRF63xx has two possible behaviors: *allow overflow* and *do not allow overflow*.

A similar situation occurs when the BRF63xx receives data packets via the codec interface faster than the BT RF link is able to transmit:

- If overflow is allowed, the BRF63xx continues receiving data, and will overwrite any data not yet sent to the codec.
- If overflow is not allowed, any RF voice packets received when the buffer is full are discarded

1.6.2 Underflow

Underflow exists if output to the codec interface occurs at a higher rate than the BRF63xx receives new data; that is, the PCM output buffer will be empty. In this case, the configured duplication data will be output to the PCM bus.

Underflow can also occur if the codec interface input rate is lower than the BT RF transmission rate. In this case as well, the configured duplication data will be output to the PCM bus.

1.6.3 Bluetooth Clock and PCM Clock Synchronization

Even when the BT and PCM data are well-matched (thereby avoiding overflow and underflow problems), a potential problem still exists: data loss as a result of long-term clock drift between the BT clock and the PCM clock is possible. This synchronization issue exists in any voice connection that uses the codec interface. However, it is most critical for UDI support.

The BRF63xx addresses this problem in this manner: When the BRF63xx is the PCM bus master, it automatically synchronizes the PCM clock to the BT clock.

Note: The Bluetooth clock is the BT timing clock provided by the Bluetooth piconet master; it should not be confused with the BRF63xx F_{REF} input.

There are four possible master-slave combinations. The BRF63xx ensures clock synchronization only when it is the PCM master. When it is the PCM slave and the BT is the master, the PCM clock cannot be relied on to meet BT accuracy specifications or to be continuous. When the BRF63xx is the BT slave and the PCM slave, it has no control over either clock. Table 1 summarizes these options.

Table 1. BT and PCM Clock Synchronization

BT Clock	PCM Clock	Result
Master	Master	Synchronized
Master	Slave	Not synchronized
Slave	Master	Synchronized
Slave	Slave	Not synchronized

1.7 PCM Loopback

The PCM loopback feature allows the user to perform loopback on the PCM bus. Loopback occurs through buffers only and is done to test the connectivity on the printed circuit board (PCB). All codec interface parameters set by the HCI_VS_Write_Codec_Configuration_Island3 command must be set prior to starting the PCM loopback process.

The PCM loopback is enabled using HCI_VS_Set_PCM_Loopback_Enable. However, the loopback delay period must first be configured using the following HCI_VS command:

HCI_VS_Set_PCM_Loopback_Configuration_Island3

1.8 Improved Algorithm for Lost Packets

The BRF63xx features an enhanced algorithm for improving voice quality when received voice data packets go missing. The algorithm uses two options:

- Repeat the last sample; this option is possible only for sample sizes up to 24 bits. For sample sizes greater than 24 bits, the last byte is repeated.
- Repeat a configurable sample of 8 bits–24 bits (depending on the actual sample size), in order to simulate silence (or anything else) in the PCM bus. The configured sample will then be written in a specific register for each channel.

The choice between these two options is separately configurable for each channel using the HCI_VS_Write_Codec_Configuration_Enhanced_Island3 command.

This feature is further improved upon by using the following new HCI_VS command:

HCI_VS_enable_EPLC

2 Voice Formats

The voice setting parameter as specified in the BT protocol controls the various settings for voice connections. The voice setting parameter controls the following configuration for voice connections:

- Input coding
- Air coding format
- Input data format
- Input sample size
- Linear PCM parameter

The formats used on the PCM interface and the RF air coding do not necessarily need to be the same.

The settings apply to all voice connections and cannot be set for individual voice connections.

The standard HCI_Write_Voice_Setting command is used to write the values for the voice setting configuration parameter; see the complete description in the Bluetooth specification version 1.2, sections 6.12, 7. 3.29 and 7.3.30.

The BRF63xx codec interface can use one of four audio coding patterns:

- Law (8-bit)
- µLaw (8-bit)
- Linear (8-bit or 16-bit)
- Transparent

Table 2 summarizes the voice setting parameters.

Table 2. Voice Setting Parameters

Value	Description
00XXXXXXX	Input coding: Linear
01XXXXXXX	Input coding: µlaw Input Coding
10XXXXXXX	Input coding: A-law Input Coding
11XXXXXXX	Reserved for future use
XX00XXXXX	Input data format: 1s complement
XX01XXXXX	Input data format: 2s complement
XX10XXXXX	Input data format: Sign-Magnitude
XX11XXXXX	Reserved for future use
XXXX0XXXX	Input sample size: 8-bit (only for Linear PCM)
XXXX1XXXX	Input sample size: 16-bit (only for Linear PCM)
XXXXXnnnXX	Linear_PCM_Bit_Pos: number of bit positions that the MSB of the sample is away from starting at MSB (only for Linear PCM)
XXXXXXXX00	Air coding format: CVSD
XXXXXXXX01	Air coding format: µlaw
XXXXXXXX10	Air coding format: A-law
XXXXXXXX11	Reserved

2.1 Using SCO/eSCO Links in the BRF63xx

2.1.1 Basic eSCO negotiation

Generally, eSCO packet types are negotiated by the host BT profiles. However, if all packets are enabled in the HCI_Setup_Synchronous_Connection command and there are no other link constraints, the default selections for the BRF63xx are the following:

- All packet types available: 2-EV3, Desco = 0, Tesco = 12, Wesco = 2, payload = 60 bytes
- All packet types, except EDR: EV4, Desco = 0, Tesco = 10, Wesco = 0, payload = 50 bytes

In both cases, throughput = 64Kbps.

2.1.2 Scatternet with SCO/eSCO

The BRF63xx can handle two simultaneous SCO (or eSCO) channels on the same or different piconets, with a packet type of HV3, EVx, 2-EVx, or 3-EVx. If two eSCO channels are used, they must have the same bandwidth configuration.

During the voice channel establishment, the greatest possible interval between the voice packets is used before accepting or changing the voice packet type.

Switching between the two networks is done automatically when needed. Various hooks are given to the firmware in order to avoid collisions between the two channels. This process occurs by changing the (e)SCO parameters on the fly, according to the network drifting rate, offset, etc., resulting in optimal QoS and link management.

For example, the BRF63xx will automatically change (e)SCO slot positions if it sees potential problems between two piconets arising from clock drift.

2.1.3 Combined SCO/eSCO and ACL Links

The voice link is typically given highest priority, except for the following scenario (as Figure 6 illustrates):

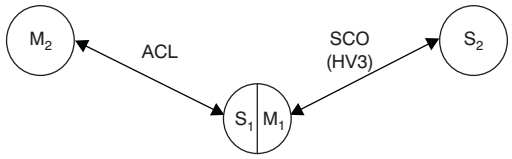

Figure 6. Combined SCO/eSCO and ACL Condition

A master (M_1) has a voice connection with a slave (S_2) with interval of three frames (HV3 packets). A second master (M_2) connects to the first master (M_1, now S_1) and establishes an ACL link. M_2 will acknowledge the ACL data from S_1 in a different frame than the one in which it received the ACL data. If S_1 (M_1) will not listen to M_2 in that frame, S_1 will not acknowledge the packet to M_2 in the next transmission.

In order to avoid an endless loop of *no acknowledges* from S_1 to M_2, S_1 must listen in consecutive frames to receive the *acknowledge* from M_2. Since there are no two consecutive frames between the SCO frames in this case, $S_1(M_1)$ must overrun on the SCO frames to S_2. The scheduler priority of $S_1(M_1)$ for the S_1–M_2 link will remain higher than the M_1–S_2 voice for one more frame, in order to receive the *acknowledge* from M_2.

For quick transactions, such as sending a business card between phones, the effect on voice quality is negligible. The host may manage this distortion by putting the device in Sniff mode and experience voice interference in the Sniff intervals only. It is important to remember that the priorities can change on the fly. however, and are fully flexible in order to enable the firmware to achieve the best link management possible.

Because of these issues, it is recommended to use eSCO rather than SCO links whenever possible for a Scatternet scenario. Because of the ability of eSCO to allow greater spacing between packets and its retransmission capability, it generally does not have the limitations seen with SCO links.

2.1.4 Support for Hands-Free Profile 1.5 (HFP1.5)

The BRF63xx provides full support for HFP1.5, as specified in the protocol.

HFP1.5 requires support for EV3 + 1 retransmission as a minimum for devices that do not support EDR packets (for example, 2-EV3). This condition is normally not allowed for a scatternet slave because there are insufficient slots to accommodate ACL links for the scatternet as well as EV3 + 1 retransmission.

The BRF63xx makes special provision for this possibility by *stealing* slots from the eSCO link in order to allow the ACL links to coexist.

The HFP1.5 profile can act both as master or slave. As a result of power consumption optimization, it is preferred that the handset act as slave when connected to a headset and as master when connected to a car kit. This preference allows the headset to set up the lowest power ACL link, and the car kit (where power is plentiful) to be controlled by the headset.

2.1.5 Support for A2DP profile

The Advanced Audio Distribution Profile (A2DP) is frequently used to connect to high-quality headphones. Therefore, the term *advanced audio* should be distinguished from *Bluetooth audio*, which indicates distribution of narrowband voice on SCO channels. A typical use case is the streaming of music content from a stereo music player to headphones or speakers.

A2DP streams are ensured asynchronous links with demand for high bandwidth and low latency. A2DP devices are agnostic to device role (master/slave). However, it is preferred that the source device be the master because this role controls the data stream; both configurations are supported nonetheless. It is assumed that the receiving device has a buffer of at least 100ms (required by AVRCP profile), and therefore the stream can handle up to 100ms peak latency.

An HCI link with 500Kbps and 3ms latency is sufficient for the High-Quality mode 1 (see Table 3); that is, the role of the BRF63xx is to receive/send A2DP data from/to a BT A2DP source over an ACL link, and then stream this data to the host that supports the required throughput and latency.

Table 3. A2DP Asynchronous Link

Parameters Set	Low-Quality Mode	High-Quality Mode 1	High-Quality Mode 2
Incoming Traffic	Control packets	Control packets	Control packets
Outgoing Traffic	Ensured service: 333 bytes every 13.3ms 48kHz, bitpool 28, subband 8, block size 16, mono, Five SBC frames per packet	Ensured service: 667 bytes every 16ms 48kHz, bitpool 48, subband 8, block size 16, joint stereo, Six SBC frames per packet	Ensured service: 181 bytes every 5.3ms 48kHz, bitpool 38, subband 8, block size 16, joint stereo, Two SBC frames per packet

2.2 Voice Over HCI (VoHCI)

In addition to the codec interface, the BRF63xx also supports transfer of voice channels over the HCI interface. In this case (unlike the PCM interface), the application is running a synchronous link through the HCI and all control is performed by the BRF63xx firmware. In other words, the data rate matches between the host and the air, buffer management and the total latency.

The main features of this interface are:

- Supports all SCO/eSCO packet types and all data rates
- All air modes supported: Transparent, CVSD, µLaw, A-Law
- Flow control support in both directions
- Supports two channels combinations—both codec and VoHCI simultaneously; that is, each channel can be configured separately to either codec or HCI
- Local loopback is available

However, this constraint exists:

- When using H5 transport layer, VoHCI is not supported.

2.2.1 Creating a Synchronous Link Over HCI

HCI_VS_Write_SCO_Configuration

The command HCI_VS_Write_SCO_Configuration allows the host to configure the following parameters of the voice channels:

- Audio type—Codec interface/Host interface (HCI)
- HCI TX buffer size—allows the host to determine the BRF63xx transmission buffer length
- Max latency—determines the maximum amount of data (in bytes) allowed in the TX buffer before it is flushed. This limit directly affects the latency of the channel. This parameter is applicable only if flow control is disabled. If flow control is enabled, then the host must regulate the data flow to keep the latency within limits.
- Accept packet with bad CRC—determines whether or not to accept packets received with a bad CRC. In eSCO with retransmission, it will not disable retransmission; such a packet will be accepted only after all retransmissions have failed.

SCO Connection Parameters and Flow Control

Return values:

- Status
- HCI TX buffer size
- Number of TX buffers

The TX buffer minimum size is 30 bytes; there must be at least two buffers. The number of buffers is simply the number of buffers that will fit into the maximum latency permitted.

Notice that if the max latency value is not a multiple of the buffer size, then it will be truncated accordingly. Therefore, to prevent uncertainty, the host is encouraged to use a max latency value that is a multiple of the buffer size.

2.2.2 Flow Control

The BRF63xx implements bi-drectional flow control. The host must handle the flow control separately for each channel because there are separate RX and TX buffers for each channel.

Host → Controller

Unlike ACL data, flow control in this direction is not mandated by the BT specification. However, it is highly recommended for ensured synchronization.

- **HCI_Write_SCO_ Flow_Control_Enable**: Used to enable or disable flow control of SCO/eSCO data
- **HCI_Read_Buffer_Size**: If flow control is enabled, the host must issue this command before it sends any data to the controller
- In case a packet is totally or partly flushed, a data buffer overflow event is sent to the host
- The host must manage flow control independently for each channel. Therefore, the SCO connection handle needs to be considered. (See the Bluetooth specification for more details.)

Controller → Host

- **HCI_Host_Buffer_Size**: The host uses this command to notify the controller of its SCO buffer pool
- **HCI_Set_Host_Controller_To_Host_Flow_Control**: The host uses this command to enable or disable flow control in this direction. (See the Bluetooth specification for more details.)

The host has control over the buffer size that the device uses, and whether the synchronous connection exists with the host or with the codec.

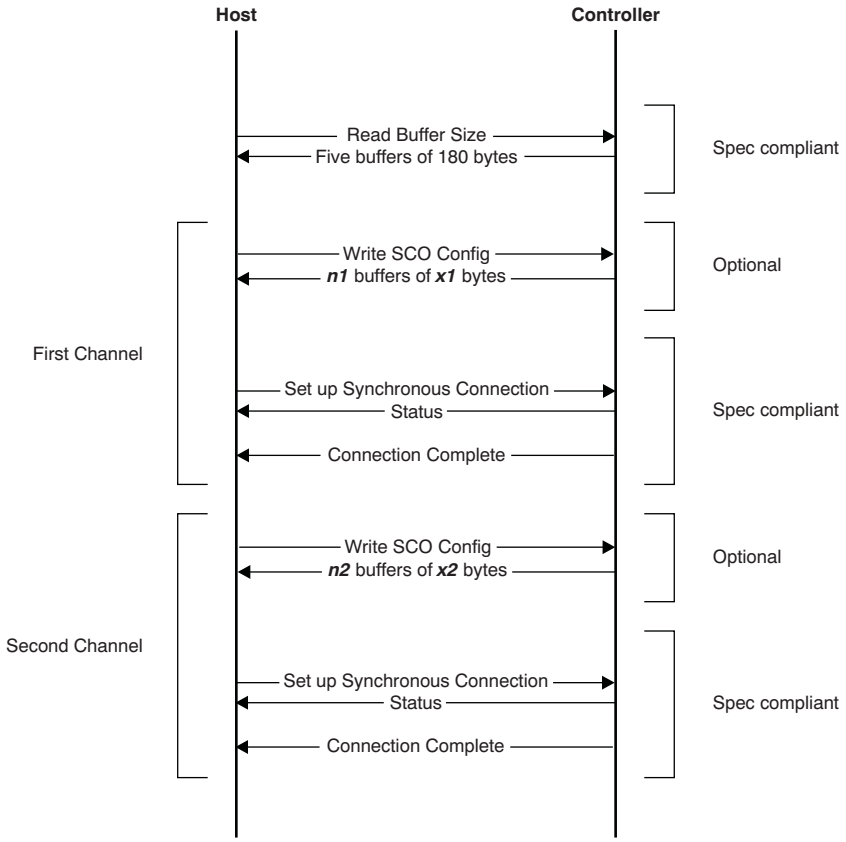

Figure 7. Synchronous Connection Creation Process

2.2.3 Special Considerations for VoHCI

2.2.3.1 Performance

There are several factors to consider when evaluating the performance of VoHCI.

- Latency: Latency is the period between sending a packet from one side until it is received by the other side. It includes the UART delay, processing delay, air delay and buffer delay. It does not include the time that the host waits for flow control before sending the packet.
- Flow control effect on the bandwidth: the ability to reach full bandwidth between the host and the device
- Performance in high data rate condition
- Idle time
- Concurrent ACL and voice data

A rough estimation for the latency is the number of baseband (BB) packets in the SCO buffer multiplied by the T_{eSCO} value. Therefore, in general, the larger the SCO buffer, the greater the latency.

2.3 FM Over BT

FM I^2S audio can be directed to the BT module. The BT module sees this data as an alternative PCM interface and can assign a eSCO channel to this data. For example, consider FM audio sent to a remote headset that supports only 64Kbps (mono) voice stream. This use case assumes an HFP headset that enables the FM transfer similar to system tones or gaming tones transferred to the headset.

See command HCIPP_FM_SET_AUDIO_PATH in the document SWRU115, *BRF6350 Vendor-Specific Commands*, for additional information.

Note that if this command is specified, the BT external PCM bus is not available (that is, all pins are in a Hi-Z state).

3 Application Examples

Special features of the BRF63xx, such as clock synchronization and optimum packet size determination, enable the device to support two other codec interfaces that can be used for both voice and music transmission.

- Inter-IC Sound (I^2S)
- UDI

These interfaces have different timing and data format requirements from the standard PCM codec interface described earlier in this document.

3.1 Inter-IC Sound (I^2S)

The BRF63xx can be configured as an Inter-IC Sound (I^2S) serial interface to an I^2S codec device. I^2S is a serial bus designed for digital audio devices and technologies such as compact disc (CD) players, digital sound processors, and digital TV (DTV) sound.

The I^2S bus consists of three serial bus lines: a line with two time-division multiplexing data channels (SD), a word-select line (WS), and a continuous serial clock line (SCK). The BRF63xx implements this interface using its standard PCM lines, with FSYNC = WS, DATA_IN/OUT = SD and CLOCK = SCK. The BRF63xx can act as an I^2S master (providing WS and SCK), or as an I^2S slave (receiving WS and SCK), as shown in Figure 8.

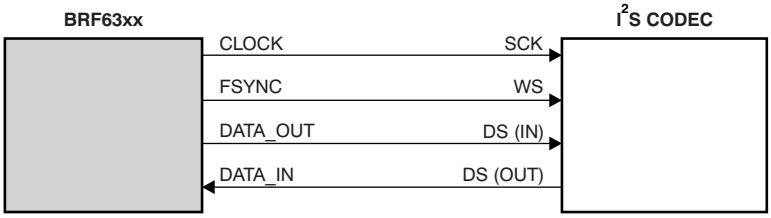

Figure 8. BRF63xx as I^2S Master

The I^2S link is implemented as a time-division multiplexed (TDM) slot-based serial interface, which is used to transfer audio data and command/status information to or from the codec device. In this mode, the BRF63xx audio codec interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 (WS low) is used for the left channel audio data, and time slot 1 (WS high) is used for the right channel audio data.

The I^2S interface handles the audio data separately from the clock signals. By separating the data and clock signals, time-related errors that cause jitter do not occur, thereby eliminating the need for anti-jitter devices.

Because the transmitter and receiver have the same clock signal for data transmission, the transmitter (as the master) must generate the bit clock, word-select signal and data. In complex systems, however, there may be several transmitters and receivers, making it difficult to define the master. In such systems, there is usually a system master controlling digital audio data-flow between the various ICs. Transmitters must generate data under the control of an external clock, and thus act as slaves. Figure 9 illustrates the I^2S signal format.

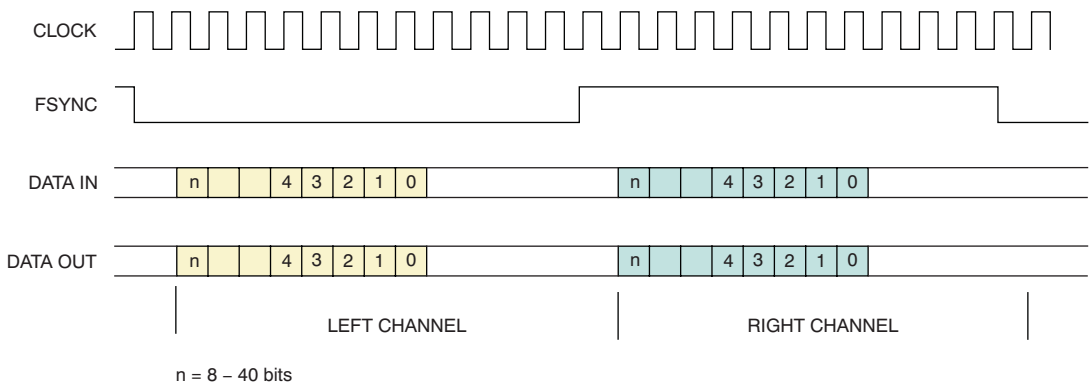

Figure 9. I²S Signal Format

In order to configure the correct timing, FSYNC should have a duty cycle of 50%. Use the HVI_VS_Write_Codec_Configuration_Island3 command.

Example 1. HCI_VS_Write_Codec_Configuration_Island2 Setting for I²S Interface

PCM clock rate: 0xC00 (3072kHz)
PCM clock direction: 0x0 (BRF63xx is the master)
Frame-sync frequency: 0x01 (8kHz)
Frame-sync duty cycle: 0x05 (50% duty cycle)
Frame-sync direction: 0x0 (BRF63xx is the master)
CH#1 data size: 0x10 (16-bit)
CH#1 data offset: 0x00 (PCM clock cycle between the rising of frame-sync and the first data bit)
CH#1 padding start: 0xFF (no padding)
CH#1 padding value: 0x0

Example 2. HCI_VS_Write_I2C_Register Setting

Slave ID: 0x1a (codec 2)
PVT clock: 0 (prescale clock divider factor)
Working frequency: 0x0190 (400kHz)
Sub address: 0x1e (an internal register address)
Data length: 0x01 (1 byte)
Data: '00' (one byte of data that is 00)

3.2 UDI

The Unrestricted Digital Information (UDI) profile defines the protocols and procedures that are used by devices implementing UDI for the 3G mobile phone systems; for example, devices with a Bluetooth connection to a 3G handset, communicating via videophone over a 3G network. Up to two channels of UDI data can be supported. The data are transferred via the codec interface using transparent mode and are sent out using eSCO EV4 Bluetooth packets (EV5 is also selectable).

3.2.1 UDI Over Bluetooth Characteristics

The 3G UDI characteristics are:

- UDI frame size = 10ms
- Clock rate = 3.84MHz (typically)
- UDI packet size = 86 bytes
- Data rate = 64Kbps or 384Kbps

Each 3G UDI packet consists of 80 data bytes and six header bytes. Only the UDI data (80 bytes) is transferred via the PCM bus. The host receives the 3G UDI packets, including header and data, and then sends the data only to the BRF63xx device via PCM. In other words, the BRF63xx receives the data only and transmits the data only, over the air.

UDI data can be transferred via PCM using any bus configuration that will supply a data rate of 64Kbps.

UDI RF data is transferred using eSCO EV4 packets every 12 BT frames, equivalent to 120 bytes every 15ms, or 64Kbps. There may be up to two UDI channels, as Figure 10 illustrates.

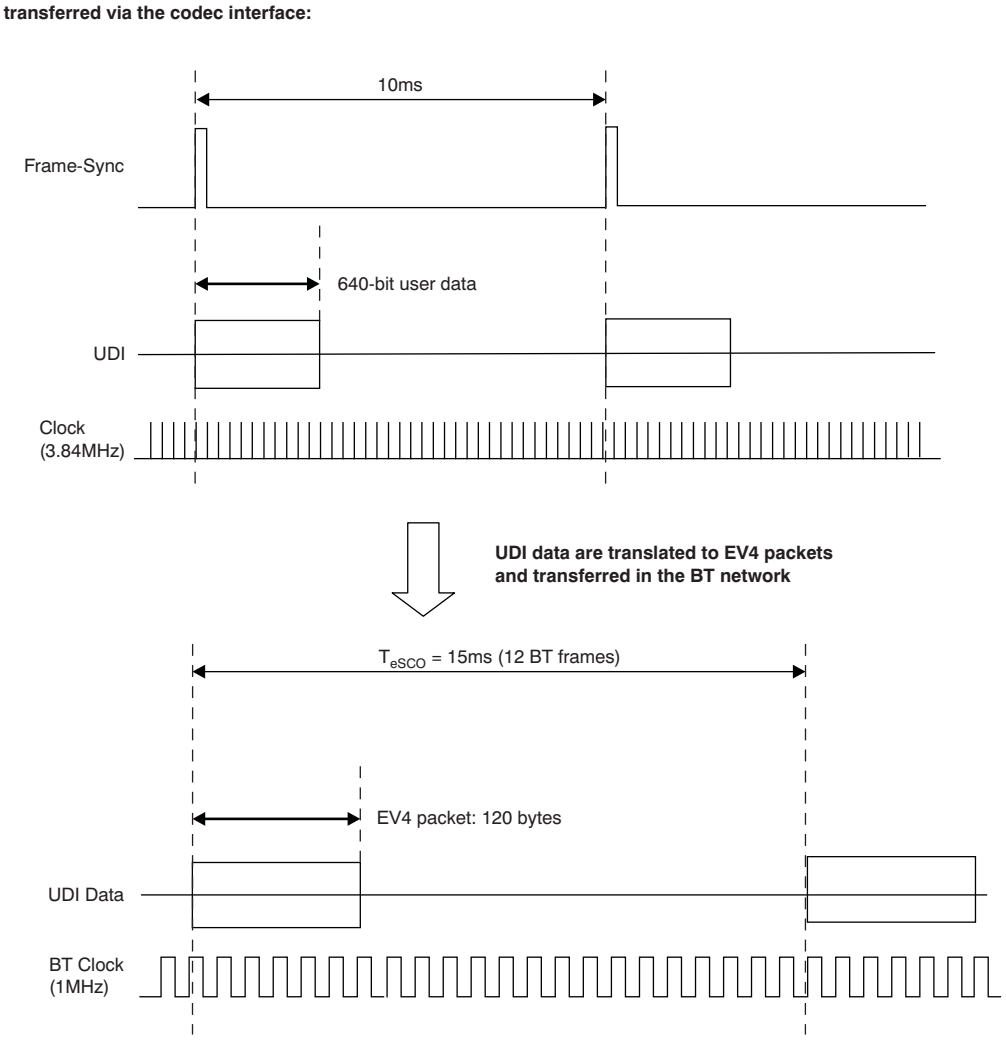

Figure 10. Transferring UDI Data

3.2.2 UDI Support Requirements

To support the UDI profile, the BRF63xx has the following abilities.

Note: According to the UDI spec, the frequency accuracy of the PCM clock must be under 100ppm and the latency in the BT part should be under 50ms. The BRF63xx supports these requirements

3.3 Stereo and MP3 Support

3.3.1 Stereo

If the SCO/eSCO BT channel is supplied from one PCM channel, then the only option is mono transmission (or dual mono, if you have two speakers) supplied by the mono codec.

If the SCO/eSCO BT channels are supplied from two PCM channels, then the I^2S configuration (described in Section 3.1) can be used to provide stereo music over one voice link.

The BT 1.2 maximum rate is EV5 (transmitting 180 bytes over three slots + one slot receiving). For example, (180 × 8) / (3 × 625µs + 625µs) = 576Kbps.

The maximum stereo rate (assuming 16 bits per sample) would therefore be: 576Kbps / 16 bits / 2 channels = 18k sample/s (18ksps).

With 3-EV5 EDR packets, this rate can be tripled to 54ksps.

These values are the maximum theoretical configuration that occupies the entire bandwidth. In reality, we must leave open slots for Scan, AFH classification, Signaling packets (LMPs), and so forth. A mroe realistic calculation, then, is to leave one free frame for every eSCO packet (two frames):

(180 × 8) / (3 × 625µs + 625µs + 1250µs) = 384Kbps

Note that the PCM interface has a Linear/CVSD digital filtering mechanism that limits the PCM to an audio frequency response bandwidth of 3.4kHz. To obtain the high samples per second data rate required by stereo music, transparent air mode must be used instead of the commonly-used CVSD. (See the Bluetooth specification for more information about the HCI_Setup_Synchronous connection.)

3.3.2 MP3

MP3 music can be transmitted as *encoded* (compressed) or *decoded* (uncompressed):

Transmitting decoded MP3 data simply requires a very high rate eSCO channel.

Transmitting encoded MP3 data requires a high data rate ACL channel and an MP3 decoder on the receiving side.

MP3 has two sample rate groups:

- 11.025ksps, 22.05ksps, or 44.1 ksps
- 12ksps, 24ksps, or 48ksps

In general, the channel rate can be calculated with the following formula:

Sample rate × number of bits/sample = channel rate

For example, 24ksps × 16 bits = 384Kbps.

Two channels of 48ksps with 32 bits/sample is equivalent to a channel rate of 1536Kbps of decoded MP3 data, or 12Kbps of encoded MP3 data.

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