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BRF6300 BGA Package Information

January 2, 2007
BT-AN-0046, Revision 0.3

Abstract

This document describes the MicroStar Junior BGA™ package used for BRF6300 Bluetooth single chip.
The areas covered are PCB design constraints, reliability issues, MicroStar Junior package testing and design, lead free information and specific 4.5x4.5 and daisy chain packages.

Revision Control

Revision 0.3

- Add ROHS data on section 6

Revision 0.1 → 0.2

- Add Cupper plug substrate change in section 2

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1. Overview

This document outlines the package information of the MicroStar BGA[tm] package used in Texas Instruments BRF6300 chip.

This information includes the package parameters that are of importance in the manufacturing process like PCB design guidelines, reflow profile and lead free information.

Daisy chain devices that match the BRF6300 packages are intended to give customers the ability to perform reliability test during the ramp up and mass production phases.

2. Introduction

The parallel pursuit of cost reduction and miniaturization in recent years has given rise to an increasing emphasis on very small integrated circuit (IC) package solutions.

This is particularly evident in consumer-based end equipment using digital signal processor (DSP) solutions such as wireless telephones, laptop computers, and hard-disk drives. Despite the formal definition, packages with an area similar in size to the IC they encapsulate are loosely referred to as chip scale packages (CSPs).

Chip scale packages are in many ways an ideal solution to the cost reduction and miniaturization requirements.

Texas Instruments produces a polyamide film-based family of CSPs called MicroStar BGA. Like most other CSPs, MicroStar BGAs use solder alloy balls as the interconnect between the package substrate and the board on which the package is soldered. The MicroStar BGA family comes in a range of solder ball pitch (0.5 mm, 0.8 mm, and 1.0 mm).

The MicroStar Junior BGA package has been fully qualified in numerous applications and is being used extensively in mobile phones, laptops, modems, handheld devices, and office environment equipment.

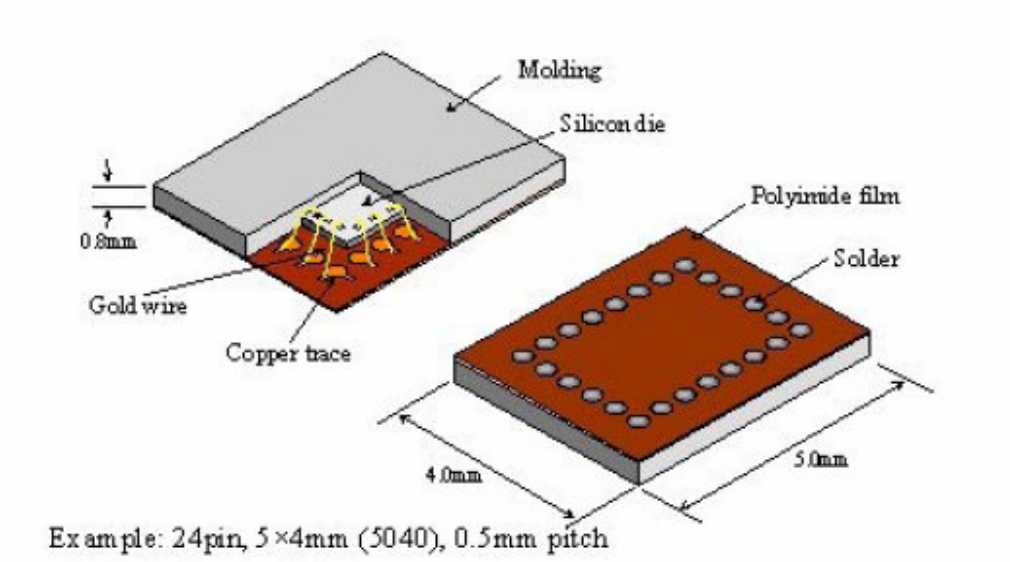


Figure 1: Exemple of TI's MicroStar Junior BGA structure

Daisy-chained units are used to gain experience in the testing, to check PCB electrical layouts, and to confirm the accuracy of the mounting equipment.
To facilitate this, Texas Instruments offers daisy-chained units in all production MicroStar BGA packages.

Reliability is one of the first questions designers ask about any new packaging technology. They want to know how well the package will survive handling and assembly operation, and how long it will last on the board.
The elements of package reliability and system reliability, while related, focus on different material properties and characteristics and are tested by different methods.

On December 6 2005, Texas Instruments Inc, Wireless Terminal Business Unit (WTBU) announced the qualification of a Copper plug substrate for 0.5mm pitch u*junior BGA devices. The Copper plug substrate will be Thin Ni plated.

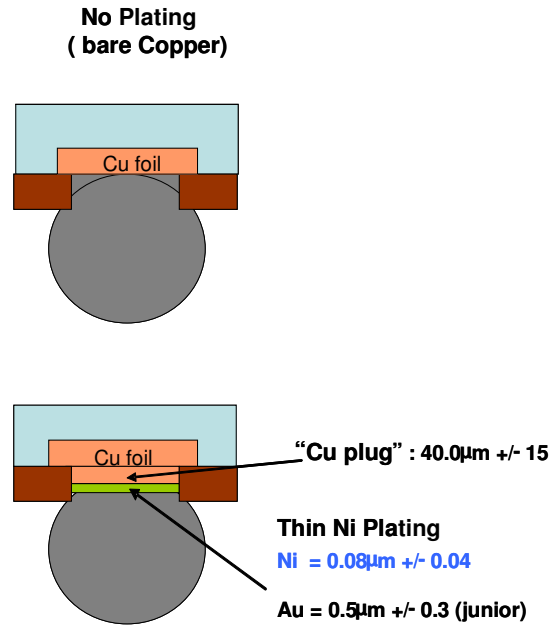


Figure 2: Cupper plug substrate change

The reason of the change is to reduce potential package out-gassing at via level during customer surface mount process. There is no affect on Fit, Form, Function and Reliability and no change in the products identification.

3. PCB Design Constraints

3.1 Solder Land Areas

Design of both the MicroStar BGA itself and the printed circuit board (PCB) are important in achieving good manufacturability and optimum reliability. In particular, the diameters of the package vias and the board lands are critical. While the actual sizes of these dimensions are important, their ratio is more critical. Figure 3 illustrates the package via-to-PCB configuration and Figure 4 illustrates why this ratio is critical.

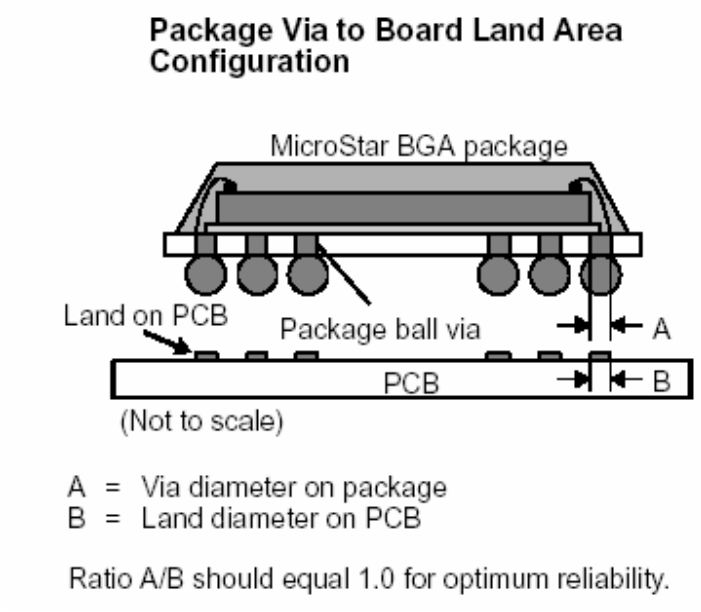


Figure 3: Package Via to Board Land Area Configuration

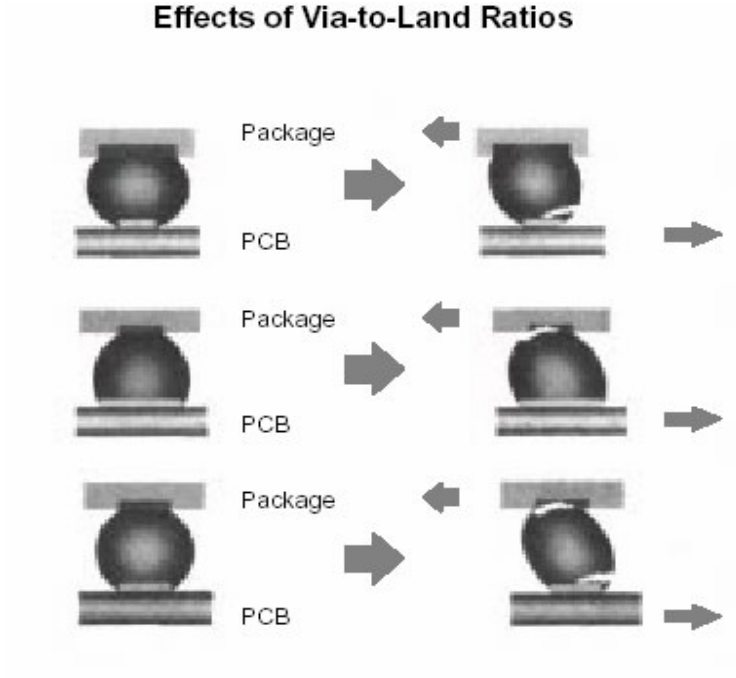


Figure 4: Effects of Via-to-Land Ratios

In the top view of Figure 4, the package via is larger than the PCB via, and the solder ball is prone to crack prematurely at the PCB interface. In the middle view, the PCB via is larger than the package via, which leads to cracks at the package surface. In the bottom view, where the ratio is almost 1:1, the stresses are equalized and neither site is more susceptible to cracking than the other.

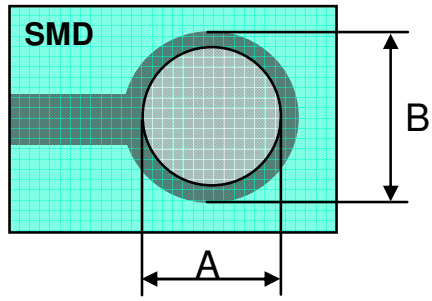
Solder lands on the PCB are generally simple round pads. Solder lands are either solder-mask-defined or non-solder-mask-defined.

Solder-mask-defined (SMD) land. With this method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Better size control is the result of photoimaging the stencils for masks. The chief disadvantage of this method is that the larger copper spot can make routing more difficult.

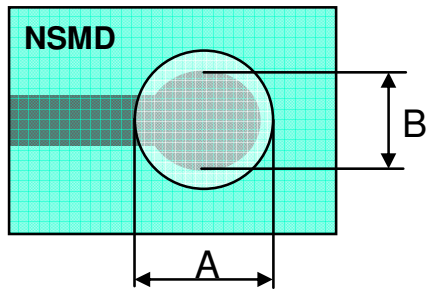
Non-solder-mask-defined (NSMD) land. Here, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the solder mask method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size.

See Figure 5 for an example of optimum land diameters and configurations (in mm) for a common MicroStar BGA pitch.

Solder Mask Defined



Non Solder Mask Defined



Ball Pitch		PWB Design		Stencil Design	
		A	B	Thickness	Opening
0.5mm	SMD	0.30	0.35	0.10	0.30
	NSMD	0.30	0.25	0.10	0.30

NOTE: We don't recommend using "U" shape PWB land because of trapping void during reflow.

Figure 5: Optimum Land Configurations

3.2 Conductor Width/Spacing

Many of today's circuit board layouts are based on at most a 100µm conductor line width and 200µm spacing. To route between 0.5–mm–pitch balls, given a clearance of roughly 190µm between ball lands, only one signal can be routed between ball pads. The 200µm ball spacing is worst case and is calculated by assuming the diameter of the solder ball land is 410µm.

Figure 5 presents some design considerations based on commonly used PCB design rules. Conventionally, the pads are connected by wide copper traces to other devices or to plated through holes (PTH). As a rule, the mounting pads must be isolated from the PTH. Placing the PTH interstitially to the land pads often achieves this.

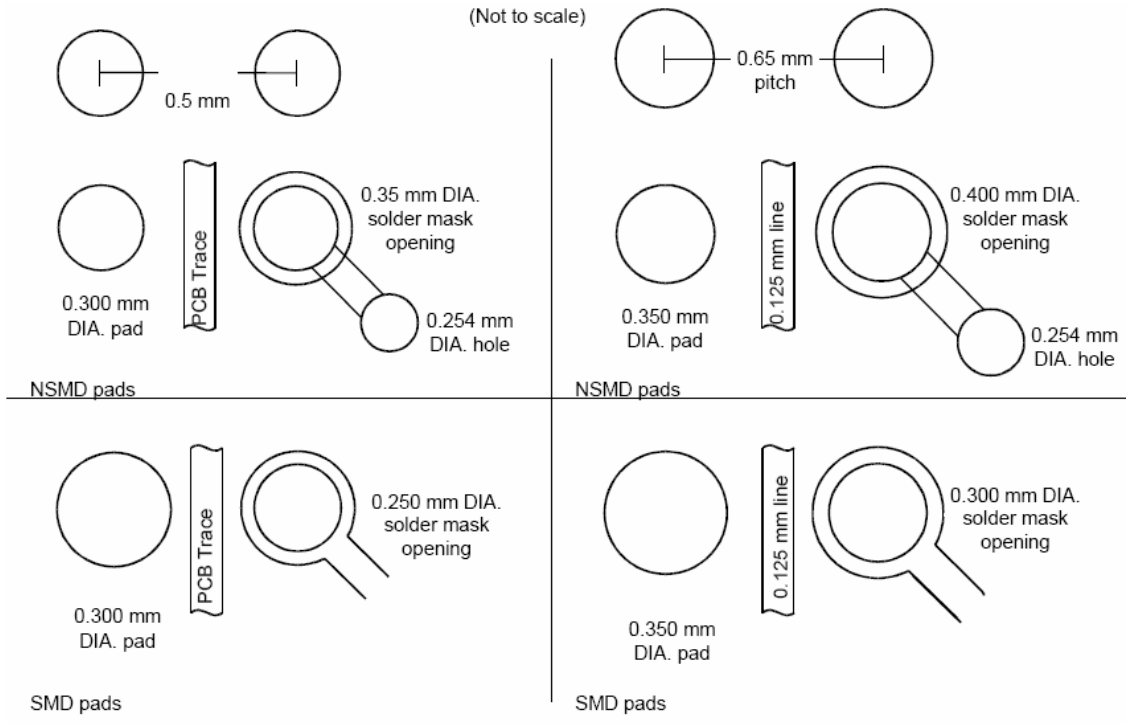


Figure 6: PCB Design Considerations (Conventional)

3.3 High–Density Routing Techniques

A challenge when designing with CSP packages is that as available space contracts, the space available for signal fanout also decreases. Routing of Micro Star Junior packages can be especially challenging because of the 0.5mm ball pitch and a full array of solder balls that most packages have. By using a few high–density routing techniques, the PCB designer can minimize many of these design and anufacturing challenges.

3.4 Via Density

Via density, as mentioned earlier, can be a limiting factor when designing high–density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia, shown in Figure 6, has solved many of the problems associated with via density.

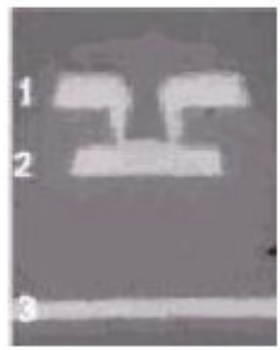


Figure 7: Microvia structure

Microvias are often created using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4–mil–thick dielectric layer, creating the 4µm microvia shown in Figure 6. The layout designer can now route to the first internal board layer. Two layers (each 4 mils thick) can be laser–drilled, creating a 200µm microvia diameter. In this case, routing to the first two internal layers is possible. The number of board layers increases as board chip density and functional pin count increase. The last layer can be used on the bottom side to place discrete components. Furthermore, by increasing the board layer stack–up to eight layers, high–density applications are possible with only 10 to 15 mils between the chips.

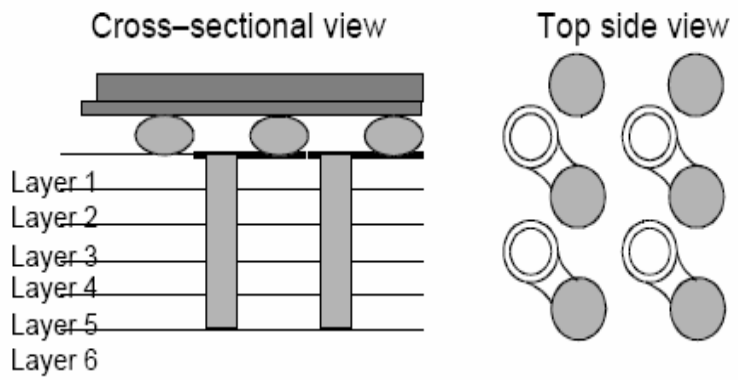


Figure 8: “Dog Bone Via” Structure

3.5 Conventional PCB Design

The relatively large via density on the package periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce or eliminate the via density problem on the periphery of the package, designers can build the PCB vertically from the BGA pad through the internal layers of the board, as shown in Figure 7.
By working vertically and mechanical drilling 250µm vias between the pads on the board and the internal layers, designers can create a "pick–and–choose" method. They can pick the layer and choose the route. A "dog bone" method is used to connect the through–hole via and the pad. This reduces the risk of trapped voids which can reduce the board mount process margin.
This method requires a very small mechanical drill to create the necessary number of vias for one package.
Although this method is the least expensive, a disadvantage is that the vias go through the board, creating a matrix of vias on the bottom side of the board. This may limit the use of using the back side for routing.

3.6 Advanced Design Methods

Another option is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers. Buried vias usually connect only the inner layers. Figure 12 illustrates this method using 4–mil laser–drilled microvias in the center of the pads and burying the dog bone on layer 2.

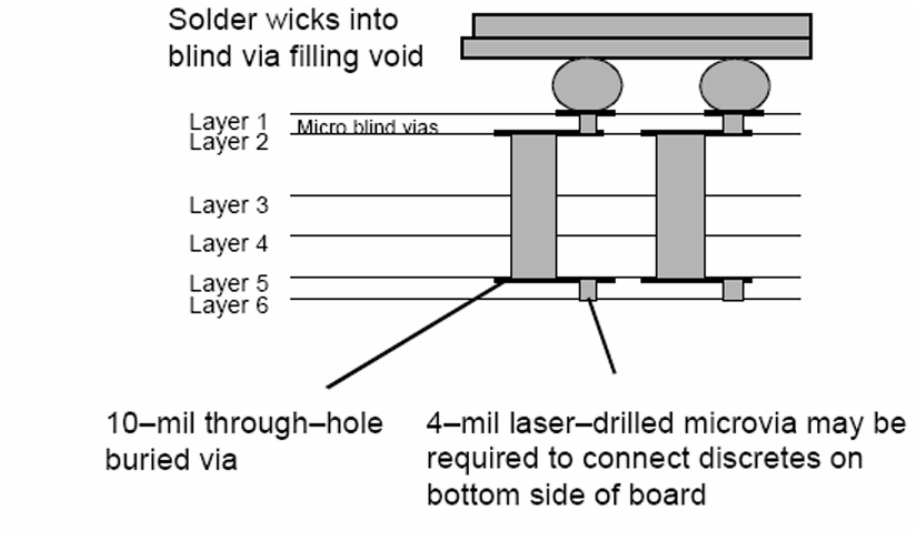


Figure 9: Buried vias

Since the buried via does not extend through the underside of the board, the designer can use another set of laser–drilled blind microvias, if needed, to connect the bypass capacitors and other discrete components to the bottom side.

4. Reliability

4.1 Daisy Chain Units

Daisy-chained units are used to gain experience in the handling and mounting of CSPs, for board-reliability testing, to check PCB electrical layouts, and to confirm the accuracy of the mounting equipment. To facilitate this, Texas Instruments offers daisy-chained units in all production MicroStar BGA packages, including the BRF6300.

Each daisy-chained pinout differs slightly depending on package layout. Daisy-chained packages are wired to provide a continuous path through the package for easy testing.

TI issues a net list for each package, which correlates each ball position with a corresponding wire pad number. The daisy-chained net list is a special case of the general net list.
When a daisy–chained package is assembled on the PCB, a complete circuit is formed, which allows continuity testing. The circuit includes the solder balls, the metal pattern on the die, the bond wires, and the PCB traces. The entire package or only a quadrant can be interconnected and tested. A diagram of the test configuration is shown in Figure 9.

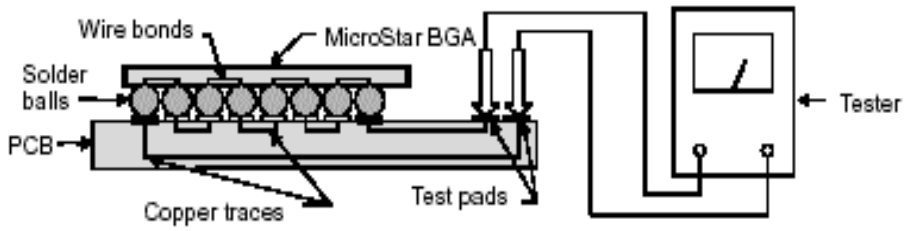


Figure 10: Daisy Chain Test Configuration

4.2 Reliability data

Reliability is one of the first questions designers ask about any new packaging technology. They want to know how well the package will survive handling and assembly operation, and how long it will last on the board. The elements of package reliability and system reliability, while related, focus on different material properties and characteristics and are tested by different methods.

Package reliability focuses on materials of construction, thermal flows, material adherence/delamination issues, resistance to high temperatures, moisture resistance and ball/stitch bond reliability. Thorough engineering of the package is performed to prevent delamination caused by the interaction of the substrate material and the mold compound.

TI subjects each MicroStar BGA to rigorous qualification testing before the package is released to production.

These tests are summarized in Table 1. All samples used in these tests are preconditioned according to Joint Electronic Device Committee (JEDEC) A113 at various levels. Typical data is presented in Table 2. MicroStar BGA packages have proven robust and reliable.

Board–level reliability (BLR) issues generally focus on the complex interaction of various materials under the influence of heat generated by the operation of electronic devices. Not only is there a complex thermal situation caused by multiple heat sources, but there are cyclical strains due to expansion mismatches, warping and transient conditions, non–linear material properties, and solder fatigue behavior influenced by geometry, metallurgy, stress relaxation phenomenon, and cycle conditions. In addition to material issues, board and package design can influence reliability. Thermal management from a system level is critical for optimum reliability, and thermal cycling tests are generally used to predict behavior and reliability. Many of these are used in conjunction with solder fatigue life models using a

modified Coffin–Manson strain range–fatigue life plots (number of cycles to failure has an inverse exponential relationship with the thermal cycle temperature range).

Test Environments	Conditions	Read Points
HAST	85RH/85°C	600 hrs. 1000 hrs.
Autoclave	121°C, 15 psig	96 hrs. 240 hrs.
Temp. Cycle	-55/125°C -65/150°C‡	500 cycles 750 cycles 1000 cycles
Thermal Shock	-65/150°C‡ -55/125°C	200 cycles 500 cycles 750 cycles 1000 cycles
HTOL	125°C, Op. voltage	500 hrs. 600 hrs. 1000 hrs.
HTOL‡	140°C, Op. voltage	500 hrs.
HTOL‡	155°C, Op. voltage	240 hrs.
Bake‡	150°C 170°C	600 hrs. 1000 hrs. 420 hrs.
HAST‡	130°C	96 hrs.

† All samples used in these tests are preconditioned according to Joint Electronic Device Committee (JEDEC) A113 at various levels.

‡ Optional tests. One or more of them may be added to meet customer requirements.

Table 1: Package Level Reliability tests

5. Surface Mounting MicroStar BGA Packages

Surface-mount technology (SMT) has evolved over the past decade from an art into a science with the development of design guidelines and rules. While these guidelines are specific enough to incorporate many shared conclusions, they are general enough to allow flexibility in board layouts, solder pastes, stencils, fixturing and reflow profiles. From experience, most assembly operations have found MicroStar BGA packages to be robust, manufacturing-friendly packages that fit easily within existing processes and profiles. In addition, they do not require special handling. However, as ball pitch becomes smaller, layout methodology and placement accuracy become more critical. Below is a review of the more important aspects of surface-mounted CSPs. The suggestions provided may aid in efficient, cost-effective production.

5.1 Design for Manufacturability

A well-designed board that follows the basic surface-mount technology considerations greatly improves the cost, cycle time, and quality of the end product. Board design should comprehend the SMT-automated equipment used for assembly, including minimum and maximum dimensional limits and placement accuracy. Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. While odd-shaped or small boards can be assembled, they require panelization or special tooling to process in-line. The more irregular the board—non-rectangular with no cutouts—the more expensive the assembly cost.

The following guidelines may be helpful:

- Automated equipment requires a minimum of two and preferably three fiducials.
- A wide range of fiducial shapes and sizes can be used. Among the most useful is a circle 1.6 mm in diameter with an annulus of 3.175/3.71 mm. The outer ring is optional, but no other feature may be within 0.76 mm of the fiducial.
- The most useful placement for the fiducials is an L configuration, which is orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0, 0).
- All components should be within 101.6 mm of a fiducial to guarantee placement accuracy. For large boards or panels, a fourth fiducial should be added.

If the edges of the boards are to be used for conveyer transfer, a cleared zone of at least 3.17 mm should be allowed. Normally, the longest edges of the board are used for this purpose, and the actual width is dependent on equipment capability. While no component lands or fiducials can be in this area, breakaway tabs may be.

Interpackage spacing is a key aspect of DFM, and the question of how close you can safely put components to each other is a critical one. The following component layout considerations are recommendations based on TI experience:

- There should be a minimum of 0.508 mm between land areas of adjacent components to reduce the risk of shorting.
- The recommended minimum spacing between SMD discrete component bodies is equal to the height of the tallest component. This allows for a 45° soldering angle in case manual work is needed.
- Polarization symbols need to be provided for discrete SMDs (diodes, capacitors, etc.) next to the positive pin.
- Pin–1 indicators or features are needed to determine the keying of SMD components.
- Space between lands (under components) on the backside discrete components should be a minimum of 0.33 mm. No open vias may be in this space.
- The direction of backside discretes for wave solder should be perpendicular to the direction through the wave.
- Do not put SMT components on the bottom side that exceed 200 grams per square inch of contact area with the board.
- If space permits, symbolize all reference designators within the land pattern of the respective components.
- It is preferable to have all components oriented in well–ordered columns and rows.
- Group similar components together whenever possible.
- Room for testing needs to be allowed.

5.2 Solder Paste

TI recommends the use of paste when mounting MicroStar BGAs. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- It helps compensate for minor variations in the planarity of the solder balls.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted component. Most assembly operations have found that no changes in existing pastes are required by the addition of MicroStar BGA, but due to the large variety of board designs and tolerances, it is not possible to say this will be true for any specific application.

Nearly as critical as paste selection is stencil design. A proactive approach to stencil design can pay large dividends in assembly yields and lower costs. In general, MicroStar Junior BGA packages are special cases of BGA packages, and the general design guidelines for BGA package assembly applies to them as well.
The typical stencil hole diameter should be the same size as the land area, and 100-120–mm–thick stencils have been found to give the best results. Good release and a consistent amount of solder paste and shapes are critical, especially as ball pitches decrease. The use of metal squeegee blades, or at the very least, high durometer polyblades, is important in achieving this.
Paste viscosity and consistency during screening are some variables that require close control.

5.3 Solder Ball Collapse

In order to produce the optimum solder joint, it is important to understand the amount of collapse of the solder balls, and the overall shape of the joint. These are a function of:

- The diameter of the package solder ball via.
- The volume and type of paste screened onto the PCB.
- The diameter of the PCB land.
- The board assembly reflow conditions.
- The weight of the package.

The original ball height on the package for a typical 0.5-mm-pitch package is 0.30 mm. After the package is mounted, this typically drops to 0.25 mm, as illustrated in
Figure 11.

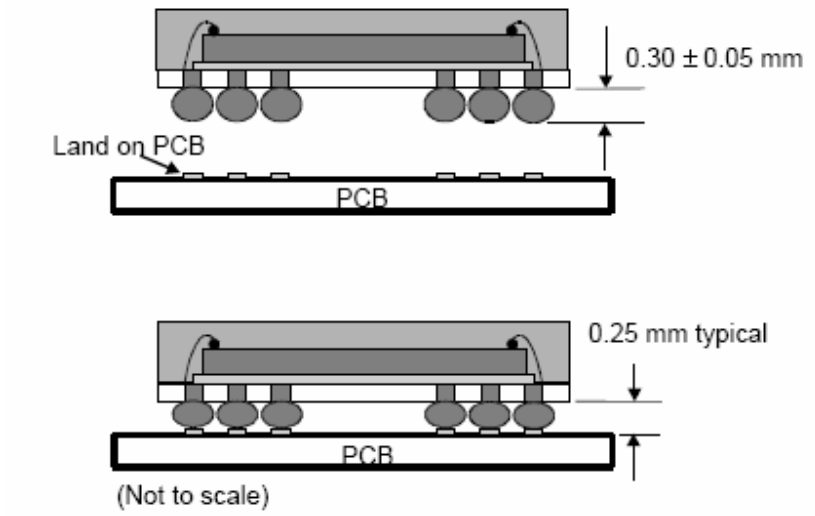


Figure 11: Solder Ball Collapse

Controlling the collapse, and thus defining the package standoff, is critical to obtaining the optimum joint reliability. Generally, a larger standoff gives better solder joint fatigue strength, but this should not be achieved by reducing the board land diameter. Reducing the land diameter will increase the standoff, but will also reduce the minimum cross-section area of the joint. This, in turn, will increase the maximum shear force at the PCB side of the solder joint. Thus, a reduction of land diameter will normally result in a worse fatigue life, and should be avoided unless all the consequences are well understood.

5.4 Reflow

Solder reflow conditions are the next critical step in the mounting process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the surfaces takes place by wicking of molten solder, the solder balls collapse, and finally solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with small or no voids and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven joint thickness, discontinuities, and insufficient fillet can occur. While the exact cycle used depends on the reflow system and paste composition, there are several key points all successful cycles have in common.

The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat or a bake, or, more commonly, a hold in the cycle at evaporation temperatures. If there is less solvent in the paste (such as in a high-viscosity, high-metal-content paste), then the hold can be shorter. However, when the hold is not long enough to get all the solvent out or too fast to allow it to evaporate, several negative things happen. These range from solder-particle splatter to trapped gases, which can cause voids and embrittlement. A significant number of reliability problems with solder joints can be solved with the warm-up step, so it needs careful attention.

The second key point that successful reflow cycles have in common is uniform heating across the package and the board. Uneven solder thickness and non-uniform solder joints may be an indicator that the profile needs adjustment. There can also be a problem when different sized components are reflowed at the same time. Care needs to be taken when profiling an oven to be sure that the indicated temperatures are representative of what the most difficult to reflow

parts are seeing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow, than with others, such as forced hot-air convection.

Finally, successful reflow cycles strike a balance among temperature, timing, and length of cycle. Mistiming may lead to excessive fluxing activation, oxidation, excessive voiding, or even damage to the package. Heating the paste too hot too fast before it melts can also dry the paste, which leads to poor wetting. Process development is needed to optimize reflow profiles for each solder paste/flux combination.

The profile shown in Figure 12 below is the recommended profile for the MicroStar/Jr. devices used in both standard packaging options and the stacked RAM used in BRF6300.

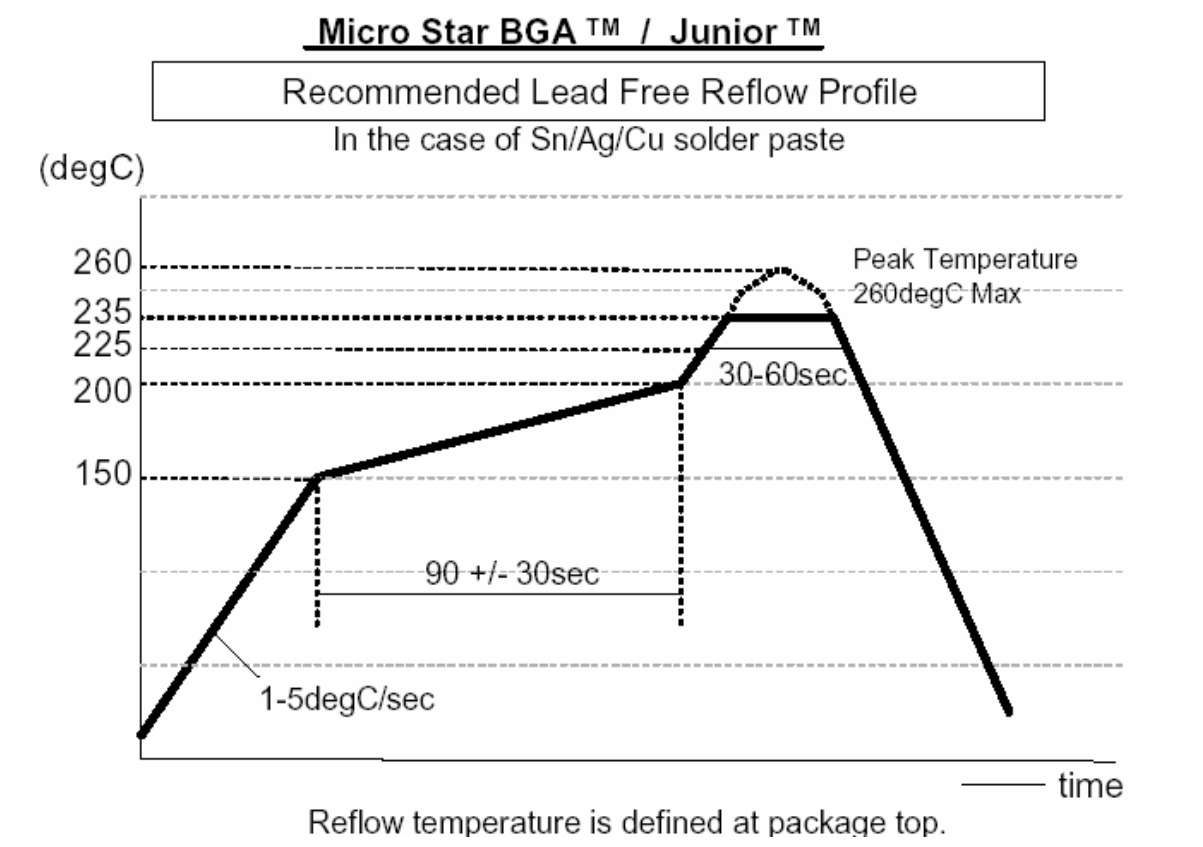


Figure 12: Recommended Reflow Profile

5.5 Inspection

MicroStar Junior BGA packages have been designed to be consistent with very high–yield assembly processes. Because of their relatively light weight, MicroStar Junior BGA packages tend to self–align during reflow. Since the pitch of the ball pattern is large compared to that of fine–pitch leaded packages, solder bridging is rarely encountered. It is recommended that a high–quality solder joint assembly process be developed using the various inspection and analytical techniques, such as cross–sectioning.

Once a quality process has been developed, detailed inspection should not be necessary. Visual methods, while obviously limited, can offer valuable clues to the general stability of the process. Electrical checks can confirm interconnection. Both transmission X–rays and laminographic X–rays have proven to be useful nondestructive tools, if desired.

6. Lead Free Solutions

Environmental concerns are driving the need for lead-free solutions to electronic components and systems. Texas Instruments (TI) has been a leader in working with our customers to provide them with products, which meet their specific needs. The first practical lead-free alternative was the Nickel/Palladium (Ni/Pd) finish introduced by TI in 1989. Since then, more than 30 billion lead-free Ni/Pd components have been supplied. Texas Instruments continues to be active in this field, working with other manufacturers to evaluate other lead-free finishes to understand their manufacturability and reliability.

Continuing this position of leadership, TI has introduced a lead-free solder ball option for the MicroStar BGA packages. Texas Instruments is also evaluating lead-free solder ball applications for other area array packages. In conjunction with this effort, TI is an active participant in the industry-wide effort to evaluate lead-free solder alloys and lead-free printing wiring board finishes. Several of the lead-free systems being proposed require a maximum reflow temperature higher than that needed with the Sn/Pb systems, so package and system reliability data must be developed. Securing the required Board Level Reliability (BLR) under various customer conditions depends on many factors: solder ball composition, solder paste, PCB design, land finish and reflow conditions.

The composition TI has selected for lead-free MicroStar BGA packages is an Sn-Ag-Cu alloy. Reliability data presented in Table 9 shows it to be a robust performer, equivalent to the Sn/Pb eutectic balls it replaces.

Extensive assembly testing has shown it to be virtually indistinguishable from Sn/Pb eutectic ball performance in current systems and superior in high temperature, lead-free systems.

The BRF6300 MicroStar packages are lead free (Green, RoHS6 & no Sb/Br).

Comment: due to the lead free the reflow temperature profile and peak temperature is higher then non-lead free packages, for exact reflow profile refer to Figure 12: Recommended Reflow .

6.1 Moisture Sensitivity

A drop of 3+ levels in moisture sensitivity (as per J-STD-20) has been indicated for several package types with the peak temperature of 260°C. Extensive testing of MicroStar BGA packages has shown they are capable of resisting the 260°C cycles without an impact on the moisture sensitivity classification.

7. Package Technical Details

7.1 Package information

Component ID code/number/name	S-PBGA-N63	
Package type and name	MicroStar Junior 63ZSL (4.5x4.5; 0.5mm pitch)	
Package marking	**Component**	TI logo
	Orientation	#A1 / bottom right corner
Package attributes	Ball count	63
	Ball pitch (mm)	0.5
	Ball diameter / dimensions (mm)	0.25 / 0.35
	Ball height / substrate standoff (mm)	0.11 / 0.21
	Coplanarity (mm)	0.08
	Package thickness (mm)	0.8 Max
	Package weight (g)	0.0258g
	Substrate type	Polyimide tape
	Substrate layer count	1
	Max footprint (mm x mm)-center to center	4.50x4.50mm
	Die size, per side	Max die size= 3.35 X 3.35 mm
	Thickness	165 um
	Interconnect method (WB, TAB, FC)	WB
	Daisy chain level (if daisy chain component)	Level 3
	Available shipping media	Tray and Tape&Reel
	Components in one shipping package / in one dry package	Tape&Reel= 2500 / bag

7.2 Package structure and materials

Substrate material	Polyimide
Substrate pad diameter	N/A
Via surface finish and thickness (um)	Bare Cu for Pb free balls
Substrate via diameter (um)	280
Substrate via filling	oZ100-337C-21-11.5TI
Conductor material	Cu
Die bond pad metallization	AL
Die coating	NO
Die attach adhesive	84-3MVB-TI (paste)
Die attach adhesive cover (%)	> 75 %
Solder Ball composition	LF35 SnAgCu based
Molding resin	CEL9500 -1 (RoHS compliant)
If wire bonded:	
Wire type and diameter	Gold, 24.3 um

7.3 PWB board design recommendations

Pad design recommendations	Pad geometry (mm)	SMD pad = 0.35 mm
		NSMD pad = 0.25 mm
	Pad opening (mm, SMD/NSMD)	SMD = 0.3mm
		NSMD = 0.3mm
PWB board technology requirements	Routing study for I/O	-
	Feasible PWB board surface finishes	-
PWB board assembly recommendations	Solder paste type (Pb free)	Sn/Ag based
	Stencil thickness (mm)	0.1
	Stencil opening (mm)	0.3
	Pick up tool	-
	Max reflow temperature (deg C)	260
	Max dwell temperature (deg C)	235
	Max dwell time (sec)	30 –60 sec
	# Reflow max	Max 3
Package storage information	Shelf life / Extended shelf life	12 months @40C/90% RH
	Storage conditions / Extended storage conditions	Dry packed
	Moisture sensitivity classification (Jedec 1, 2a, 2b, 3…)	Level 3 – 260 deg C max
	Packages prebaked before shipment	Yes
	Packages prebaked recommendations and how many times it can be performed	150C, 8hrs
	Trays or tapes tolerate prebaking	Tray: Yes
		Tape: No

7.4 Package qualifications

<table>
<tr><td rowspan="6">Package level tests</td><td rowspan="6">Done
(Pass)</td><td colspan="3">Test</td><td>Condition</td><td colspan="2">Read point</td></tr>
<tr><td colspan="3">TC</td><td>-55/+125 C</td><td colspan="2">1000 cycles</td></tr>
<tr><td colspan="3">TS</td><td>-55/+125 C</td><td colspan="2">200 cycles</td></tr>
<tr><td colspan="3">AU</td><td>121 C/2 ATM</td><td colspan="2">96 hours</td></tr>
<tr><td colspan="3">THB</td><td>85 C/85% RH</td><td colspan="2">1000 hours</td></tr>
<tr><td colspan="3">STO</td><td>150 C</td><td colspan="2">1000 hours</td></tr>
<tr><td>Board level tests</td><td>Done
(Pass)</td><td colspan="6">• Temperature cycles (-40 to 120 C): 1000 cycles.
• Key push: (20% change)
• Drop test: (500 drops)</td></tr>
<tr><td rowspan="11">Thermal characteristics</td><td colspan="4" rowspan="2">Power consumption (Max and Typical)</td><td>Max</td><td>Typical</td></tr>
<tr><td>0.54W (@ 125C junction & 85C ambient)</td><td>-</td></tr>
<tr><td colspan="4">Recommended operating temperature range (Junction and case)</td><td>125 deg C Junc</td><td></td></tr>
<tr><td colspan="4">Maximum allowed temperature (junction and case)</td><td>260 deg C (1)</td><td></td></tr>
<tr><td colspan="4">Thermal resistance junction to case with 2s</td><td></td><td></td></tr>
<tr><td colspan="3" rowspan="3"></td><td>Maximal Die size</td><td></td><td>3.35 X 3.35 mm</td></tr>
<tr><td>Still air</td><td></td><td>115.4 C/W</td></tr>
<tr><td>Moving air</td><td></td><td>N/A</td></tr>
<tr><td colspan="4">Thermal resistance junction to ambient with standard 2s2p</td><td></td><td></td></tr>
<tr><td rowspan="3"></td><td colspan="2">Die size</td><td></td><td></td><td>3.35 X 3.35 mm</td></tr>
<tr><td>Still air</td><td>0</td><td></td><td></td><td>74.3</td></tr>
<tr><td></td><td>150</td><td></td><td></td><td>71.0</td></tr>
</table>

		Moving air LFM	250		69.3
			500		67.2

(1) Maximum reflow for Pb-free process compliant product

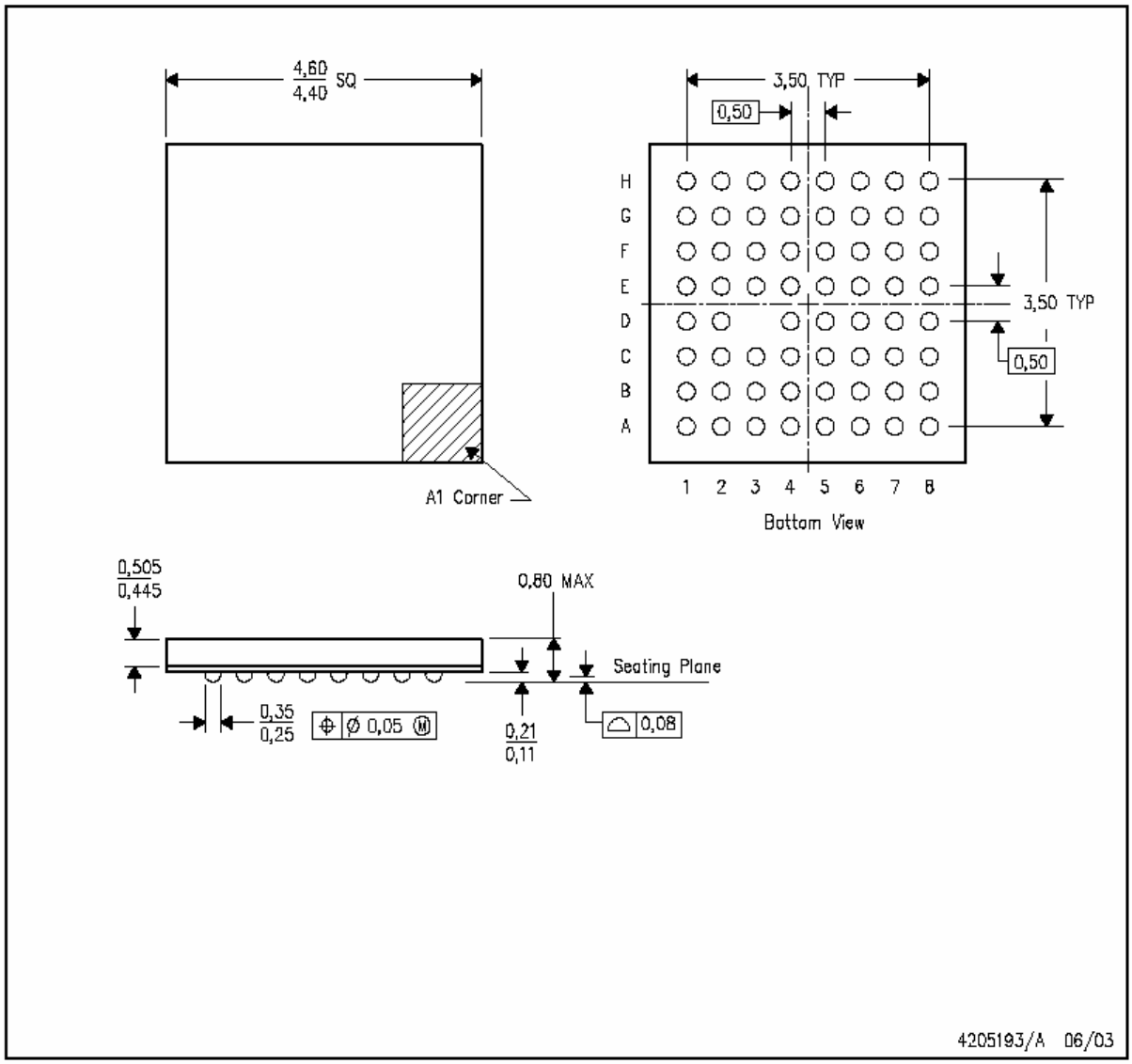
7.5 Package material properties

Item		Materials	Thickness (um)	Young Modulus (GPA)	Poisson Ratio	CTE (ppm)	Density (Kg/mm3)
Die		Silicon	165	130	0.28	2.9	2.33E-06
Die coating		Si-Nitride	Prop.	150	0.2	1.1	2.50E-06
Passivation layer		None	None	None	None	None	None
Die attach		Film	100	15	0.2	19	1.77E-06
Bonding wire		Gold	24.3	57	0.42	19.5	1.93E-05
Substrate		Polymide	50	9.24	0.3	19.5	1.42E-06
Copper races	0.5 mm pitch	Copper	18	130	0.34	17	8.9E-06
Substrate via	Solder (LF35)	Sn-Ag based	62	36.3	0.36	20.9	7.30E-06
Substrate pad	0.5 mm pitch	Copper	18	130	0.34	17	8.9E-06
Mold_cmpd		Biphenol Resin	650	23	0.21	21.6	2.03E-06
Solder ball	LF35	Sn-Ag based	0.25	36.3	0.36	21.5	7.3E-06

7.6 ZSL Package, 63 balls, 4.5mm x 4.5 mm

MECHANICAL DATA

ZSL (S–PBGA–N63) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. This package is lead–free.

7.7 Stacked RAM Package, 63 balls, 4.5mmx4.5mm

The stacked RAM device is available for development use only and is not available in high volumes. Its main use is to enable customers to update the firmware code during the development phase of the device, thus enables to get the advantage of testing the latest BRF6300 firmware releases as they become available, and before it is available on the ROM device.

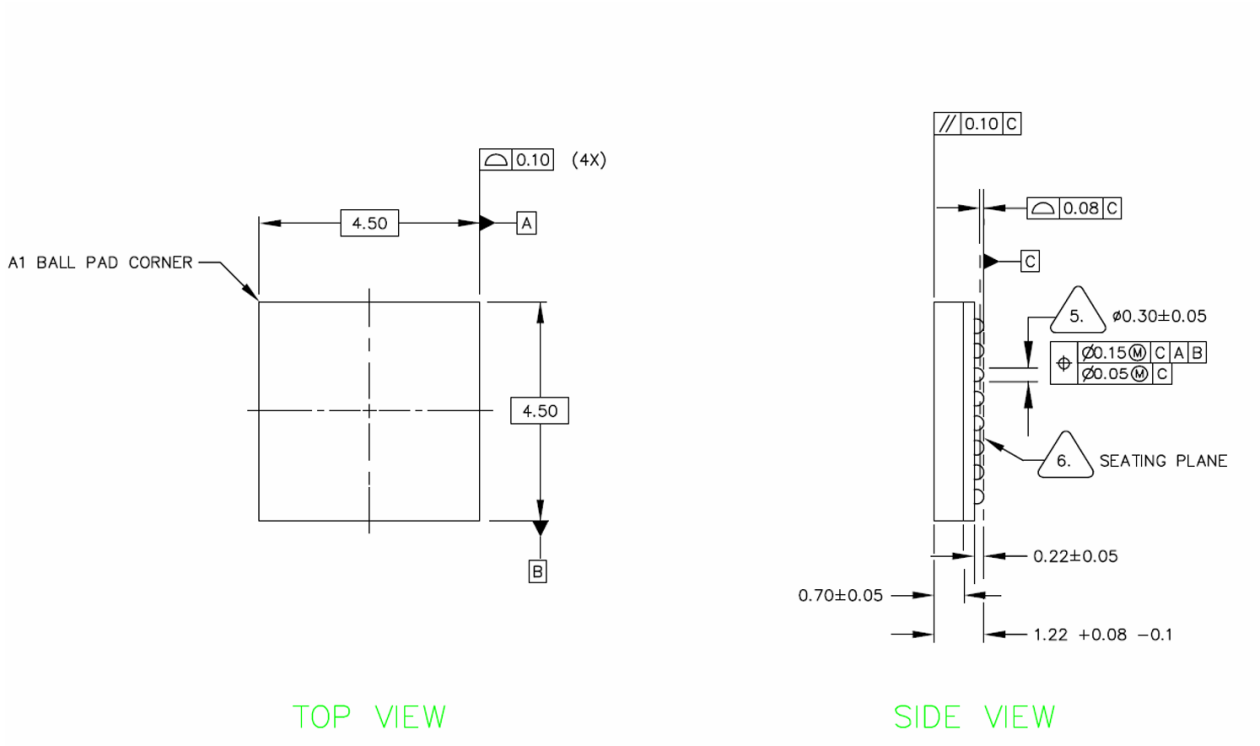


Figure 13: Stacked RAM package top and side view

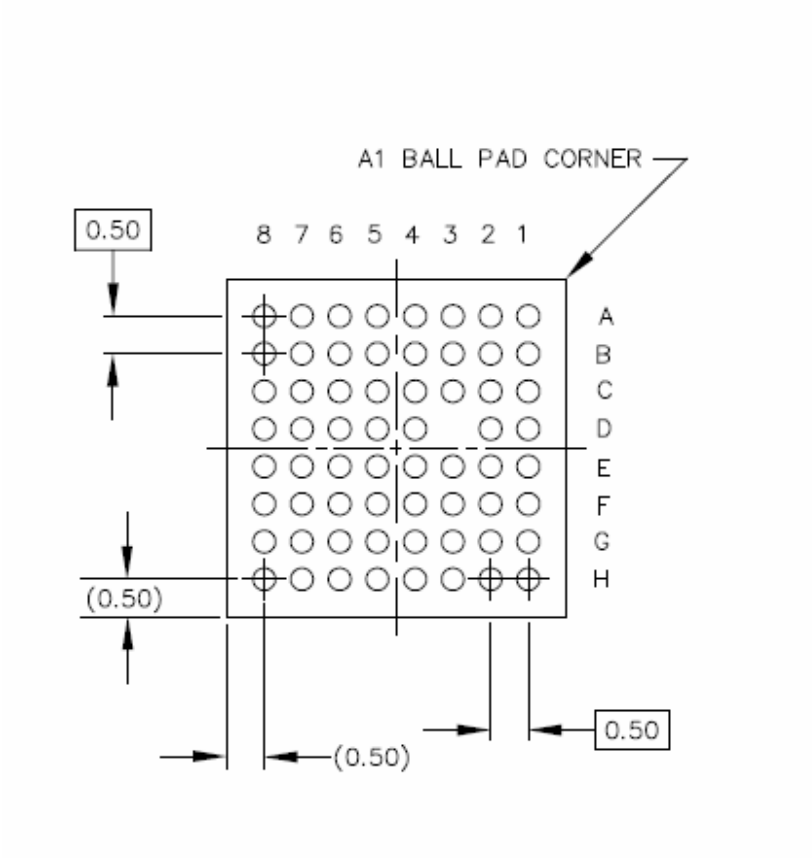
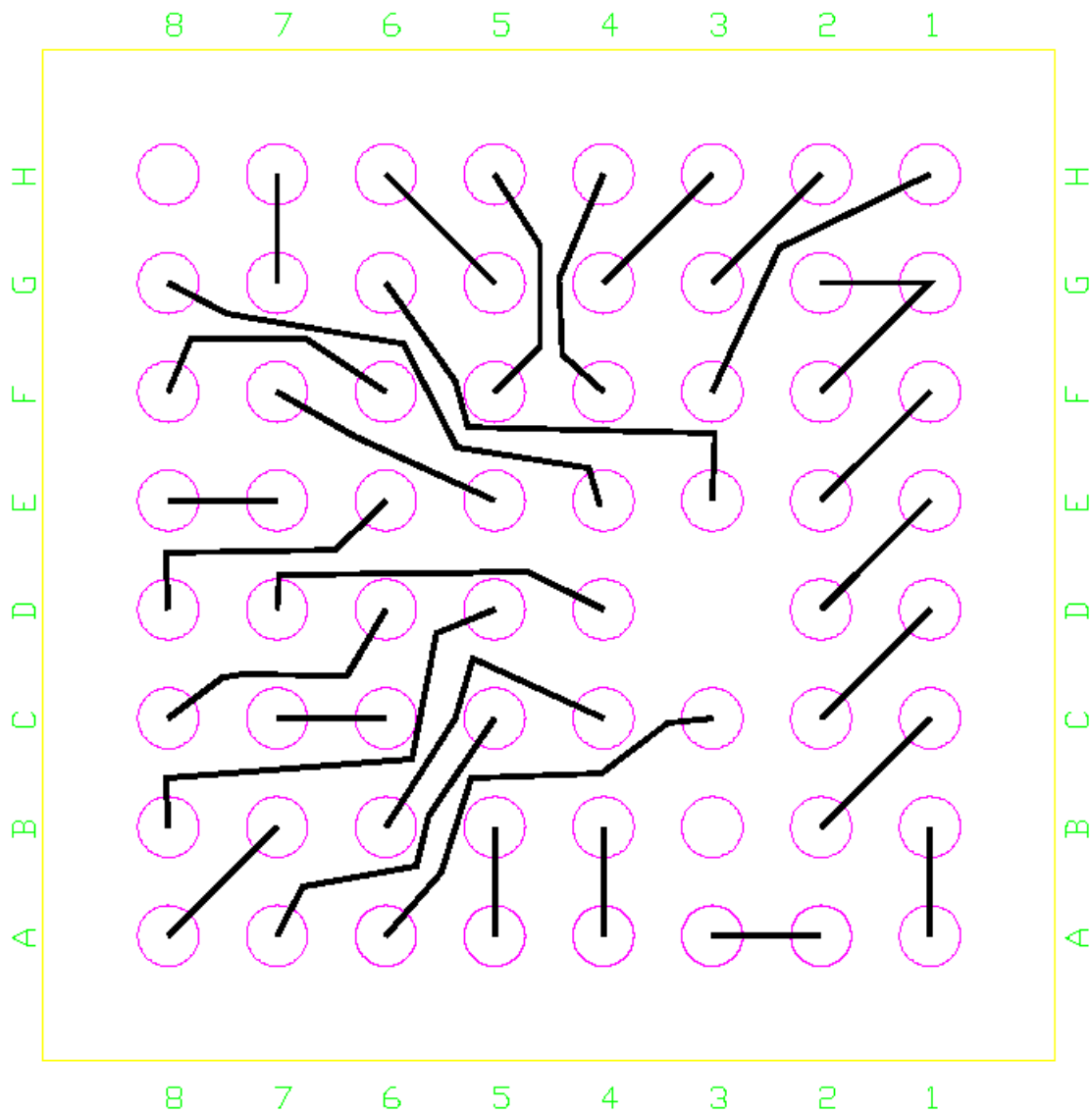


Figure 14: Stacked RAM package bottom view

7.8 Daisy Chain Package, 63 balls, 4.5mm x4.5mm

The part number of the daisy chain package is DC63AZSLR.



7.8.1 4.5 x 4.5 Daisy Chain device net list

Below are the net list connections that are also illustrated in the previous section

Ball to	Ball	Ball to	Ball	Ball to	Ball
A1	B1	F5	H5	C8	D6
B2	C1	G5	H6	D5	B8
C2	D1	G6	E3	C7	C6
D2	E1	H7	G7	A8	B7
E2	F1	G8	E4	C5	A7
F2	G1,G2	F6	F8	B6	C4
H1	F3	F7	E5	A6	C3
H2	G3	E8	E7	B5	A5
H3	G4	E6	D8	B4	A4
H4	F4	D4	D7	A3	A2

Table 2: 4.5 x4.5 Daisy Chain device net list

BRF6300 BGA Package Information

January 2, 2007
BT-AN-0046, Revision 0.3

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