Application Note

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BRF6300 PCB Design Guidelines, Rev 0.3

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ABSTRACT

BRF6300 is a RF device, targeted to operate on a cellular board. When designing board with the BRF6300 device, design rules and layout guidelines must be taken into consideration.

This document describe the guidelines for designing PCB, including placement , layout rules and the reflow profile for soldering the device.

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1 Overview

This document describes PCB design guidelines, PCB placement and layout guidelines for BRF6300.

Also described is the reflow soldering profile recommendations for BRF6300 device.

2 Introduction

BRF6300 is a RF device, targeted to operate on a cellular board. When designing board with the BRF6300 device, design rules and layout guidelines must be considered.

The following sections of this document describe the guidelines for designing PCB, including: placement, layout rules and the reflow profile for soldering the device.

This document is complementary to the BRF6300 data sheet, and is not intended to replace it. It is strongly recommended to use the full range of data sheet and application notes for a system design.

It is strongly recommended to follow the design rules in this document, to achieve good performance similar to the performance measured in Texas Instrument's labs.

These guidelines are based on previous experience with BRF6300 on cellular board. Following these rules will help to avoid mistakes that would result in unnecessary spins to the PCB, and as a result, longer time to market

For any question or issue faced during the layout process that contradicts one of the following rules, please consult Texas Instrument's representative.

3 PCB and Stack-Up

The recommendations in this document refer to a PCB with BRF6300 based on standard FR4 with six layers, which is the technology commonly used in Cellular application.

Among these 6 layers, there should be at least two signaling layers, one Ground Layer and one Power Layer. It is recommended that Layer 3 would be the ground Layer, for good RF reference ground. The reference ground should be at distance of about 8mil beneath the RF path (for BGA package).

A PCB with more layers can be used, though is not required.

A PCB with four layers can be used as well.

When using the BRF6300 WSP Package, in order to enable connection of traces to each pad; Micro-Vias must be used. Micro-Vias should be used between layer 2 -3 to allow routing of the device.

Using Micro-Vias has many advantages, since Micro-Vias are smaller than through Vias, it adds flexibility to the design, shorten lead lengths, enable smaller design, and more effective connection between traces in different layers.

The reference design (as can be seen in the following examples) is based on a board with through Vias connecting internal layers, and Micro-Vias connecting two external layers.

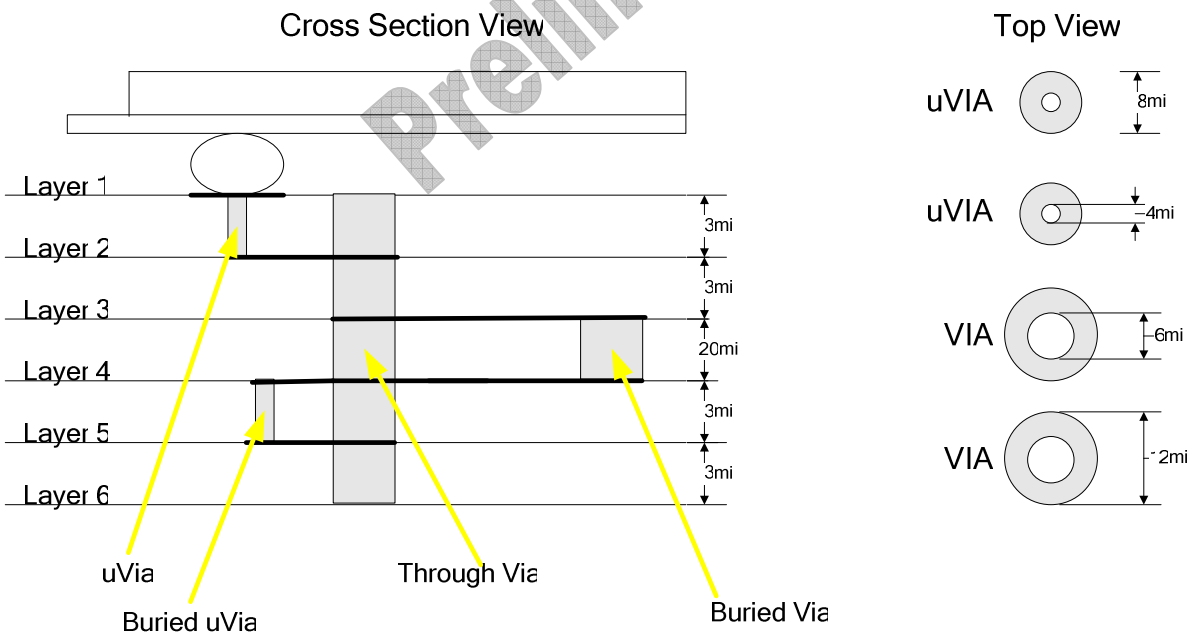


Figure 1 - Via structure of reference design

4 Placement of External Components

The external components should be placed near the BRF6350. The traces should be as short as possible from the pads of the BRF6350 to the pads of the external components (refer to Figure).

4.1 LDOs capacitors

The capacitors connected to LDO outputs should be placed as close as possible to BRF6300. The trace connecting the capacitors to the device should be as short as possible, and should use wide traces if possible. Capacitors ground connections should be strengthened with Vias. The Vias should be on the ground pad or next to the ground pad of the capacitor, to internal ground plane (Layer 3). If not possible to apply this rule for all capacitors, use the following priorities:

1. OSC_LDO_OUT
2. ANA_LDO_OUT, RFIO_LDO_OUT
3. BB_LDO_OUT, FLDO_OUT

Please note that the Vias of the capacitors below should all be connected to ground plane on Layer 3. For example see below.

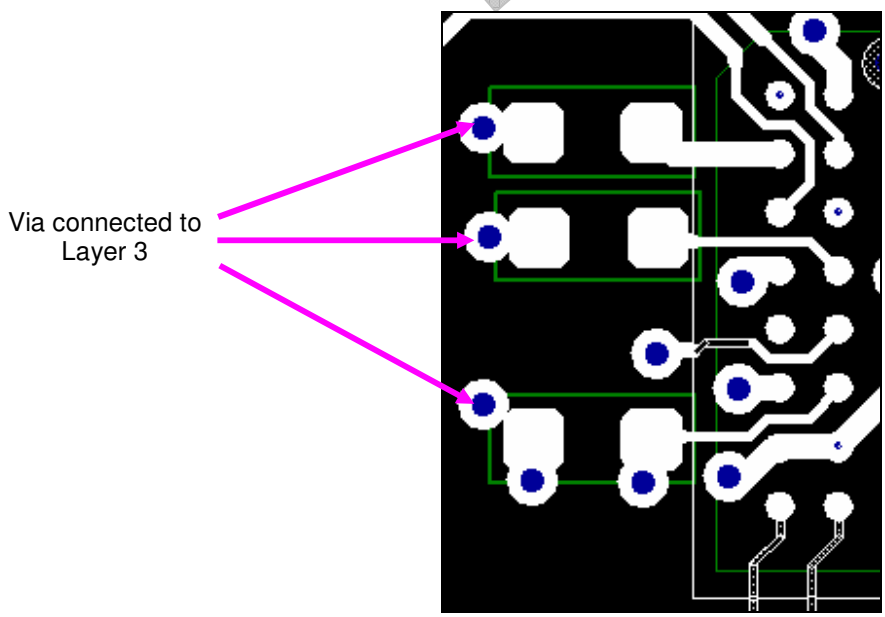


Figure 2 – Capacitors close to BRF6300 with strong ground

5 Clocks

The clock signals have great influence on the RF performance, and are susceptive to noise. The clock signals can also act as interferers to other signals.

As a general guideline, the clock signals should be as short as possible.

5.1 Clock signal isolation

Separate the clock signals supplied to the device from other signals, using grounded strips. The fast clock should not have traces in close proximity and the trace should not be routed in parallel to other signals.

5.2 Clock routing

Special care should be taken to avoid cutting the ground plane beneath the RF part with the clock trace.

The below example shows the Fast Clock routed ***incorrectly***, crossing the whole area of the BRF6300 device above passing very close to the Slow Clock, this type of error should be avoided. When routing a signal and required to route over a digital clock signal, it is recommended to route at a **90°** to minimize coupling.

As a general layout recommendation it is recommended to route adjacent layers in opposite directions, one layer vertical routing and other layer horizontal routing for minimal interference.

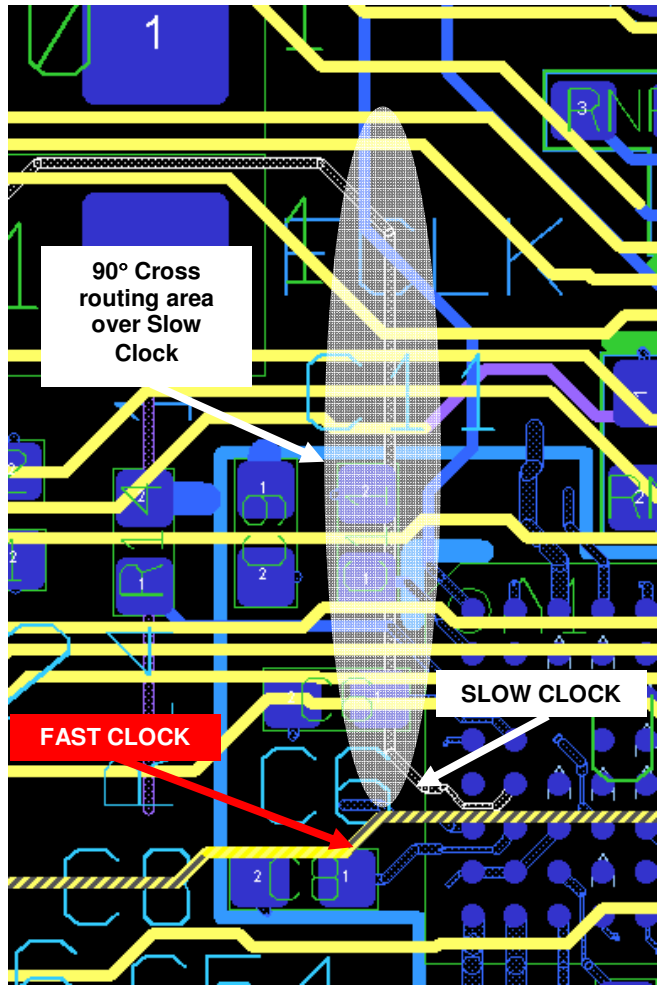


Figure 3 - Problematic example of Fast Clock routing

5.3 Slow Clock and Digital Clock Signals

The following signals are digital clock signals:

- Slow Clock
- Audio Clock (AUD_CLK)
- I^2C Clock (SCL)
- SDIO / SPI Clock (IO7)

Slow clock signals and the digital clocks signals described above are a source of noise. Special care should be taken to avoid laying the traces next to sensitive signals such as RF path, OSC_LDO, RFIO_LDO, etc.

Whenever possible the traces of these signals should be as short as possible and keep-out clearance should be kept around them.

5.3.1 Crystal as the clock source

In case using crystal as the clock source, the parasitic characteristics of the clock trace influence the oscillation. The crystal should be placed as close as possible to the BRF6300. The traces should be as short as possible. Too wide traces may lead to excessive capacitance, while too narrow traces may lead to parasitic inductance of the clock trace. Trace width of about 10mil should be used for **short** clock traces.

6 BT RF Design

When designing the RF path, placement and layout rules must be followed.

6.1 RF path

The BT RF path should be laid out on the Top Layer only, with traces kept as short as possible on the unbalanced section. It is recommended to keep the entire BT RF path in straight line. See for WSP package layout example.

The vertical traces (x2) connecting to the capacitors have been set to a specific length, simulating the required impedance in order to acquire the required matching.

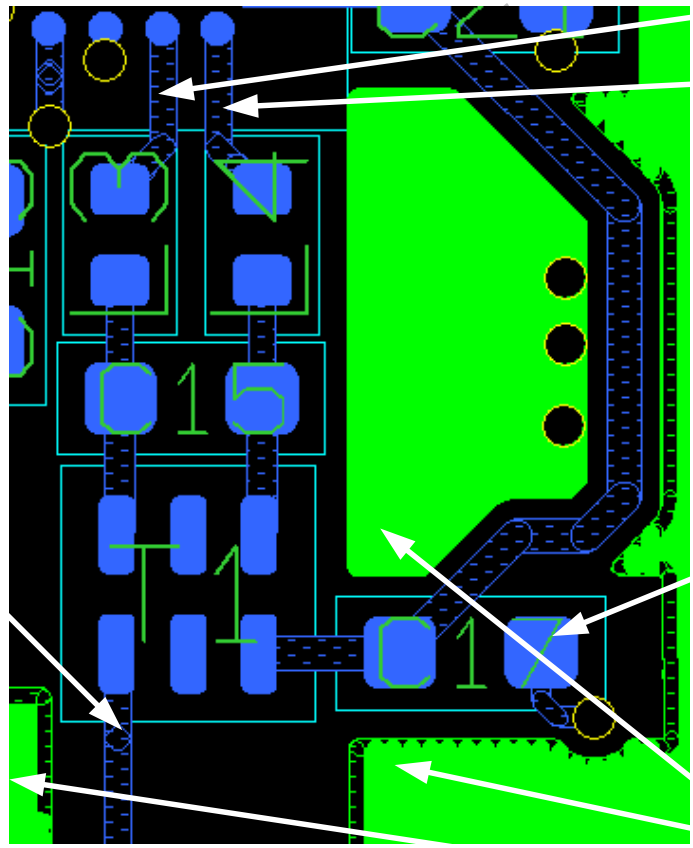


Figure 4 – BT RF path

6.2 Balanced BT RF lines

The differential lines (between the Balun / Filter and the BRF6300) at the BT RF input / output pads should be routed with the same length (as short as possible in accordance to Balun manufactures requirements) and must be parallel and symmetrical. The width of the differential lines should not be wide, in order to avoid excessive parasitic capacitance before the BALUN / Filter (about 8mil). There is no need to use matched impedance traces for the Balanced RF lines. Refer to . The differential lines should be simulated and calculated using a RF simulator program to achieve the best matching network.

When using a matched BALUN / Filter please strictly follow the manufactures requirements.

6.3 Unbalanced BT RF line

The single ended part of the RF path (after the BALUN / Filter), must use trace width, calculated for 50ohm impedance matching (according to the distance from the reference ground). Refer to .

6.4 Ground beneath BT RF path

In order to avoid parasitic capacitance and parasitic RF coupling, the area beneath the BT RF components, in layers 1 and layer 2 must ***not*** be ground, and must be free from other signals. A minimal distance to the RF Ground Layer of 6mil should be kept to ensure small parasitic capacitance.

However, the area in Layer 3 (Ground Layer) beneath the **Balanced BT RF lines** and beneath the BT RF components must be complete ground plane, without any other trace of other signals cutting it. This rule is critical in the balanced part of the BT RF lines (between BRF6300 and the Balun), but is less critical in the un-balanced RF line (between Balun / Filter and Antenna). Refer to .

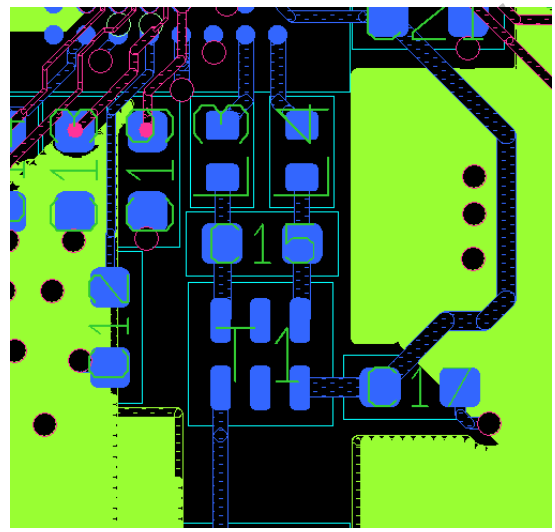


Figure 5 - No ground beneath BT RF path in Layer 2

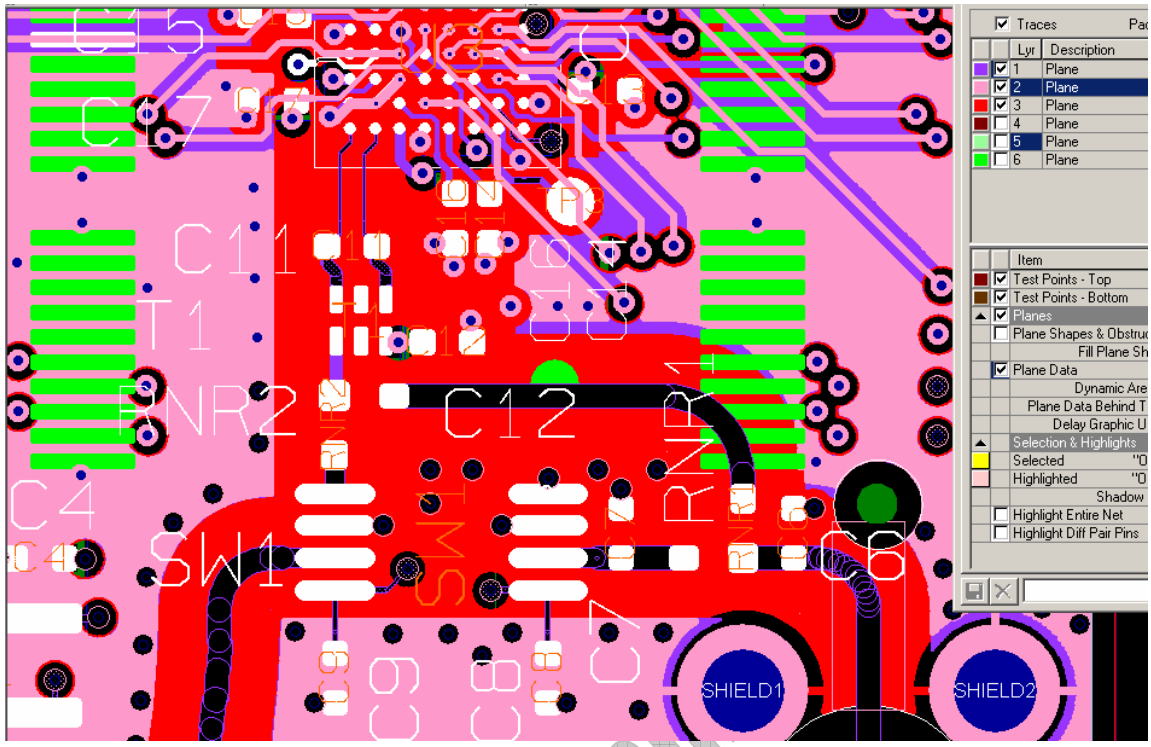


Figure 6 - Ground under RF path on Layer 3, colored red

6.5 RF path isolation

Isolate the BT RF area from the rest of the board by placing BT RF ground traces / area around the BT RF path. This applies to layers 1 and 2. See Figure 10.

Co-planning (50 Ohm) should not only be done with ground layer (layer 3) but also with the top layer surroundings to provide improved sheilding, as shown in the figure below.

The ground area around the RF trace should be strengthened with as many VIAs as possible and VIAs should be places on the ground area plane edge

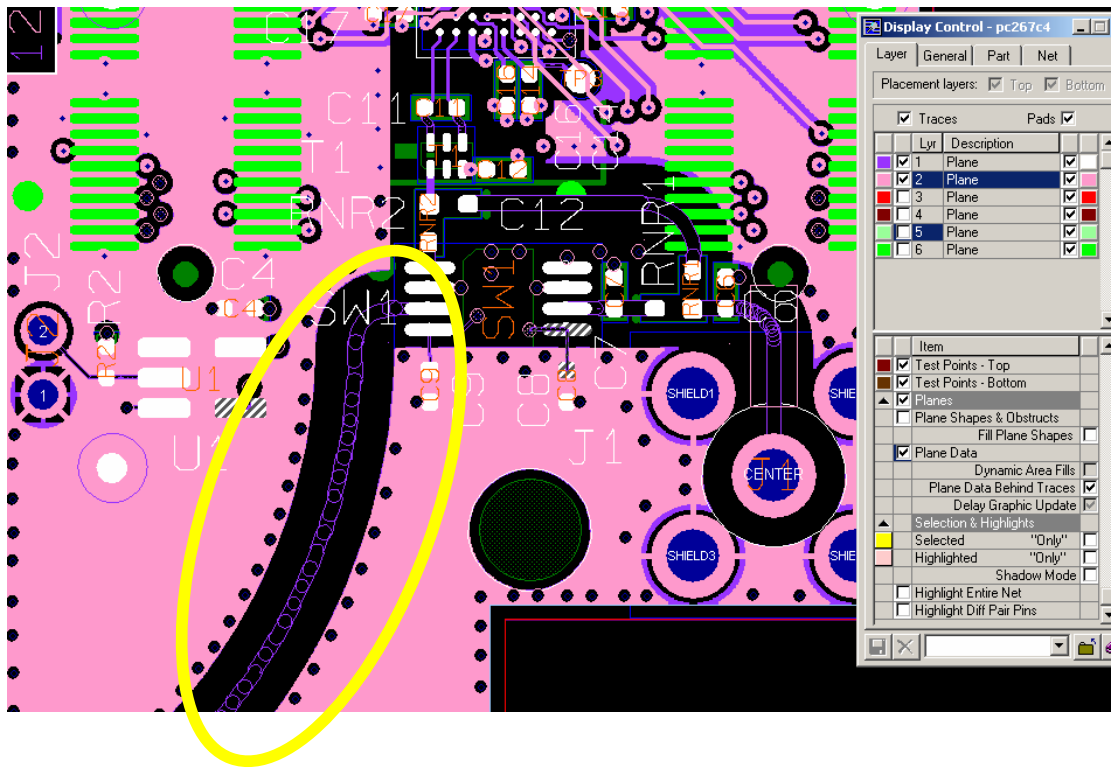
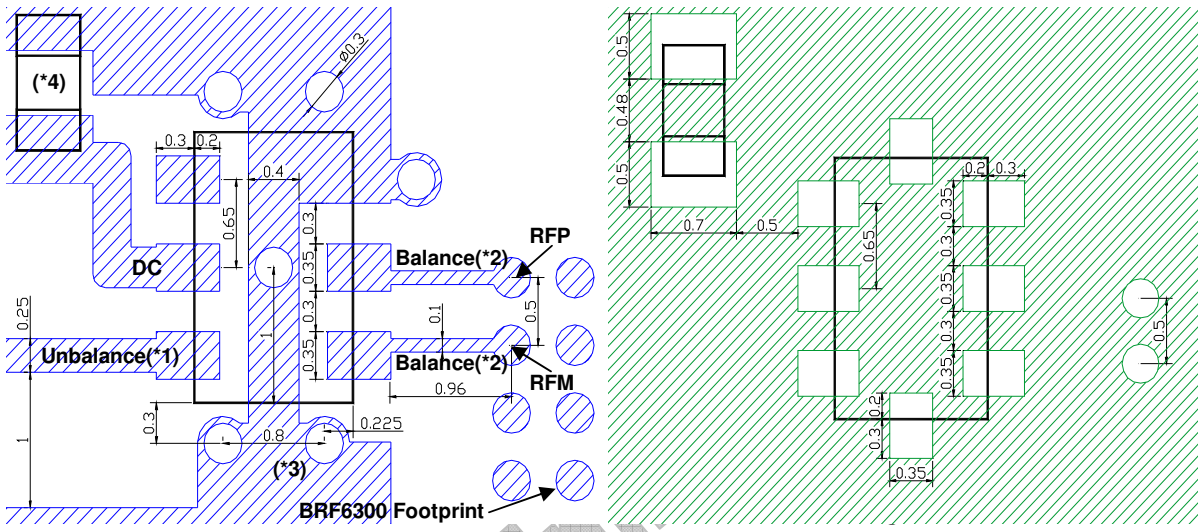


Figure 7 - Isolation of RF path

BALUN / Filter coupling capacitor

Usually BALUN components must use a coupling capacitor to ground, connected to the DC supply pin. The placement of the capacitor has great impact on the frequency response, and must be placed according the **BALUN manufacturer's recommendation**. The ground of the capacitor should be the same reference ground of the other BT RF elements. It should be strengthened with Vias to the Ground Layer. Refer to , Figure and Figure.



*1 - 50 ohm impedance Line
*2 - Assuming tracing inductance is 0.4-0.5nH
*3 - Ground Plane
*4 - Decoupling Capacitor

Figure 8 - Recommended land pattern for DBF81H904 for TI BRF6300

7 Power supply:

The power supply regulator should be placed as close as possible to the BRF6300.

7.1 Power supply traces

The power should be supplied to the BRF6300 device using traces with the following characteristics:

- Wide traces. The typical width should be 10mil.
- As short as possible traces
- The power supply traces should be places in a dedicated layer, and connected with Vias to the power supply pads.
- Coupling capacitor should be placed before the trace that go the different balls of BRF6300
- Whenever possible, the power should be supplied to the different pads on BRF6300 in “Star-like” architecture, and not in series. An even better approach would be to connect by Vias directly to the Power Layer.

7.2 Isolation of power supply

The Bluetooth power supply traces, and the Bluetooth regulator (if exists) should be separated from other devices. Special caution should be taken to separate the power supply from other RF devices, such as GSM PA’s (Power amplifier).

7.3 Power supply distribution

If the same regulator is used to power few devices, they should be connected with “Star-like” architecture: every device should be connected directly to the regulator.

8 Antenna and placement

Although the antenna layout should be based on the antenna's manufacturer recommendations, the following guidelines should be considered.

8.1 Antenna Area

All area beneath the Antenna should be free from Ground, unless specifically recommended by antenna manufacturer. This should be applied for all internal layers.

8.2 RF isolation between Bluetooth and other RF component

When designing the cellular board, caution should be taken when placing the cellular RF components and antenna:

- The Bluetooth and the cellular RF part, along with the antennas (GSM or other) should be placed as far as possible from each other. It is recommended to keep them in the opposite sides of the board.
- The isolation between the Bluetooth antenna and the cellular RF antenna should be as great as possible.
- The two antenna polarizations should be orthogonal (90 deg), for increased isolation.
- It is recommended to use HPF (high pass filter) matching network for the Bluetooth antenna, and LPF (low path filter) matching network for the cellular antenna.

9 Ground Planes and Ground Layer

The BRF6300 device uses 3 different ground signals for analog and for digital.

The digital and analog ground can only be connected together in the internal Ground Layer (Layer 3) and must not be connected together on the Top Layer (later 1).

Ground layout rules must be followed, in order to achieve good RF performance.

9.1 Ground of digital signals

The same ground should be connected between Bluetooth and other digital elements on the board. Connection between two pads creates a current loop. The current passes in the ground plane, in the shortest possible route. The ground should be a plane, as solid as possible. Avoid running traces through the ground plane, to enable short and straight current routes. This applies also to other digital grounds with other elements e.g. Codec.

9.2 Ground for RF devices

Different RF devices such as GSM RF device, or external PA, should be interconnected between ground clusters. In order to minimize interference between the devices, the ground connection of each device should be clustered together before connecting to other devices RF ground.

For example, if the two ground planes are in the same layer, a gap should be created between the grounds, Beneath the Bluetooth to the ground and beneath the other RF device ground.

9.3 Ground clusters

Digital ground pads, Analog ground pads and HV_VSS pads of the BRF6300 must **not** be connected together on the top Layer. The best performance is achieved by using Vias to connect each ground pad to the ground Layer (Layer 3). uVias may be used where usage of Via is not possible. Pads from the same type (digital/analog/HV_VSS) can be connected together (clustered) on the top Layer, and shorted with as many Vias as possible to the internal ground Layer.

Connecting analog ground pads to the digital ground pads, and only then connecting to the internal ground Layer results in parasitic noise, and spurs may appear on the RF, and degrade the device performance; therefore such wiring must be avoided.

The ground pads of BRF6300 (BGA package) are herby described:

VSS – B8, G8, H7, A5, A2	(Digital ground)
VSS_HVM – F4	(Digital high-voltage module Ground)
VSSA – H4, D1	(Analog ground)
VSS_RFIO – G1	(RF Analog ground)
VSSA – G2, F3	(RF Analog ground)

Due to the pads placement in the 6300 and the restrictions described above, only certain pads are able to be clustered to one group. However it is also possible to connect each of these two pads separately to the Ground Layer.

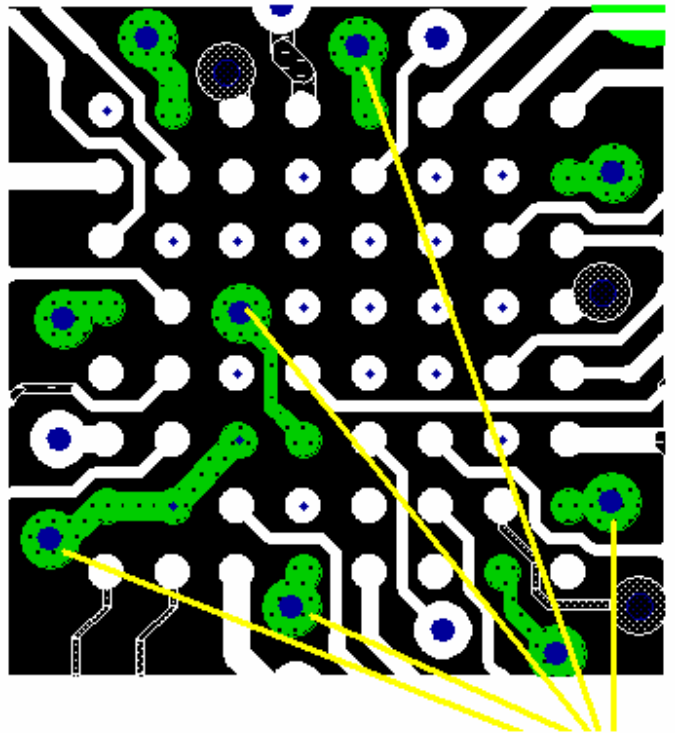


Figure 9 - Ground Clusters – digital and analog ground

9.4 Main Ground Layer (Layer 3)

The digital, analog ground and HV_VSS ground can only be connected together in the internal Ground Layer (Layer 3) and must not be connected together on the Top Layer (layer 1) or Layer 2. The Ground Layer (Layer 3: minimum of 6 mil beneath BRF6300) should be a solid ground plane, beneath the entire Bluetooth area.

In Layer 2 no signals should be routed beneath the RF area so that nothing separates between the RF area and the Ground Layer (refer to). It is extremely important to follow this rule beneath the balanced RF part, from RFIO pads to the BALUN.. It is recommended that any ground area or ground trace should be connected with several Vias to the ground plane (Layer 3).

The Ground Layer (Layer 3: minimum of 6 mil beneath BRF6300) should be a solid ground plane, beneath the entire Bluetooth area.

9.5 Unused layout area

Upon finishing the layout, it is recommended to fill all free area in layers 1 and 2 with ground planes. An exception for this is beneath the BT RF path including the antenna). Where ground filling is appropriate - strengthen the planes to the internal ground plane (Layer 3) with as many vias as possible. Refer to and Figure.

As shown in Figure 3 layers 1 and 2 have been cleaned from ground under and aside the RF path (components and traces).

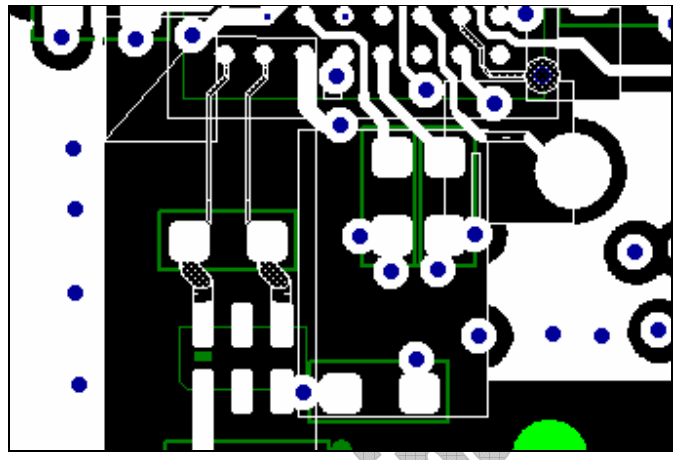


Figure 10 - Unused layout area, and free area beneath RF parts (Layer 1 & 2)

10 Miscellaneous

10.1 Shielding

In an application with more than one RF device, it is recommended to shield the Bluetooth area, to improved immunity to interferers.

10.1.1 Avoid digital lines beneath BRF6300

It is recommended not to route any digital traces of other devices beneath the Bluetooth area on the PCB. If digital traces have to pass beneath the Bluetooth area, ground plane must isolate it from the Bluetooth signals, and from the Bluetooth device. Special care should be taken with other device's fast clock.

10.1.2 IF test points

ANA_TST1 and ANA_TST2 are used to monitor the internal IF for debug purposes. If used on the board, the two signals must be symmetrical and should follow parallel path. (Similar to RF recommendations)

11 PCB example – BRF6300 Reference design

This section demonstrates the implementation of the layout recommendations in TI reference design for the BRF6300. The reference design's PCB is composed of six layers, with the following Vias and Micro-vias:

Micro-Vias between:

- Layer 1 and Layer 2
- Layer 2 and Layer 3
- Layer 4 and Layer 5
- Layer 5 and Layer 6

Buried Vias between:

- Layer 3 and Layer 4

Through Vias

- All layers

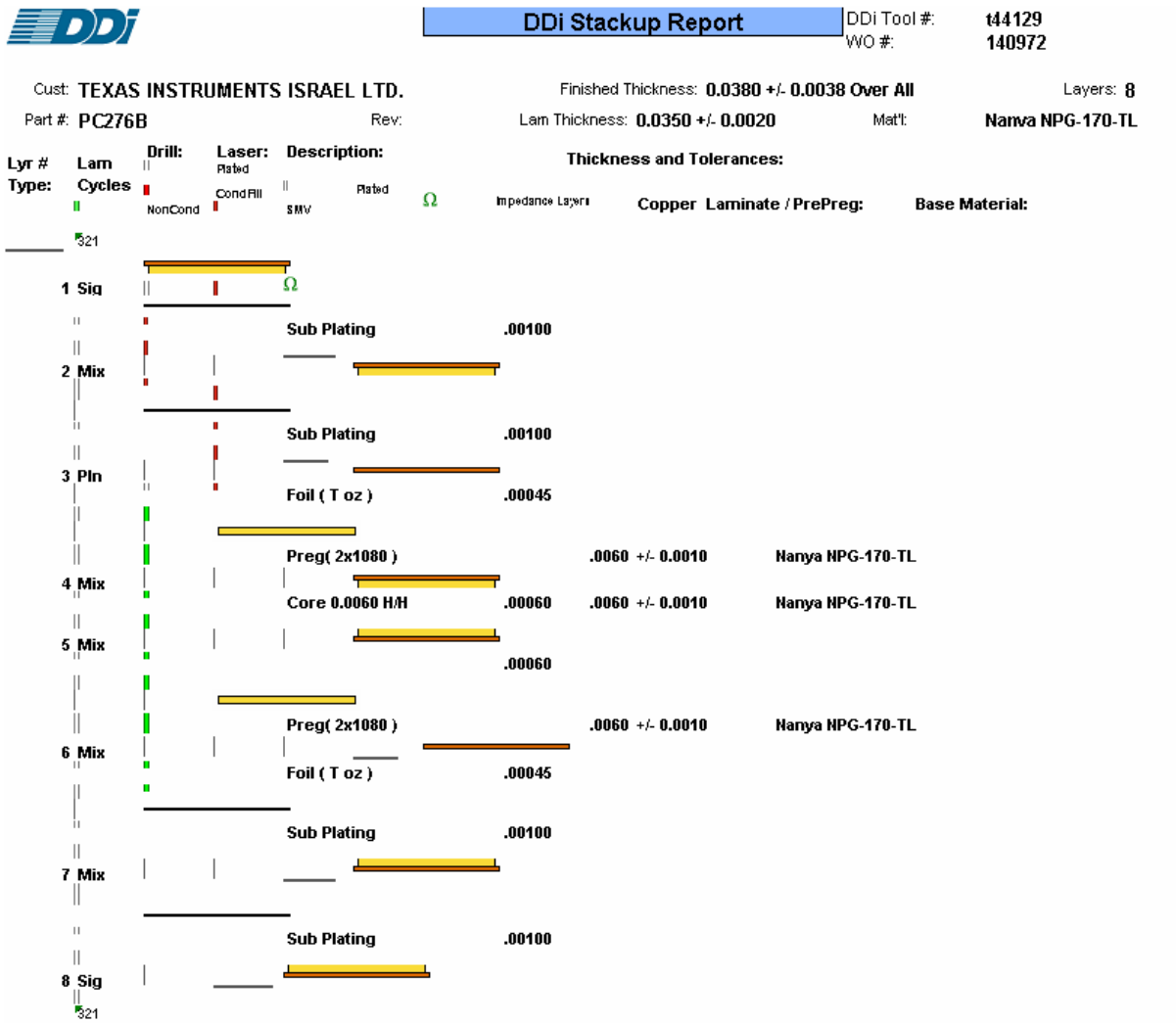


Figure 11 – Example Stack-Up of TI Reference Design for BRF6300

11.1.1 Complete ground Layer

Figure 4 below shows Layer 3 ground plane with RF path. Vias have been set along both sides of the RF path to strengthen the ground between Layer 1 and layer 3.

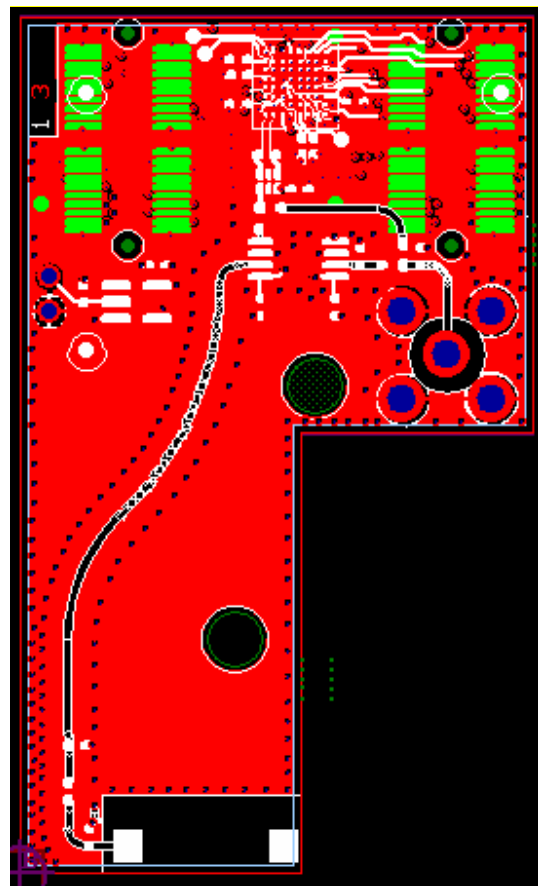


Figure 12: Complete ground layer in Layer 3, particularly, beneath RF area

11.1.2 Ground on Layer 1

Any ground trace on the top level should be connected with Vias to the ground plane (Layer 3). It is recommended to connect areas of ground on the top level with several Vias, for strong and effective ground connection. Refer to Figure 13.

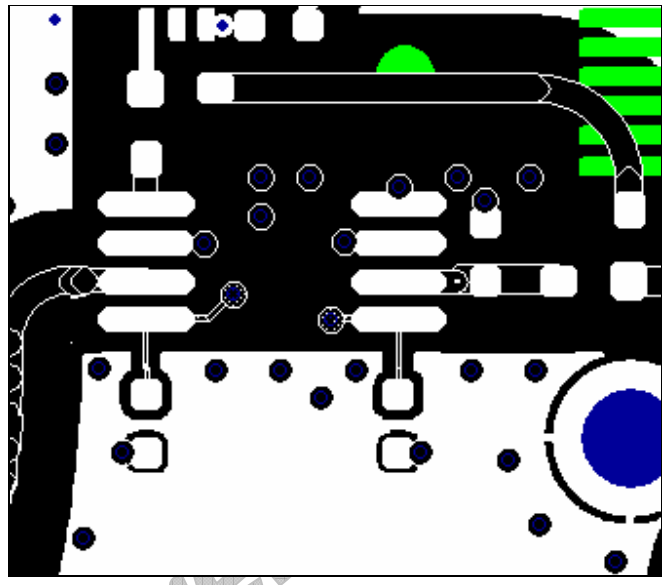


Figure 13: Strengthen closed and semi closed ground area, to internal ground

The following figures depict the placement recommendation and layout recommendation for the different PCB layers.

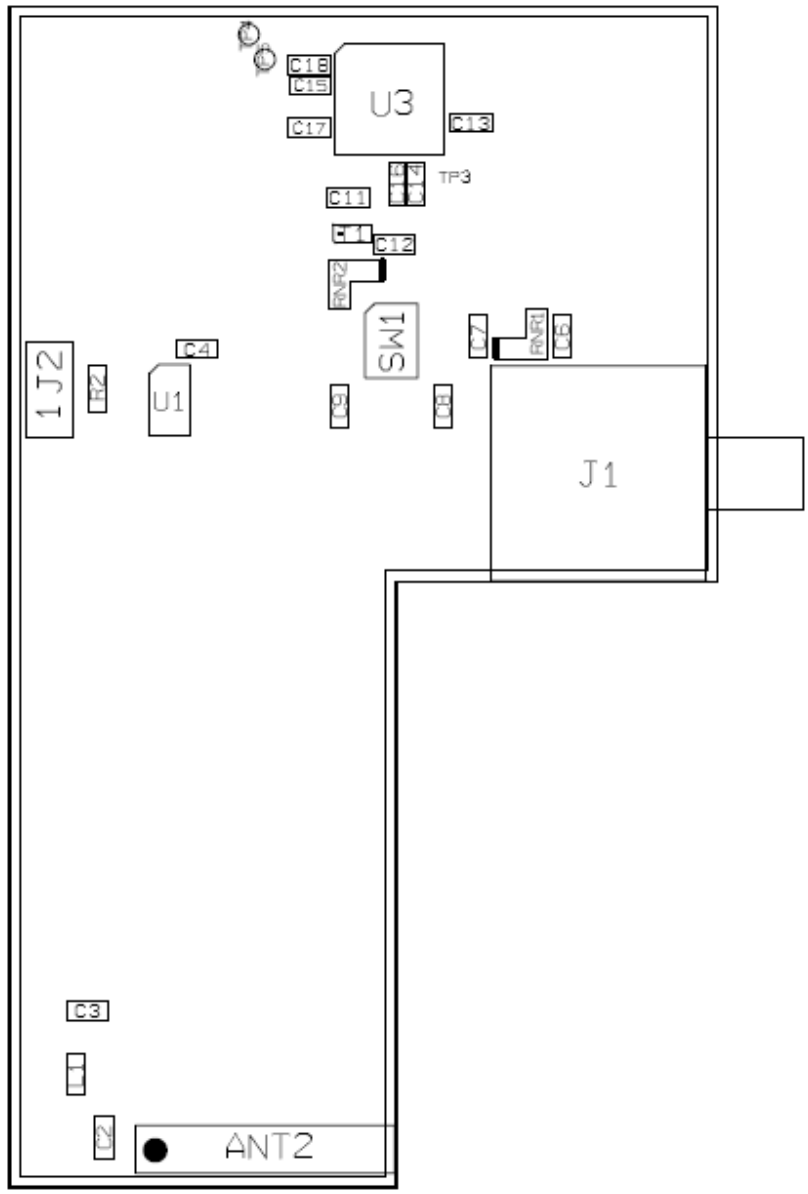


Figure 14: Layout recommendation - placement

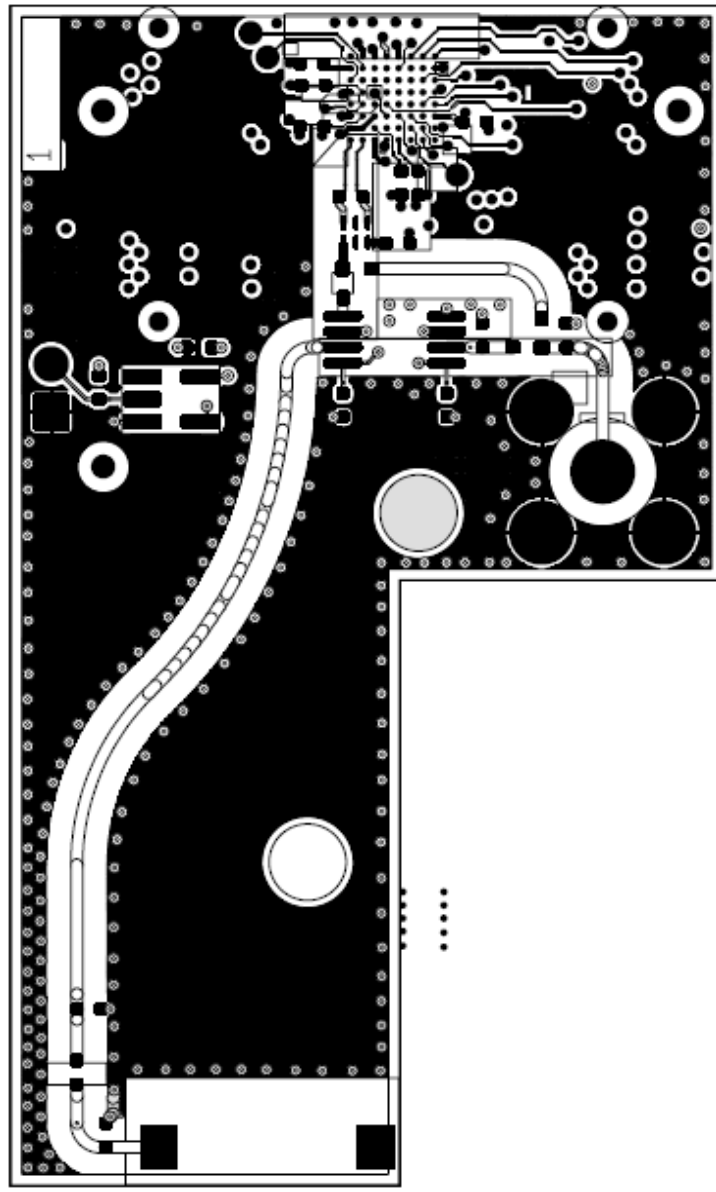


Figure 15: Layout recommendation Layer 1 – components side, Signaling layer

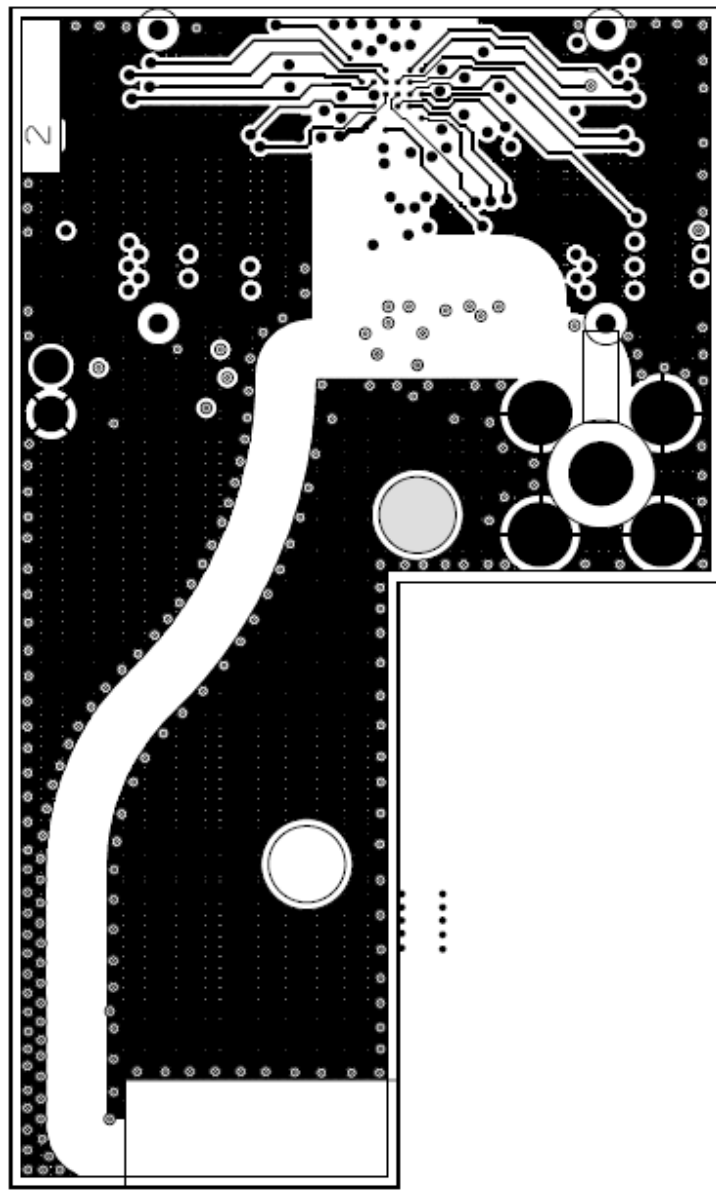


Figure 16: Layout recommendation Layer 2 – INT1, Power supply and signaling

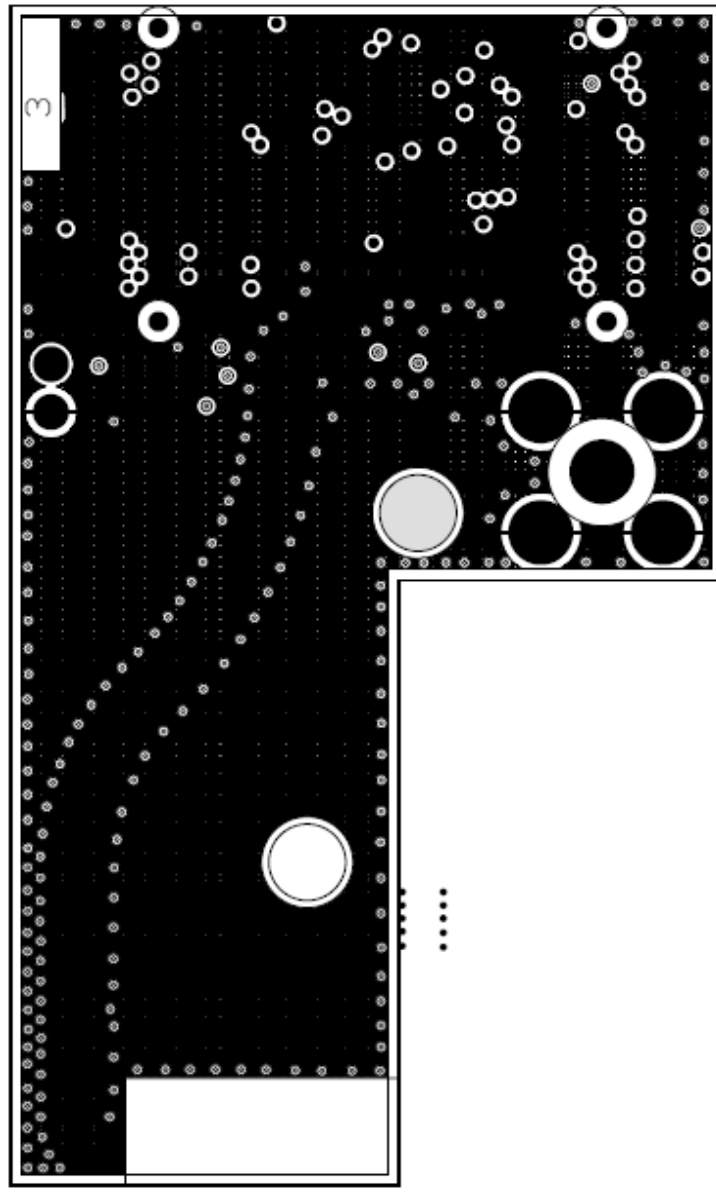


Figure 17: Layout recommendation Layer 3 – INT2, Ground Layer

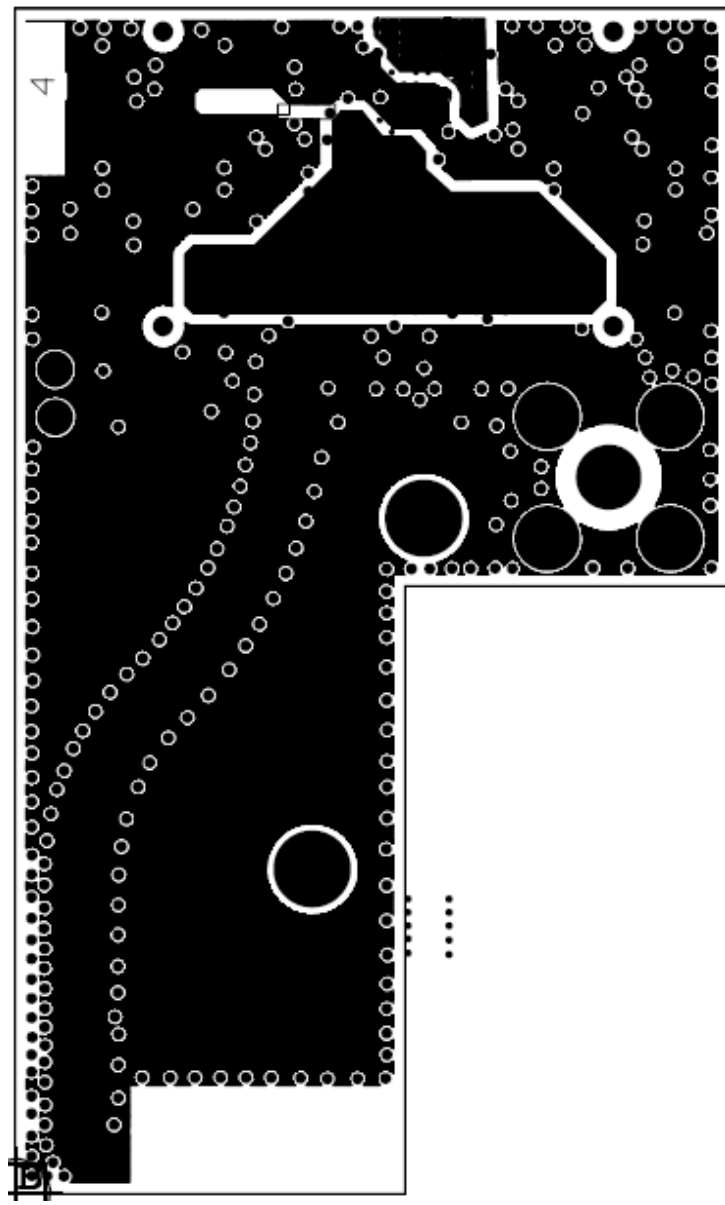


Figure 18: Layout recommendation Layer 4 – INT3, IN/IO Power Layer

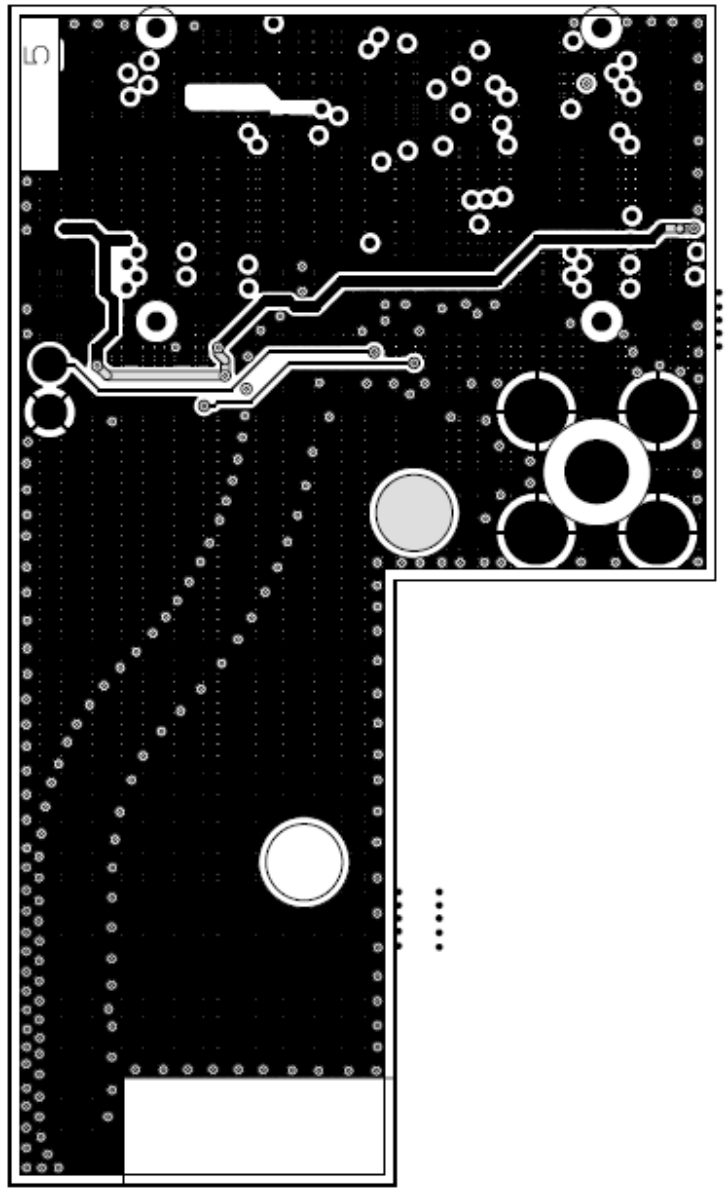


Figure 19: Layout recommendation Layer 5 – Ground and signaling layer

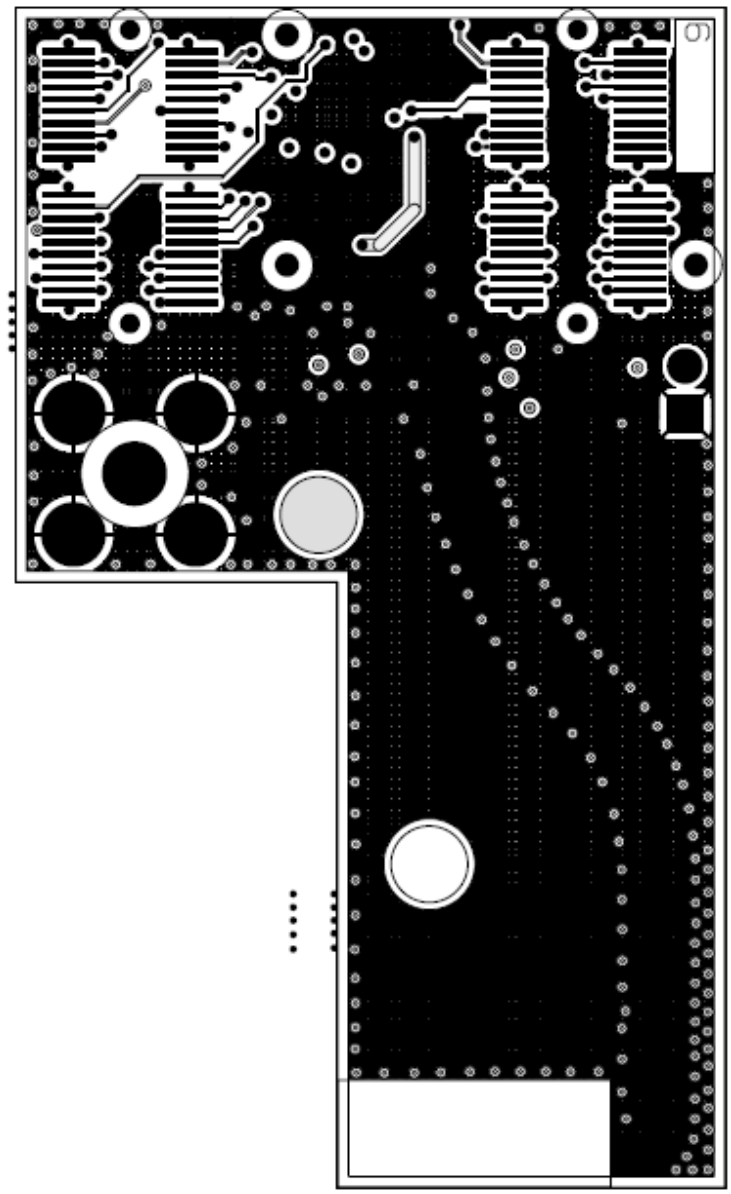


Figure 20: Layout recommendation Layer 6 – Print side, Ground and signaling layer

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