BT-AN-0055 (BRF6300/BRF6350 Clock Sharing, Rev 0.5)

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ABSTRACT

This document describes the clock sharing between the BRF6300 and an external Host or another external device.

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Revision Control

Author Name	Description	Revision	Date	Approved By	Date
Eyal Haberman	Creation	0.1	November 17, 2005		
Dana Ram	Implemented R&D rejections and added scan_sync section	0.2	November 28, 2005		
Dana Ram	Revised Section 1. Added Section 4.3- clock management by Host.	0.3	December 4, 2005		
Dana Ram	Implemented WLAN-related comments	0.4	December 7, 2005		
Dana Ram	Fixed Figure 1. and Figure 3.	0.5	June 20, 2006		

1 Overview

The BRF6300 contains built-in hardware features to share clock resources and to synchronize sleep periods with a host processor on the same PCB. This results in minimum chip count and power consumption.

2 Introduction

In its active modes, the BRF6300 always needs a “fast clock” in order to function. In Deep Sleep (low power mode), the fast clock can be disabled in order to save power. However, the BRF6300 will need the clock enabled periodically to make itself discoverable or check if it is being polled by another device.

The ability to enable and disable the fast clock is therefore needed for correct operation:

If the BRF6300 is using its own on-chip oscillator then this control is done internally. However, where an external fast clock source is used, it is necessary to have some other means of control.

In applications where the BRF6300 has the sole use of a dedicated fast clock oscillator module, the enabling or disabling of the clock is achieved simply by using the EXT_CLK_REQ_OUT signal (Figure 1)

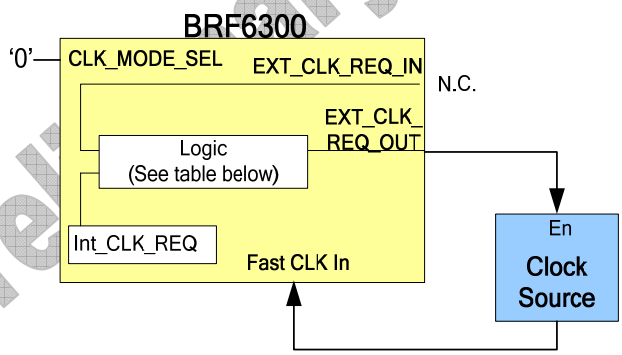


Figure 1: Internal clock control by BRF6300

Note: When working with an external clock source instead of a crystal, the internal oscillator cell must be switched off after power up. This cell can be switched off by using a vendor-specific command:

Send_HCI_VS_Fast_Clock_Configuration 0xFD0E, 0, 5000, 2000, 0, 0xF, 0x0, 0, 250

Wait_HCI_Command_Complete_VS_Fast_Clock_Configuration_Event 5000, any, HCI_VS_Fast_Clock_Configuration, 0x00

The above example is valid for DC-coupling (for AC-coupling refer to BT-SW-0029 document).

For further description of this command refer to BT-SW-0029.

If the application allows, it is usually more cost-effective to use the same fast clock for both the BRF6300 and the host processor (and other devices in the system such WLAN (WL1251) – in this case, either device must be able to enable the clock, when needed.

There are several different methods of achieving this.

The BRF6300 support the following fast clock sharing mechanism:

1. Internal clock-sharing scheme – In this scheme two BRF6300 pins are used to get the clock request from the host and to output the combined clock request (active high/low polarity): EXT_CLK_REQ_IN and EXT_CLK_REQ_OUT. An internal logic (OR/AND) allows the host to send its clock request via the BRF6300, and the BRF6300 outputs the EXT_CLK_REQ_OUT to the clock source (combination of the host clock request and the BRF6300 clock request).

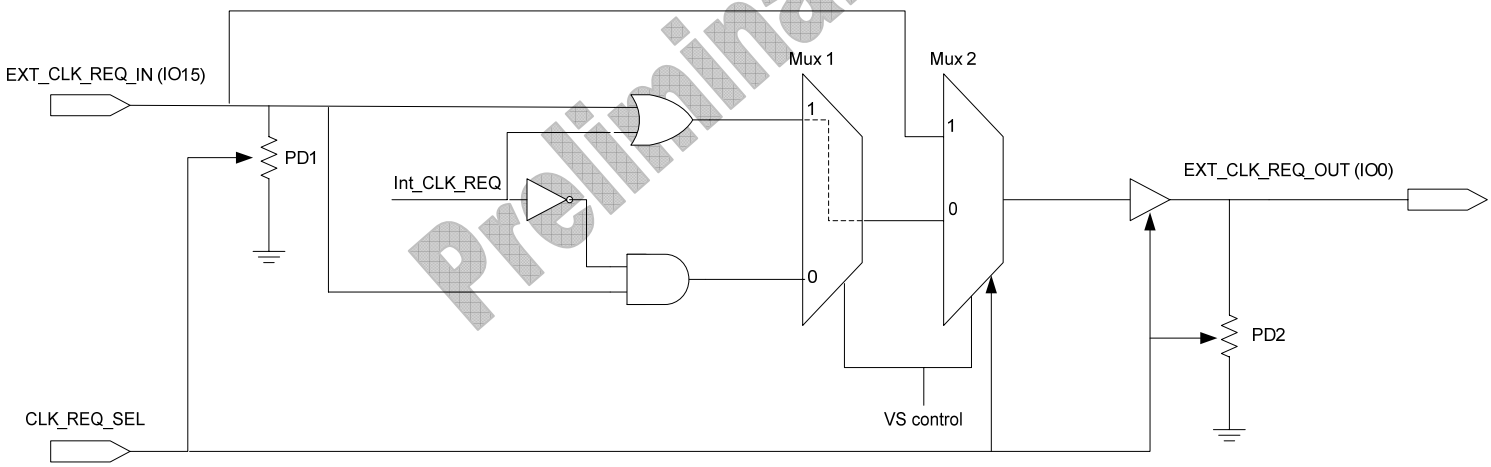
2. External clock-sharing scheme – In this scheme only the EXT_CLK_REQ_OUT is used (the EXT_CLK_REQ_IN is not used and can be used as a general purpose output). In this mode several devices can be wired-OR with the BRF6300 EXT_CLK_REQ_OUT

A third terminal, CLK_MODE_SEL is used to select between these two schemes.

3. External clock management by the Host – In this scheme, the Host has the responsibility for controlling the fast clock module

Note: in both clock-sharing schemes it is required that all the system components using the clock source must be able to receive a clock signal even when not requesting it. This should not cause any excessive power consumption or reliability issues.

The figure below shows the concept of the BRF6300 internal implementation that is used for all three clock-sharing schemes.



1. The CLK_MODE_SEL controls PD1, PD2, output buffer and Mux 2:
   - CLK_MODE_SEL=1 PD1, PD2 are disabled, output buffer = drive,
   - CLK_MODE_SEL =0 PD1, PD2 are enabled, output buffer = dynamic*
   - The default state of MUX2 is also controlled by CLK_MODE_SEL : CLK_MODE_SEL =1 →INPUT1 ; CLK_MODE_SEL = 0 →INPUT0
2. The dotted line shows the default (during shut down and power up, until VS command is sent by the host) – Mux 1 outputs INPUT1 by default.
3. The state of Mux1 and Mux2, in active mode, can be controlled by a VS command

* Dynamic= When the driving signal (EXT_CLK_REQ_OUT) is H , the related pull down (PD2) is disabled
When the driving signal (EXT_CLK_REQ_OUT) is L , the related pull down (PD2) is enabled

Figure 2: BRF6300 Internal Logic for Clock Sharing Scheme

3 Internal Clock Sharing Scheme (CLK_MODE_SEL=1)

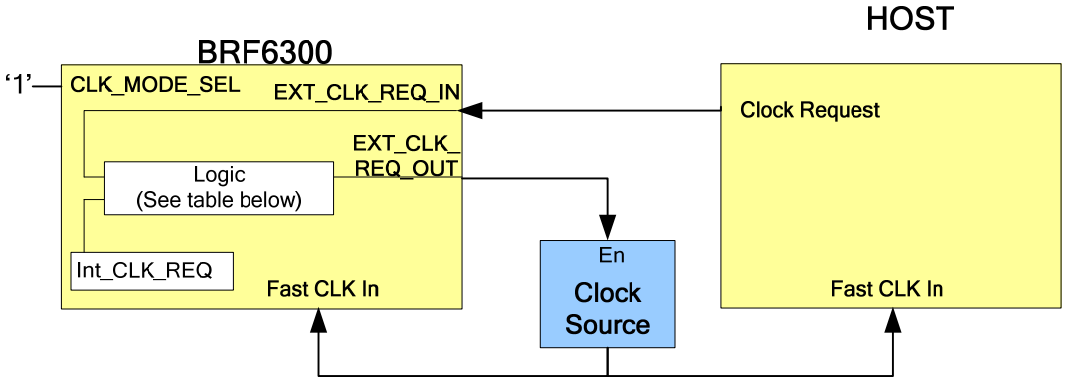


Figure 3 : Internal Clock Sharing Scheme

In this mode the clock sharing scheme is implemented by using the BRF6300 internal logic.

The Host clock request signal is input to the BRF6300 EXT_CLK_REQ_IN terminal and combined internally with the BRF6300 internal Clock Request signal. The output of the logic generates the EXT_CLK_REQ_OUT, which is used to enable the clock source.

The internal logic may be OR or AND. In the case of OR logic, the clock request signal's logic should be active high, and for AND logic the clock request signal's logic should be active low (refer to Figure 2).

NOTE: when the system consists of other external devices such WLAN (WL1251/WL1253) or a DTV device, this configuration is not to be used. The configuration described in Section 4 should be used instead.

3.1 Shutdown Mode

During shutdown the pull downs on EXT_CLK_REQ_IN and EXT_CLK_REQ_OUT are disabled, and the output buffer is driving according to the level of EXT_CLK_REQ_IN.

The Host terminal, which drives EXT_CLK_REQ_IN, can drive high or low, or can be at high-Z with pull up or with pull down. The EXT_CLK_REQ_OUT will drive high or low, according to the state of EXT_CLK_REQ_IN.

This can be referred to as if there is a short between the EXT_CLK_REQ_IN and EXT_CLK_REQ_IN (refer to Figure 1)

Table 1. Internal Clock Sharing Scheme During Shutdown

BRF6300 Mode	Clock sharing scheme	BRF6300 clock (int)	EXT_CLK_ REQ_IN	EXT_CLK_ REQ_OUT	Notes
Shut down	Internal clock sharing (CLK_MODE_SEL = 1)	Clk not req	'0'	'0'	No internal PDs are enabled in this mode
		Clk not req	'1'	'1'	

3.2 Active (or Deep-Sleep) Mode

The short between the EXT_CLK_REQ_IN and EXT_CLK_REQ_OUT that was described in the previous section will remain until a VS command is sent to route the EXT_CLK_REQ_IN to the internal logic (internal OR or internal AND).

Note: When using this scheme the Host must send the VS command that will soon be described after exiting shutdown mode.

The polarity of the clock request (active-high or active-low) determines whether the internal OR should be used (active high) or internal AND should be used (active low).

3.2.1 Active-High Polarity

When the polarity of the clock request is active-high (‘1’ means the clock is requested), the following VS command should be sent by the Host:

Send_HCI_VS_Configure_Clock_Sharing 0xFD0A, 1, 1, 0, 0x02, 0x02

Wait_HCI_Command_Complete_VS_Configure_Clock_Sharing_Event 5000, any, HCI_VS_Configure_Clock_Sharing, 0x00

Table 2. depicts all the different combination for the BRF6300 and the external device clock requests and the resulting clock request at the output of the BRF6300 (EXT_XLK_REQ_OUT) for the internal clock sharing scheme with active-high polarity.

Table 2. **Active state mode while in Active-High Polarity**

BRF6300 Mode	Clock sharing scheme	BRF6300 clock (int)	EXT_CLK_ REQ_IN	EXT_CLK_ REQ_OUT	Notes
Active or Deep-Sleep	Internal clock sharing (CLK_MODE_SEL = ‘1’)	Clk not req	’0’	’0’	No internal PDs are enabled in this mode.
		Clk not req	‘1’	‘1’	
		Clk req	’0’	‘1’	
		Clk req	‘1’	‘1’	

3.2.2 Active-Low Polarity

When the polarity of the clock request is active-low (‘0’ means the clock is requested), the following VS command should be sent by the Host:

Send_HCI_VS_Configure_Clock_Sharing 0xFD0A, 1, 0, 0, 0x02, 0x02

Wait_HCI_Command_Complete_VS_Configure_Clock_Sharing_Event 5000, any, HCI_VS_Configure_Clock_Sharing, 0x00

Table 3. depicts all the different combination for the BRF6300 and the external device clock requests and the resulting clock request at the output of the BRF6300 (EXT_XLK_REQ_OUT) for the internal clock sharing scheme with active-low polarity.

Table 3. **Active High mode while in Active-Low Polarity**

BRF6300 Mode	Clock sharing scheme	BRF6300 clock (int)	EXT_CLK_ REQ_IN	EXT_CLK_ REQ_OUT	Notes

Active or Deep-Sleep	Internal clock sharing (CLK_MODE_SEL = ‘1’)	Clk not req	’0’	’0’	No internal PDs are enabled in this mode.
		Clk not req	‘1’	‘1’	
		Clk req	’0’	’0’	
		Clk req	‘1’	’0’	

4 External Clock Sharing Scheme (CLK_MODE_SEL=0)

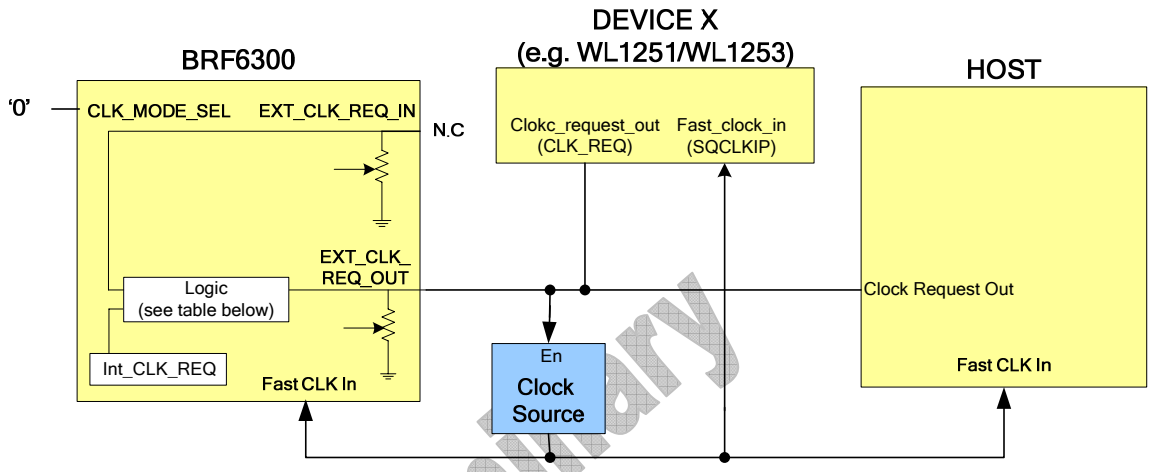


Figure 4 : External Clock Sharing Scheme

In this mode the external devices’ clock requests are not input into the BRF6300. All the clock requests of the system are wired-OR with the BRF6300 EXT_CLK_REQ_OUT pin. Whenever a clock is required by the BRF6300 or an external device, it asserts to high its clock request output pin in order to enable the clock source.

Note: Applying this external clock sharing scheme requires all the devices in the system to drive Hi-Z to the clock-request terminal when the clock is not required.

In this mode the EXT_CLK_REQ_IN *should not* be driven as an input by an external device. Since if EXT_CLK_REQ_IN is driving high, the output buffer drives high (this would be interpreted wrongly as a clock request). Moreover there will be a current drawn from the pull down on EXT_CLK_REQ_IN. Therefore, as stated earlier, ***when CLK_MODE_SEL=0, EXT_CLK_REQ_IN should be used only as an output***.

If any of the above requirements cannot be met then an external OR gate can be used to OR between all the clock requests of the different devices and then input to the clock source enable pin.

4.1 Shutdown Mode

During shutdown the pull down on EXT_CLK_REQ_IN is enabled and the EXT_CLK_REQ_OUT signal is in high-z with the pull down enabled. (The latter is conditioned on the EXT_CLK_REQ_IN being not connected – as recommended).

Upon leaving shut down mode and when requesting a clock, the BRF6300 will drive high the EXT_CLK_REQ_OUT pin and disable its pull down.

Table 4. depicts all the different combination for the BRF6300 and the external device clock requests and the resulting clock request at the output of the BRF6300 (EXT_XLK_REQ_OUT) for the external clock sharing scheme during shutdown.

Table 4. Shutdown mode while in External Clock Sharing Scheme

BRF6300 Mode	Clock sharing scheme	BRF6300 clock (int)	EXT_CLK_REQ_IN	EXT_CLK_REQ_OUT	Notes
Shut down	External Clock Sharing (CLK_MODE_SEL = '0')	Clk not req	N/C + PD	Hi-Z + PD	
		Clk not req	'1' + PD	'1'	Not recommended

4.2 Active (or Deep-Sleep) Mode

Table 5.depicts all the different combination for the BRF6300 and the external device clock requests and the resulting clock request at the output of the BRF6300 (EXT_CLK_REQ_OUT) for the external clock sharing scheme while active.

Note: *In the external clock sharing scheme there is no need for the host to send a VS command. This scheme is enabled by default.*

However in the scheme active-low logic is not applicable.

Table 5. Active mode while in External Clock Sharing Scheme

BRF6300 Mode	Clock sharing scheme	BRF6300 clock (int)	EXT_CLK_REQ_IN	EXT_CLK_REQ_OUT	Notes
Active or Deep - Sleep	External Clock Sharing (CLK_MODE_SEL = '0')	Clk not req	N/C + PD	Hi-Z + PD	EXT_CLK_REQ_IN can be used as GP output.
		Clk req	N/C + PD	'1'	

5 External Clock Management by the Host

Another possibility is that Host has the responsibility for controlling the fast clock module.

The logic state of CLK_MODE_SEL will determine the logic state of EXT_CLK_REQ_OUT when the BRF6300 is in shutdown or when not requesting a clock. According to the Host requirements on its clock_request_in pin, the logic state of CLK_MODE_SEL should be determined.

The following two sections explain this in detail.

5.1 CLK_MODE_SEL = '0'

This scheme shown in Figure 5 presents a scheme in which the Host has the responsibility for controlling the fast clock module and CLK_MODE_SEL='0'.

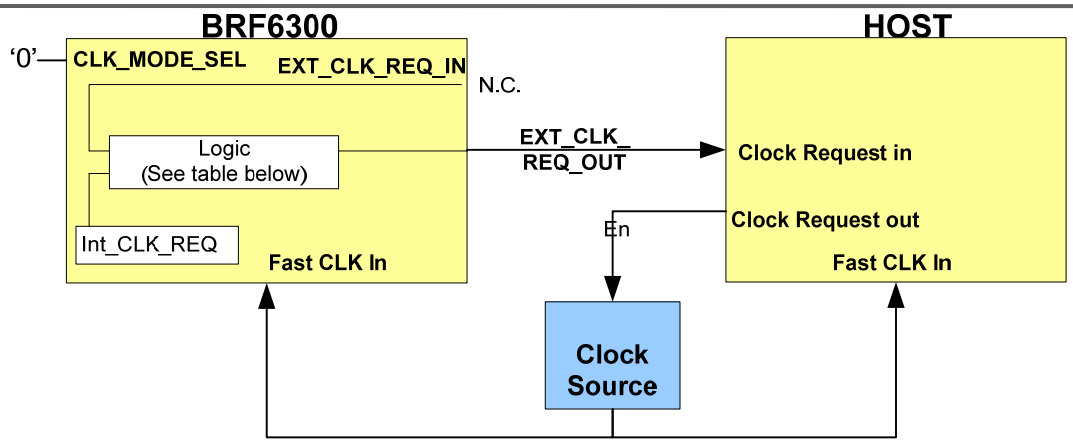


Figure 5 : External clock management by host, CLK_MODE_SEL='0'

In this scheme, when the BRF6300 is in shutdown or when not requiring a clock, EXT_CLK_REQ_OUT= Hi-Z.

5.2 CLK_MODE_SEL = '1'

This scheme shown in Figure 6 presents a scheme in which the Host has the responsibility for controlling the fast clock module and CLK_MODE_SEL='1'.

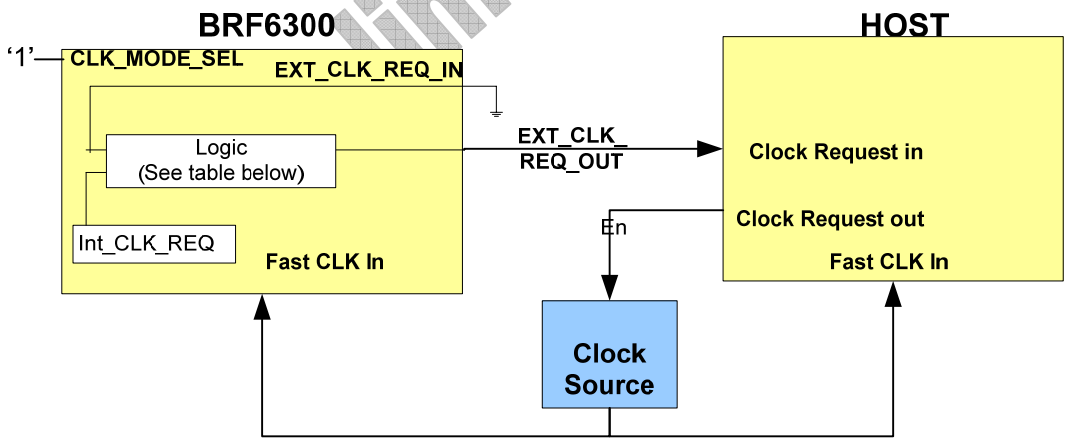


Figure 6 : External clock management by host, CLK_MODE_SEL='1'

In this scheme, when the BRF6300 is in shutdown or when not requiring a clock, EXT_CLK_REQ_OUT= '0'.

5.3 Hardware and Software Host Requirements

In this case, the host has the responsibility for controlling the fast clock module. To allow the host to manage the clock correctly, the EXT_CLK_REQ_OUT signal from the BRF6300 is connected to an I/O on the host. Since the host is controlling the NSHUT_DOWN signal to the BRF6300, it is aware of when the BRF6300 is in Shut-down, and can ignore the false clock request during this time. When the BRF6300 is not Shut-down, however, the host can detect that the BRF6300 requires the clock, and enable it.

This method requires that the host (if asleep) must wake up whenever BRF6300 requires the clock.

The efficiency of this method may be improved by synchronizing the BRF6300 wake-up to the periodic wake-up of the host. This method is described in the following section.

NOTE: Use of this method requires an interrupt software routine in Host that may require substantial software changes and/or increased cost on the Host side.

5.3.1 Host Requirements:

1. The GPIO PIN connected to EXT_CLK_REQ_OUT must be interruptible. The interrupt will force the Host to wake-up (if asleep) if the BRF6300 needs the clock for scanning.
2. The interrupt can be triggered either by rising edge or by level since EXT_BT_CLK_REQ is active high.
3. The GPIO can be accessed by the SW running on the host side to read its value (i.e., to know whether it is HIGH or LOW).
4. By default the clock should be supplied to the BRF6300 15ms after the assertion of the EXT_BT_CLK_REQ. This interval can be changed by a VS command HCI_VS_Set_Settling_Time_Island2.

5.3.2 Host software requirements:

1. On initialization - configure the GPIO to be an interrupt input triggered by rising edge.
2. Create an empty interrupt handler to avoid any other use of this interrupt by the SW on the Host side.
3. Change HCILL code as follows: on the "Enter Sleep" function (or "can I go to sleep" equivalent function), before checking whether the HCILL state is ASLEEP, read the GPIO value and if the GPIO is HIGH, then do not allow going to sleep.
4. The SW is not required to control the CLOCK_ENABLE signal. This should be controlled by the system's hardware. It will go to HIGH (requesting the CLOCK) immediately as a result of the BRF clock request's interrupt (or by other interrupt in the system that require the clock).

6 The HCI_VS_Configure_Clock_Sharing Command

In active mode, the host can determine the following parameters using this VS command:

1. Which logic to use (OR for active high clock request, AND for active low clock request)
2. Selects Mux 2 input 0, to transfer the internal logic to EXT_CLK_REQ_OUT
3. EXT_CLK_REQ_OUT mode (high-Z or output)
4. Disabling or enabling of the pull downs

Command	Opcode	Command Parameters	Return Parameters
HCI_VS_Configure_Clock_Sharing	0xFD0A	Internal (OR/AND) Enable Polarity Output mode (Tri-state/Output/wired) Input pull enable Output pull enable	status

Description:
This command **configures** the selected clock sharing mode.
Note that prior to sending this command the clock sharing configuration is determined by external CLK_SEL pin.

Default values:
Default behavior is determined by the CLK_SEL pin. The below values are the register defaults which only take place when sending this command.

Internal (OR/AND) Enable =1 (Internal OR is configured).
Polarity =1
Tri-state output Enable =0 (Output mode is selected)
Input pull enable =1
Output pull enable =1

Command Parameters:

Internal (OR/AND) Enable	Size: 1 Byte
Value	**Parameter Description**
0x0	Internal (OR/AND*) disabled
0x1	Internal (OR/AND*) enabled

* OR/AND is selected according to the configured polarity

Polarity:	Size: 1 Byte
Value	**Parameter Description**
0x0	Active low polarity of the output PIN (EXT_CLK_REQ_OUT)
0x1	Active high polarity of the output PIN (EXT_CLK_REQ_OUT)

Output Mode	Size: 1 Byte
Value	**Parameter Description**
0x0	Output mode is determined according to CLK_MODE_SEL pin. CLK_MODE_SEL=1 -the output is always driven. CLK_MODE_SEL = 0 - the output is Hi-Z when clock is not required and H when clock is requested.
0x1	**Reserved**.
0x2	Output always drives
0x3	Clock is required→ output is H , Clock is not required → output is Hi-Z **Applicable for active-high polarity and wired-OR scheme**
0x4	**Reserved**.

Input pull Enable	Size: 1 Bytes

Value	Parameter Description
0x0	Input pull (on IO15) is statically disabled
0x1	Input pull (on IO15) is statically enabled
0x2	According to CLK_MODE_SEL: CLK_MODE_SEL = '1' → pull down is disabled CLK_MODE_SEL = '0' → pull down is enabled

Output pull Enable	Size: 1 Bytes
Value	**Parameter Description**
0x0	Output pull (on IO0) is statically disabled
0x1	Output pull (on IO0) is statically enabled
0x2	According to CLK_MODE_SEL: CLK_MODE_SEL = '1' → pull down is disabled CLK_MODE_SEL = '0' → pull down is enabled

Return Parameters:

Status:	Size: 1 Byte
Value	Parameter Description
0x00	Command Succeeded.
0x01-0xFF	Command failed. See error codes table in BT-SW-0029

Events Generated:
Command Complete Event

7 Reference Documents

Document	Reference
BRF6300 Product Review	BT-DS-0023
BRF3000 Scan Sync to Host AN	BT-AN-0056
BRF6300 HCI VS command Rev	BT-SW-0029

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