Texas Instruments

Design Guidelines
SWRA128–February 2007

BRF6300 PCB Design Guidelines

The BRF6300 is a radio frequency (RF) device, targeted to operate on a cellular board. When designing a printed circuit board (PCB) with the BRF6300 device, design rules and layout guidelines must be taken into consideration.

This document describes the guidelines for designing the PCB, including device placement, layout rules and a reflow profile for soldering the device.

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1 Overview

This document discusses the PCB design guidelines, placement and layout guidelines for the BRF6300. Reflow soldering profile recommendations for the BRF6300 device are also presented.

2 Introduction

The following sections of this document describe the guidelines for designing the PCB, including device and circuit placement, layout rules and the reflow profile for soldering the device.

This document complements the BRF6300 data sheet, and is not intended to replace it. It is strongly recommended to use the full range of product data sheet and application notes for a complete system design.

It is also strongly recommended that users follow the design rules presented in this document in order to achieve performance similar to that measured in Texas Instruments lab and test environments. These guidelines are based on previous experience with the BRF6300 on a cellular board. Following these rules will help users to avoid mistakes that may result in unnecessary spins to the PCB, and as a result, generate longer time to market.

For any questions or issues that arise during the layout process that contradict these guidelines, please consult your local TI representative.

3 PCB and Stack-Up

The recommendations given in this document reference a six-layer PCB with the BRF6300 based on a standard flame-retardant 4 (FR4) board, the technology commonly used in cellular applications.

Included in these six layers should be at least two signal layers, one ground layer and one power layer. It is recommended that Layer 3 be the ground layer, for a stable RF reference ground. The reference ground should be about 8 mils below the RF path (for BGA packages).

A multilayer PCB with more than six layers can be used, though additional layers are not required. A PCB with four layers can be used as well.

When using the BRF6300 wafer chip-scale package (WCSP), microvias must be used in order to enable connection of traces to each pad. microvias should also be used between Layers 2 and 3 to allow routing of the device.

The use of microvias has many advantages; most importantly, because microvias are smaller than through-hole vias, they add flexibility to the design, shorten lead lengths, and enable smaller footprints as well as more effective connection between traces in different layers.

The reference design (as shown in Figure 1 as well as the other illustrations) is based on a board with through-hole vias connecting internal layers, and microvias connecting two external layers.

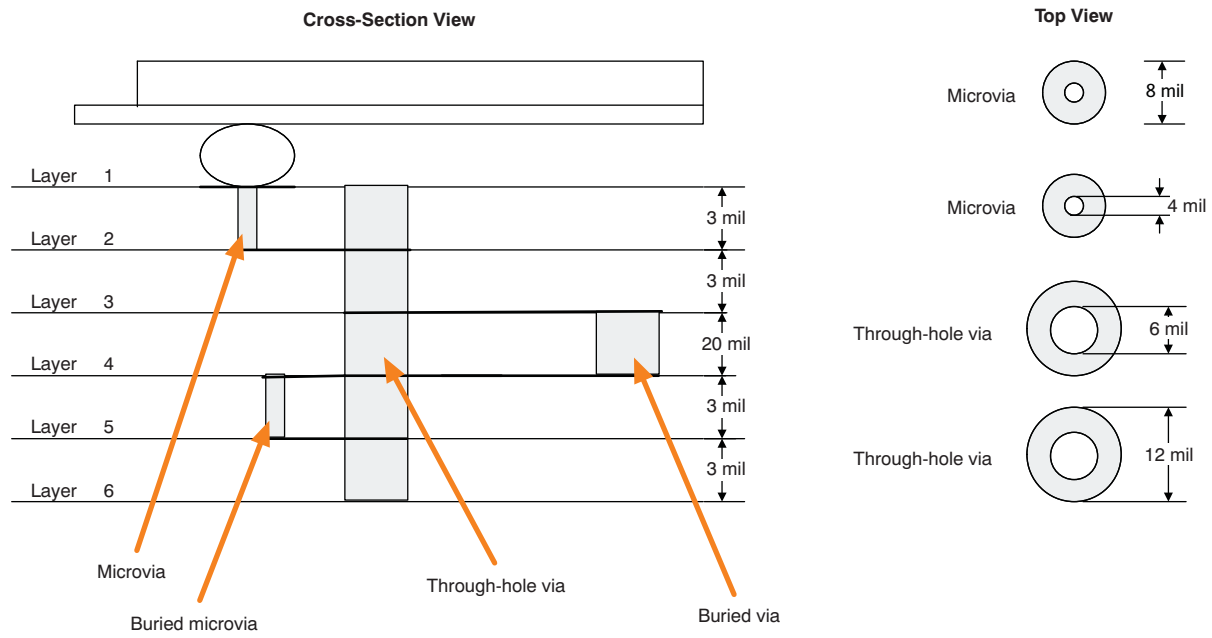


Figure 1. Via Structure of Reference Design

4 Placement of External Components

Place the external components near the BRF6300. Traces should be as short as possible from the BRF6300 pads to the pads of the external components (refer to Figure 2).

4.1 LDO Capacitors

Place the capacitors connected to the LDO outputs as close as possible to the BRF6300. The trace connecting the capacitors to the device should be as short as possible; both capacitor paths should also use wide traces, if possible. Capacitor ground connections should be strengthened with vias. These vias should be on the ground pad or next to the ground pad of the capacitor, and connected to the internal ground plane (as noted earlier, for best performance, this plane should be Layer 3). If it is not possible or practical to apply these guidelines to all capacitors, follow these priorities:

1. OSC_LDO_OUT
2. ANA_LDO_OUT, RFIO_LDO_OUT
3. BB_LDO_OUT, FLDO_OUT

Note that the vias of the capacitors below should all be connected to the ground plane on Layer 3; see Figure 2.

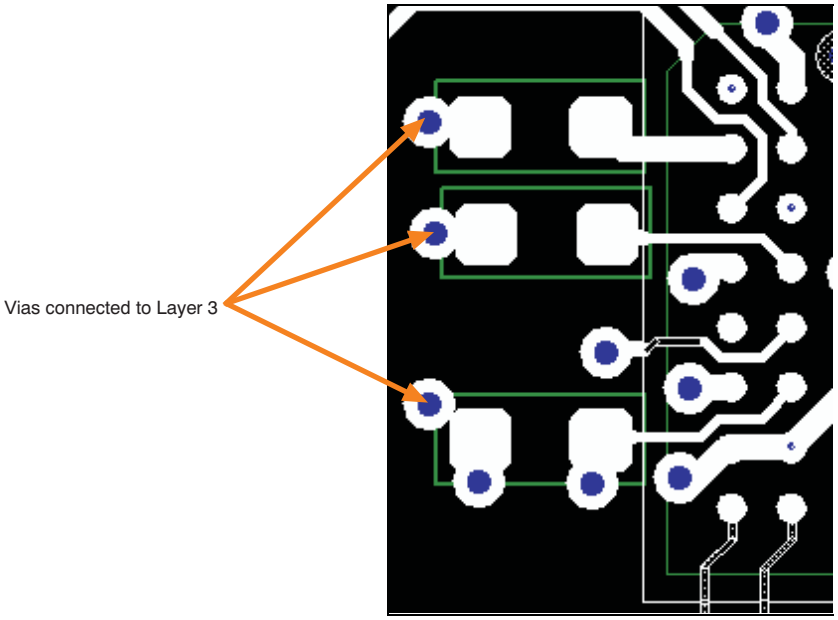


Figure 2. Capacitors Close to BRF6300 with Strong Ground

5 Clocks

Clock signals significantly influence the RF performance of the device, and are susceptible to noise from a variety of sources. Clock signals can also generate interference to other signals.

As a general guideline, clock signals should be as short as possible.

5.1 Clock Signal Isolation

Separate the clock signals supplied to the device from other signals, using grounded strips. The fast clock should not have traces that are in close proximity to each other, and traces should not be routed in parallel to other signals.

5.2 Clock Routing

Use care to avoid cutting the ground plane beneath the RF part with the clock trace.

Figure 3 shows the fast clock routed incorrectly, crossing the whole area of the BRF6300 device above and passing very close to the slow clock. This type of error should be avoided. When routing a signal and it is required to route the path over a digital clock signal, it is recommended to lay out the route at a 90-degree angle in order to minimize coupling.

As a general layout recommendation, route adjacent layers in opposite directions; that is, lay out one layer with vertical routing and the other layer with horizontal routing for minimal interference.

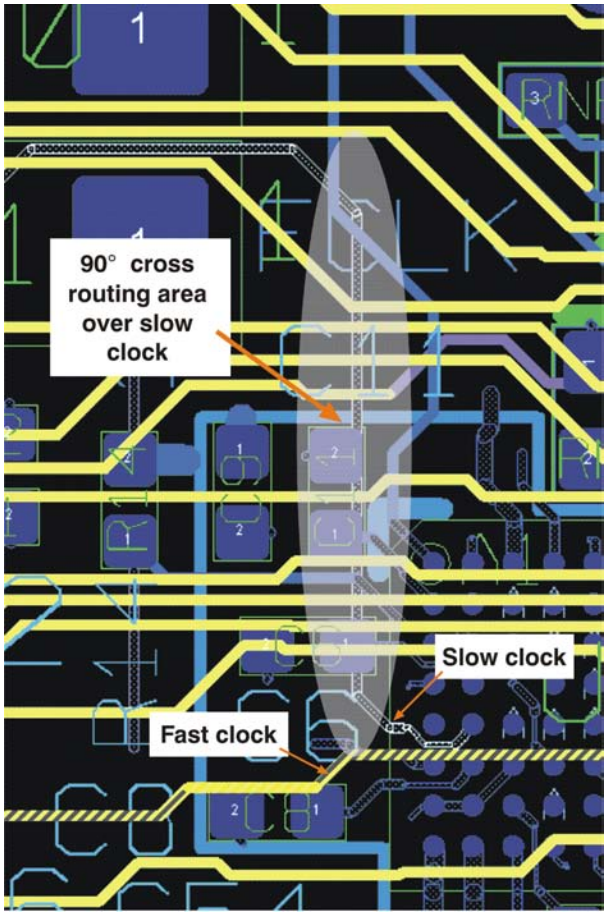


Figure 3. Example of Incorrect Fast Clock Routing

5.3 Slow Clock and Digital Clock Signals

The following signals are digital clock signals:

- Slow Clock
- Audio Clock (AUD_CLK)
- I²C™ Clock (SCL)
- SDIO / SPI Clock (IO7)

Slow clock signals and the digital clocks signals described here are sources of noise. Special care should be taken to avoid laying the traces next to sensitive signals such as the RF path, OSC_LDO, RFIO_LDO, and so forth.

Whenever feasible, the traces of these signals should be as short as possible; be sure to maintain clearance around them.

5.3.1 Crystal as the Clock Source

When using a crystal as the clock source, the parasitic characteristics of the clock trace typically influence the oscillation. Position the crystal as close as possible to the BRF6300; keep traces as short as possible. Traces that are too wide can lead to excessive capacitance, while traces that are too narrow may generate parasitic inductance of the clock trace. Trace width of about 10 mils should be used for short clock traces.

6 Bluetooth® RF Design

When designing the RF path for a Bluetooth (BT) application, these placement and layout rules must be followed.

6.1 RF Path

Lay out the BT RF path on the top layer only. Keep traces as short as possible on the unbalanced section. Keep the entire BT RF path in straight line. See Figure 4.

The vertical traces (x2) connecting to the capacitors have been set to a specific length, simulating the required impedance in order to acquire the required matching.

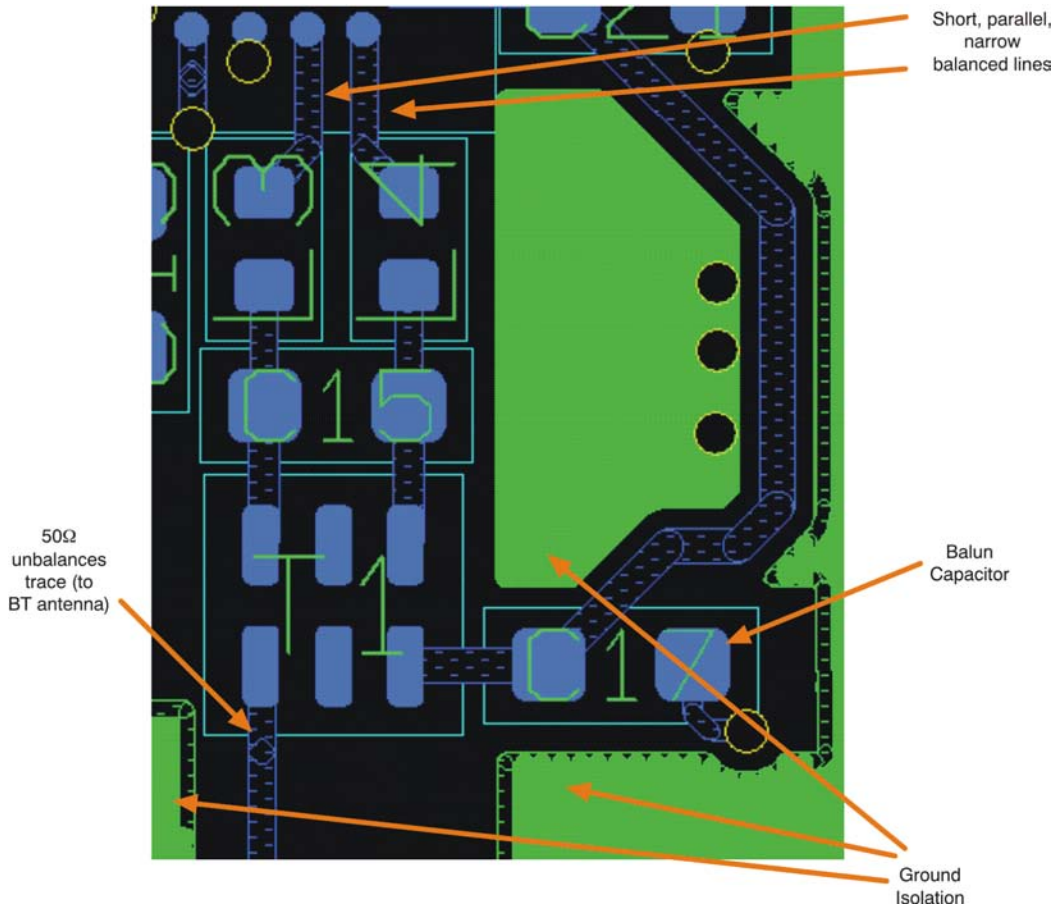


Figure 4. Bluetooth RF Path

6.2 Balanced BT RF Lines

The differential lines between the balanced/unbalanced (balun)/filter sections and the BRF6300 at the BT RF input/output pads should be routed with the same trace length (that is, these traces should be as short as possible in accordance with balun manufacturer requirements), and must be parallel and symmetrical. The differential line width should not be too wide (about 8 mils), in order to avoid excessive parasitic capacitance before the Balun/Filter. There is no need to use matched impedance traces for the balanced RF lines. Refer to Figure 4. The differential lines should be simulated and calculated using an RF simulator program to achieve the best matching network.

When using a matched balun/filter, strictly follow the manufacturer requirements.

6.3 Unbalanced BT RF Line

The single-ended portion of the RF path (after the balun/filter) must use a trace width that is calculated for 50Ω impedance matching (according to the distance from the reference ground). Refer to Figure 4.

6.4 Ground Beneath BT RF Path

In order to avoid parasitic capacitance and parasitic RF coupling, the area beneath the BT RF components on Layers 1 and 2 must not be ground, and must be free from other signals. A minimal distance to the RF ground layer (Layer 3) of 6 mils should be maintained to ensure the least parasitic capacitance.

However, the area on Layer 3 (ground layer) beneath the balanced BT RF lines and beneath the BT RF components must be a complete ground plane, without any other signal trace cutting across it. This rule is critical in the balanced part of the BT RF lines (that is, between the BRF6300 and the balun), but is less critical in the unbalanced RF line (between the balun/filter and antenna). See Figure 5 and Figure 6.

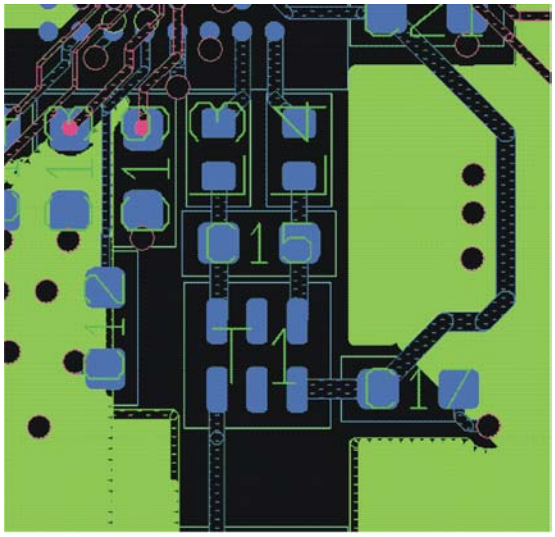


Figure 5. No Ground Beneath BT RF Path on Layer 2

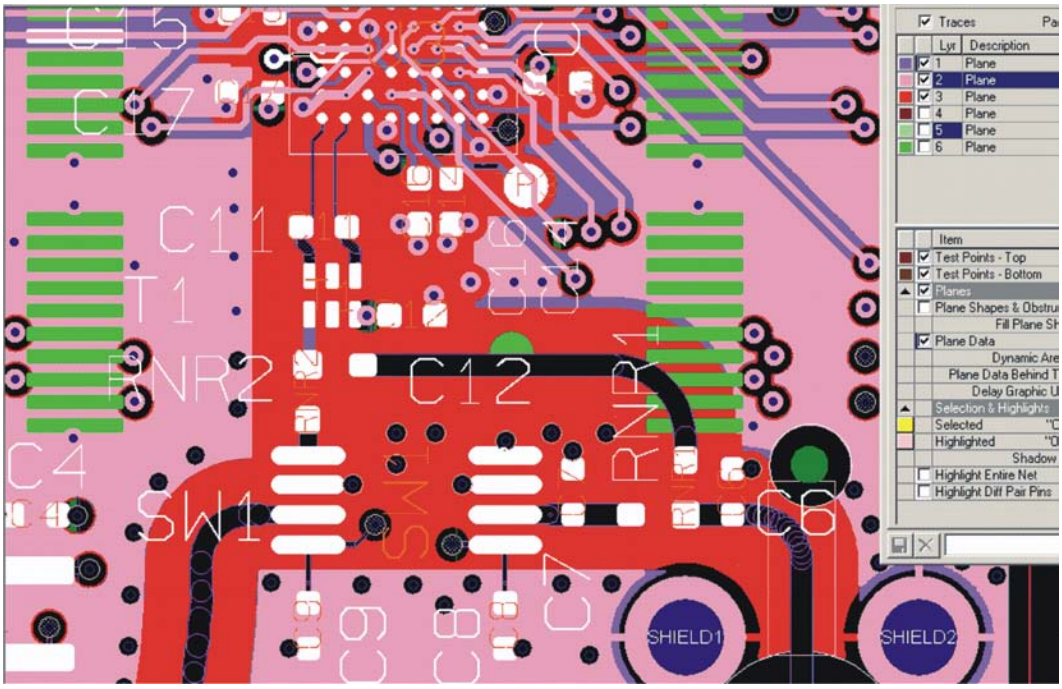


Figure 6. Ground Under RF Path on Layer 3 *(shaded red)*

6.5 RF Path Isolation

Isolate the BT RF area from the rest of the board by placing ground traces and laying out the area to go around the BT RF path. This guideline applies to Layers 1 and 2; see Figure 10.

50Ω matching should not only be done with the ground layer (Layer 3) but also with the top layer environment in order to provide improved shielding, as shown in Figure 7.

The ground area around the RF trace should be strengthened with as many vias as possible, placed on the edge of the ground area and the edge of the plane.

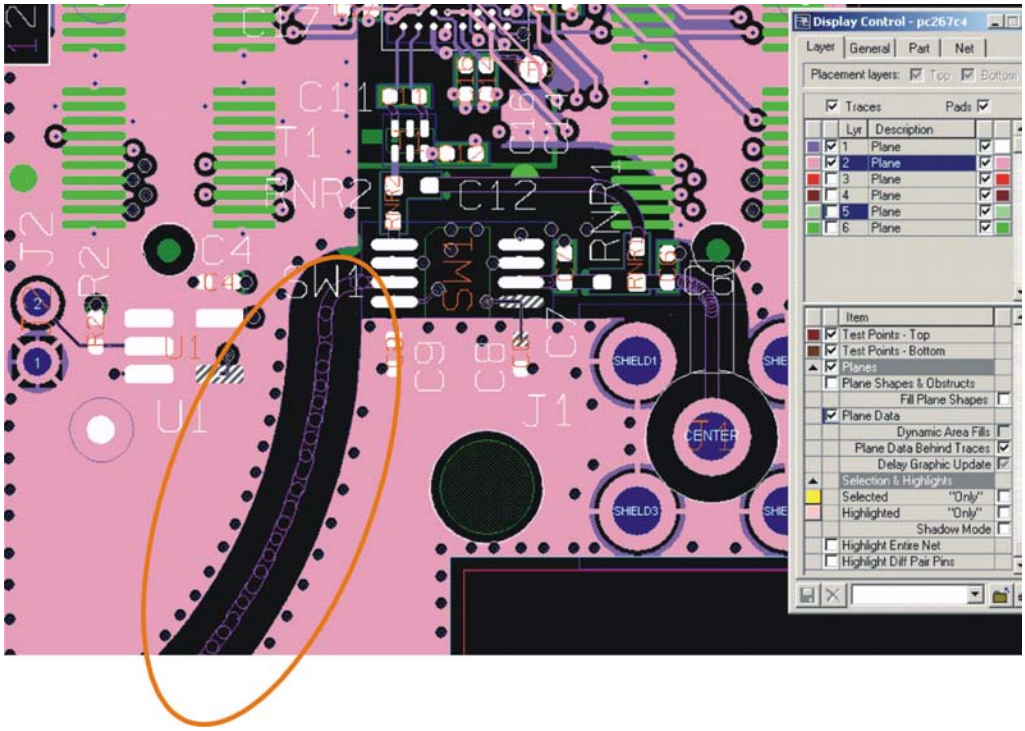
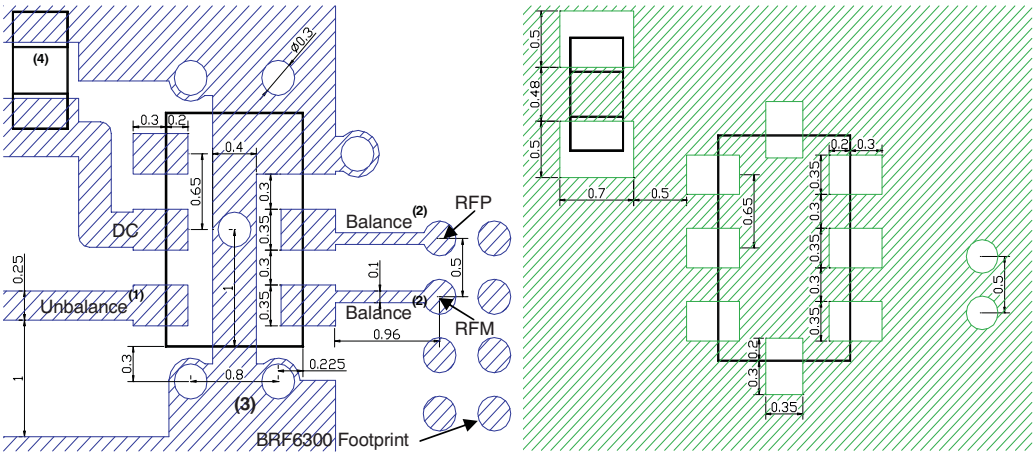


Figure 7. BT RF Path Isolation

6.5.1 Balun/Filter Coupling Capacitor

Generally, balun components must use a coupling capacitor to ground. This capacitor must be connected to the dc supply pin. Placement of the capacitor has great impact on the frequency response, and therefore it must be placed according to the balun manufacturer recommendations. The ground of the capacitor should be the same reference ground as the other BT RF elements. It should also be strengthened with vias to the ground layer.



NOTES: (1) 50Ω impedance line
(2) Assuming trace inductance is 0.4–0.5nH
(3) Ground plane
(4) Decoupling capacitor

Figure 8. Recommended Land Pattern for DBF81H904 for TI BRF6300

7 Power Supply

Place the power supply regulator as close as possible to the BRF6300.

7.1 Power Supply Traces

Power should be supplied to the BRF6300 device using traces with the following characteristics:

- Wide traces; typical width should be 10 mils.
- As short as possible.
- Placed in a dedicated layer, and connected with vias to the power supply pads.
- Coupling capacitor should be placed before the trace that goes to the different balls of the BRF6300.
- Whenever possible and practical, power should be supplied to the different pads on BRF6300 in a *star-like* architecture, and not in series. An even better approach would be to connect (by vias) directly to the power layer.

7.2 Power Supply Isolation

Separate the Bluetooth power supply traces and the Bluetooth regulator (if it is present) from any other devices on the PCB. Be sure to separate the power supply from other RF devices, such as Global System for Mobile Communications power amplifiers (GSM PAs).

7.3 Power Supply Distribution

If the same regulator is used to power only a few devices, these devices should be connected with *star-like* architecture; that is, every device should be connected directly to the regulator.

8 Antenna and Placement

Although the antenna layout should be based on the antenna manufacturer recommendations, the following guidelines should also be considered.

8.1 Antenna Area

All of the area beneath the antenna should be free from ground, unless specifically recommended by antenna manufacturer. This practice should be applied to all internal layers.

8.2 RF Isolation Between Bluetooth and Other RF Components

When designing the cellular board, follow these precautions when placing the cellular RF components and antenna:

- Place the Bluetooth device and the cellular RF part, along with the antennas (GSM or other), as far as possible from each other. It is recommended to keep these devices on the opposite sides of the board.
- Isolate the Bluetooth antenna and the cellular RF antenna as much as possible.
- The two antenna polarizations should be orthogonal (at 90 degrees) for increased isolation.
- It is recommended to use a high-pass filter (HPF) matching network for the Bluetooth antenna, and a low-pass filter (LPF) matching network for the cellular antenna.

9 Ground Planes and Ground Layer

The BRF6300 device uses three different ground signals for analog and for digital.

The digital and analog ground can only be connected together in the internal ground layer (Layer 3) and must not be connected together on the top layer (Layer 1).

This section describes the recommended guidelines to achieve good RF performance.

9.1 Digital Signal Ground

Connect the BT element with the other digital elements on the board with the same ground. The ground should be as solid a plane as possible. Avoid running traces through the ground plane in order to enable short and straight current routes. This principle applies also to other digital grounds with other elements (for example, a codec).

9.2 Ground for RF Devices

Different RF devices, such as a GSM RF device or an external power amplifier, should be interconnected between ground clusters. In order to minimize interference between these devices, the ground connection of each device should be clustered together before connecting to another device RF ground.

For example, if the two ground planes are in the same layer, a gap should be created between the grounds, beneath the Bluetooth to the ground and beneath the other RF device ground.

9.3 Ground Clusters

Digital ground pads, analog ground pads and HV_VSS pads of the BRF6300 must not be connected together on the top layer. Best performance is achieved by using vias to connect each ground pad to the ground Layer (Layer 3). Microvias may be used where usage of traditional vias is not possible. Pads from the same type (digital/analog/HV_VSS) can be connected together (clustered) on the top layer, and shorted with as many vias as possible to the internal ground layer. (See Figure 9.)

Connecting analog ground pads to the digital ground pads, and only then connecting to the internal ground layer, results in parasitic noise. Spurs may appear on the RF and further degrade device performance. Therefore, such wiring configurations must be avoided.

Table 1 describes the ground pads of the BRF6300 (BGA package).

Table 1. BRF6300 Ground Pads (BGA Package)

Pad	Description	Ground Type
VSS	B8, G8, H7, A5, A2	Digital
VSS_HVM	F4	Digital high-voltage module
VSSA	H4, D1	Analog
VSS_RFIO	G1	RF Analog
VSSA	G2, F3	RF Analog

As a result of the pad placement in the BRF6300 and the restrictions described above, only certain pads are able to be clustered to one group. However, it is also possible to connect each of these two pads separately to the ground layer.

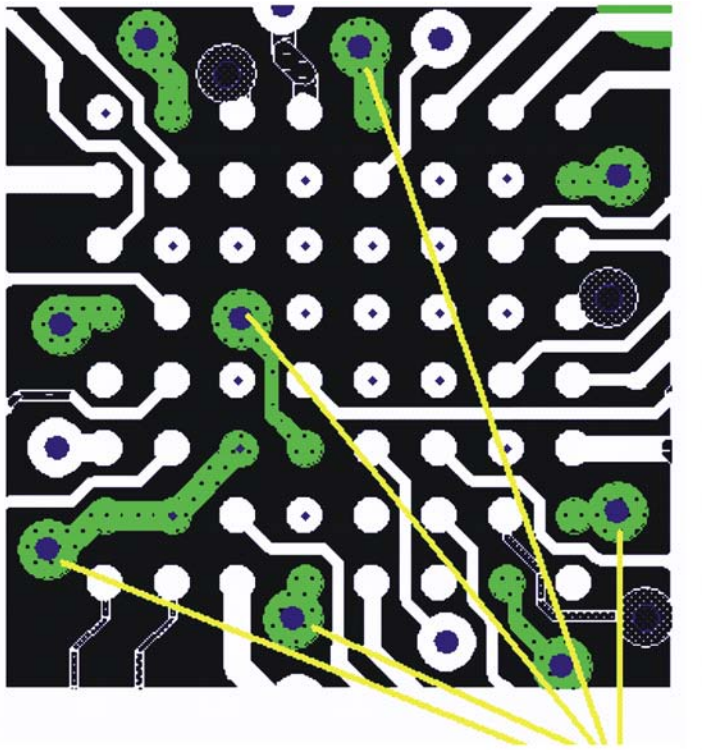


Figure 9. Ground Clusters—Digital and Analog Ground

9.4 Primary Ground Layer (Layer 3)

The digital ground, analog ground and HV_VSS ground can only be connected together in the internal ground layer (Layer 3), and must not be connected together on the top layer (Layer 1) or Layer 2. The ground layer must be a minimum of 6 mils beneath the BRF6300; it should also be a solid ground plane beneath the entire Bluetooth area.

On Layer 2, no signals should be routed beneath the RF area so that nothing separates the RF area and the ground layer (refer to Figure 12). It is extremely important to follow this rule beneath the balanced RF part, from RFIO pads to the BALUN. It is also recommended that any ground area or ground trace be connected with several vias to the ground plane.

9.5 Unused Layout Area

When finishing the layout, fill all free area in Layers 1 and 2 with ground planes. An exception to this guideline is the area beneath the BT RF path (including the antenna). Where ground filling is applied, strengthen the planes to the internal ground plane (Layer 3) with as many vias as possible.

As seen in Figure 10, Layers 1 and 2 are clear from ground under and near the RF path (components and traces).

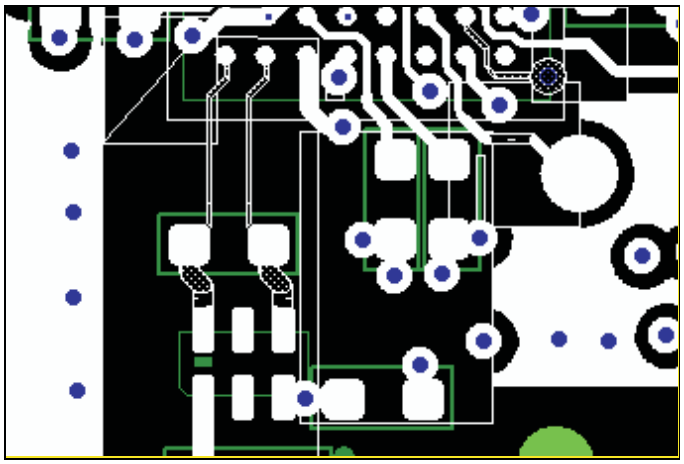


Figure 10. Unused Layout Area and Free Area Beneath RF Parts (Layers 1 and 2)

10 Miscellaneous

10.1 Shielding

In applications with more than one RF device, shield the Bluetooth area in order to improve immunity to interference.

10.1.1 Avoid Digital Lines Beneath the BRF6300

Do not route any digital traces from other devices beneath the Bluetooth area on the PCB. If digital traces must pass beneath the Bluetooth area, the ground plane must isolate it from the Bluetooth signals and from the Bluetooth device. Use caution with the fast clock placement of other devices.

10.1.2 IF Test Points

ANA_TST1 and ANA_TST2 are used to monitor the internal IF for debug purposes. If used on the board, the two signals must be symmetrical and should follow a parallel path (similar to the RF recommendations).

11 PCB Example—BRF6300 Reference Design

This section demonstrates the implementation of the layout recommendations in the TI reference design for the BRF6300. The reference design PCB is composed of six layers (as summarized in Figure 11), with the following vias and microvias.

Microvias are used between:

- Layer 1 and Layer 2
- Layer 2 and Layer 3
- Layer 4 and Layer 5
- Layer 5 and Layer 6

Buried vias are used between:

- Layer 3 and Layer 4

Through-hole vias are used between:

- All layers

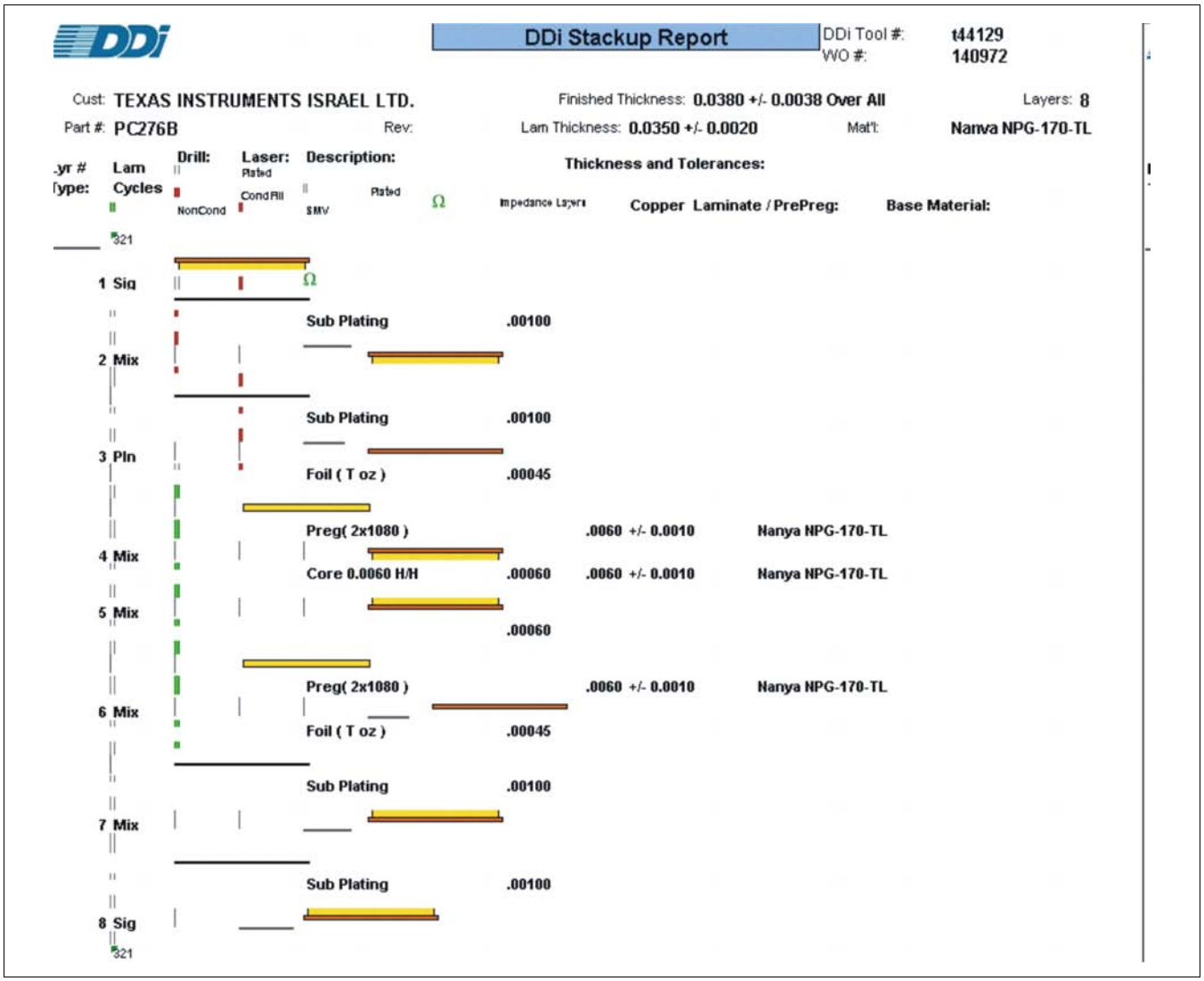
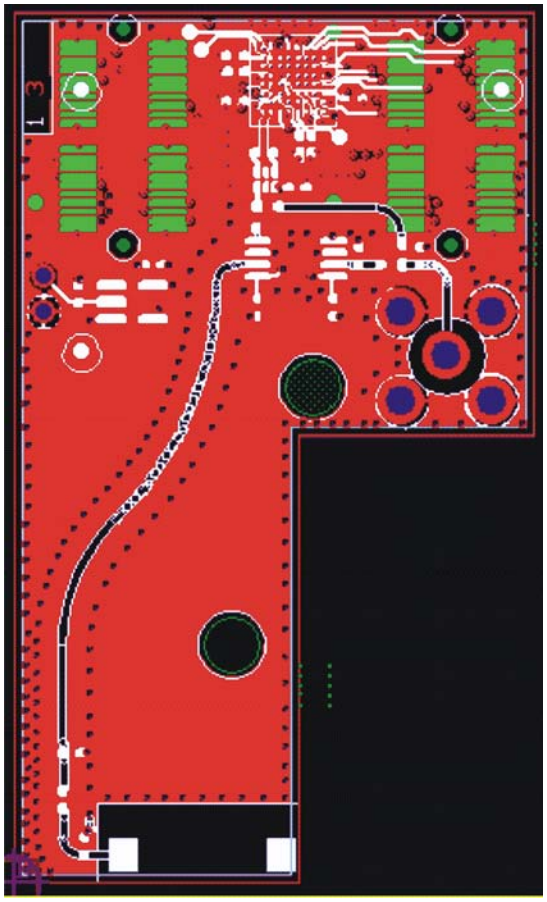


Figure 11. Example Stack-Up of TI Reference Design for BRF6300

11.1 Complete Ground Layer

Figure 12 below shows Layer 3 (the ground plane) with the RF path. Vias have been set along both sides of the RF path to strengthen the ground between Layer 1 and Layer 3.



Note the ground particularly beneath the RF area.

Figure 12. Layer 3: Ground Layer

11.2 Ground on Layer 1

Connect any ground trace on the top level to the ground plane (Layer 3) with vias. It is recommended to connect areas of ground on the top level with several vias, for a strong and effective ground connection. Refer to Figure 13.

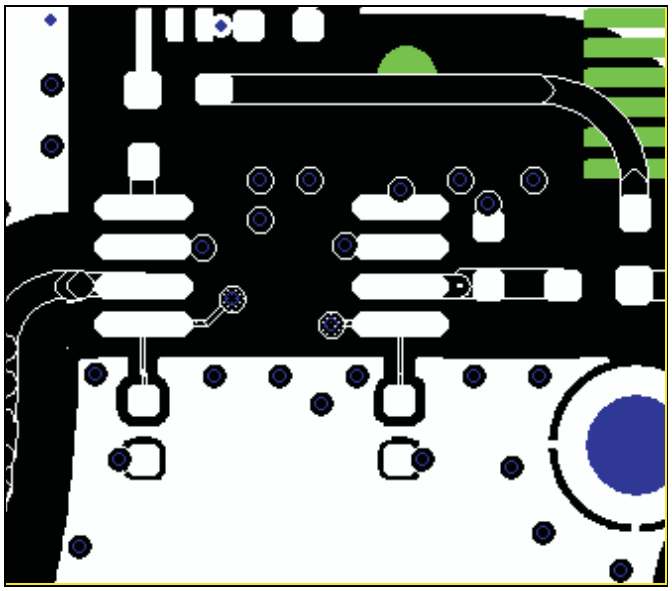


Figure 13. Closed and Partially-Closed Ground Area, Connected to Internal Ground

Figure 14 through Figure 20 depict the placement and layout recommendations for the different PCB layers.

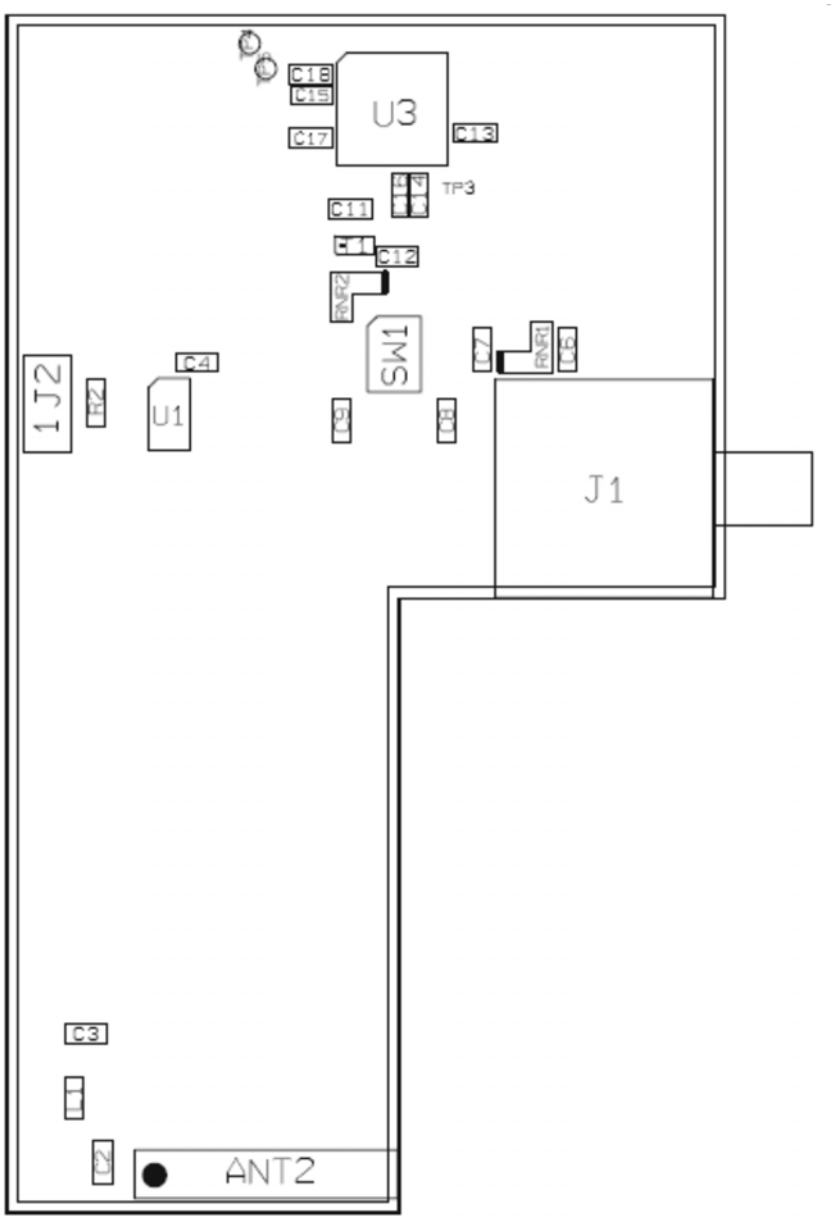


Figure 14. Recommended Layout Placement

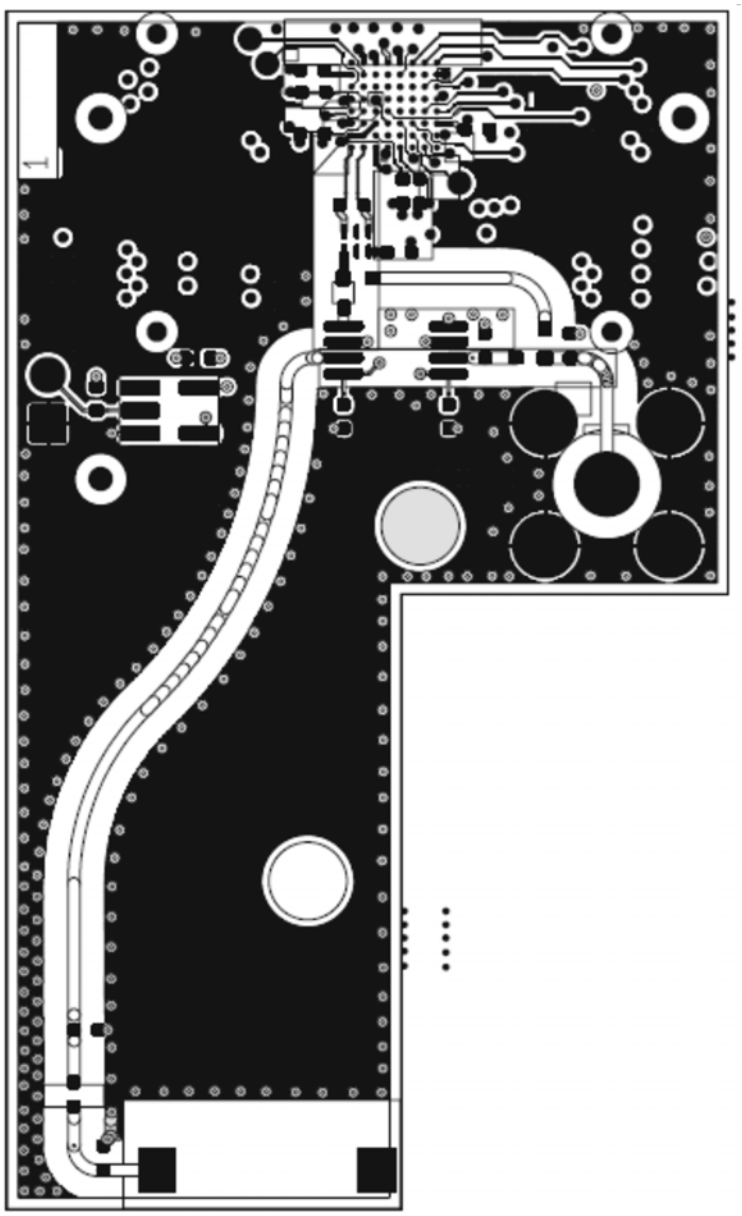


Figure 15. Layer 1 Recommended Layout—Component (Top) Side, Signal layer

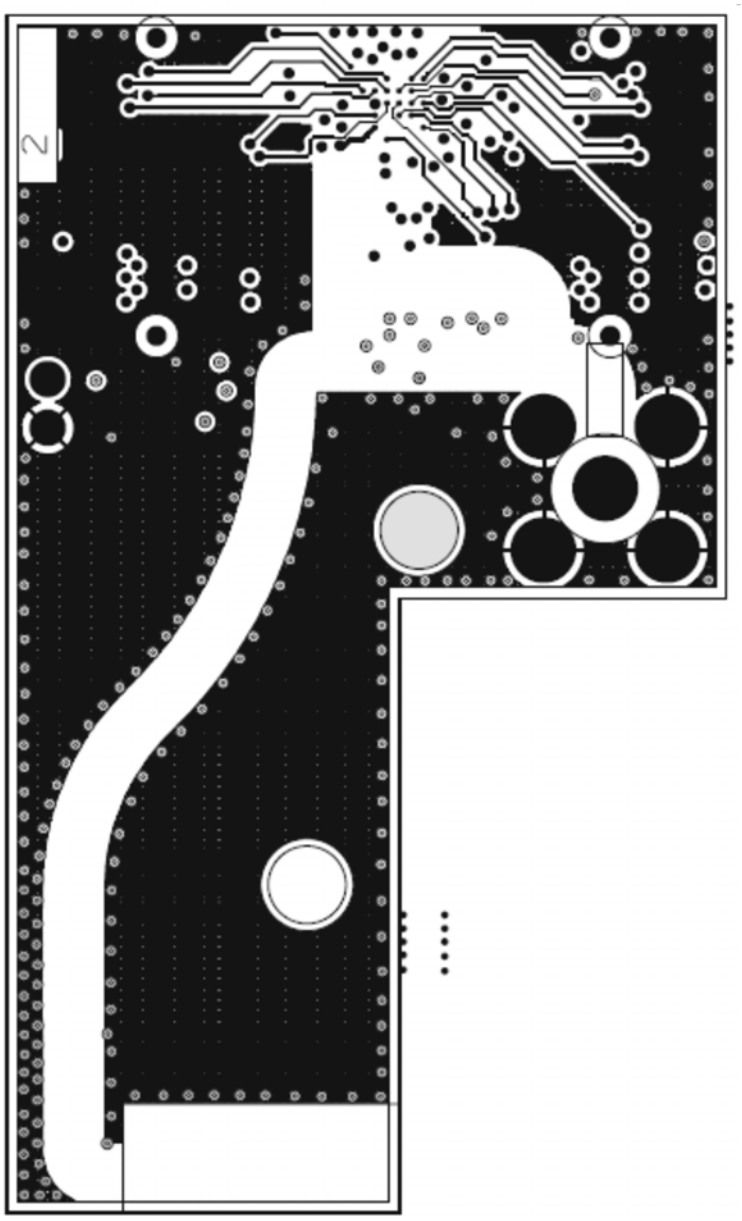


Figure 16. Layer 2 Recommended Layout—INT1, Power Supply and Signaling

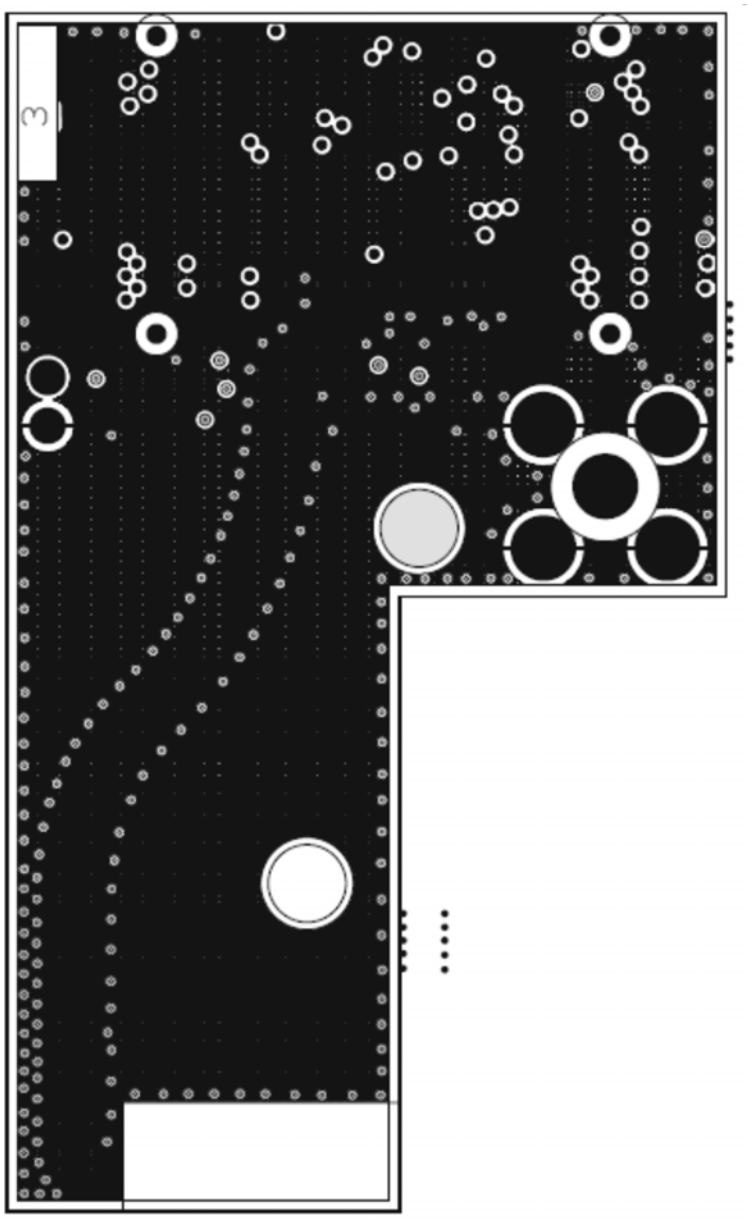


Figure 17. Layer 3 Recommended Layout— INT2, Ground Layer

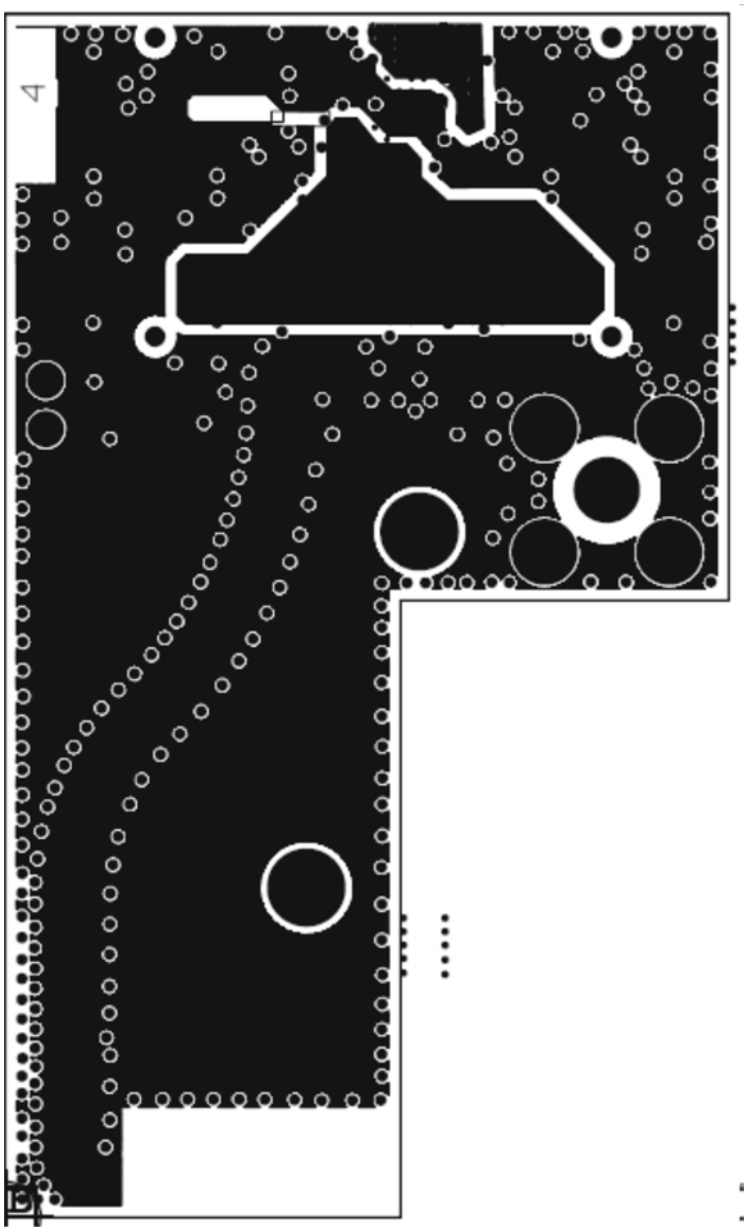


Figure 18. Layer 4 Recommended Layout— INT3, IN/IO Power Layer

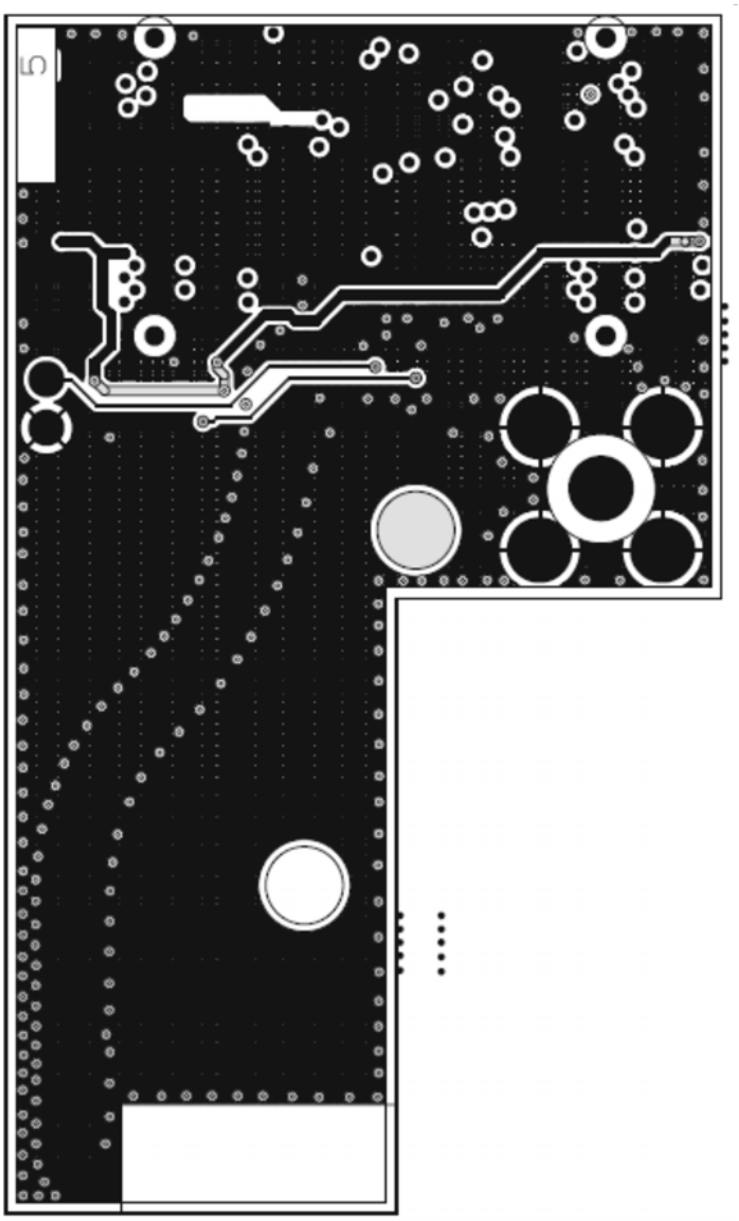


Figure 19. Layer 5 Recommended Layout— Ground and Signal Layer

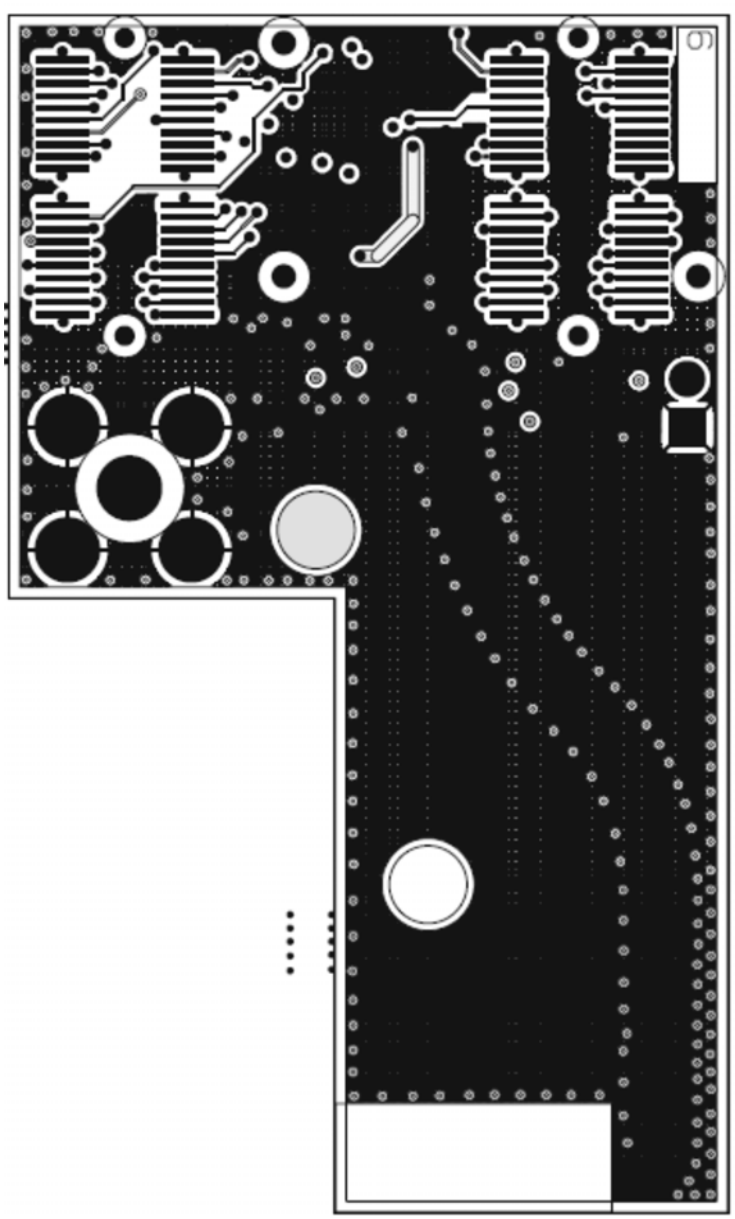


Figure 20. Layer 6 Recommended Layout— Silkscreen (Bottom) Side, Ground and Signal Layer

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