BRF6300 Single-Chip Bluetooth Device

Data Manual

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- **Bluetooth 1.1, 1.2, and 2.0 specifications compliant—up to host controller interface (HCI) level**
- **Enhanced data rate (2 and 3 Mbps)**
- **Enhanced host interfaces (UART, SDIO, and BTSPI)**
- **Very low power consumption**
- **Pin-to-pin compatible with the BRF6150 device**
- **On-chip digital radio processor (DRP)**
  - **Integrated 2.4-GHz RF transceiver**
  - **All digital phase-locked loop (PLL) transmitter with digitally-controlled oscillator**
  - **Near-zero IF architecture**
  - **On-chip TX/RX switch**
- **Support for Class 1 applications**
- **Embedded ARM7TDMIE Microprocessor System On Chip**
- **High rate H4/H5 UART, SDIO, and BTSPI HCI transport layers**
- **Flexible PCM and I2S interfaces: full flexibility for data order, sampling, and positioning**
- **Automatic clock detection mechanism**
- **Patch trap mechanism that enables feature changes in ROM (ROM updates, improvements)**
- **On-chip power management adapted to cellular applications**
  - **Direct connection to battery or external LDO 1.7 V to 5.5 V**
  - **IO supply voltage—1.62 V to 1.925 V**
  - **Power-saving mode**
  - **Shutdown mode to minimize power consumption when Bluetooth is not used**
- **Temperature detection and compensation mechanism ensures minimal variation in the RF performance over the entire operational temperature range**
- **Seamless integration with TI OMAP™ application processors and GSM-GPRS-UMTS chipsets**
- **Enhanced support for WLAN coexistence (bandwidth sharing, antenna sharing)**
- **Spurious emissions compatible with GPS applications**
- **Five external capacitors and balun/matching network required—total PCB area required only 34.3 mm^2 (BGA package)**
- **Packages:**
  - **4.5 x 4.5 mm, 0.5-mm ball pitch, Pb-free MicroStar Junior BGA (ZSL)**
  - **3.2 x 3.2 mm, 0.4-mm ball pitch, Pb-free WSP**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

2 Introduction

This section describes the BRF6300 device.

2.1 Description

The BRF6300 device is a highly integrated single-chip CMOS (90-nm process) Bluetooth device that forms a complete standalone Bluetooth wireless communication system. The BRF6300 device is based on the BRF6150 device and is pin-to-pin backwards compatible with the BRF6150 device when a VDD_IO of 1.8 V is used. The BRF6300 is the third generation of Texas Instruments' single-chip BT devices, succeeding the BRF6150 and the BRF6100 devices.

This device implements an advanced solution for the Bluetooth protocol with easy interfacing to a host system. The BRF6300 comprises:

- Digital radio processor (DRP)
- Embedded Bluetooth point-to-multipoint hardware core for highly optimized execution of the Bluetooth protocol according to Bluetooth specifications 1.1, 1.2, and 2.0 (including EDR 2 or 3 Mbps).
- On-chip ROM
- On-chip RAM
- Embedded ARM7TDMIE microprocessor

The firmware running on the ARM7TDMIE processor includes the lower layers of the Bluetooth protocol up to host controller interface (link controller, link manager, HCI, and HCI transport layer). These functions, combined with several on-chip peripherals, enable easy integration with a variety of applications.

2.2 Enhancements over the BRF6150

- EDR support: 2 or 3 Mbps RF data rate, up to 4 Mbps host interface UART
- Additional host interfaces (BTSPI and SDIO)
- Enhanced DRP for improved power consumption
- Better RF blocking (receiving) and adjacent channel power (transmitting)
- Expanded software update facility (24 patch traps)
- Support wider range of crystal for fast clock
- Extended voltage range (See Section 4)
- Better power supply ripple immunity
- Enhanced clock sharing mechanism—internal logic and wired-OR
- Two additional GPIOs increase feature capability; for example, improved WLAN coexistence
- Better BT/WLAN bandwidth and antenna sharing are achieved by new WLAN coexistence interface, SG 2.0.
- Bluetooth core enhancements:
  - Faster and lower power inquiries are achieved by multiple inquiry access codes (IACs)—identification capability of up to three IACs simultaneously.
  - Improved codec interface capabilities—clock rate and bit ordering
  - Improved QoS obtained through new SNR algorithm (gives enhanced AFH and optimum packet size)

2.3 Functional Block Diagram

The BRF6300 offers an integrated solution for Bluetooth applications. Figure 2−1 presents the device's block diagram.

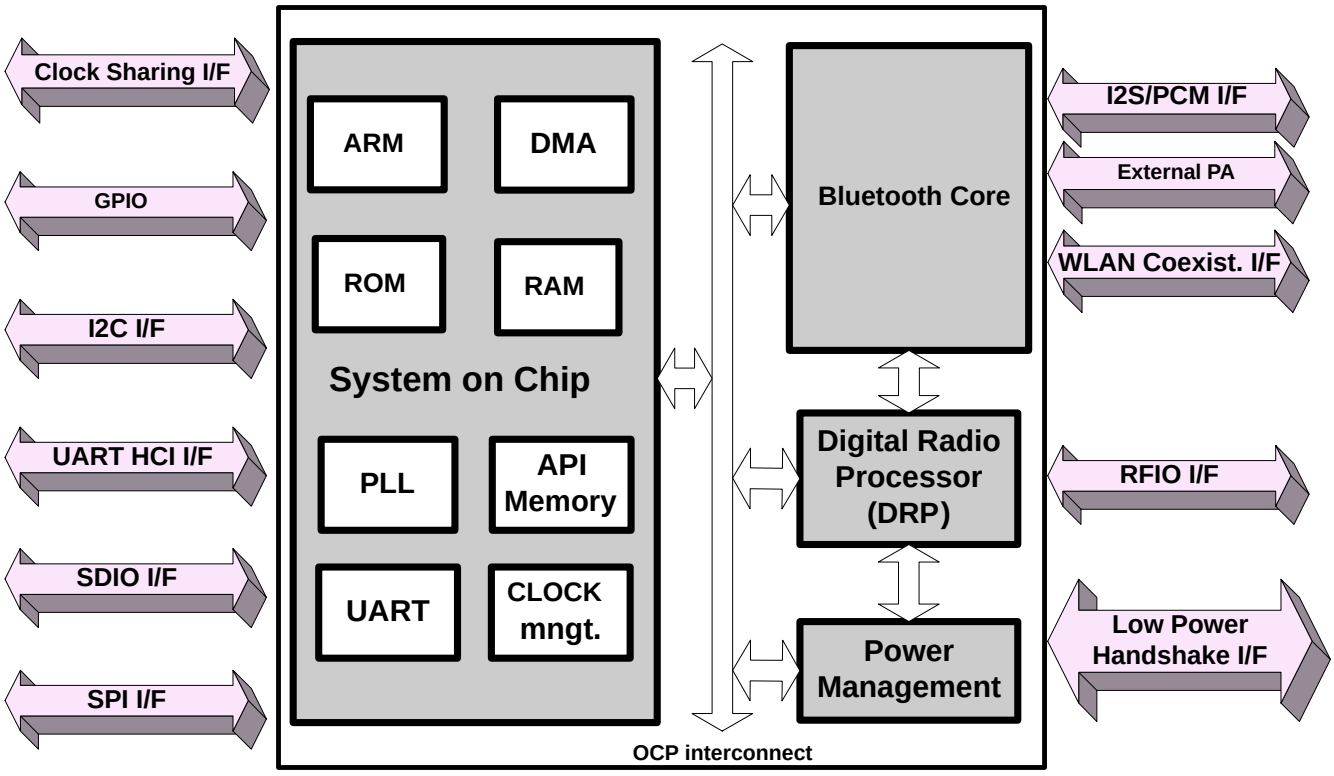


Figure 2−1. BRF6300 Block Diagram

2.4 Power Management

Power management is based on the BRF6150 architecture with the following improvements:

- Extended VDD_IN power range
- Ultralow-power consumption is achieved by shutdown mode.
- Better ripple immunity
- LDO improvements: short-circuit protection

2.5 Codec and Voice Features

- Master or slave mode
- Output clock frequency of up to 4.096 MHz as master
- Input clock frequency of up to 16 MHz as slave
- Full flexibility for bit order, sampling, and positioning
- Packet loss concealment based on last byte repetition

2.6 Host Controller Interface

The BRF6300 supports several HCI transport layers and its main features are:

- Automatic transport layer detection
- UART transport layer; UART rate: 37.5 kbps to 4 Mbps (for the standard cellular fast clock frequencies)

NOTE: There are some exceptions. See TI Baudrate Calculator utility.

- Four-wire UART transport layer (H4)
- Three-wire UART transport layer (H5)
- SDIO transport layer: clock rate up to 20 MHz, 1 bit, slave, V1.0 specification, 1.8 V
- BTSPI transport layer: clock rate up to 13 MHz, 5-wire, slave

2.7 Package Information

The BRF6300 is available in two package types:

- 4.5-mm x 4.5-mm MicroStar Junior BGA Pb-free package (ZSL) (63 pins) with 0.5-mm ball pitch—ROM device
- 3.2-mm x 3.2-mm, 0.4-mm ball pitch, Pb-free WSP (47 pins)

The total solution size for each package is:

- WSP: 25.2 mm^2
- BGA: 34.3 mm^2

This includes the BRF6300 device, LDO decoupling capacitors, and matched balun circuit.

See Section 9 for the mechanical data on the two packages.

2.8 Ordering Information

All devices are lead-free.

TRAY P/N	TAPE & REEL P/N	ROM/SR	SIZE & TYPE (MM)	HEIGHT (MM)	REMARKS
BRF6300CZSL	BRF6300CZSLR	ROM	4.5 x 4.5 BGA	0.8	Production device
	PBRF6300CYFAR	ROM	3.2 x 3.2 WSP	0.625	Preproduction device

2.9 BRF6300 ROM Device Pinouts BGA and WSP (Top View)

Figure 2−2 and Figure 2−3 present the BRF6300 package pin layout.

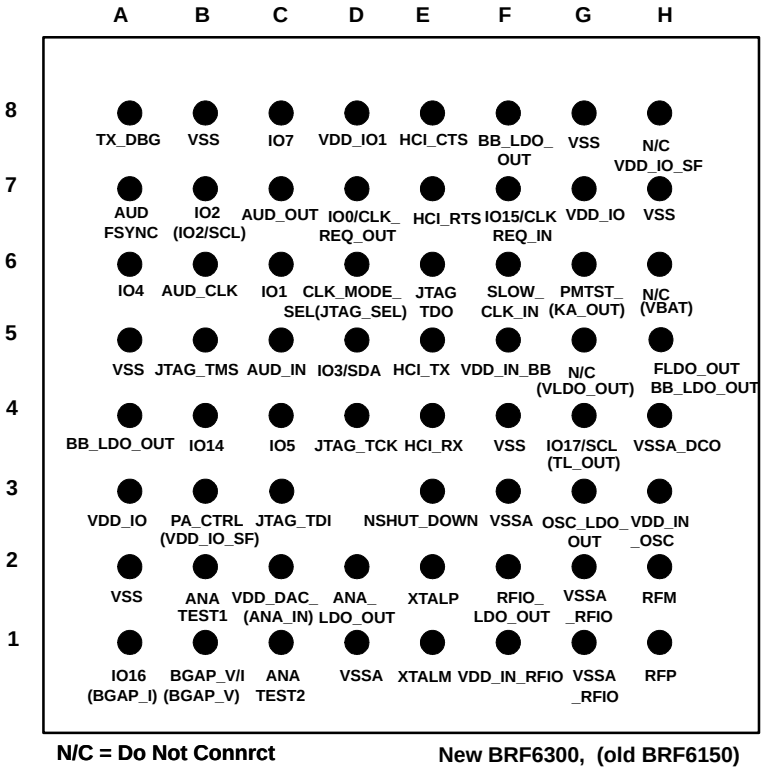


Figure 2−2. BRF6300 BGA Pinouts

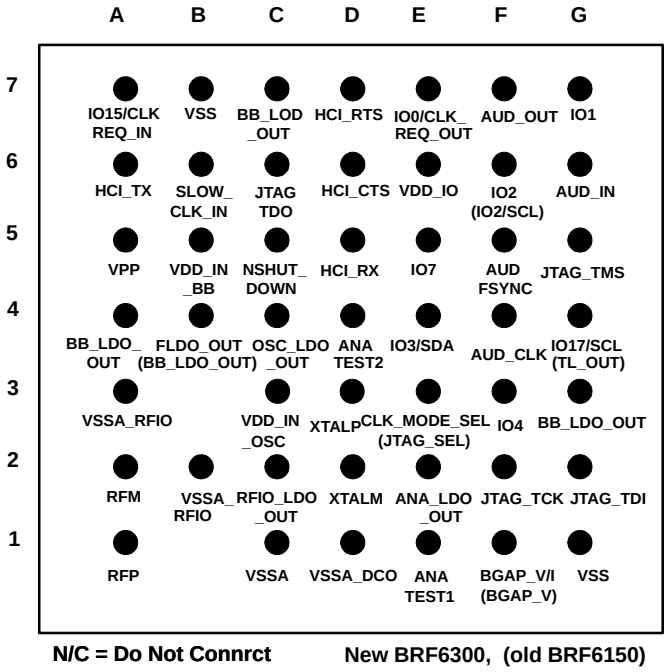


Figure 2−3. BRF6300 WSP Pinouts

2.10 Terminal Functions Description

Table 2−1 presents the terminal functions description.

Table 2−1. Terminal Functions Description

DEFAULT TERMINAL FUNCTION	63 BGA PINS	ESD BGA(3)	47 WSP PINS	ESD WSP(3)	PULL @ RESET	I/O TYPE(1)	BUFFER TYPE(2)	DESCRIPTION OF OPTIONS
HCI_RX SDIO_CMD	E4	2	D5		PU	I IO	B, C	HCI UART data receive (Input) SDIO command, BTSPI_DI
HCI_TX SDIO_DATA	E5	2	A6		PU	O IO	B, C	HCI UART data transmit SDIO data, BTSPI_DO
HCI_RTS SDIO_IRQ	E7	2	D7		PU	O	A, C	HCI UART request-to-send SDIO interrupt, BTSPI_IRQ
HCI_CTS	E8	2	D6		PU	I	B, C	HCI UART clear-to-send BTSPI_CS
AUD_FSYNC	A7	2	F5		PD	IO	A, C	PCM frame synchronization control (O−master, I−slave)
AUD_CLK	B6	2	F4		PD	IO	B, C	PCM clock (O−master, I−slave)
AUD_IN	C5	2	G6		PD	I	A, C	PCM audio data input
AUD_OUT	C7	2	F7		PD	O	B, C	PCM audio data output
JTAG_TMS	B5	2	G5		PU	I	B	JTAG test mode
JTAG_TCK	D4	2	F2		PD	I	B	JTAG test clock
JTAG_TDO	E6	2	C6		PD	IO	B, C	JTAG test data out / JTAG mode select: See Section 2.12
JTAG_TDI	C3	2	G2		PU	I	B	JTAG test data in
CLK_MODE_SEL	D6	2	E3		−−	I	A	Clock sharing mode selection
TX_DBG	A8	2			PU	O	A, C	Default: Debug UART data transmit Options: BT_TX_CONFX*, BT_FREQ*, EXT_PA_CMD1, EXT_PA_CMD2, nEXT_PA_EN, *** Not recommended due to PU.** For WSP device; TX_DBG can be multiplexed to AUD_OUT.
IO0/ CLK_REQ_OUT	D7	2	E7		PD	IO	A, C	Default: External clock request output Options: GPIO0
IO1	C6	2	G7		PD	IO	A, C	Default: GPIO1 Options: BT_TX_CONFX, EXT_PA_EN
IO2	B7	2	F6		PD	IO	A, C	Default: GPIO2 Options: EXT_PA_EN, EXT_PA_CMD1, BT_FREQ, BT_RF_ACTIVE, SYS_SYNC
IO3/SDA	D5	2	E4		PU	IO	A, C	Default: GPIO3/ SDA-I2C data (BRF6300 master) Options: BT_FREQ, EXT_PA_CMD2, nEXT_PA_EN
IO4	A6	2	F3		PD	IO	A, C	Default: GPIO4 Options: BT_RF_ACTIVE, BT_PRIORITY, EXT_PA_CMD1, nEXT_PA_EN, SYS_SYNC

Table 2−1. Terminal Functions Description (Continued)

DEFAULT TERMINAL FUNCTION	63 BGA PINS	ESD BGA(3)	47 WSP PINS	ESD WSP(3)	PULL @ RESET	I/O TYPE(1)	BUFFER TYPE(2)	DESCRIPTION OF OPTIONS
IO5	C4	2			PD	IO	A, C	Default: GPIO5 Options: BT_RF_ACTIVE, SYS_SYNC
IO7 (BT_WAKEUP) SDIO_CLK	C8	2	E5		PD	IO I	A, C	Default: GPIO7 Options: EXT_PA_CMD1, EXT_PA_CMD2 SDIO clock input, BTSPI_CLK
IO14	B4	2			PD	IO	A, C	Default: GPIO14 Options: EXT_PA_EN, BT_RF_ACTIVE, EXT_PA_CMD2, BT_FREQ
IO15/CLK_REQ_IN	F7	2	A7		PD	IO	A, C	Default: GPIO15 / external clock request input Options: nEXT_PA_EN, EXT_PA_CMD2, BT_PRIORITY
IO16	A1	2			PU	IO	A, C	Default: GPIO16 Options: nEXT_PA_EN, BT_FREQ, EXT_PA_CMD1
IO17/SCL	G4	2	G4		PD	IO	A, C	Default: GPIO / SCL / I^2C clock (BRF6300 master) Options: EXT_PA_CMD1, EXT_PA_CMD2, BT_RF_ACTIVE
SLOW_CLK_IN	F6	2	B6		−−	I		32.768-kHz clock input
XTALM	E1	2	D2		−−	I		Negative fast crystal in
XTALP/FAST_CLK_IN	E2	2	D3		−−	I		Positive fast crystal in / fast clock input
RFP	H1	0.3	A1		−−	ANA		Receive/transmit differential RF IO. External RFIO_LDO_OUT voltage required via balun.
RFM	H2	0.3	A2		−−	ANA		Receive/transmit differential RF IO. External RFIO_LDO_OUT voltage required via balun.
ANATEST1	B2	2	E1		−−	ANA		Analog tests—TI use only
ANATEST2	C1	2	D4		−−	ANA		Analog tests—TI use only
VDD_DAC	C2	1			−−	ANA		Reserved—tie to GND
PA_CTRL	B3	2			−−	ANA		Reserved
Not used (BRF6150: VLDO_OUT)	G5	2			−−	P		G5 internally connected to H6 to maintain pin compatibility with BRF6150 designs. For new BRF6300 designs, the pins must be left unconnected.
Not used (BRF6150: VBAT)	H6	2			−−	P		
PMTEST	G6	2			−−	P		Power management test—TI use only
nSHUT_DOWN	E3	1	C5			I		Device shutdown input (active low), also acts as power-on reset (POR)
VDD_IO	D8	2	E6		−−	P		I/O power supply
VDD_IO	G7	2			−−	P		I/O power supply
VDD_IO	A3	2			−−	P		I/O power supply
N.C.	H8	2			−−	P		

Table 2−1. Terminal Functions Description (Continued)

DEFAULT TERMINAL FUNCTION	63 BGA PINS	ESD BGA(3)	47 WSP PINS	ESD WSP(3)	PULL @ RESET	I/O TYPE(1)	BUFFER TYPE(2)	DESCRIPTION OF OPTIONS
FLDO_OUT	H5	0.5	B4		−−	P		FLDO output
BB_LDO_OUT	A4 F8	2	A4 C7 G3		−−	P		Baseband LDO output
ANA_LDO_OUT	D2	0.5	E2		−−	P		Analog LDO output
RFIO_LDO_OUT	F2	0.3	C2		−−	P		RFIO LDO output
OSC_LDO_OUT	G3	0.5	C4		−−	P		OSC LDO output
VDD_IN_BB	F5	0.5	B5		−−	P		Baseband LDO input (VDD_IN power supply)
VDD_IN_RFIO	F1	0.5			−−	P		RFIO LDO input (VDD_IN power supply)
VDD_IN_OSC	H3	0.5	C3		−−	P		OSC LDO input (VDD_IN power supply)
BGAP_V/I	B1	2	F1		−−	P		BGAP reference—TI use only
Vpp			A5					Die ID programming voltage—must be N.C.
VSS	B8	−−			−−	P		Digital ground
VSS	G8	−−	B7		−−	P		Digital ground
VSS	H7	−−			−−	P		Digital ground
VSS	A5	−−			−−	P		Digital ground
VSS	A2	−−	G1		−−	P		Digital ground
VSS	F4	−−			−−	P		Digital ground
VSSA_DCO	H4	−−	D1		−−	P		DCO analog ground
VSSA	D1	−−	C1		−−	P		Analog ground
VSSA_RFIO	G1	0.3	B2		−−	P		RF analog ground
VSSA_RFIO	G2	0.3	A3		−−	P		RF analog ground
VSSA	F3	−−			−−	P		Analog ground

NOTES: 1. I = input; O = output; IO = bidirectional; P = power pin (VDD, ground or LDO output); ANA = analog pin
2. A= input buffer without hysteresis; B= input buffer with hysteresis; C = 8 mA output buffer.
3. Human Body Model (HBM) in kV. JEDEC 22-A114 two-wire method.
CDM: All pins pass 500 V (BGA).
4. Latchup (BGA): 200 mA at 25°C − pass, 100 mA at 90°C − pass.

2.11 I/O States—Normal Versus Shutdown

Table 2−2 presents the I/O states.

Table 2−2. I/O States—Normal Versus Shutdown

IO NAME	ACTIVE STATE(1)		SHUTDOWN STATE	
	I/O	LEVEL	I/O	LEVEL
AUD_CLK	I	PD	Z	PD
AUD_FSYNC	I	PD	Z	PD
AUD_IN	I	PD	Z	PD
AUD_OUT	Z	PD	Z	PD
IO0/CLK_REQ_OUT	I	PD	Act(3)	PD1(3)
IO1	I	PD	Z	PD
IO2	I	PD	Z	PD
IO3/SDA	I	PU	Z	PU
IO4	I	PD	Z	PD
IO5	I	PD	Z	PD
IO7	I	PD	Z	PD
IO14	I	PD	Z	PD
IO15/CLK_REQ_IN	I	PD	I(3)	PD
IO16	I	PU	Z	PU
IO17/SCL	I	PD	Z	PD
HCI_RX	I	See Note 2	Z	PU
HCI_TX	O	See Note 2	Z	PU
HCI_RTS	O	See Note 2	Z	PU
HCI_CTS	I	See Note 2	Z	PU
JTAG_TCK	I	PD	Z	PD
JTAG_TDI	I	PU	Z	PU
JTAG_TDO	Z	PD	Z	PD
JTAG_TMS	I	PU	Z	PU
TX_DBG	O	PU	Z	PU

NOTES: 1. I = input, O = output, Z = HiZ, Act = active, if used as output.
2. Pulls remain enabled until the interface is detected after the first byte is received. Thereafter, pulls are disabled for the UART and SPI, and enabled for the SDIO.
3. For CLK_MODE_SEL = 1 (internal logic clock select mode), PD1 is disabled. For CLK_MODE_SEL = 0 (wired-OR mode), IO0 and IO15 are HiZ.

2.12 JTAG Boundary Scan Operation

The BRF6150 uses a dedicated pin, JTAG_SEL, to select the JTAG boundary scan. Because BRF6300 uses this pin for other functionality, JTAG_TDO is used instead. JTAG_TDO performs a dual-function of JTAG selection and test data out. Initially, JTAG_TDO acts as an input that selects the JTAG boundary scan mode. JTAG_TDO (as input) is sampled on the first rising edge of JTAG_TCK and reverts to an output at the first falling edge of JTAG_TCK. A low on JTAG_TDO selects the boundary scan.

Note that JTAG_TDO has internal PD (typically 20 μA). Therefore, when the JTAG_TCK clock function is present and there is no external PU on JTAG_TDO, the JTAG boundary scan is automatically selected.

JTAG ID number for BRF6300 = 1011 0110 1001 1110b

Hawkeye_Component_name: F761804. Hawkeye_ID: 23591

2.13 I²C External EEPROM Automatic Detection

The BRF6300 automatically detects and downloads an initialization script from an external EEPROM using the I²C bus on pins IO3 (SDA) and IO17 (SCL). If a high is detected on IO17 during power up, the BRF6300 automatically configures IO3 and IO17 as outputs for the I²C master interface and attempts to read the EEPROM.

For this reason, if IO17 is used for some other purpose, care must be taken that it is not high at power up. IO17 has an internal PD at power up and can be left open if it is not used.

3 Detailed Description

The BRF6300 architecture comprises a digital radio processor (DRP) and a point-to-multipoint baseband core. The architecture is based on a single-processor ARM7TDMIE core. The device includes several on-chip peripherals to enable easy communication with a host system and the Bluetooth core.

3.1 Digital Radio Processor

The BRF6300 is the third generation of TI Bluetooth single-chip devices using DRP architecture. Modifications and new features have been added to the DRP to further improve radio performance. Figure 3−1 presents the DRP block diagram.

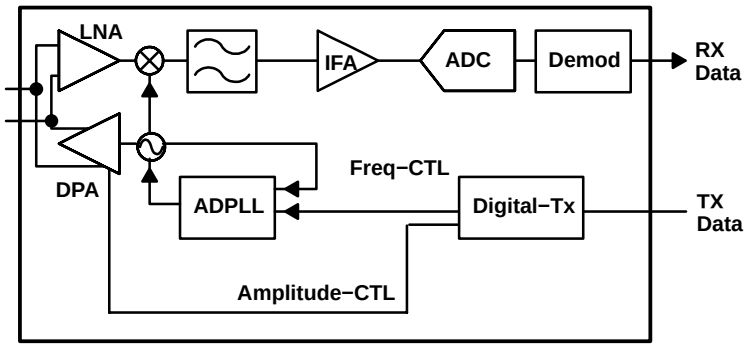


Figure 3−1. DRP Block Diagram

3.1.1 Receiver

The receiver uses near-zero IF architecture to convert the RF signal to baseband data. The received signal from the external antenna and balun is input to an internal RF switch and a differential low-noise amplifier (LNA). This signal is then passed to a mixer which downconverts the signal to an IF, followed by a filter and amplifier. The signal is then quantized by a sigma-delta analog-to-digital converter (ADC). The quantized signal is further processed to reduce the interference level.

The demodulator digitally downconverts the signal to zero IF and recovers the data bit-streams by an adaptive decision mechanism. The demodulation includes an EDR process with state-of-the-art performance. It includes a maximum likelihood sequence estimator (MLSE) for improved performance of basic rate GFSK sensitivity and an adaptive-equalization for enhancing EDR modulation.

New features include:

- A new Rx demodulator is included to support EDR modulation
- The LNA input range is narrowed to increase blocking performance
- The IFA is optimized for improved co-channel performance

3.1.2 Transmitter

The transmitter is based on an all-digital sigma-delta phase-locked loop (PLL) with a digitally-controlled oscillator (DCO) at 2.4 GHz as the RF frequency clock. The modulation is achieved by directly modulating the digital PLL. The power amplifier is also digitally controlled.

For EDR modulation, the transmitter uses a polar-modulation technique. In this mode, in addition to the frequency modulation that controls the direct-modulated ADPLL, an amplitude control modulates the PA. To support this, a new block called digital-transmitter has been added. This block receives the input bit-stream and converts these signals to phase-modulated control words. The phase-modulated digital signal is then processed to provide frequency-modulation control to the ADPLL.

New features include:

- New digital-Tx block is added to support EDR modulation with a polar-modulation architecture which gives best spectral purify with low current consumption EDR.

3.2 Power Supply and Power Management

The BRF6300 single-chip Bluetooth solution is intended to work within power-minded devices such as cellular phones, headsets, hand-held PCs, and other battery-operated devices. One of the main differentiators of the BRF6300 is its power management—its ability to draw as little current as possible. The power-management system in BRF6300 is based on an improved version of the BRF6150 power-management system.

3.2.1 Power Sources

The BRF6300 device requires two kinds of power sources:

- The main power supply for the system core—VDD_IN (pins VDD_IN_BB, VDD_IN_OSC, VDD_IN_RFIO)
- The power source for the I/O ring—VDD_IO

The BRF6300 includes several on-chip voltage regulators that help increase noise immunity.

3.2.2 Operation During Shutdown—Static States

The nSHUT_DOWN pin can shutdown the entire device and reduce the current consumption to the very minimum (only leakage through the power supply connections).

Table 3−1 describes the static states that the device can operate in. The general rule is that nSHUT_DOWN may not be high if VDD_IN is low.

Table 3−1. BRF6300 Static States

VDD_IN	VDD_IO	NSHUT_DOWN	REMARKS
Low	Low	Low	Shutdown mode
Low	Low	High	Not allowed
Low	High	Low	Shutdown mode
Low	High	High	Not allowed
High	Low	Low	Shutdown mode, but no voltages allowed on any I/O pin
High	Low	High	Not allowed
High	High	Low	Shutdown mode
High	High	High	Active mode

nSHUT_DOWN is low if it is driven low or left floating.

3.2.3 Improvements over BRF6150

The following improvements are included in the Island3 power-management system:

- Reduced the number of required decoupling capacitors
- Wider range of VDD_IN is supported to allow direct battery connection or EXT_LDO on the same input
- VBAT/external-LDO core power supply—VDD_IN
- Same value of decoupling capacitor for all LDOs

Figure 3−2 describes the core power connection to the device. The LDO inputs are connected directly to the battery or external LDO.

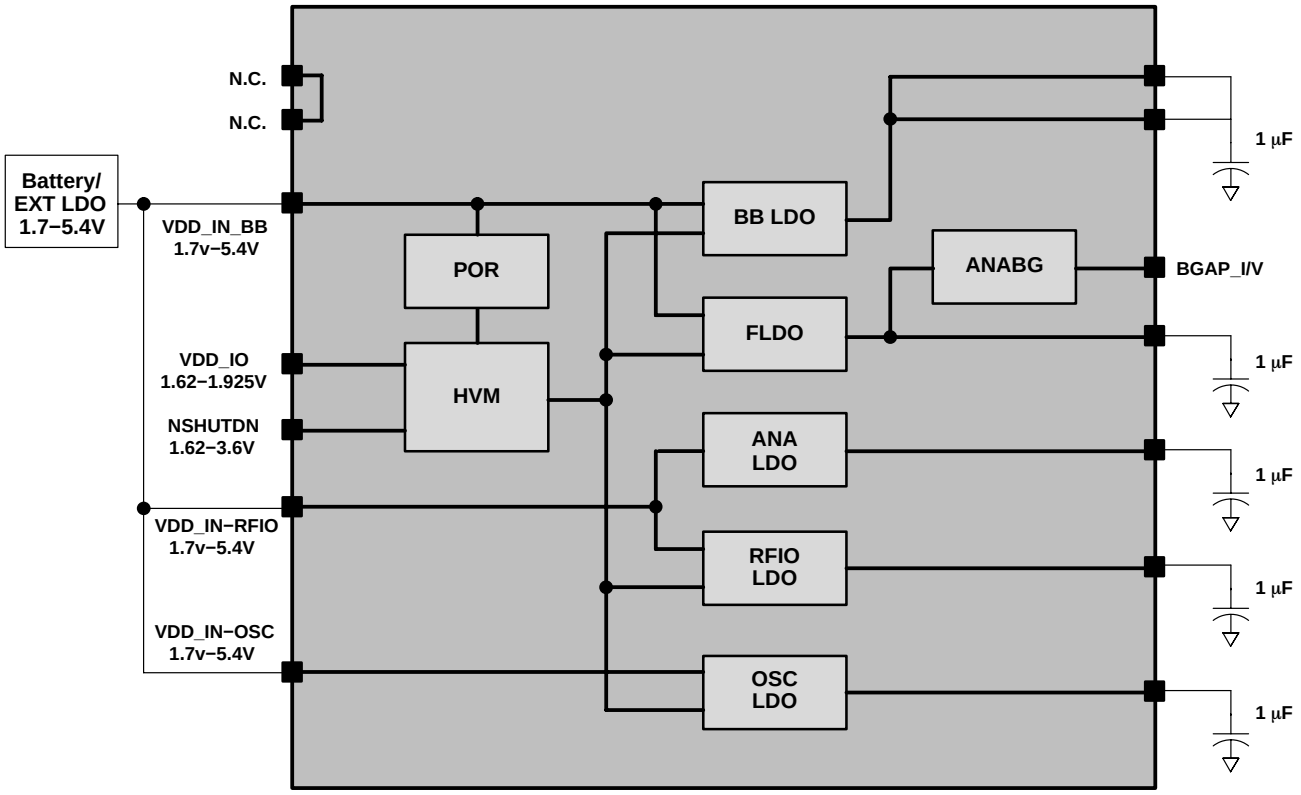


Figure 3−2. VBAT/External LDO Connection

3.2.4 I/O Power Supply—VDD_IO

The BRF6300 supports the following power supply voltage range for the I/O ring (VDD_IO): 1.62 V to 1.925 V.

Note that the BRF6300 I/Os are not fail safe. Fail safe means that the pins will not draw any dc power from an external voltage applied to the pin when no I/O power is supplied to the BFR6300 device. Only the clock inputs, XTALP/FAST_CLK_IN and SLOW_CLK_IN, are fail safe.

Damage to device may result if external voltages are applied to I/O pins when no VDD_IO supply is present.

3.2.5 Powerup/Powerdown Sequence

Powerup requirements:

- nSHUT_DOWN must be low. VDD_IN and VDD_IO are don't-care during nSHUT_DOWN low. However, no signals are allowed on IOs if no VDD_IO (not fail safe), as damage to the device may occur.
- VDD_IN, VDD_IO, and slow clock must be stable before releasing nSHUT_DOWN.
- The nSHUT_DOWN signal rise time must not exceed 20 µs.
- Fast clock must be stable maximum 30 ms after nSHUT_DOWN goes high.

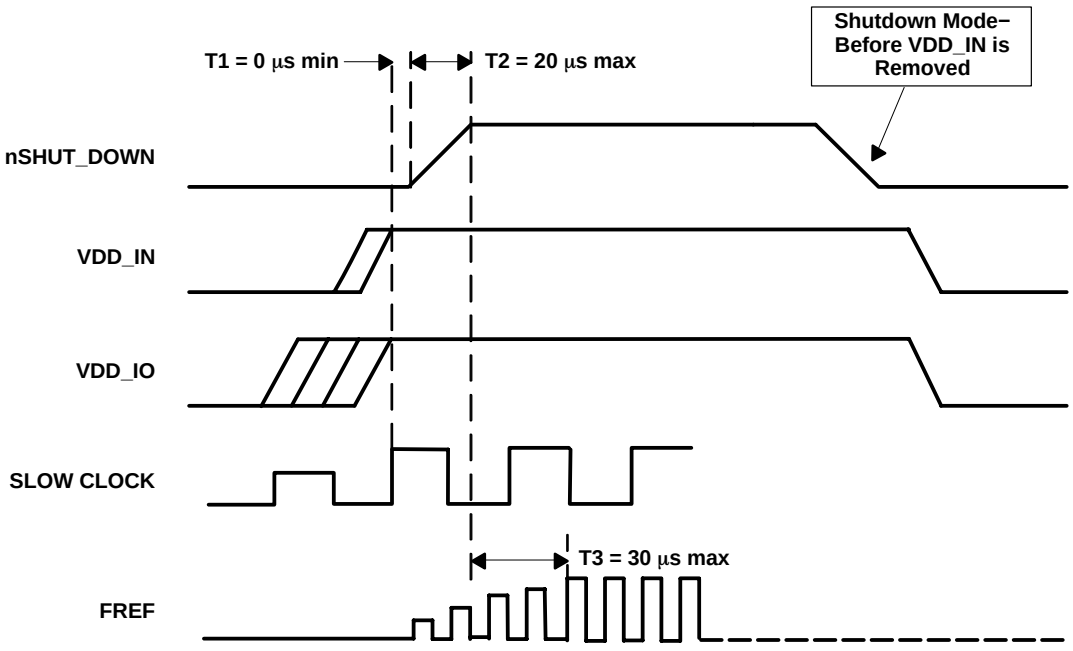


Figure 3−3. Powerup/Powerdown Sequence

The BRF6300 indicates completion of powerup sequence by asserting RTS low. This occurs approximately 150 ms after nSHUT_DOWN goes high.

3.2.6 BRF6300 Power Consumption In Different Modes

The BRF6300 has several modes of operation with different power consumptions in each mode.

3.2.6.1 Shutdown Mode

This mode represents the ultralow-power mode. In this mode the device is not functional and consumes the absolute minimum power. This mode is entered by asserting the nSHUT_DOWN pin low. Even though VDD_IN and VDD_IO may be supplied to the device, no voltage is supplied internally to the device.

During this mode, the VDD_IO supply may be removed provided no external voltage is present on any BRF6300 I/O pin, such as codec, I/Os, UART I/F, etc. Only the slow clock and XTALP/XTALM fast clock inputs may have signals present.

If nSHUT_DOWN is left floating, an internal pulldown will keep the device in shutdown mode.

During shutdown, all I/Os are in hi-Z with pulls enabled.

3.2.6.2 Deep Sleep Mode

The device can be placed in the deep sleep mode when not connected to or not communicating with the host, or in low-power connection such as sniff, park, and hold. Deep sleep represents the second lowest power mode. Power is supplied to the device and all pins retain their states and the values of their pulls, as they were just before entering deep sleep.

However, most of the device is internally shutdown. Only the slow clock digital portion of the BRF6300 is active and requires the external slow clock. The fast clock to the BRF6300 can be switched off. This mode is first enabled by the host using an HCI vendor-specific command. Thereafter, this mode is entered and exited automatically by the BRF6300.

When exiting from deep sleep, CLK_REQ_OUT is immediately asserted and the BRF6300 waits for a specific settling time until the external fast clock is stable. The default settling time can be changed to always be longer than the actual system clock settling time, by using a vendor-specific HCI command, from 2 to 125 ms. Default is 15 ms.

3.2.6.3 Standby Mode

The device is in standby mode when it is actively connected with another Bluetooth device and not transmitting or receiving; that is, just after power-on, or during the wake-up periods of a low-power connection.

3.2.6.4 Transmit Mode

Transmitter circuitry is enabled and receiver circuitry is disabled.

3.2.6.5 Receive Mode

Receiver circuitry is enabled and transmitter circuitry is disabled.

3.2.7 TX/RX Power Consumption

Table 3−2 and Table 3−3 give the average power consumption for different Bluetooth scenarios.

Conditions: VDD_IN = 3.6 V, VDD_IO = 1.8 V, 25°C, 26-MHz fast clock, power level 6 (~0 dBm) output power-on device pins, and best RX performance.

Table 3−2. Average Power Consumption—Basic Rate

MODE DESCRIPTION	MASTER/SLAVE	AVERAGE CURRENT CONSUMPTION	UNIT
Standby	Master/Slave	4.0	mA
Continuous TX		40	mA
Continuous RX		40	mA
SCO link HV1	Master/Slave	34.3	mA
SCO link HV2 (ACL connection in sniff mode)	Master/Slave	19.3	mA
SCO link HV3 (ACL connection in sniff mode)	Master/Slave	14.2	mA
eSCO link EV3 64 Kbps, no retransmission	Master	14.8	mA
eSCO link EV3 64 Kbps, no retransmission	Slave	19.9	mA
eSCO link EV4 64 Kbps, no retransmission	Master	12.5	mA
eSCO link EV4 64 Kbps, no retransmission	Slave	18.7	mA
eSCO link EV5 64 Kbps, no retransmission	Master	9.7	mA
eSCO link EV5 64 Kbps, no retransmission	Slave	16.4	mA
DH1/DH1 full data rate	Master/Slave	36	mA
DH1−5/DH1−5 (except DH1/DH1) full data rate	Master/Slave	39	mA
Sniff 1280 ms, 2 attempts	Master	77	µA
Sniff 1280 ms, 2 attempts	Slave	116	µA
Page or inquiry scan, 1.28 s, 11.25 ms	Master/Slave	400	µA
Page + inquiry scan, 1.28 s, 11.25 ms each	Master/Slave	800	µA
Park 1.28 s	Master	550	µA
Park 1.28 s	Slave	180	µA

Table 3−3. Average Power Consumption—EDR

MODE DESCRIPTION	MASTER/SLAVE	AVERAGE CURRENT CONSUMPTION	UNIT
Continuous TX (EDR3)		44	mA
TX = 2 − EV3, RX = 2 − EV3, 64 Kbps, no retransmission	Master	9.6	mA
TX = 2 − EV3, RX = 2 − EV3, 64 Kbps, no retransmission	Slave	16.2	mA
TX = 3 − EV3, RX = 3 − EV3, 64 Kbps, no retransmission	Master	7.9	mA
TX = 3 − EV3, RX = 3 − EV3, 64 Kbps, no retransmission	Slave	14.8	mA
TX = 2 − EV5, RX = 2 − EV5, 64 Kbps, no retransmission	Master	7.1	mA
TX = 2 − EV5, RX = 2 − EV5, 64 Kbps, no retransmission	Slave	14.4	mA
TX = 3 − EV5, RX = 3 − EV5, 64 Kbps, no retransmission	Master	6.3	mA
TX = 3 − EV5, RX = 3 − EV5, 64 Kbps, no retransmission	Slave	13.6	mA
TX = 2 − DH1/3 − DH1, RX = 2 − DH1/3 − DH1	Master/Slave	37	mA
TX = 2 − DH1/3 − DH1, RX = 2 − DH3/3 − DH3	Master/Slave	39	mA
TX = 2 − DH1/3 − DH1, RX = 2 − DH5/3 − DH5	Master/Slave	39	mA
TX = 2 − DH3/3 − DH3, RX = 2 − DH3/3 − DH3	Master/Slave	40	mA
TX = 2 − DH5/3 − DH5, RX = 2 − DH5/3 − DH5	Master/Slave	41	mA

3.3 BRF6300 Clocks

The BRF6300 operates with two different input clocks: fast and slow.

3.3.1 Slow Clock

The slow clock is always supplied from an external source. It is input on the SLOW_CLK_IN pin and can be a digital signal in the range of 0 to 3.6 V. The slow clock must be 32.768 kHz ±250 ppm, as per Bluetooth requirements.

3.3.2 Fast Clock

Clock sources for the fast clock are either from a crystal or from an external clock source fed through an internal squarer cell. The BRF6300 supports common clock frequencies in the range 12-MHz to 40-MHz fast clock.

According to the Bluetooth specification, the accuracy of the fast clock source must not exceed ±20 ppm. The BRF6300, however, has the ability to work with a fast clock source (external oscillator or crystal) with a fixed offset of up to ±150 ppm from the required frequency, and still meet the BT specification. This offset is sent to the BRF6300 via a vendor-specific command. Thereafter, the clock source must remain within ±20 ppm of the specified frequency.

An automatic clock recognition algorithm detects the clock frequency.

The external clock can be:

- ac-coupled
- dc-coupled
- External crystal

The following paragraphs describe the requirements for each condition.

To optimize the internal clock detection circuitry for the various fast clock configurations, the VS command HCI_VS_Clock_Configuration must be issued by the host as soon as possible after power up or shutdown.

NOTE:

The following typical dc voltages are present at Fast_clk_in:

- Reset and deep sleep = 0 V
- Active modes = 400 mV

3.3.2.1 External Input dc-Coupled

Figure 3−4 illustrates the configuration when using a dc-coupled external source for the fast clock input.

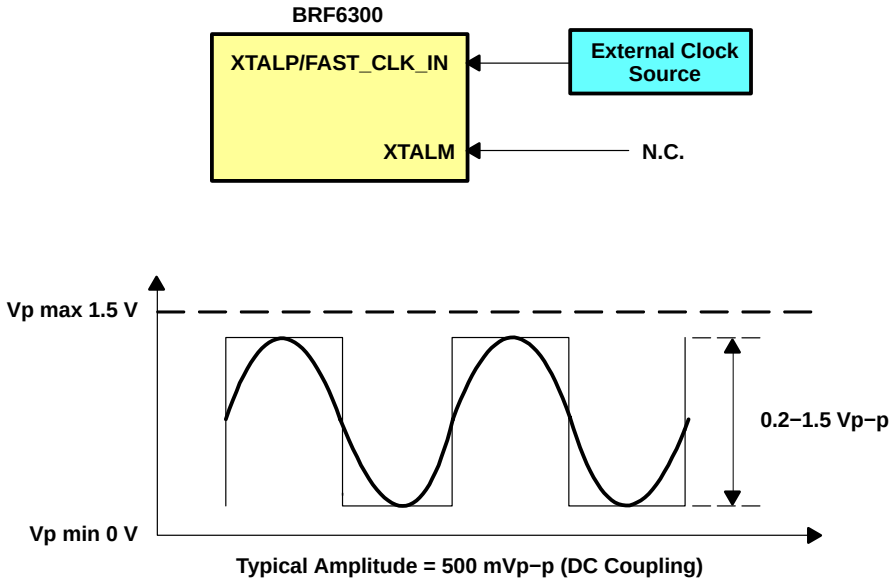


Figure 3−4. External Fast Clock (dc-Coupled)

3.3.2.2 External Input ac-Coupled

Figure 3−5 illustrates the configuration when using an ac-coupled external source for the fast clock input.

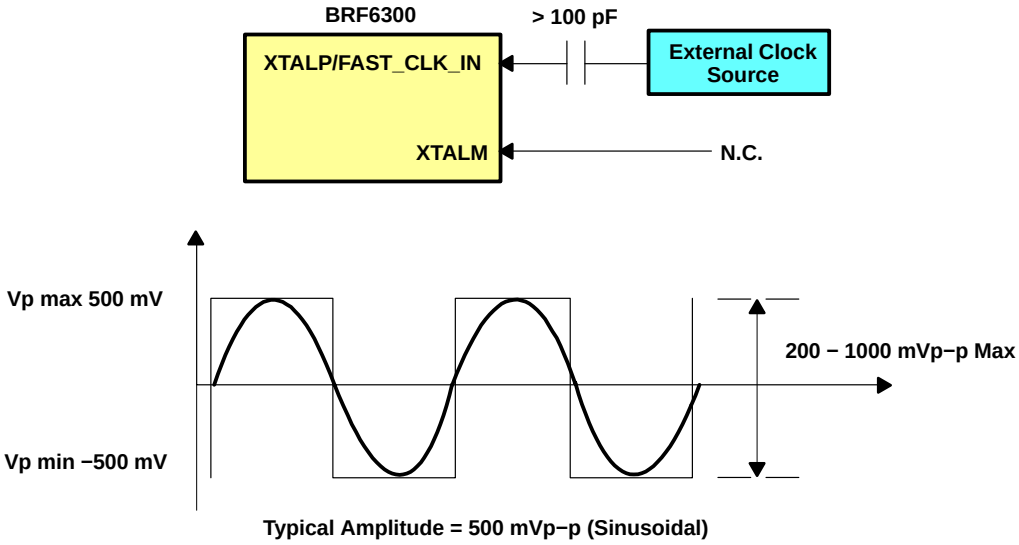
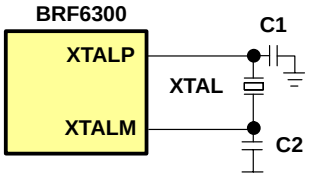


Figure 3−5. External Fast Clock (ac-Coupled)

In cases where the input amplitude is greater than 1 V, the amplitude can be reduced to be within the ac-coupled limits above by using a smaller capacitor instead of the 100-pF capacitor shown. This forms a voltage divider with the internal ~2-pF input capacitance to provide the required amplitude at the BRF6300 input.

3.3.2.3 Crystal Configuration

If an external crystal is used, it must be connected as shown in Figure 3−6.



FREQUENCY (MHz)	C1 (pF)	C2 (pF)
13	9	10
26	11	12

Figure 3−6. Fast Clock Crystal Circuit

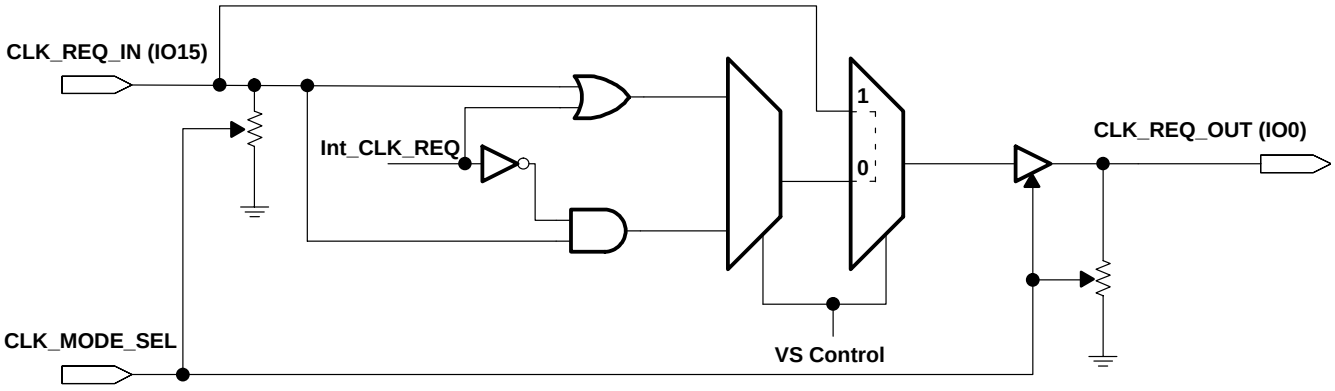
3.3.2.4 Clock Sharing With System

The BRF6300 supports the following fast clock sharing mechanism in all BRF6300 modes:

- Internal logic clock-sharing scheme. In this scheme two BRF6300 pins receive the clock request from the host and output the combined clock request (active high/low polarity): CLK_REQ_IN and CLK_REQ_OUT. An internal logic (OR/AND) allows the host to send its clock request via the BRF6300, and the BRF6300 outputs the CLK_REQ_OUT signal to the clock source (combination of the external host clock request and the BRF6300 clock request).
- Wired-OR clock-sharing scheme. Only in this scheme is the CLK_REQ_OUT signal used. The CLK_REQ_IN signal is not used and can be used as a general-purpose output.
- A third terminal, CLK_MODE_SEL, selects between these two modes.
- In both modes, the polarity of inputs and outputs are selectable via the VS command. Default is true high.
- For no sharing, CLK_MODE_SEL must be low.

NOTE:

In both clock-sharing schemes it is required that all system components using the clock source must be able to receive the clock signal at all times, even when not requesting it. This must not cause excessive power consumption or reliability issues. Figure 3−7 shows the internal BRF6300 clock-sharing concept:

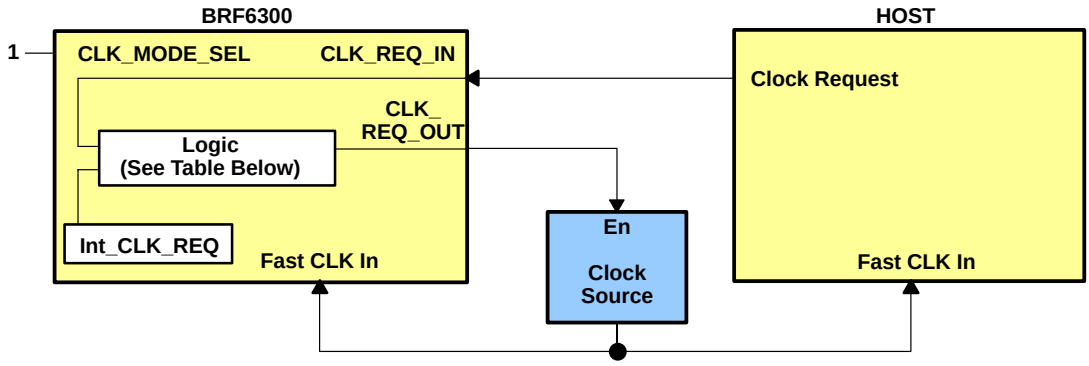


CLK_MODE_SEL Controls the PDs and Output Buffer
CLK_MODE_SEL = 0 δ PDs are enabled, Output Buffer = Dynamic
CLK_MODE_SEL = 1 δ PDs are Disabled, Output Buffer = Drive

Figure 3−7. Clock Sharing Logic Diagram

For more information, see BT−AN−0055 (BRF6300 Clock Sharing) application note.

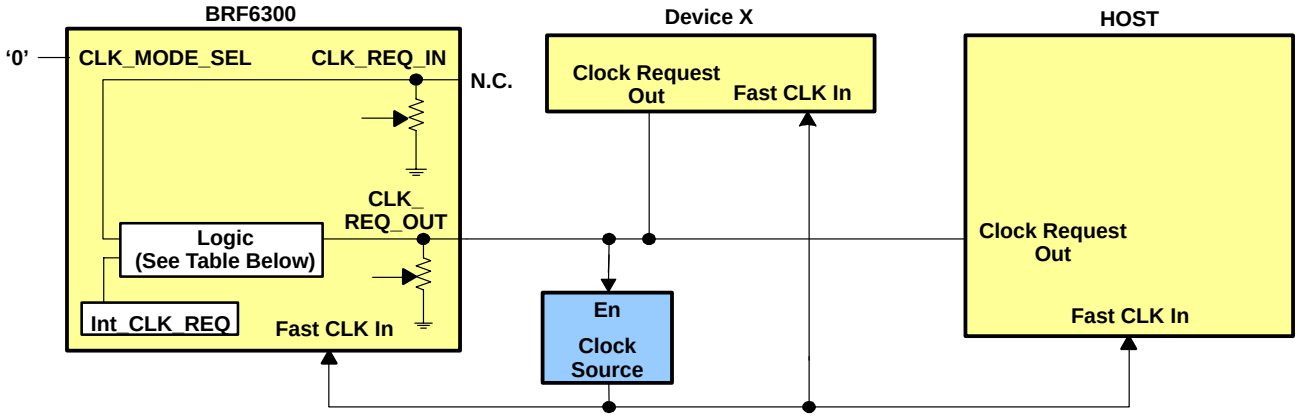
3.3.2.5 Internal Logic Clock Sharing Scheme (CLK_MODE_SEL = 1)



CLK_MODE_SEL=1: The host clock request signal is input into the BRF6300 CLK_REQ_IN terminal and combined internally with the BRF6300 internal clock request signal. The output of the logic generates the CLK_REQ_OUT which enables the clock source.

NOTE:
The internal BRF6300 clock request is only output after HCI_VS_Configure_Clock_Sharing is sent.

3.3.2.6 Wired-OR Clock Sharing Scheme (CLK_MODE_SEL = 0)



In this method, the clock sharing is implemented by using a wired-OR mechanism.

CLK_MODE_SEL=0: During shutdown mode, CLK_REQ_OUT is hi-Z with the pulldown enabled. When exiting from shutdown mode, the BRF6300 drives high on CLK_REQ_OUT and disables its pulldown.

The host clock request output signal is connected to the BRF6300 CLK_REQ_OUT pin (and to possibly other devices' clock requests out). Whenever a clock is required by the BRF6300 or the host (or other devices), it asserts its clock request output pin high to enable the clock source.

3.3.2.7 Clock-Sharing Summary

Table 3−4 summarizes the BRF6300 clock sharing signals behavior:

Table 3−4. Clock Sharing Signals Behavior Summary

MODE	CLOCK SHARING SCHEME	BRF6300 CLOCK (INT)	CLK_ REQ_IN	CLK_ REQ_OUT	NOTES
Shutdown	Wired OR (CLK_MODE_SEL = L)	Clk not req	N/C + PD	Hi-Z + PD	
		Clk not req	H + PD	H	Not recommended
	Internal logic (CLK_MODE_SEL = H)	Clk not req	L	L	No internal PDs enabled in this mode
		Clk not req	H	H	
Active or deep sleep	Wired OR (CLK_MODE_SEL = L)	Clk not req	N/C + PD	Hi-Z + PD	CLK_REQ_IN can be used as GPIO.
		Clk req	N/C + PD	H	
	Internal logic (CLK_MODE_SEL = H)	Clk not req	L	L	No internal PDs enabled in this mode. Polarity of external input and output can be changed via the VS command. Default = not inverted. *** Not after shutdown** HCI_VS_Configure_Clock_Sharing must first be sent.
		Clk not req	H	H	
		Clk req	L *	H *	
		Clk req	H	H	

All PDs are internal to the BRF6300.

3.4 BRF6300 Shutdown

The nSHUT_DOWN signal puts the BRF6300 in ultralow-power mode and also performs an internal reset to the device. nSHUT_DOWN must be applied for a minimum of 5 ms.

All I/O pins are set to the high impedance state during shutdown and power up of the BRF6300 device to prevent conflicts with external signals. The internal pull resistors are enabled on each of the I/O pins as described in the terminal function section.

The power-on reset duration can take between 2.5 to 7.5 ms.

3.5 UART/SDIO/BTSPI—HCI Transport Layers

3.5.1 Introduction

The BRF6300 incorporates one UART/SDIO/BTSPI module dedicated to the HCI transport layer. The HCI interface transports commands, events, ACL, and synchronous data between the Bluetooth device and its host using HCI data packets. The BRF6300 supports the following HCI transport layers (detected automatically when communication starts):

- UART four-wire (H4) or three-wire (H5)
- SDIO
- BTSPI

The three interfaces are multiplexed on BRF6300 as follows:

Table 3−5. Transport Layer Pin Multiplexing

UART	SDIO 1-bit	BTSPI
IO7	SDIO_CLK (I)	BTSPI_CLK (I)
HCI_RX (I)	SDIO_CMD (B)	BTSPI_DI (I)
HCI_CTS (I)	SDIO_IRQ (O)	BTSPI_CS (I)
HCI_RTS (O)	SDIO_IRQ (O)	BTSPI_IRQ (O)
HCI_TX (O)	SDIO_DATA (B)	BTSPI_DO (O)

NOTES: 1. I − Input, O − Output, B − Bidirectional
2. SDIO_IRQ output on both E7 and E8

3.5.2 UART HCI Transport Layers

The HCI transport layers support most baud rates (including all PC rates) for all fast clock frequencies—up to a maximum baud rate of 4 Mbaud. However, some exceptions exist—see the TI Baudrate Calculator utility.

After powerup, the baud rate is set for 115.2 Kbaud, irrespective of fast clock frequency. The maximum baud rate deviation supported is +1.5%, −2.5%.

The baud rate can thereafter be changed with a VS command. The BRF6300 responds with a command complete event (still at 115.2 Kbps) after which the baud rate change takes place. The only parameter needed is the desired baud rate.

HCI hardware includes the following features:

- Supports standard PC baud rates, or any other baud rate
- Receiver detection of break, idle, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTR/RTS hardware flow control

Table 3−6. UART Default Setting

PARAMETER	VALUE
Bit rate	115.2 Kbps
Data length	8 bits
Stop bit	1
Parity	None

There are two possible logical transport layers available in the UART mode:

- 4 wire (H4)
- 3 wire (H5)

The BRF6300 automatically detects the transport layer required by the host.

3.5.2.1 UART 4-Wire Interface—H4

The interface includes four signals: TXD, RXD, CTS, and RTS. Flow control between the host and the BRF6300 is per byte (CTS/RTS).

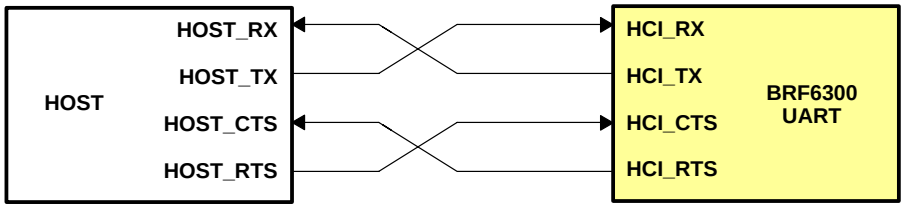


Figure 3−8. HCI UART Connection

Flow control is obtained by the following:

When hardware flow control is used, the UART, CTS, and RTS are responsible for flow control during reception/transmission of data. When the UART RX buffer of the BRF6300 passes the flow control threshold, it sets the UART_RTS signal high to stop transmission from the host.

When the UART_CTS signal is set high, the BRF6300 stops its transmission on the interface. In case HCI_CTS is set high in the middle of transmitting a byte, the BRF6300 finishes transmitting the byte and then stops the transmission.

3.5.2.2 UART 3-Wire Interface—H5

This interface consists of three signals: TXD, RXD, and GND. XON/XOFF software flow control is normally used.

Table 3−7. 3-Wire HCI UART Interface

PIN NAME	DESCRIPTION
HCI RXD	Receive data on the UART interface
HCI TXD	Transmit data on the UART interface
GND	Ground

The BRF6300 also supports a four-wire mode for H5, where hardware flow control can be achieved using RTS/CTS.

Because the same UART module is used for the 3- and 4-wire HCI UART interface, all features supported by the 4-wire interface are also supported for the 3-wire interface.

H5 features:

- Flow control (configured with HCI_VS command): software (XON/XOFF), hardware (RTS/CTS), none
- Power management
- Configurable timers for retransmission management
- CRC

3.5.3 SDIO HCI Transport Layer

The BRF6300 includes an additional module to implement the Secure Digital Input/Output (SDIO) interface. The following SDIO slave interfaces are supported:

- SDIO 1-bit SD mode
- TI-specific shared SDIO interface for multiple devices (glueless interface to TNETW1251 WLAN device)
- Up to 20-MHz external clock rate
- Maximum number of data bytes transferred in one transaction: 128 bytes
- Status registers available to host

Figure 3−9 shows the SDIO interface signals.

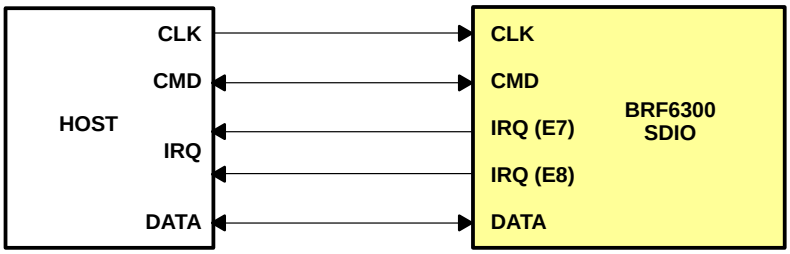


Figure 3−9. SDIO Interface Description

SDIO_IRQ is output on both E7 and E8 pins. This provides the following options to the host:

- Use E7 only: E7 first goes low as chip-initialization-complete signal. Thereafter, E7 functions as SDIO_IRQ. Note that in this scheme, SDIO_IRQ is low initially, even though the BRF6300 may not want to interrupt the host.
- Use E7 and E8: E8 is used as SDIO_IRQ. E7 is used as chip-initialization-complete signal. Note, however, that E7 does not remain low, but toggles as SDIO_IRQ signal as well.

Both E7 and E8 are set high after the device is powered. Only E7 goes low to indicate device initialization is complete.

3.5.4 BTSPI HCI Transport Layer

The BTSPI is TI's implementation of the SPI interface in the BRF6300.

Figure 3−10 shows the BTSPI interface signals to the host:

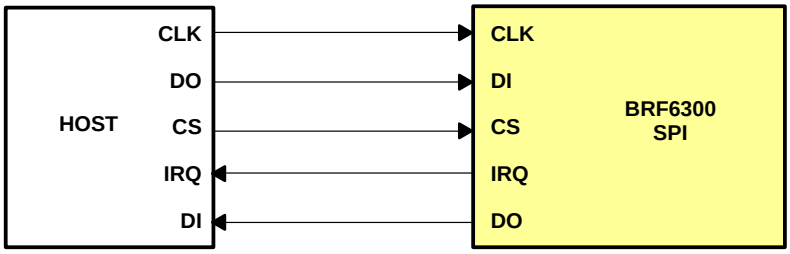


Figure 3−10. BTSPI Interface Description

During reset all outputs are in high impedance mode with pull resistors enabled.

3.5.4.1 General Features

- The interface includes a deep sleep protocol.
- The transport layer used is H4.
- Supports BTSPI clock rates from 0 to 13 MHz.
- The protocol is half-duplex and does not require simultaneous operation of DI and DO.
- The BRF6300 is a slave in this protocol and all transactions are initiated by the host.
- All data is 16-bit aligned.
- A single BTSPI read/write transaction includes a full HCI packet.
- The number of bytes for each BTSPI transaction is always even. Odd numbers are padded with one byte at the end of the HCI packet and will not be reflected in the HCI header (H4 packet length ignores this byte).
- The polarity of the clock used by the BTSPI protocol can be switched by initiating a vendor-specific command through the BTSPI interface. The switching command is sent using the default clock polarity and then switched for subsequent transactions.

For more information, see BT−AN−0058 (BRF6300 BTSPI Interface) application note.

3.6 General-Purpose I/O (ARMIO)

The BRF6300 device includes several configurable general-purpose I/O pins. These pins are controlled through the ARM and can be configured by using a vendor-specific command. Each GPIO has a default function and value.

Some of these pins are multiplexed with other peripheral pins (I^2C, WLAN, clock request, etc.).

See Section 2.10 for all IO pins and the signals that can be multiplexed on these pins.

3.7 Audio Codec Interface

3.7.1 Overview

The codec interface is a fully dedicated programmable serial port that provides the logic to interface to several kinds of PCM or I2S codecs. The interface supports:

- Two voice channels
- Master/slave modes
- μ-Law, A-Law, linear coding schemes
- Variable frame frequency
- Different data sizes, order and positions
- High-rate PCM interface for EDR
- Enlarged interface options to support a wider variety of codecs
- PCM bus sharing

3.7.2 PCM Hardware Interface

The PCM interface is a 4-wire interface. It contains the following lines:

- Clock—configurable direction (input or output)
- Frame sync—configurable direction (input or output)
- Data In—input
- Data Out—output/tri-state

The Bluetooth device can be either the master of the interface where it generates the clock and the frame-sync signals or the slave where it receives these two signals. The PCM interface is fully configured by means of a VS command.

For slave mode, clock input frequencies of up to 16 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.

For master mode, the BRF6300 can generate any clock frequency between 64 kHz and 4.096 MHz.

3.7.3 Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits, in 1-bit increments, when working with two channels, or up to 640 bits when using 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable in with 1 clock (bit) resolution and can be set independently (relative to the edge of the frame sync signal) for each channel.
- The Data_In and Data_Out bit order can be configured independently. For example; Data_In can start with MSB while Data_Out starts with LSB. Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample sizes up to 24 bits.
- The data in and data out size do not necessarily have to be the same length.
- The Data_Out line is configured to hi-Z output between data words. Data_Out can also be set for permanent hi-Z, irrespective of data out. This allows BRF6300 to be a bus slave in a multislave PCM environment. At power up, Data_Out is configured as hi-Z.

3.7.4 Frame Idle Period

The codec interface has the capability for frame idle periods, where the PCM clock can take a break and become 0 at the end of the PCM frame after all data has been transferred.

The BRF6300 supports frame idle periods both as master and slave of the PCM bus.

When BRF6300 is the master of the interface, the frame idle period is configurable. There are two configurable parameters:

- Clk_Idle_Start. Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock will become 0.

- Clk_Idle_End. Indicates the time from the beginning of the frame until the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

For example, for PCM clock rate = 1 MHz, frame sync period = 10 kHz, Clk_Idle_Start = 60, Clk_Idle_End I = 90:

Between every 2 frame syncs there will be 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and will last 90 − 60 = 30 clock cycles. This means that the idle period will end 100 − 90 = 10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.

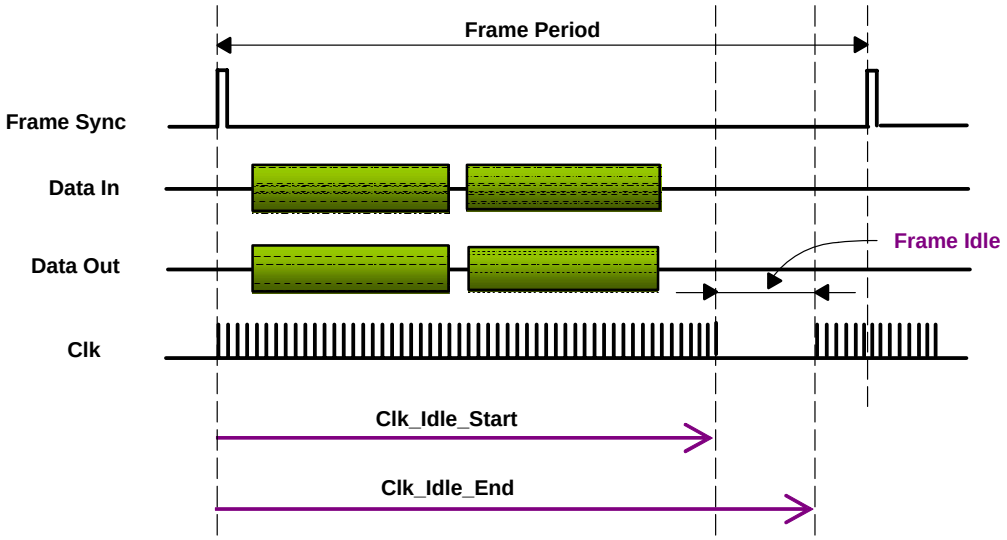


Figure 3−11. Frame Idle Period

3.7.5 Clock-Edge Operation

The codec interface of the BRF6300 can work on the rising or falling edge of the clock. It also has the ability to sample the frame sync and data at inversed polarity.

Figure 3−12 shows operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame sync signal is updated (by the codec) on the falling clock edge and therefore is sampled (by the BRF6300) on the next rising clock. The data from the codec is sampled (by the BRF6300) on the clock falling edge.

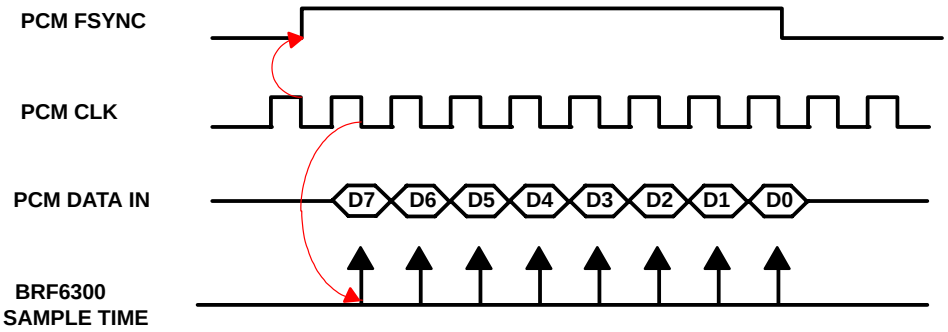


Figure 3−12. Negative Clock Edge PCM Operation

3.7.6 Two-Channel PCM Bus Example

In Figure 3−13, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus frame. (FT stands for Frame Timer)

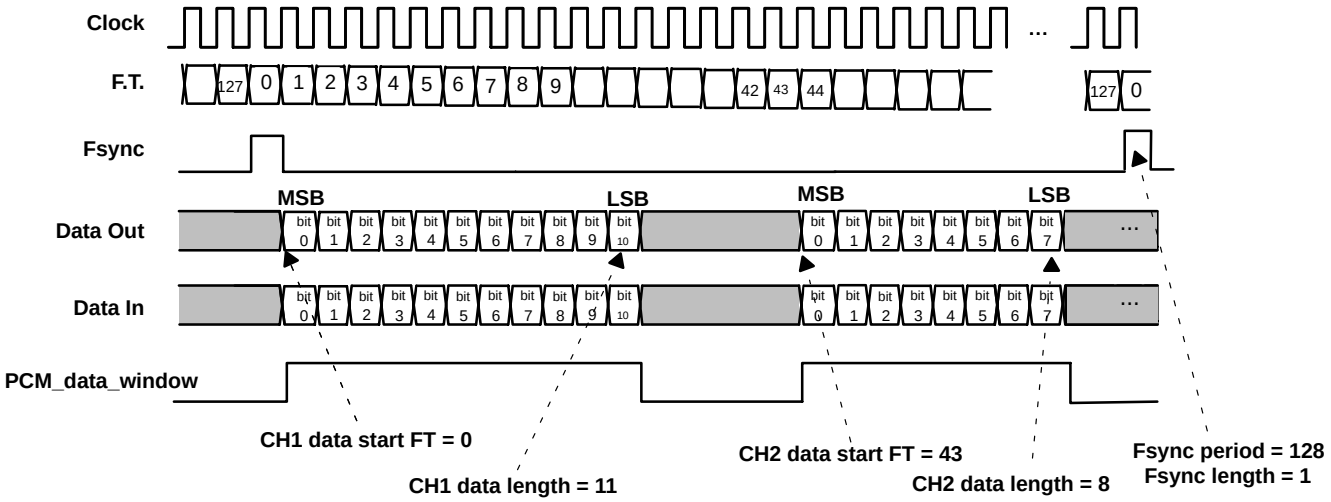


Figure 3−13. Two-Channel PCM Bus Timing

3.7.7 Audio Encoding

The BRF6300 codec interface can use one of four audio coding patterns:

- Law (8-bit)
- µLaw (8-bit)
- Linear (8- to 16-bit)

3.7.8 Improved Algorithm For Lost Packets

The BRF6300 features an improved algorithm for improving voice quality when the received voice data packets go missing. There are two options:

- Repeat the last sample—possible only for sample sizes up to 24 bits. For sample sizes >24 bits, the last byte is repeated.
- Repeat a configurable sample of 8 to 24 bits (depends on the real sample size), to simulate silence (or anything else) in the PCM bus. The configured sample is written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

3.7.9 BT/PCM Clock Mismatch Handling

In BT RX, the BRF6300 receives RF voice packets and writes these to the codec I/F. If the BRF6300 receives data faster than the codec I/F output allows, an overflow occurs. In this case, the BT has two possible behavior modes: allow overflow and don't allow overflow.

If overflow is allowed, the BT continues receiving data and overwrites any data not yet sent to the codec.

If overflow is not allowed, the RF voice packets received when the buffer is full are discarded.

3.7.10 Inter-IC Sound (I2S)

The BRF6300 can be configured as an inter-IC sound (I2S) serial interface to an I2S codec device. The BRF6300 audio codec interface is configured as a bidirectional, full-duplex interface, with 2 time slots per frame: Time slot 0 is used for the left channel audio data and time slot 1 for the right channel audio data. Each time slot is configurable up to 40 serial clock cycles in length and the frame is configurable up to 80 serial clock cycles in length.

3.7.11 UDI Support

The UDI profile defines the protocols and procedures that are used by devices implementing UDI for the 3G mobile phone systems; for example, a device with Bluetooth connection to a 3G handset communicating via videophone over a 3G network. Up to two channels of UDI data can be supported. The data is transferred via the codec interface using transparent mode and is sent out using eSCO EV4 Bluetooth packets (EV5 is also selectable).

3.8 Low-Power Mode Protocols

The BRF6300 device includes a mechanism that handles the transition between the operating mode and the deep sleep low-power mode. The protocol is performed via the UART and is known as eHCILL (enhanced HCI low level) power-management protocol.

This protocol is backward compatible with the BRF6150 HCILL protocol, so a host that implements the HCILL for BRF6150 does not need to change anything to work with the BRF6300. The enhanced portion of the HCILL introduces changes that allow a simpler host implementation of this protocol.

See BT−SW−0024 (*BRF Enhanced HCILL 4-Wire Power Management Protocol*) application note.

In addition to the HCILL protocol, the BRF6300 also supports the power-management schemes inherent in the UART H5, SDIO, and BTSPI transport layers.

3.9 BRF6300 BT Key Features

3.9.1 General

The BRF6300 implements the Bluetooth protocol stack up to the HCI layer. This software stack incorporates the link controller (LC), link manager (LM), host controller interface (HCI), and the HCI transport layer as shown in Figure 3−14.

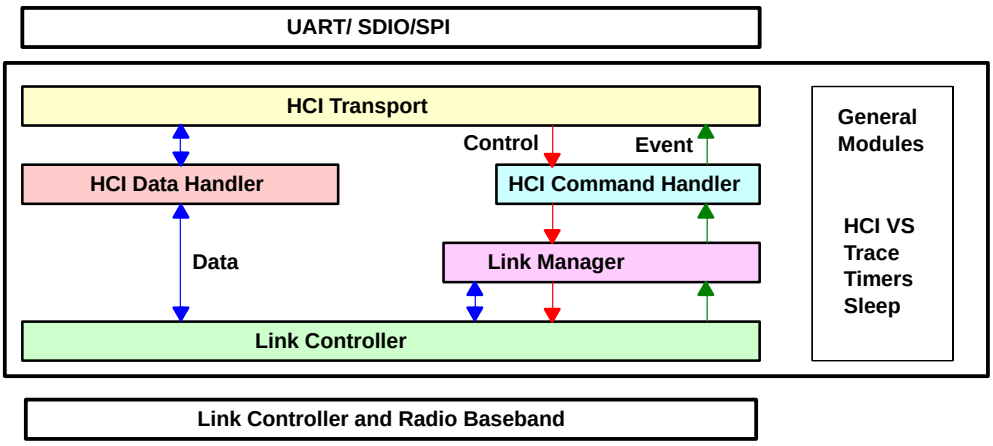


Figure 3−14. BRF6300 Software Stack

3.9.2 Features

The BRF6300 firmware supports all the features described in Bluetooth Specifications 1.1, 1.2, and 2.0 (including EDR 2 or 3 Mbps). All standard BT features are supported, such as:

- Firmware implements all lower layers up to HCI (link controller, link manager, host controller interface, and UART transport layer)
- Point-to-point and point-to-multipoint connection

- Scatternet: up to three piconets simultaneously
- Up to seven active devices
- Up to two SCO links
- Voice over HCI
- All packet types
- Pairing, authentication, encryption, inquiry, inquiry-scan, page, page-scan, hold, sniff, park, M/S switch, broadcast, QoS, test mode, flow specification, and flush timeout
- Sound: All BT formats
- Class 1−3 power control
- RSSI − range of −88 to −20 dBm with accuracy of 3 dB
- Faster connection: First FHS, interlaced page scan, interlaced inquiry scan, RSSI
- Adaptive frequency hopping: hopping kernel that supports several hopping sets, channel classification as master or slave

For more information, see BT−RN−0024 (BRF6300 Firmware Release Note).

3.9.3 High Performance Scatternet Capabilities

The BRF6300 can participate in up to three piconets simultaneously—in one piconet as the master and in the other two as slaves. Two voice channels on two different piconets, are supported.

The new scatternet architecture inherent in the BRF6300 has three independent Bluetooth clocks running simultaneously. One is the local clock (the piconet clock where the device is master) and two remote (or network) clocks.

The three clocks are implemented in hardware to enable the BRF6300 to quickly switch between networks, with minimum bandwidth waste. Network switching is done automatically using the tightest timing possible. Information to and from the different piconets can be transferred without the ARM processor resources. Network switching is accomplished according to the scheduling mechanism, configured by the software, according to the QoS requirements for each network. In this way, the BRF6300 architecture assures optimal bandwidth utilization and best performance.

3.10 Support for Class 1 Applications

The BRF6300 supports Class 1 applications using an external power amplifier (PA).

Support is provided for digitally-controlled external PAs—selectable by VS command.

The BRF6300 supports different control levels for the external PA, on a per-handle basis.

3.10.1 Improvements from BRF6150

- Dynamic path selection (Class1−2 switching) per handle is supported.
- New VS commands allow easier user implementation with their specific external PA.

3.10.2 Digital Control of External PA

Figure 3−15 shows an example usage of the BRF6300 for a digitally-controlled external PA for Class 1 applications.

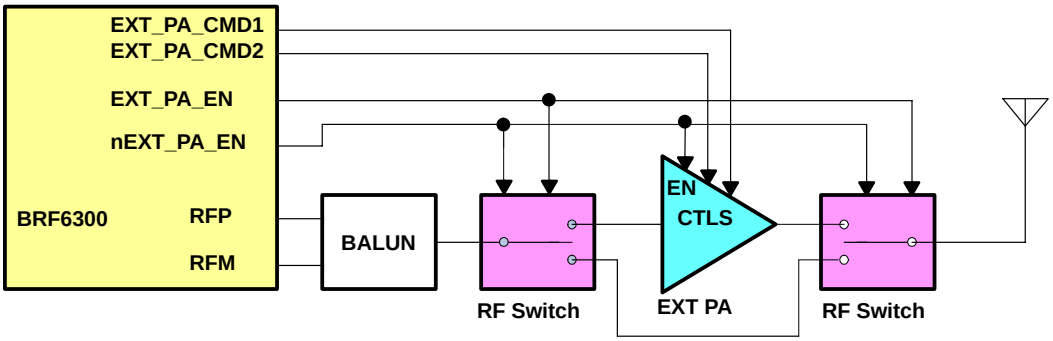


Figure 3−15. Digital Control of External PA

The following control signals are used:

- Switch control
- PA enable/disable
- EXT_PA_CMD1 and EXT_PA_CMD2 to provide four levels of digital control

3.10.3 Switch Control

The switches require two complementary control signals, one is the inverse of the other. This is achieved using an internal inverter to create nEXT_PA_EN from EXT_PA_EN.

3.10.4 PA Enable/Disable

For this purpose, one of the signals EXT_PA_EN or nEXT_PA_EN is used, according to the type of the PA (active high or active low enable pin). Because most of the known PAs in the market are active high enabled, the default value of EXT_PA_EN is low (the PA is disabled).

3.10.5 Class 1 Control Signals

The Class 1 control signals are multiplexed on the IO pins. There are several multiplexing options, as described in Table 3−8:

Table 3−8. Class 1 Control Signals

FUNCTIONALITY	IO PIN
EXT_PA_CMD1	TX_DBG, IO2, IO4, IO7, IO16, IO17
EXT_PA_CMD2	TX_DBG, IO3, IO7, IO14, IO15, IO17
EXT_PA_EN	IO1, IO2, IO14
nEXT_PA_EN	TX_DBG, IO3, IO4, IO15, IO16
PA_CTRL	Reserved

For more detailed design information, see BT-AN-0051 (BRF6300 Class 1 implementation) application note.

3.11 Wireless LAN Interoperability

3.11.1 General Description

The BRF6300 WLAN interface offers the capability of simultaneous and efficient use of the 2.4-GHz bandwidth for Bluetooth and WLAN applications. For example, Bluetooth voice connection at the same time as WLAN data transfer such as WEB browsing. The coexistence mechanism is a collaborative solution between the BRF6300 and WLAN devices, using time division multiplexing and other means to allocate the bandwidth between the two devices and to minimize interference between the WLAN and BT RF signals. This results in a user perception of simultaneous operation of BT and WLAN traffic.

The coexistence mechanism supports both separate antennas or a shared antenna between the BT and WLAN devices.

The BRF6300 supports TI proprietary SG2.0 (Soft Gemini 2.0) and several customer-specific WLAN coexistence interfaces. The BRF6300 will work seamlessly with all TI WiLink 4.0 devices such as WL1251 and WL1253 WLAN devices.

3.11.2 SG2.0 Block Diagram

Four signals support Bluetooth and WLAN coexistence: Two signals inform the WLAN about the Bluetooth real-time status and one signal is used by the WLAN to enable the Bluetooth RF transmission. One signal is reserved for future use.

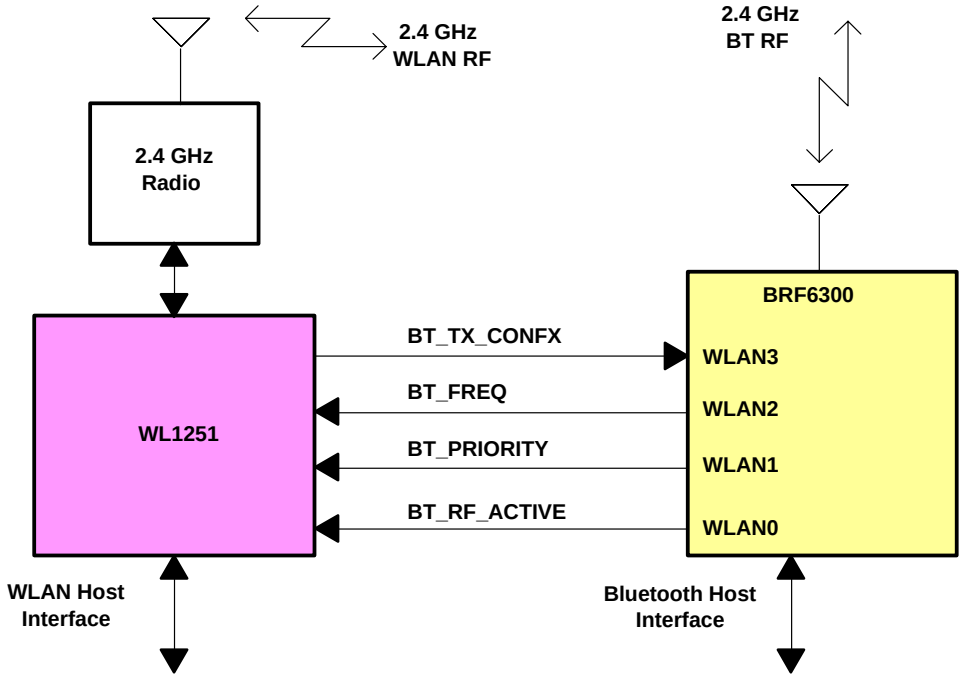


Figure 3−16. SG2.0 BT/WLAN Interface

3.11.3 SG2.0 Signal Description

Table 3−9. BRF6300 BT/WLAN Interface Signals

IO PIN OPTIONS	FUNCTIONALITY	DESCRIPTION	DIRECTION
IO1 TX_DBG(1)	BT_TX_CONFX (RF shutdown, WLAN3)	When asserted, this signal disables the internal PA of the BRF6300. When the signal is not asserted, the PA state is control by the internal BRF6300 logic. When the BRF6300 is attempting to transmit (as indicated by BT_RF_ACTIVE being valid), and BT_TX_CONFX is asserted, the BRF6300 will finish to transmit the current packet and only then will shut off the PA. The polarity (active high/low) is set by a vendor-specific command.	WLAN to BT
IO4 IO15	BT_PRIORITY (Priority Data, WLAN1)	This signal is dual-purpose: A 20-µs pulse indicates immediately after RF_ACTIVE goes high indicates that a priority data transaction is about to occur or is occurring on the Bluetooth link. This signal is used for high priority traffic, such as voice, high priority ACL, page, inquiry, and sniff. As an improvement over the BRF6150, the BRF6300 allows ACL links to be set as priority data, on a per-handle basis. Thereafter, the signal provides TX/RX indication (high if TX).	BT to WLAN
IO2, IO4, IO5, IO7, IO14, IO17	BT_RF_ACTIVE (RF active, WLAN0)	This signal is active when the BT frame begins on or when the BRF6300 is receiving. There is a configurable option to set this line only when the current frame frequency is a WLAN frequency.	BT to WLAN
IO2, IO3 TX_DBG IO14, IO16	BT_FREQ (WLAN2)	Reserved for future use	BT to WLAN

NOTE 1: Not recommended due to PU on TX_DBG

Because the WLAN interface signals are multiplexed on the general-purpose IO pins, these pins need to be configured to WLAN functionality using VS commands.

For more information, see BT−AN−0047 (BRF6300_BRF6350 WLAN Coexistence) application note.

3.12 Die ID Device Identification

The BRF6300 includes an e-Fuse register burned during the fabrication process. This register contains configuration data such as BD address, RF trimming values, etc. Each device is separately tested and trimmed during production.

3.13 Tape-and-Reel Packing Method

The embossed tape-and-reel method is the standard way BGA and WSP packages are shipped. The tape is made from an antistatic/conductive material. The cover tape, which peels back during use, is heat-sealed to the carrier tape to keep the devices in their cavities during shipping and handling. The tape-and-reel packaging used by Texas Instruments is in full compliance with EIA Standard 481-C, *8-mm Through 200-mm Embossed Carrier Taping and 8-mm and 12-mm Punched Carrier Taping of Surface Mount Components for Automatic Handling*. The static-inhibiting materials used in the carrier-tape manufacturing provide device protection from static damage, while the rigid, dust-free polystyrene reels provide mechanical protection and clean-room compatibility with the dereeling equipment currently available on most high-speed automated placement systems.

3.13.1 Tape Format

Typical tape format is shown in Figure 3−17. The variables used in this figure and in the following table are defined as follows: W is the tape width; P is the pocket pitch; A0 is the pocket width; B0 is the pocket length; K0 is the pocket depth; K is the maximum tape depth; and F is the distance between the drive hole and the centerline of the pocket.

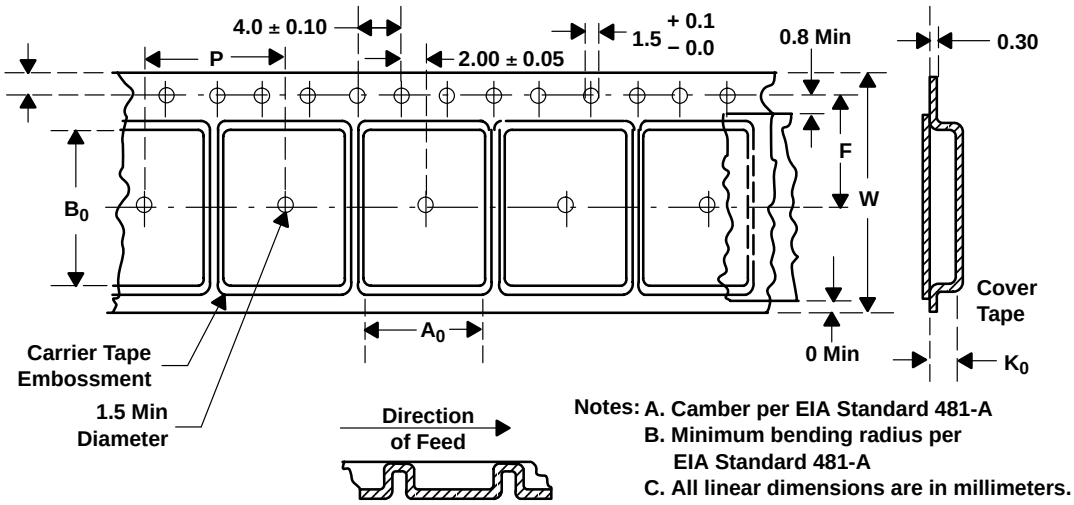


Figure 3−17. Tape Dimensions

Table 3−10. Tape Dimensions for Package Size of 4.5x4.5 (in mm)

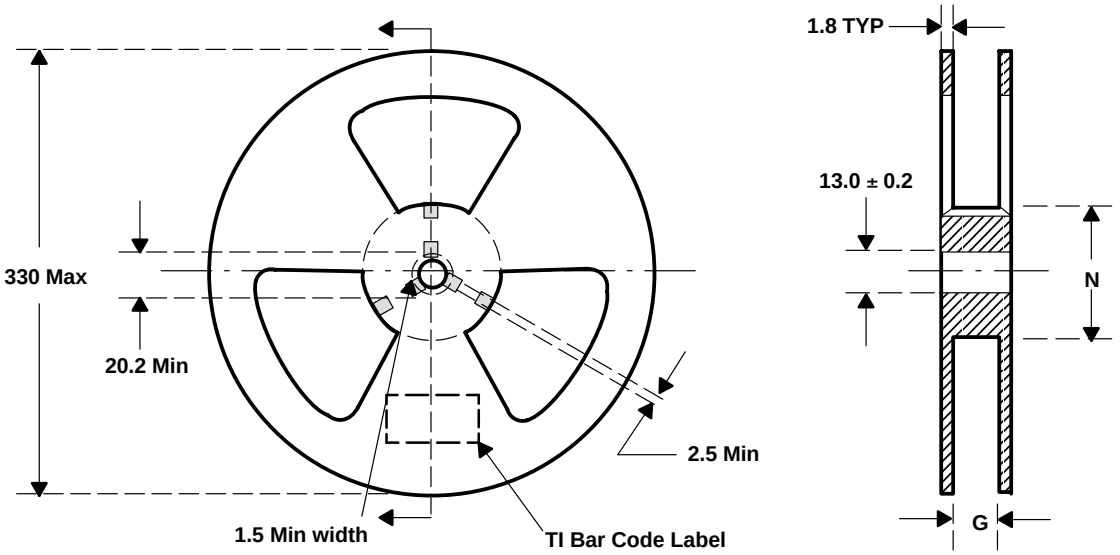
PACKAGE	TAPE WIDTH	POCKET PITCH	POCKET WIDTH	POCKET LENGTH	TAPE DEPTH	POCKET DEPTH	CENTERLINE TO DRIVE HOLE
Symbol	W	P	A0	B0	K1	K0	F
WSP	12 ± 0.3	8 ± 0.1	3.46 ± 0.1	3.46 ± 0.1		0.75 ± 0.1	5.5 ± 0.1
BGA	12 ± 0.3	8 ± 0.1	4.75 ± 0.1	4.75 ± 0.1	0.9 ± 0.1	1.6 ± 0.1	5.5 ± 0.1

Once the taping has been completed, the end of the leader is fixed onto the reel with tape. The product name, lot number, quantity, and date code are recorded on the reel and the cardboard box used for tape delivery.

Each reel is separately packed in a cardboard box for delivery.

3.13.2 Reel Dimensions

Figure 3−18 shows the reel. In this figure, G is the width of the tape, N is the diameter of the hub, and T is the total reel thickness.



Note: All linear dimensions are in millimeters.

Figure 3−18. Reel Dimensions

TAPE WIDTH (G)	REEL HUB DIAMETER (N)	PARTS PER REEL
12.4 +2/−0	100 (min)	2500

3.13.3 Reel Packing

After the parts are loaded into the reel, each individual reel is packed in its own *pizza* box for shipping, as shown in Figure 3−19.

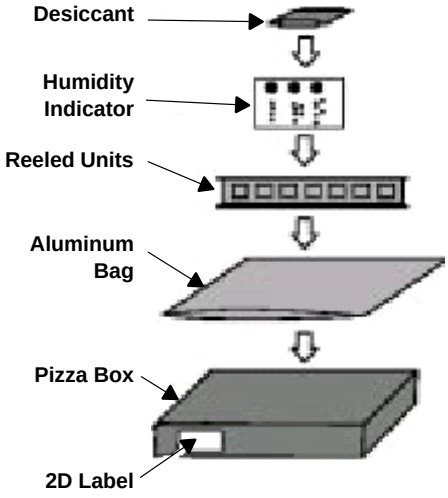


Figure 3−19. Tape and Reel Packing

3.13.3.1 Device Insertion

Devices are inserted toward the outer periphery of the tape by placing the side with the device name faces up and the side with the balls attached face down. The pin−1 indicator is placed in the top left−hand corner of the pocket, next to the sprocket holes.

3.13.3.2 Packaging Method

For reels, once the taping has been completed, the end of the leader is fixed onto the reel with tape. The product name, lot number, quantity, and date code are recorded on the reel and on the cardboard box used for tape delivery. Each reel is separately packed in a cardboard box for delivery.

Trays are packed with five loaded trays and one empty tray on top for support and to keep packages secure. The stack is secured with stable plastic straps and sealed in a moisture-proof bag.

Customer-specific bar code labels can be added under request or general purchasing specifications.

Moisture-sensitive packages are baked before packing and are packed within 8 hours of coming out of the oven. Both the tape-and-reel and the tray moisture-proof bags are sealed and marked with appropriate labeling warning that the packages inside the bags are dry-packed and giving the level of moisture sensitivity.

4 Electrical Characteristics

This device can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled using appropriate precautions. Failure to observe proper handling and installation procedures can cause damage to the device. This damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.1 Absolute Maximum Ratings

Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range: VDD_IN‡ . . . . . −0.5 V to 6.5 V
VDD_IO . . . . . −0.5 V to 2.1 V
VDD_DAC . . . . . −0.5 V to 3.3 V
Input voltage to analog pins§ . . . . . −0.5 V to 2.1 V
Input voltage to all other pins . . . . . −0.5 V to VDD_IO + 0.5 V
Operating ambient temperature range . . . . . −40°C to +85°C
Storage temperature range . . . . . −55°C to +125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Maximum allowed depends on accumulated time at that voltage: 4.9 V lifetime, 5.5 V for 10%, 6.5 V for 10 s.
§ Analog pins: RFIO pins, XTALP, XTALM

NOTE:

All parameters are supplied in the following conditions unless stated otherwise:
VDD_IN = 3.6 V, VDD_IO = 1.8 V

4.2 Recommended Operating Conditions

RATING	CONDITION	SYMBOL	MIN @ 25°C	MAX @ 25°C	MIN @ −40°C	MAX @ −40°C	MIN @ 85°C	MAX @ 85°C	UNIT
Power supply voltage(1)		VDD_IN	1.7	5.5	1.7	5.5	1.7	5.5	V
IO ring power supply voltage		VDD_IO	1.62	1.925	1.62	1.925	1.62	1.925	V
High-level input voltage		V_{IH}	0.65 x VDD_IO	VDD_IO	0.65 x VDD_IO	VDD_IO	0.65 x VDD_IO	VDD_IO	V
Low-level input voltage		V_{IL}	0	0.35 x VDD_IO	0	0.35 x VDD_IO	0	0.35 x VDD_IO	V
High-level output voltage	@ 4 mA	V_{OH}	VDD_IO − 0.45	VDD_IO	VDD_IO − 0.45	VDD_IO	VDD_IO − 0.45	VDD_IO	V
	@ 1 mA		VDD_IO − 0.25	VDD_IO	VDD_IO − 0.25	VDD_IO	VDD_IO − 0.25	VDD_IO	
Low-level output voltage	@ 4 mA	V_{OL}	0	0.45	0	0.45	0	0.45	V
	@ 1 mA		0	0.25	0	0.25	0	0.25	
Input transitions time t_R/t_F from 10% to 90% (digital IO)		t_R/t_F	0	25	0	25	0	25	ns
Output rise time from 10% to 90% (digital pins)	C_L = 10 pF	t_R		5		5		5	ns
Output fall time from 10% to 90% (digital pins)	C_L = 10 pF	t_F		5		5		5	ns
Ripple on VDD_IN, (sine wave)	1 kHz to 1 MHz			25		25		25	mVp-p
Voltage dips on VDD_IN (due to GSM polling: duration = 577 µs, period = 4.6 ms)				400		400		400	mV

NOTE 1: 5.5 V for 10% of time. Continuous = 4.9 V

4.3 Electrical Characteristics

CHARACTERISTICS	MIN @ 25°C	TYP @ 25°C	MAX @ 25°C	MIN @ −40°C	TYP @ −40°C	MAX @ −40°C	MIN @85°C	TYP @ 85°C	MAX @ 85°C	UNIT
Current consumption in shutdown mode(1)		5	8		5			5		µA
VDD_IN current during deep sleep		20	80		15			200		µA
nSHUT_DOWN pin current during active and deep sleep		20	28		20			20		µA
Total IO leakage current		1	3			5			5	µA
IO terminals pull resistor current	10	20	34	10	20	34	10	20	34	µA
IO terminals input capacitance			2.8			2.8			2.8	pF

NOTE 1: Excluding IO currents

4.4 nSHUT_DOWN Requirements

PARAMETER	SYM	MIN @ 25°C	MAX @ 25°C	MIN @ −40°C	MAX @ −40°C	MIN @ 85°C	MAX @ 85°C	UNIT
Operation mode level(1)	V_{IH}	1.45	3.6	1.45	3.6	1.45	3.6	V
Shutdown mode level(1)	V_{IL}		200		200		200	mV
Minimum time for nSHUT_DOWN low		5		5		5		ms
t_R / t_F			20		20		20	µs

NOTE 1: Internal pulldown retains shutdown mode when no external signal is applied to this pin

4.5 External Fast Clock (f_{REF}) Input (−40°C to 85°C)

CHARACTERISTICS		CONDITION		SYM	MIN	TYP	MAX	UNIT
Supported frequencies				f_{REF}	12, 13, 19.2, 19.44, 26			MHz
Reference frequency accuracy(1)		Initial + temperature + aging					±20	ppm
Fast clock input voltage limits Sine or square wave		dc-coupled	Amplitude		0.2		1.5	Vp-p
			Limits		0		1.5	V
		ac-coupled amplitude			0.2		1.0	Vp-p
f_{REF} input impedance	19.2 MHz	Input resistance		R_P		25		kΩ
		Input capacitance		C_P		2.5		pF
	26 MHz	Input resistance		R_P		22		kΩ
		Input capacitance		C_P		2.5		pF
Duty cycle					36%	50%	64%	
Jitter							40	pSRMS
Phase noise	13 MHz	@ offset = 1 kHz					−125	dBc/Hz
		@ offset =10 kHz					−131	
		@ offset =1 MHz					−135	
	26 MHz	@ offset = 1 kHz					−120	
		@ offset =10 kHz					−126	
		@ offset =1 MHz					−130	

NOTE 1: See description of the maximum initial frequency accuracy (up to ±150 ppm) in the fast clock section

4.6 External Fast Clock Crystal

CHARACTERISTICS	CONDITION	SYM	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	UNIT
Supported frequencies		f_{IN}	12, 13, 19.2, 19.44, 26									MHz
Frequency accuracy(1)	Initial + temp + aging				±20			±20			±20	ppm
Crystal negative resistance	13 MHz, C_L = 8 pF, I_{OSC} = 300 µA			800			800			800		Ω
Phase noise of internal oscillator	@ offset ≥ 1 kHz				−120			−120			−120	dBc/Hz
	@ offset ≥10 kHz				−135			−135			−135	

NOTE 1: See description of the maximum initial frequency accuracy (up to ±150 ppm) in the fast clock section

4.7 External Digital Slow Clock

CHARACTERISTICS	CONDITION	SYM	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	UNIT
Input slow clock frequency				32768			32768			32768		Hz
Input slow clock accuracy	Initial + temperature + aging				±250			±250			±250	ppm
Input transition time t_R / t_F from 10% to 90%		t_R / t_F			10			10			10	µs
Frequency input duty cycle			15%	50%	85%	15%	50%	85%	15%	50%	85%	
Slow clock input voltage limits	Square wave	V_{IH}	0.9		3.6	0.9		3.6	0.9		3.6	V
		Vil	0		0.4	0		0.4	0		0.4	V

NOTE:

For the following RF testing:
All f_{REF} dependant parameters in sections 4.8 to 4.21 below are verified at the following fast clock frequencies: 12, 13, 19.2, 19.44, 26 MHz.
All measurements given at device pins of TI EVB test board, unless otherwise indicated.
All specifications over process and voltage.

4.8 Receiver Characteristics—In-band Signals

CHARACTERISTIC	CONDITION	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
Operation frequency range		2402		2480	2402		2480	2402		2480		MHz
Channel spacing			1			1			1			MHz
Sensitivity, (1, 2)	GFSK, BER = 0.1%	−82	−85		−82	−85		−82	−85		−70	dBm
	Pi/4−DQPSK, BER = 0.01%	−82	−85		−82	−85		−82	−85		−70	
	Pi/4−DQPSK, BER error floor = 0.001%	−75	−77		−75	−77		−74	−76		−60	
	8DPSK, BER = 0.01%	−74	−80		−74	−80		−74	−80			
	8DPSK, BER error floor = 0.001%	−73	−77		−73	−77		−73	−76			
Maximum useable input power	GFSK, BER = 0.1%	−10	−5		−10	−5		−10	−5		−20	dBm
	Pi/4−DQPSK, BER = 0.1%	−10	−5		−10	−5		−10	−5			
	8DPSK, BER = 0.1%	−10	−5		−10	−5		−10	−5			

CHARACTERISTIC	CONDITION		MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
C/I performance Note: Numbers show wanted signal to interfering signal ratio. Smaller numbers indicate better C/I performance. For > 3 MHz: Five exceptions allowed in BT 2.0 spec. BRF6300 passes with two exceptions.	GFSK, Cochannel			9	11		9	11		9	11	11	dB
	EDR, Cochannel	Pi/4−DQPSK		11	13		11	13		11	13	13	
		8DPSK		19	21		19	21		19	21	21	
	GFSK, adjacent + 1 MHz (image)			−8	−3		−8	−3		−8	−3	0	
	EDR, adjacent +1 MHz, (image)	Pi/4−DQPSK		−8	−3		−8	−3		−8	−3	0	
		8DPSK		−2	2		−2	2		−2	2	5	
	GFSK, adjacent − 1 MHz			−8	−5		−6	−3		−8	−5	0	
	EDR, adjacent −1 MHz	Pi/4−DQPSK		−8	−4		−6	−2		−8	−4	0	
		8DPSK		−6	−1		−4	1		−6	−1	5	
	GFSK, adjacent −2 MHz			−35	−33		−35	−33		−35	−33	−30	
	EDR, adjacent −2 MHz	Pi/4−DQPSK		−35	−33		−35	−33		−35	−33	−30	
		8DPSK		−33	−28		−33	−28		−33	−28	−25	
	GFSK, adjacent + 2 MHz, (image + 1 MHz)			−25	−23		−25	−23		−25	−23	−20	
	EDR, adjacent +2 MHz (image + 1 MHz)	Pi/4−DQPSK		−25	−23		−25	−23		−25	−23	−20	
		8DPSK		−23	−18		−23	−18		−23	−18	−13	
	GFSK, adjacent +3 MHz, (image + 2 MHz)			−46	−40		−45	−40		−47	−41	−40	
	EDR, adjacent +3 MHz, (image + 2 MHz)	Pi/4−DQPSK		−47	−40		−47	−40		−47	−40	−40	
		8DPSK		−40	−36		−40	−36		−40	−36	−33	
	GFSK, adjacent − 3 MHz			−45	−42		−45	−42		−45	−42	−40	
	EDR, adjacent −3 MHz	Pi/4−DQPSK		−45	−42		−45	−42		−45	−42	−40	
		8DPSK		−40	−36		−40	−36		−40	−36	−33	
	GFSK, Adjacent > 3 MHz			−45	−42		−45	−42		−45	−42	−40	
	EDR, adjacent > 3 MHz	Pi/4−DQPSK		−45	−42		−45	−42		−45	−42	−40	
		8DPSK		−40	−36		−40	−36		−40	−36	−33	

NOTES: 1. Possible 2-dB degradation in sensitivity for some f_{REF}s. for example, 19.44. No degradation for f_{REF}s 19.2, 26 MHz. Others TBD.
2. Sensitivity degradation up to −75 dBm may occur for up to three BT channels where an odd number multiplied by f_{REF} falls within the BT range, for example, 26 MHz x 93 = 2418 MHz

4.9 Receiver Characteristics—Blocking Measurements A

CHARACTERISTICS	CONDITION	MIN +25°C	TYP +25°C	MIN −40°C	TYP −40°C	MIN +85°C	TYP +85°C	UNIT
Blocking performance for various cellular standards Hopping on Wanted signal: −72dBm (GFSK & Pi/4−DQPSK), −67dBm (8DPSK) DH1 packets with modulated blocking signal BER = 0.1%, PER = 1%, For EDR, 2DH1 or 3DH1, BER = 0.1%	824−848 MHz (GSM) (1)	−9	−4	−9	−4	−9	−4	dBm
	824−848 MHz (CDMA) (2)	−6	−4	−6	−4	−6	−4	
	880−915 MHz (GSM)	−7	−3	−7	−3	−7	−3	
	1710−1910 MHz (GSM)	−16	−11	−16	−11	−16	−11	
	1710−1875 MHz (DCS)	−16	−11	−16	−11	−16	−11	
	1850−1910 MHz (PCS)	−10.5	−8.5	−10.5	−8.5	−10.5	−8.5	
	1850−1910 MHz (CDMA)	−19.5	−13.5	−19.5	−13.5	−19.5	−13.5	
	1850−1910 MHz (WCDMA)	−11.5	−6.5	−11.5	−6.5	−11.5	−6.5	
	1850−1910MHz (GSM)	−13.5	−8.5	−13.5	−8.5	−13.5	−8.5	
	1920−1980 MHz (WCDMA)	−11	−6	−11	−6	−11	−6	
	5.04−5.32 GHz (WLAN)	4	5	4	5	4	5	
	5.50−5.58 GHz (WLAN)	4	5	4	5	4	5	
	5.60−5.805 GHz (WLAN)	4	5	4	5	4	5	

NOTES: 1. Except for frequencies where [3 * F_BLOCKER] falls within the BT band (2400 MHz to 2483.5 MHz)
2. Except for frequencies in which [3 * (F_BLOCKER − BW)] falls within the BT band. BW is the channel spacing.

4.10 Receiver Characteristics—Blocking Measurements B

CHARACTERISTICS	CONDITION	MIN 25°C	TYP 25°C	MIN −40°C	TYP −40°C	MIN 85°C	TYP 85°C	UNIT
Blocking performance over full range, according to BT specification (1)	30 to 2000 MHz	−10		−10		−10		dBm
	2000 MHz to 2399 MHz	−27		−27		−27		
	2484 MHz to 3000 MHz	−27		−27		−27		
	3 GHz to 12.75 GHz	−10		−10		−10		

NOTE 1: 10 exceptions out of the total 24 allowed in the BT spec.

4.11 Transmitter PA, GFSK

CHARACTERISTICS	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
RF output power (1)	1	3.5	6	1	3.5	6	1	3.5	6		dBm
Gain control range		30			30			30			dB
Power Control Step	2	5	8	2	5	8	2	5	8	2 to 8	dB
Adjacent Channel Power |M−N| = 2		−45	−41		−45	−41		−45	−41	= −20 dBm	dBm
Adjacent Channel Power |M−N| > 2		−57	−52		−57	−52		−57	−52	= −40 dBm	dBm

NOTE 1: When the device is matched for the RX path.

4.12 Transmitter PA, EDR(1)

CHARACTERISTICS		MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
EDR output power(2)		−1	1.5	4	−1	1.5	4	−1	1.5	4		dBm
EDR rel power(3)	Pi/4−DQPSK	−2	−0.5	1	−2	−0.5	1	−2	−0.5	1	−4 to 1	dB
	8DPSK	−2	0	1	−2	0	1	−2	0	1	−4 to 1	dB
Gain control range(2)		20	30		20	30		20	30			dB
Power control step(2)		2	5	8	2	5	8	2	5	8	2 to 8	dB
Adjacent channel power |M−N| = 1(2)			−32	−28		−32	−28		−32	−28	= −26	dB
Adjacent channel power |M−N| = 2(2)			−42	−40		−42	−40		−42	−40	= −20	dBm
Adjacent channel power |M−N| > 2(2)			−46	−44		−46	−44		−46	−44	= −40	dBm

NOTES: 1. When the device is matched for the RX path
2. For both Pi/4−DQPSK and 8DPSK
3. GFSK header rel to EDR payload. For power level 7. Meets BT specification for all other power levels.

4.13 Synthesizer

CHARACTERISTICS	CONDITION	SYM	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
Operation frequency range			2402		2480	2402		2480	2402		2480		MHz

4.14 Modulation, GFSK

CHARACTERISTICS	CONDITION	SYM	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
Bit rate				1			1			1		1	MHz
−20 dB BW	GFSK			900	1000		900	1000		900	1000	=1000	kHz
Average deviation Detector bandwidth –10 MHz	Mod Data = 4−1, 4−0 11110000111 10000...	F1 avg	140	160	175	140	160	175	140	160	175	140 to 175	kHz
Instantaneous deviation	Mod data = 1010101...	F2 max	115	130		115	130		115	130		> 115	kHz
dF2/dF1			85%			85%			85%			> 80%	
Absolute carrier frequency drift	DH1				20			20			20	< 25	kHz
	DH3 & DH5			10	35		10	35		10	35	< 40	kHz
Drift rate				5	20		5	20		5	20	< 20	kHz/ 50µs
Initial carrier frequency tolerance (1)					±25			±25			±25	±75	kHz

NOTE 1: For 0 ppm fast clock

4.15 Modulation, EDR

CHARACTERISTICS	CONDITION	SYM	MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	BT SPEC	UNIT
Carrier frequency stability	(1)			3	10		3	10		3	10	10	kHz
Initial carrier frequency tolerance(2)					±25			±25			±25	±75	kHz
RMS DEVM (3,4)	Pi/4−DQPSK			8%	13%		8%	13%		8%	13%	20%	
	8DPSK			10%	13%		10%	13%		10%	13%	13%	
99% DEVM (3, 4)	Pi/4−DQPSK			13%	16%		13%	16%		13%	16%	30%	
	8DPSK			16%	20%		16%	20%		16%	20%	20%	
Peak DEVM (3, 4)	Pi/4−DQPSK			18%	35%		18%	35%		18%	35%	35%	
	8DPSK			15%	25%		15%	25%		15%	25%	25%	

NOTES: 1. For all blocks within the measured packet. Results are valid for all packet types specified in EDR RF test Specification v2.0 E2
2. For 0 ppm fast clock
3. Max performance refers to Max TX power.
4. Typical performance refers to the following TX power

4.16 Transceiver

CHARACTERISTICS	CONDITION	TYP 25°C	MAX 25°C	TYP −40°C	MAX −40°C	TYP 85°C	MAX 85°C	UNIT
Spurious emission during operation (1)	30 MHz to 1 GHz	−53	−48	−53	−48	−53	−48	dBm
	1 GHz to 12.75 GHz	−30	−25	−30	−25	−30	−25	
	1.8 GHz to 1.9 GHz	−72	−67	−72	−67	−72	−67	
	5.15 GHz to 5.3 GHz	−45	−40	−45	−40	−45	−40	
TX and RX out-of-band emission	869 to 960 MHz (CDMA, GSM)	−143	−138	−143	−138	−143	−138	dBm/ Hz
	925 to 960 MHz (GSM)	−143	−138	−143	−138	−143	−138	
	1570 to 1580 MHz (GPS)	−146	−141	−146	−141	−146	−141	
	1805 to 1990 MHz (GSM, DCS)	−140.5	−135.5	−140.5	−135.5	−140.5	−135.5	
	1930 to 1990 MHz (GSM, PCS, CDMA, WCDMA)	−140.5	−135.5	−140.5	−135.5	−140.5	−135.5	
	2010 to 2170 MHz (WCDMA)	−133.5	−128.5	−133.5	−128.5	−133.5	−128.5	
RX mode LO leakage(2)	Frf	−85	−68	−85	−68	−85	−68	dBm

NOTES: 1. As defined in Bluetooth spec with following exceptions:
350 to 500 MHz = −33 dBm for GFSK and EDR, 800 to 830 MHz = −40 dBm for GFSK and EDR, second and third harmonics = −20 dBm.
2. f_{RF} is the received RF frequency + 0.5 MHz

4.17 Audio Codec Interface

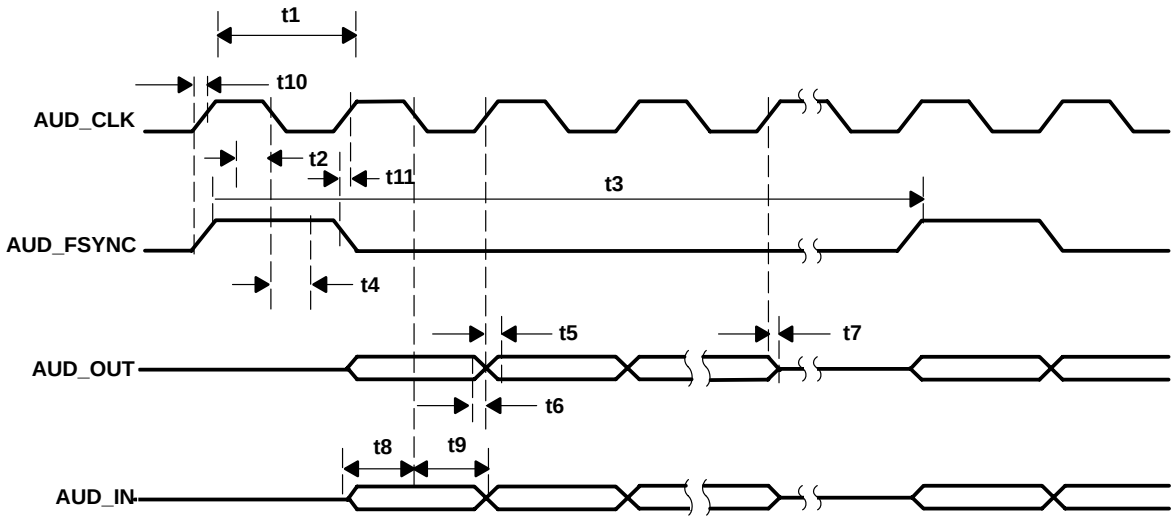


Figure 4−1. PCM Interface Timing

4.17.1 BRF6300 as PCM Master

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Master clock frequency	1/t1	64		4096	kHz
Master clock accuracy				±1	ppm
Clock jitter				1	f_{REF} clock cycle
Synchronization clock period	t3	8 x t1		65535 x t1	
Synchronization clock accuracy relative to f_{REF}				±1	ppm
Synchronization signal width		t1		65535 x t1	
Setup time for AUD_IN valid to AUD_CLK low	t8	30			ns
Hold time from AUD_CLK low to AUD_IN invalid	t9	10			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t5			10	ns
Delay time from AUD_CLK low to last data bit AUD_OUT output set to high impedance	t7			10	ns
Delay time from AUD_CLK high to AUD_FSYNC high	t10			10	ns

4.17.2 BRF6300 as PCM Slave

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Master clock frequency	1/t1	64		16000	kHz
Clock duty cycle		40%	50%	60%	
Synchronization clock period	1/t3	8 x t1		65535 x t1	
Synchronization signal width		t1		65535 x t1	
Setup time for AUD_FSYNC high to AUD_CLK low	t2	5			ns
Hold time from AUD_CLK low to AUD_FSYNC low	t4	8			ns
Setup time for AUD_IN valid to AUD_CLK low	t8	5			ns
Hold time from AUD_CLK low to AUD_IN invalid	t9	8			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t5			20	ns
Delay time from AUD_CLK low to last data bit of AUD_OUT output set to high impedance	t7			20	ns

4.18 UART Interface

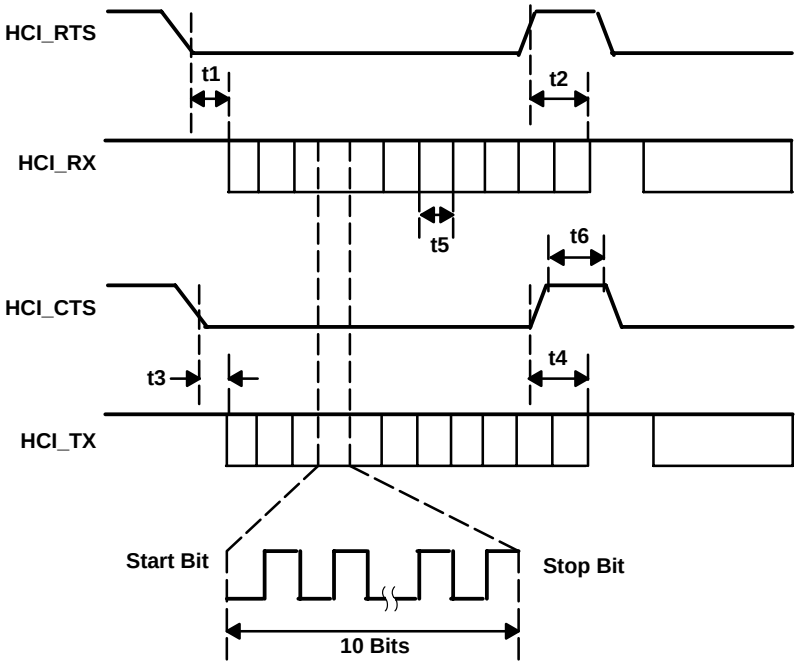
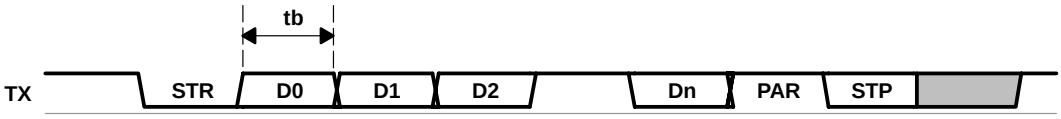


Figure 4−2. UART Timing Diagram



STR—Start bit

D0..Dn—Data bits (LSB first)

PAR—Parity bit (if parity is used)

STP—Stop bit

CHARACTERISTICS	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Baud rate	Any rate (1)		37.5	115.2	4000	Kbps
Baud rate accuracy	Receive/transmit	t5/t7			−2.5 to 1.5	%
CTS low to TX_DATA on		t3	0	2		µs
CTS high to TX_DATA off	Hardware flow control	t4			1	Byte
CTS High Pulse Width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		µs
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes
Bit width (Jitter)	See Note 1	tb				% relative to ideal bit width

NOTE 1: Exception for 19.2 MHz: Maximum baud rate = 3.84 Mbps. For complete coverage of f_{REF} verses baud rate exceptions (including Jitter specifications), use TI UART Calculator software utility.

4.19 BTSPI Interface Timing

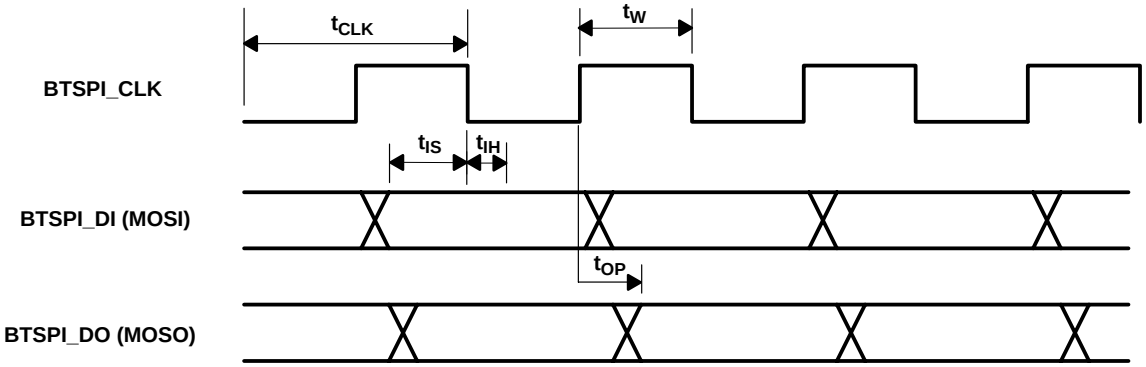


Figure 4−3. BTSPI Interface Timing

SYMBOL	PARAMETER	MAX [NS]	MIN [NS]	LOAD[PF]
t_{CLK}	Cycle time		76	
t_{CLKJ}	Cycle time with 5% jitter		72	
t_W	pulse duration	0.6*Tclkj = 43.2	0.4*Tclkj = 28.8	
t_{IP}	MOSI setup time		3	
t_{IH}	MOSI hold time		0	
t_{OP}	MISO propagation time	17		20

4.20 SDIO Interface Timing

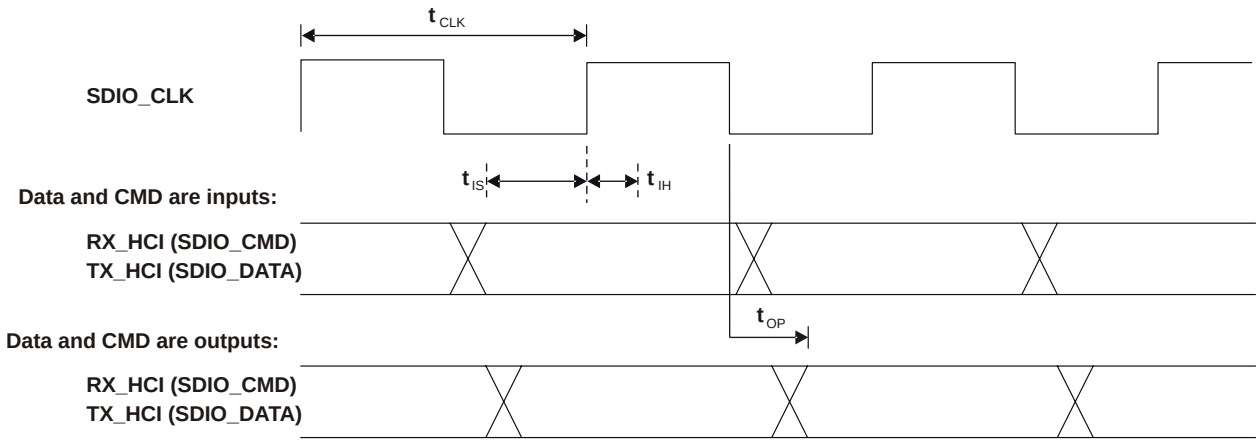


Figure 4−4. SDIO Interface Timing

SYMBOL	PARAMETER	MAX [NS]	MIN [NS]	LOAD[PF]
t_{CLK}	Cycle time (50% duty cycle)		50 (20 MHz)	
t_{CLK}	Cycle time (40% duty cycle)		62.5 (16 MHz)	
t_{IS}	SDIO CMD setup time	5		
t_{IH}	SDIO CMD hold time		0	
t_{IS}	SDIO DATA setup time	5		
t_{IH}	SDIO DATA hold time		0	
t_{OP}	SDIO CMD propogation time	18	3	25
t_{OP}	SDIO DATA propogation time	18	3.5	25

4.21 I²C Interface

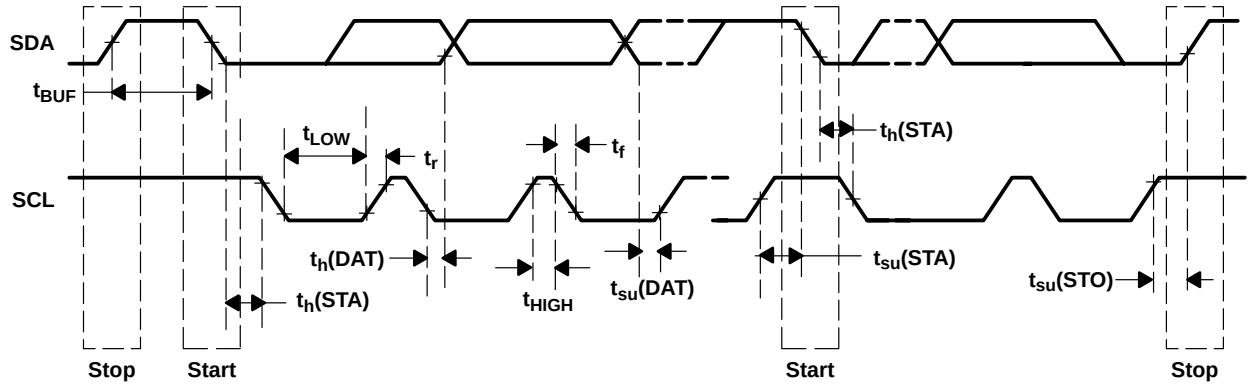


Figure 4−5. I²C Bus Timing Diagram

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}		100		400	kHz
Bus free time between a stop and start condition	t_{BUF}	4700		1300		ns
Hold time (repeated) start condition. After this period, the first clock pulse is generated	$t_{HD(STA)}$	4000		600		ns
Low period of SCL clock	t_{LOW}	4700		1300		ns
High period of SCL clock	t_{HIGH}	4000		600		ns
Setup time for a repeated start condition	$t_{SU(STA)}$	4700		600		ns
Data hold time	$t_{HD(DAT)}$	0		0		ns
Data setup time	$t_{SU(DAT)}$	250		100		ns
Rise time of both SDA and SCL	t_R		1000		300	ns
Fall time of both SDA and SCL	t_F		300		300	ns
Setup time for STOP condition	$t_{SU(STO)}$	4000		600		ns

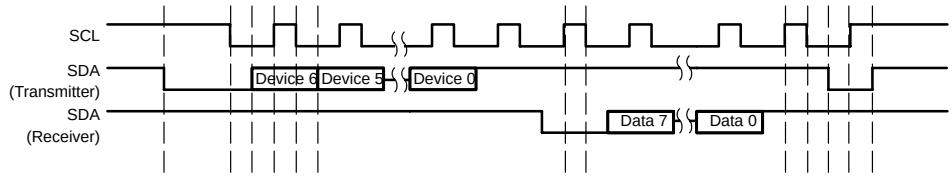


Figure 4−6. I²C Bus Write Access Timing

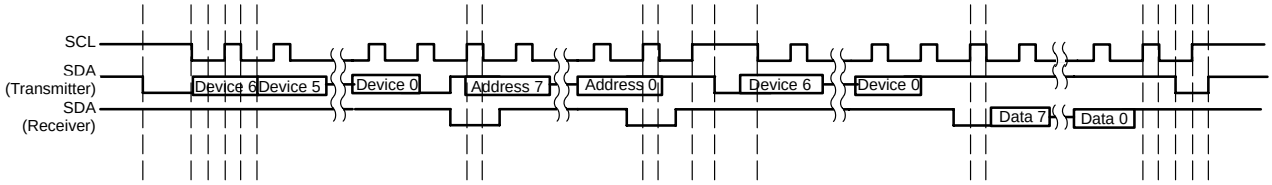


Figure 4−7. I²C Bus Read Access Timing

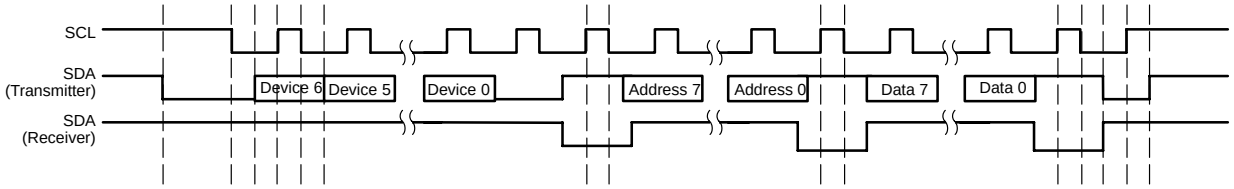
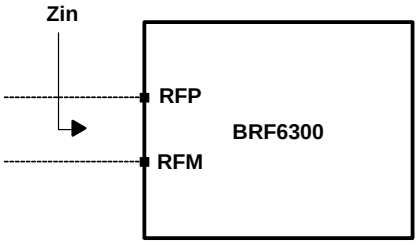


Figure 4−8. I²C Bus Combined Read Access Timing

4.22 Input Impedance (RX Mode)



FREQUENCY (GHz)		Z_{IN}, DIFFERENTIAL INPUT IMPEDANCE (Ω)									UNIT
		MIN 25°C	TYP 25°C	MAX 25°C	MIN −40°C	TYP −40°C	MAX −40°C	MIN 85°C	TYP 85°C	MAX 85°C	
BGA	2.45		4.4−j24.7								
WSP	2.45		4.3−j34.3								

5 Tools

The BRF6300 is supplied with the following set of tools and documentation to assist the user with product development:

5.1 Starter Kit

Demonstration platform and development environment provide easy migration to final product. It consists of two boards:

- BTM− Bluetooth Module which holds the complete BRF6300 Reference design
- GIB – Generic Interface Board. This board holds the BTM and provides it with needed power and clock. It also contains all peripherals needed to communicate with BRF6300, as well as provides platform for measurement of power consumption or evaluation of RF Performance.

The Starter Kit can be connected to a PC or host application.

5.2 HCI Commander and HCI Tester

These applications allow users to operate TI Bluetooth devices via PC COM or USB ports. The applications can transmit HCI commands and receive HCI events from TI baseband devices.

5.3 Logger

The BRF6300 has the ability to send debug messages through the TX DBG line using a RS232 protocol during functional operation. The logger is a PC based tool which can capture and display messages from HCI to LM level including sent and received RSSI messages.

5.4 Protocol Monitor

This tool captures trace messages and UART data and parses the information. It synchronizes to the BT clock to show a real-time view of the BT activity.

5.5 Link Quality Monito

This tool shows RSSI/PER/BER statistics during a connection in run-time.

5.6 Production Line Testing

A set of built in self test commands is provided to help the user in his production line testing

5.7 Reference Design with TI Chipset

This reference design describes interface between TI GSM−GPRS−UMTS chipset. Evaluation Platform from TI Chipset (D−Sample, E−Sample) includes TI Bluetooth Reference Design

5.8 Reference Design with TI OMAP Application Processor

This reference design describes interface between TI’s OMAP application processor and the Bluetooth chipset.

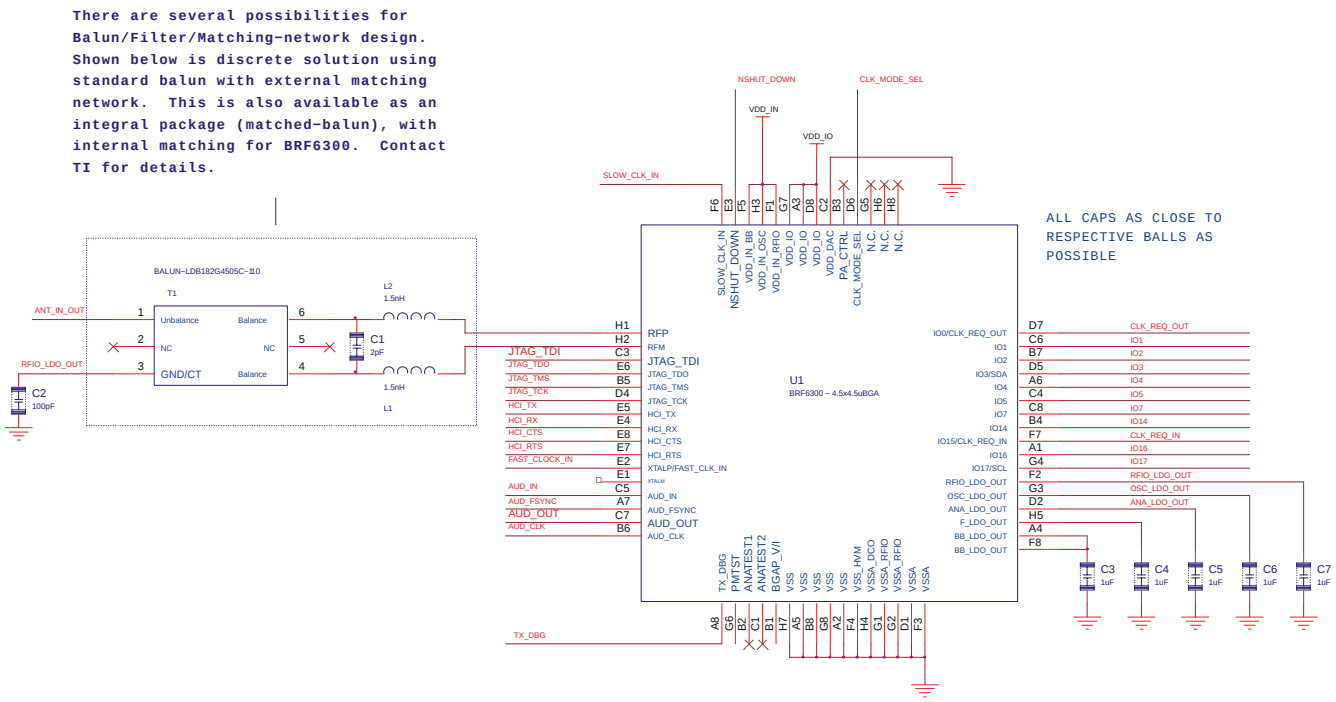
5.9 Reference Design with TI WLAN

Specifics feature have been designed in both TI Bluetooth Chipset and TI WLAN Chipset to ensure coexistence of the two solutions.

6 Reference Designs

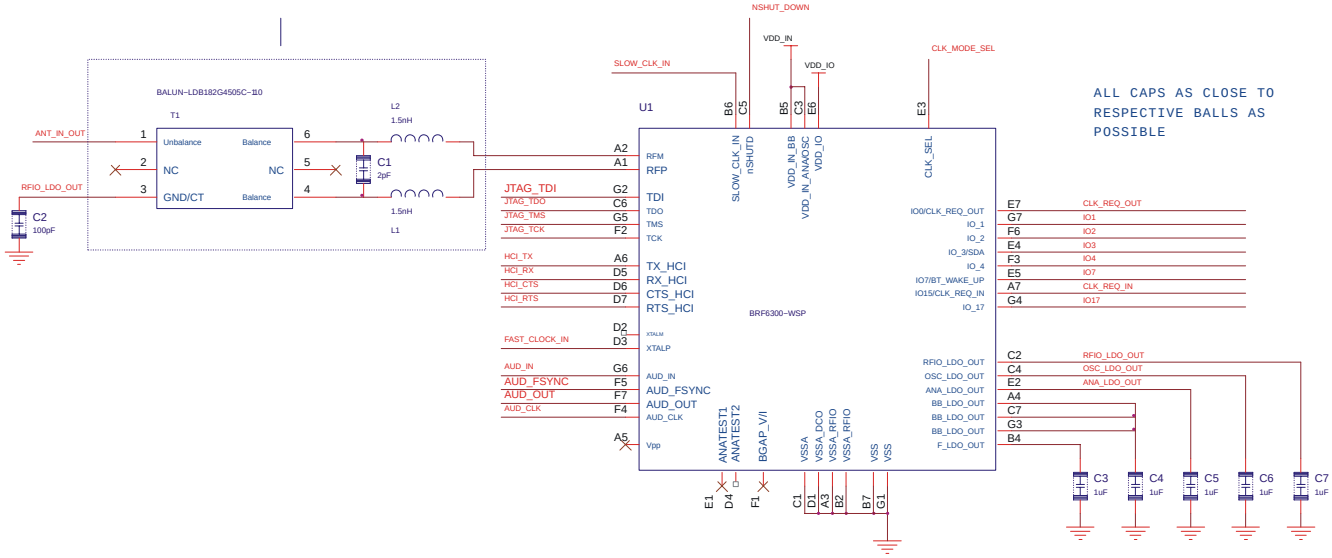
Application circuit schematic for power and radio connections.

6.1 BGA Pinout



6.2 WSP Pinout

There are several possibilities for Balun/Filter/Matching-network design. Shown below is discrete solution using standard balun with external matching network. This is also available as an integral package (matched-balun), with internal matching for BRF6300. Contact TI for details.



6.3 Bill of Materials

ITEM	QTY	VALUE	REFERENCE	FOOTPRINT	PART NO.	MANUFACTURER	TOLERANCE
1	1	2 pF	C1	C0402	CL05C020JBNC	Samsung	NPO ±0.25 pF
2	1	100 pF	C2	C0402	CL05C101JBNC	Samsung	NPO ±5%
3	5	1 µF	C3−C7	C0402	JMK105BJ105KV	Taiyo Yuden	X5R ±10%
4	2	1.5 nH	L1, L2	L0402	LQP10A1N5COOT 1M00−01	Murata	±0.2 nH
5	1	Balun	T1		LDB182G4505C−110	Murata	
6	1	BRF6300	U1			TI	

7 Reference Documents

The following section lists all the currently-available BRF6300 documents and application notes in addition to this data manual.

- BT−AN−0046 (BRF6300 Package Information).pdf
- BT−AN−0047 (BRF6300_WLAN Coexistence).pdf
- BT−AN−0051 (BRF6300 Class1 Implementation).pdf
- BT−AN−0052 (BRF6300 Voice configuration).pdf
- BT−AN−0055 (BRF6300 clock sharing).pdf
- BT−AN−0056 (BRF6300 sync to host Rev 0 2).pdf
- BT−RN−0024 (BRF6300 Firmware Release Note).pdf
- BT−SW−0024 (BRF61XX HCILL 4 wire Power Management Protocol).pdf
- BT−SW−0029 (BRF6300 HCI Vendor Specific Command).pdf

8 Glossary

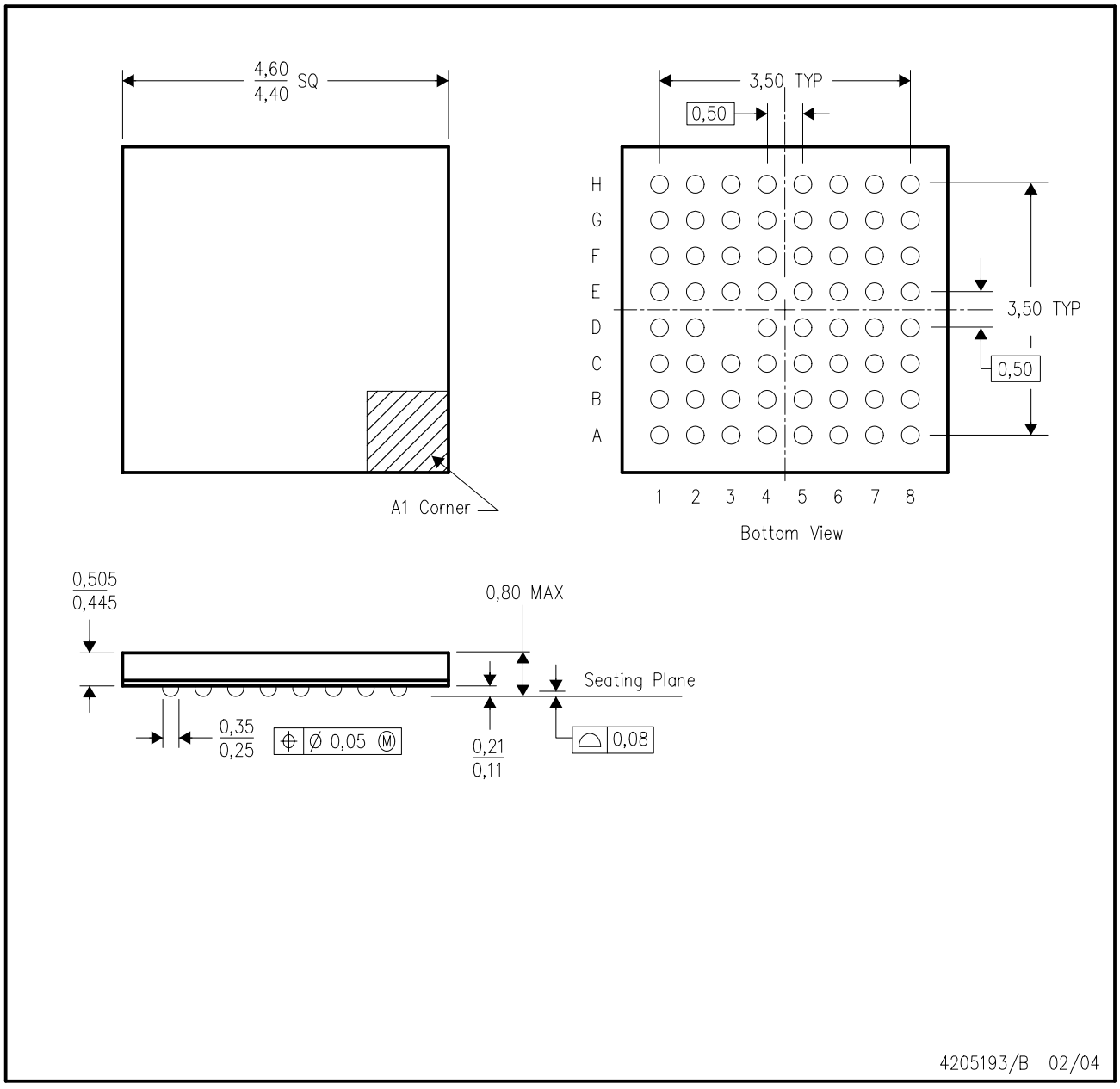
ACL	Asynchronous Connectionless
ADC	Analog-to-Digital Converter
A-Law	Audio encoding standard
BGA	Ball Grid Array
BIST	Built-In Self Test
C/I	Carrier Over Interference
CMOS	Complementary Metal Oxide Semiconductor
Codec	Coder Decoder
CPU	Central Processing Unit
CVSD	Continuously-Variable Slope-Delta Modulation
DCO	Digitally Controlled Oscillator
DFIR	Decimation FIR Filter
DPLL	Digital Phase-Locked Loop
DRP	Digital Radio Processor
eSCO	Extended Synchronous Connection-Oriented
FIFO	First In, First Out
FIR	Finite Impulse Response
FW	Firmware
HCI	Host Controller Interface
I2S	Inter-IC Sound
JTAG	Joint Test Action Group (TI hardware debugging interface)
LDO	Low Drop Out
LNA	Low-Noise Amplifier
LNTA	Low-Noise Transconductance Amplifier
MTDSM	Multitap direct sampling mixer
PA	Power amplifier
PCM	Pulse-Code Modulation
PLL	Phase-Locked Loop
PSRR	Power Supply Rejection Ratio
RAM	Random-Access Memory
RF	Radio Frequency
ROM	Read-Only Memory
RSSI	Received Signal Strength Indicator
SCO	Synchronous Connection-Oriented
UART	Universal Asynchronous Receiver/Transmitter
VS	Vendor-Specific
μ-Law	Audio Encoding Standard

9 Mechanical Data

9.1 63-Ball BGA Package

The following illustration presents the mechanical data for the plastic ball grid array package.

ZSL (S–PBGA–N63) PLASTIC BALL GRID ARRAY



NOTES. A: All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. This package is lead–free.

9.2 47-Ball WSP Package