BRF6300 Voice Configuration

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Approval table

Role	Name	Revision	Date
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Anthony Levine	Document creation	0.1	30.5.2005
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Abstract

This document describes the capabilities of the BRF6300 voice system. It describes the different audio formats supported by the BRF6300 and how to interface with them using the PCM bus. It also describes voice over HCI in the BRF6300 and some issues regarding eSCO links.

Contents

1. Audio CODEC interface

1.1. Overview

The CODEC interface is a fully dedicated programmable serial port that provides the logic to interface to several kinds of PCM or I2S codecs. The interface supports:

- Two voice channels
- Master / slave modes
- u-Law, A-Law, Linear and Transparent coding schemes
- Variable length frames and frame sync duty cycles
- Variable data size, position and bit order.
- PCM bus sharing
- High rate PCM interface for EDR.
- Various voice formats (standard PCM, I2S, UDI) and a wide variety of Codecs.

1.2. PCM hardware interface

The PCM interface is a 4-wire interface. It contains the following lines:

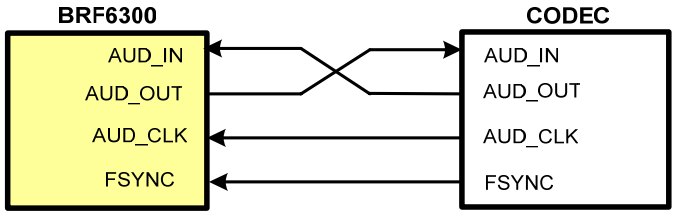


Figure 1 – PCM interface (BRF6300 as slave)

AUD_IN	-	Input
AUD_OUT	-	Output
AUD_CLK	-	Configurable direction (input or output)
FSYNC	-	Configurable direction (input or output)

The Bluetooth device can be either the master of the interface where it generates the clock and the frame-sync signals, or slave where it receives these two signals. i.e. Clock and frame-sync can act as inputs or outputs. Configured is done by HCI_VS_Write_Codec_Configuration_Island3. (For all VS information, see BT-SW-00xx (BRF6300 Vendor specific commands, Rev x)).
After reset or power up, the PCM interface is set to slave by default. All pull-down's are active.

1.2.1. AUD_CLK

For slave mode, clock input frequencies of up to 16 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.
For master mode, the BRF6300 can generate any clock frequency between 64 KHz and 4.096 MHz, with 1ppm accuracy. Clocks are generated from the fast clock and will be synchronous to it.

EDR support affects the maximum PCM clock rate. The maximum data rate will be achieved when using 3-EV5 packets. The maximum rate of one asymmetric 3-EV5 channel is 1.154MHz (= one 3-EV5 packet every 3 frames). The maximum rate of 2 asymmetric 3-EV5 channels is 1.382MHz (= two 3-EV5 packets every 5 frames).
This means that in order to support 2 channels, the clock rate needs to be at least 1.382MHz.

1.2.2. AUD_OUT

The Data Out line is configured as HiZ output between data words. Data Out can also be set for permanent HiZ, irrespective of data out. This allows BRF6300 to act as a bus slave in a multi-device PCM bus.

1.2.3. FSYNC

For both master and slave modes, the interface supports Fsync periods from 1 to 65535 times the Audio Clock period, in 1 clock increments.
For both master and slave modes, the interface supports Fsync duty cycles of 1 to 65535 times the Audio Clock period, in 1 clock increments. A value of 0x0000 sets for 50% duty cycle (e.g. required by I2S interface)

1.2.4. Clock-edge operation

The CODEC interface of the BRF6300 can work on rising or falling edge of the clock. It also has the ability to sample the frame sync and the data at inversed polarity.
The following diagram shows operation of a falling-edge-clock type of codec. The codec is the master of the PCM bus. The frame sync signal is updated by the codec on the falling clock edge and therefore shall be sampled by the BRF6300 on the next rising clock. The data from the codec will be driven from the falling edge and therefore sampled by the BRF6300 on the clock falling edge.

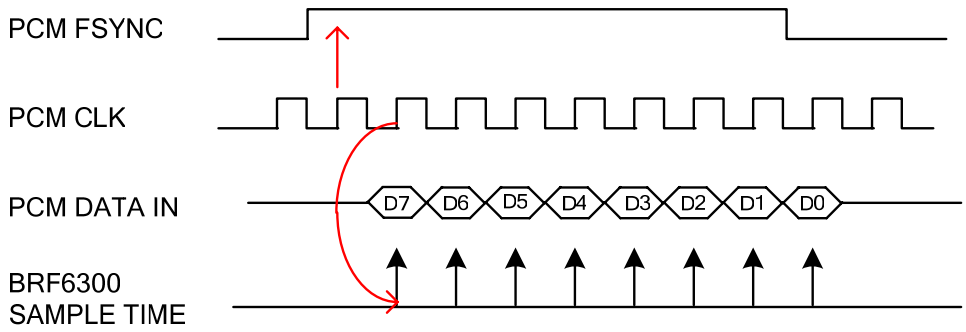


Figure 2 – Negative clock edge PCM operation

1.3. Data bits configuration

1.3.1. Size

The data length can be set from 8 to 640 bits, per channel. Up to two channels are possible and data length can be set independently for each channel.
Data in and data out do not necessarily have to be the same size.

1.3.2. Order

There are CODECs in which the bit-order is inversed, i.e. LSB is first. The BRF6300 CODEC interface supports both MSB first and LSB first.
The bits order of data in and data out can be configured independently.
The order for each channel is separately configurable.

1.3.3. Position / offset

There are CODECs in which the input and output data do not have the same timing – for example PCM3008, a stereo audio codec of TI.
In general, the data position within a frame is configurable in with 1 clock (bit) resolution and can be set independently for each channel, relative to the beginning edge of the frame sync signal.

1.3.4. HCI_VS_write_codec_config_Island3

Command	Opcode	Command Parameters	Size
Write_codec_config_Island3	0xFD06	PCM clock rate	2 bytes
		PCM clock direction	1 byte
		Frame sync frequency	2 bytes
		Frame sync duty cycle	2 bytes
		Frame sync edge	1 byte
		Frame sync polarity	1 byte
		Reserved**	1 byte
		CH1 data out size	2 bytes
		CH1 data out offset	2 bytes
		CH1 data out edge	1 byte
		CH1 data in size	2 bytes
		CH1 data in offset	2 bytes
		CH1 data in edge	1 byte
		Reserved	1 byte
		CH2 data out size	2 bytes
		CH2 data out offset	2 bytes
		CH2 data out edge	1 byte
		CH2 data in size	2 bytes
		CH2 data in offset	2 bytes
		CH2 data in edge	1 byte
		Reserved	1 byte

Description:
This command is used to configure the codec interface general parameters.

Default Values:	**HW default**
PCM clock rate	N.A
PCM direction	1 (Input)
Frame sync frequency	N.A
Frame sync duty cycle	N.A
Frame sync edge	0 (rising edge)
Frame sync polarity	0 (active high)
Reserved	N.A
CH1 data out size	0
CH1 data out offset	0
CH1 data out edge	0 (rising edge)
CH1 data in size	0
CH1 data in offset	0
CH1 data in edge	0 (rising edge)
Reserved	N.A
CH2 data out size	0
CH2 data out offset	0
CH2 data out edge	0 (rising edge)
CH2 data in size	0
CH2 data in offset	0
CH2 data in edge	0 (rising edge)
Reserved	N.A

Command Parameters:

PCM clock rate Size: 2 Bytes

Value	**Parameter Description**
64 – 16000	The PCM clock rate is between 64k to 4096k for master mode, or 64K to 16M for slave mode. It affects other parameters like wait cycles and frequency rate calculation and therefore must be configured even if external clock is used

PCM direction Size: 1 Byte

Value	**Parameter Description**
0x00	PCM clock and Fsync direction is output (BRF6300 is master of the PCM bus) and sampled on rising edge
0x01	PCM clock and Fsync direction is input (BRF6300 is slave of the PCM bus)

Frame sync frequency Size: 2 Bytes

Value	Parameter Description
100Hz – 173KHz	Frame sync frequency in Hz.

Frame sync duty cycle Size: 2 Byte

Value	Parameter Description
0x0000	50 % of frame sync period
0x0001 – 0xFFFF	Number of cycles of PCM clock that FSYNC is active (high or low)

Frame sync edge Size: 1 Byte

Value	Parameter Description
0x00	Driven/sampled at rising edge
0x01	Driven/sampled at falling edge

Frame sync polarity Size: 1 Byte

Value	Parameter Description
0x00	Active-high
0x01	Active-low

CHx data out size Size: 2 Bytes

Value	Parameter Description
0x0001 .. 0x0280	Sample size in bits for each codec Fsync. The value is from 1 to 640 bits. If size > 24 bits, the size should be dividisible by 8. (i.e.. 1-24, 32, 40, 48…)

CHx data out offset Size: 2 Bytes

Value	Parameter Description
0x0000 .. 0x????	Number of PCM clock cycles between rising of frame sync to data start

CHx out clock edge Size: 1 Byte

Value	Parameter Description
0x00	Data output from rising edge
0x01	Data output from falling edge

CHx data in size Size: 2 Bytes

Value	Parameter Description
0x0001 .. 0x0280	Sample size in bits for each codec Fsync. The value is from 1 to 640 bits. For data size > 24 bits, the size should be dividisible by 8. (i.e. 1-24, 32, 40, 48…)

CHx in offset Size: 2 Bytes

Value	Parameter Description
0x0000 .. 0x????	Number of PCM clock cycles between rising of frame sync to data start

CHx in edge Size: 1 Byte

Value	Parameter Description
0x00	Data sampled at rising edge
0x01	Data sampled at falling edge

Events Generated:
Command Complete Event.

1.3.5. HCI_VS_write_codec_config_enhanced_Island3

Command	Opcode	Command Parameters	Size
Write_codec_config_enhanced_Island3	0xFD07	PCM clock shutdown	1 Byte
		PCM clock start	2 Bytes
		PCM clock stop	2 Bytes
		Reserved	1 Byte
		CH1 din order	1 Byte
		CH1 dout order	1 Byte
		CH1 dout mode	1 Byte
		CH1 dout duplication	1 Byte
		CH1 tx_dup_value	4 Bytes
		CH1 data quant	1 Byte
		Reserved	1 Byte
		CH2 din order	1 Byte
		CH2 dout order	1 Byte
		CH2 dout mode	1 Byte
		CH2 dout duplication	1 Byte
		CH2 tx_dup_value	4 Bytes
		CH2 data quant	1 Byte
		Reserved	1 Byte

Description:
This command is used to configure enhanced configuration of the codec interface. This command is optional and need not be used if all default parameters are acceptable.
When this command is used, it must be sent after Write_codec_config_Island3.

Default Values:	**HW default**
PCM clock shutdown	0 (Disable)
PCM clock start	0
PCM clock stop	0
Reserved	N.A
CH1 din order	0 (MSB-first)

CH1 dout order	0 (MSB-first)
CH1 dout mode	2 (input when idle)
CH1 dout duplication	0 (last sample)
CH1 tx_dup_value	0
CH1 data quant	0
Reserved	N.A

CH2 din order	0 (MSB-first)
CH2 dout order	0 (MSB-first)
CH2 dout mode	2 (input when idle)
CH2 dout duplication	0 (last sample)
CH2 tx_dup_value	0
CH2 data quant	0
Reserved	N.A

PCM clock shutdown Size: 1 Byte

Value	Parameter Description
0x00	PCM clock shutdown feature is disabled
0x01	PCM clock shutdown feature is enabled. Time of start/stop is defined in the following 2 fields (used in Master mode only)

PCM clock start Size: 2 Bytes

Value	Parameter Description
0x0000..0x????	Number of PCM clock cycles relative to the PCM frame sync to start PCM clock (for example – start 2 clocks before frame sync)

PCM clock stop Size: 2 Bytes

Value	Parameter Description
0x0000..0x????	Number of PCM clock cycles relative to the PCM frame sync to stop PCM clock (for example – stop 20 clocks after frame sync)

CHx din order Size: 1 Byte

Value	Parameter Description
Bit 0 = 0 Bit 0 = 1	Data driven MSB-first Data driven LSB-first
Bit 1 = 0 Bit 1 = 1	Don't swap bytes within the sample. swap bytes within the sample in bit-wise mode when data size > 8 ([XYZ]->[ZYX])
Bit 2 = 0 Bit 2 = 1	Don't shift sample. Shift sample by (24|16-dout_size) bits from MSB to LSB (Controls sample alignment inside internal register (23:0) in bit-wise mode only)

CHx dout order Size: 1 Byte

Value	Parameter Description
Bit 0 = 0 Bit 0 = 1	Data driven MSB-first Data driven LSB-first

Bit 1 = 0 Bit 1 = 1	Don't swap bytes within the sample. swap bytes within the sample in bit-wise mode when data size > 8 ([XYZ]->[ZYX])
Bit 2 = 0 Bit 2 = 1	Don't shift sample. Shift sample by (24|16-dout_size) bits from MSB to LSB (Controls sample alignment inside internal register (23:0) in bit-wise mode only)

CHx dout mode Size: 1 Byte

Value	**Parameter Description**
0x00	Always 3-state (input)
0x01	Always output
0x02	Switch to 3-state (input) when idle
0x03	Always 3-state (input)

CHx dout duplication Size: 1 Byte

Value	**Parameter Description**
0x00	Retransmit last sample when no data available
0x01	Transmit DUP_VALUE when no data available

CHx tx_dup_value Size: 4 Bytes

Value	**Parameter Description**
0x00000000 .. 0x00FFFFFF	Replacement value to transmit when no data is available

CHx data quant Size: 1 Byte

Value	**Parameter Description** In bit-wise mode, the basic data unit is the whole sample (8-24bits). In byte-wise mode, the basic data unit is one byte
0x00	Bit-wise mode. Possible if both data in and data out size are up to 24bits
0x01	Byte-wise mode

Events Generated:
Command Complete Event.

2. Two channel PCM bus Example

In the following figure, a 2-channel PCM bus is shown where the two channels have different word sizes and arbitrary positions in the bus' frame.

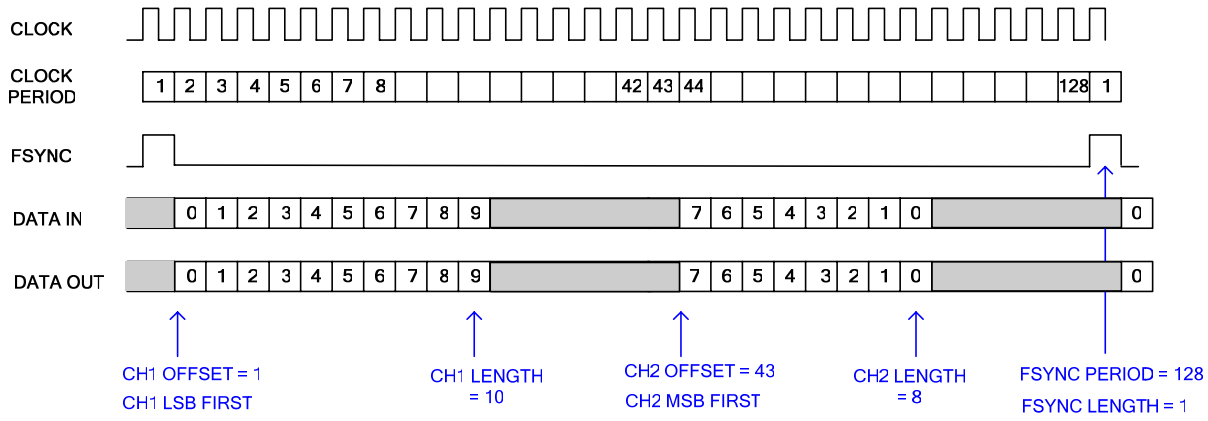


Figure 3: Two channel PCM bus timing

HCI_VS_Write_Codec_Configuration_Island3 setup:

- PCM clock rate 0x0800 (2.048 MHz)
- PCM clock direction 0x01 (BRF6300 is slave)
- Frame sync frequency 0x03E80 (16 KHz)
- Frame sync duty cycle 0x0001 (high for 1 period of PCM clock)
- Frame sync edge 0x00 (rising edge)
- Frame sync polarity 0x00 (active high)
- Reserved 0x00
- CH1 data out size 0x000A (10 bits)
- CH1 data out offset 0x0001 (1 clock from rising edge of fsync)
- CH1 data out edge 0xFF (data out driven at clock rising edge)
- CH1 data in size 0x000A (10 bits)
- CH1 data in offset 0x0001 (1 clock from rising edge of fsync)
- CH1 data in edge 0xFF (data out driven at clock rising edge)
- Reserved 0x00
- CH2 data out size 0x0008 (8 bits)
- CH2 data out offset 0x002C (44 clocks from rising edge of fsync)
- CH2 data out edge 0xFF (data out driven at clock rising edge)
- CH2 data in size 0x0008 (8 bits)
- CH2 data in offset 0x002C (44 clocks from rising edge of fsync)
- CH2 data in edge 0xFF (data out driven at clock rising edge)
- Reserved 0x00

HCI_VS_Write_Codec_Configuration_Enhanced_Island3 setup:

- PCM clock shutdown 0x00 (disabled)
- PCM clock start 0x0000 (N/A)
- PCM clock stop 0x0000 (N/A)
- Reserved 0x00
- CH1 data in order 0x01 (LSB first)
- CH1 data out order 0x01 (LSB first)

- CH1 data out mode 0x02 (Hi-Z when idle)
- CH1 data out duplication 0x00 (Retransmit last sample for missing data)
- CH1 tx_dup_valve 0x00000000 (N/A)
- CH1 data quant 0x00 (Use bit mode if < 24 bits)
- Reserved 0x00
- CH2 data in order 0x00 (MSB first)
- CH2 data out order 0x00 (MSB first)
- CH2 data out mode 0x02 (Hi-Z when idle)
- CH2 data out duplication 0x00 (Retransmit last sample for missing data)
- CH2 tx_dup_valve 0x00000000 (N/A)
- CH2 data quant 0x00 (Use bit mode if < 24 bits)
- Reserved 0x00

3. Frame Idle Period

The CODEC interface has the capability for frame idle periods, where the PCM clock can “take a break” and become ‘0’ at the end of the PCM frame, i.e. after all data has been transferred.
This feature is configured by HCI_VS_Write_Codec_Config_Enhanced, described above.

The BRF6300 supports frame idle periods both as master and slave of the PCM bus.
When BRF6300 is the master of the interface, the frame idle period is configurable. There are 2 configurable parameters:

- Clk_Idle_Start - Indicates the number of PCM clock cycles from the beginning of the frame till the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock will become ‘0’.
- Clk_Idle_End – Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of PCM clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

e.g. For PCM clock rate = 1MHz, frame sync period = 10 KHz, Clk_Idle_Start = 60, Clk_Idle_End I = 90:

Between each 2 frame syncs there will be 70 clock cycles (instead of 100). The clock idle period will start 60 clock cycles after the beginning of the frame and will last 90-60=30 clock cycles. This means that the idle period will end 100-90=10 clock cycles before the end of the frame. The data transmission must end prior to the beginning of the idle period.

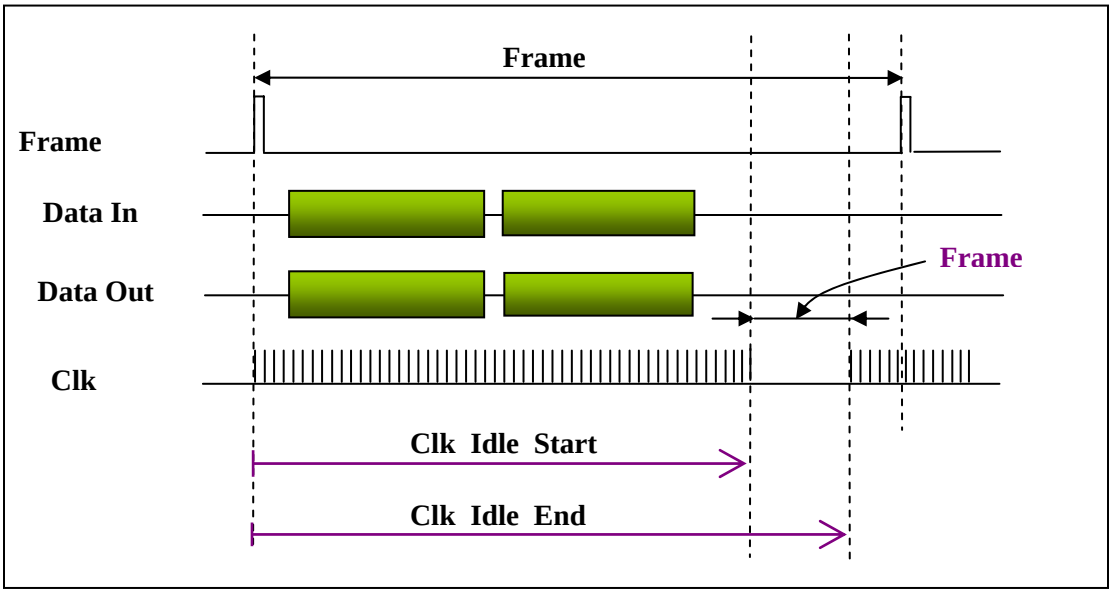


Figure 4 – Frame Idle Period

Behavior with no input clock
As an improvement over the BRF6150 and in addition to the above, the BRF6300 (as slave) features a flexible recovery mechanism when the clock stops unexpectedly during a SCO/eSCO link. Little impact will be noticeable on the voice channel.

4. PCM Bus Sharing

The BRF6300 supports multi device configuration, in which there are several devices on the PCM bus. The pin AUD_OUT can be configured to High impedance when it is not in use (i.e. between data words). Combining this mode and setting the PCM interface to Slave mode (AUD_CLK and AUD_FSYNC are Inputs), allows sharing the same codec for both Bluetooth and other applications. When the BRF6300 is not used, the codec interface is configured as described above and other devices can be active on the PCM bus.

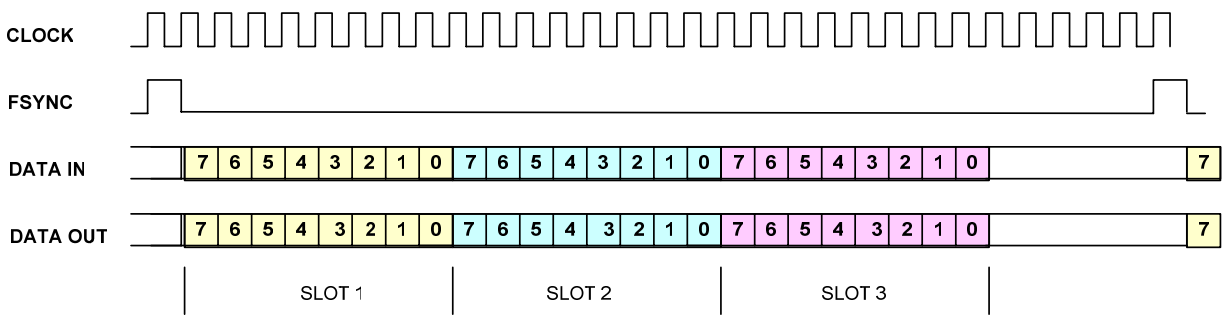


Figure 5 – PCM bus sharing

5. RF link/PCM clock mismatch handling

The BRF6300 receives audio data from external codec or similar on the PCM interface and transmits these over Bluetooth 2.4GHz RF channels. Similarly, the BRF6300 receives audio data via Bluetooth 2.4GHz RF channels and transmits these to external codec via the PCM interface. These input and output data rates will not usually be the same, and therefore an audio data overflow or underflow can occur.

5.1. Overflow

The BRF6300 receives RF voice packets and writes these to the CODEC interface. If the BRF6300 receives data faster than the CODEC I/F output allows, an overflow will occur. In this case, the BRF6300 has two possible behavior modes: 'allow overflow' and 'don't allow overflow'.
A similar situation occurs when the BRF6300 receives data packets via the codec interface, faster than the BT RF link is able to transmit.

- If overflow is allowed, the BRF6300 will continue receiving data and will overwrite any data not yet sent to the CODEC.
- If overflow is not allowed, RF voice packets received when buffer is full, will be discarded.

5.2. Underflow

Underflow will occur if output to the CODEC interface occurs at a higher rate than the BRF6300 receives new data over the air. i.e. The PCM output buffer will be empty.

- In this case, the configured duplication data will be output to the PCM bus.

Underflow can also occur if CODEC interface input rate is lower than the BT RF transmitting rate.

- In this case, the last PCM sample will be re-sent over the air.

5.3. Bluetooth clock and PCM clock synchronization.

Even when the BT and PCM data are well matched to avoid the problems or overflow and underflow above, there still exists a potential problem of data loss due to long-term clock drift between the BT clock and the PCM clock. This synchronization issue exists in any voice connection that uses the CODEC interface. However, it is most critical for UDI support.
The BRF6300 solves this problem by the following: When the BRF6300 is the PCM bus master, it will automatically synchronize the PCM clock to the BT clock.
Note: Bluetooth clock is the Bluetooth timing clock provided by the Bluetooth piconet master and should not be confused with the BRF6300 Fref input.

There are 4 possible master-slave combinations. The BRF6300 can guarantee clock synchronization only when it is PCM master. When it is PCM slave and BT master, the PCM clock can not be relied on to meet BT accuracy specifications or to be continuous. In the case of the BRF6300 being the BT slave and the PCM slave, it has no control over either clock.

This is shown in the following table:

BT clock	PCM clock	Result
Master	Master	Synchronized
Master	Slave	Not synchronized

Slave	Master	Synchronized
Slave	Slave	Not synchronized

6. PCM Loop back

The PCM loop back feature allows performing loop back on the PCM bus. The loop back is done through buffers only and is used to test the connectivity on the PCB.

All the codec interface parameters, set by the HCI_VS_Write_Codec_Configuration_Island3 command, need to be set prior starting the PCM loop back.

The PCM loop back is enabled using HCI_VS_Set_PCM_Loopback_Enable. However, the loopback delay must first be configured using the following HCI_VS command:

HCI_VS_Set_PCM_Loopback_Configuration_Island3 (0xFD04)

Command	Opcode	Command Parameters	Return Parameters
HCI_VS_Set_PCM_Loopback_Configuration_Island3	0xFD04	PCM loopback delay	Status

Description:

This command is used to configure the default PCM loopback delay on the bus between the PCM input data to the PCM output data. The new delay will affect the next PCM loopback channel enabled. In case a PCM loopback channel is already activated, disable it and then enable it again in order to use the new delay.

Command Parameters:

PCM loopback delay Size: 2 Byte

Value	Parameter Description
0x0001 - 0x0544	This value defines the delay in sample units (i.e. number of Frame sync) between the input sample to BRF6300 and the output of the same sample from BRF6300

Return Parameters:

Status: Size: 1 Byte

Value	Parameter Description
0x00 0x01-0xFF	Command Succeeded. Command failed. See **Error! Reference source not found.** on page **Error! Bookmark not defined.**

Events Generated:

Command Complete Event

7. Improved algorithm for lost packets

The BRF6300 features an improved algorithm for improving voice quality when received voice data packets go missing. There are two options:

- Repeat the last sample – possible only for sample sizes up to 24 bits. For sample sizes >24 bits, the last byte is repeated.
- Repeat a configurable sample of 8-24 bits (depends on the real sample size), in order to simulate silence (or anything else) in the PCM bus. The configured sample will be written in a specific register for each channel.

The choice between those two options is configurable separately for each channel using the HCI_VS_Write_Codec_Configuration_Enhanced_Island3 described above.

This feature is further enhanced using the following new HCI_VS command:

HCI_VS_enable_EPLC

Command	Opcode	Command Parameters	Size
Enable_EPLC	0xFD08	EPLC enable EPLC N value EPLC R value Reserved	1 Byte 1 Byte 1 Byte 1 Byte

Description:
This command is used to enable Enhanced Packet Loss Concealment and configure the N value (repeat last packet counter) and R value (repeat noise counter).

Default Values:	HW default	HCI Tester command
EPLC enable	0 (Disable)	0 (Disable)
EPLC N value	0	0
EPLC R value	0	0
Reserved	N.A	0

EPLC enable Size: 1 Byte

Value	Parameter Description
0x00	disable enhanced packet loss control feature
0x01	enable enhanced packet loss control feature

EPLC N value Size: 1 Byte

Value	Parameter Description
0-15	N parameter used in EPLC (previous packet transmissions count)

EPLC R value Size: 1 Byte

Value	Parameter Description
0-15	R parameter used in EPLC (noise packet transmissions count) Note: recommended maximum 3 noise repetitions.

Events Generated:

Command Complete Event.

8. Voice formats

The voice setting parameter as specified in the BT specification, controls the various settings for voice connections. The voice setting parameter controls the following configuration for voice connections: Input Coding, Air coding format, input data format, Input sample size, and linear PCM parameter. The formats used on the PCM interface and RF air coding, need not necessarily be the same.
The settings apply to all voice connections and can not be set for individual voice connections.
The standard HCI_Write_Voice_Setting command is used to write the values for the voice setting configuration parameter (see description in the Bluetooth spec version1.2 sections 6.12, 7. 3.29 and 7.3.30).

The BRF6300 CODEC interface can use one of four audio coding patterns:

- A-Law (8-bit)
- μ-Law (8-bit)
- Linear (8 or 16-bit)
- Transparent

Command Parameters

Value	Description
00XXXXXXXX	Input Coding: Linear
01XXXXXXXX	Input Coding: μ-law Input Coding
10XXXXXXXX	Input Coding: A-law Input Coding
11XXXXXXXX	Reserved for Future Use
XX00XXXXXX	Input Data Format: 1's complement
XX01XXXXXX	Input Data Format: 2's complement
XX10XXXXXX	Input Data Format: Sign-Magnitude
XX11XXXXXX	Reserved for Future Use
XXXX0XXXXX	Input Sample Size: 8 bit (only for Liner PCM)
XXXX1XXXXX	Input Sample Size: 16 bit (only for Liner PCM)
XXXXXnnnXX	Linear_PCM_Bit_Pos: # bit positions that MSB of sample is away from starting at MSB (only for Liner PCM)
XXXXXXXX00	Air Coding Format: CVSD
XXXXXXXX01	Air Coding Format: μ-law
XXXXXXXX10	Air Coding Format: A-law
XXXXXXXX11	Reserved

Table 1: Voice setting parameters

9. Voice over HCI (VoHCI)

In addition to the codec interface, the BRF6300 also supports transfer of voice channels over the HCI interface. In this case (and unlike when using the PCM interface), the application is running a synchronous link through the HCI and all control is performed by the BRF6300 firmware; the data rate matching between the host and the air, buffer management and the total latency.

Main features:

- Supports all SCO/eSCO packet types and all data rates.
- All air modes supported: Transparent, CVSD, μLaw, aLaw.
- Flow control support in both directions
- Support 2 channels combinations – both Codec and VoHCI simultaneously. i.e. Each channel can be configured separately to CODEC or HCI
- Local Loopback is available.

Constraints:

- When using H5 transport layer, the Voice over HCI is not supported.

9.1. Creating a Synchronous link over HCI

9.1.1. HCI_VS_Write_SCO_Configuration

The command HCI_VS_Write_SCO_Configuration allows the host to configure the following parameters of the voice channels:

- Audio type: Codec interface/ Host interface (HCI)
- HCI TX buffer size – allows the host to determine the BRF6300 transmission buffer length.
- Max latency – determines the maximum amount of data (in Bytes) allowed in the TX buffer before it is flushed. This directly affects the latency of the channel. This parameter is applicable only if flow control is disabled. If flow control is enabled, then the host must regulate the data flow to keep the latency within limits.
- Accept packet with bad CRC – determines whether to accept packets received with bad CRC. In eSCO with retransmission, it will not disable retransmission - packet will be accepted only after all retransmissions have failed.
- SCO connection parameters and the flow control.

Return values:

- Status.
- HCI TX buffer size.
- Number of TX buffers.

The TX buffer minimum size is 30 bytes and there has to be at least 2 buffers.
The number of buffers is simply the number of buffers that will fit into the max latency given.
Notice that if the max latency value is not a multiple of the buffer size then it will be truncated accordingly. Therefore to prevent uncertainty, the host is encouraged to use max latency that is a multiple of the buffer size.

9.1.2. Flow Control

The flow control is implemented in both directions. Since there are separate RX and TX buffers for each channel, the host has to handle the flow control separately for each channel.

Host → Controller

- Unlike ACL data, the flow control in this direction is not mandated by the BT specification, however it is highly recommended to be used for guaranteed synchronization
- HCI_Write_SCO_ Flow_Control_Enable: Used to enable / disable flow control of SCO/eSCO data
- HCI_Read_Buffer_Size: If flow control is enabled, Host must issue the command before it sends any data to the Controller.
- In case a packet is totally or partly flushed, a "data buffer overflow" event is sent to the Host
- Host has to manage flow control independently for each channel. Therefore, the SCO connection handle needs to be considered. See the BT specification for more detail.

Controller → Host

- HCI_Host_Buffer_Size: The host uses this command to notify the controller of its SCO buffer pool.
- HCI_Set_Host_Controller_To_Host_Flow_Control: The host uses this command to enable/disable flow control in this direction. See the BT specification for more detail.
- Host has the control over the buffer size that the device will use and whether the synchronous connection is with the host or with the codec.

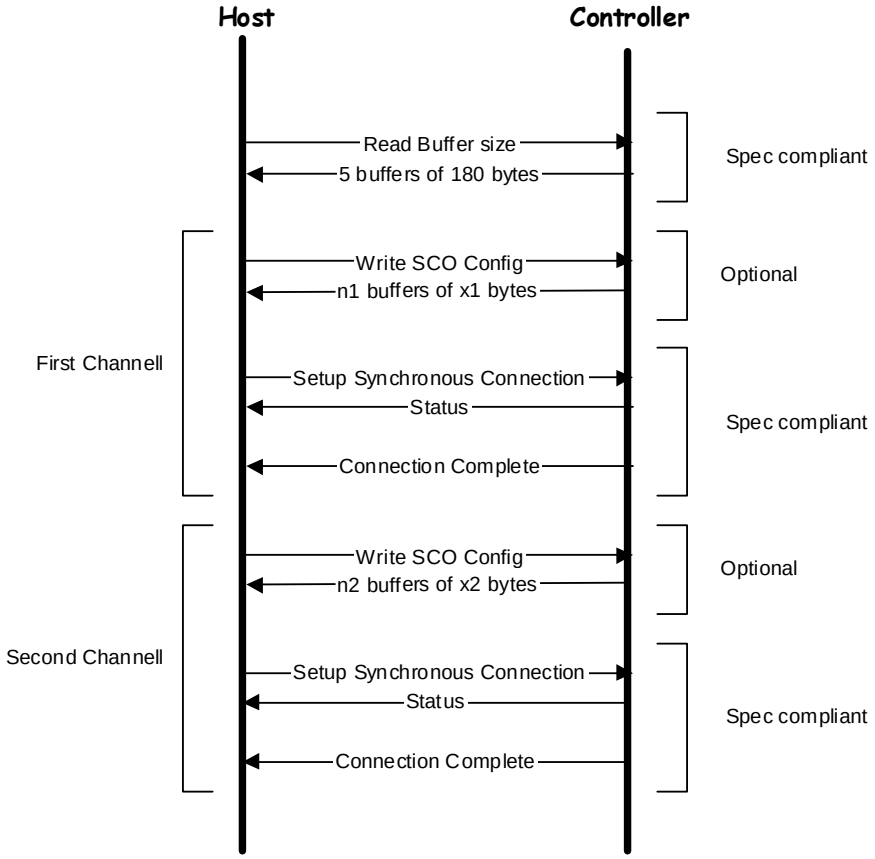


Figure 6: Synchronous connection creation procedure

9.2. Special considerations for voice over HCI

9.2.1. Performance

There are several factors to consider when evaluating the performance of VoHCI:

- Latency – The duration starting when sending a packet from one side until the other side receives it. It includes the UART delay, processing delay, air delay and buffer delay. It does not include the time that the host waits for flow control before sending the packet.
- Flow control affect on the BW – ability to reach full BW between the host and the device.
- Performance in high data rate.
- Idle time.
- Concurrent ACL and voice data.

A rough estimation for the latency is the number of BB (baseband) packets in the SCO buffer multiplied by the T_esco. Therefore, the bigger the SCO buffer, the larger the latency.

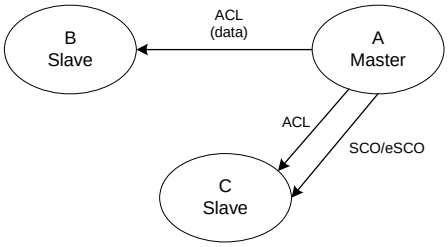
10. Using SCO/eSCO links in the BRF6300

The BRF6300 can handle multi-slot packets in parallel to synchronous links, for both TX and RX. Determination of the optimal packet size is done automatically by the BRF6300.

10.1. Constrains:

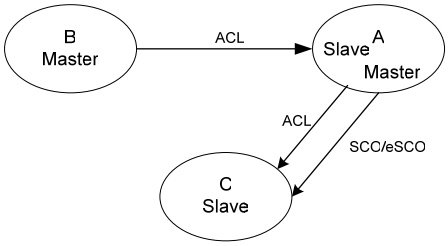
- The memory space BRF6300 reserves for synchronous data, may not be sufficient for some scenarios with two high BW synchronous links. If the occurs, the BRF6300 will reject an attempt to create a second synchronous link.

10.2. Point to multipoint



eSCO packet type = EV5, Tesco = 36, Wesco = 0, ACL(data) packet type = DH5/DH3 -> 361.6/195.2 Kbps
eSCO packet type = EV5, Tesco = 36, Wesco = 0, ACL(data) packet type = DH5/DH1 -> 602.6/48 Kbps

10.3. Scatternet



eSCO packet type = EV5, Tesco = 32, Wesco = 0, ACL(data) packet type = DH1/DH1 -> 151.2/151.2 Kbps
All of the above numbers are theoretical.

11. Application examples

The special features of BRF6300 such as clock synchronization and optimum packet size determination, enables the device to support two other CODEC interfaces, which can be used for both voice and music transports.:

- Inter-IC Sound (I2S)
- UDI

These interfaces have different timing and data format requirements to the standard PCM codec interface described above.

11.1. Inter-IC Sound (I2S)

The BRF6300 can be configured as a Inter-IC Sound (I2S) serial interface to a I2S CODEC device. I2S is a serial bus designed for digital audio devices and technologies such as compact disc (CD) players, digital sound processors, and digital TV (DTV) sound.

The I2S bus consists of three serial bus lines: a line with two time-division multiplexing data channels (SD), a word select line (WS), and a continuous serial clock line (SCK). The BRF6300 implements this using its standard PCM lines, with FSYNC = WS, DATA_IN/OUT = SD and CLOCK = SCK. The BRF6300 can act as an I2S master (provides WS and SCK), or as an I2S slave (receives WS and SCK).

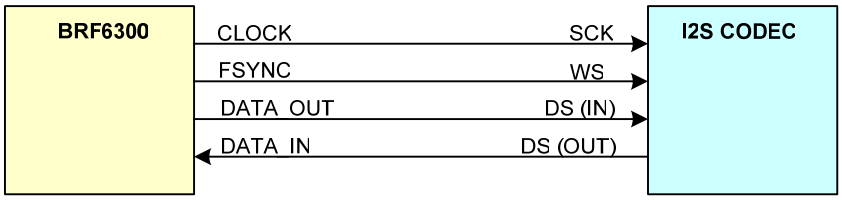


Figure 7: BRF6300 as I2S Master

The I2S link is implemented as a time division multiplexed (TDM) slot based serial interface, which is used to transfer audio data and command/status to or from the CODEC device. In this mode, the BRF6300 audio CODEC interface is configured as a bi-directional, full duplex interface, with two time slots per frame: Time slot 0 (WS low) is used for the left channel audio data and time slot 1 (WS high) for the right channel audio data.

The I2S interface handles the audio data separately from the clock signals. By separating the data and clock signals, time-related errors that cause jitter do not occur, thereby eliminating the need for anti-jitter devices.

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock, word-select signal and data. In complex systems however, there may be several transmitters and receivers, which makes it difficult to define the master. In such systems, there is usually a system master controlling digital audio data-flow between the various ICs. Transmitters have to generate data under the control of an external clock, and so act as slaves.

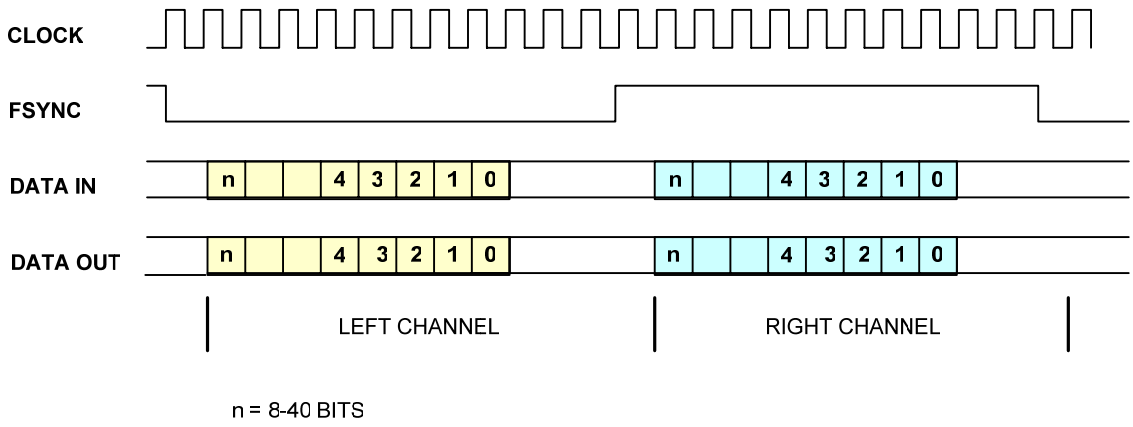


Figure 8: I2S signal format

In order to work in I2S configuration, SCL (IO2) is used for clock and SDA (IO3) for data. For more details see BRF6300 IO Configuration document. Also, in order to configure the correct timing, Fsync should have a duty cycle of 50%. Use HVI_VS_Write_Codec_Configuration_Island3.

HCI_VS_Write_Codec_Configuration_Island2 setting for I2S interface example:

- PCM clock rate – 0xC00 (3072 KHz)
- PCM clock direction – 0x0 (BRF6300 is Master)
- Frame sync frequency – 0x01 (8 KHz)
- Frame sync duty cycle – 0x05 (50% duty cycle)
- Frame sync direction – 0x0 (BRF6300 is Master)
- CH#1 data size – 0x10 (16 bit)
- CH#1 data offset – 0x00 (PCM clock cycle between the rising of frame sync and the first data bit.)
- CH#1 padding start – 0xFF (no padding)
- CH#1 padding value – 0x0

HCI_VS_Write_I2C_Register setting example:

- Slave ID – 0x1a (codec 2)
- PVT clock - 0 (pre scale clock divider factor)
- Working frequency – 0x0190 (400 khz)
- Sub address – 0x1e (an internal register address)
- Data length – 0x01 (1 byte)
- Data – "00" (one byte of data which is 00)

11.2. UDI

The UDI profile defines the protocols and procedures that are used by devices implementing UDI for the 3G mobile phone systems. e.g. device with Bluetooth connection to a 3G Handset, communicating via videophone over a 3G network. Up to 2 channels of UDI data can be supported. The data will be transferred via the CODEC interface using transparent mode and will be sent out using eSCO EV4 Bluetooth packets (EV5 is also selectable).

11.2.1. UDI over Bluetooth Characteristics

The 3G UDI characteristics are:

- UDI frame size = 10ms.
- Clock rate = 3.84MHz (usually).
- UDI packet size = 86 bytes.
- Data rate = 64 or 384 Kbps

Each 3G UDI packet consists of 80 data bytes and 6 header bytes. Only the UDI data (80 bytes) is transferred via the PCM bus. The host receives the 3G UDI packets, including header and data, and then sends the data only to the BRF6300 device via PCM. I.e, the BRF6300 gets the data only and transmits the data only, over the air.

The UDI data can be transferred via PCM using any bus configuration that will supply a data rate of 64 kbps.

UDI RF data is transferred using eSCO EV4 packets every 12 BT frames = 120 bytes every 15 msec = 64 Kbps. There may be up to 2 UDI channels.

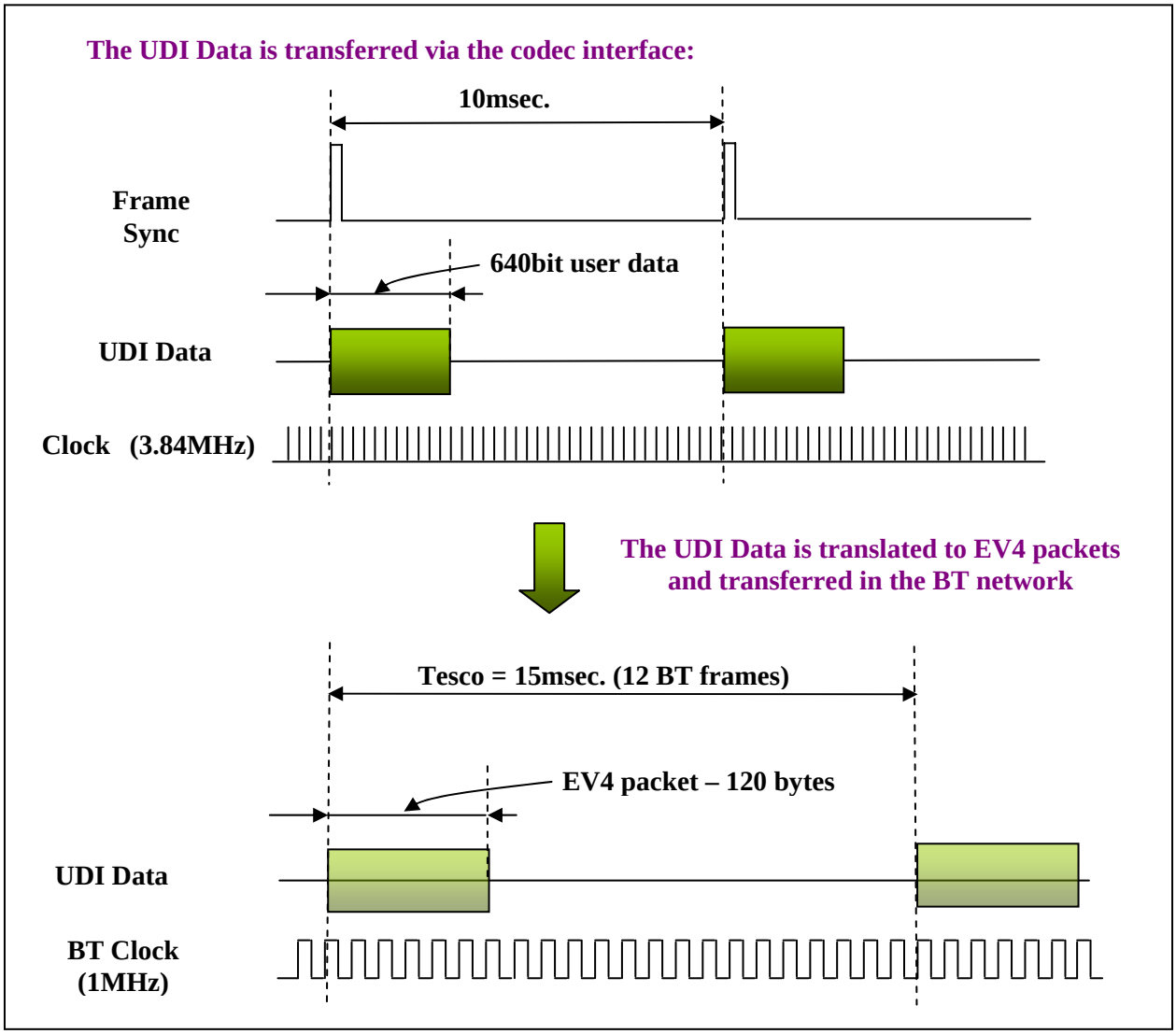


Figure 9 – Examples of transferring UDI data

11.2.2. UDI Support Requirements

To support the UDI profile, the BRF6300 has the following abilities:

Support clock rate of 3.84MHz as input and as output.

Note:
According to the UDI spec, the frequency accuracy of the PCM clock must be under 100ppm and the latency in the BT part should be under 50msec. The BRF6300 supports these requirements.

11.3. Stereo music and MP3 support

11.3.1. Stereo

If SCO/eSCO BT channel is supplied from 1 PCM channel, then the only option is mono (or dual mono if you got 2 speakers) supplied by the mono CODEC.
If SCO/eSCO BT channels are supplied from 2 PCM channels, then I2S configuration (described above) can be used to provide stereo music over 1 voice link.

BT 1.2 maximum rate is EV5 (TX 180 bytes over 3 slots + 1 slot RX).
i.e.: (180 * 8) / (3 * 625us + 625us) = 576 Kbps
Max stereo rate (assuming 16 bits per sample) would therefore be:
576kbps / 16bits / 2 chan = 18 Ksample/s.
With 3-EV5 EDR packets, this can be tripled to 54 Ksample/s.

These numbers are the maximum theoretical configuration that occupies the entire bandwidth. In real life, we must leave open slots for Scan, AFH classification, Signaling packets (LMP's) etc. So a more calculation is to leave 1 free frame for every eSCO packets (2 frames):
(180 * 8) / (3 * 625usec + 625usec + 1250usec) = 384kbps

Note that the PCM interface has Linear/CVSD digital filtering mechanism which limits the PCM to an audio frequency response bandwidth of 3.4KHz. To obtain the high sample/s data rate required by stereo music, transparent air mode must be used instead of the usually used CVSD. See BT specification HCI_Setup_Synchronous connection.

11.3.2. MP3

MP3 music can be transmitted as encoded (compressed) or decoded (uncompressed):
Transmitting decoded mp3 simply requires a very high rate eSCO channel.
Transmitting encoded mp3 requires a high data rate ACL channel and an MP3 decoder on the receiving side.

MP3 has 2 sample rate groups:

- 11.025, 22.05, 44.1 Ksample/sec
- 12k, 24, 48 Ksample/sec

Sample rate X number of bits/sample = channel rate:
e.g. 24 Ksample/s * 16 bits = 384 Kbps

e.g. 2 channels of 48 Ksample/s with 32 bits/sample = Channel rate of 1536Kbps of decoded MP3
= Channel rate of 512Kbps of encoded MP3

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