TCS2300 PROGRAM

(LOCOSTO)

Electrical Specifications

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Change History

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2006-Feb-16	AD		0.1		1
2006-Mar-8	SJ		0.5		2
2006-Apr-4	SJ	Internal review	0.6		3
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2006-Jul-25	FS	Program Manager	1.4		12
2006-Jul-31	FS	Program Manager	1.5		13
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2006-Sep-14	FS, AD	VV, FS	1.7		15
2006-Oct-5	FS	FS	1.8		16
2007-Oct-18	AD	DR, FS	1.9		17

Note:

(1) Creation
(2) Adding functional description for different interfaces and their timing parameters.
(3) Updating with comments from internal review.
(4) Updating with comments from internal review.
(5) a) Updating ckout_13mhz characteristics
b) Adding gpio mode specification for bq0031s cell.
c) Adding I2c timings.
(6) Updating with USB timings.
(7) Updating with comments from internal review.
(8) history page 4 removing internal names, remove “preliminary” comment and update version to 1.0
(9) Updating LCD interface section for RS pin description and timing parameters.
(10) Updating pads drive strength (Table 6)
(11) Chapter 4 (Package mechanical data) and 5 (Device nomenclature) created from chapter 4 of previous version (Package information). Addition in new chapter 5 of package marking and part-number generic coding + several examples.
(12) Addition of ESD ratings (chapter 7) and RF characteristics (Reference clock, Receiver and Transmitter) in chapter 25
(13) Addition of D6928BZPH (non-secure device) to the list of part-number available for ES2.0 production.
(14) Added functional block diagrams in Device description and RF chapters;
Added applicable silicon revision and DRP FirmWare script revision in Device description;
Power pin table clean-up and ball-out view addition
Absolute maximum ratings: operating temperature changed from -40/+85C to -25/+85C to match RF specification;
Updates for RF chapter:
Removed external crystal reference table: replaced by pointing application note APN221
Changed DCXO startup time: 2.5-5 to 5-12ms typ/max values
Changed TX output power in High-band: 2.5-4.5-6.5 to 2.5-5-8dB min/typ/max values
Changed output spectrum at 400kHz typ value: -67 to -66 in LB, -67 to -63 in HB

Changed RMS Phase Error typ value in HB: 2 to 2.5 deg
Added quick reference to dithering circuit app note number : APN224
Noise figure in blocking condition: 12dB specified room temp
IP2 in high: Min specified at 25dB
Remove several DRP design related parameters that are covered by RF global performance: DCXO supply voltage, DCXO consumption, DCXO max temp drift, 1dB input.

(15) Peak phase error in low-band changed to 14deg as in High-band. Peak phase error at device output (without PA) in RF Transmitter chapter
Phase Noise 20MHz in Low-band: Typ value changed from -166 to -164 dBc/Hz, Max value changed from -164 to -162.5 dBc/Hz in RF Transmitter chapter
Phase Noise 20MHz in High-band: Typ value changed from -158 to -156 dBc/Hz in RF Transmitter chapter.
IP3 specification changed from -21/-20/-19dBm Min-2/Min-1/Typ to -22/-21/-19dBm in RF receiver chapter
Spurs guaranteed on FTA channels
Added rise time, fall time details for SIM_RST, SIM_CLK, SIM_IO, SIM_PWRCTRL pins in “SIM Card” chapter.
Corrected maximum load for ckout_13Mhz pin from 10 pF to 100 pF in “Clocks,Reset and Power Management” chapter.
IDDQ leakage current specification added in Chapter 8.

(16) Phase Noise 20MHz in in Low-band: Typ value changed from -164 to -163 dBc/Hz, Max value changed from -162.5 to -160 dBc/Hz in RF Transmitter chapter.
Added reference to APN222 “RF band arrangement” in RF chapter for the mapping of the RF inputs for dual, tri and quad-band support
ESD ratings aligned with the level achieved for Locosto ES2.0 RTP
Device nomenclature section updated to reflect the part-number strategy change with 4 different part-number for production: dual-band EU, dual-band US, tri-band EU and quad-band (quad-band also covering tri-band US)

(17) F3 and F11 values for EMIF timing. Included Dissipation Rating Table. Updated ESD Ratings Section.

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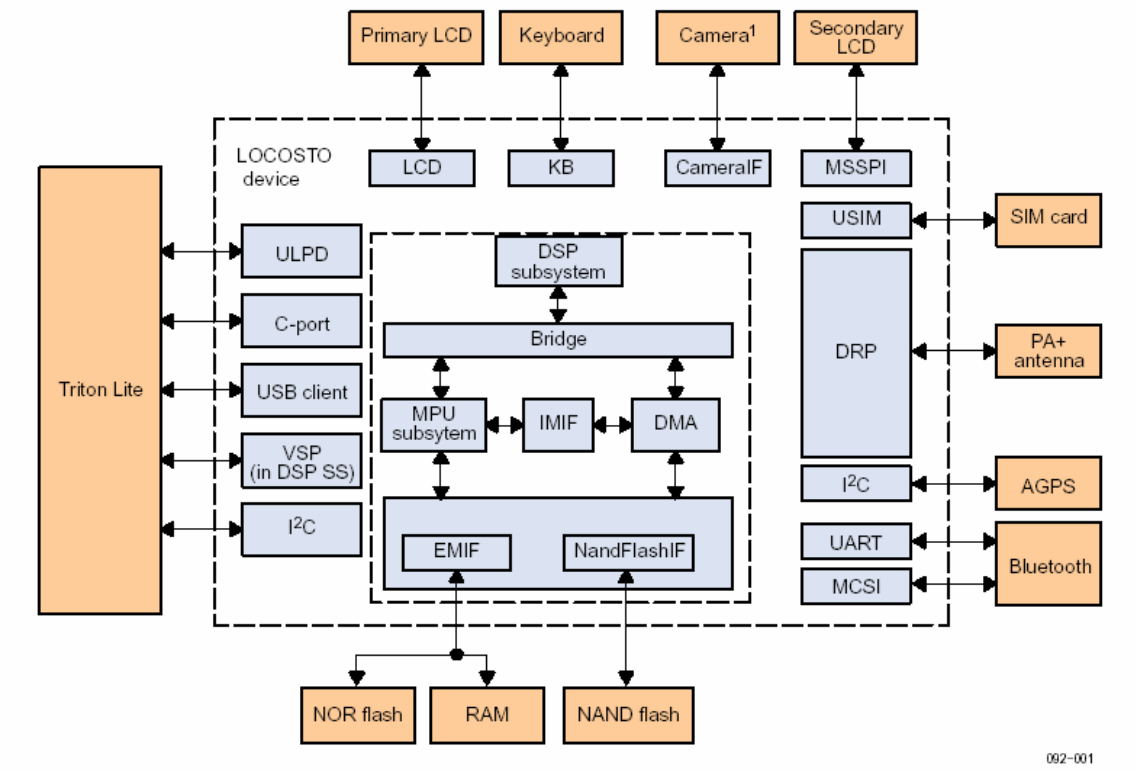
1 DEVICE OVERVIEW

Locosto device is an integrated solution that embeds on the same die a DBB (Digital Base Band) and a DRP (Digital radio processor). This device targets low cost GSM/GPRS solutions.

The DRP part is a digital RF transceiver that support up to GPRS class12. It is designed for Quad band operation supporting both the European and the US bands (E-GSM 900 and DCS 1800 bands, GSM 850 and PCS 1900 bands respectively).

The DBB supports the processing of GSM radio signals in switching circuit mode and packet data mode (GPRS) for up to class 12, including evolution such as SAIC & localization system (A-GPS) in compliance with the ETSI specification. Locosto's silicon process technology is a c027 90 nm digital CMOS.



Two versions of Locosto can be distinguished: Locosto and Locosto Lite**.**

Locosto Lite device is a lighter version of Locosto device. This document details the features of Locosto and Locosto Lite. However, when "Locosto" is mentioned, this refers to both Locosto and Locosto Lite devices, except when the contrary is specified.

This document applies up to ES2.0 silicon revision.
RF transceiver performance is guaranteed with associated FirmWare (running on DRP script processor): revision 137.05.03.

2 SIGNAL PINS

Pin Number	BGA Address	Power Domain	BGA Name	PUPD(*) Type	DIR	IO Cell
1	T2	vdd_io_1	trstn	PUPD	I	BQ0066S
2	M6	vdd_io_1	gpio_0	PU	IO	BC1850CSHYPU
3	U2	vdd_io_1	spare_2		IO	BC1825DS
4	K8	vdd_io_1	gpio_1	PUPD	IO	BQ0062S
5	T3	vdd_io_1	gpio_2	PUPD	IO	BQ0054S
7	R4	vdd_io_1	i2c_scl		IO	BQ0045S
8	N6	vdd_io_1	i2c_sda		IO	BQ0045S
9	T4	vdd_io_1	Usb_rcv	PD	I	IC18SHYPD
10	L8	vdd_io_1	Usb_se0	PU	IO	BC1850CSHYPU
11	R5	vdd_io_1	Usb_dat	PUPD	IO	BQ0057S
12	M7	vdd_io_1	Usb_txen		O	OC1825DS
13	N7	vdd_io_1	Scl_trit		IO	BQ0045S
14	R6	vdd_io_1	Sda_trit		IO	BQ0045S
15	K9	vdd_io_1	vfsrx	PD	I	IC18SHYPD
17	M8	vdd_io_1	vdr	PD	I	IC18SHYPD
18	T6	vdd_io_1	vdx		O	OC1850CS
20	R7	vdd_io_1	vclkrx		I	IC18SHYPD
21	P8	vdd_io_1	abb_irq	PU	IO	BC1850CSHYPU
23	T7	vdd_io_1	ck13mhz_en	PU	I	IC18SHYPU
24	N8	vdd_io_1	Ckout_13mhz		O	OC1825DS
26	R8	vdd_io_1	wakeup_req		O	OC1850CS
27	T8	vdd_io_1	ckin_32khz		I	IC18SHY
28	M9	vdd_io_1	csync	PD	IO	BC1850CSHYPD
29	P9	vdd_io_1	csclk	PD	IO	BC1850CSHYPD
30	T9	vdd_io_1	cdo		O	OC1850CS
31	R9	vdd_io_1	gpio_4	PUPD	IO	BQ0055S
32	N9	vdd_io_1	gpio_5	PUPD	IO	BQ0055S
33	T10	vdd_io_1	Usb_boot		IO	BC1825DS
35	N10	vdd_rst	on_noff		I	IQ0041S
37	T11	pbias out	sim_pbias		IO	BAFTHRUDDS(3)
38	P10	vdd_usim	Sim_clk	PUPD	O	BQ0242S
40	R11	vdd_usim	Sim_io	PUPD	IO	BQ0242S
43	M10	vdd_usim	sim_pwrctrl	PUPD	O	BQ0242S
44	N11	vdd_usim	Sim_rst	PUPD	O	BQ0242S
46	R12	vdd_apc	apcldofilter		IO	APCV0P1
47	L9	vdd_apc	apcspare1		IO	APCV0P1
48	M11	vdd_apc	apcout		IO	APCV0P1
49	R13	vdd_apc	apcvref		IO	APCV0P1
52	T17		anatst1		IO	SC_DRP2_V1P0_GS50
53	U17		anatst2		IO	SC_DRP2_V1P0_GS50
54	U15		xanatst3		IO	SC_DRP2_V1P0_GS50

55	U16		xanatst4		IO	SC_DRP2_V1P0_GS50
56	T16		xanatst5		IO	SC_DRP2_V1P0_GS50
57	R17		xanatst6		IO	SC_DRP2_V1P0_GS50
64	R16		vref1		I	SC_DRP2_V1P0_GS50
65	R15		iref		O	SC_DRP2_V1P0_GS50
70	N17		rxgsmm		I	SC_DRP2_V1P0_GS50
72	M16		rxegsmm		I	SC_DRP2_V1P0_GS50
73	L16		rxegsmp		I	SC_DRP2_V1P0_GS50
75	M17		rxgsmp		I	SC_DRP2_V1P0_GS50
77	L17		rxdcsp		I	SC_DRP2_V1P0_GS50
79	K16		rxpcsp		I	SC_DRP2_V1P0_GS50
80	J16		rxpcsm		I	SC_DRP2_V1P0_GS50
82	K17		rxdcsm		I	SC_DRP2_V1P0_GS50
94	G17		txhb		O	SC_DRP2_V1P0_GS50
96	F17		txlb		O	SC_DRP2_V1P0_GS50
99	E17		vref		O	SC_DRP2_V1P0_GS50
102	D15		xtal		I	SC_DRP2_V1P0_GS50
105	G11	vdd_io_2	kbc_0		O	OC1850CS
106	C16	vdd_io_2	kbc_1		O	OC1850CS
108	E13	vdd_io_2	kbc_2		O	OC1850CS
109	C15	vdd_io_2	kbc_3		O	OC1850CS
111	B16		i_force		I	IPMCSWS(2)
112	F12	vdd_io_2	tspact_11		IO	BQ0021S
113	A16		sense		O	OPMCSWS(2)
114	H10	vdd_io_2	tspact_12		IO	BQ0021S
117	C14	vdd_io_2	tspact_13		IO	BQ0021S
118	E12	vdd_io_2	tspact_14		IO	BQ0021S
120	G10	vdd_io_2	tspact_15		IO	BQ0021S
122	F11	vdd_io_2	kbr_0	PUPD	IO	BQ0055S
123	E11	vdd_io_2	kbr_1	PUPD	IO	BQ0055S
124	C12	vdd_io_2	kbr_2	PUPD	IO	BQ0055S
125	H9	vdd_io_2	kbr_3	PUPD	IO	BQ0055S
127	F10	vdd_io_2	kbr_4	PUPD	IO	BQ0055S
128	B12	vdd_io_2	kbc_4	PUPD	IO	BQ0054S
130	C11	vdd_io_2	nemu0	PUPD	IO	BQ0062S
131	D10	vdd_io_2	nemu1	PUPD	IO	BQ0062S
133	B11	vdd_io_2	gpio_12	PUPD	IO	BQ0062S
134	E10	vdd_io_2	gpio_13	PUPD	IO	BQ0055S
136	C10	vdd_io_2	Lcd_nrst	PD	IO	BC1850CSHYPD
137	B10	vdd_io_2	Lcd_stb	PUPD	IO	BQ0077S
138	F9	vdd_io_2	Lcd_rnw	PUPD	IO	BQ0077S
139	D9	vdd_io_2	Lcd_rs	PUPD	IO	BQ0054S
140	B9	vdd_io_2	gpio_17	PUPD	IO	BQ0054S
142	E9	vdd_io_2	lcd_data_0		IO	BC1825DSHY
143	B8	vdd_io_2	lcd_data_1		IO	BC1825DSHY

144	C8	vdd_io_2	lcd_data_2		IO	BC1825DSHY
145	E8	vdd_io_2	lcd_data_3		IO	BC1825DSHY
147	B7	vdd_io_2	lcd_data_4		IO	BC1825DSHY
148	D8	vdd_io_2	lcd_data_5		IO	BC1825DSHY
150	C7	vdd_io_2	lcd_data_6		IO	BC1825DSHY
151	B6	vdd_io_2	lcd_data_7		IO	BC1825DSHY
152	A6	vdd_io_2	gpio_18	PUPD	IO	BQ0077S
153	F8	vdd_io_2	gpio_19	PU	IO	BQ0031S.1
154	E7	vdd_io_2	gpio_20	PU	IO	BQ0031S.2
155	A5	vdd_io_2	gpio_21	PU	IO	BQ0031S.1
156	C6	vdd_io_2	gpio_22	PU	IO	BQ0031S.2
157	G9	vdd_io_2	gpio_23	PD	IO	BC1825DSHYPD
158	F7	vdd_io_2	gpio_24	PD	IO	BC1825DSHYPD
159	C5	vdd_io_2	gpio_25	PD	IO	BC1825DSHYPD
160	E6	vdd_io_2	gpio_26	PUPD	IO	BQ0054S
161	G8	vdd_io_2	gpio_27	PUPD	IO	BQ0054S
163	C4	vdd_io_2	gpio_28	PU	IO	BC1825DSHYPU
165	G7	vdd_io_2	gpio_29	PD	IO	BC1825DSHYPD
166	B3	vdd_io_2	gpio_30	PD	IO	BC1825DSHYPD
167	A2	vdd_io_2	tms	PUPD	I	BQ0066S
168	E5	vdd_io_2	nd_nwp		IO	BC1825DSHY
169	C3	vdd_io_2	gpio_31	PU	IO	BC1825DSHYPU
170	A1	vdd_io_2	tck	PUPD	I	BQ0066S
171	B2	vdd_io_2	tdo		O	OQ0028S
172	F6	vdd_io_2	gpio_32	PD	IO	BC1825DSHYPD
173	B1	vdd_io_2	tdi	PUPD	I	BQ0066S
174	H8	vdd_io_2	gpio_33	PD	IO	BC1825DSHYP
175	C2	vdd_io_2	gpio_34	PU	IO	BC1825DSHYPU
177	D3	vdd_io_2	Nd_ce1		O	OC1825DS
178	F5	vdd_io_2	gpio_35	PU	IO	BC1825DSHYPU
179	D2	vdd_io_2	gpio_36	PU	IO	BC1825DSHYPU
180	H7	vdd_io_2	gpio_37	PD	IO	BC1825DSHYPD
181	E3	vdd_io_2	ncs0	PU	IO	BC1825DSHYPU
182	G6	vdd_io_2	gpio_7	PD	IO	BC1825DSHYPD
183	G5	vdd_mif	gpio_39	PD	IO	BC1825DSHYPD
184	F3	vdd_mif	add_21	PD	IO	BC1825DSHYPD
185	J8	vdd_mif	add_20		O	OC1825DS
187	H6	vdd_mif	add_19		O	OC1825DS
188	F2	vdd_mif	add_18		O	OC1825DS
189	F1	vdd_mif	add_17		O	OC1825DS
190	G3	vdd_mif	add_16		O	OC1825DS
191	H4	vdd_mif	add_data_15		IO	BC1825DS
192	G1	vdd_mif	add_data_14		IO	BC1825DS
193	G2	vdd_mif	add_data_13		IO	BC1825DS
194	H5	vdd_mif	add_data_12		IO	BC1825DS

196	H3	vdd_mif	add_data_11		IO	BC1825DS
197	H2	vdd_mif	add_data_10		IO	BC1825DS
198	J6	vdd_mif	add_data_9		IO	BC1825DS
199	J4	vdd_mif	add_data_8		IO	BC1825DS
200	J2	vdd_mif	add_data_7		IO	BC1825DS
201	J3	vdd_mif	add_data_6		IO	BC1825DS
202	J5	vdd_mif	add_data_5		IO	BC1825DS
203	K2	vdd_mif	add_data_4		IO	BC1825DS
204	K3	vdd_mif	add_data_3		IO	BC1825DS
205	K5	vdd_mif	add_data_2		IO	BC1825DS
207	L2	vdd_mif	add_data_1		IO	BC1825DS
208	K4	vdd_mif	add_data_0		IO	BC1825DS
209	L1	vdd_io_1	rnw		O	OC1825DS
210	L3	vdd_io_1	nbhe		O	OC1825DS
211	M2	vdd_io_1	nble		O	OC1825DS
212	M1	vdd_io_1	nmoe		O	OC1825DS
213	K6	vdd_io_1	fdp		O	OC1825DS
214	L5	vdd_io_1	ncs3		O	OC1825DS
216	M3	vdd_io_1	nrdy	PU	IO	BC1850CSHYPU
217	J7	vdd_io_1	adv	PU	IO	BC1850CSHYPU
218	L6	vdd_io_1	gpio_42	PU	IO	BC1825DSHYPU
219	N3	vdd_io_1	gpio_43	PU	IO	BC1825DSHYPU
220	M5	vdd_io_1	gpio_44	PU	IO	BC1825DSHYPU
221	K7	vdd_io_1	gpio_45	PU	IO	BC1825DSHYPU
222	P2	vdd_io_1	gpio_46	PU	IO	BC1825DSHYPU
223	P3	vdd_io_1	uart_tx		O	OC1825DS
225	L7	vdd_io_1	uart_rx	PD	IO	BC1825DSHYPD
226	R2	vdd_io_1	uart_cts	PD	IO	BC1825DSHYPD
227	T1	vdd_io_1	nbscan	PU	I	IC18SHYPU
228	N5	vdd_io_1	gpio_47	PU	IO	BC1850CSHYPU
229	R3	vdd_io_1	rts_sdirda		O	OC1825DS
230	U1	vdd_io_1	spare_3	PU	IO	BC1825DSHYPU

(*) – PU = Pull up, PD = Pull down.
Note: (1) For Pull reset state and pins multiplexed see LOCOSTO TRM
(2) For TI internal test only. Not to be connected on board
(3) To be kept open

Feedthru pad: BAFTHRUDDS

Table 1 : Signal Pins Description

3 POWER PINS

Power name	Description
VDD_DBB	DBB core voltage
VDDR1	DRP_VR1 domain
VDDR2	DRP_VR2 domain.
VDD_MIF	External memory I/O bus supply
VDD_USIM	USIM I/O bus supply.
VDD_IO_1*	Generic IO power supply 1
VDD_IO_2*	Generic IO power supply 2
VDD_RST	Reset input cell power supply
VDD_PLL	DPLL/APLL subchip dedicated power supply inside DBB
APC_VDO	APC module power supply
VDDX (Decoupling)	Internal LDO_DCXO regulator output. Used to connect to filter capacitor
VDDOSC (Decoupling)	Internal LDO_OSC regulator output. Used to connect to filter capacitor.
VDDRF (Decoupling)	Internal LDO_RF regulator output. Used to connect to filter capacitor
VDDA (Decoupling)	Internal LDO_ANA regulator output. Used to connect to filter capacitor

(*) VDD_IO_1 and VDD_IO_2 are available as separate IO ring structures . They can either be used separately or can be connected together at the board.

Table 2 : Power Domains

BGA Address	BGA Name
U3, U7	vdd_io_1
U10	vdd_rst
U11	Vsspbias
T12	vdd_usim
L9, U13	apc_vdo
N13	apc_vss
N15,M13	Vssa
P15,P16	Vdda
T15	vddr1rx1
M13, N15	Vssa
M15,L13,K14,K15,L15	vssrf
H17	vddrf
J15,J14,H15	vssosc
H16	vddosc
H14,G15	Vssrf1
G16	Vddrf1
F16	vddr1tx1
F15	Vddr2
E15	Vssx

D16	Vddx
A17, B17	Vpp
A15, C9, A3	vdd_io_2
B14	vss_pll
C13	vdd_pll
A13, A11, A8, B4, N1, B15, R10, U6	vdd_dbb
A12, A10, A7, C1, R1, H1, T14, R14, U5, U8, U12, C17	Vss
E1, K1	vdd_mif

Table 3: Power pins

4 PACKAGE MECHANICAL DATA

- **Series**: µStar-BGA
- **Balls**: 241
- **Pitch**: 0.50 mm.
- **Height**: 1.20 mm.
- **SQ size:** 10.00x10.00 mm^2.

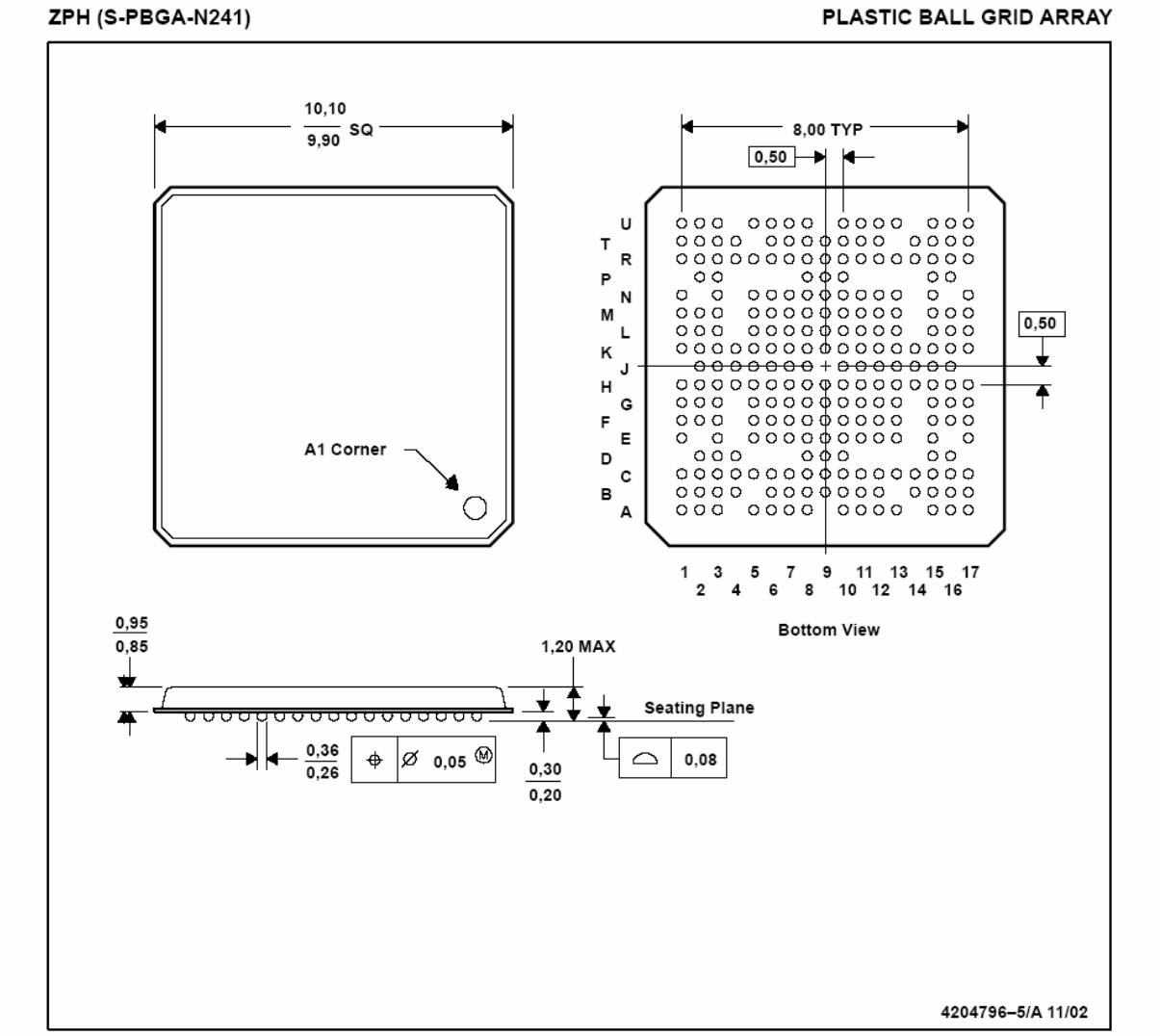


Figure 1 : Mechanical Dimensions for the Locosto Package

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Dissipation rating table for a maximum T_J = 125°C (Model : Free air)					
Package	T_A < 30°C Power rating	Thermal resistance J-to-A Above T_A = 30°C	T_A = 50°C Power rating	T_A = 70°C Power rating	T_A = 85°C Power rating
241-ZPH	3.05W	31.1°C/W (2S2P)	2.41W	1.77W	1.29W

Table 4 : Dissipation Rating Table (for $T_{J\text{-}MAX}$ = 125°C)

Ballout view:

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
U	anatst2	xanatst4	xanatst3	NoBall	apc_vdo	vss	vsspbias	vdd_rst	NoBall	vss	vdd_io	vdd_dbb	vss	NoBall	vdd_io	spare_2	spare_3
T	anatst1	xanatst5	vddr1rx1	vss	NoBall	vdd_usim	sim_pbias	usb_boot	cdo	ckin_32khz	ck13mhz_en	vdx	NoBall	usb_rcv	gpio_2	trstn	nbscan
R	xanatst6	vref1	iref	Reserved	apcvref	apcldofilter	sim_io	vdd_dbb	gpio_4	wakeup_req	vclkrx	sda_trit	usb_dat	i2c_scl	rts_sdirda	uart_cts	vss
P	NoBall	vdda	vdda	NoBall	NoBall	NoBall	NoBall	sim_clk	csclk	abb_irq	NoBall	NoBall	NoBall	NoBall	uart_tx	gpio_46	NoBall
N	rxgsmm	NoBall	vssa	NoBall	apc_vss	NC	sim_rst	on_noff	gpio_5	ckout_13mhz	scl_trit	i2c_sda	gpio_47	NoBall	gpio_43	NoBall	vdd_dbb
M	rxgsmp	rxegsmm	vssrf	NoBall	vssa	NC	apcout	sim_pwrctrl	csync	vdr	usb_txen	gpio_0	gpio_44	NoBall	nrdy	nble	nmoe
L	rxdcsp	rxegsmp	vssrf	NoBall	vssrf	NC	NC	NC	apcspare1	usb_se0	uart_rx	gpio_42	ncs3	NoBall	nbhe	add_data_1	rnw
K	rxdcsm	rxpcsp	vssrf	vssrf	NC	NC	NC	NC	vfsrx	gpio_1	gpio_45	fdp	add_data_2	add_data_0	add_data_3	add_data_4	vdd_mif
J	NoBall	rxpcsm	vssosc	vssosc	NC	NC	NC	NC	NoBall	add_20	adv	add_data_9	add_data_5	add_data_8	add_data_6	add_data_7	NoBall
H	vddrf	vddosc	vssosc	vssrf1	NC	NC	NC	tspact_12	kbr_3	gpio_33	gpio_37	add_19	add_data_12	add_data_15	add_data_11	add_data_10	vss
G	txhb	vddrf1	vssrf1	NoBall	NC	NC	kbc_0	tspact_15	gpio_23	gpio_27	gpio_29	gpio_7	gpio_39	NoBall	add_16	add_data_13	add_data_14
F	txlb	vddr1tx1	vddr2	NoBall	NC	tspact_11	kbr_0	kbr_4	lcd_rnw	gpio_19	gpio_24	gpio_32	gpio_35	NoBall	add_21	add_18	add_17
E	vref	NoBall	vssx	NoBall	kbc_2	tspact_14	kbr_1	gpio_13	lcd_data_0	lcd_data_3	gpio_20	gpio_26	nd_nwp	NoBall	ncs0	NoBall	vdd_mif
D	NoBall	vddx	xtal	NoBall	NoBall	NoBall	NoBall	nemu1	lcd_rs	lcd_data_5	NoBall	NoBall	NoBall	Reserved	nd_ce1	gpio_36	NoBall
C	vss	kbc_1	kbc_3	tspact_13	vdd_pll	kbr_2	nemu0	lcd_nrst	vdd_io	lcd_data_2	lcd_data_6	gpio_22	gpio_25	gpio_28	gpio_31	gpio_34	vss
B	vpp	i_force	vdd_dbb	vss_pll	NoBall	kbc_4	gpio_12	lcd_stb	gpio_17	lcd_data_1	lcd_data_4	lcd_data_7	NoBall	vdd_dbb	gpio_30	tdo	tdi
A	vpp	sense	vdd_io	NoBall	vdd_dbb	vss	vdd_dbb	vss	NoBall	vdd_dbb	vss	gpio_18	gpio_21	NoBall	vdd_io	tms	tck

5 Device nomenclature

5.1 Pre-production devices

The package symbolization and SAP part-number convention apply to the devices available before release to production of the dual-band EU device.

5.1.1 Standard package symbolization

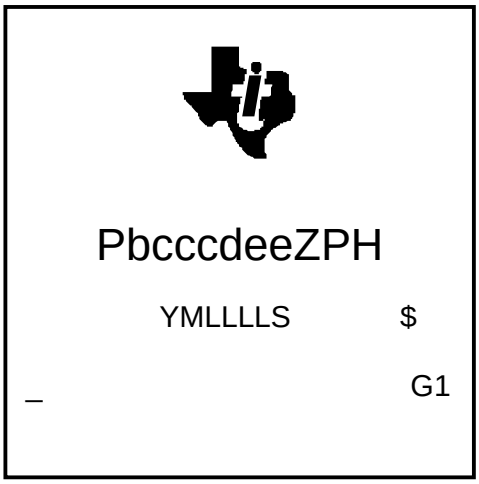


Figure 2 : Printed Device References

Fields	Meaning
P	Marking used to note pre-production device
b	Process version descriptor (c035 = 5, c027 = 6)
ccc	Locosto device type: Locosto-lite = 928, Locosto-Plus = 553
d	Mask set version description: initial silicon = “BLANK”, first silicon revision = A, second silicon revision = B, ….)
ee	Two characters “Customer code” set to differentiate customer for custom secure devices (Table driven). “BLANK” if not custom/secure device
YMLLLLS	Date (Y= Year, M = Month) & Lot code
$	Fab planning code (UMC12A = $N)
G1	E-CAT category
-	PIN1 indicator

Note: BLANK in the symbol or part-number is collapsed so there are no gaps between characters.

5.1.2 SAP part number

The actual part-number used in the system will follow this syntax:

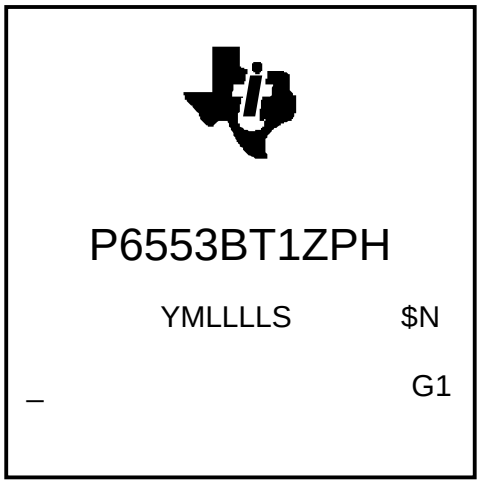
SAP P/N = PbcccdeeZPHf

Fields	Meaning
P	Marking used to note pre-production device (P)
b	Process version descriptor (c027 = 6)
ccc	Locosto device type: Locosto-lite = 928, Locosto-Plus = 553
d	Mask set version description: initial silicon = “BLANK”, first silicon revision = A, second silicon revision = B, ….)
ee	Two characters “Customer code” set to differentiate customer for custom secure devices (Table driven). “BLANK” if not custom/secure device
f	Shipping method: Trays = “BLANK”, Tape&Reel = “R”

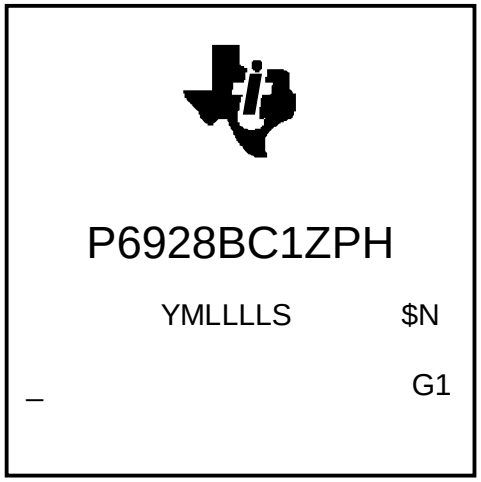
Note: BLANK in the symbol or part-number is collapsed so there are no gaps between characters.

5.1.3 Examples

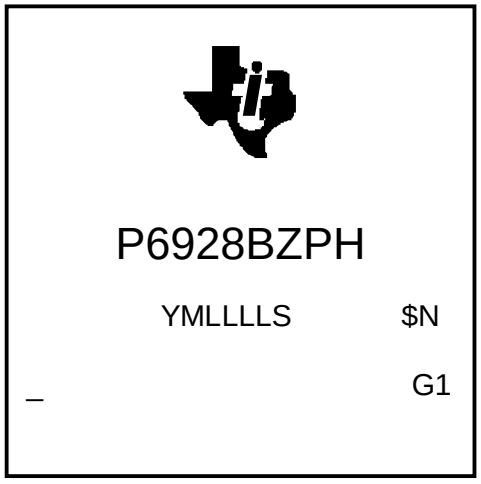
Example 1: Locosto-Plus ES2.0 silicon revision, pre-production, secure device with TI keys 1
SAP P/N: P6553BT1ZPH (Tray delivery method)
SAP P/N: P6928BT1ZPHR (Tape & Reel delivery method)



Example 2: Locosto-Lite ES2.0 silicon revision, pre-production, custom/secure device for customer C key file 1
SAP P/N: P6928BC1ZPH (Tray delivery method)
SAP P/N: P6928BC1ZPHR (Tape & Reel delivery method)



Example 3: Locosto-Lite ES2.0 silicon revision, pre-production, non custom/secure device.
SAP P/N: P6928BZPH (Tray delivery method)
SAP P/N: P6928BZPHR (Tape & Reel delivery method)



5.2 Dual-band EU devices for 1st production version

The package symbolization and SAP part-number convention apply to the dual-band EU production/qualified devices. It is limited to the 1st version in production on ES2.0 silicon.

Next production version (DRP Firmware or silicon change) will have package symbolization and SAP part-number convention aligned with other bands devices as described in chapter

5.2.1 Package symbolization

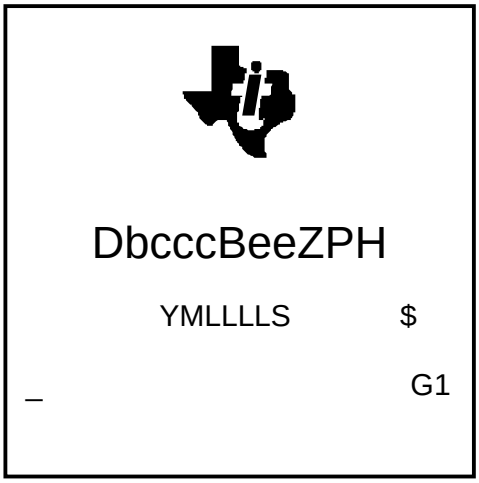


Figure 3 : Printed Device References

Fields	Meaning
D	Marking used to note qualified/production device (D)
b	Process version descriptor (c027 = 6)
ccc	Locosto device type: Locosto-lite = 928, Locosto-Plus = 553
B	Mask set version description: ES2.0 = B
ee	Two characters “Customer code” set to differentiate customer for custom secure devices (Table driven). “BLANK” if not custom/secure device
YMLLLLS	Date (Y= Year, M = Month) & Lot code
$	Fab planning code (UMC12A = $N)
G1	E-CAT category
-	PIN1 indicator

Note: BLANK in the symbol or part-number is collapsed so there are no gaps between characters.

5.2.2 SAP part number

The actual part-number used in the system will follow this syntax:

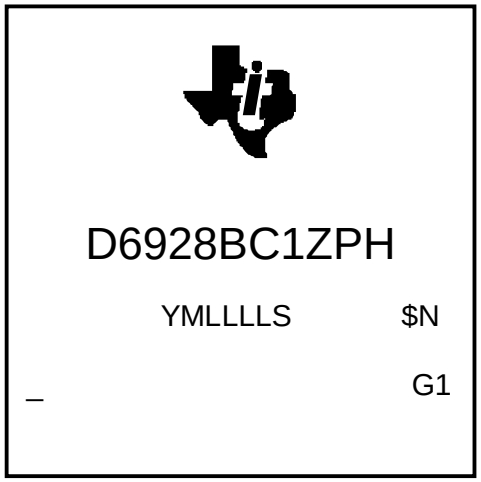
SAP P/N = DbcccBeeZPHf

Fields	Meaning
D	Marking used to note qualified/production device (D)
b	Process version descriptor (c035 = 5, c027 = 6)
ccc	Locosto device type: Locosto-lite = 928, Locosto-Plus = 553
B	Mask set version description: initial silicon = “BLANK”, first silicon revision = A, second silicon revision = B, ….)
ee	Two characters “Customer code” set to differentiate customer for custom secure devices (Table driven). “BLANK” if not custom/secure device
f	Shipping method: Trays = “BLANK”, Tape&Reel = “R”

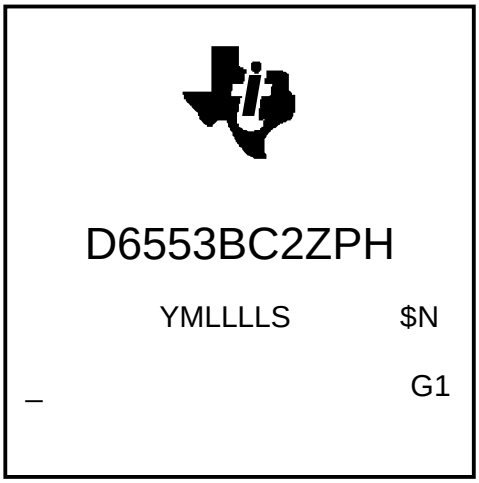
Note: BLANK in the symbol or part-number is collapsed so there are no gaps between characters.

5.2.3 Examples

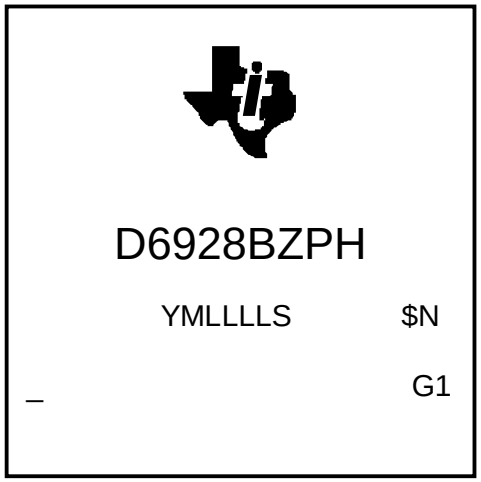
Example 1: Locosto-Lite ES2.0 silicon revision, production/qualified, custom/secure device for customer C key file 1
SAP P/N: D6928BC1ZPH (Tray delivery method)
SAP P/N: D6928BC1ZPHR (Tape & Reel delivery method)



Example 2: Locosto-Plus ES2.0 silicon revision, production/qualified, custom/secure device for customer C key file 2
SAP P/N: D6553BC2ZPH (Tray delivery method)
SAP P/N: D6928BC2ZPHR (Tape & Reel delivery method)



Example 3: Locosto-Lite ES2.0 silicon revision, production/qualified, non custom/secure device.
SAP P/N: D6928BZPH (Tray delivery method)
SAP P/N: D6928BZPHR (Tape & Reel delivery method)



5.3 Dual, Tri, Quad band devices

The package symbolization and SAP part-number convention below apply to all devices except the exceptions listed in previous chapters (Pre-production devices and dual-band EU 1st production version).

5.3.1 Standard package symbolization

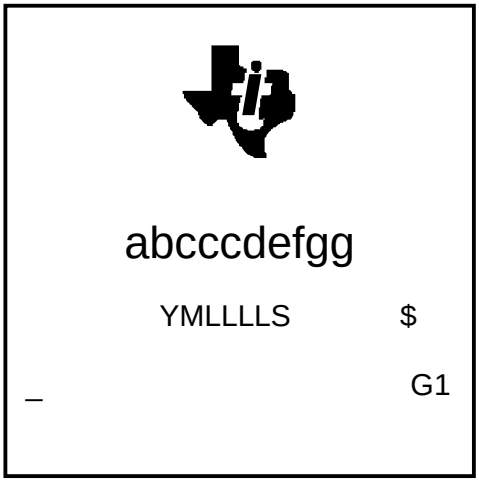


Figure 4 : Printed Device References

Fields	Meaning
P	Marking used to note pre-production device (P) or production/qualified devices (D)
b	Process version descriptor (c027 = 6)
ccc	Locosto device type: Locosto-lite = 928, Locosto-Plus = 553, Locosto = 591
d	Mask set version description: initial silicon = “BLANK”, first silicon revision = A, second silicon revision = B, ….)
e	GSM bands indicator (Dual-band EU = “BLANK”, Dual-Band US = “U”, Tri-Band EU = “T”, Tri-Band US and Quad-band = “Q”
f	DRP FirmWare revision: initial revision = “BLANK”, first revision = “A”, ...etc
gg	Two characters “Customer code” set to differentiate customer for custom secure devices (Table driven). “BLANK” if not custom/secure device
YMLLLLS	Date (Y= Year, M = Month) & Lot code
$	Fab planning code (UMC12A = $N)
G1	E-CAT category
-	PIN1 indicator

Note: BLANK in the symbol or part-number is collapsed so there are no gaps between characters.

5.3.2 SAP part number

The actual part-number used in the system will follow this syntax:

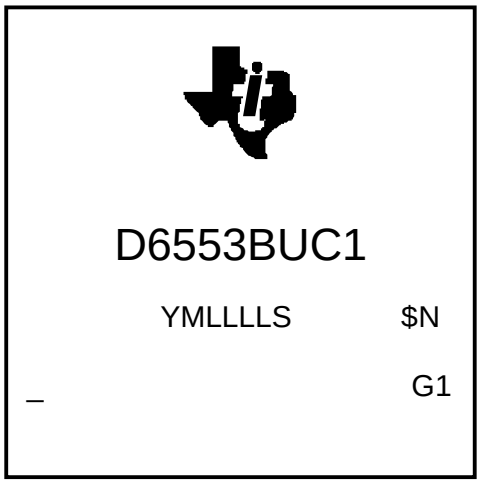
SAP P/N = abcccdefggZPHf

Fields	Meaning
P	Marking used to note pre-production device (P)
b	Process version descriptor (c035 = 5, c027 = 6)
ccc	Locosto device type: Locosto-lite = 928, Locosto-Plus = 553
d	Mask set version description: initial silicon = “BLANK”, first silicon revision = A, second silicon revision = B, ….
e	GSM bands indicator (Dual-band EU = “BLANK”, Dual-Band US = “U”, Tri-Band EU = “T”, Tri-Band US and Quad-band = “Q”
f	DRP FirmWare revision: initial revision = “BLANK”, first revision = “A”, ...etc
gg	Two characters “Customer code” set to differentiate customer for custom secure devices (Table driven). “BLANK” if not custom/secure device
f	Shipping method: Trays = “BLANK”, Tape&Reel = “R”

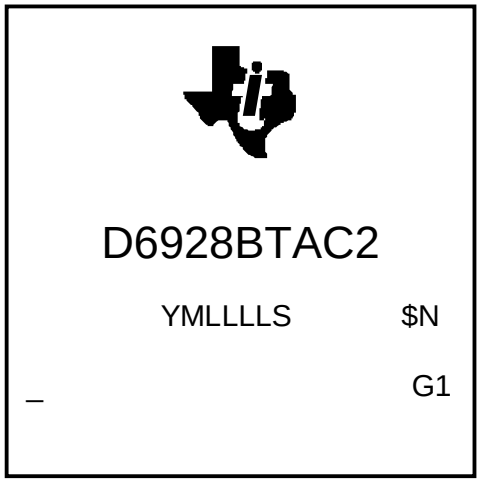
Note: BLANK in the symbol or part-number is collapsed so there are no gaps between characters.

5.3.3 Examples

Example 1: Locosto-Plus ES2.0 silicon revision, production/qualified device, dual-band US, initial FirmWare revision, custom device for customer C with key file 1
SAP P/N: D6553BUC1ZPH (Tray delivery method)
SAP P/N: D6553BUC1ZPHR (Tape & Reel delivery method)

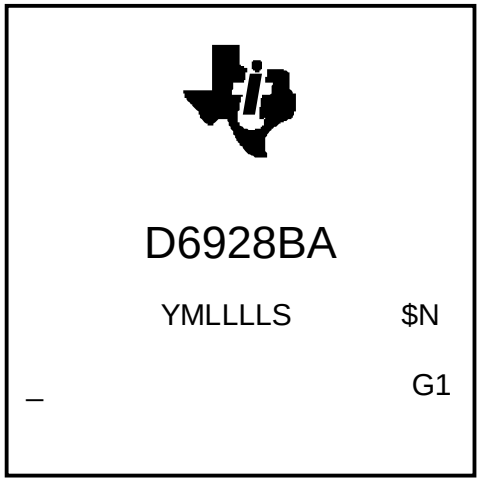


Example 2: Locosto-Lite ES2.0 silicon revision, production/qualified, Tri-band Eu, 1st firm-ware revision, custom/secure device for customer C key file 2,
SAP P/N: D6928BTAC2ZPH (Tray delivery method)
SAP P/N: D6928BTAC2ZPHR (Tape & Reel delivery method)



Example 3: Locosto-Lite ES2.0 silicon revision, production/qualified, non custom/secure device, quad-band
SAP P/N: D6928BQZPH (Tray delivery method)
SAP P/N: D6928BQZPHR (Tape & Reel delivery method)

Example 4: Locosto-Lite ES2.0 silicon revision, production/qualified, non custom/secure device, dual-band EU, firmware 1st revision
SAP P/N: D6928BAZPH (Tray delivery method)
SAP P/N: D6928BAZPHR (Tape & Reel delivery method)



6 ABSOLUTE MAXIMUM RATINGS

The list of absolute maximum ratings is specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All supply voltage values (core and I/O) are with respect VSS.

This section provides the absolute maximum ratings for the LOCOSTO device.

Parameter	Min	Max
Supply voltage range (core), CV_{DD}	-0.5 V	1.7V
Supply voltage range DV_{DD} , DV_{DDDPLL}	-0.5 V	DV_{DD} + 0.5 V
Supply voltage range $DV_{DDS1\ to\ 2}$	-0.5 V	DV_{DDS} + 0.5 V
Input voltage range, VI (26Mhz and 32-kHz oscillator)	-0.5 V	DV_{DDS} + 0.5 V
Input voltage range, VI(standard LVCMOS)	-0.5 V	DV_{DDS} + 0.5 V
Input voltage range, VI (I2C)	-0.5 V	DV_{DDS} + 0.5 V
Output voltage range, VO (standard LVCMOS)	-0.5 V	DV_{DDS} + 0.5 V
USIM voltage range, VO(USIM)	-0. 5V	DV_{DDS}’(*) + 0.5
Output voltage range, VO (I2C)	-0.5 V	DV_{DDS} + 0.5 V
Operating free air temperature range, TC	-25 °C	85 °C
Storage temperature range, Tstg	-65 °C	150 °C

(*) DVDDS could be 1.8V or 2.8 V
Notes : 1) Refer section 22 for APC specifications
2) Refer section 23 for DRP specifications

Table 5 : Absolute Maximum Ratings

7 ESD RATINGS

ESD Method	Standard Reference	Pin Name	Ball Location	x6553BxxZPH x6928BxxZPH x6591BxxZPH	TI Standard Requirements
Human Body Model	EIA/JEDEC22-A114-A	Vddrf***	H17	**7.1 >100V,< +300V** **7.2 • -500V**	RF • 1000V OTHER • 2000V
		Sim_pbias**	T11	**7.3 • 300V**	
		Vdd_usim**	T12		
		Vddrf1	G16		
		Vddx	D16		
		Apc_vdo	L9		
		Apc_vdo	U13		
		Vdda	P15		
		Vdda	P16		
		Vddosc	H16		
		Vddr1rx1	T15		
		Vddr1tx1	F16		
		Vddr2	F15		
		All others		**• 500V**	
Charge Device Model	EIA/JEDEC22-C101-A	RX_EGSMM	M16	7.4 **• 100V**	• 500V
		RX_EGSMP	L16		
		RX_PCSP	K16		
		RX_DCSP	L17		
		RX_GSMP	M17		
		RX_GSMM	N17		
		RXDCSM	K17		
		RXPCSM	J16		
		All others		**• 200V**	

8 RECOMMENDED OPERATING CONDITIONS

8.1 Power PADS

Parameter		Min	Typ	Max	Unit
VDD_DBB, VDD_RST	MAX CPU Frequency 104 MHz	1.24	1.3	1.36	V
	Deep sleep	1.0	1.05	1.1	V
VDDR1	DRP-VR1 Supply Voltage	2.7	2.85	2.95	V
VDDR2	DRP-VR2 Supply Voltage	2.7	2.85	2.95	V
VDD_MIF	Emif address data multiplexed bus power supply	1.7	1.8	1.9	V
VDD_USIM	USIM Extended Drain IO power supply	1.65	1.8	1.95	V
		2.7	2.85	2.95	V
VDD_IO_1, VDD_IO_2	IO power supply	1.7	1.8	1.9	V
VDD_PLL	Supply voltage for DPLLs and analog supply voltage for slicer	1.24	1.3	1.36	V
APC_VDO	APC analog supply	2.7	2.85	2.95	V
VDDX	Internal LDO_DCXO regulator output. Used to connect to filter capacitor.	1.37	1.4	1.43	V
VDDOSC	Internal LDO_OSC regulator output. Used to connect to filter capacitor	1.37	1.4	1.43	V
VDDRF	Internal LDO_RF regulator output. Used to connect to filter capacitor	1.37	1.4	1.43	V
VDDA	Internal LDO_ANA regulator output.. Used to connect to filter capacitor	1.37	1.4	1.43	V
VSS	Ground power supply		0		V
VSSA	Analog ground for		0		V
VSS_PLL	Ground for DPLLs		0		V
VSSPBIAS	Ground power supply for bandgap of sim pbias		0		V
VSSX	DCXO ground		0		V
VPP	Programming power connection used to program the eFuse ROM		0		V

Table 6 : Recommended Operating Conditions for Power PADS

IDDQ (max)	Leakage(uAmp)	Leakage(uAmp)	Leakage(uAmp)	Leakage(uAmp)
	T=30degC	T=30degC	T=30degC	T=30degC
	V=1.05	V=1.05	V=1.3V	V=1.3V
	RET ON	RET OFF	RET ON	RET OFF
VDD_DBB	**162**	**243**	**277**	**400**

8.2 Interface PADS

BQ0021S		Min	Typ	Max	Unit
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 4 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 4 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		8		mA
Iz	Leakage current			± 20 (1)	• A
BQ0031S (Differential mode)		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	25			mV
VIL	Low level input voltage			-25	mV
VCM	Input common mode voltage	VDDS/2 - 0.4	VDDS/2	VDDS/2 + 0.4	V
	BQ0031S (GPIO mode)	**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 4 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 4 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		4		mA
Iz	Leakage current			± 20 (1)	• A
BQ0045S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.7VDDS			V
VIL	Low level input voltage			0.3VDDS	V
I_I	Input leakage current			±1	• A
VOH	High level output voltage, IO = 3 mA	0.8VDDS			V
VOL	Low level output voltage, IO = 3 mA			0.2VDDS	V
Iz	Leakage current			± 20 (1)	• A
BQ0054S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 4 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 4 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		8		mA
PU	PU resistance		90		k•
PD	PD resistance		90		k•
Iz	Leakage current			± 20 (1)	• A
BQ0055S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 4 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 4 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		8		mA

PU	PU resistance		18		k•
PD	PD resistance		90		k•
Iz	Leakage current			± 20 (1)	• A
BQ0057S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		4		mA
PU	PU resistance		90		k•
PD	PD resistance		90		k•
Iz	Leakage current			± 20 (1)	• A
BQ0062S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		4		mA
PU	PU resistance		18		k•
PD	PD resistance		90		k•
Iz	Leakage current			± 20 (1)	• A
BQ0066S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
I_I	Input leakage current			±1	• A
PU	PU resistance		90		k•
PD	PD resistance		18		k•
Iz	Leakage current			± 20 (1)	• A
BQ0077S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		4		mA
PU	PU resistance		18		k•
PD	PD resistance		90		k•
Iz	Leakage current			± 20 (1)	• A
BQ0242S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	1.15			V
VIL	Low level input voltage			0.61	V
VOH	High level output voltage, IO = 4 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 1 mA			0.4	V

I_I	Input leakage current			±1	• A
Iout	Output current		4		mA
PU	PU resistance		32		k•
PD	PD resistance		30		k•
Iz	Leakage current			± 30 (1)	• A
BC1825DSHY/PU/PD/ BC1825DS		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		8		mA
PU	PU resistance		18		k•
PD	PD resistance		18		k•
Iz	Leakage current			± 20 (1)	• A
BC1850CSHY/PU/PD		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
I_I	Input leakage current			±1	• A
Iout	Output current		4		mA
PU	PU resistance		18		k•
PD	PD resistance		18		k•
Iz	Leakage current			± 20 (1)	• A
IC18SHY		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
I_I	Input leakage current			±1	• A
Iz	Leakage current			± 20 (1)	• A
IQ0041S		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.33VDDS	V
OC1825DS					
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
Iout	Output current		8		mA
Iz	Leakage current			± 20 (1)	• A
OC1850CS					
VOH	High level output voltage, IO = 2 mA	VDDS - 0.45			V
VOL	Low level output voltage, IO = 2 mA			0.45	V
Iout	Output current		4		mA
Iz	Leakage current			± 20 (1)	• A
OQ0028S		**Min**	**Typ**	**Max**	**Unit**
VOH	High level output voltage, IO = 4 mA	VDDS - 0.45			V

VOL	Low level output voltage, IO = 4 mA			0.45	V
Iout	Output current		8		mA
IC18SHY PD/PU		**Min**	**Typ**	**Max**	**Unit**
VIH	High level input voltage	0.65VDDS			V
VIL	Low level input voltage			0.35VDDS	V
PU	PU resistance		18		k•
PD	PD resistance		18		k•
I_I	Input leakage current			±1	• A
Iz	Leakage current			± 20 (1)	• A

- For APCV0P1 specifications refer section 22.
- For SC_DRP2_V1P0_GS50 specifications refer section 23.

Note:

(1) IZ is the total leakage current through the PAD connection of a driver/receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.

Table 7 : Recommended Operating Conditions for Interface PADS

9 EXTERNAL MEMORY INTERFACE EMIF

9.1 FUNCTIONAL DESCRIPTION

The External Memory Interface (EMIF) manages synchronous/asynchronous 16-bit data bus read/write accesses between external memories, the MPU, and the DMA controller. A total of 4 chip-selects are supported with 32M bytes for each chip-select (except for CS0 with 28M bytes).

The synchronous/asynchronous EMIF supports the most common memory interface protocols through a flexible programming and timing signal control. A number of different muxed/nonmuxed memory types connect with the EMIF. These memory types share pins on the device, but their functionalities and controlling logic may differ.

Pad Name	Direction	Description
DATA_ADD[15:0]	I/O	Address and data inputs/outputs multiplexed
ADD[23:16]	O	Most-significant bits (MSB) of address
nCS[0:3]	O	Activates the device memory: 0: Device memory activate 1: Device memory deactivate (for each chip select)
RnW	O	Writes an enable signal to the memory device: 0: Write 1: Read
NMOE	O	Controls data outputs during the Bus Read operation of the device memory: 0: Output enable 1: Output disable
nBE[0:1]	O	High and low byte enable for byte write & read access.
FDP	O	Usually connected to memory reset, thus reducing the current consumption
ADV	O	Indicates to memory device that a valid address is present on the address inputs (address bits A15 down to A0 are multiplexed, address bits A23 down to A16 are address only).
NFWP	O	Gives an additional hardware protection for write action on memory device: 0: Disable write on memory 1: Enable write

CKM	O	Synchronizes the memory to the frequency of the EMIF during synchronous operations such as burst mode.
NRDY	I	Provides data-valid feedback during read and write in full-handshaking mode.

Table 8 : EMIF Interface Pins Description

9.2 ELECTRICAL CHARACTERISTICS

9.2.1 EMIF Synchronous Mode

The following tables assume testing over the recommended operating conditions

NO.	PARAMETER			MIN	MAX	UNIT
F12	tsu(DV-CLKH)	Setup time, emif_memdata_[15:0] valid before emif_memclk high	RT = 0 (1)	8		ns
			RT = 1 (1)	1		ns
F13	th(CLKH-DIV)	Hold time, emif_memdata_[15:0] valid after emif_memclk high	RT = 0 (1)	-5		ns
			RT = 1 (1)	1		ns
F19	tsu(RDYL-CLKH)	Setup time, emif_memrdy low before emif_memclk high	RT = 0 (1)	8		ns
			RT = 1 (1)	1		ns
F20	th(CLKH-RDYL)	Hold time, emif_memrdy low after emif_memclk high	RT = 0 (1)	-5		ns
			RT = 1 (1)	1		ns

Notes:

(1) Re-timing control: RT = EMIF_CONFIG_CSx[2] (0: Retiming disable; 1: Retiming enable)

Table 9 : EMIF Timing Requirements - Synchronous Mode

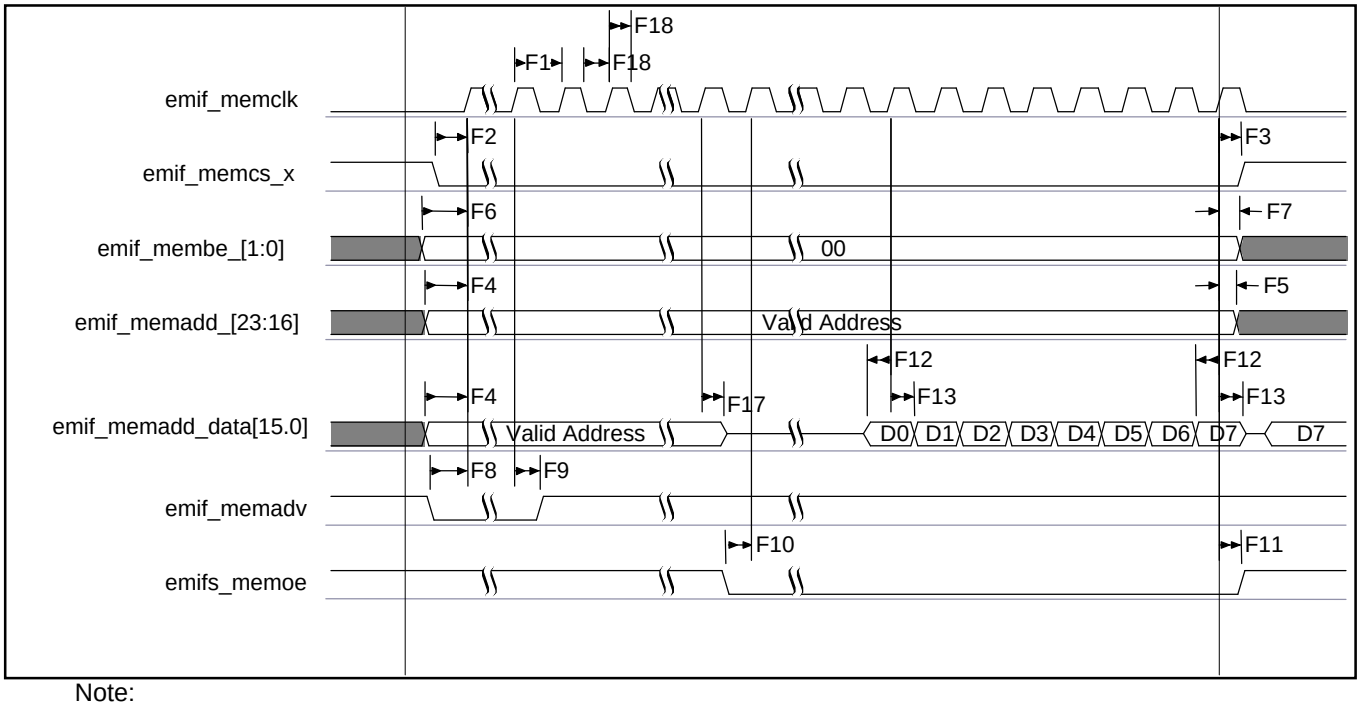
NO.	PARAMETER		MIN	MAX	UNIT
F1	tc(CLK)	Cycle time, emif_fclk	18.1		ns
F2	$T_d(_{CSV\text{-}CLKV})$	Delay time, CSx low to CLK high Delay time, emif_memcs _x (2) valid to emif_memclk first clock edge	A(1) – 4	A(1) + 2.5	ns
F3	td(CLKH-nCST)	Delay time, emif_memclk rising edge to emif_memcs_x (2) transition	A(1) - 2	A(1) + 4	ns
F4	td(ADDV-CLKFE)	Delay time, emif_memadd_[23:16] valid to emif_memclk first clock edge	A(1) -1.5	A(1) + 1	ns
F5	td(CLKH-ADDT)	Delay time, emif_memclk rising edge to emif_memadd_[22:16] transition	-2	1.5	ns
F6	td(nBEV-CLKFE)	Delay time, emif_membe _[1:0] valid	A(1) – 3	A(1) + 1	ns

		to emif_memclk first clock edge			
F7	td(CLKH-nBET)	Delay time, emif_memclk rising edge to emif_membe_[1:0] transition	-3	1	ns
F8	td(nADV-CLKFE)	Delay time, emif_memadv valid to emif_memclk first clock edge	A(1) – 4	A(1) + 1.8	ns
F9	td(CLKH-nADT)	Delay time, emif_memclk rising edge to emif_memadv transition	-1.8	4	ns
F10	td(nOE-CLKFE)	Delay time, emif_memoe valid to emif_memclk first clock edge	A(1) - 2	A(1) + 3	ns
F11	td(CLKH-nOET)	Delay time, emif_memclk rising edge to emif_memoe transition	A(1) - 3	A(1) + 2	ns
F14	td(nWE-CLKFE)	Delay time, emif_memwe valid to emif_memclk first clock edge	A(1) - 2.5	A(1) + 2.5	ns
F15	td(CLKH-nWET)	Delay time, emif_memclk rising edge to emif_memwe transition	-2.5	2.5	ns
F16	td(DV-CLKFE)	Delay time, emif_fdata _[15:0] valid to emif_memclk first clock edge	A(1) – 10	A(1) + 3.5	ns
F17	td(CLKH-DT)	Delay time, emif_memclk rising edge to emif_fdata_[15:0] transition	-2.5	1.5	ns
F18	tw(CLK)	Pulse duration, emif_memclk low or high	0.4 A(1)	0.6 A(1)	ns

Notes:

(1) A = emif_memclk period (Max frequency 52 MHz)
(2) x = 0 to 3

Table 10 : EMIF Switching Characteristics - Synchronous Mode



Note:

x = 0 to 3

Figure 5 : EMIF Timing - Synchronous Burst Read

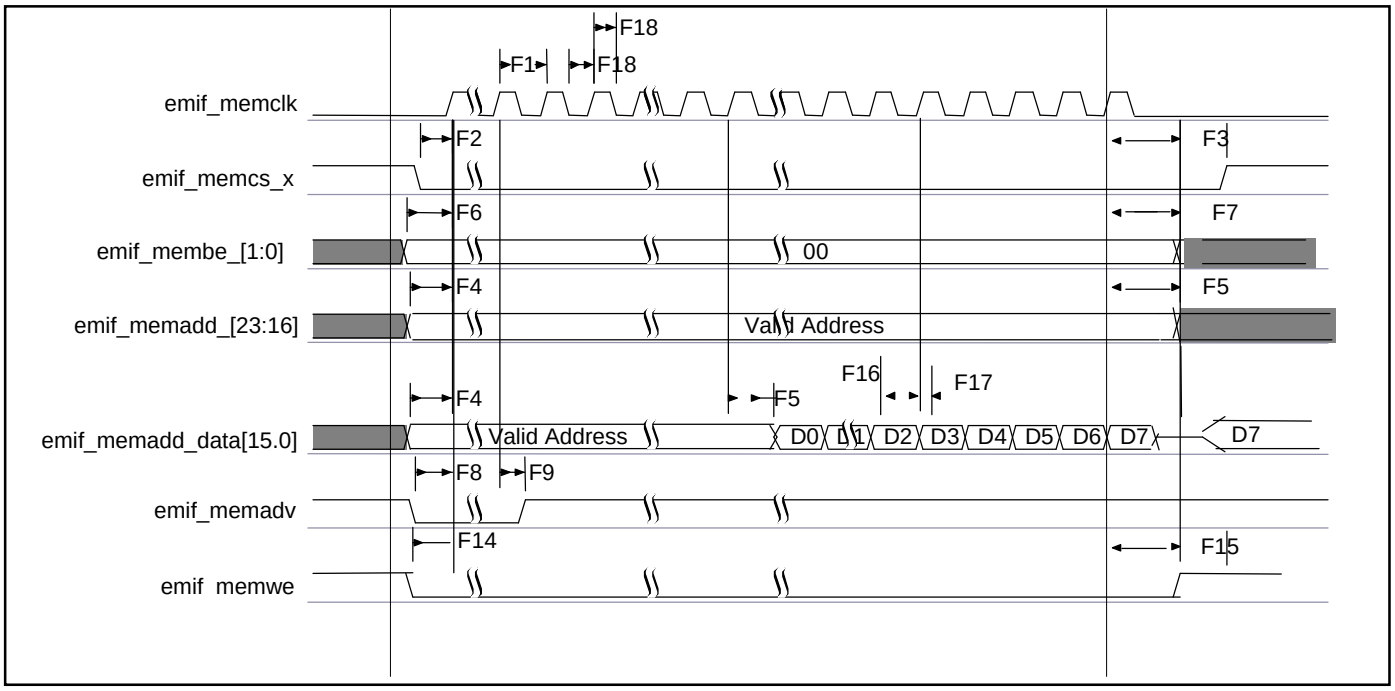


Figure 6 : EMIF Timing - Synchronous Burst Write

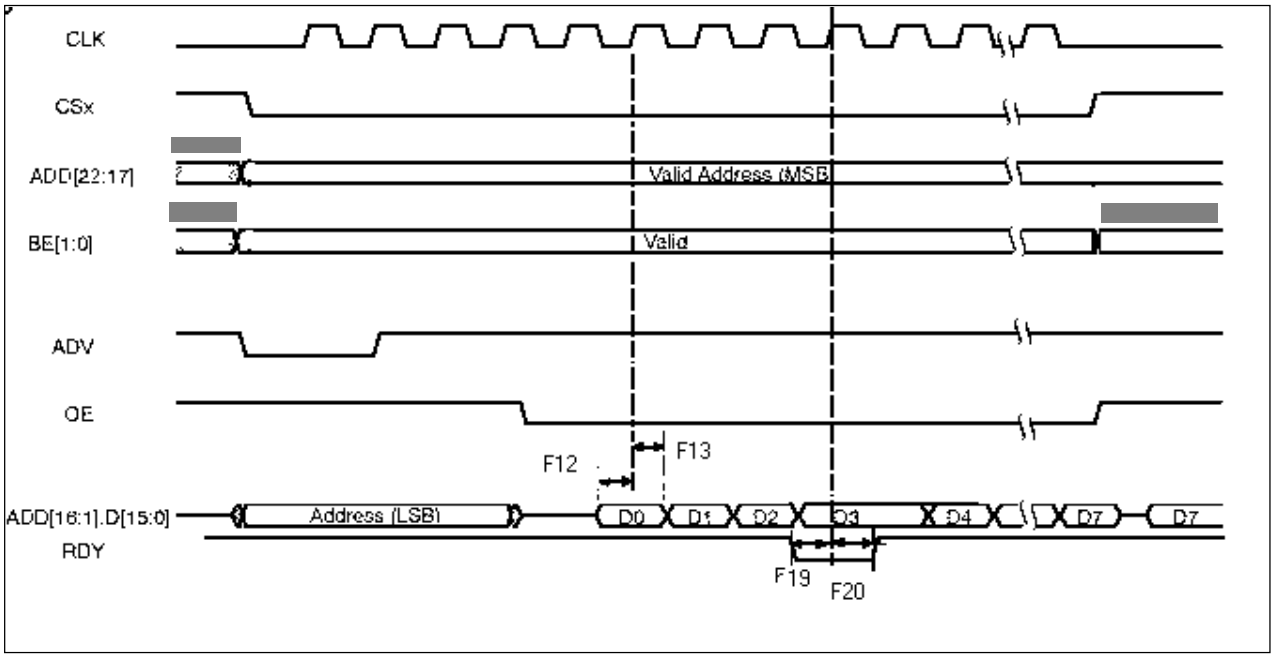


Figure 7 : Synchronous burst read operation with full handshaking mode

Note : All other timing parameters will remain same as of Emif – synchronous burst read operation with Non-full handshaking mode.

9.2.2 EMIF Asynchronous Mode

The following tables assume testing over operating conditions

NO.	PARAMETER		MIN	MAX	UNIT
F29	tsu(DV-nOEH)	Setup time, emif_fdata_[15:0] valid before emif_memoe high	8		ns
F30	th(nOEH-DV)	Hold time, emif_fdata_[15:0] valid after emif_memoe high	-5		ns

Table 11 : EMIF Timing Requirements - Asynchronous Mode

NO.	PARAMETER		MIN	MAX	UNIT
F21	tw(nCSxL)	Pulse duration, emif_memcs_x(9) low	A(1)		ns
F22	td(nCSxL-ADV)	Delay time, emif_memcs_x(9) low to emif_memadd_[22:17] valid	-1	3	ns
F23	td(nCSxL-nBEV)	Delay time, emif_memcs_x(9) low to emif_membe_[1:0] valid	-1	1.5	ns
F24	tw(nBEV)	Pulse duration, emif_membe_[1:0] valid	A(1)		ns
F25	td(nCSxL-nADVL)	Delay time, emif_memcs_x(9) low to emif_memadv low	-3	4	ns
F26	tw(nADVL)	Pulse duration, emif_memadv low	B(2)		ns
F27	td(nCSxL-nOEL)	Delay time, emif_memcs_x low to emif_memoe low	C(3) – 4	C(3) +2	ns
F28	tw(nOEL)	Pulse duration, emif_memoe low	D(4)		ns
F35	tw(nCSxH)	Pulse duration, emif_memcs_x(9) high	G(5)		ns
F36	td(nCSxL-nWEL)	Delay time, emif_memcs_x(9) low to emif_memwe low	H(6) – 3.5	H(6) + 2	ns
F37	tw(nWEL)	Pulse duration, emif_memwe low	I(7)		ns
F38	td(nCSxL-DV)	Delay time, emif_memcs_x(9) high to emif_fdata_[15:0] invalid (Write)	-3.5	1.5	ns
F39	td(nOEL-ADIV)	Delay time, emif_memoe low to emif_memadd_[15:0] invalid	-1	1.5	ns
F40	td(nADVH-DV)	Delay time, emif_memadv high to emif_fdata_15:0] valid (Write)	J(8) - 1	J(8) + 3.5	ns

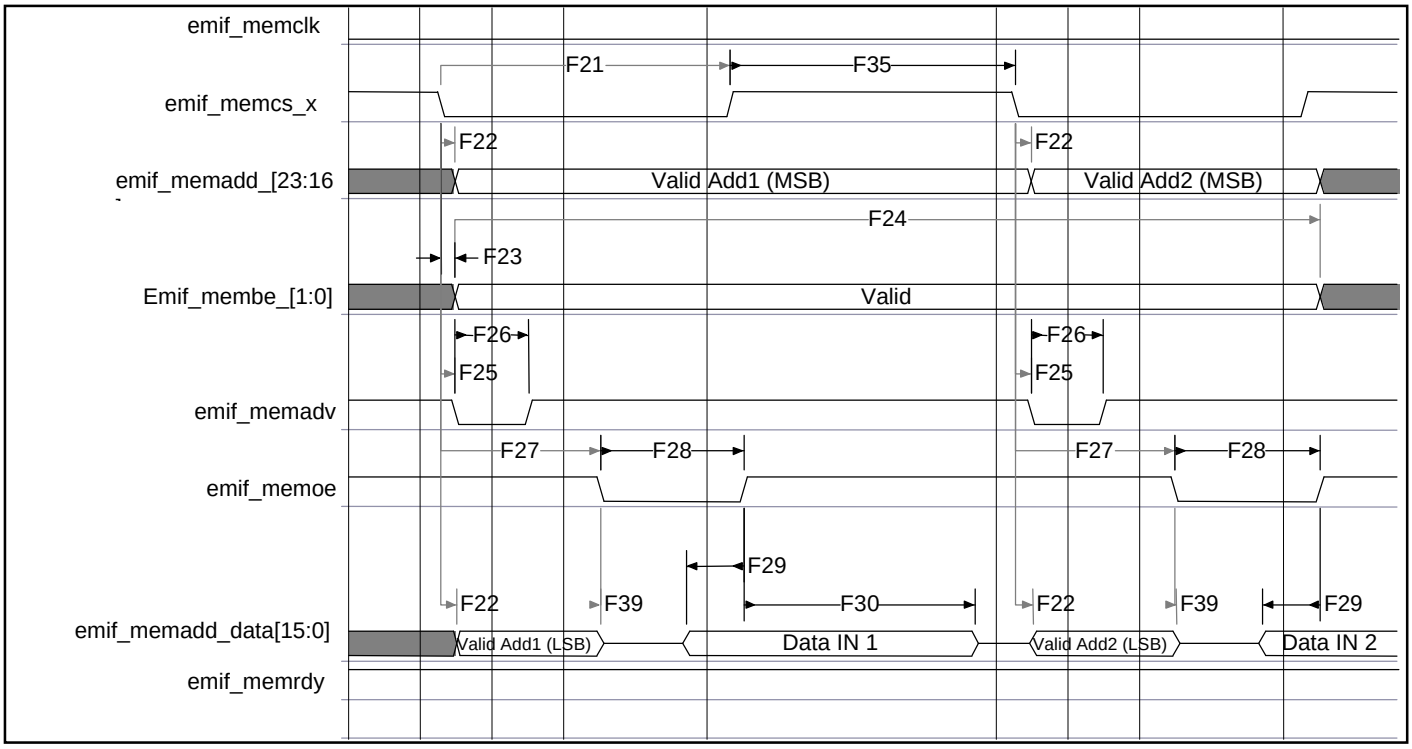
Notes:

(1) A = (RDWST + 2) * emif_memclk period
(2) B = (ADVHOLD + 1) * emif_memclk period
(3) C = OESETUP * emif_memclk period
(4) D = (RDWST + 2 - OESETUP) * emif_memclk period
(5) G = (BTWST + 1) * emif_memclk period
(6) H = (WRWST) * emif_memclk period
(7) I = (WELEN + 1) * emif_memclk period

(8) J = emif_memclk period
(9) x = 0 to 3

The capacitive load is equivalent to 15pF

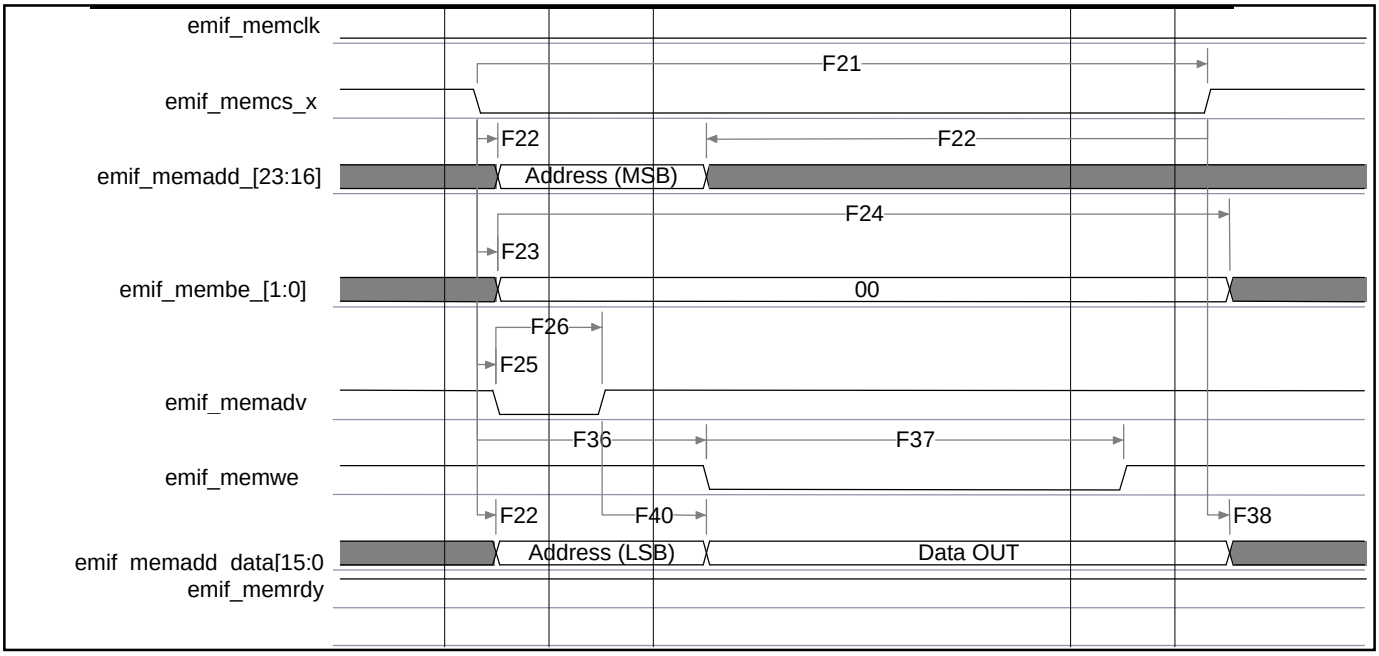
Table 12 : EMIF Switching characteristics- Asynchronous Mode



Note:

x = 0 to 3

Figure 8 : EMIF/Multiplexed - Asynchronous Read – 32-bit Timing



Note:

x = 0 to 3

Figure 9 : EMIF/Multiplexed - Asynchronous Write - Single Word Timing

10 MCSI

10.1 FUNCTIONAL DESCRIPTION

The multi-channel serial interface (MCSI) has multi-channel transmission capability. MCSI expand the parallel interface of a MPU or DSP to connect to external devices such as audio codecs and GSM system simulators.

The MCSI on the LOCOSTO processor provide full duplex transmission and master or slave clock control. All transmission parameters are configurable to cover the maximum number of operating conditions.

Signal Name	Direction	Description
mcsi_bclk	IO	Serial Clock I/O
mcsi_sdi	I	Serial Data Input
mcsi_sdo	O	Serial Data Output
mcsi_sync	IO	Frame Synchronization I/O

Table 13 : MCSI Pins Description

10.2 ELECTRICAL CHARACTERISTICS

10.2.1 MCSI Interface Timings in Slave Mode

The following tables assume testing over the recommended operating conditions.

NO.	PARAMETER		MIN	MAX	UNIT
M1	tsu(dataV-bclkA)	Setup time, mcsi_din valid before mcsix_bclk active edge	5		ns
M2	th(dataV-bclkA)	Hold time, mcsi_din valid after mcsix_bclk active edge	1		ns
M3(1)	tsu(syncV-bclkA)	Setup time, mcsi_sync valid before mcsix_bclk active edge	5		ns
M4(1)	th(syncV-bclkA)	Hold time, mcsi_sync valid after mcsix_bclk active edge	1		ns
M12	tc(bclk)	Cycle time(2), mcsi_bclk period	154		ns
M13	tW(bclk)	Pulse duration, mcsi_bclk high or low	0.45 P(3)	0.55 P(3)	ns

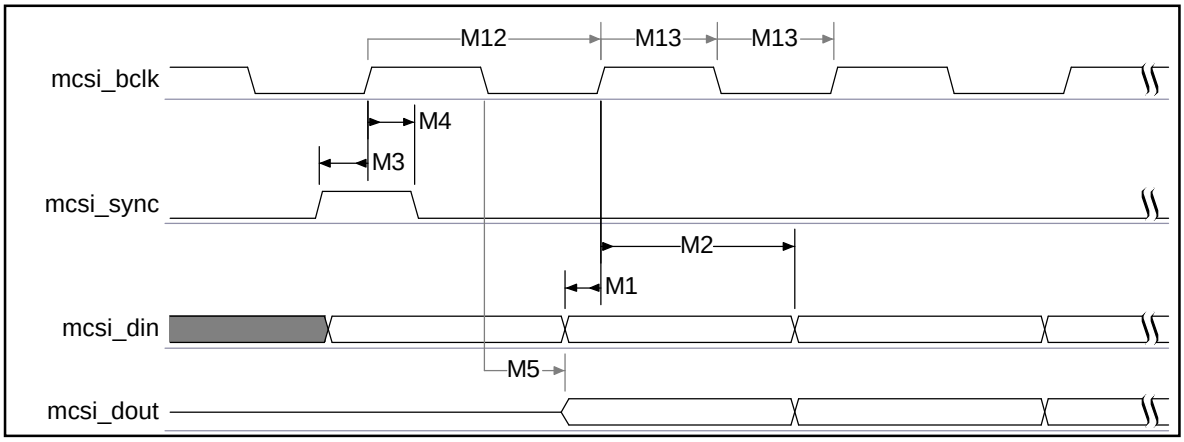
Notes:

(1) These timings are available for all configuration of the frame synchronization signal (long/short, polarity).
(2) 154=2/B with B is the System Clock frequency for LOCOSTO (13 MHz).
(3) P = mcsi_bclk period. The clock polarity can be configured by software.

Table 14 : MCSI Timing Requirements – Slave Mode

NO.	PARAMETER		MIN	MAX	UNIT
M5	td(bclk-dataT)	Delay time, mcsi_bclk active edge to mcsix_dout shifted	1.5	10	ns

Table 15 : MCSI Switching Characteristics – Slave Mode



Note:

The polarity of mcsi_sync and mcsi_bclk are software configurable with MAIN_PARAMETER_REG register. For more information, refer to the MCSI chapter of LOCOSTO TRM.

Figure 10 : MCSI Interface Timing – Slave Mode

10.2.2 MCSI Interface Timings in Master Mode

The following tables assume testing over the recommended operating conditions

NO.	PARAMETER		MIN	MAX	UNIT
M6	tsu(dataV-bclkA)	Setup time, mcsi_din valid before mcsi_bclk active edge	6		ns
M7	th(dataV-bclkA)	Hold time, mcsi_din valid after mcsi_bclk active edge	0		ns

Table 16 : MCSI Timing Requirements – Master Mode

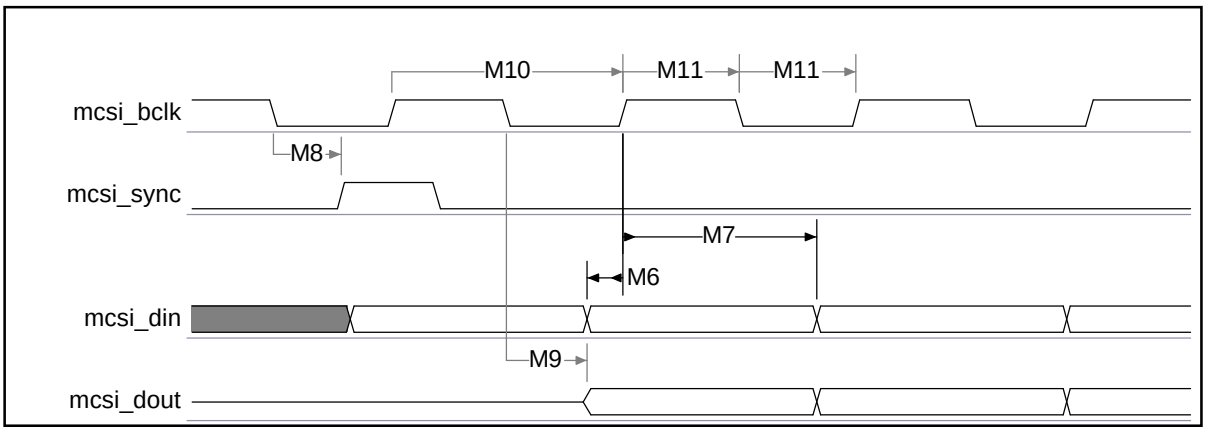
NO.	PARAMETER		MIN	MAX	UNIT
M8(1)	td(bclk-syncT)	Delay time, mcsi_bclk active edge to mcsi_sync shifted		2	ns
M9	td(bclk-dataT)	Delay time, mcsi_bclk active edge to mcsi_dout shifted	-2	2	ns
M10	tc(bclk)	Cycle time(2), mcsi_bclk period	154		ns
M11	tW(bclk)	Pulse duration, mcsi_bclk high or low	0.45 P(3)	0.55 P(3)	ns

Notes:

(1) These timings are available for all configuration of the frame synchronization signal (long/short, polarity).
(2) 154=2/B with B is the System Clock frequency for LOCOSTO (13 MHz).
(3) P = mcsi_bclk period. The clock polarity can be configured by software.

The input timing requirements are given by considering a rising and a falling time of 1ns
The switching characteristics are realized with a capacitive load equivalent to 15pF for output signals.

Table 17 : MCSI Switching Characteristics – Master Mode



Note:

The polarity of mcsi_sync and mcsi_bclk are software configurable with MAIN_PARAMETER_REG register.
The synchronization pulse duration is configurable with the MAIN_PARAMETER_REG register in SHORT (equal to the bit duration) or LONG (equal to the channel duration) frame. For more information, refer to the MCSI chapter of LOCOSTO TRM.

Figure 11 : MCSI Interface Timing – Master Mode

11 INTER INTEGRATED CIRCUIT (I^2C)

11.1 FUNCTIONAL DESCRIPTION

The multimaster I^2C peripheral provides an interface between a local host (LH) such as an MPU or DSP processor and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit/receive up to 8-bit data to/from the LH device through the two-wire I^2C interface.

This I^2C peripheral supports any slave or master I^2C-compatible device. Locosto devices contain 2 separate I^2C modules.
The I^2C bus is a multi-master bus. The I^2C controller supports the multi-master mode that allows more than one device capable of controlling the bus to be connected to it. Each I^2C device, including the TI processor, is recognized by a unique address and can operate as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I^2C bus can also be considered as master or slave when performing data transfers. Note that a master device is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. During the transfer, any device addressed by this master is considered a slave.

MCU & DSP I^2C: 2 single-mode pins, Fails-safe Input, Open Drain output		
SCL_TriTon	IN/OUT	I2C interface Master serial clock reserved for TriTon Lite Control
SDA_TriTon	IN/OUT	I2C interface Serial bi-directional data reserved for TriTon Lite Control

Note: This I2C interface is reserved for TriTon Lite ABB control.

MCU App I^2C: 2 single-mode pins, Fails-safe Input, Open Drain output		
SCL	IN/OUT	I2C interface Master serial clock
SDA	IN/OUT	I2C interface Serial bi-directional data

Table 18 : I2C Pins Description

11.2 ELECTRICAL CHARACTERISTICS

11.2.1 I2C Interface Timings

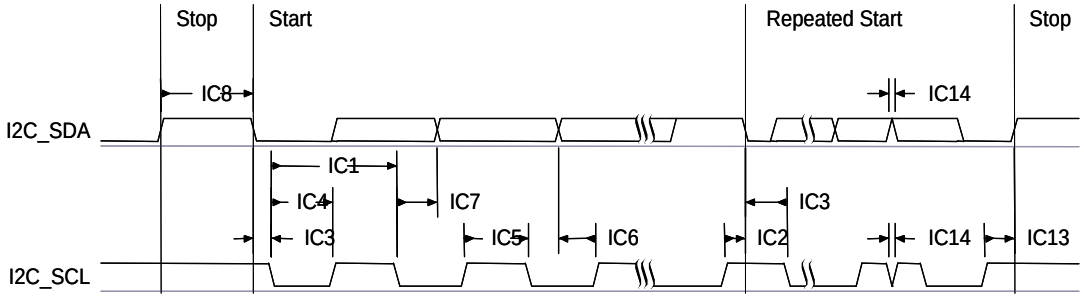
The table assumes testing over recommended operating conditions

NO.	PARAMETER		Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
IC1	1 / [tc(SCL)]	Operating frequency, I2C_SCL		0.1 (1)		0.4	MHz
IC2	tsu(SCLH–SDAL)	Setup time, I2C_SCL high before I2C_SDA low (for a repeated START condition)	4.7		0.6		µs
IC3	th(SCLL–SDAL)	Hold time, I2C_SCL low after I2C_SDA low (for a repeated START condition)	4		0.6		µs
IC4	tw(SCLL)	Pulse duration, I2C_SCL low	4.7		1.3		µs
IC5	tw(SCLH)	Pulse duration, I2C_SCL high	4		0.6		µs
IC6	tsu(SDA–SDLH)	Setup time, I2C_SDA valid before	250	(2)	100		ns

		I2C_SCL high					
IC7	th(SDA–SDLL)	Hold time, I2C_SDA valid after I2C_SCL low (for I2C bus devices)	0		0	0.9	µs
IC8	tw(SDAH)	Pulse duration, I2C_SDA high between STOP and START conditions	4.7		1.3		µs
IC9	tr(SDA)	Rise time, I2C_SDA(3)		1000		300	ns
IC10	tr(SCL)	Rise time, I2C_SCL(3)		1000		300	ns
IC11	tf(SDA)	Fall time, I2C_SDA(3)		300		300	ns
IC12	tf(SCL)	Fall time, I2C_SCL(3)		300		300	ns
IC13	tsu(SCLH–SDAH)	Setup time, I2C_SCL high before I2C_SDA high (for STOP condition)	4		0.6		µs
IC14	tw(SP)	Pulse duration, spike (must be suppressed)			0	50	ns
IC15	Cb	Capacitive load for each bus line		400		400	pF

(1) In the master-only I2C operating mode of Locosto, minimum cycle time for I2C_SCL is 12 µs.
(2) The maximum th(SCLL-SDAL) has only to be met if the device does not stretch the low period (tw(SCLL)) of the I2C_SCL signal.
(3) Max of falling and rising time were measured while considering an internal pull-up value of 520 Ohms

Table 19 : I2C Signals (I2C_SDA and I2C_SCL) Switching Characteristics



Notes :

A device must internally provide a hold time of at least 300 ns for the I2C_SDA signal (referred to the VIHmin of the I2C_SCL signal) to bridge the undefined region of the falling edge of I2C_SCL.

A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement tsu(SDA- SDLH) ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line tr max + tsu(SDA- SDLH) =1000 + 250 = 1250 ns (according to the standard-mode I2C-bus specification) before the I2C_SCL line is released.

Figure 12 : I^2C Timings

12 SERIAL PORT INTERFACE (SPI)

12.1 FUNCTIONAL DESCRIPTION

The Master Slave SPI (MSSPI) is compliant with the SPI standard.

It is a bidirectional, four-line interface consisting of:

- The clock used to shift-in and shift-out data.
- The device enable.
- The data input.
- The data output.

There is one MSSPI module in LOCOSTO processor. It is based on a looped shift register, thus allowing both transmit and receive modes. It can operate in master or in slave mode using MPU / DSP or DMA protocol.

In Master mode, the SPI provides up to 3 chip-selects: spi_ncs0, spi_ncs1 and spi_ncs2. In Slave mode, spi_ncs0 is used as the SPI module chip select.

Signal Name	Direction	Description
spi_clk	O	MSSPI serial clock
spi_data_mosi	O	MSSPI serial data master-out
spi_data_miso	I	MSSPI serial data master-in
spi_ncsi	O	MSSPI chip select i output, i=[0:2]

Table 20 : MSSPI Pins Description in Master Mode

Signal Name	Direction	Description
spi_clk	I	MSSPI serial clock
spi_data_mosi	I	MSSPI serial data slave-in
spi_data_miso	O	MSSPI serial data slave-out
spi_ncs0	I	MSSPI enable

Table 21 : MSSPI Pins Description in Slave Mode

12.2 ELECTRICAL CHARACTERISTICS

12.2.1 Serial Port Interface (SPI) Timings

The following tables assume testing over recommended operating conditions

No	Parameter			Min	Max	Unit
SPI1	1/tc(SCLK)	Operating Frequency, SPI_CLK(3)	Slave mode		B(1)	MHz
SPI2	tw(SCLKH)	Pulse Duration, SPI_CLK high or low	Slave mode	0.45*P(2)	0.55*P(2)	ns
SPI5	tsu(DV-CLKH)	Setup time, SPI_DATA_MISO valid before SPI_CLK active edge(3)	Master mode	5		ns
		Setup time, SPI_DATA_MOSI valid before SPI_CLK active edge(3)	Slave mode	1.5		ns

SPI6	th(CLKH-DV)	Hold time, SPI_DATA_MISO valid after SPI_CLK active edge(3)	Master mode	7		ns
		Hold time, SPI_DATA_MOSI valid after SPI_CLK active edge(3)	Slave mode	2.5		ns

(1) B = Clock frequency can be 13, 24 or 26 MHz to support 13,24 or 26Mbps
(2) P = Period of SPI_CLK in nanoseconds (ns).
(3) Polarity of SPI_CLK and the active clock edge (rising or falling) on which DOUT is driven and DIN data is latched is all software configurable. These timings apply to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.

Table 22 : SPI Interface Timing Requirements

No	Parameter			Min	Max	Unit
SPI1	1/tc(SCLK)	Operating Frequency, SPI_CLK(3)	Master mode		B(1)	MHz
SPI2	tw(SCLKH)	Pulse Duration, SPI_CLK high or low	Master mode	0.45*P(2)	0.55*P(2)	ns
SPI3	td(CS-SCLK)	Delay time, SPI_NCSx active to SPI_CLK active	Master mode	P(2)-2.5	P(2)+5	ns
SPI4	td(SCLK-DOUT)	Delay time, SPI_CLK active edge to SPI_DATA_MOSI transition(3)	Master mode	-6	3.5	ns
		Delay time, SPI_CLK active edge to SPI_DATA_MISO transition(3)	Slave mode	1.5	8.5	ns

(1) B = Clock frequency can be 13, 24 or 26 MHz to support 13,24 or 26Mbps
(2) P = Period of SPI_CLK in nanoseconds (ns).
(3) Polarity of SPI_CLK and the active clock edge (rising or falling) on which DOUT is driven and DIN data is latched is all software configurable. These timings apply to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.

Table 23 : SPI Interface Switching Characteristics

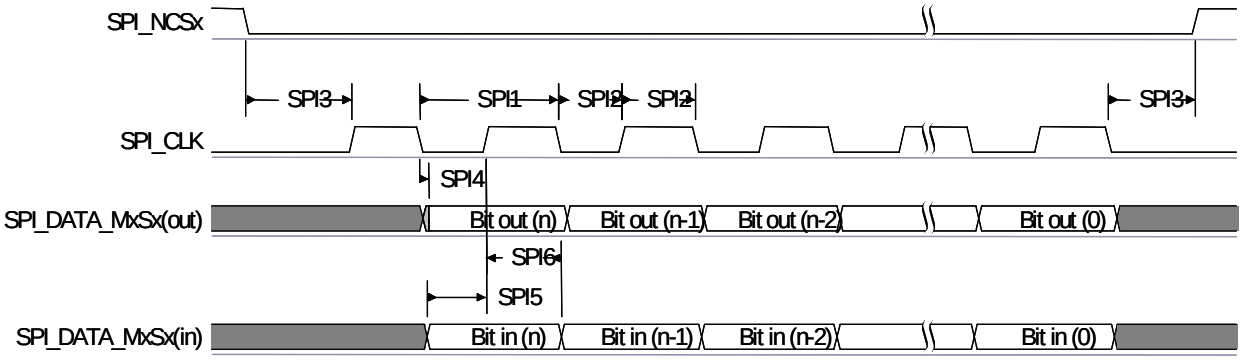


Figure 13 : SPI Interface - Transmit and Receive in Master or Slave timings

13 USB

13.1 FUNCTIONAL DESCRIPTION

LOCOSTO provides a full-speed USB device compatible with USB Specification Revisions 1.1. The USB_W2FC module provides an interface between a local host (LH) , that is ARM and the USB wire. LOCOSTO does not include an integrated USB transceiver.

Interface operating modes: 3- or 4-pin bidirectional		
Signal Name	**Direction**	**Description**
usb_se0	I/O	SE0 function in 3-pin bidirectional DAT_SE0 mode
	I/O	VM function in 4-pin bidirectional VP_VM mode
usb_dat	I/O	DAT function in 3-pin bidirectional DAT_SE0 mode
	I/O	VP function in 4-pin bidirectional VP_VM mode
usb_txen	O	USB Transmit enable
usb_rcv	I	USB Differential receiver signal input (not used in 3-pin DAT_SE0 mode)

Table 24 : USB Pins Description

13.2 ELECTRICAL CHARACTERISTICS

13.2.1 USB Interface Timings

NO.	PARAMETER		MIN	MAX	UNIT
3-pins bi-directional (DAT/SE0)					
FSU6	td(DATL,SE0L)	Time duration, usb_dat and usb_seo low together during transition		14.0	ns
FSU7	td(DATH,SE0H)	Time duration, usb_dat and usb_seo high together during transition		8.0	ns
4-pins bi-directional (VP/VM)					
FSU13	td(VPL,VML)	Time duration, usb_vp and usb_vm low together during transition		14.0	ns
FSU14	td(VPH,VMH)	Time duration, usb_vp and usb_vm high together during transition		8.0	ns

Table 25 : USB Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
3-pins bi-directional (DAT/SE0)					
FSU1	td(TXENA-DATV)	Delay time usb_txen active to usb_dat valid	19.8	22.8	ns
FSU2	td(TXENA-SE0V)	Delay time usb_txen active to usb_seo valid	19.8	22.8	ns
FSU3	ts(DAT-SE0)	Skew between usb_dat and usbx_seo		2	ns
FSU4	td(TXENH-DATV)	Delay time, USB IF ready to read usb_dat after usb_txen high	20.8	21.8	ns
FSU5	td(TXENH-SE0V)	Delay time, USB IF ready to read usb_seo after usb_txen high	20.8	21.8	ns
4-pins bi-directional (VP/VM)					
FSU8	td(TXENA-DATV)	Delay time usb_txen active to usb_dat valid	19.8	22.8	ns
FSU9	td(TXENA-SE0V)	Delay time usb_txen active to usb_seo valid	19.8	22.8	ns
FSU10	ts(DAT-SE0)	Skew between usb_dat and usb_seo		2	ns
FSU11	td(TXENH-DATV)	Delay time, USB IF ready to read usb_dat after usb_txen high	20.8	21.8	ns
FSU12	td(TXENH-SE0V)	Delay time, USB IF ready to read usb_seo after usb_txen high	20.8	21.8	ns

Notes:

USB_SYNCHRO bit must be set "1" to guarantee USB signal balancing
The capacitive load is equivalent to 15pF
The input timing requirements are given by considering a rising and a falling time of 1 ns

Table 26 : USB Switching Characteristics

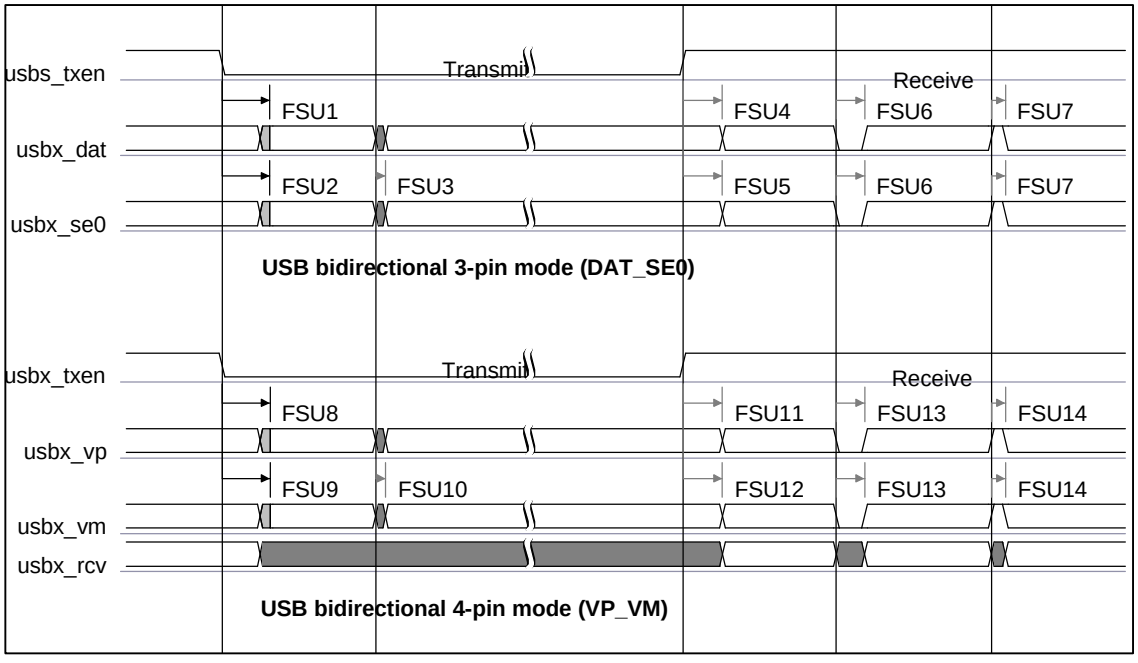


Figure 14 : USB Interface Timings

14 UARTs AND IrDA CONTROLLER

14.1 FUNCTIONAL DESCRIPTION

The LOCOSTO device contains a UART module shared between the microprocessor unit (MPU) and the digital signal processor (DSP) using a TIPB/ OCP static switch. Two modes are selectable through a set of configuration registers, UART or IrDA. This module connects an external modem device through a standard wired interface or an IrDA module. The two functions can be supported dynamically with additional general-purpose inputs/outputs (GPIOs) and software control.

Signal	Direction	Description
UART MODEM Signals		
uart_rx	I	Serial data input
uart_tx	O	Serial data output.
uart_cts	I	Clear to send
uart_rts	O	Request to send
UART MODEM/IrDA Signals		
RX	I	Receive Data.
TX	O	Transmit Data.
CTS	I	Clear To Send.
RTS_SDIRDA	O	In the UART mode: Request-to-send (RTS) when active (low), In IrDA Mode: SD mode is used to configure the transceivers. Infrared shutdown is used to shut down an external IR transceiver via software. Can also be used to configure the IR transceiver for SIR/MIR/FIR modes in conjunction with the TX input pin of the transceiver device.
DSR_RXIR	O	In UART mode: Data set ready is an active-low modem status signal.. In IrDA mode: Serial data input
DCD_TXIR	I/O	In UART mode: Data carrier detect is an active-low modem status signal. In IrDA mode: Serial data output

Table 27 : UART Pins Description

Note : Uart signals are multiplexed with other signals and are not the primary function of the pin.
See LOCOSTO TRM for details

14.2 UART/IRDA BAUD RATE

Baud Rate	Oversampling	Divisor	Error (%)
300	16	10000	0
600	16	5000	0
1200	16	2500	0
2400	16	1250	0
4800	16	625	0
9600	16	312	0.16
14400	16	208	0.16
19200	16	156	0.16
28800	16	104	0.16
38400	16	78	0.16
57600	16	52	0.16
115200	16	26	0.16
230400	16	13	0.16
460800	13	8	0.16
921600	13	4	0.16
1843200	13	2	0.16
3000000	16	1	0
3686400	13	1	0.16

Table 28 : UART Baud Rates, Divisor Values, and Error Rates

Baud Rate	Oversampling	Divisor	Error (%)
2400	16	1250	0
9600	16	312	0.16
19200	16	156	0.16
38400	16	78	0.16
57600	16	52	0.16
115200	16	26	0.16
576000	41/42	2	0
1152000	41/42	1	0
4000000	6	-	0

Table 29 :IRDA Baud Rates, Divisor Values, and Error Rates

15 SIM Card

15.1 FUNCTIONAL DESCRIPTION

The Locosto includes a hardware interface module dedicated to Universal Subscriber Identity Module (USIM).

All baud-rates defined in ISO 7816-3 standard are supported for high-speed transmission.

USIM module external pads are controlled by Locosto configuration to provide:

- USIM controller muxed pin configuration.
- USIM controller IOs power-down mode.
- USIM PBIAS cell configuration.

Embedded PBIAS cell provides the bias voltage to the USIM controller extended drain IOs.

Signal Name	Direction	Description
SIM_RST	OUT	Card Reset
SIM_IO	IN/OUT	Card I/O Data
SIM_CLK	OUT	Card Reference Clock
SIM_PW_CTL	OUT	Pull-Up power control

Table 30 : USIM Pins Description

Signal Name	Direction	Description
sim_pbias	IO	Backup solution: PBIAS reference voltage provider
VDD-USIM	I	USIM Extended Drain IO power supply

Table 31 : USIM PBIAS Pins Description

15.2 ELECTRICAL CHARACTERISTICS

15.2.1 USIM Interface Timings

NO.	PARAMETER		MIN	MAX	UNIT
U1	tC(clk)	Cycle time, sim_clk period	76.9		ns
U2	tW(clkH)	Pulse duration, sim_clk high	0.45 P(1)	0.55 P	ns
U3	tW(clkL)	Pulse duration, sim_clk low	0.45 P	0.55 P	ns
	tr(SIM_RST)	Rise time, SIM_RST		5(2)	ns
	tf(SIM_RST)	Fall time, SIM_RST		5(2)	ns
	tr(SIM_CLK)	Rise time, SIM_CLK		5(2)	ns
	tf(SIM_CLK)	Fall time, SIM_CLK		5(2)	ns
	tr(SIM_IO)	Rise time, SIM_IO		5(2)	ns
	tf(SIM_IO)	Fall time, SIM_IO		5(2)	ns
	tr(SIM_PWRCTRL)	Rise time, SIM_PWRCTRL		5(2)	ns

	tf(SIM_PWRCTRL)	Fall time, SIM_PWRCTRL		5(2)	Ns

(1) P = USIM interface frequency
(2) 10pF load

Table 32 : USIM timing parameters

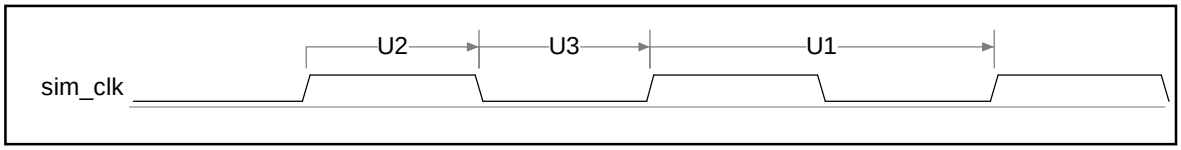


Figure 15 : USIM Interface Timing – Clock Specification

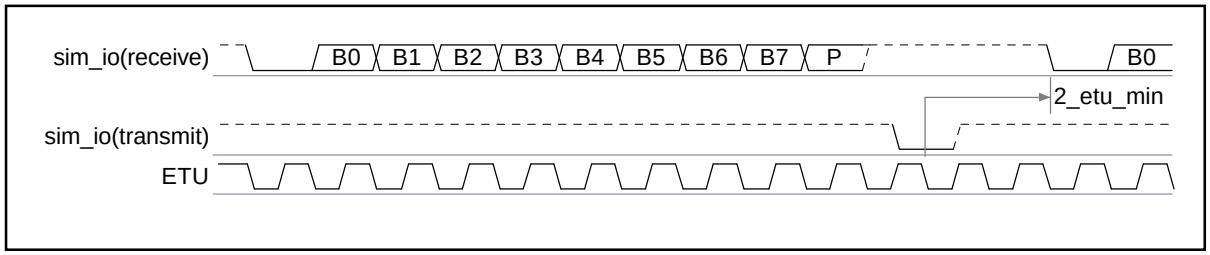


Figure 16 : USIM Interface Timing – Transmit Phase

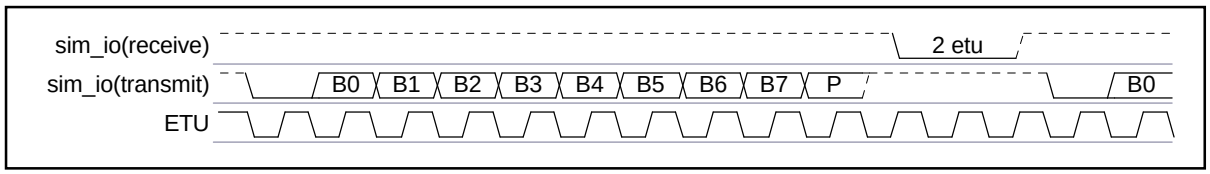


Figure 17 : USIM Interface Timing – Receive Phase

Notes:

The internal clock called ETU (elementary time unit) is equal to the usim interface reference clock divided by the factor N and a factor F/D schedule the data emission (for more information see TRM LOCOSTO)
etu = Period of the ETU clock (for more information see TRM LOCOSTO)

16 LCD INTERFACE

16.1 FUNCTIONAL DESCRIPTION

The chip integrates an 8-bit parallel interface module dedicated to the connection of an external LCD-controller chip. This interface is compliant with the 8-bit 6800-Series and 8086-Series Parallel interface standard in order to support a large range of LCD displays available on the market.

The transfer of the LCD data from the LCD interface to the external LCD controller is performed at a fractional rate (1,2,4,8) of the 13Mhz reference clock

Signal Name	Direction	Description
lcd_data[7:0]	I/O	Data bus from/to external LCD controller
lcd_ncs0	O	LCD interface chip select for chip 0 (active low)
lcd_ncs1	O	LCD interface chip select for chip 1 (if lcd_ncs0 is already set to 0, lcd_ncs1 can not be set to 0) (active low)
Lcd_nreset	O	LCD interface reset (active low)
Lcd_rnw	O	6800-mode: Read/Not write control When high: read, when low: write
		8086-mode: Write enable clock
lcd_estrb	O	6800-mode: Strobe enable
		8086-mode: Read enable clock.
Lcd_rs	O	Selection of instruction / display data type. Active level depend on the controller in used(1).

(1) The most of controller used the following convention : lcd_rs = 0 => instructions, lcd_rs =1 => graphical data

Table 33 : LCD Pins Description

16.2 ELECTRICAL CHARACTERISTICS

16.2.1 LCD 8086 mode timings

NO.	PARAMETER		MIN	MAX	UNIT
C1	Tw(LCD)	Pulse Duration	A/2 -1	A/2 + 1	Ns
C2	Tcyc	Cycle time	A	A	Ns
C3	Tacc	Access Time	A -1	B	Ns
C4	Tod	Output delay	B	B	Ns
C5	Tdacc	Data access time		4	Ns
C6	Tdod	Data output disable time	-4		Ns
C7	Tds	Setup time of read data	3.5		Ns
C8	Tdh	Hold time of read data	2		Ns

A = n/13Mhz , where n can be 1,2,4 or 8 depending on RX_CLOCK_DIV/TX_CLOCK_DIV field programming of CNTL register. Refer to Locosto TRM for details.

B= depends on programming of LCD_NCS0/LCD_NCS1/RS bit field of LCD_CNTL_REG . Refer to Locosto TRM for details.

Table 34 : LCD 8086 mode timing parameter

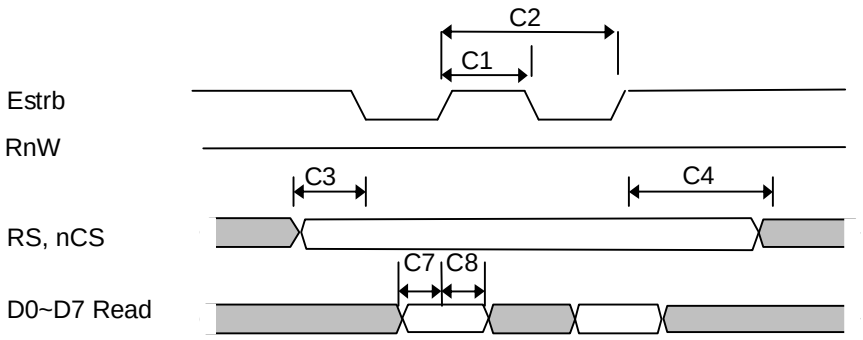


Figure 18 : LCD 8086 mode read timings

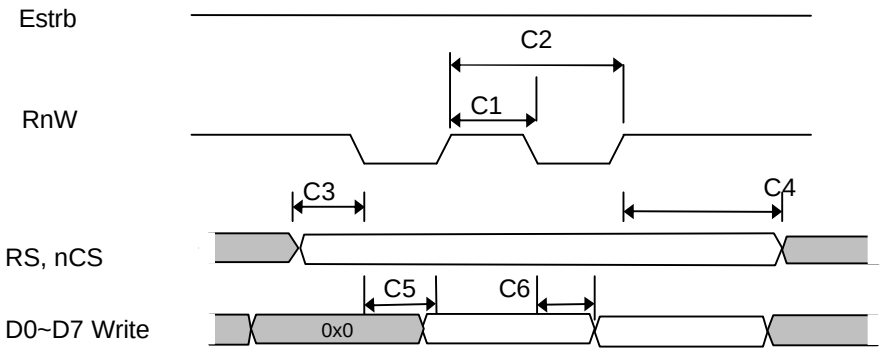


Figure 19 : LCD 8086 mode write timings

16.2.2 LCD 6800 mode timings

NO.	PARAMETER		MIN	MAX	UNIT
C1	Tw(LCD)	Pulse Duration	A/2 -1	A/2 + 1	Ns
C2	Tcyc	Cycle time	A	A	Ns
C3	Tacc1	Access time of Rnw	A - 1.5	A + 3	Ns
C4	Tacc2	Access time of RS,nCS	A - 1.5	B	Ns
C5	Tod1	Output delay of RnW	$\frac{tcyc}{2}$ - 1.5	$\frac{tcyc}{2}$ + 1.5	Ns
C6	Tod2	Output delay of RS, nCS	B	B	Ns
C7	Tdacc	Data access time		4	Ns
C8	Tdod	Data output disable time	-4		Ns
C9	Tds	Setup time of read data	3.5		Ns
C10	Tdh	Hold time of read data	2		Ns
C11	Tod3	Output delay of RnW for read operation	A – 1.5		Ns

A = n/13Mhz , where n can b 1,2,4 or 8 depending on RX_CLOCK_DIV/TX_CLOCK_DIV field programming of CNTL register. Refer to Locosto TRM for details.
B = depends on programming of LCD_NCS0/LCD_NCS1/RS bit field of LCD_CNTL_REG. Refer to Locost TRM for details.

Table 35 : LCD 6800 mode timing parameter

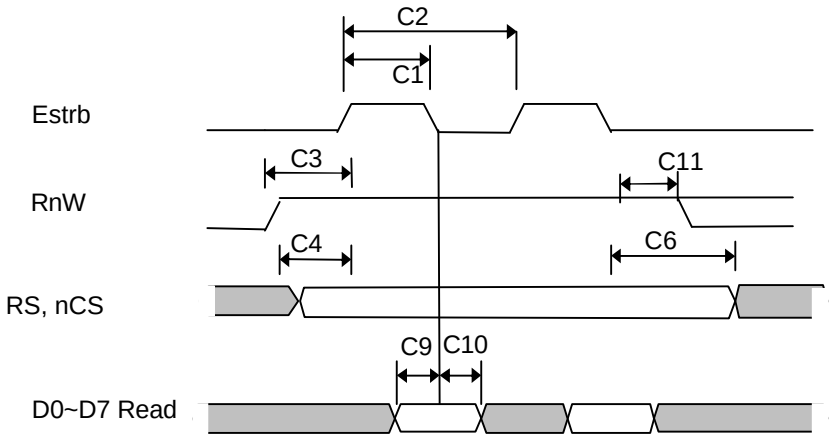


Figure 20 : LCD 6800 mode read timings

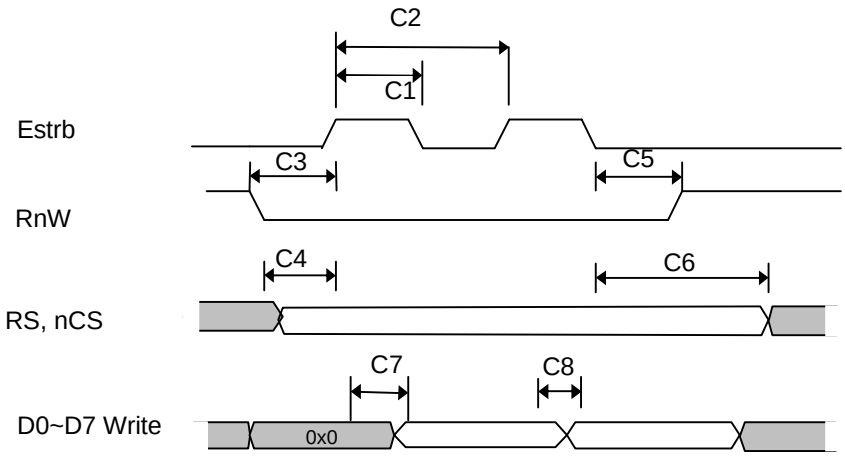


Figure 21 : LCD 6800 mode write timings

17 CAMERA INTERFACE

17.1 FUNCTIONAL DESCRIPTION

The camera module provides the system interface and functionality to connect image sensor modules to the Locosto GPRS multimedia processor.
The main part of camera module is the camera core which is used to ensure image sensor data format detection and transmission to the system.

The camera core module supports two image sensor interfaces. Both are mutually exclusive.

- Serial interface: compact camera port (CCP) interface. Maximum clock of 208 MHz provided externally. Support YUV, Bayer RGB444 or RGB565 input data format. Clock and data are transferred on a differential Sub-LVDS link for low EMI.
- Parallel interface: 8. Maximum clock of 48 MHz. Supports two operating modes:
  - BT656: ITU-R BT656 compatible parallel interface
  - NOBT: general parallel interface with vertical and horizontal synchronization signals.

Signal Name	Direction	Description
cam_hs	I	Line trigger input signal.
cam_vs	I	Frame trigger input signal.
cam_xclk	O	External clock for the image sensor module.
cam_lclk	I	Latch clock for the parallel input data.
cam_d_[7:0]	I	Input data bits 0 to 7 .

Table 36 : Camera Generic Configuration Pins Description

Signal Name	Direction	Description
cam_xclk	O	External clock for the image sensor module.
cam_d_[7:0]	I	Input data bits 0 to 7
cam_lclk	I	Latch clock for the parallel input data.

Table 37 : Camera Pins Description in ITU-R BT.656 Configuration

Signal Name	Direction	Description
cam_s_data	I	Serial data input.
cam_s_clk	I	Serial clock input.

Note:

From the Locosto device point of view, the CCP interface is composed of 4 differential inputs representing 2 effective signals: the serial data and the clock.
From the camera core point of view, the CCP interface is composed of 2 serial inputs (cam_s_data and cam_s_clk) that are the result of low voltage differential signal (sub-LVDS) converters.

Table 38 : Camera Pins Description in CCP Serial Configuration

Signal Name	Direction	Description	Pin Configuration
Gpio_19	I	cam_s_clk	Ball F8 (mode0)
Gpio_20	I		Ball E7(mode0)
Gpio_21	I	cam_s_data	Ball A5(mode0)
Gpio_22	I		Ball E6(mode0)

Table 39 : Serial Camera Sensor Generic Pins Multiplexing Configuration

17.2 ELECTRICAL CHARACTERISTICS

17.2.1 Parallel Camera Interface(Main/Alternate) Timings

The following table assumes testing over recommended operating conditions.

NO.	PARAMETER		MIN	MAX	UNIT
C1	1 / [tc(LCLK)]	Operating frequency, CAM_LCLK		48(4)	MHz
C2	1 / [tc(EXCLK)]	Operating frequency, CAM_XCLK	1.6	48(4)	MHz
C3	tw(LCLK)	Pulse duration, CAM_LCLK high or low	0.45 P1(1)	0.55 P1(1)	ns
C4	tw(EXCLK)	Pulse duration, CAM_XCLK high or low	0.45 P2(2)	0.55 P2(2)	ns
C5	tr(LCLK)	Rise time, CAM_LCLK		0.15 P1	ns
C6	tf(LCLK)	Fall time, CAM_LCLK		0.15 P1	ns
C7	tr(EXCLK)	Rise time, CAM_XCLK		0.15 P2	ns
C8	tf(EXCLK)	Fall time, CAM_XCLK		0.15 P2	ns
C9	tsu(LCLKH-DV)	Setup time, CAM_D_[7:0] data valid before CAM_LCLK high	3.5 (3)		ns
C10	th(DV-LCLKH)	Hold time, CAM_D_[7:0] data valid after CAM_LCLK high	-0.6 (3)		ns
C11	tsu(LCLKH-DV)	Setup time, CAM_VS/CAM_HS active before CAM_LCLK high	3.5 (3)		ns
C12	th(DV-LCLKH)	Hold time, CAM_VS/CAM_HS active after CAM_LCLK high	-0.8 (3)		ns
C13	tw(VS)	VS minimum pulse with	(5)		
C14	td(VS rise- HS rise)	Time delay VS rise to HS rise	0		ns
C15	td(HS fall –VS fall)	Time delay HS fall to VS fall	0		ns
C16	Tw(HS)	HS minimum pulse width	1		Clk cycle

Note: Input slew requirement is 0.9v/ns
Electrical level used for timing measurements – 0.25Vdds to 0.75Vdds (rise)
0.75Vdds to 0.25Vdds (fall)

(1) P1 = period of CAM_LCLK in nanoseconds (ns).
(2) P2 = period of CAM_XCLK in nanoseconds (ns).
(3) Polarity of CAM_LCLK is selectable via the POLCLK bit in the CTRLCLOCK register. Although data is latched on rising CAM_LCLK in the timing diagrams, these timing parameters also apply to falling CAM_LCLK when POLCLK = 1.
(4) The clock domain can be as high as 48MHz for 8-bit data .
(5) 10 clk cycles when line is not multiple of 12 bytes.
1 clk cycle when line is multiple of 12 bytes.

Table 40 : Camera Interface Timing Requirements

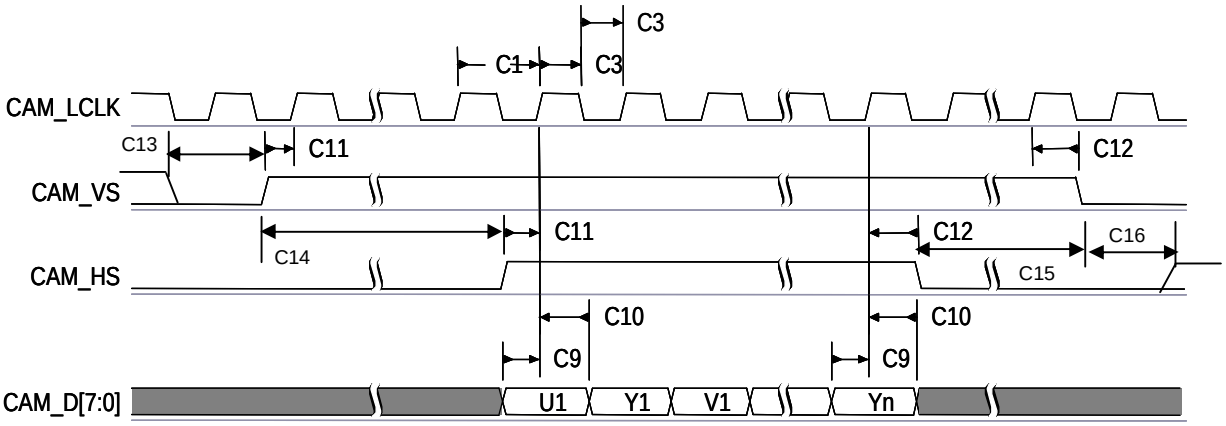
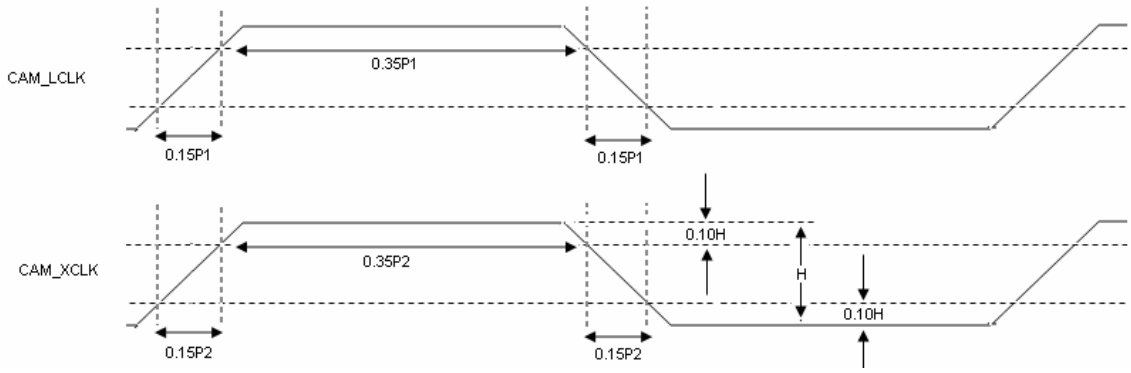


Figure 22 : Camera Interface Timings

NOTES:

The parallel interface mode supports two operating modes : ITU-R BT656-compliant and general parallel interface.



17.2.2 Compact Serial Camera Port (CCP) Timings

The following table assumes testing over recommended operating conditions

NO.	PARAMETER		MIN	MAX	UNIT
C1	1 / [tc(CLK)]	Operating Frequency, CAM_S_CLK input frequency(1)		104	MHz
C2	tw(CLK)	Pulse duration, CAM_S_CLK high or low	0.4 P(2)	0.6 P(2)	ns
C3	tsu(DV-CLKH)	Setup time, CAM_S_DATA valid before CAM_S_CLK high	5.3		ns
C4	th(CLKH-DV)	Hold time, CAM_S_DATA valid after CAM_S_CLK high	- 0.7		ns

Table 41 : CCP Interface Timing Requirements with Pixel Clock @ 104 MHz

NO.	PARAMETER		MIN	MAX	UNIT
C1	1 / [tc(CLK)]	Operating Frequency, CAM_S_CLK input frequency(1)		208	MHz
C2	tw(CLK)	Pulse duration, CAM_S_CLK high or low	0.4 P(2)	0.6 P(2)	ns
C3	tsu(DV-CLKH)	Setup time, CAM_S_DATA valid before CAM_S_CLK high	3.6		ns
C4	th(CLKH-DV)	Hold time, CAM_S_DATA valid after CAM_S_CLK high	-0.3		ns

(1) When nothing is being transferred, Clk has to remain high level, except in power shut-down.

(2) P = period of CAM_S_CLK in nanoseconds (ns).

Table 42 : CCP Interface Timing Requirements

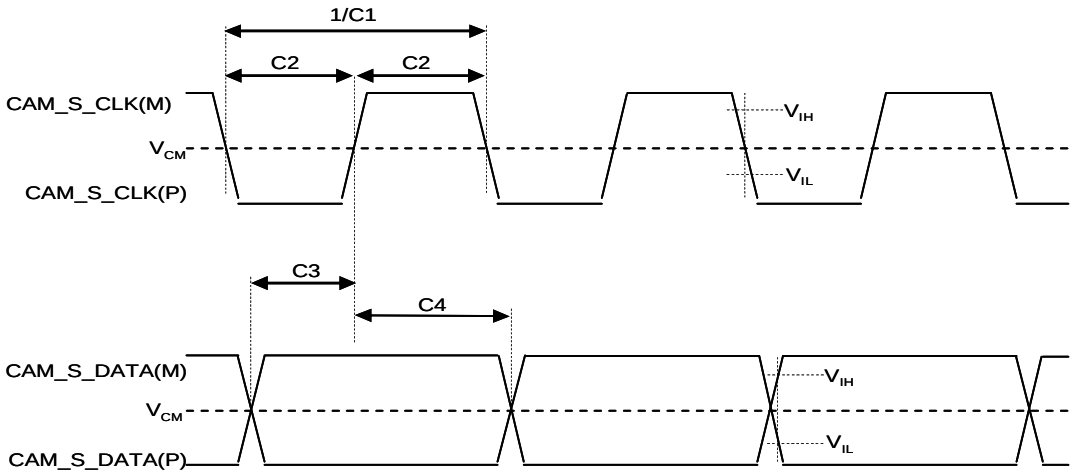


Figure 23 : CCP Interface Timings

18 KEYBOARD CONTROLLER

18.1 FUNCTIONAL DESCRIPTION

The keyboard controller implements a built-in scanning algorithm for hardware-based key press decoding. It allows MPU software overhead reduction.

Locosto keyboard controller can handle up to 5*5 keyboards. It works on a 32 kHz clock clocks so on all chip activity modes, including sleep mode.

Signal Name	Direction	Description
kbr_0	I	Keyboard matrix row 0 input
Kbr_1	I	Keyboard matrix row 1 input
kbr_2	I	Keyboard matrix row 2 input
kbr_3	I	Keyboard matrix row 3 input
kbr_4	I	Keyboard matrix row 4 input
kbc_0	O	Keyboard matrix column 0 output
kbc_1	O	Keyboard matrix column 1 output
kbc_2	O	Keyboard matrix column 2 output
kbc_3	O	Keyboard matrix column 3 output
kbc_4	O	Keyboard matrix column 4 output

Table 43 : Keyboard Controller Pins Description

19 CLOCKS, RESET AND POWER MANAGEMENT

19.1 FUNCTIONAL DESCRIPTION

The LOCOSTO device clocks/reset/power architecture includes the functional clocks, interface clocks, reset distribution and wake-up requests for the LOCOSTO platform, and LOCOSTO peripherals.

Except the 32KHz source (clkin_32khz) and the external clock (clkm_clk), the clocks dispatched through the Locosto core are generated from one 13MHz source (ClkDRP13) provided by the DRP2.0 module These clocks are controlled by the Clock Manager module (CLKM) which also manages the power saving modes with the help of the Ultra Low Power Down (ULPD) module. Four different clock frequencies are provided to the CLKM module before dispatching the clocks through the core:

Signal Name	Direction	Description
Ckin_32khz	I	External 32-kHz clock source input
On_off	I	Power-on reset from Triton Lite
Wakeup_req	O	wake up request to Ttriton Lite
Ckout_13mhz	O	External clock from Locosto to Triton Lite and peripherals.

Table 44 : Clock and reset pin description.

19.2 ELECTRICAL CHARACTERISTICS

19.2.1 ON_nOFF timings

The ON_nOFF signal is the active-low asynchronous reset input responsible for the reset of the entire LOCOSTO device. ON_nOFF must be asserted low a minimum of two 32-kHz clock cycles after stable power supplies.

NO.			MIN	TYP	MAX	UNIT
RS1	$t_{w(ON\_nOFF)}$	Pulse duration, ON_nOFF		13.15 (1)		ms

Note:
(1) See TRITON LITE Datasheet

Table 45 : LOCOSTO Device Reset Timing Requirements

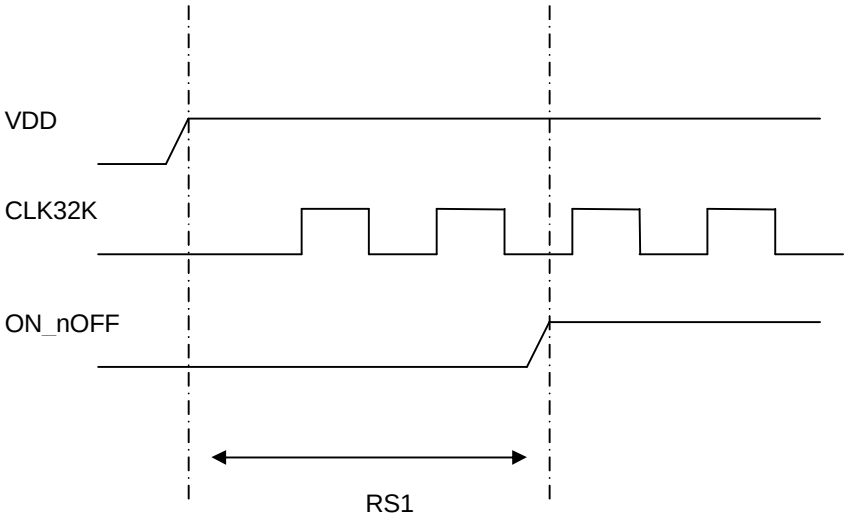


Figure 24 : Device Reset Timings

19.2.2 CKIN_32Khz Clock timings

A 32.768-kHz clock signal (often abbreviated to 32-kHz) can be supplied by an external 1.8V CMOS signal on pin ckin_32khz. The following table summarizes the electrical constraints imposed to the clock source.

NAME	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency (1)		32.768		kHz
C_i	Input capacitance		1.0653		pF

Table 46 : 32-kHz Input Clock Source Electrical Characteristics

NAME	PARAMETER DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	1/ tc(32k)	Frequency, ckin_32khz		32.768		KHz
CK1	tw(32k)	Pulse duration, ckin_32khz low or high	0.40 * tc(32k)		0.60 * tc(32k)	ns
CK2	tJ(32k)	Peak-to-peak jitter (1), ckin_32khz	-0.1		0.1	%
CK3	tr(32k)	Rise time, ckin_32khz			10	ns
CK4	tf(32k)	Fall time, ckin_32khz			10	ns

Note:

(1) Peak-to-peak jitter is defined as the difference between the maximum and the minimum output period on a statistical population of 300 period samples. The sinusoidal noise is added on top of the V_{DDS} supply voltage.

Table 47 : 32-kHz Input Clock Source Timing Requirements

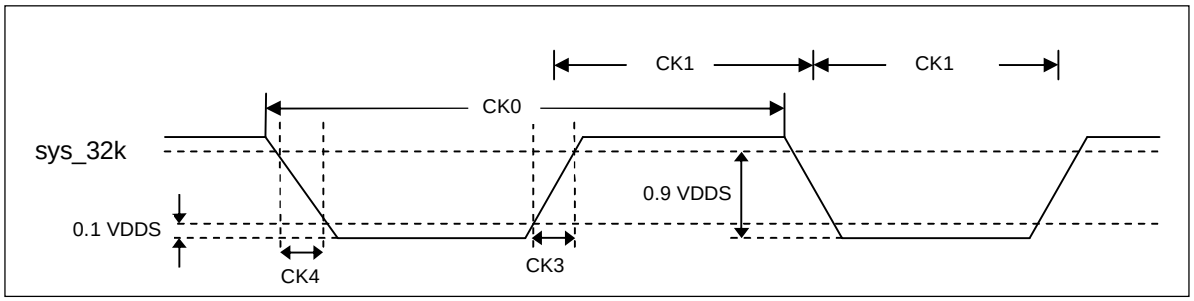


Figure 25 : LOCOSTO 32-kHz Clock

19.2.3 CKOUT_13Mhz output Clock timings

An output clock (pin ckout_13mhz) is available and can provide the 13 MHz reference system clock, it is routed to the TRITON power IC.

NAME	PARAMETER DESCRIPTION	MIN	MAX	UNIT
f	Frequency		13	MHz
C_l	Load capacitance		100	pF

Notes:
Load capacitance is adapted to a frequency.

Table 48 : 13Mhz Output Clock Electrical Characteristics

NAME	PARAMETER DESCRIPTION		MIN	MAX	UNIT
CO0	1 / tc(ckout)	Frequency		13	MHz
CO1	tw(ckout)	Pulse duration, sys_clkout low or high	0.45* tc(ckout)	0.55* tc(ckout)	ns
CK2	tJ(13m)	Peak-to-peak jitter, ckout_13mhz	-0.1	0.1	%
CK3	tr(13m)	Rise time, ckout_13mhz		3	ns
CK4	tf(13m)	Fall time, ckout_13mhz		3	ns

Table 49 : 13Mhz Output Clock Switching Characteristics

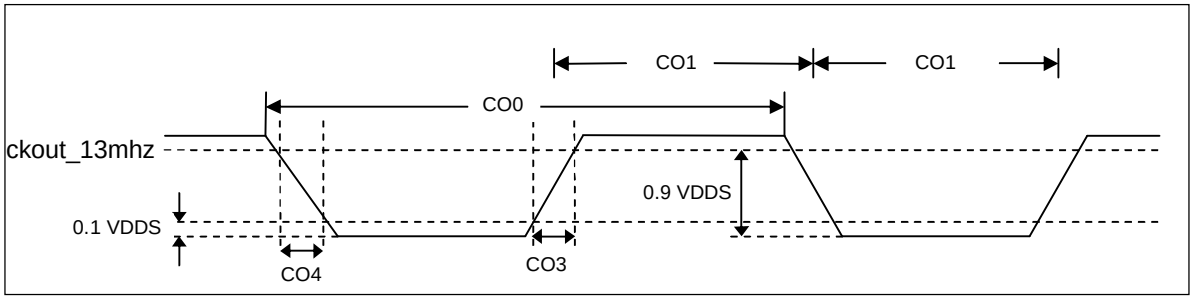


Figure 26 : LOCOSTO System Output Clock

20 JTAG AND DEBUG

20.1 FUNCTIONAL DESCRIPTION

LoCosto Test Access Port controller interfaces the standard IEEE JTAG serial protocol.

The chip integrates 5 x TAP/JTAG controllers to control respectively the LoCosto chip and the DRP2.0 Sub-Chip test hardware configurations, the Fuse-Farm controller, the ARM7TDMI MCU and the C54x DSP emulation's.

Signal Name	Direction	Description
TCK	I	JTAG clock
TMS	I	Test mode select.
TDI	I	JTAG data input
TDO	O	JTAG data output

Table 50 : JTAG pin description.

20.2 ELECTRICAL CHARACTERISTICS

20.2.1 JTAG INTERFACE TIMINGS

NAME	PARAMETER DESCRIPTION		MIN	MAX	UNIT
C0	td(TDO)	Delay time, TCK low to TDO valid		15	ns
C1	th(TDO)	Hold time , TCL low to TDO invalid	2.5		Ns

Table 51 : JTAG switching characteristic

NAME	PARAMETER DESCRIPTION		MIN	MAX	UNIT
C2	tsu(TMS)	Setup time, TMS valid before TCK rise edge	5		ns
C3	th(TMS)	Hold time, TMS valid after TCL rise edge	5		ns
C4	ts(TDI)	Setup time, TDI valid before TCK rise edge	5		ns
C5	th(TDI)	Hold time, TDI valid after TCL rise edge	5		ns

Table 52 : JTAG timing requirement

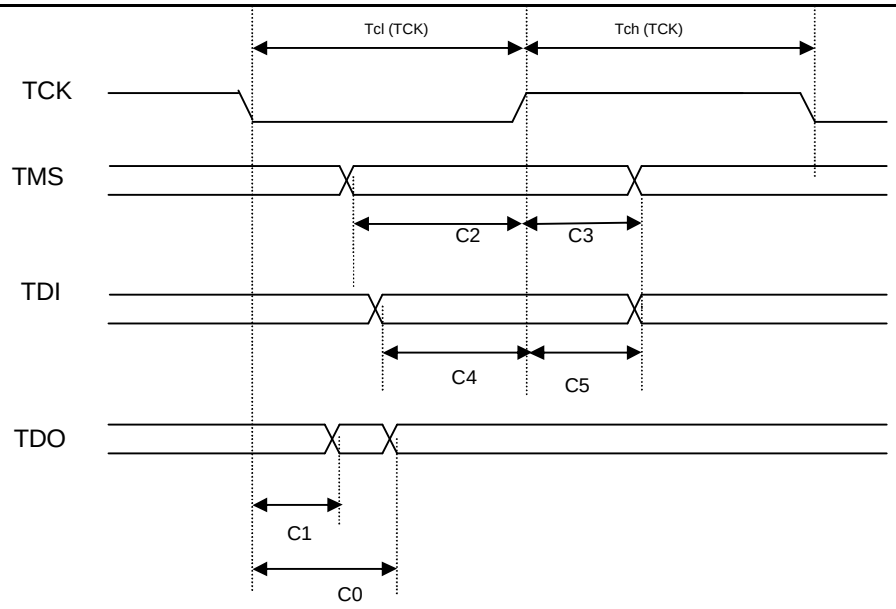


Figure 27 : JTAG interface timing.

21 NAND FLASH INTERFACE

21.1 FUNCTIONAL DESCRIPTION

The Nand Flash controller is the interface between the host processor and the Nand Flash Memory: it allows connecting NAND Flash EEPROM as an external mass storage facility.
The aim of this controller is to have a fully automatic transfer process from/to the Nand Flash Port: the interface implements a 8 bits parallel data bus (commands, addresses and data are multiplexed) in addition to the control signals for selecting chip, writing/reading, command and address latching, ready/busy status.

The Nand Flash Controller is multiplexed with the LCD interface in the default configuration. The Nand data bus is also accessible on other balls (gpio optional configuration), please go to Locosto TRM Configuration chapter for detailed information about this optional nand data bus access.

Pin Name	I/O	Description
ndf_dyn_[7:0](1)	I/O	NandFlash Address/Data Bus
ndf_[7:0](2)	I/O	NandFlash Address/Data Bus
nd_ce1	O	NandFlash chip enable
nd_we	O	NandFlash write enable
nd_re	O	NandFlash read enable
nd_cle	O	NandFlash command latch enable
nd_ale	O	NandFlash address latch enable
nd_rdy	I	NandFlash ready/busy signal
nd_nwp	O	NandFlash write protect signal

(1) ndf_dyn_[7:0] bus is muxed with lcd_data bus and is accessible on lcd_data* balls

(2) ndf_[7:0] bus is accessible on balls other than lcd_data*. Refer LOCOSTO TRM for details.

Table 53 : Nand Flash Controller Pins Description

21.2 ELECTRICAL CHARACTERISTICS

21.2.1 NAND FLASH CONTROLLER INTERFACE TIMINGS

The following tables assume testing over recommended operating conditions

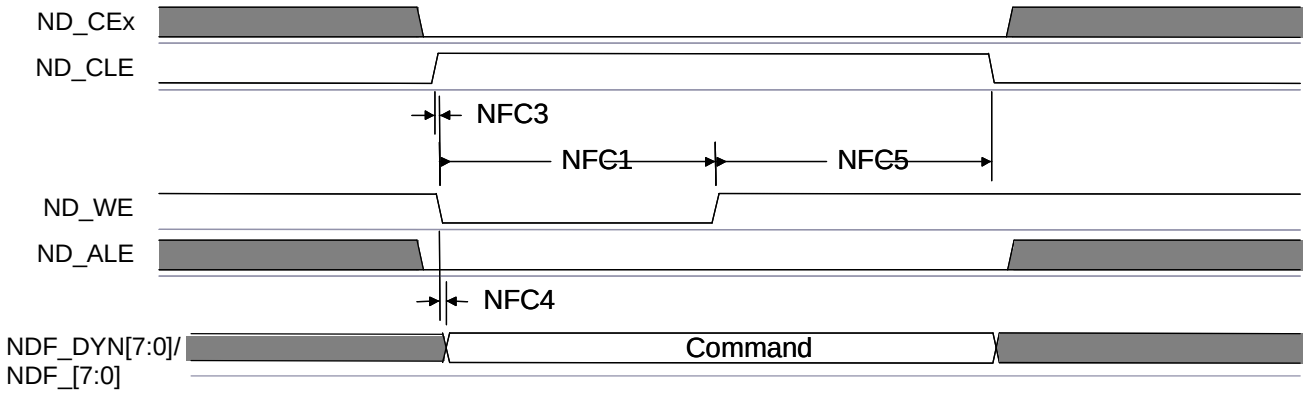
No	Parameter		Min	Max	Unit
NFC10	tsu(IOV-REH)	Setup time, NFLS_FD[7:0] valid before NFLS_RE high	5		ns
NFC11	th(REH-IOV)	Hold time, NFLS_FD[7:0] valid after NFLS_RE high	5		ns

Table 54 : Nand Flash controller Timing Requirements

No	Parameter		Min	Max	Unit
NFC1	tW(WEV)	NFLS_WE low duration	P(1)-1.5	P(1)+1	ns
NFC2	tW(WEIV)	NFLS_WE high duration	P(1)-1	P(1)+1.5	ns
NFC3	td(CLEV-WEV)	Delay time, NFLS_CLE high to NFLS_WE low	-0.3	+3.3	ns
NFC4	td(WEV-IOV)	Delay time, NFLS_WE high to NFLS_FD valid	1	+8	ns
NFC5	td(WEiV-CLEL)	Delay time, NFLS_WE high to NFLS_CLE low	P(1) – 3.3	P(1)+0.3	ns
NFC6	td(ALEV-WEV)	Delay time, NFLS_ALE high to NFLS_WE low	-1	+3.3	ns
NFC7	td(WEiV-ALEL)	Delay time, NFLS_WE high to NFLS_ALE low	P(1)-3.3	P(1)+1	ns
NFC8	tW(REV)	NFLS_RE low duration	P(1)-1.5	P(1)+1.5	ns
NFC9	tW(REIV)	NFLS_RE high duration	P(1)-1.5	P(1)+1.5	ns

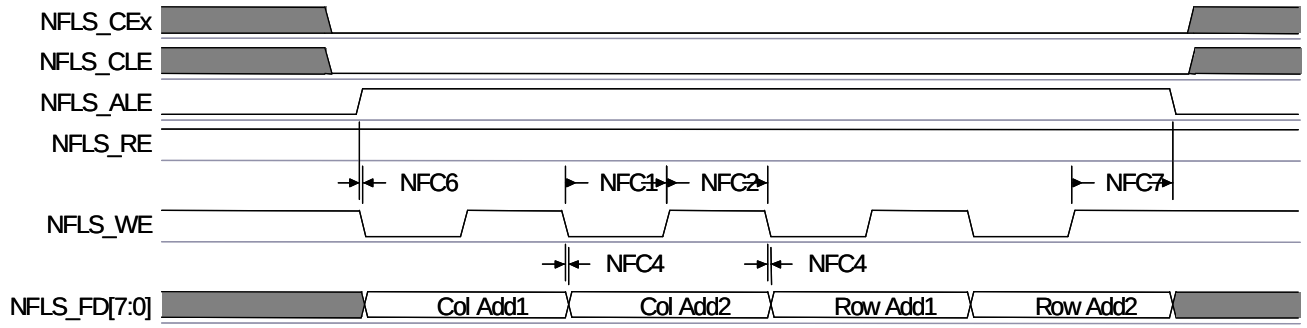
(1) P = (NND_CNTL_CLK_DIV register value) *(ARM clock period * 2).

Table 55 : Nand Flash Controller Switching Characteristics



Note : NFLS_CE1 signal is under software control. It should be asserted before attempting any access to the memory and deasserted after accesses are complete.

Figure 28 : Nand Flash Controller - Command Latch Timing



Note : NFLS_CE1 signal is under software control. It should be asserted before attempting any access to the memory and deasserted after accesses are complete.

Figure 29 : Nand Flash Controller - Address Latch Timing

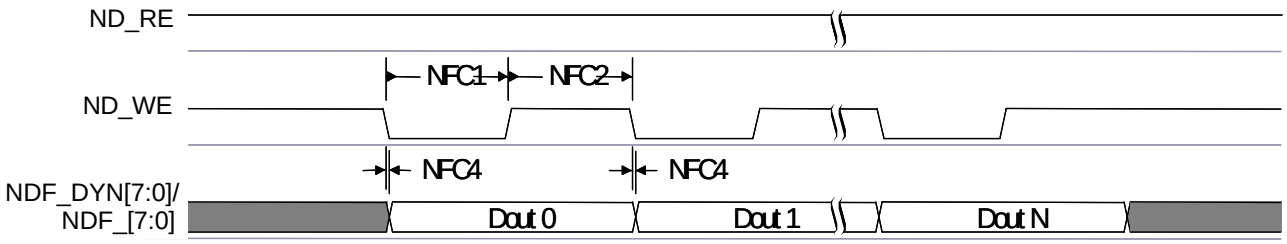


Figure 30 : Nand Flash Controller - Memory Write Timing

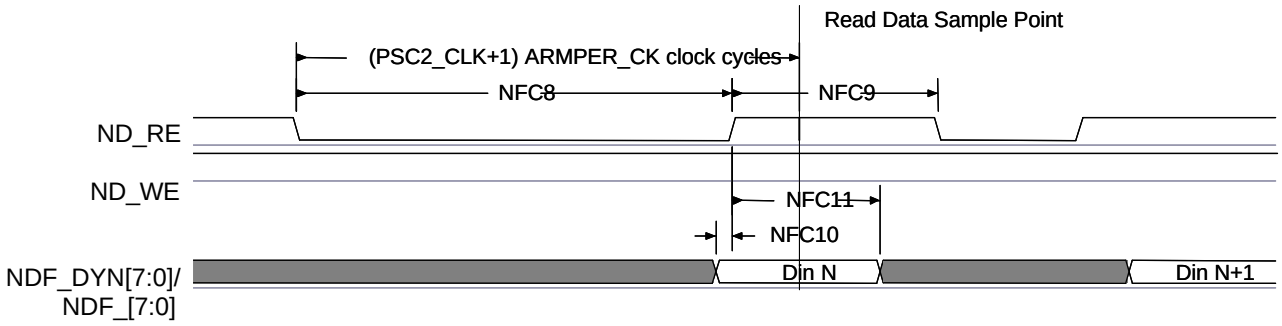


Figure 31 : Nand Flash Controller - Memory Read Timing

22 CPORT

22.1 FUNCTIONAL DESCRIPTION

The LOCOSTO includes a CODEC port (C-port) interface module dedicated to audio applications. The Codec port (C-port) interface is a serial interface used to transfer data between the DSP or MPU and a CODEC device The C-port interface can be configured to support several industry standard serial interface protocols. These protocols include:

- the Inter-IC sound (I2S) mode
- the 16-bit Pulse Code modulation (PCM) mode : LSB-justified format or Standard format
- the AC'97 Revision 1.x without sample rate converter mode.

An external companion chip can be provided for serial audio interface. C-port can be used both in slave and master modes.

Signal Name	I/O			Description
	I2S	PCM	AC97	
csync	O (master mode) I (slave mode)	O	O	CODEC port interface frame synchro
csclk	O (master mode) I (slave_mode)	O	I	CODEC port interface serial clock
cdo	O	O	O	CODEC port interface serial data output
cdi	I	I	I	CODEC port interface serial data input
pmc_reset	O (master mode only)	O	O	CODEC port interface output reset
pmc_clk	I (master mode only)	I	I	CODEC port interface input master clock (provided by an external clock generator)

Table 56 : C-PORT Pins Description

The pmc_reset, pmc_clk and cdi signals are respectively multiplexed with gpio_1, gpio_2, and gpio_4 pins.
The csync, csclk and cdo signals are available in:

- Primary mode 0: for direct access on these signals
- Multiplexed mode: csync (input mode only), csclk (input mode only)

Note:

- In master mode, the serial and synchro clocks (44.1-kHz clock) are generated using a divider of a clock that should be fixed at 11.2896 MHz to achieve such a frequency. In LOCOSTO device, by default the C-port clock frequency is fixed at 13 MHz in slave mode and if the user want to configure the C-port interface in master mode with a slave codec, he must apply to external input clock pin (pmc_clk) a clock generator at the right frequency (11.2896 MHz in I2S and PCM modes, 12.288 MHz in AC'97 mode). pmc_clk and pmc_reset signals are used in master mode only.
- In slave mode, the serial and synchro clocks are generated through the 13-Mhz ClkCport clock.

22.2 ELECTRICAL CHARACTERISTICS

22.2.1 INTERFACE TIMINGS

NAME	PARAMETER DESCRIPTION		MIN	MAX	UNIT
C0	Tw(CSCLK)	Pulse duration, serial port clock	651		Ns
C1	Tc(CSCLK)	Cycle time, serial port clock	1302		Ns
CSCLK = external clock / CSYNC = input					
C2	Td(CDO)	Delay time, Data valid after CLK rising		15	Ns
C3	Th(CDO)	Hold time, Data valid after CLK rising	2		Ns
C4	Tsu(CDI)	Setup, Data valid before CLK falling	5		Ns
C5	Th(CDI)	Hold time, Data valid after CLK falling	1		Ns
C6	Tsu(CSYNC)	Setup, CSYNC valid before CLK falling	7.5		Ns
C7	Th(CSYNC)	Hold time, CSYNC after CLK falling	1		Ns
CSYNC = output					
C8	Td(CSYNC)	Delay time, CSYNC after CLK falling edge		15	Ns
C7	Th(CSYNC)	Hold time, CSYNC after CLK falling edge	2		Ns
CSCLK = internal clock / CSYNC = input					
C6	Tsu(CSYNC)	Setup, CSYNC valid before CLK falling	10		Ns
C7	Th(CSYNC)	Hold time, CSYNC after CLK falling	1		Ns
CSCLK = internal clock / CSYNC = output					
C8	Td(CSYNC)	Delay time, CSYNC after CLK falling edge		15	Ns
C7	Th(CSYNC)	Hold time, CSYNC after CLK falling edge	2		Ns

Table 57 : C-PORT timing parameters

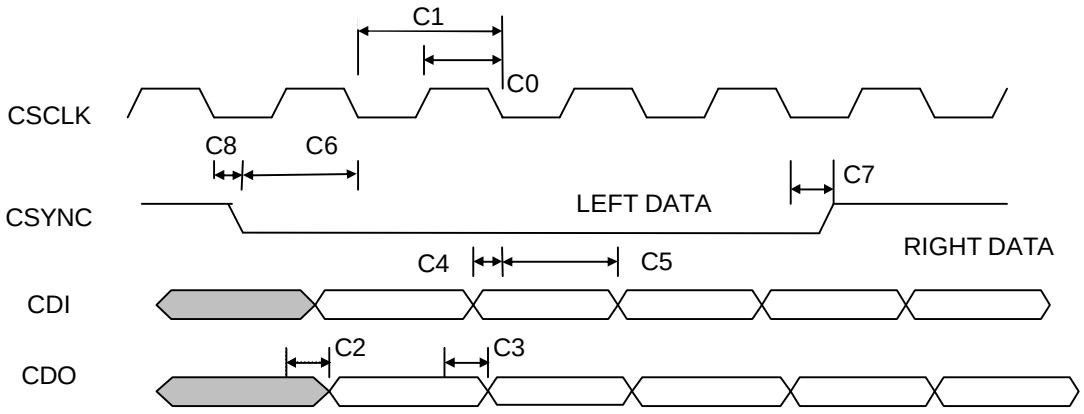


Figure 32 : CPORT interface timings

23 VSP

23.1 FUNCTIONAL DESCRIPTION

The voice serial port (VSP) is a bi-directional (transmit/receive) serial port that directly connects the c30L154's Serial Port Interface (DSP SPI) to the voice CODEC of the ABB companion chip (Triton Lite).
Format is 16-bit data packet with frame synchronization. Clock frequency is 500 KHz.

Signal Name	I/O	Description
Vclkrx	I	Clk input from triton
vfsrx	I	Frame synchronization signal from triton
vdr	I	Receive data input from triton
vdx	O	Transmit data output to triton

Table 58 : VSP pin description.

23.2 ELECTRICAL CHARACTERISTICS

23.2.1 INTERFACE TIMINGS

PARAMETER		MIN	MAX	UNIT
t_{RSD}	Setup time VDR valid before VCLK fall edge	3		ns
t_{RHD}	Hold time VDR valid after VCLK fall edge	1		ns
t_{RSS}	Setup time VFS valid before VCLK fall edge	4		ns
t_{RHS}	Hold time VFS valid after VCLK fall edge	3		ns

Table 59 : VSP timing requirement with respect to VCLK

PARAMETER		MIN	MAX	UNIT
t_{DX}	Delay time VCLK rise edge to data valid	3.5	14	ns

Table 60 : VSP switching characteristics.

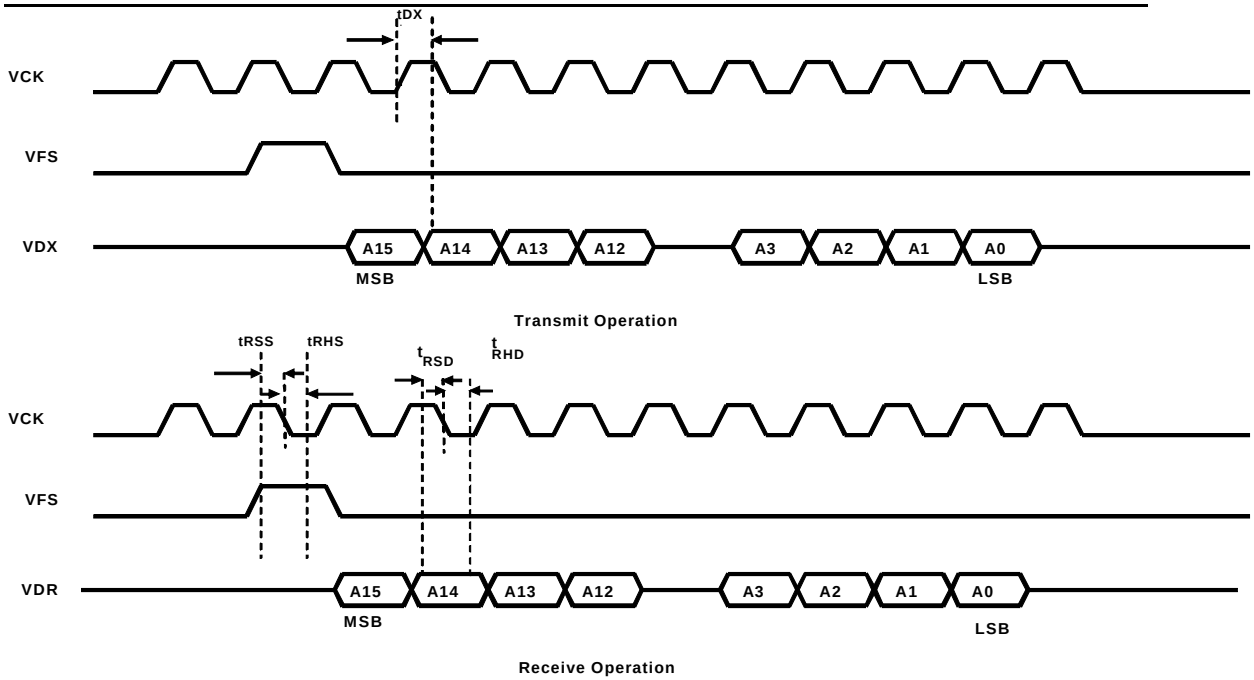


Figure 33 : VSP interface timings.

24 APC

24.1 FUNCTIONAL DESCRIPTION

The automatic power control (APC) generates an envelope signal to control the power ramp-up, power ramp down and the power level of the radio burst coming out of the power amplifier. The APC structure is intended to support single-slot and multi-slot transmission with smooth power transition when consecutive bursts are transmitted at different power levels.

APC consists of a digital section and the analog section. Digital section (APCD) generates the correct ramping profiles from coefficients stored in a RAM and handles the sequencing of the ramp up/down operation. Analog section of the APC consists of a DAC, an output amplifier and a reference and LDO to produce the correct output power levels.

The shape of ramp-up/down is computed from the value of the power level step and from the coefficients of the desired shaping filter:

- The power step is obtained by subtracting the previous power level (initialized to zero when Tx_Start goes low) from the new power level (APCLEV: 10 bits word).
- The ramp shape is sampled at Fs= 4* 270.833kHz. Its duration (ramp-up or ramp-down) is 5 bits duration (5/270.833e3= 18.4us). So the ramp shape (up or down) is constituted by 20 coefficients which are stored in a RAM (APCRAM). APCRAM register includes 20 16-bits words. The 8 LSBs of each word represent the coefficients of the ramp-up shape, the 8 MSBs represent the coefficients of the ramp-down shape.

According to the sign of the power step to be performed, ramp-up or ramp-down coefficients are selected.

The sequence of 10-bits words fed to the 10bit APC DAC is:

Fs= 4* 270.833 kHz:

$$Level(i) = Level_{init} + (step_{level} / 256) \cdot \left(up[i] * (1 - sign_{step}) + dw[i] * sign_{step} \right)$$

where:

$level_{init}$ is the current power level
$step_{lev}$ is the power level step to be done
up[i] are the coefficients of the ramp-up
dw[i] are the coefficients of the ramp-down
$sign_{step}$ is the sign of $step_{lev}$ (0 for plus, 1 for minus)

This ramp is therefore constituted by 20 steps for ramp-up and 20 steps for ramp-down (Fs=4*270.833kHz). No further interpolation is needed.

Before being fed to the 10-bit DAC, the content of the offset register (APCOFF) is added to the 10-bit words computed before.
To have the proper behavior the analog part has to be turned on sequentially.

Sequence is :

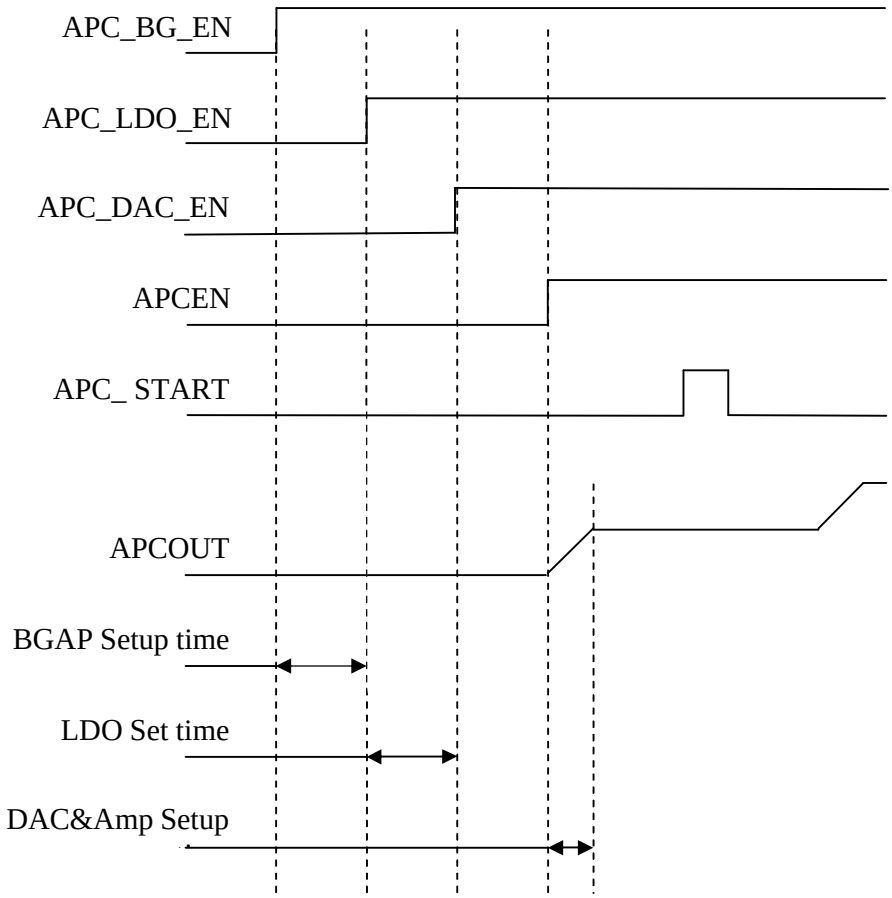


Figure 34 : APC ramp up sequence

Signal Name	I/O	Description
APC_OUT	OUT	APC output ramp signal
APC_LDO_FILTER	-	LDOAPC pin
APC_VDD	-	VDD pin
APC_VREF	-	Vref pin
APC_VSS	-	Ground pin

Table 61: APC analog pins description

24.2 ELECTRICAL CHARACTERISTIC

Signal Name	Test Conditions	min	nom	max	unit
Global Parameters					
Supply Voltage (VDD-APC)		2.7	2.8	2.95	V
BG reference for APC internal use		0.882	0.9	0.918	V
BG quiescent current		160	220	240	•A
BGAP setup time		-	-	1	ms
BG external filter Cap	±10%	-	470	-	nF
LDO Output voltage for internal use		1.71	1.8	1.95	V
LDO setup time		-	-	1	•s
LDO Decoupling Cap		-	100	-	nF
APC Output stage Slew rate		-	1	-	V/•s
Max code APC output voltage	Code = 1023	2.1	2.25	-	V
Min code APC output voltage	Code =0	-	-	100	mV
Output voltage level at APC_OUT in power down		-	-	50	mV
Output current		-	-	200	•A
Output load capacitance		-	-	50	pF
Output load resistance		10	-	-	K Ohm
INL	Between 0.1V to 2.1V output	-2	-	2	LSB
DNL	Between 0.1V to 2.1V output	-2	-	2	LSB

Table 62 : APC Electrical characteristic.

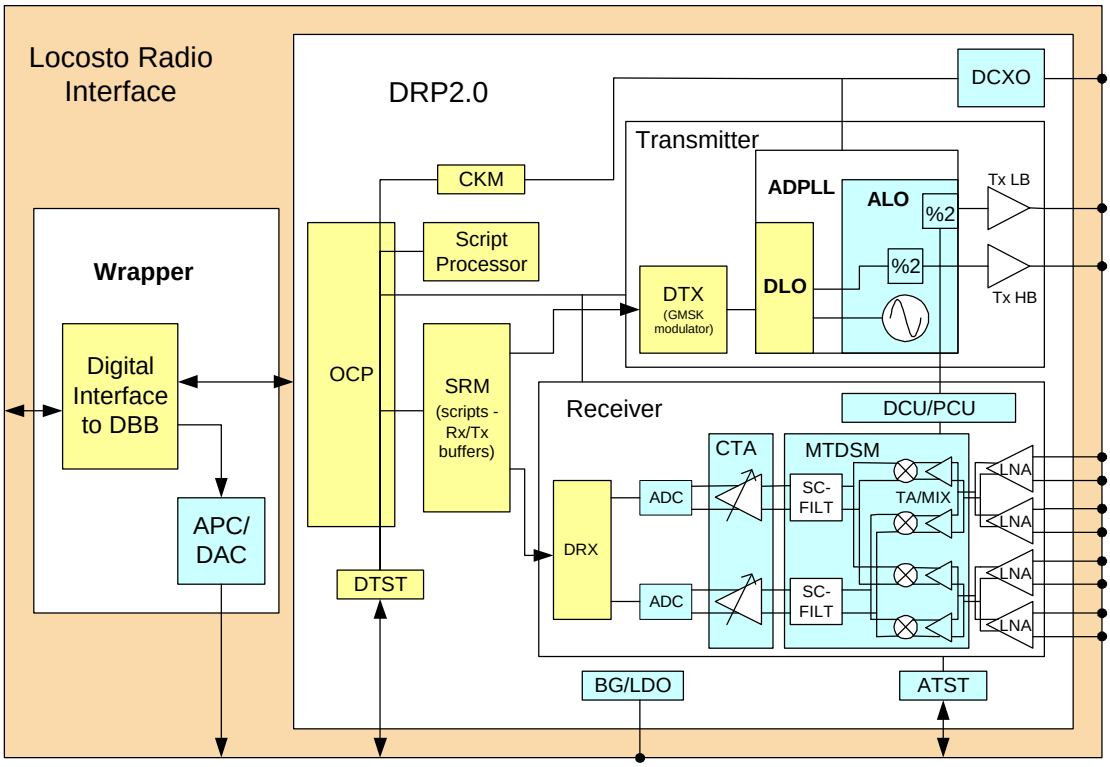
25 RF

25.1 FUNCTIONAL DESCRIPTION

Locosto Radio Interface is a quadruple band transceiver sub-module suitable for GSM850, E-GSM900, DCS1800 and PCS1900 GPRS Class 12 applications.

Locosto Radio Interface is based on the DRP2.0 module. This module integrates a receiver based on a near zero IF or a zero IF architecture and a transmitter based on an ADPLL synthesizer which has a phase/frequency modulation capability. The receiver LO generation is performed by the ADPLL synthesizer.

Locosto supports dual-band, tri-band and quad-band operations.
Same low-band inputs are used for the 2 types of dual-band and tri-band phones (EU/US):
GSM 850 inputs for 850MHz (US) and 900MHz (EU) bands
Same high-band inputs are used for the 2 types of dual-band phones (EU/US)
DCS 1800 inputs for 1800MHz (EU) and 1900MHz (US) bands
This is described in APN222.



25.2 Reference Clock

The reference clock is based on a Digitally-Controlled-Crystal-Oscillator (DCXO) architecture. The oscillator uses an external 26 MHz crystal. The AFC is done by programming the corresponding register through the control interface. Frequency correction is accomplished by digital control of the internal oscillator capacitor.

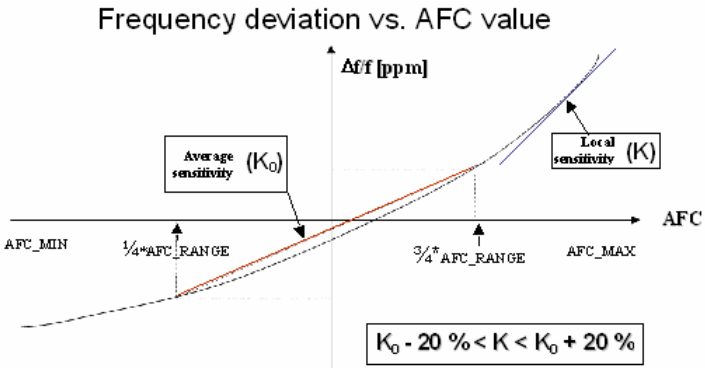
External Crystal

The 26MHz crystal requirements for crystal manufactures is covered by application note APN221. Please contact TI support team to get crystal requirements for Locosto.

DCXO

Typical: Ta = +25°C, nominal supply voltage - Min 1 and Max 1: Ta= +25°C over Process and supply voltage
Min2 and Max 2: Ta= -25°C to +85°C over Process and supply voltage

Parameters	Test conditions	Symbol	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
Center Frequency			-	-	26	-	-	MHz
Frequency error before calibration			-50	-	-	-	+50	ppm
Dynamic range	After calibration		-20/+20					ppm
Frequency resolution	Step to step		0	-	0.03	-	+0.05	ppm/LSB
Number of control bits					14			bits
Frequency settling time	Stable output frequency (+/- 1ppm of final) after frequency step				50			us
Sensitivity accuracy[1]	Over Temp and over tuning range		-20	-	-	-	+20	%
Startup Time	From clock request to stable output frequency (+/-0.1ppm of final)		-	-	5	-	12	ms



[1] The sensitivity accuracy is how much the "local sensitivity" can differ from the average sensitivity. In other words, it is the derivate of the sensitivity. See the plot below.

25.3 Transmitter

25.3.1 Low Band Output

Dedicated to GSM850 and E-GSM900
Random Data Bit Stream applied at the transmitter input
Typical: nominal supply voltage Ta = +25°C; Min 1 and Max 1: Ta= +25°C, nominal supply voltage over Process
Min2 and Max 2: Ta= -25°C to +85°C, over supply voltage and over Process

Parameters	Test conditions	Symbol	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
Output Frequency	GSM850	Fout	824	-	-	-	849	MHz
	GSM900	Fout	880	-	-	-	915	MHz
Output Return Loss							-10	dB
Output Power	PPA is ON 24us before useful bit	Pout	6	-	8	-	10	dBm
RMS Phase Error (dithering on channel multiple of 26MHz) (2)			-	-	1.5		3	degrees
Peak Phase Error							14	degrees
Phase Noise	In 925 – 935 MHz when in E-GSM900 (10MHz offset)		-	-	-163	-151		dBc/Hz
	In 935 – 960 MHz when in E-GSM900 (20MHz offset)					-160		
	In 869 – 894 MHz when in GSM850 (20MHz offset)				-163	-160		
Settling time	From power down to final frequency @20MHz averaged frequency error over one burst						235	us

Notes:
(1) Dithering on channel multiple of 26MHz is required to meet phase error performance (Dithering consists of injecting a non-synchronous signal of relatively small amplitude with respect to reference signal into XTAL input pin thru a filtering network). This "dithering signal" is generated by routing a clock signal from a DBB pin at *frequency* controlled by DRP software).
External circuitry is required to perform this function and recommended schematic is available from TI application note **APN227**.
(2) Peak phase error value measured at device output.

GSM850/GSM900 Modulated Output Spectrum

Typical: nominal supply voltage Ta = +25°C; Min 1 and Max 1: Ta= +25°C, nominal supply voltage over Process
Min2 and Max 2: Ta= -25°C to +85°C, over supply voltage and over Process

Parameters	Test conditions	Symbol	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
Output Spectrum in 30kHz BW	@200kHz offset		-	-	-34	-	-33	dBc
	@400kHz offset		-	-	-66	-	-62	dBc
	>600kHz and <1.8MHz		-	-	-70	-	-67	dBc
Output Spectrum in 100kHz BW	>1.8MHz and <3MHz		-	-	-80	-	-70	dBc
	>3MHz and <6MHz		-	-	-86	-	-80	dBc
	>6MHz		-	-	-92	-	-86	dBc

25.3.2 High Band Output

Dedicated to DCS1800 and PCS1900
Random Data Bit Stream applied at the transmitter input
Typical: nominal supply voltage Ta = +25°C; Min 1 and Max 1: Ta= +25°C, nominal supply voltage over Process
Min2 and Max 2: Ta= -25°C to +85°C, over supply voltage and over Process

Parameters	Test conditions	Symbol	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
Output Frequency	DCS1800	Fout	1710	-	-	-	1785	MHz
	PCS1900	Fout	1850	-	-	-	1910	MHz
Output Return Loss							-10	dB
Max. Output Power	PPA is ON 24us before first useful bit	Pout	2.5	-	5	-	8	dBm
RMS Phase Error (dithering on channel multiple of 26MHz) (1)			-	-	2.5		3.5	degrees
Peak Phase Error	With PA						14(2)	degrees
Phase Noise @20MHz offset	In 1805 – 1880 MHz when in DCS 1800 In 1930 – 1990 MHz when in PCS 1900				-156 -156	-152 -152		dBc/Hz
Settling time	From power down to final frequency @ 40 Hz averaged frequency error over one burst		-	-	-	-	235	us

Notes:
(1) Dithering on channel multiple of 26MHz is required to meet phase error performance (Dithering consists of injecting a non-synchronous signal of relatively small amplitude with respect to reference signal into XTAL input pin thru a filtering network). This "dithering signal" is generated by routing a clock signal from a DBB pin at *frequency* controlled by DRP software).
External circuitry is required to perform this function and recommended schematic is available from TI application note **APN227**.
(2) Peak phase error measured at device output.

DCS1800/PCS1900 Modulated Output Spectrum

Typical: nominal supply voltage Ta = +25°C; Min 1 and Max 1: Ta= +25°C, nominal supply voltage over Process
Min2 and Max 2: Ta= -25°C to +85°C, over supply voltage and over Process

Parameters	Test conditions	Symbol	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
Output Spectrum in 30kHz BW	@200kHz offset		-	-	-34	-	-33	dBc
	@400kHz offset		-	-	-63	-	-61	dBc
	>600kHz and <1.8MHz		-	-	-70	-	-65	dBc
Output Spectrum in 100kHz BW	>1.8MHz and <6MHz		-	-	-80	-	-70	dBc
	>6MHz		-	-	-92	-	-80	dBc

dBc in this table means power relative to a measurement in 30kHz on the carrier

25.3.3 Spurious emissions

E-GSM 900

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-69	dBc
	from 1 GHz to 12.75 GHz				-63	dBc
	in the band [925 ~ 935 MHz]				-100	dBc
	in the band [935 ~ 960 MHz]				-112	dBc
	in the band [1805 ~ 1880 MHz]				-104	dBc
	in the bands [1900 ~1920 MHz], [1920 ~ 1980 MHz], [2010 ~ 2025 MHz] and [2110 ~ 2170 MHz]				-99	dBc

DCS 1800

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-66	dBc
	from 1 GHz to 12.75 GHz				-60	dBc
	in the band [925 ~ 935 MHz]				-97	dBc
	in the band [935 ~ 960 MHz]				-109	dBc
	in the band [1805 ~ 1880 MHz]				-101	dBc
	in the bands [1900 ~1920 MHz], [1920~ 1980 MHz], [2010 ~ 2025 MHz] and [2110 ~ 2170 MHz]				-96	dBc

GSM 850

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-69	dBc
	from 1 GHz to 12.75 GHz				-63	dBc
	in the band [869 ~ 894 MHz]				-112	dBc
	in the band [1930 ~ 1990 MHz]				-104	dBc

PCS 1900

Maximum allowed level when allocated channel	from 9 kHz to 1 GHz				-66	dBc
	from 1 GHz to 12.75 GHz				-60	dBc
	in the band [869 ~ 894 MHz]				-109	dBc
	in the band [1930 ~ 1990 MHz]				-101	dBc

5 exceptions maximum on any band measured at FTA channels and external PA output.

25.4 Receiver

25.4.1 Global Performances GSM850/GSM900

Typical: nominal supply voltage Ta = +25°C; Min 1 and Max 1: Ta= +25°C, nominal supply voltage over Process
Min2 and Max 2: Ta= -25°C to +85°C, over supply voltage and over Process

Parameters	Test conditions	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
RF Input Frequency	GSM850 Pins	869	-	-	-	894	MHz
	GSM900 Pins	925	-	-	-	960	MHz
Balanced RF Input Impedance	After external matching	-	-	150	-	-	Ohms
Voltage Gain[2]	High Gain (Maximum AFE-ABE gain settings)			62			dB
	Low Gain (Minimum AFE-ABE gain settings)	11	11	12	12	13	dB
RF Input Return Loss	High Gain	-	-	-	-	-10	dB
	Low Gain	-	-	-	-	-4	dB
Noise Figure[3]	High Gain	-	-	2.2	3.6	4.5	dB
Input 3rd order intercept point[4]	High Gain	-22	-21	-19		-	dBm
Noise Figure in blocking conditions[5]	High Gain				12		dB
Image rejection	After digital compensation algorithm (Max gain)	32					dB
IIP2[6]	High gain	22					dBm
Receiver Settling Time		-	-	-	-	140	µs

Offset from carrier	Power level at LNA input (dBm)
600 kHz	-45dBm
3 Mhz	-25dBm
10 Mhz	-25dBm
20 MHz	-22dBm
20 MHz	-23dBm

Table 63: Receiver noise figure in blocking condition: blocker frequency and power levels

[2] Equivalent voltage gain of the Rx analog section from 50 Ohm single ended voltage source (matched to LNA differential input) to one digital receiver differential output, assuming 0.9V reference voltage. See Annex 1 for more details.
[3] Noise Figure is measured from LNA matched differential input to one receiver digital output. Matching losses with low Q components are included. Noise is averaged over 1kHz to 100 kHz.
[4] Interferers(800kHz and 1.6MHz offset from carrier) for IIP3 test are applied at LNA matching network input with a power level = -51dBm
[5] Blocking signal power level and its frequency offset from carrier are defined in Table 64
[6] IIP2 test conditions: Two tones signal (at -6MHz offset from carrier) for IIP2 test is applied at LNA matching network input with a power level = -31dBm. Frequencies used: f1 = Fcarrier -6Mhz-IFreq and f2 = Fcarrier-6MHz-offsetfreq)

25.4.2 Global Performances DCS1800/PCS1900

Typical: nominal supply voltage Ta = +25°C; Min 1 and Max 1: Ta= +25°C, nominal supply voltage over Process
Min2 and Max 2: Ta= -25°C to +85°C, over supply voltage and over Process

Parameters	Test conditions	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
RF Input Frequency	DCS1800 Pins	1805	-	-	-	1880	MHz
	PCS1900 Pins	1930	-	-	-	1990	MHz
Balanced RF Input Impedance	After external matching	-	-	150	-	-	Ohms
Voltage Gain[7]	High Gain (Maximum AFE-ABE gain settings)			62			dB
	Low Gain (Minimum AFE-ABE gain settings)	11	11	11	12	13	dB
RF Input Return Loss	High Gain	-	-	-	-	-10	dB
	Low Gain	-	-	-	-	-4	dB
Noise Figure[8]	High Gain	-	-	2.4	3.6	4.5	dB
Input 3rd order intercept point[9]	High Gain	-22	-20	-19		-	dBm
Noise Figure in blocking conditions[10]	High Gain				12		dB
Image rejection	After digital compensation algorithm (Max gain)	32					dB
IIP2[11]	High gain	25					dBm
Receiver Settling Time		-	-	-	-	140	µs

Offset from carrier	Power level at LNA input (dBm)
600 kHz	-45dBm
3 Mhz	-28dBm
20 MHz	-27dBm
20MHz	-23dBm
100MHz	-23dBm

Table 64: Receiver noise figure in blocking condition: blocker frequency and power levels

[7] Equivalent voltage gain of the Rx analog section from 50 Ohm single ended voltage source (matched to LNA differential input) to one digital receiver differential output, assuming 0.9V reference voltage. See Annex 1 for more details.
[8] Noise Figure is measured from LNA matched differential input to one receiver digital output. Matching losses with low Q components are included. Noise is averaged over 1kHz to 100 kHz.
[9] Interferers(800kHz and 1.6MHz offset from carrier) for IIP3 test are applied at LNA matching network input with a power level = -51dBm
[10] Blocking signal power level and its frequency offset from carrier are defined in Table 64
[11] IIP2 test conditions: Two tones signal (at -6MHz offset from carrier) for IIP2 test is applied at LNA matching network input with a power level = -31dBm. Frequencies used: f1 = Fcarrier -6Mhz-IFreq and f2 = Fcarrier-6MHz-offsetfreq)

25.4.3 Front end measurement schematic

To measure front-end characteristics, considering its 100 ohms input, following schematic is proposed:

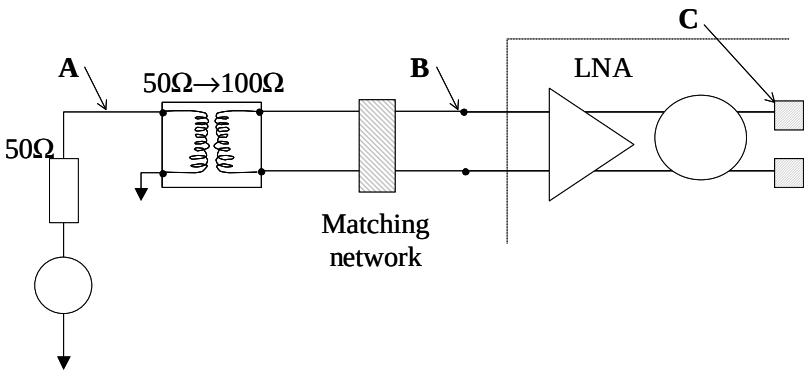


Figure 35: Rx RF gain definition

For the 50 to 100 Ω balun, following components can be used:

- Murata LDB20C101A0900
- Unbalance Impedance: 50 ohm
  Balance Impedance (Differential): 100 ohm
  Frequency range: 900 ± 100 MHz band
  Maximum insertion loss: 0.8dB (25°C); 0.9dB max. (-25~+85°C)
- Murata LDB20C101A1900
  Unbalance Impedance: 50 ohm
  Balance Impedance (Differential): 100 ohm
  Frequency range: 1900 ± 100 MHz band
  Maximum insertion loss: 0.8dB (25°C); 0.9dB max. (-25~+85°C)

All front-end data are specified and should be measured with:

- input point = A
- Output point = C (internal pads or test outputs)
- Balun losses have to be removed from measurement. They are not included in specification.
- Matching network must be built with standard capacitors and “LQG series” inductors. Its losses must be included in receiver noise figure.

25.5 LDOs / VREF / IREF SPECIFICATIONS

Parameter	*Unit*	LDOX	LDOOSC	LDORF	LDOA	VREF	IREF
Vout typ (after trim)	*V*	1.4	1.4	1.4	1.4	0.9	0.5
Max average current (during 625us)	mA	5	30	30	30	-	
External Cap	*uF*	1	4.7	1	1	0.47	
Main "function"		Low noise @low freq	Low noise @high freq	Low cost-area	Low cost-area		current reference
Vout range	*V*	1.393/1.407	1.2/1.8	1.1/1.8	1.1/1.8	0.882/0.918	between 0.2 and 0.6 V load voltage
Iinput range	*uA*						20*
Tied to		DCXO Temp sensor buffer	DCO Freq divider Buffers	PPA SAM LNTA	ABB		45K ohm resistance on board
Noise typ (1kHz)	*nV/Hz^0.5*	0.25	6.3	6.3	6.3		5nA/Hz^0.5
Noise typ (400kHz)	*nV/Hz^0.5*	27	9.1	23	23	16	1.6nA/Hz^0.5

Table 65 : DRP LDO / vref / iref specifications

25.6 TSPACT

The execution of the GSM scenario is based on real-time micro-instructions to schedule the programming of the real-time parallel port (TSPACT) that control the embedded Digital Radio Processor as well as the external RF Front End. There are 6 TSPACT signals provided which are controlled by TPU(time processing unit) and can be toggled with quarter bit accuracy.

Signal Name	I/O	Description
Tspact_7	O	Not used
Tspact_8	O	STARTADC input of TWL3029
Tspact_9	O	Not used
Tspact_10	O	Timestamp input of TWL5002
Tspact_11	O	B3 input of the TX module
Tspact_12	O	Not used
Tspact_13	O	B1 input of the Tx module
Tspact_14	O	Tx_enable input of the Tx module & PA_EN input of TWL5002
Tspact_15	O	B2 input of Tx module

Note : Table gives an example of use of TSPACT in the RFMD PA case used on I-sample

Table 66 : TSPACT pin description.

Appendices

A. Acronyms

ALE	Address Latch Enable
APE	Application Chip
APLL	Analog Phase Locked Loop
BIST	Built In Self Test
BT	Bluetooth
CE	Chip Enable
CLE	Common Latch Enable
CMT	Cellular Mobile Telephone
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CS	Chip Select
CTS	Clear To Send
DMA	Direct Memory Access
DPLL	Digital Phase Lock Loop
DSP	Digital Signal Processor
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMIF	External Memory Interface Slow
EOF	End Of File
FEC	Frame End Code
FIFO	First In First Out
FIQ	Fast Interrupt Request
FIR	Fast Infrared
GP	General Purpose
GPIO	General Purpose Input Output
HS	High Speed
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ID	Identification
IF	Interface
IO	Input Output
IrDA	Infrared Data Association
IRQ	Interrupt Request
JTAG	Joint Test Action Group, IEEE 1149.1 standard.
KBC	Keyboard Column
KBR	Keyboard Row
LCD	Liquid-Crystal Display
LEC	Line End Code
LH	Local Host
LPG	Light Pulse Generation
LSC	Line Start Code
LVDS	Low Voltage Differential Signaling
MCSI	Multi Channel Serial Interface
MCU	Micro Controller Unit
MIR	Medium Infrared
MMC/SD	Multi Media Card / Secure Data
MMU	Memory Management Unit
MPU	Micro Processor Unit

NDFLASH	Nand Flash Controller
OCP	Open Core Protocol
OS	Operating System
PCM	Pulse Code Modulation
PD	Pull-Down
PU	Pull-Up
PWM	Pulse Width Modulation
R/B	Read / Busy
RAM	Random Access Memory
RE	Read Enable
ROM	Read Only Memory
RTC	Real Time Clock
RTS	Request To Send
RX	Receive
SDR	Single Data rate
SPI	Serial Port Interface
SRAM	Static Random Access Memory
TAP	Test Access Port
TIPB	TI Peripheral Bus
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
ULPD	Ultra Low Power Device
USB	Universal Serial Bus
WE	Write Enable
WP	Write Protect

B. Glossary

International Mobile Telecommunication 2000 (IMT-2000/ITU-2000) Formerly referred to as FPLMTS (Future Public Land-Mobile Telephone System), this is the ITU's specification/family of standards for 3G. This initiative provides a global infrastructure through both satellite and terrestrial systems, for fixed and mobile phone users. The family of standards is a framework comprising a mix/blend of systems providing global roaming. <URL: http://www.imt-2000.org/>