TCS2300 TRITON LITE TOP LEVEL

Errata list

TRITON LITE TOP LEVEL

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Change History

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02/23/07	B. Boukharchouf	P.Perney D. Rouchouse R.Harrando	1.6	Approved	7

1 – Initial version.
2 – WEBS #11 (PG2.2_val) added
3 – WEBS # 9 and WEBS # 14 (PG2.2_val) added
Update of 3- Limited features summary for the car kit function
4 – Webs#14 (PG2.2_val) Auto-start issue on HSPLUG event updated
5 – Webs#17 (PG2.2_val) ACTIVE to SLEEP transition authorized when VBUS is plugged and in no precharge mode
6 – WEBS # 1 (PG2.4 VAL) added (VAC voltage limitation: 10V instead of 20V).
Paragraph 4.2.57 updated (VAC voltage limits: $10V_{RMS}$, $18V_{PEAK}$).
7 – Adding section: 4.2.58 JTAG CLAMP an HIGHZ test mode.

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1 Introduction

That document is intended to cover Triton Lite (TWL3031) Errata.
All the Errata open for Engineering Samples ES1.0 / ES1.1 are Triton items (found on Neptune platform)
For Engineering Samples ES2.0 / ES2.1 / ES2.2 , all the errata are common to Triton / Triton Lite samples.

2 Revision summary

Webs #	Title	ES1.0	ES1.1	ES2.0	ES2.1	ES2.2	ES2.4
4	Register PB_CFG_I2C , bit BUSY = 1 after I2C to PMB xmit (Webs #4)	NOK	NOK	OK			
7	USB/VRPC Block: LVS_USB2IO_AUTO is not set at 1 at reset (Webs #7)	NOK	OK	OK			
9	Voice Wideband and MCLK selection (Webs #9)	NOK	OK	OK			
11	VBUS auto-start (Webs #11)	NOK	OK	OK			
12	VRPLL 1.05V by default instead of 1.3V (Webs #12)	NOK	OK	OK			
13	Backup Battery current charge is not working for code 2 and 3 (Webs #13)	NOK	OK	OK			
16	USB RX latch functionality is not working (Webs #16)	NOK	NOK	OK			
17	Need two i2c read to access to RTC_CTRL_REG (Webs #17)	NOK	NOK	OK			
19	MBATLOW (COMP32) Interrupt not functional when bit SEQ_MSK_BAT_PRE=0 (Webs #19)	NOK	NOK	OK			
20	Precharge from USB is not functional (Webs #20)	TBC	TBC	OK			
21	Unexpected interrupts on INT2 after switch-on (Webs #21)	NOK	NOK	OK			
22	Speaker in Audio-stereo mode (Webs #22)	NOK	NOK	OK			
23	Audio 12KHz (Webs #23)	NOK	NOK	OK			
26	FM radio loop control (Webs #26)	NOK	NOK	OK			
27	Pull-down on ONNOFF pad not enable when ONNOFF is low and VRIO not enable (Webs #27)	NOK	NOK	OK			
32	Leakage on SPKVDD when TRITON is in OFF Mode (Webs #32)	NOK	NOK	OK			
	Voice narrow band master clock decoder not working with master clock 12Mhz or 19.2MHz	NOK	NOK	OK			
28	Speed problem for Extest mode	NOK	NOK	OK			
29	USB supplies issue : Programmable short from VBAT to VBUS	NOK	NOK	OK			
33	Pin CKEN Pull-down control inverted (Webs #33)	NOK	NOK	OK			
	Car kit is not functional.	NOK	NOK	TBC			
37	BCI : ICTLAC1 is not "0" when a Regulated Constant Current charge is applied (Webs #37)	OK	OK	OK			
39	Bit SETUP_DONE reg PMB_CFG_TEST stuck at 0 (Webs #39)	NOK	NOK	OK			
42	Backup battery, end of charge voltage thresholds (Webs #42)	NOK	NOK	OK			
50	LED B and LED C are not functional if LED A is off (Webs #50)	NOK	NOK	OK			
60	No SIM Card detection if card is present	NOK	NOK	OK			

	before battery (Webs #60)						
95	Abnormal VREXTH and VRIO output voltage rising up at power-up of Triton (Webs #95)	NOK	NOK	OK			
65	IDD leakage during Triton Sleep mode (Webs #65)	NOK	NOK	OK			
66	IDD leakage during Triton ON mode (Webs #66)	NOK	NOK	OK			
127	WLEDS Open/short protection issue (Webs #127)	NOK	NOK	OK			
132	WLEDS Stroboscopic visual effect (Webs #132)	NOK	NOK	OK			
136	RTC : read access to clock issue (Webs #136)	NOK	NOK	OK			
RTL 103	USB : Fail to USB 2.0 ECN for pull-up precision (RTL Webs #103)	NOK	NOK	NOK			
(PG2.0) 9	CarKit and Charger Detection: VBUS detection threshold 4.4Volts measured at 4.6Volts (Webs #9 – PG2.0)	-	-	NOK	OK		
(PG2.0) 27	WLEDs driver: residual current when using code 00Hex	-	-	NOK	OK		
(PG2.0) 13	OFF -> Active transition when doing a charger unplug	-	-	NOK	OK		
(PG2.0) 67	I2S right-shift justified format does not work properly	-	-	NOK	OK		
(PG2.0) 38	DP and DM input impedance value lower than the specified one	-	-	NOK	OK		
(PG2.0) 90_Val	Battery Charger detection ITs are generated for pulsed charge with 20-V non-regulated chargers	-	-	NOK	OK		
(PG2.0) 80	WLEDs driver: current peaks on VBAT each 6ms	-	-	NOK	OK		
(PG2.0) 79	Cracking noise on Class-AD output	-	-	NOK	OK		
(PG2.0) 73	Charger unplug detection when TWL3029 is in pre-charge mode	-	-	NOK	OK		
(PG2.0) 81	USB OTG VBUS interrupts	-	-	NOK	OK		
(PG2.1) 16_val	Class A/D TSNR			NOK	OK		
(PG2.2) 5	HSOVMID / AUVMID			OK	NOK	OK	
(PG2.2) 1, 2, 7	HOOK Detection issue			NOK	NOK	OK	
(PG2.2) 1, 2, 7	Headset Plug/Unplug detection issue			NOK	NOK	OK	
(PG2.2) 3	Charger Unplug detection			NOK	NOK	OK	
(PG2.1) 17_val	Leakage current in bias cell of USB module (in sleep mode)			NOK	NOK	OK	
(PG2.1) 52_val	VBUS Plug issue			NOK	NOK	OK	
(PG2.1) 56_val	USB Charge (not functional in some application corners)			NOK	NOK	OK	
(PG2.2) 8_val	Phone Reset with PWON longer than 8.2s (without Battery removal)			NOK	NOK	OK	
(PG2.2) 11_val	Parasitic IT's on USB plug			NOK	NOK	OK	
(PG2.2) 9_val	Triton Lite reset for high dV/dt chargers			NOK	NOK	OK	
(PG2.2) 14_val	Triton Lite switch-ON with HS-plug event			NOK	NOK	OK	

(PG2.2) 17_val	ACTIVE to SLEEP transition authorized when VBUS is plugged and in no pre-charge mode			NOK	NOK	OK	
(PG2.4) 1_Val	VAC max output voltage limitation ($10V_{RMS}$ / $18V_{PEAK}$ instead of 20V)			NOK	NOK	OK with waiver	OK

Note 1: IDD values (Sleep and ON) are in spec – improvement under investigation.

3 Limited features summary

- the CEA-Carkit I/F Limitations are described now described in Triton Lite datasheet – section 9.1

4 Errata description

4.1 Limited features description

4.2 Bugs description

4.2.1 Register PB_CFG_I2C , bit BUSY = 1 after I2C to PMB xmit (Webs #4)

4.2.1.1 Impact

For the PG 1.x, this bit can't be used. No board impact.

4.2.1.2 Description

After a WORDC/WORDD writing, to send an I2C command to PMB , the bit BUSY in PB_CFG_I2C is stuck at 1.
The bit is set and clear at the same time as the bus is free when the request arrived. Priority is set to SET in REL_1.0 and set to CLEAR in PG2.0

4.2.1.3 Workaround

If more than 2 accesses are done, you have to wait 1.2ms between two PMB accesses.

4.2.1.4 Decision status

Fixed for PG2.0

4.2.2 USB/VRPC Block: LVS_USB2IO_AUTO is not set at 1 at reset (Webs #7)

4.2.2.1 Impact

USB peripheral boot of Neptune is not available with Triton transceiver. No board impact.

4.2.2.2 Description

The LVS_USB2IO_AUTO is not set at 1.

4.2.2.3 Workaround

N/A

4.2.2.4 Decision status

Fixed in PG1.1 is done.

4.2.3 Voice Wideband and MCLK selection (Webs #9)

4.2.3.1 Impact

No Wideband AMR possible for the phone. No board impact.

4.2.3.2 Description

For Narrowband, MCLK=13MHz->VFS=8KHz, MCLK=12MHz->VFS=7.44KHz, MCLK=19.2MHz->VFS=14.6KHz
But for Wideband whatever the MCLK, there is no VFS

4.2.3.3 Workaround

N/A

4.2.3.4 Decision status

Temporary fix on PG1.1 : Voice wideband functional on ES1.1.
Final fix done for PG2.0

4.2.4 VBUS auto-start (Webs #11)

4.2.4.1 Impact

Triton automatically switch-on on MB plug when VBUS is floating. Board impact.

4.2.4.2 Description

Triton automatically switch-on on MB plug when VBUS is floating.

4.2.4.3 Workaround

Need to tie VBUS to GND to avoid automatic switch-on

4.2.4.4 Decision status

Fixed in PG1.1

4.2.5 VRPLL 1.05V by default instead of 1.3V (Webs #12)

4.2.5.1 Impact

Maximum frequency of Neptune is not as high as possible. No board impact.

4.2.5.2 Description

VRPLL output voltage is by default 1.05V instead of being 1.3V by default.

4.2.5.3 Workaround

Set VRPLL to 1.3V

4.2.5.4 Decision status

Fixed in PG1.1

4.2.6 Backup Battery current charge is not working for code 2 and 3 (Webs #13)

4.2.6.1 Impact

Back-up battery cannot be charged up to voltages defined by code 2 and 3. No board impact.

4.2.6.2 Description

Code 2 and 3 are not functional (BB charging is not cut when reaching threshold defined in spec).

4.2.6.3 Workaround

Use code 1.

4.2.6.4 Decision status

Fixed in PG1.1

4.2.7 USB RX latch functionality is not working (Webs #16)

4.2.7.1 Impact

Risk of data corruption on RX path. No board impact.

4.2.7.2 Description

The USB RX latch functionality is not working as expected.

4.2.7.3 Workaround

N/A

4.2.7.4 Decision status

Fixed in PG2.0

4.2.8 Need two i2c read to access to RTC_CTRL_REG (Webs #17)

4.2.8.1 Impact

For PG 1.0 and 1.1, two read are needed for reg RTC_CTRL_REG and reg RTC STATUS (this is a bug). No board impact.

4.2.8.2 Description

In RTC block, After a write cycle, to read the exact value on RTC_CTRL_REG, you need to access 2 times to this register. The first read is corrupted.

4.2.8.3 Workaround

For PG 1.0 and 1.1, two read are needed for reg RTC_CTRL_REG and reg RTC STATUS (this is a bug).

4.2.8.4 Decision status

Fixed in PG2.0.

4.2.9 MBATLOW (COMP32) Interrupt not functional when bit SEQ_MSK_BAT_PRE=0 (Webs #19)

4.2.9.1 Impact

Low battery interrupt is not generated if battery presence check is enabled. Battery presence detection is not functional in both OFF2ACTIVE and ACTIVE modes. No board impact.

4.2.9.2 Description

P1_INT2 is not generated when bit SEQ_MSK_BAT_PRE (reg SEQ_CFG_MODE) is set to 0. The test is made with the following sequence :
Set COMP32 resource in ACTIVE (write I2C to PMB command)
Set bits SEQ_MSK_BAT_CMP=0 SEQ_MSK_BAT_PRE=0 in Register SEQ_CFG_MODE
Decrease VBAT voltage down to 2.9V , check P1_INT2 falling

4.2.9.3 Workaround

Same sequence with SEQ_MSK_BAT_PRE=1 is functional (P1_INT2 falling @ VBAT ~ 3V)

4.2.9.4 Decision status

Fixed done for PG2.0.

4.2.10 Precharge from USB is not functional (Webs #20)

4.2.10.1 Impact

USB precharge cannot start.

4.2.10.2 Description

USB Detection is not functional and so the USB Precharge is not starting.

4.2.10.3 Workaround

N/A

4.2.10.4 Decision status

USB precharge is implemented in another way in PG2.0.

4.2.11 Unexpected interrupts on INT2 after switch-on (Webs #21)

4.2.11.1 Impact

Interrupts generated on INT2 with no reason. Board impact.

4.2.11.2 Description

HSDET parasitic interrupts are sent if HSDET is floating

4.2.11.3 Workaround

If Headset plug / unplug detection needs to be used then ensure that HSDET is not floating : disconnect HSDET from HSOL and add a Pull-down of 1 kOhm on HSDET.
If feature is not used then mask interrupt (INT2_P2_STS_B [7]=1).
Note : at reset, interrupts are not masked.

4.2.11.4 Decision status

Hook detect output was inverted in PG1.X leading to inverted behavior : an IT was generated when there is no plug. Design correction is made for PG2.0.

4.2.12 Speaker in Audio-stereo mode (Webs #22)

4.2.12.1 Impact

None (cf work-around). No board impact.

4.2.12.2 Description

In Stereo mode, there is no enable signal to enable the voice input clock coming from the clock generator: then there is no clock at the input of the Voice pll.

4.2.12.3 Workaround

In PG1.0 to set VULON or VDLON at '1'.

4.2.12.4 Decision status

Fix implemented for PG2.0

4.2.13 Audio 12KHz (Webs #23)

4.2.13.1 Impact

All audio mode but the 12kHz sampling frequency one are working. No board impact.

4.2.13.2 Description

12kHz sampling frequency for the audio does not work.

4.2.13.3 Workaround

Use any other sampling frequency when possible

4.2.13.4 Decision status.

Fix done for PG2.0

4.2.14 FM radio loop control (Webs #26)

4.2.14.1 Impact

VULON bit must be ON to use FM radio loop to Headset speaker. No board impact.

4.2.14.2 Description

FM radio loop to Headset speaker does not work if VULON is not ON.

4.2.14.3 Workaround

Set VULON to ON.

4.2.14.4 Decision status

Fixed for PG2.0.

4.2.15 Pull-down on ONNOFF pad not enable when ONNOFF is low and VRIO not enable (Webs #27)

4.2.15.1 Impact

Reset is not done properly. Board impact.

4.2.15.2 Description

Pull-down is controlled by ONNOFF signal , it has to be controlled but not(ONNOFF) signal

4.2.15.3 Workaround

Add 100 kΩ Pull-down on ONOFF to ensure that level is asserted as low when required.

4.2.15.4 Decision status

Fixed in PG2.0

4.2.16 Leakage on SPKVDD when TRITON is in OFF Mode (Webs #32)

4.2.16.1 Impact

Impact from D1 : A leakage around 80uA is measured through SPKVDD when TRITON is in OFF Mode. This leakage disappears when TRITON is switched on in ACTIVE Mode. No board impact.

Impact from D2 : High current flow can be observed external to Triton up to 500mA (through 8 Ohm load). Board impact

4.2.16.2 Description

D1 : Leakage on SPKVDD when Triton is in OFF mode : A leakage around 80uA is measured through SPKVDD when TRITON is in OFF Mode.
This leakage disappears when TRITON is switched on in ACTIVE Mode.

D2 : SPKVDD high leakage current in off mode due to SPKND High and SPKPD Low.

4.2.16.3 Workaround

Workaround for D1 : N/A
Workaround for D2 : Disconnect SPKVDD when not used.

4.2.16.4 Decision status

Fix identified and validated for both D1 and D2 leakage issues for PG2.0.

4.2.17 Voice narrow band master clock decoder not working with master clock 12Mhz or 19.2MHz

4.2.17.1 Impact

No impact for Neptune GSM default mode at 13MHz. No board impact.

4.2.17.2 Description

12MHz or 19.2MHz cannot be used as master clock for voice narrow band.

4.2.17.3 Workaround

N/A

4.2.17.4 Decision status

Support for 12MHz, 19.2MHz and 26MHz for master clock is removed from Triton PRD. Top specification for PG2.0 is updated accordingly.

4.2.18 Speed problem for Extest mode (Webs #28)

4.2.18.1 Impact

Board testing cannot be done at frequency higher than TBD. No board impact.

4.2.18.2 Description

Speed problem for Extest mode.

4.2.18.3 Workaround

Lower speed.

4.2.18.4 Decision status

Fix done for PG2.0.

4.2.19 USB supplies issue : Programmable short from VBAT to VBUS (Webs #29)

4.2.19.1 Impact

Short can occur if VBAT > 4.2V and USB power is supplied by Triton. No board impact.

4.2.19.2 Description

Programmable short VBAT to VBUS if USB power is supplied by Triton (VBUS_VRVUSB=1 in CR_PSM_CTRL (Car kit PSM Control register)).

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4.2.19.3 Workaround

Use Li-ion battery (VBAT < 4.2V).

4.2.19.4 Decision status

Fix done for PG2.0

4.2.20 Pin CKEN Pull-down control inverted (Webs #33)

4.2.20.1 Impact

Depending on power connection of RF device, could generate high power consumption during startup phase. So it is board and RF device dependent. Board impact.

4.2.20.2 Description

Pull-down is controlled by CKEN signal, it has to be controlled by not (CKEN) signal.

4.2.20.3 Workaround

Is board dependent : may require external Pull-down on CKEN.

4.2.20.4 Decision status

Fix done in PG2.0

4.2.21 Car kit is not functional.

4.2.21.1 Impact

Car kit function cannot be used. No board impact.

4.2.21.2 Description

Car kit is not functional.

4.2.21.3 Workaround

N/A

4.2.21.4 Decision status

Mini USB Analog Carkit Interface implemented for PG2.0 (specification CEA-936rAv39 of Nov 24, 2004).

4.2.22 BCI : ICTLAC1 is not "0" when a Regulated Constant Current charge is applied (Webs #37)

4.2.22.1 Impact

False issue. No impact.

4.2.22.2 Description

False issue : measurement problem. This WEBS is rejected.

4.2.22.3 Workaround

N/A

4.2.22.4 Decision status

N/A

4.2.23 Bit SETUP_DONE reg PMB_CFG_TEST stuck at 0 (Webs #39)

4.2.23.1 Impact

In case that default configuration of power management is not used and is re-programmed, a trace of it cannot be kept. No board impact.

4.2.23.2 Description

Cannot change the value of bit SETUP_DONE in register PMB_CFG_TEST. Write 1 to this bit, read always 0.

4.2.23.3 Workaround

N/A

4.2.23.4 Decision status

Fix done for PG2.0.

4.2.24 Backup battery, end of charge voltage thresholds (Webs #42)

4.2.24.1 Impact

Mismatch between specification and measure for backup battery end of charge thresholds. No board impact.

4.2.24.2 Description

Measure100mV mismatch versus specification for Backup battery end of charge voltage thresholds : measurement are 100mV above values in specification.

4.2.24.3 Workaround

N/A

4.2.24.4 Decision status

Fix done for PG2.0 (adjustment of Backup Charger resistor string).

4.2.25 LED B and LED C are not functional if LED A is off (Webs #50)

4.2.25.1 Impact

LED B and LED C are not functional if LED A is off. No board impact.

4.2.25.2 Description

LED B and LED C are not functional if LED A is off.

4.2.25.3 Workaround

Turn on LED A when LED B or LED C is needed.

4.2.25.4 Decision status

Fix done for PG2.0.

4.2.26 No SIM Card detection if card is present before battery (Webs #60)

4.2.26.1 Impact

No IT is generated at Power on. No board impact.

4.2.26.2 Description

No SIM Card detection is done if SIM Card is present before battery. The SIMCD signal is indicating an insertion or extraction of the card. It is not a presence indication.

4.2.26.3 Workaround

SIM Card detection must be done by SW.

4.2.26.4 Decision status

WEBS rejected, issue closed. The SIM Card detection will be better specified in Triton datasheet.

4.2.27 Abnormal VREXTH and VRIO output voltage rising up at power-up of Triton (Webs #95)

4.2.27.1 Impact

Glitch is caused on VRDBB. No board impact.

4.2.27.2 Description

The high dv/dt of the regulator voltage (VRIO, VREXTH, VRABB) when switching on, implies a very high peak current (~1A) pulled on the battery. The peak current and the subsequent battery voltage drop-down are causing a glitch on VRDBB.

4.2.27.3 Workaround

N/A

4.2.27.4 Decision status

Fix done for PG2.0 (current limitation improved for all LDOs).

4.2.28 IDD leakage during Triton Sleep mode (Webs #65)

4.2.28.1 Impact

IDD measured higher than expected in Triton Sleep mode. No board impact.

4.2.28.2 Description

IDD measured is around 2.2mA instead of 270uA target (with VRDBB in OFF mode).

4.2.28.3 Workaround

N/A

4.2.28.4 Decision status

Fix implemented in PG2.0 and new one in PG2.1 :
Idd SLEEP with VRDBB OFF (using software patches) PG2.0: 241 uA
Idd SLEEP with VRDBB OFF (using software patches) PG2.1: 182 uA

4.2.29 IDD leakage during Triton ON mode (Webs #66)

4.2.29.1 Impact

IDD measured higher than expected in Triton ON mode. No board impact.

4.2.29.2 Description

IDD higher than expected in ON mode, with VRDBB in OFF mode and CK13M OFF
IDD measured is around 2.8mA instead of 520uA target.
IDD higher than expected in ON mode, with VRDBB in OFF mode and CK13M ON
IDD measured is around 3.1mA instead of 850uA target.

4.2.29.3 Workaround

N/A

4.2.29.4 Decision status

Fix implemented in PG2.0 and new one in PG2.1 :
Idd ON IDLE (CK13M off) with vrdbb OFF PG2.0 : 590uA
Idd ON IDLE (CK13M off) with vrdbb OFF PG2.1 : 560uA

Idd ON (CK13M on) with vrdbb OFF PG2.0 : 780 uA
Idd ON (CK13M on) with vrdbb OFF PG2.1: 750 uA

4.2.30 WLEDS Open/short protection issue (Webs #127)

4.2.30.1 Impact

Board impact : have an external Zener diode to protect the device.

4.2.30.2 Description

The actual configuration does not allow to protect (as it is recommended) the power transistor of the DCDC of the WLEDs driver since the output can raise up to 30V max (in some very particular cases) and the power NMOS is guaranteed up to 28V. The risk is reliability issue and failure.
Note: the driver's output can raise up to 30V really in very particular cases: it is necessary to have two WLEDs broken in two different legs.

4.2.30.3 Workaround

Have an external Zener diode to protect the device.

4.2.30.4 Decision status

Have an external Zener diode to protect the device.

4.2.31 WLEDS Stroboscopic visual effect (Webs #132)

4.2.31.1 Impact

No board impact. Stroboscopic visual effect on keypad.

4.2.31.2 Description

Low output frequency of WLeds driver of 55.6 Hz induces a stroboscopic visual effect when associated to very thin part of plastic keypad.

4.2.31.3 Workaround

N/A

4.2.31.4 Decision status

Fix done for PG2.0 : implementing a programmable switching frequency allow to switch @ 56-Hz (as before, x1), @ 112-Hz (x2) and @ 168-Hz (x3).

4.2.32 RTC : read access to clock issue (Webs #136)

4.2.32.1 Impact

No board impact. SW impact. Wrong data read at transitions hour : min : sec.

4.2.32.2 Description

Problem with the hour : min : sec that are displayed when doing sequential reading of the clock. For example it can go from 1:59:58 +1sec to 2:00:59.

4.2.32.3 Workaround

SW workaround : either reading the seconds register twice and checking it is consistent, either reading the registers and checking the interrupt status bit to confirm correct.

4.2.32.4 Decision status

Implement SW workaround. No hardware fix implemented for PG2.0.

4.2.33 USB : Fail to USB 2.0 ECN for pull-up precision (RTL Webs #103)

4.2.33.1 Impact

Do not comply to the 5% accuracy for DP / DM pull-up. May fail the USB certification.

4.2.33.2 Description

A USB device is recognized by its pull-up resistor on either DP or DM. This resistor can be implemented two different ways. One solution developed in the USB ECN, is to integrate a variable pull-up resistor which value depends on the status of the USB line. When in suspend / idle data bus state, the

pull-up resistor value is between [900-1575] ohms. When the line is active, the value is between [1425-3090] ohms. A detection of the data bus is made by the differential receiver. Depending on the speed (LS / FS), differential '1' and '0' are encoded as 'J' and 'K'. A two-state asynchronous machine decides if the pull-up resistor should be at a low or high value. By default, it is low. Once a J->K transition is detected, the resistor is high. Nevertheless, if the bus stays longer than 0.5bit time in SE0 state or longer than 7bit time in J state, the resistor should be set back to its low value. So only pull-up range of [900-1575] Ohm is kept for DP / DM for PG2.0 (20% precision).

4.2.33.3 Workaround

N/A

4.2.33.4 Decision status

Only pull-up range of [900-1575] Ohm is kept for DP / DM for PG2.0 (20% precision).
It requires a certification waiver , datasheet is updated accordingly

4.2.34 CarKit and Charger Detection: VBUS detection threshold 4.4V measured at 4.6V (Webs #9 – PG2.0)

4.2.34.1 Impact

Threshold of VBUS detection is specified to 4.4V (max). In the design it is set to 4.6V.

4.2.34.2 Description

To detect a carkit, the protocol used comes directly from the carkit specification CEA_936. A comparator senses VBUS input of the TWL3029 device. If VBUS is higher than 4.4V, VBUSSTS status bit is forced to 1. An INT2 interrupt is generated when the comparator detect the VBUS voltage. If VBUSSTS is forced to 1, a pull-up resistor tie DPLUS pin of the TWL3029 device to high and a comparator senses DMINUS pin of the TWL3029 device. If DMINUS level is high, a comparator senses DPLUS. If both DPLUS and DMINUS levels are high in the same time, a car kit is present. A pull-up resistor tie DMINUS to high and the status bit CARKITSTS is forced to 1. In the current implementation, the threshold for VBUS detection has been set to 4.6V instead than 4.4V.

4.2.34.3 Workaround

N/A

4.2.34.4 Decision status

Fix implemented in PG2.1.

4.2.35 WLEDs driver: residual current when using code 00Hex (Webs #27 – PG2.0)

4.2.35.1 Impact

Residual backlight is present when a WLEDs series is driven with a 0 current level (00Hex code) and one other leg (with the same number of WLEDs, or more) is driven with a non-0 current level.

4.2.35.2 Description

A residual current is present in WLEDs legs when a leg is driven with a 0 current level (code 00Hex) and another leg (with the same or more WLEDs) is driven with a non-0 current level. This problem induces an unwanted residual backlight in these conditions. This issue is confirmed by the design team. No issue when all the legs are driven with 0 current level (or when a leg with less WLEDs is driven).

4.2.35.3 Workaround

N/A

4.2.35.4 Decision status

Fix implemented in PG2.1. This fix allows to reduce of a factor 100 the residual current.

4.2.36 Triton OFF -> ACTIVE transition if ADCIN5 resistance disconnected and charger unplugged

4.2.36.1 Impact

No impact for the application.

4.2.36.2 Description

If we unplug the charger with no main battery and a backup battery present, we will discharge the node VBAT. When VBAT is discharged, we will switch in backup mode and reset the power state machine, the start sequence will be stopped. Thus, we cannot discharge the backup battery with this issue.

4.2.36.3 Workaround

N/A

4.2.36.4 Decision status

No fix in PG2.1 (since there is no impact for the application).

4.2.37 I2S right-shift justified format does not work properly (WEBS PG2.0 SI_67)

4.2.37.1 Impact

PG1.X: I2S Right justify NOT implemented
PG2.0: I2S Right justify implemented but NOT functional. Only Left-shift justified will be available.
PG2.1: I2S Right justify implemented and functional.

4.2.37.2 Description

Serial2Parallel conversion does not work properly in I2S right-shift justified mode.

4.2.37.3 Workaround

Software workaround is NOT possible since RIGHT channel cannot be corrected with software fix (only LEFT channel is corrected)

4.2.37.4 Decision status

HW fix implemented in PG2.1.

4.2.38 DP and DM input impedance value lower than the specified one

4.2.38.1 Impact

DP / DM input impedances are not in specification.

4.2.38.2 Description

The audio carkit module connects a resistor between the DP / DM lines to the VMID signal. When measurements are performed, the audio section is powered down and VMID is tied to ground causing a leakage current which modifies the values of the impedances.

4.2.38.3 Workaround

N/A.

4.2.38.4 Decision status

HW fix in PG2.1.

4.2.39 Battery Charger Detection ITs generated for pulsed charge with 20-V non-regulated chargers

4.2.39.1 Impact

Parasitic ITs are generated when charging (PWM charge) the battery with 20-V non-regulated chargers.

4.2.39.2 Description

During the PWM charge of the battery through a 20-V non-regulated charger, parasitic ITs are generated (Battery charger detection IT).

4.2.39.3 Workaround

SW workaround has been identified. Battery charger detection IT must be masked and the detection of a charger un-plug must be done by monitoring CHGSTS bit (STS_HW_CONDITION register) during the off-phase of the PWM.

4.2.39.4 Decision status

No HW fix in PG2.1 (SW workaround).

4.2.40 WLEDs driver: current peaks on VBAT each 6ms (refresh time)

4.2.40.1 Impact

Current peaks (@ 1.2-1.5A in PG2.0) are generated on VBAT by the WLEDs driver at the beginning of each refresh period.

4.2.40.2 Description

At the beginning of each refresh period, the WLEDs DCDC must change its regulated voltage. This causes an increase of the current drawn from the battery. Thus, each 6ms (refresh period), we have a current peak close to 1.2-1.5A on VBAT.

4.2.40.3 Workaround

Capacitor between pins LED_A and LED_B and between LED_B and LED_C can be added to strongly reduce these peaks.

4.2.40.4 Decision status

HW fix in PG2.1. Current limiting resistor has been increased to limit the peaks @ 390mA (soldered samples, typical conditions, V_{BAT} = 3.6V).
Samples anyway are characterized on socket: socket resistor limits the value of the current peaks, so that there is a delta (110mA, with a socket resistor of 100mOhm) between (1) current peaks when measuring samples on socket and (2) current peaks in soldered samples.
Current peaks measured on socket shows a typical value @ 280mA and a max value @ 350mA (all corner lots tested @ -40, 27, 95 deg): this drives to a max value of 460mA in soldered samples. Anyway, current peaks in soldered samples cannot be measured in production test: thus, max current in soldered samples is guaranteed by design. Table below summarizes specifications and test conditions.

Parameter	Test Conditions	Min	Typ	Max
Current peaks (mA)	Measurements done on socket (1) with R_S > 100 mΩ		280	350
	Operational conditions, VBAT = 3.6V (soldered sample)		390	460

Note: (1) the resistance of the socket (RS) introduces a constant current peak reduction compared to the operational case (soldered sample)

4.2.41 Cracking noise on Class-AD output (when using Voice path and comfort noise data @ VSP input)

4.2.41.1 Impact

Audible cracking sound effect is present on Class-AD during Handsfree communication. This noise is present when using the Voice path and the comfort noise data at VSP input.

4.2.41.2 Description

Audible cracking sound effect is present on Class-AD during Handsfree communication. This noise is present when using the Voice path and the comfort noise data at VSP input. Conditions used to reproduce the issue are: (1) small data on VSP interface input (equivalent to comfort noise), (2) Class-AD gain set to 8.5dB.

4.2.41.3 Workaround

N/A.

4.2.41.4 Decision status

HW fix in PG2.1.

4.2.42 Charger unplug detection when the device is in pre-charge mode

4.2.42.1 Impact

Charger unplug not detected when the device is in pre-charge mode.

4.2.42.2 Description

When the device is in pre-charge mode (2.0V<VBAT<3.2V), if the charger is unplugged, it looks like the pre-charge is still on-going.

4.2.42.3 Workaround

N/A.

4.2.42.4 Decision status

HW fix in PG2.1.

4.2.43 USB OTG VBUS interrupts

4.2.43.1 Impact

Added logic to filter useless IT’s causes a bad functioning of VB_SESS_END interrupt.

4.2.43.2 Description

Added logic to filter useless IT’s causes a bad functioning of VB_SESS_END interrupt. Logic must be simplified in order to get the correct behavior of the USB module.

4.2.43.3 Workaround

N/A.

4.2.43.4 Decision status

HW fix in PG2.1.

4.2.44 CLASS A/D TSNR

4.2.44.1 Impact

Class A/D TSNR performances are marginal versus specification

4.2.44.2 Description

Measurements done on typical lot with application schematic without 2 external capacitors (see specification *16_01_02_bls_0003_audio_PG2*) are too close to specification for production (see below).

Psophometric TSNR (Harmonic Distortion + SNR)	3 dBm0 (Maximum Digital Code)	35
1 kHz Tone	0 dBm0	50
Measured at: SPKP-SPKN @2.5dB, Load = 8 Ω, L = 22 uH	-10 dBm0	56
	-20 dBm0	47
	-30 dBm0	37
	-40 dBm0	27
	-50 dBm0	17

4.2.44.3 Workaround

Added to 2 external capacitors of 220nF will let reach the above performances.

4.2.44.4 Decision status

N/A

4.2.45 HSOVMID / AUVMID

4.2.45.1 Impact

A drop is observed in the Audio VMID voltage due to a parasitic leakage

- from 1.50V down to 1.34V (VMIDSEL= ‘1’)
- from 1.35V down to 1.26V (VMIDSEL= ‘0’)

which limits the linearity of the Audio section for high-level signals.

4.2.45.2 Description

The leakage current is caused by a parasitic diode between VMID and VRUSB (when VRUSB is Off)

4.2.45.3 Workaround

SW Workaround needed (Turn VRUSB and VRVBUS On when Audio is On) and regulator external schematic implemented. Possible reduction of USB features.

4.2.45.4 Decision status

HW fix in PG2.2

4.2.46 HOOK Detection issue

4.2.46.1 Impact

Hook detection function does not work in PG2.1.

4.2.46.2 Description

Multiple interrupts are generated by the debouncing logic every 8ms (due to a reset problem of the debouncer).

4.2.46.3 Workaround

No SW workaround possible in PG2.1

4.2.46.4 Decision status

HW fix in PG2.2 concerning the internal digital logic: the implemented modification will allow not generating parasitic interrupts as in PG2.1. Only plug event will generate an interrupt. Using specified RC filter (R= 330Ω, C= 10uF) at HSMICBIAS regulator output will allow external analog debouncing (10ms).
Nevertheless, the analog detection system (which drives the digital logic) can generate a parasitic interrupt both on for the plug and the unplug event depending on the slope of the current variation (which is function of the employed button) used to detect the plug event.
To get rid of this sensibility to the used button a SW debouncing is needed. A Hook detection status bit has been added to allow an additional SW debouncing (in case a higher debouncing is required).
Register: **POPTEST1** (address: 234, page: 0)
Bit number: 1 (Meaning: '1'->hook button switched off, '0'->hook button switched on)
Implementation of the SW debouncing is on-going.

4.2.47 Headset Plug/Unplug Detection issue

4.2.47.1 Impact

Headset plug/unplug detection function does not work in PG2.1.

4.2.47.2 Description

Multiple interrupts are generated by the debouncing logic every 8ms (due to a reset problem of the debouncer).

4.2.47.3 Workaround

No SW workaround possible in PG2.1

4.2.47.4 Decision status

HW fix in PG2.2. Internal debouncing counter bug will be fixed: thus, a digital debouncing of 8ms will be available in PG2.2. An additional RC filter (nice-to-have) between Headset output and Hsdet input can be added to have an analog debouncing (in case a higher-than-8ms debouncing is required).
A headset plug/unplug detect status bit has been added to allow an additional SW debouncing (in case a higher-than-8ms debouncing is required).
Register: **POPTEST1** (address: 234, page: 0)
Bit number: 0 (Meaning: '1'->HS unplug, '0'->HS plug)

4.2.48 Charger Unplug Detection issue

4.2.48.1 Impact

No detection of Charger removal during charge (for VBAT higher than 4.2V)

4.2.48.2 Description

The trig level is sensitive to the Battery level. It is ok for up to 4.2V Battery (room temp)

4.2.48.3 Workaround

N/A

4.2.48.4 Decision status

HW fix in PG2.2

4.2.49 Leakage current in bias cell of USB module (in sleep mode)

4.2.49.1 Impact

Leakage current in bias cell of the USB module (in sleep mode only)

4.2.49.2 Description

Leakage current in bias cell of the USB module due to a floating node

4.2.49.3 Workaround

SW patch (already used in PG2.0)

4.2.49.4 Decision status

No HW fix in PG2.2

4.2.50 VBUS Plug issue

4.2.50.1 Impact

Platform won't switch on first USB plug with a VBUS lower than 4.4 V and if platform have never been in ACTIV state before.

4.2.50.2 Description

VBUS need to be plugged twice (only in test boards) in order to be detected if capacitor on PM_D IO is higher than 25 pF.

4.2.50.3 Workaround

1) No load higher than 25 pF on PM_D .

4.2.50.4 Decision status

No design modification as PMB is not externally used on platform and PM_D IO max load of 25 pF will be added in datasheet

4.2.51 USB Charge (not functional in some application corners)

4.2.51.1 Impact

In some application corners, if VBUS voltage is lower than the threshold of the comparator, a false VBUS unplug is detected. Consequently, battery is not charged.

4.2.51.2 Description

VBUS voltage is specified at 4.4V, while the VBUS comparator used by the SW patch is specified in the range [4.4-4.8V]. When VBUS voltage is lower than the threshold of the comparator, a false VBUS unplug is detected. Consequently, battery is not charged.

4.2.51.3 Workaround

The VBUS unplug can be detected during the battery charge by making regular VBUS measurements via MADC (Note: SW patch successfully validated on EMI-Conso board)

4.2.51.4 Decision status

No HW modification will be done in PG2.2. Problem solved by SW patch.

4.2.52 Phone Reset with PWON longer than 8.2s (without Battery removal)

4.2.52.1 Impact

Phone reset (RTC content erased) without main battery removal.

4.2.52.2 Description

To reset Triton state machine, the specified procedure is to press the power-on key more than 8.2s, then remove the main battery (then, a low level reset, reset_por, is generated).

On current Triton version, to reset Triton state machine, the procedure is to press the power-on key more than 8.2s (then, a low level reset, reset_por, is generated).

Reset Triton state machine will erase RTC registers and provide a global reset (reset_por).

4.2.52.3 Workaround

N/A

4.2.52.4 Decision status

No HW fix necessary, just a datasheet update.

4.2.53 Parasitic IT's on USB plug

4.2.53.1 Impact

Parasitic IT's at USB plug/unplug.

4.2.53.2 Description

Bouncing effect observed at USB plug/unplug events (all the 3 different ways to generate the IT have been tested: [1] real USB cable, [2] external DC source for VBUS, [3] ID_USB pin shorted to ground).

4.2.53.3 Workaround

S/W workaround possible (under implementation).

4.2.53.4 Decision status

No HW fix necessary.

4.2.54 Triton Lite reset for high dV/dt chargers

4.2.54.1 Impact

Triton Lite is reset when using high dV/dt (> 5V/us) chargers.

4.2.54.2 Description

A high voltage step on VAC pin turns on the ESD protection of this I/O and causes Triton reset (due to current injection in the IC substrate).

4.2.54.3 Workaround

Define a dV/dt Max in the datasheet (BCI section 10.13).

4.2.54.4 Decision status

No HW fix necessary.

4.2.55 Triton Lite switch-ON with HS-plug event

4.2.55.1 Impact

Triton Lite is switched-ON through a HS-plug event.

4.2.55.2 Description

Triton Lite is switched-ON by a HS-plug event due to current injection in the IC substrate. This current is injected by the external 22uF capacitor connecting HSOL I/O to HSDET I/O. This current generates a glitch on ID_USB I/O (high-to-low), which is interpreted as a normal switch-on condition.

4.2.55.3 Workaround

Adding a 10nF-capacitor between ID_USB and ground solves the issue (no more auto-start).

4.2.55.4 Decision status

No HW fix necessary.

4.2.56 ACTIVE to SLEEP transition authorized when VBUS is plugged and in no precharge mode

4.2.56.1 Impact

Triton Lite can go in sleep mode when a VBUS is present and Triton Lite is not in precharge mode (even if a VBUS plug presence is a wakeup condition)

4.2.56.2 Description

In Triton Lite sleep mode , 32kHZ of BCI is stopped therefore BCI watchdog is stopped and no interrupt from BCI can be generated

4.2.56.3 Workaround

Two possible workarounds :
- either : prevent the Triton lite to go in deep sleep during USB charge (in SW sleep manager)
- or : enable BCI CK32K clock when Triton Lite is in USB charge mode (BIT3=1 inTESTUNLOCK register)

4.2.56.4 Decision status

No HW fix necessary.

4.2.57 VAC max output voltage limitation ($10V_{RMS}$ / $18V_{PEAK}$ instead of 20V)

4.2.57.1 Impact

VAC voltage must be limited up to $10V_{RMS}$ and $18V_{PEAK}$.

If VAC voltage is higher than the limits reported in the previous lines, the VGS stress of an internal switch (PMOS transistor) is not acceptable. This stress could damage the gate oxide of this transistor (GOI is granted for 50sec for VAC @ 20V, 8 years for VAC @ $10V_{RMS}$ and VAC_{PEAK} < 18V with 100 ppm). Vt drift is negligible when VAC is limited up to $10V_{RMS}$ and $18V_{PEAK}$.
The first consequence is that VAC level is not measurable after the switch gets damaged and then is no more possible to charge the battery.

4.2.57.2 Description

When using chargers that do not respect the previously listed conditions, the PMOS switch enabling the measurement of VAC level through the embedded M-ADC gets stressed. This can damage the gate-oxide of the PMOS switch and in any case causes a large drift of the Vt voltage of this transistor.

4.2.57.3 Workaround

Limit VAC up to $10V_{RMS}$ and $18V_{PEAK}$ (this guarantees a good GOI, and a negligible Vt drift).

4.2.57.4 Decision status

HW fix in PG2.4

4.2.58 JTAG CLAMP and HIGHZ test mode

4.2.58.1 Impact:

After setting JTAG in CLAMP or HIGHZ mode, the boundary chain doesn't toggle even if data is shifted through TDI.

4.2.58.2 Description:

When CLAMP mode is set, data already loaded in boundary scan is applied to outputs, and Bypass register is connected between TDI & TDO (normal behavior).
When shifting, data go also to boundary scan as well as Bypass register, and if we do an updated the value of output pads will change according to the new content of boundary scan.
This is in contradiction whit the IEEE JTAG standard.

4.2.58.3 Workaround

N/A

4.2.58.4 Decision status

No HW fix necessary.