Technical Note

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US export control classification changed.				

0.3 References, Abbreviations, Terms

Table of Contents

1 Introduction

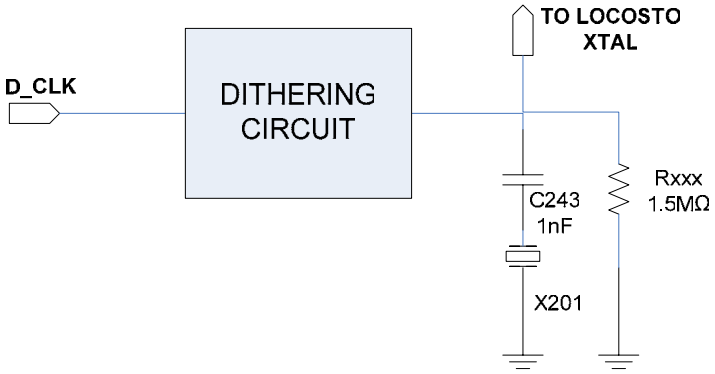
This document describes the concept for FREF dithering that is the solution being proposed for improving Max RMS phase error at DCS1800 and PCS1900 integer channels (Note: In this document integer channels means channels which coincide with harmonics of 13 MHz)

A proposed dithering circuit and guidelines for simulation, tuning and implementation is given.

1.1 HW Overview

The basic idea is to inject a non-synchronous signal referred to as *dithering signal* of relatively small amplitude with respect to reference FREF signal into XTAL input pin. The dithering signal is generated by taking a digital level signal (**D_CLK**) through the *dithering circuit*, which is a filtering network.

D_CLK is a 3.25 MHz square wave with an amplitude of nominal 1.8V. It is only active during TX slots, and only when transmitting on integer channels.



Band	Integer Channel #	Frequency [MHz]
DCS1800	541	1716
	606	1729
	671	1742
	736	1755
	801	1768
	866	1781
PCS1900	556	1859
	621	1872
	686	1885
	751	1898

Figure 1. Block diagram for dithering implementation, and the relevant integer channels.

1.2 SW Overview

The document also describes the SW changes needed to implement *dithering.* There are three possibilities for D_CLK sources in order to allow implementation with minimum impact to existing GPIO selection.

This document describes SW settings for the three different Locosto outputs

- ND_nWP
- GPIO_17
- LCD_nRST).

The SW description is to be used from SW 5.13/12.8 release using DRP data script (version 136.02 or newer).

2 HW implementation.

2.1 D_CLK Generation

D_CLK is generated under DRP software control. D_CLK is only active when transmitting on integer channels.

D_CLK is a clock signal with 50% duty cycle and a frequency of 3.25 MHz (*dithering frequency*)

D_CLK is routed to one of the possible D_CLK pins dependent of the SW settings described in section 3.1.2.

2.2 Dithering Circuit

This circuit must filter D_CLK, reduce the amplitude and couple the dithering signal into the DCXO (Locosto XTAL pin)

2.2.1 Requirements

The DCXO circuit is by nature very sensitive and the dithering circuit should not result in excessive loading of the crystal. From DCXO simulations it has been determined that the total load from the additional dithering circuit should not exceed a parallel equivalent of 0.6pF // 200 kΩ including PCB trace and pad capacitance.

The strength of the dithering is determined by measuring the dithering sidebands at ±3.25 MHz from the 13 MHz system clock output from Locosto (**CKOUT_13MHZ**). Optimum result is obtained at a sideband level of -46 dBc ±3 dB. From experiments and simulation it has been found that the gain of the dithering circuit at 3.25 MHz (DGAIN) should be -38 ±3 dB.

The bandwidth of the dithering circuit must be low enough to prevent overshoot and ringing of **D_CLK** from affecting the dithering. From experiments and simulation it has been determined that the gain of the dithering circuit at 9.75 MHz (HGAIN) should be -48 ±3 dB.

2.2.2 Implementation

The proposed dithering circuit is shown on Figure 2. This circuit conforms to all known requirements, and gives an acceptable performance (measured on I-sample, the Locosto RDP)

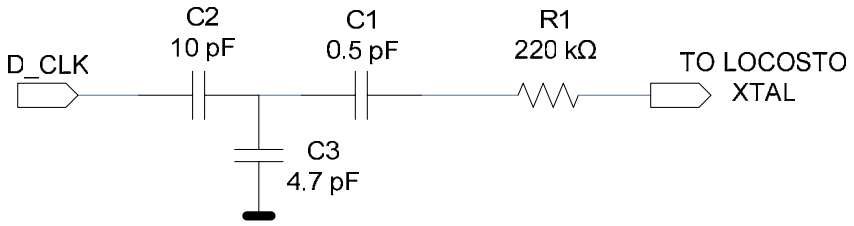


Figure 2. Proposed dithering circuit

On some platforms good results have been obtained with C2 removed. In this case D_CLK is not voltage divided by the capacitors C2 and C3, and R1 should be increased to keep the level of dithering signal on the same level as the proposed circuit on Figure 2.

2.2.3 Simulating XTAL load.

When simulating/calculating the additional XTAL load by the dithering circuit the stray capacitance generated by PCB traces and component pads is very important. In this document we are assuming that all routing is done one the top layer and that GND is separated from top layer by 65um or 130um. Requirement for the load is less than 220kΩ//0.6pF (parallel equivalent circuit).

Stray capacitance is calculated as shown in Appendix B.

A "typical" placement and layout is shown on Figure 3. Component pads are 0.5x0.5mm. Track width is 0.1 mm. Trace from the top of C1 to the XTAL node is assumed to be 1mm long.

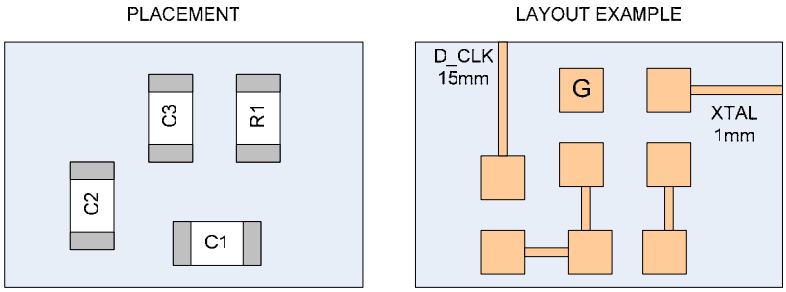


Figure 3. Placement and layout example sketch

The worst case load on the XTAL node is simulated with the circuit shown in Figure 4. Stray capacitance is calculated with SCN being stray capacitance normalized to 1 mm^2. Areas (in mm^2) are estimated from the layout example above. As an example the first node is one pad (0.25 mm^2) and one trace (0.1 mm^2) and the stray capacitance on this node is therefore 0.35 * SCN (C103). In fact C103 at the port 1 node is the most important stray capacitance. Only minimal influence comes from C101 and C102.

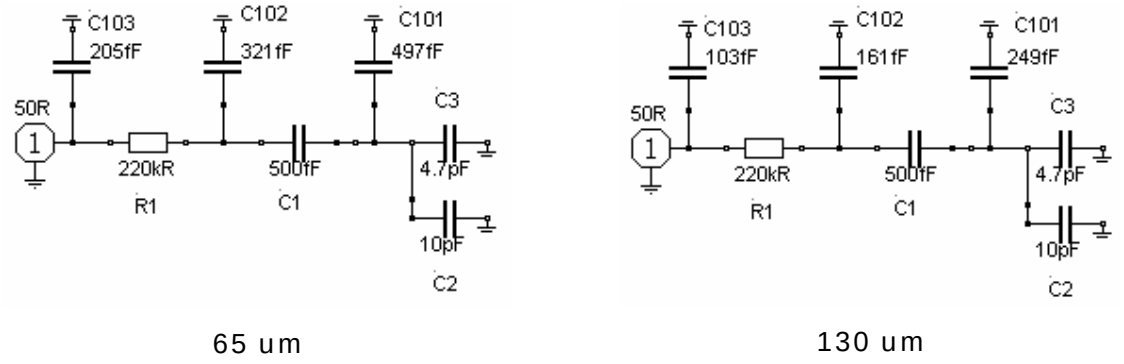


Figure 4. Simulation circuits for calculating circuit load on XTAL node

During simulations the load impedance seen on port 1 (XTAL node) is converted to a parallel RC equivalent circuit. Calculation of component values is done at 26 MHz.

With 65um distance between traces and GND – RC parallel equivalent is 220kΩ//0.206pF

With 130um distance between traces and GND – RC parallel equivalent is 220kΩ//0.104pF

In both cases the load is within the 200kΩ//0.6pF requirement. If R1 and C1 is swapped the RC parallel equivalent becomes 595kΩ//0.4 pF (65um).

2.2.4 Gain Simulations.

The transfer function of the dithering circuit is also simulated. For this purpose a simple equivalent of the 26 MHz crystal is used. A 12 pF capacitor represents the total load from the DCXO including stray capacitance of the DCXO / XTAL circuit. Also on Locosto PG 2.0 a 1.5 MΩ resistor is mounted to secure oscillator start-up. This is modelled by the input resistance of a buffer with unity gain and low output resistance. Stray capacitance of the dithering circuit is modelled with three discrete capacitors. When looking at the gain only it is clear that only the stray capacitance between R1 and C1 affects the gain since the other stray capacitance is parallel to actual circuit capacitors.

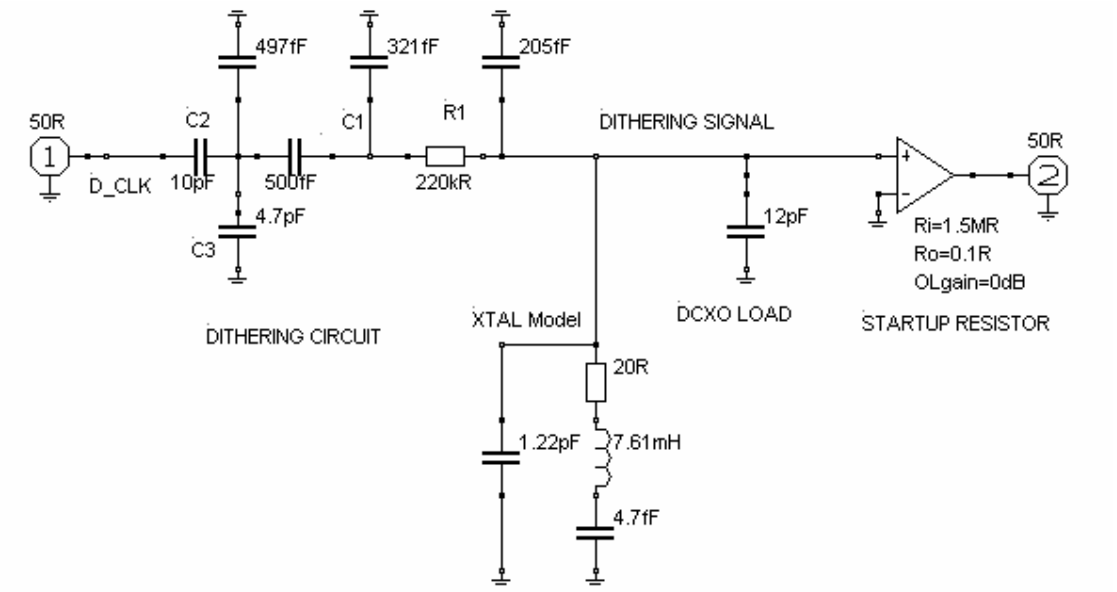


Figure 5. Circuit for simulating the gain of the dithering circuit.

By testing a number of different circuits and component values, and simulating the same circuits using an approach as described above it has been found that the sideband level is correlated with the simulated gain at 3.25 MHz (*DGAIN*) and that performance is also linked with gain at 9.75 MHz (*HGAIN*). Therefore we recommend that a simulation values for any dithering circuit should be :

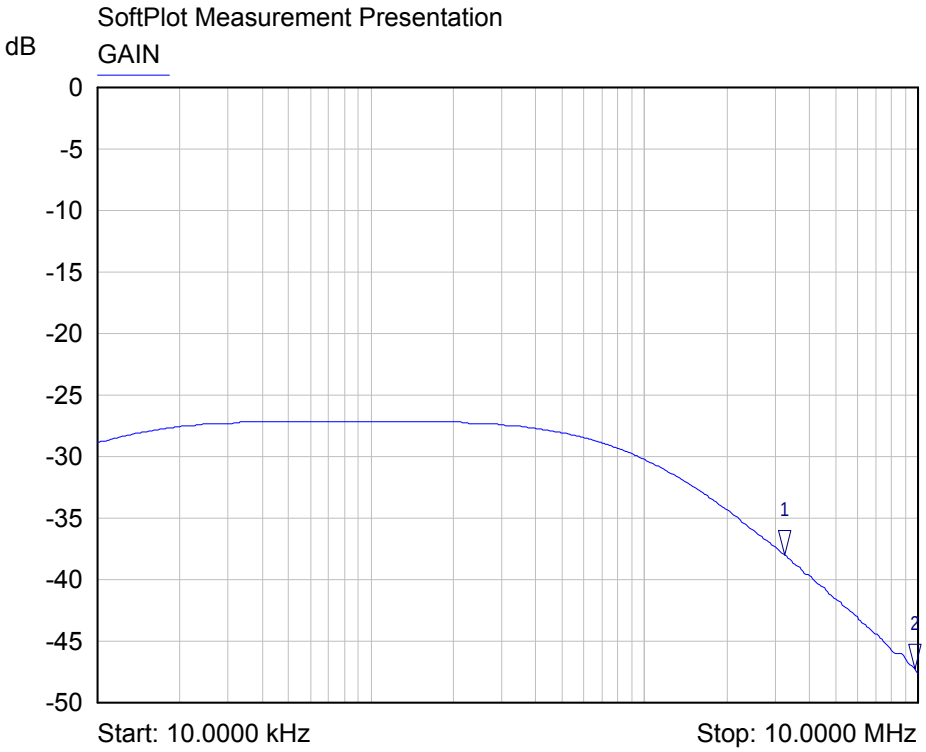
DGAIN **-38 ±3 dB @ 3.25 MHz** – corresponding to a Sideband level of approx. -46 ±3 dBc

In appendix A the sideband level vs. simulated DGAIN is shown for various dithering circuits.

HGAIN **-48 ±3 dB @ 9.75 MHz**

Note that the above statement does not state that circuits outside these values can't have good performance, but merely that all circuits tested that are within the above simulation limits have adequate performance.

Results of the gain simulation for the proposed dithering circuit can be seen on Figure 6.



Mkr	Trace	X-Axis	Value	Notes
1 ▽	GAIN	3.2500 MHz	-38.06 dB	DGAIN
2 ▽	GAIN	9.7269 MHz	-47.23 dB	HGAIN

Figure 6. Gain simulation for the proposed dithering circuit.

2.2.5 Circuit Validation and Tuning

When measuring the performance of the dithering the primary interest will be the phase error performance on the integer channels. However as part of the design validation the sideband levels caused by dithering needs to be verified, and if outside the recommended level range the component values of the dithering circuit need to be tuned.

The sideband level is measured on (**CKOUT_13MHZ**). When taking measurements used in this document a small attenuator and DC-block circuit was used in order not to overload the Locosto output.

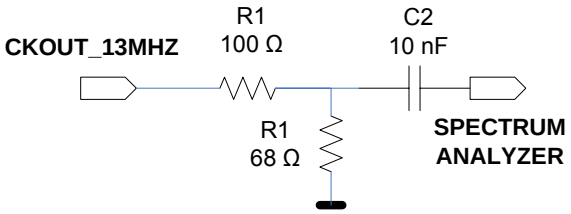
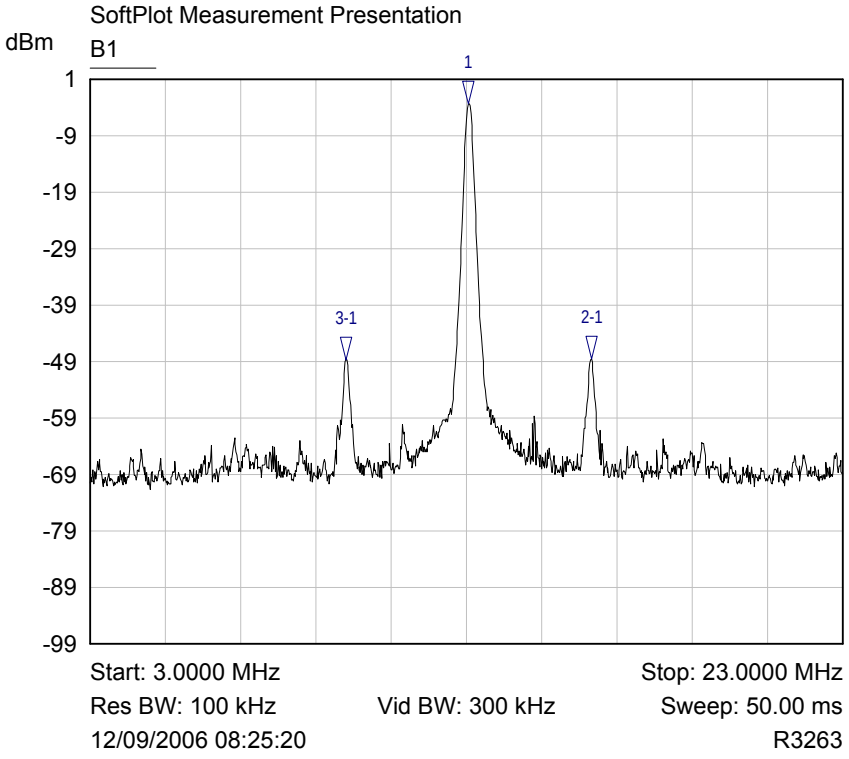


Figure 7. Simple circuit for measuring dithering sidebands.

Since the dithering signal is only active when transmitting on integer channels it is necessary to setup a call with the traffic channel set to an integer channel, and to set the spectrum analyzer to "max hold".

On Figure 8 results for the proposed dithering circuit is shown. As it can be seen the sideband level is −45.5 dBc. From the DGAIN simulation value of -38.1 dB the expected value was around -46.1 dBc. (see Appendix A, page 17)



Mkr	Trace	X-Axis	Value	Notes
1 ▽	B1	13.0600 MHz	-3.27 dBm	
2-1 ▽	B1	3.2600 MHz	-45.30 dB	
3-1 ▽	B1	-3.2600 MHz	-45.47 dB	

Figure 8. Dithering sideband level measured with proposed dithering circuit.

2.3 Layout Recommendations

As mentioned the stray capacitance of the dithering circuit layout is critical for circuit performance, and as any circuit connected to the reference crystal oscillator noise should be kept low. See example on Figure 3.

- To avoid noise from PCB lines coupling into the dithering network the layout should be as compact as possible and should have a ground plane under the dithering circuit. The distance between component layer and ground plane should as a general guideline be as high as possible, but it is not recommended to route any signal or supply lines between the dithering circuit and its ground plane.
- Traces from XTAL node to R1 should be kept as short as possible to reduce the stray capacitance. If possible the ground planes could be removed (cut-out) from the layers closest to the top layer under the trace and the R1 pad closest to the XTAL. For the rest of the dithering circuit it is recommended to keep traces as short as possible in order to minimize noise pickup.
- When routing D_CLK from Locosto to the dithering circuit the line should be as short as possible, and should be kept well away from the TX matching circuits to avoid D_CLK harmonics and sidebands on the TX signal.

3 SW implementation

This section will explain the needed SW changed to enable dithering for ND_nWP configuration in 5.13/12.8 release using the latest DRP data script.

In order to understand the changes required for the customization for pin other than ND_nWP, this section gives examples of switch from ND_nWP to GPIO_17 and ND_nWP to LCD_nRST.

The section incorporates information about files to be changed along with the changes required and the procedure for testing dithering.

3.1 Files Changes

3.1.1 Files Modified

Following EIGHT files have been modified. Please find the files in the SW release.

- init.c

path=chipsetsw\system\init_common or \csw-system\init_common

- armio.c

path=chipsetsw\drivers\drv_core\armio\ or \csw-system\drv_core\armio

- camcore_api.c

path=chipsetsw\drivers\drv_app\camd\camcore\ or \csw-system\drv_app\camd\camcore

- l1_init.c

path=chipsetsw\layer1\cfile\ or \L1\layer1\cfile. This one did not exist in N5.12/N12.7

- drp_defines.h

path=chipsetsw\layer1\drp\ or \L1\layer1\drp

- drp_script_data.c

path=chipsetsw\layer1\drp\ or \L1\layer1\drp

- drp_api.h

path=chipsetsw\layer1\drp\ or \L1\layer1\drp

- tpudrv61.h

path=chipsetsw\layer1\tpu_drivers\source1 or \chipsetsw\layer1\tpu_drivers\source1

Please merge all the files to the above defined locations in the 5.13/12.8 release.

3.1.2 Modifications Required

Changes independent of pin:

The below changes are already taken care off in the reference SW.

File Names	Line Number	Actions
Armio.c	670	Comment the line given below. CONF_LOCOSTO_DEBUG = 0x02;
Drp_defines.h	32	#define DRP_SILICON_1P1 0 #define DRP_SILICON_1P2 1

Drp_script_data.c		Replace the file with the one given in the SW release
Tpudrv61.h		Replace the file with the one given in the SW release

For ND_nWP :

By default, ND_nWP configuration is active. Hence, no changes are required for ND_nWP to make it active. But to change the configuration, ND_nWP changes needs to be understood. Following changes have been made to enable dithering using ND_nWP.

File Names	Line Number	Actions
Init.c	1917 and 1929	Comment the two lines given below. CONF_ND_NWP = MUX_CFG(0, PULLOFF); CONF_ND_NWP = MUX_CFG(2, PULLOFF);
Camcore_api.c	319	change line CONF_ND_NWP &= ((~0x3) | 0x02); to CONF_ND_NWP &= ((~0x3) | 0x03);
L1_init.c	1584	Add the following code. #if (L1_DRP_DITHERING == 1) (*(volatile UINT8 *)CONF_LOCOSTO_DEBUG) = 0x00; (*(volatile UINT8 *)CONF_MUX_VIEW28) = 0x01; (*(volatile UINT8 *)CONF_DEBUG_SEL_TST_28) = 0x07; (*(volatile UINT8 *)CONF_ND_NWP) = 0x03; #endif
Drp_api.h	71	Add the following lines. #define L1_DRP_DITHERING 1 //MUX defines for enabling TSTCLK0 on ND_nWP #define CONF_MUX_VIEW28 0xFFFE926D #define CONF_DEBUG_SEL_TST_28 0xFFFE921C #define CONF_ND_NWP 0xFFFEF184 #define CONF_LOCOSTO_DEBUG 0xFFFEF020

For GPIO_17:

By default, ND_nWP configuration is active. Hence, first undo all the changes mentioned above under ND_nWP configuration. Now, make the following changes for enabling dithering using GPIO_17:

File Names	Line Number	Actions
Init.c	1894	Comment the line given below. CONF_GPIO_17= MUX_CFG(0, PULLOFF);
L1_init.c	1584	Add the following code. #if (L1_DRP_DITHERING == 1) (*(volatile UINT8 *)CONF_MUX_VIEW8) = 0x01; (*(volatile UINT8 *)CONF_DEBUG_SEL_TST_8) = 0x07; (*(volatile UINT8 *)CONF_GPIO_17) = 0x02; (*(volatile UINT8 *)CONF_LOCOSTO_DEBUG) = 0x00; #endif
Drp_api.h	71	Add the following lines. #define L1_DRP_DITHERING 1 //MUX defines for enabling TSTCLK0 on GPIO_17 #define CONF_GPIO_17 0xFFFEF156 #define CONF_MUX_VIEW8 0xFFFE9259 #define CONF_DEBUG_SEL_TST_8 0xFFFE9208 #define CONF_LOCOSTO_DEBUG 0xFFFEF020

For LCD_nRST:

By default, ND_nWP configuration is active. Hence, first undo all the changes mentioned above under ND_nWP configuration. Now, make the following changes for enabling dithering using LCD_nRST

File Names	Line Number	Actions
Init.c	1789	Comment the line given below. CONF_LCD_NRST = MUX_CFG(0, PULLOFF);

L1_init.c	1584	Add the following code. #if (L1_DRP_DITHERING == 1) (*(volatile UINT8 *)CONF_MUX_VIEW12) = 0x01; (*(volatile UINT8 *)CONF_DEBUG_SEL_TST_12) = 0x06; (*(volatile UINT8 *)CONF_LCD_NRST) = 0x01; (*(volatile UINT8 *)CONF_LOCOSTO_DEBUG) = 0x00; #endif
Drp_api.h	71	Add the following lines. #define L1_DRP_DITHERING 1 //MUX defines for enabling TSTCLK0 on GPIO_17 #define CONF_MUX_VIEW12 0xFFFE925D #define CONF_LCD_NRST 0xFFFEF14E #define CONF_DEBUG_SEL_TST_12 0xFFFE920C #define CONF_LOCOSTO_DEBUG 0xFFFEF020

3.2 Hardware and Software Requirements

Testing environment needs the following:

Hardware: I-Sample 2.5 including Visu daughter card.

Software: 5.13/12.8 release.

3.3 Testing Procedure

Please follow the steps given below if needed to test the changes on I-Sample 2.5:

1) Build the image with changes suggested above in the document.

2) Attach the Visu Daughter Card to main board.

3) After building and booting up the image, connect an oscilloscope.

And probe

a) A126 (ND_nWP) pin, present in daughter card at J104 for ND_nWP pin.

b) A154 (DTS8) pin, present in daughter card at J109 for GPIO_17 pin.

c) A170 (LCDnRST) pin, present in daughter card at J104 for LCD_NRST pin.

4) Now validate either by making a call setup and go to a integer channel on high band or use ETM by entering the following commands

tms 1

use rf

rfpw 7 3 0

rfpw 2 621

txpw 1 15

rfe 3

Above command will let the pulse be present and it can be measured by the oscilloscope at integer-channel 621 in PCS1900. This confirms the dithering presence.

To change channel the command rfpw 2 xxx can be executed, where xxx indicates the channel number.

rfe 0

Above command will disable the transmitter and the dithering signal is also deactivated.

A Appendix: Dithering Sideband Level vs. simulated DGAIN.

A number of different dithering circuits have been built and tested on the I-sample platform, and the same circuits have been simulated as described. The figure below shows the simulated DGAIN versus the measured sideband level (±3.25 MHz).

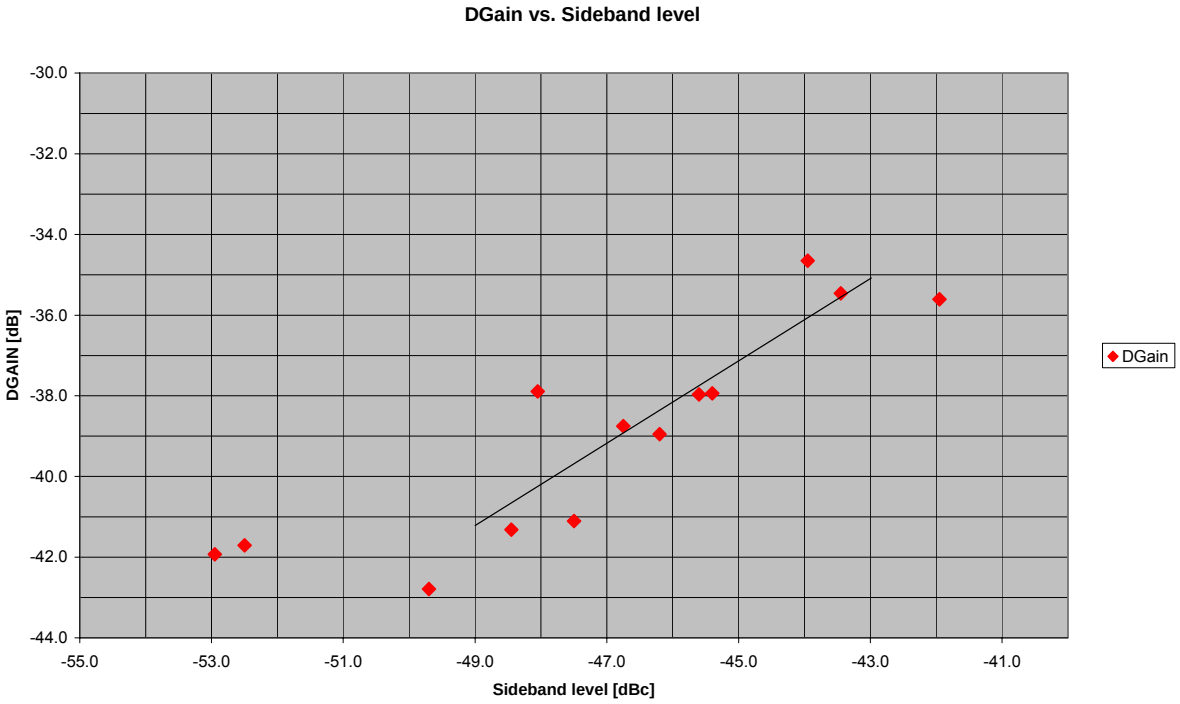
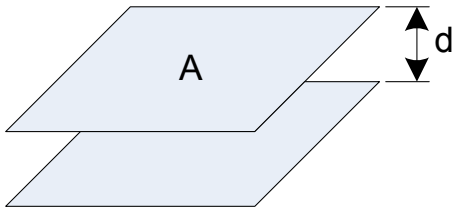


Figure 9. Dithering sideband level vs. simulated DGAIN for various different dithering circuits.

B Appendix: Stray Capacitance Calculation

In this document a simplified approach for calculating stray capacitance is used. The formula for a simple plate capacitor is used and therefore the fringing effects are not taken into account. The advantage of this is that the stray capacitance (SC) can be normalized to 1 mm^2 (SCN), and the total stray capacitance of a circuit node can be calculated just by multiplying SCN by the area expressed in mm^2.



$$SC = \frac{\varepsilon_r \cdot A}{113 \cdot d}$$

Where A is area in mm^2, and d is distance in mm. ε_r is the relative dielectric constant (4.3 used in this document. The Normalized stray capacitance is therefore:

$$SCN = \frac{\varepsilon_r}{113 \cdot d}$$

For I-sample the SCN values is calculated as:

d = 65 um is 0.585 fF/mm^2

d = 130 um is 0.293fF/ mm^2

In general SCN vs. d under the above conditions can be seen below.

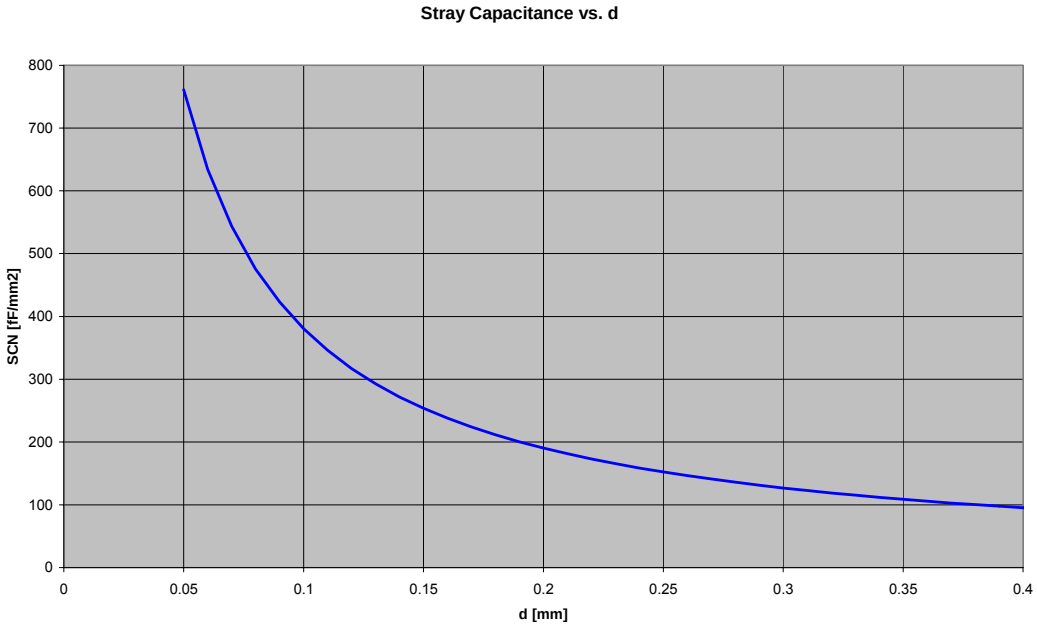


Figure 10. Normalized stray capacitance vs. d.