Making
Wireless

2.5 G GSM/GPRS
LOCOSTO-IC DBB

Texas Instruments Shanghai
Wireless Customer Integration & Design Center

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AGENDA

- SYSTEM OVERVIEW
- DBB OVERVIEW
- ARMIF
- EMIF
- SYSTEM DMA
- CLOCK MANAGEMENT
- CAMERA APPLICATION
- EXTERNAL PERIPHERALS
- SECURE ENVIRONMENT

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LOCOSTO-IC

SYSTEM OVERVIEW

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LOCOSTO-IC CHIPSET OVERVIEW

- **Locosto+:**
  - Serves the GPRS hi-end market
  - Support the high end requirements such as Camera, MP3 player, Midi32, Stereo, BT, IrDA
  - Supports a fairly rich Application suite
- **Locosto:**
  - Serves the entry GSM/GPRS market with basic feature sets
  - Midi16, camera
  - Supports basic Application suite
- **LocostoLite**
  - Serves GSM only market
  - Supports Basic Messaging functions

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LOCOSTO-IC CHIPSET OVERVIEW

- **TCS2300: TI low-cost ChipSet, addressing 2.5G**
- **LoCosto-IC: GSM/GPRS SoC (C027 /90nm ASIC lib)**
  - Ø **Digital Base Band structure (ARM7/c54x)**
  - Ø **Radio Frequency Sub-System (DRP2.0)**
- **Triton Lite: Analog Base Band chip (A07 TI Analog process)**
  - Ø **Voice & Stereo Audio**
  - Ø **Power & Battery management**
  - Ø **RTC, USB Transceiver…**
- **TCR3.2x: Software layer (TCR3.1x Based)**
  - Ø **Modem GSM/GPRS**
  - Ø **Applications suite**

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LOCOSTO-IC CHIPSET OVERVIEW

External/Extra Sub-System Supported

- LoCosto-IC
  - Flash
  - SIM Card
  - KeyBoard
  - Color LCD
  - USB 1.1, Full-Speed, Client
  - 26MHz Crystal
  - Power-Amplifier
  - Front-End Module
  - TI-Bluetooth (BRF6150) Wireless Short-Distance Connectivity
  - TI-AGPS /TWL5002 localization system (I/F provision)
  - Digital Camera systems.
  - UART Cable or IRDA
  - FM Radio receiver (ex. Philips TEA5767/68…)
  - NandFlash
  - CarKit &/ USB charger

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LOCOSTO-IC CHIPSET OVERVIEW

Basic External Sub-System:

- **TriTon Lite**
  - **HandSet Microphone & Speaker**
  - **HeadSet Mono/Stereo-Audio speakers & microphone connection**
  - **Melodie-Ringer (HandFree) &/ Buzzer**
  - **Battery Pack (Nimh/Li-ion) & 6-7V Reg or 20V Non-Reg Charger**
  - **Vibrator motor control**
  - **RTC 32KHz crystal**

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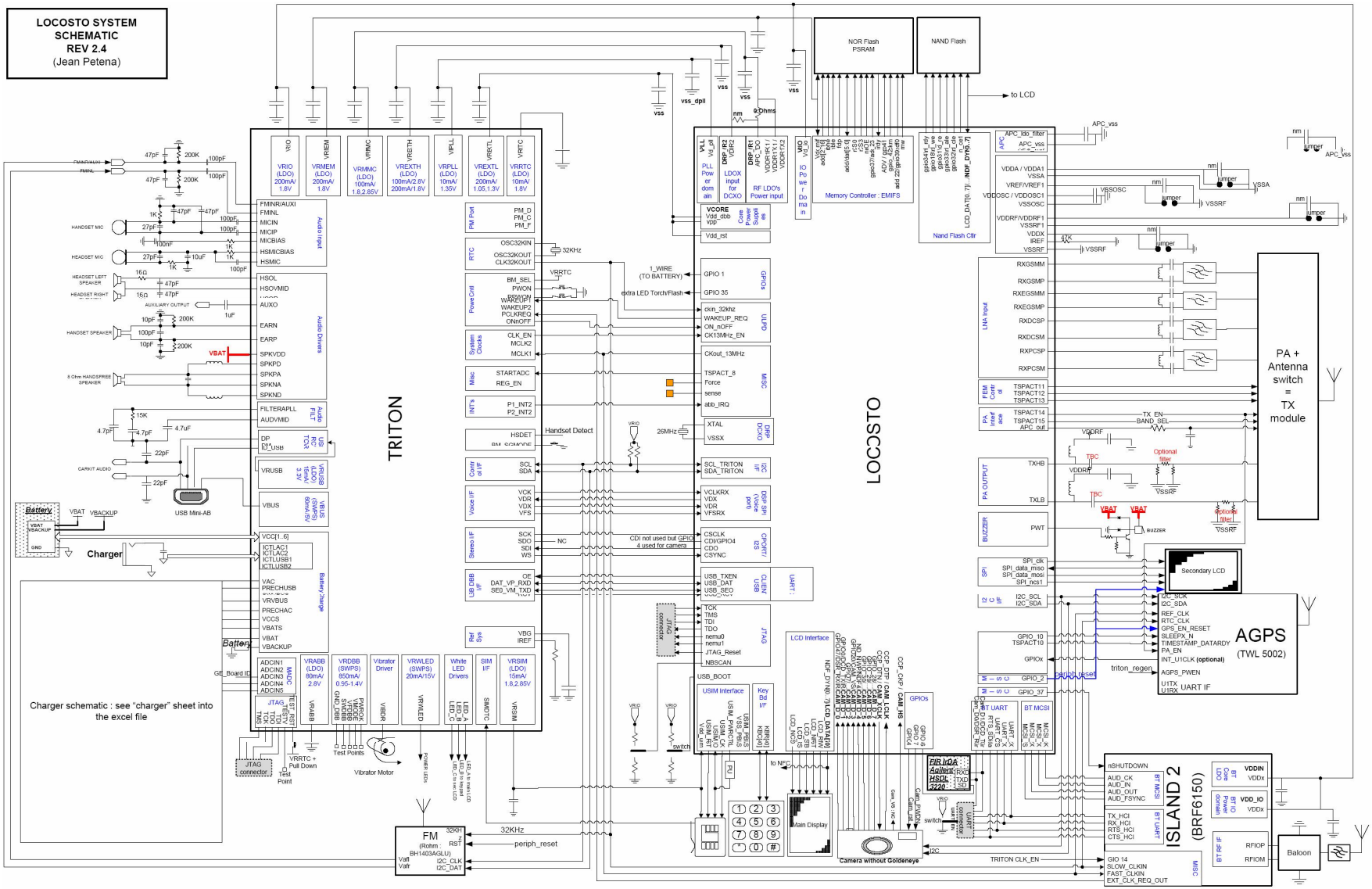
LOCOSTO-IC CHIPSET OVERVIEW



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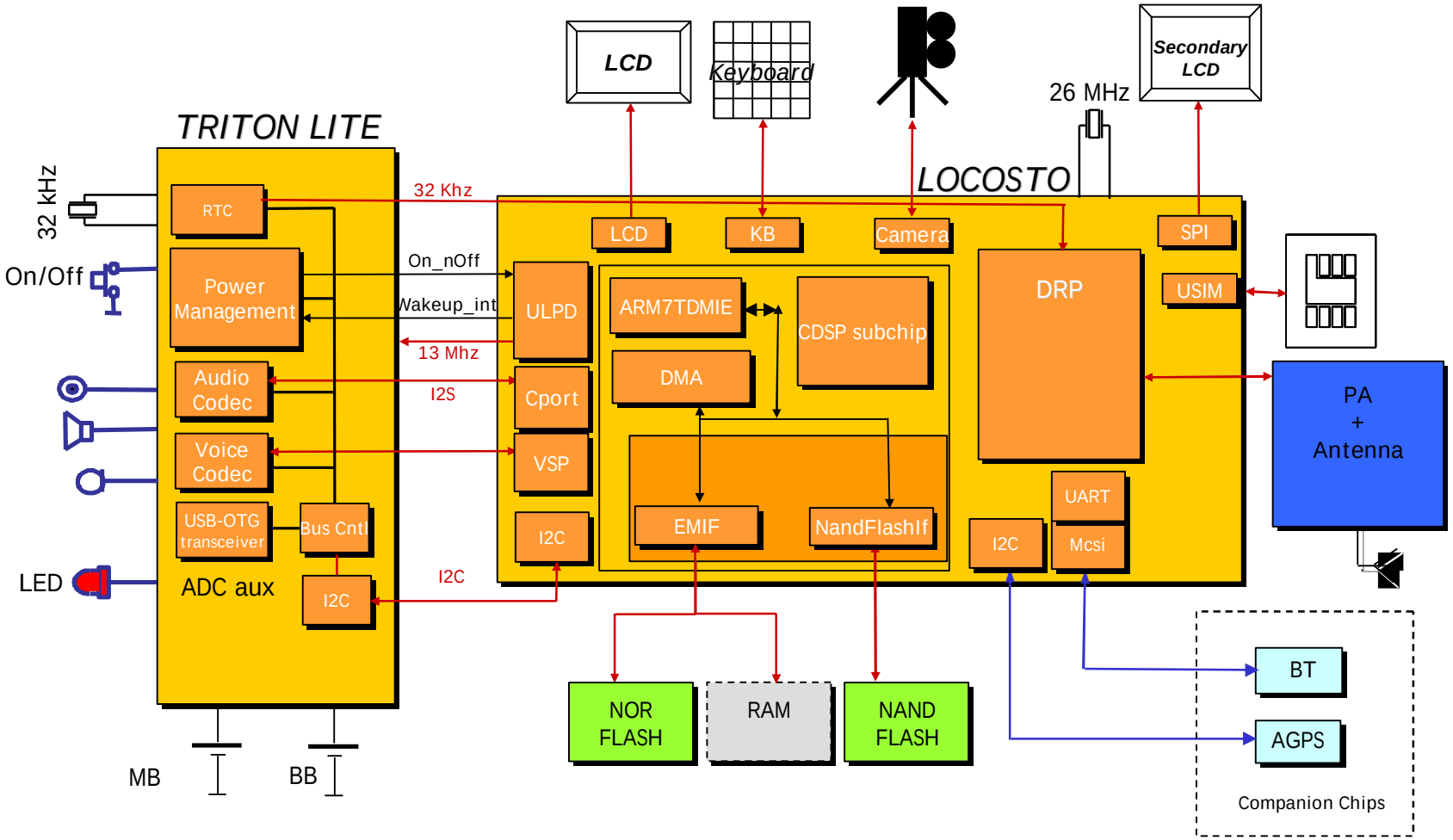
LOCOSTO-IC CHIPSET OVERVIEW



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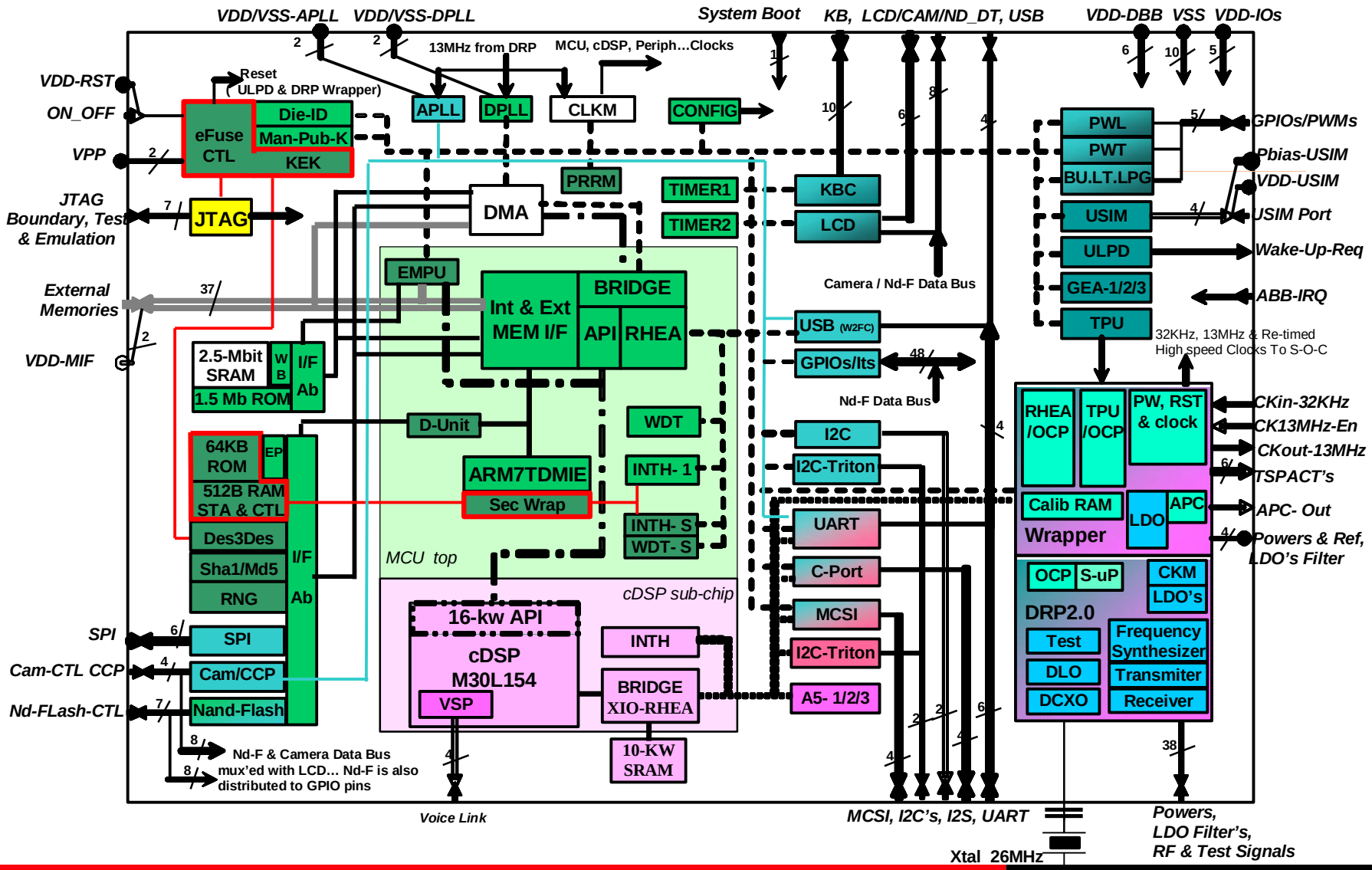
LOCOSTO-IC Hardware Architecture



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DBB Generic SoC Functions

- **DPLL & CLKM**
  - **System Clock & Reset Control.**
- **DMA**
  - **Direct Memory Access**
- **EMIF**
  - **External Memory Interface**
- **Interrupt Handler & Secure Interrupt handler**
  - **Main INTH 31 lines**
  - **Secure INTH 5 lines**
- **IO Configuration**
  - **I/O's mode selection (Multi-function I/O's, Test & debug…)**

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Making Wireless DBB Generic SoC Functions (continue)

- **2 General-Purpose Timers.**
  - **Auto-Reload / One-Shot modes.**
  - **Interrupts upon underflow.**
  - **13MHz clocking source.**
- **1 Watch-Dog or General-Purpose Timer.**
  - **Same as above or watch-dog timer (default)**
  - **13MHz/14 clocking source.**
- **Debug Unit**
  - **64 x 32-bit words FIFO**
  - **Continuous data record (MCU clock-cycle based)**
- **JTAG & eFuse Controller**
  - **Manufacturing, Test & Debug Facilities…**

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Dedicated Peripherals (Rhea Bus)

- **Ultra Low-Power Down controller (ULPD)**
  - Ø **Power-ON/Down & Deep-Sleep mode management**
  - Ø **Maintains GSM time base from the 32KHz low-power reference clock**
- **Time Processing Unit (TPU)**
  - Ø **2 ports RAM of 1024 words of 16 bits scenario's storage unit**
  - Ø **micro-instructions based Scheduler**
  - Ø **Real Time control (GSM Q-Bit) of RF & Analog (TSPACT 7-int / 9-Ext)**
- ***RF Transceiver; Digital Radio Processor (DRP2.0)***
- ***GPRS Encryption Algorithm (GEA1/2/3)***
  - Ø **Support Frame Check Sequence & ciphering/deciphering mode 1,2 and 3. (GSM 01.61, 04.64 recommendations).**
- ***GSM Cipher-processor (A51/2/3)***
  - Ø **implements A51, A52 (GSM Rec03.20) and new A5/3 Kasumi algorithm (GSM/EDGE Cipher algorithm)**

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Dedicated Peripherals (Rhea Bus)

- **USIM Interface**
  - Ø **GSM SIM-card controller**
  - Ø **H/W management for T-0 and T-1 transmission protocols, (ISO7816.3)**
- **2 I2C H/W-controller @400Kbps (1 MCU + 1 DSP /same bus I/F)**
  - Ø **TriTon Lite ABB (Power, USB-Xcvr, Voice & Stereo Codec's, RTC)**
- **1 C-port/I2S Audio-Stereo Codec serial interface**
  - Ø **Slave up to 3.072Mbps (Exclusive Static sharing DSP/MCU)**
  - Ø **TriTon Lite ABB (Stereo-Audio codec data)**
- **1 Voice Serial Port Slave @500kbps (cDSP internal TI-Bus)**

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Making Wireless LOCOSTO-IC DBB External I/F's (1/4)

All connectivity interfaces support a 1.8V maximum voltage with the exception of the USIM pin's that are 3V compliant.

- **RHEA Bus (MCU &/ cDSP) @52Mhz**
  - Ø **1 Enhanced Keyboard controller**
    - ü **Up to 5-Row x 5-Column matrix /25 keys (interrupt driven)**
  - Ø **1 LCD-controller 8-bit parallel I/F @13MHz**
    - ü **6800 or 8080 protocol**
    - ü **DMA capability**
  - Ø **1 Multi-Channel Serial Interface @13Mbps**
    - ü **Exclusive Static sharing DSP/MCU with DMA capability**
    - ü **Voice Interface for external BlueTooth PCM-Codec connection**
    - ü **cDSP sub-system debug…**

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- **RHEA Bus (MCU &/ cDSP) @52Mhz (Continued)**

  - **1 UART Modem/IRDA, Auto-Baud capability @115.2Kbps**
    - **Exclusive Static sharing DSP/MCU with DMA capability**
    - **Data Interface for external BlueTooth Modem connection**
    - **Or Host serial cable (support Manufacturing Flash Loader @3.25Mbps)**
    - **Or IRDA up to FIR @4Mbps**

  - **1 I2C H/W-controller @400Kbps (MCU only) for controlling optional implementation such as:**
    - **A-GPS module**
    - **Frequency Modulation Radio chip(FM Stereo Radio)**
    - **Camera Sensor/Module**
    - **B/W LCD…**

  - **2 I2C H/W-controller @400Kbps (1 MCU + 1 DSP /same bus I/F)**

  - **1 USIM (Universal Subscriber Identity Module) Interface @100Kbps**

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LOCOSTO-IC DBB External I/F's (3/4)

- **RHEA Bus (MCU &/ cDSP) @52Mhz (Continued)**

  - **1 C-port/I2S Audio-Stereo Codec serial interface, Slave up to 3.072Mbps**

  - **1 USB 1.1 client full speed (12Mbps)**
    - **Host serial cable (PC connection…)**
    - **Car-kit**
    - **Battery charger**

  - **Up to 48General Purpose I/O's with Interrupt capability**

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Making Wireless LOCOSTO-IC DBB External I/F's (4/4)

- **Peripheral Bus (MCU)**
  - Ø **1 Parallel Camera-port**
    - ü **Camera module (RGB & YUV output format)**
  - Ø **1 Nand-Flash 8-bit I/F up to 26MHz intended for Data storage.**
  - Ø **1 Master/Slave SPI up to 26Mbps with DMA capability**

- **cDSP embedded TI Bus**
  - Ø **1 Voice Serial Port Slave @500kbps (DSP sub-system)**

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LOCOSTO-IC DBB SECURITY

- **IMIF Bus (MCU)**
  - Ø **64-KByte Boot ROM,**
  - Ø **512-Byte Secure RAM**

- **<u>Peripheral Bus (MCU)</u>**
  - Ø **Protected Mode control & status register**
  - Ø **Random Number Generator**
  - Ø **Hashing SHA-1/MD5 Crypto-processor**
  - Ø **Symmetrical encryption DES/3-DES Crypto-processor**

- **RHEA Bus (MCU)**
  - Ø **Secure Interrupt Handler**
  - Ø **Secure Watch-Dog/Timer**
  - Ø **Protected Resources Reset Manager**
  - Ø **Enhanced Memory Protection Unit**
  - Ø **DMA's secure-Channel**
  - Ø **CLKM; system-Clock's Lock**
  - Ø **Manufacturer Public Key**

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LOCOSTO-IC Engine Performance

- **DSP Sub-System @104Mhz**
  - Ø **c54x CPU based**
  - Ø **30-K 16-bit word RAM (including 16-Kw API)**
  - Ø **154-K 16-bit word ROM**
  - Ø **10-K 16-bit word RAM (external to cDSP; Patch, MP3…)**
  - Ø **Memory-mapped control & status register (XIO/RHEA @52MHz)**

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LOCOSTO-IC Engine Performance

- **ARM7 @104Mhz, (Host processor)**
  - Ø 2.5-Mbit SRAM, single-cycle access @104MHz
  - Ø 1.5-Mbit ROM (Midi, JPEG…) single-cycle access @104MHz
  - Ø 16-Kw ARM/cDSP RAM I/F (API), 2-cycle @104Mhz
  - Ø Memory-mapped control & status register
    - Ø RHEA @52MHz
    - Ø "Memory-Like" Peripherals @52MHz
  - Ø External memory extension Burst @52MHz

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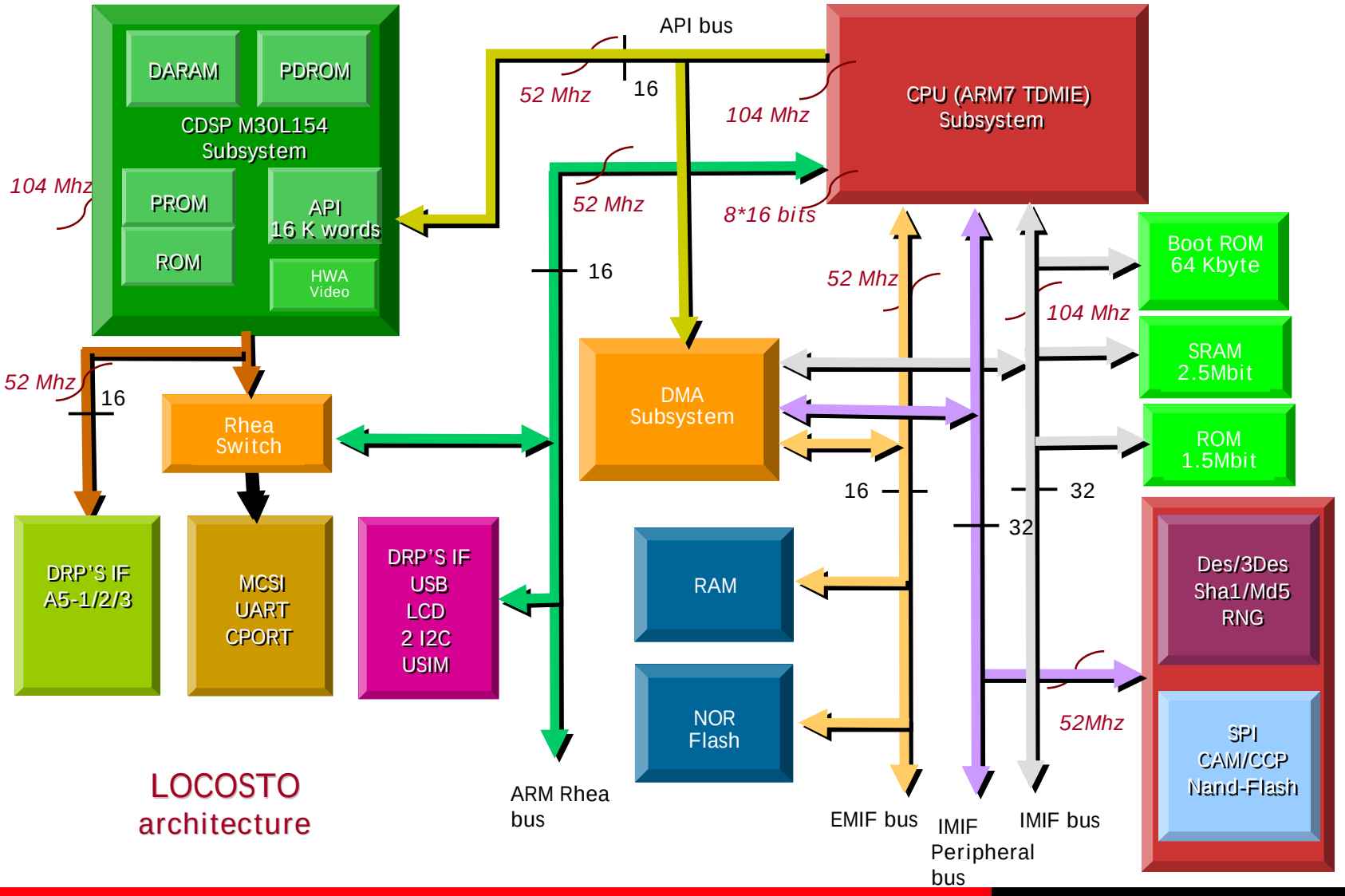
LOCOSTO-IC Architecture Performances



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LOCOSTO-IC ARMIF
ARM MEMORY INTERFACE

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LOCOSTO-IC ARMIF

- **The Arm memory interface handles**
  - Ø **Internal Arm memory access management**
  - Ø **Internal Arm peripheral access management**
  - Ø **External Arm Memory interface (EMIF) access management**
  - Ø **Arm to API memory access management**
  - Ø **Arm to Rhea bridge access management**
  - Ø **Arm nWAIT and access control flags generation**

- **The Arm memory interface does not perform external memory decode anymore and depends upon the EMIF module to manage the external accesses**

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LOCOSTO-IC EMIF
EXTERNAL MEMORY INTERFACE

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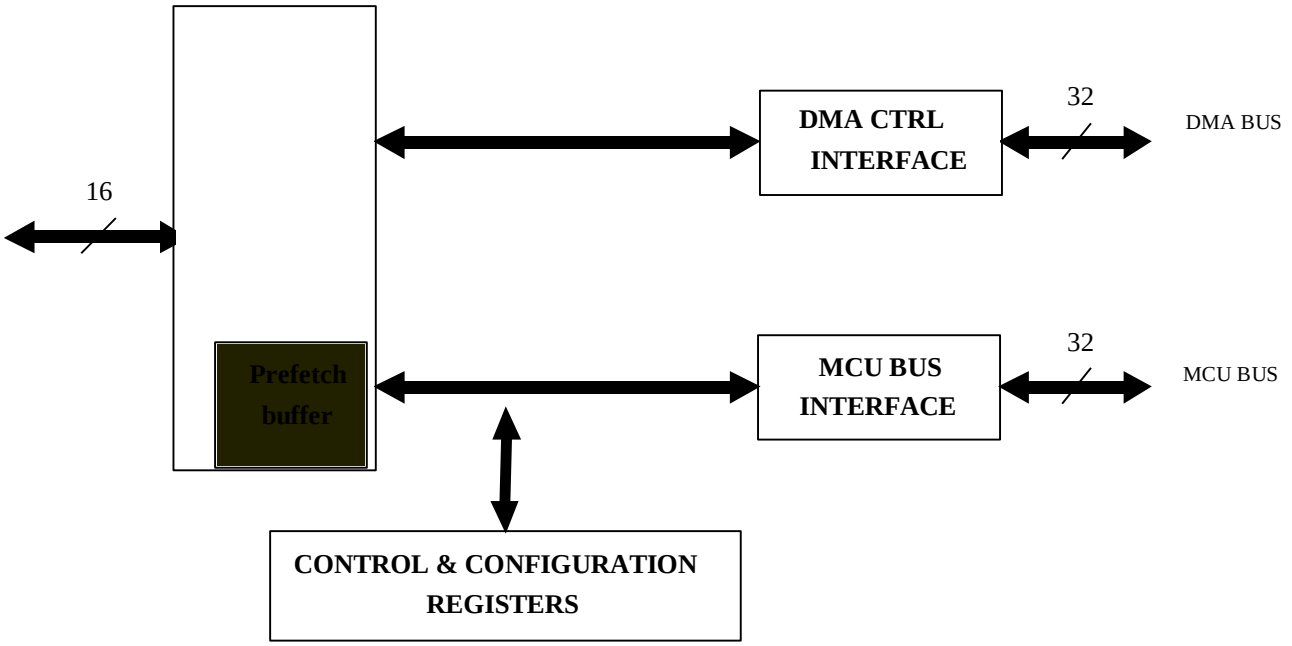
EMIF Block Diagram

The External Memory Interface (**EMIF**), is part of MCU sub-system that manages the read/writes between MCU/DMA and external memory (like flashes and SRAMs).



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EMIF Features

- **Support 8/16/32 bit read/write from MCU/DMA**
- **Burst read/write from DMA.**
- **16-bit word data-bus**
- **Supports up to 4 chip selects, each chip 32Mbyte**
- **Each CS separately configurable for**
  - **Asynchronous Read/Write** (Default)
    - Programmable Wait-States
    - Support dynamic access time through external nRDY signal
  - **Synchronous Burst Read/Write**
    - Continuous, 4-, 8- 16 word burst
    - 52Mhz clock for burst accesses
- **Support wait state insertion for read and write access**
- **External memory frequency configuration**
- **Protect mode support (Read only)**
- **Support only little endian format.**

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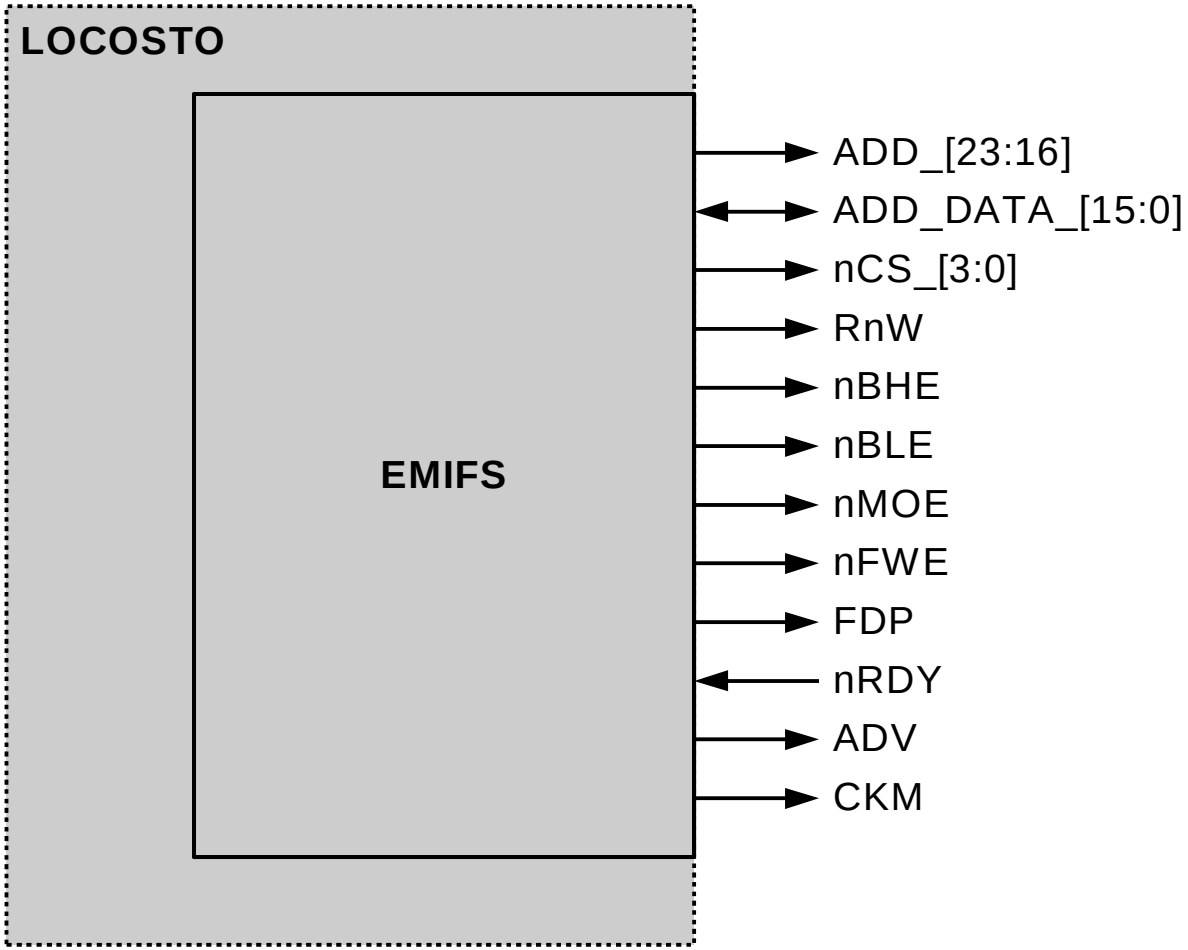
EMIF External signals



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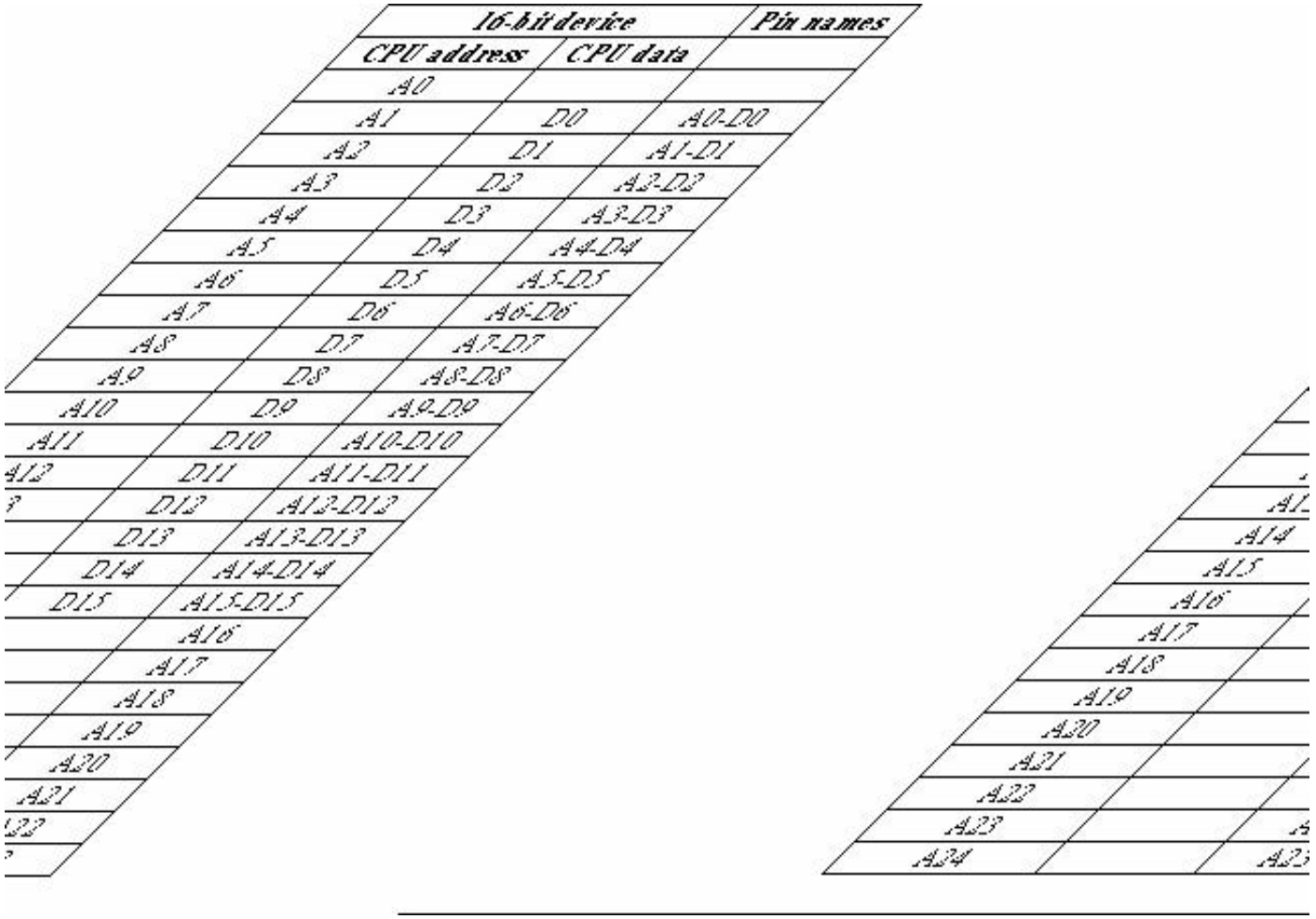
EMIF Multiplexed bus Address/Data



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EMIF Protocol mode

Different modes available through MEMMODE field of EMIF chip select configuration registers

MEMMODE	Read operation	Write operation
0	Async read.	Async Write
1	Synchronous burst read protocol1 (Flash)	Async write(flash)
10	Synchronous burst read Protocol2(CellularRAM™)	Synchronous burst Write Protocol2(CellularRAM™)
11	Reserved.	Reserved.
100	Reserved	Reserved
101	Reserved	Reserved
110	Reserved	Reserved
111	Reserved	Reserved

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EMIF Handshaking mode

- **EMIF support the ready/Wait signal from the external memory in two modes. Assertion of ready/wait signal extend the access time until the ready/wait is de-asserted.**

Ø **Non-full handshaking mode**

In this mode of operation the ready/wait signal from the memory is ignored.

Ø **Full handshaking mode**

In this mode of operation the ready/signal from external memory extend the access time. In this there are two modes of support.

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EMIF Power Save Mode

- EMIF supports two power saving modes:
  - Ø Global IDLE mode
  - Ø Dynamic power saving mode

- Power saving modes depend on the:
  - Ø PDE
  - Ø PWD_en

  bit fields of EMIF configuration register

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LOCOSTO-IC DMA

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DMA Features

- **6 channels**
  - Channel allocation ARM or DSP
  - Secured channel configurable
- **4 ports**
  - RHEA
  - API
  - IMIF
  - EMIF

- **2 levels of priority on each channel.**
- **Both hardware / software request capability.**
- **Transfer of data up to 32 bits.**
- **Data burst capability.**
- **Data packing / splitting.**

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DMA Features

- **Data bursting.**
- **3 addressing modes**
  - constant,
  - post-increment
  - frame-indexed.
- **Auto-initialization capability.**
- **Auto Gating capability**
- **Generation of interrupts on various events.**
  - End of block
  - End of frame
  - Half block
  - Request drop
  - Timeout

- An element
  can be 1,2 and 4 bytes, programmable
- A frame
  can contain 1~65535 elements, programmable
- A block
  can contain 1~65535 frames, programmable

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DMA Channel Mapping

1 2	DRP	TX RX
3	LCD interface	TX
4 5	UART IRDA/MODEM	TX RX
6 7	MSSPI	TX RX
8	*Unused*	TX
9	*Unused*	RX
10 11 12 13 14 15	USB	RX 1 TX 1 RX 2 TX 2 RX 3 TX 3
16 17	I2C (Triton)	RX TX
18	*Unused*	--NA--
19 20	USIM	RX TX
21 22	Reserved *Unused*	-----NA---- -----NA----
23	*Unused*	RX/TX
24	NAND flash	RX/TX
25 26	I2C	RX TX
27	SHA-1	TX
28 29	DES-3/DES	RX TX
30 31	C-PORT (I2S)	RX TX

Note:
TX means data transfer from DMA to Peripheral

RX means data transfer from Peripheral to DMA

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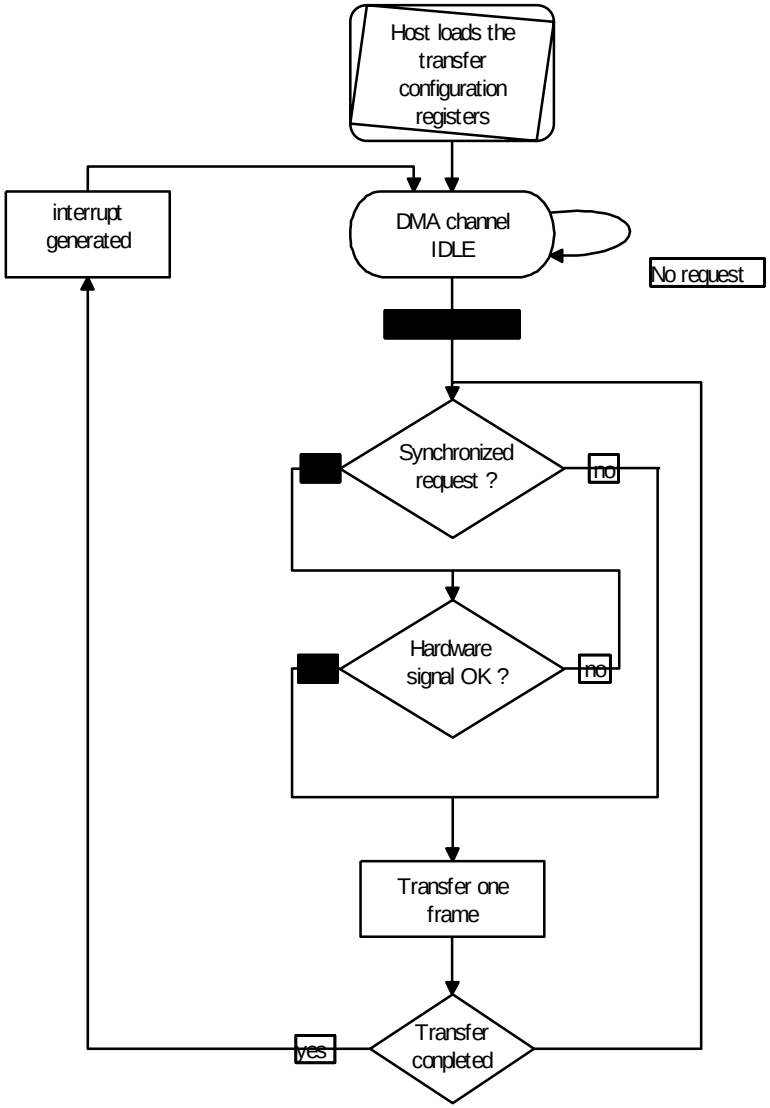
Basic flow of DMA transfer



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LOCOSTO-IC CLKM
CLOCK MANAGEMENT

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CLOCK MANAGEMENT

- **The Clock-Management system:**
  - Ø DPLL
  - Ø CLKM
  - Ø APLL

- **Each associated to memory-mapped registers for programming DBB system clocks frequencies (DSP, MCU, Rhea-Bridge & Peripherals clocks).**

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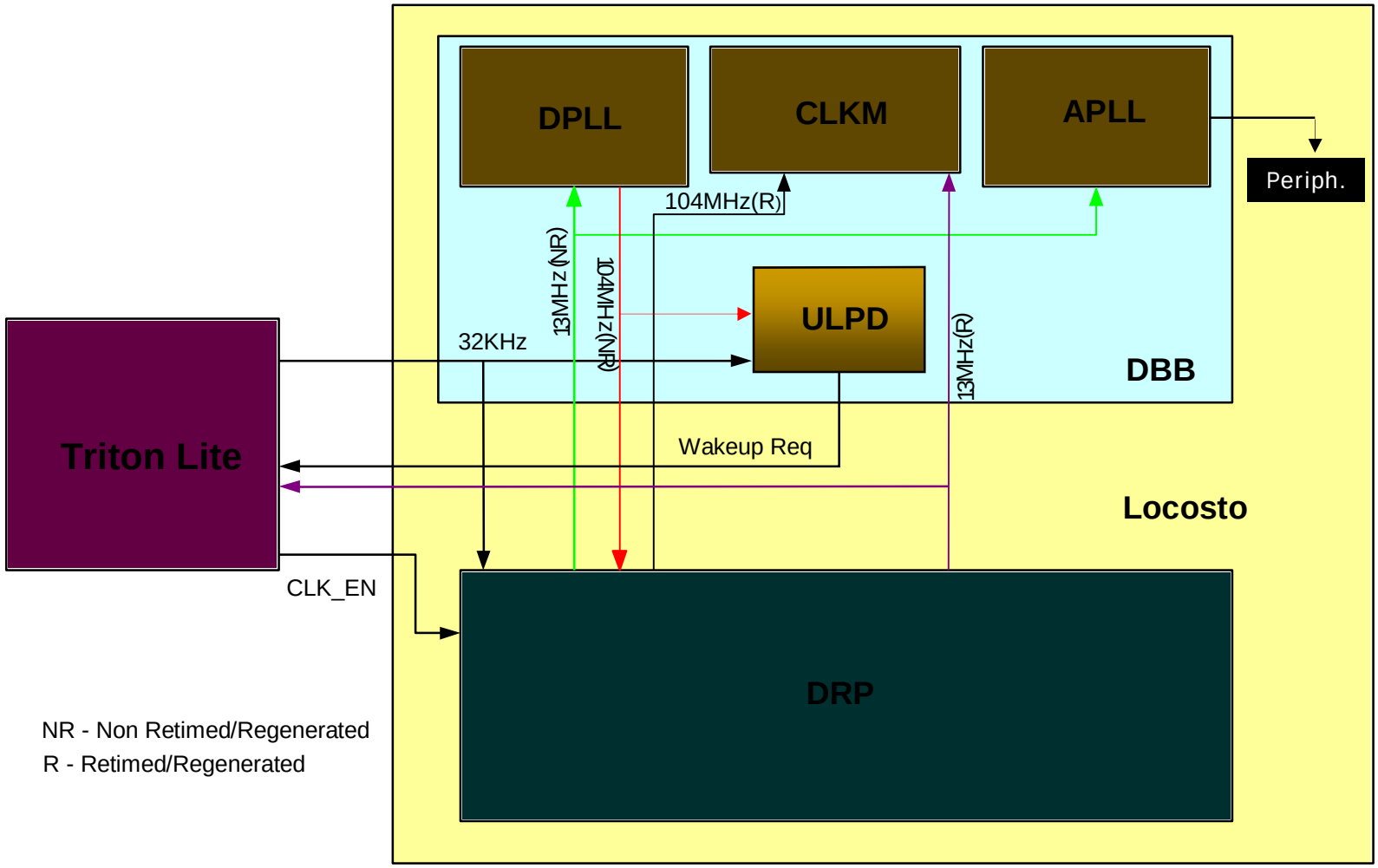
CLOCK MANAGEMENT OVERVIEW



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CLOCK MANAGEMENT OVERVIEW

- **Locosto DBB has primarily four independent clock domains and many more derived clock domains.**

- **The primary clock domains are:**
  - Ø **32KHz clock from Triton Lite**
  - Ø **13MHz clock from DRP**
  - Ø **104MHz clock from DPLL**
  - Ø **48 MHz clock from APLL**

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DSP/MCU Clock Regeneration

- To reduce the digital switching noise, MCU/DSP 104MHz clock also needs to be synchronous to the RF clock (ADPLL clock).

- DPLL block uses the DRP non-retimed 13MHz clock to generate the 104MHz. This 104MHz from DPLL is only used by ULPD (for gauging).

- MCU/DSP don’t directly use this clock but use a regenerated version of this clock.

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CLOCK MANAGEMENT DPLL

- **The DPLL is programmable in "multiplication-mode" with the following values:**

$$F_{out} = F_{in} \times \frac{m}{d}$$

m = 1 up-to 32 (step 1) d = 1, 2, 3 or 4

And in "division-Mode" with the following values:

$$F_{out} = \frac{F_{in}}{k}$$

k = 1, 2 or 4

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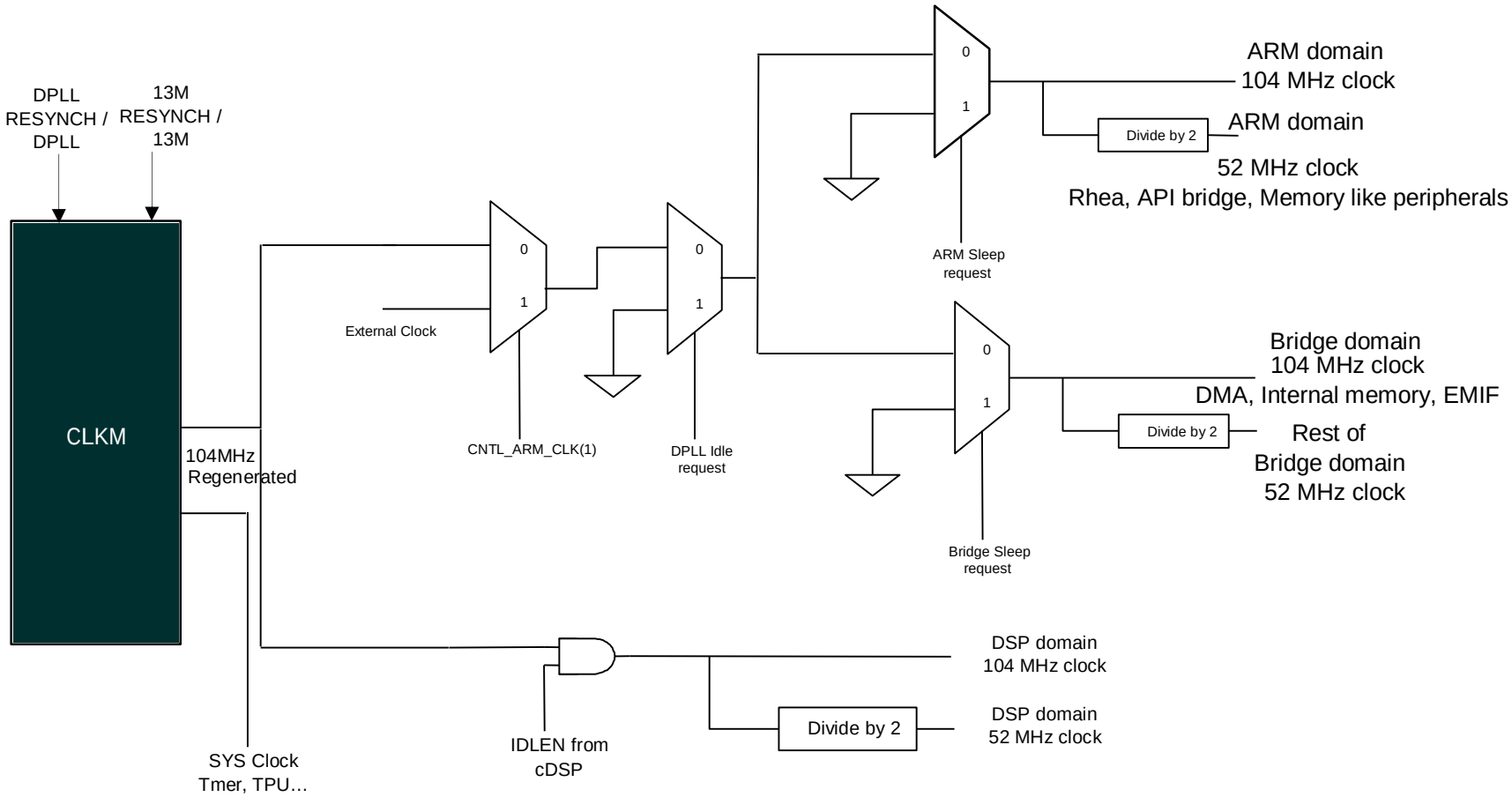
CLKM CLOCK TREE



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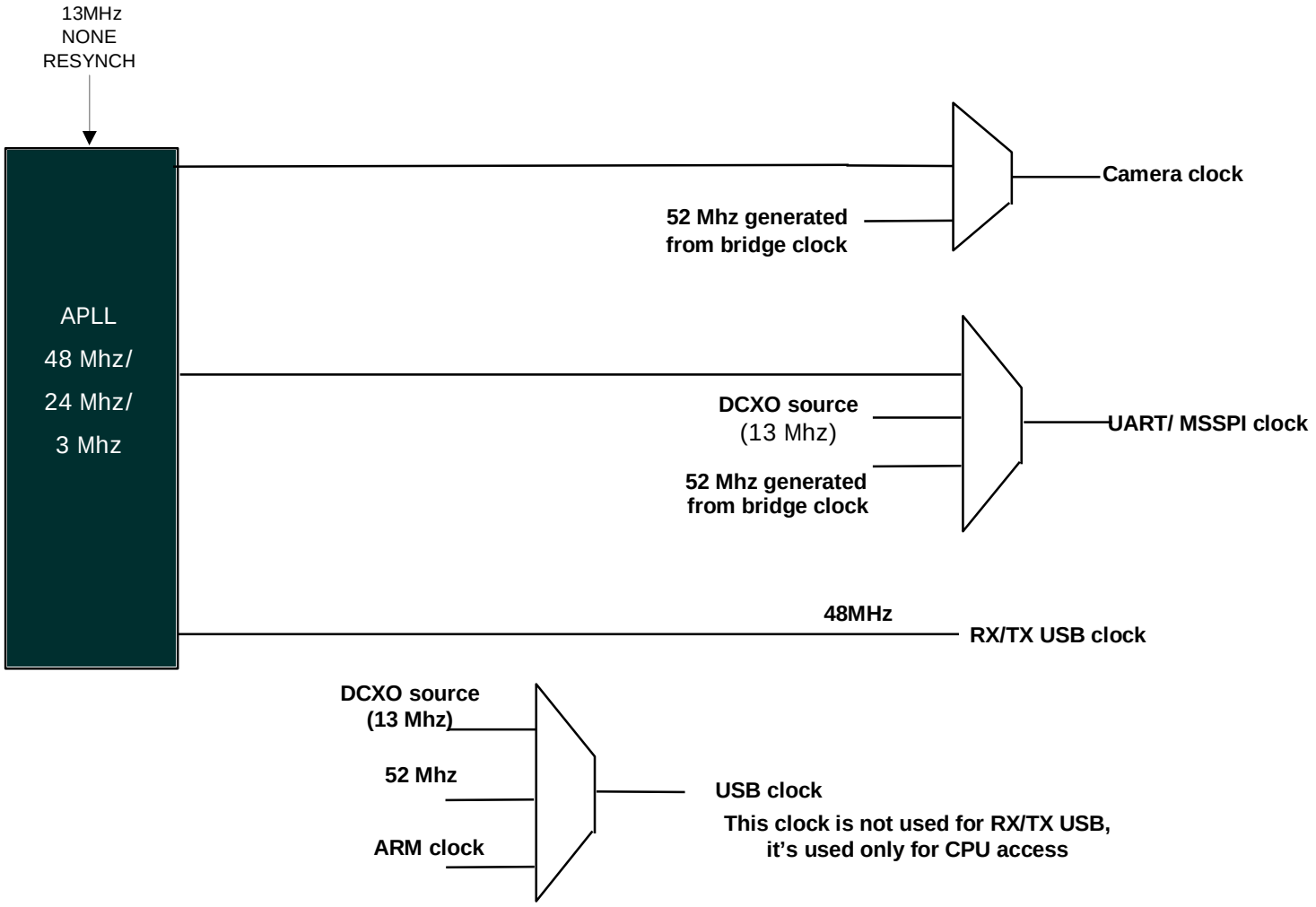
PERIPHERALS CLOCK TREE



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LOCOSTO-IC LCD INTERFACE

LOCOSTO-IC
LCD INTERFACE

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LCD INTERFACE FEATURES

- 8-bit parallel Interface
- Compliant 6800/8086 .
- Can interface two external LCD (2 Chips select)
- Compliant for QCIF (176x144) /QVGA (160x120) resolution.
- The maximum transfer rate is 13Mbytes per seconds.
- DMA management

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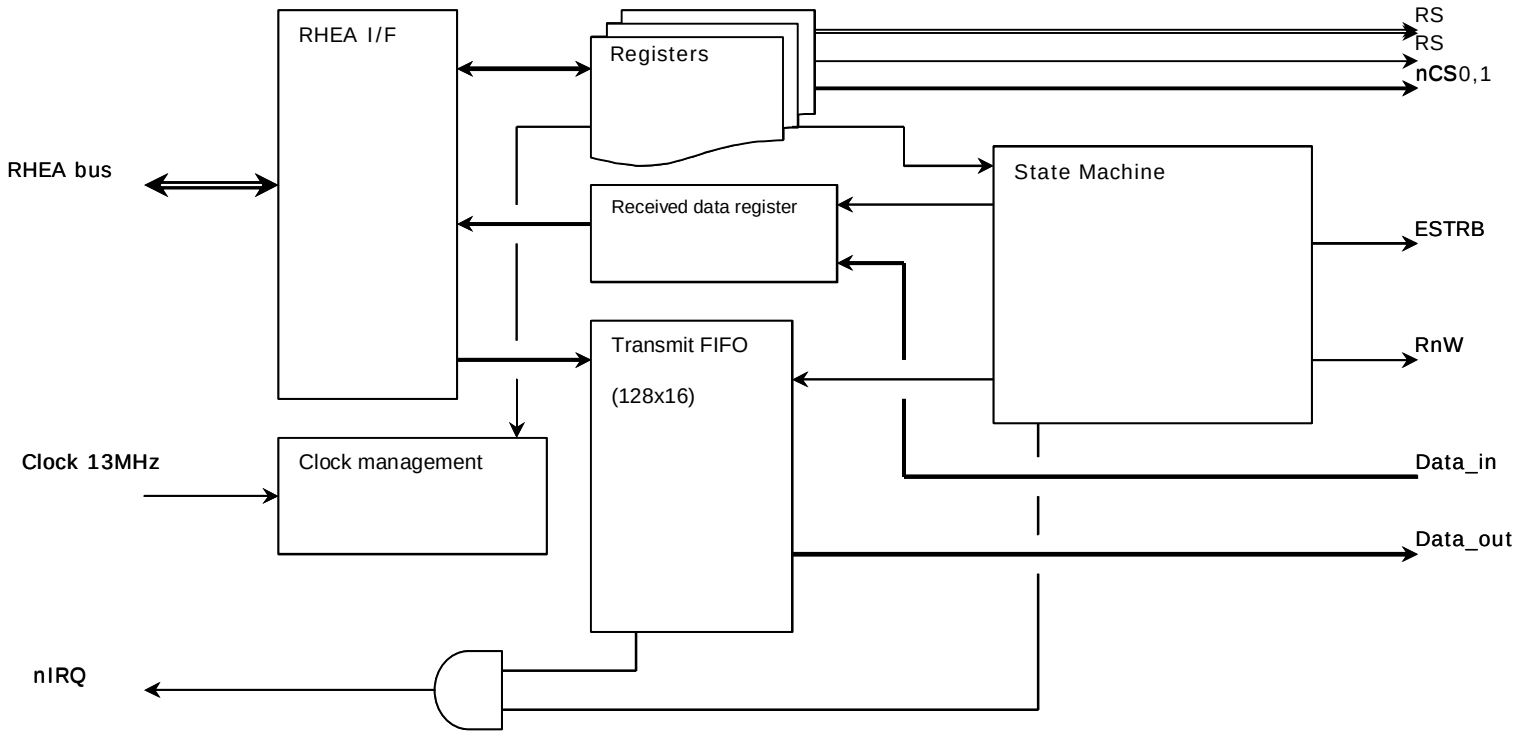
LCD INTERFACE OVERVIEW



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LCD INTERFACE SIGNALS

lcd_ncs0	out	Lcd interface chip select, for chip 0. Data IO are available when Low. When High, Data IO are in high impedance state.	1	1
lcd_ncs1	out	Lcd interface chip select, for chip 1. Data IO are available when Low. When High, Data IO are in high impedance state.	1	1
lcd_rs	out	Lcd interface register selection.	1	0
lcd_rnw	out	6800-mode : Read / Write control Pin. When High: Read, when Low: write.	1	0
		8086-mode : write enable clock. Send data to the LCD controller on the rnw falling edge.		
lcd_estrb	out	6800-mode : strobe enable. Read data from LCD controller on Strobe falling edge, send data to the LCD controller on Strobe rising edge.	1	0
		8086-mode : Read enable. Read data from LCD controller on the Strobe rising edge.		
lcd_nreset	out	Lcd interface reset.	1	0
lcd_data[7:0]	in	Lcd interface data in/out bus	8	

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LOCOSTO-IC NAND FLASH INTERFACE

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NAND FLASH INTERFACE FEATURES

- Flexible architecture to support different sizes of Nand Flash Memory
- 8-bit data (commands, addresses and data are multiplexed) and 8 bits control interface to Nand Flash Memory
- 8, 16 and 32 bits interface from host processor to buffer, 32 bits for registers.
- Double page Buffer implementation (2*128 bytes)
- Programmable Nand Flash access time
- Interrupt and flag (polling operations) for end page, end transfer, end ECC and end busy
- Fully automatic transfer process
- Programmable number of bytes for command, address and data
- Support different page size of Nand Flash Memory
- Low consumption in idle
- Support DMA transfer and DMA request
- Support sequential read in Nand Flash Memory
- Support Error Code Correction (ECC)

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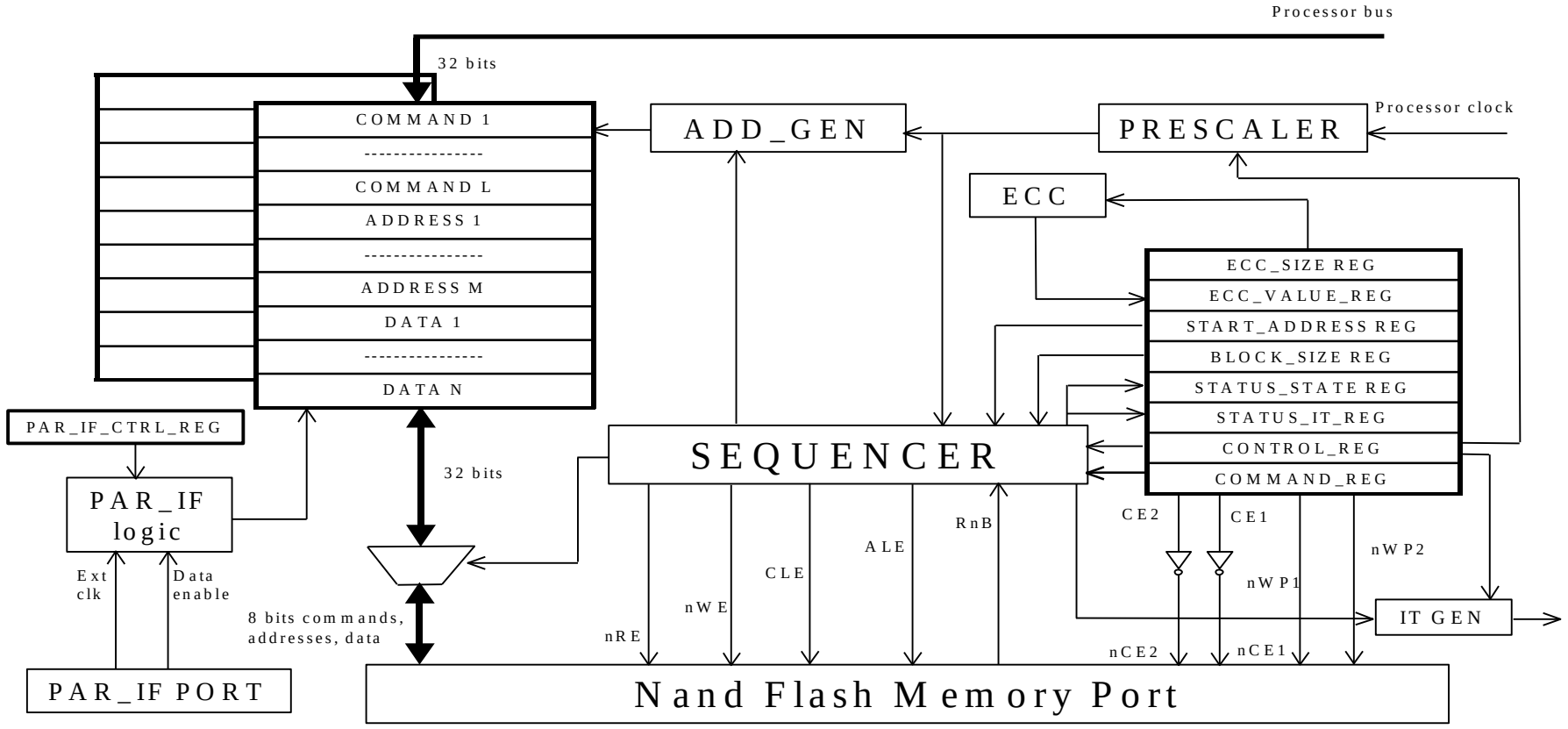
NANDFLASH INTERFACE BLOCK DIAGRAM



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NAND FLASH INTERFACE SIGNALS

IO_nd_flash	Data Input/Output Flash Memory	IN	8
ale_nd_flash	Address latch enable to Nand Flash Memory	OUT	1
cle_nd_flash	Command latch enable to Nand Flash Memory	OUT	1
nre_nd_flash	Read enable to Nand Flash Memory	OUT	1
nwe_nd_flash	Write enable to Nand Flash Memory	OUT	1
nwp1_nd_flash	Write protect to Nand Flash Memory 1	OUT	1
nwp2_nd_flash	Write protect to Nand Flash Memory 2	OUT	1
nce1_nd_flash	Chip enable 1 to Nand Flash Memory 1	OUT	1
nce2_nd_flash	Chip enable 2 to Nand Flash Memory 2	OUT	1
Ready_nbusy_nd_flash	Ready/busy from Nand Flash Memory	IN	1

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CAMERA APPLICATION

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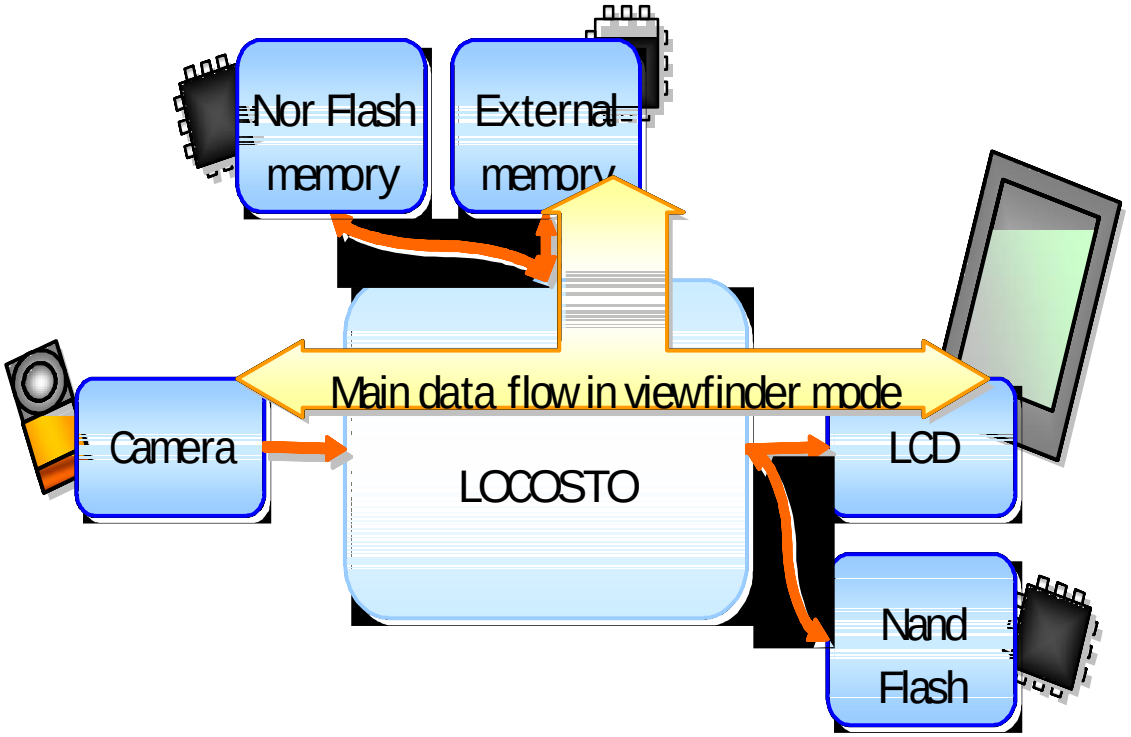
CAMERA FLOW



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CAMERA USE

- Preview mode: in this mode, the current view is displayed on the LCD, so that the user can adjust its position. The display is refreshed at 15 fps.

- Snapshot mode: in this mode, the current picture is captured into RAM. It is then compressed into JPEG format and sent to an appropriate storage device (e.g. flash RAM).

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SYSTEM REQUIREMENTS

- Camera and LCD RGB data format (used during viewfinder) must match, and integrate properly with the existing graphics software.
- I/O voltage: Locosto I/O voltage is 1.8V.
- Viewfinder frame rate of no less than 15 fps is targeted.
- Total time for snapshot capture to memory must be less than 1/5 s.
- Total “shot to shot” delay must be less than 5 s.

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CAMERA SYSTEM IMPROVEMENT

- **Double the frequency of the CPU from 52 MHz to 104 MHz, to increase performances**
- **Add a DMA to external memory, to diminish the impact of the increased external RAM bandwidth usage on the CPU load**
- **Use Read/Write burst RAM, to maintain acceptable external RAM throughput**
- **Add a prefetch buffer for CPU code fetches, to maintain acceptable performances when fetching code from external RAM**
- **Embed some software engines (MIDI and JPEG) in an internal ROM. This makes it possible to benefit from fast, 32bit accesses for those CPU demanding routines, while accounting for only ¼ of the equivalent RAM size on the silicon**

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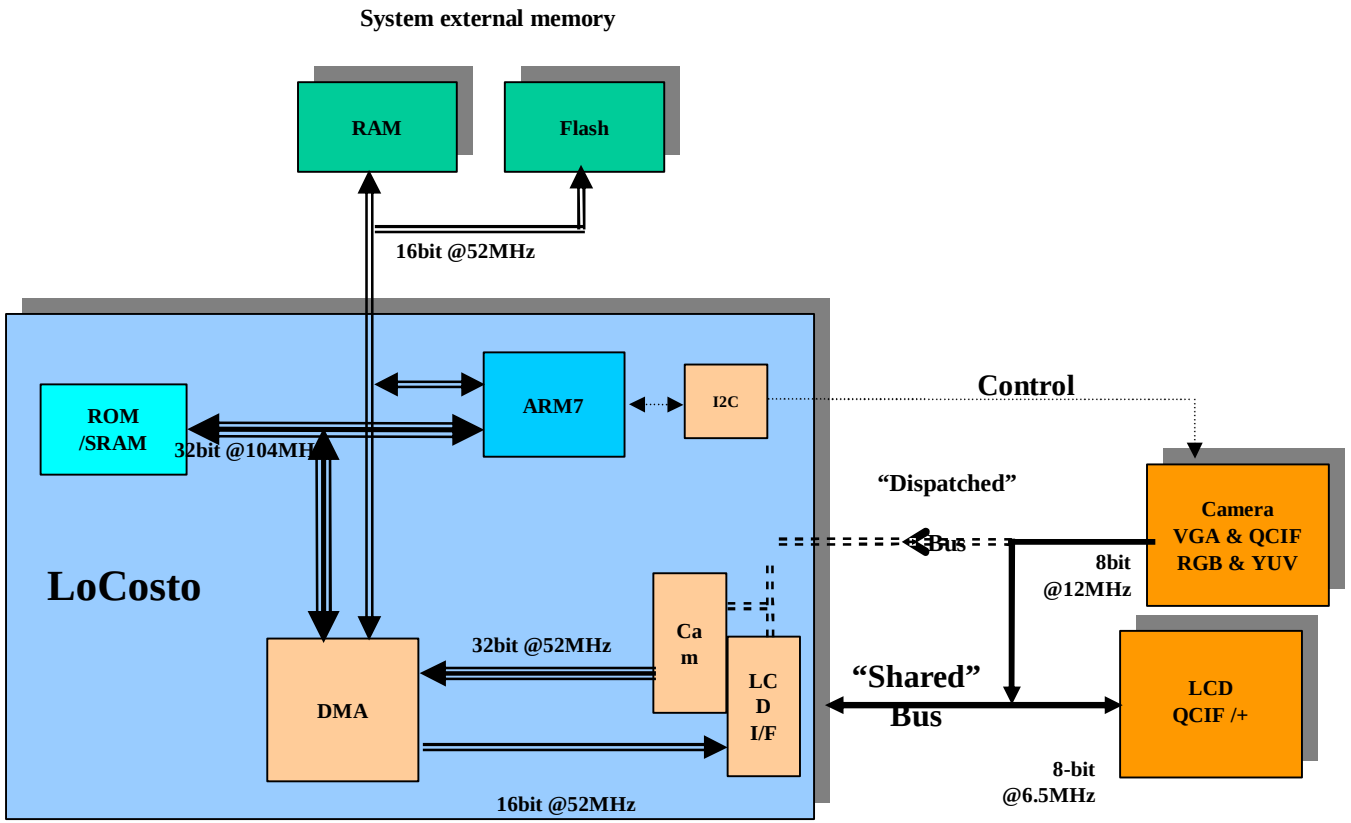
CAMERA HARDWARE SYSTEM DIAGRAM



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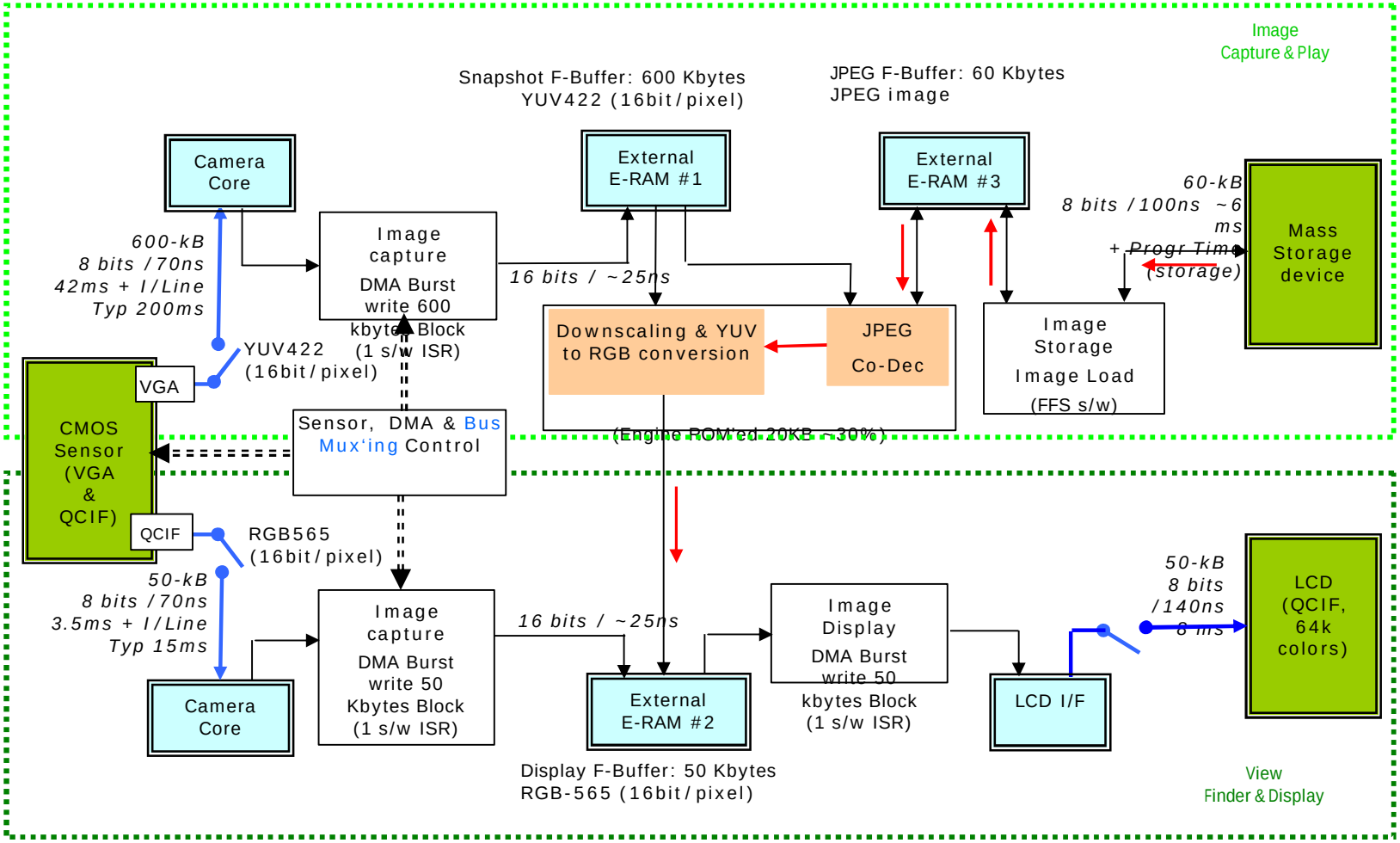
CAMERA SYSTEM ARCHITECTURE



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CAMERA REQUIREMENTS

- **Picture size: The camera module must be able to deliver pictures in the range QCIF / 176x144 up to VGA / 640x480.**
- **Frame rate: The targeted frame rate in viewfinder mode is 15 fps.**
- **Data format: The output formats that need to be supported natively by the camera module are the following:**
  - RGB888 and/or RGB565
  - YUV 4:2:2
- **Data interface: an 8 bit parallel data interface is used when the camera is connected directly to Locosto. The frequency depends on the picture size, but is limited to 48 MHz.**
- **Tristate capability (according to pin mux configuration).**
- **Control interface: the control commands will be send through I2C in the case of a directly connected parallel camera.**
- **I/O voltage:1.8 V. In case of 2.8V I/O camera module is to use external level shifters on the board.**

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LCD REQUIREMENTS

- **LCD size: a typical LCD for the camera application will be QCIF / QCIF+ (i.e. 220x170 pixels).**
- **Data format: the LCD needs to accept data in RGB565 (two bytes) format and/or RGB888 (three bytes) format.**
- **LCD Interface: Locosto comprises an 8 bit large LCD interface, that can run at a fraction of 13 MHz in {1, 2, 4, 8}.**
- **I/O voltage: due to Locosto C027 process, Locosto LCD interface's I/O support 1.8V. The LCD component has to support 1.8V I/O for proper connection.**

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LOCOSTO-IC EXTERNAL PERIPHERALS

- Keyboard
- MCSI
- UART
- I2C
- USIM
- C-PORT
- USB

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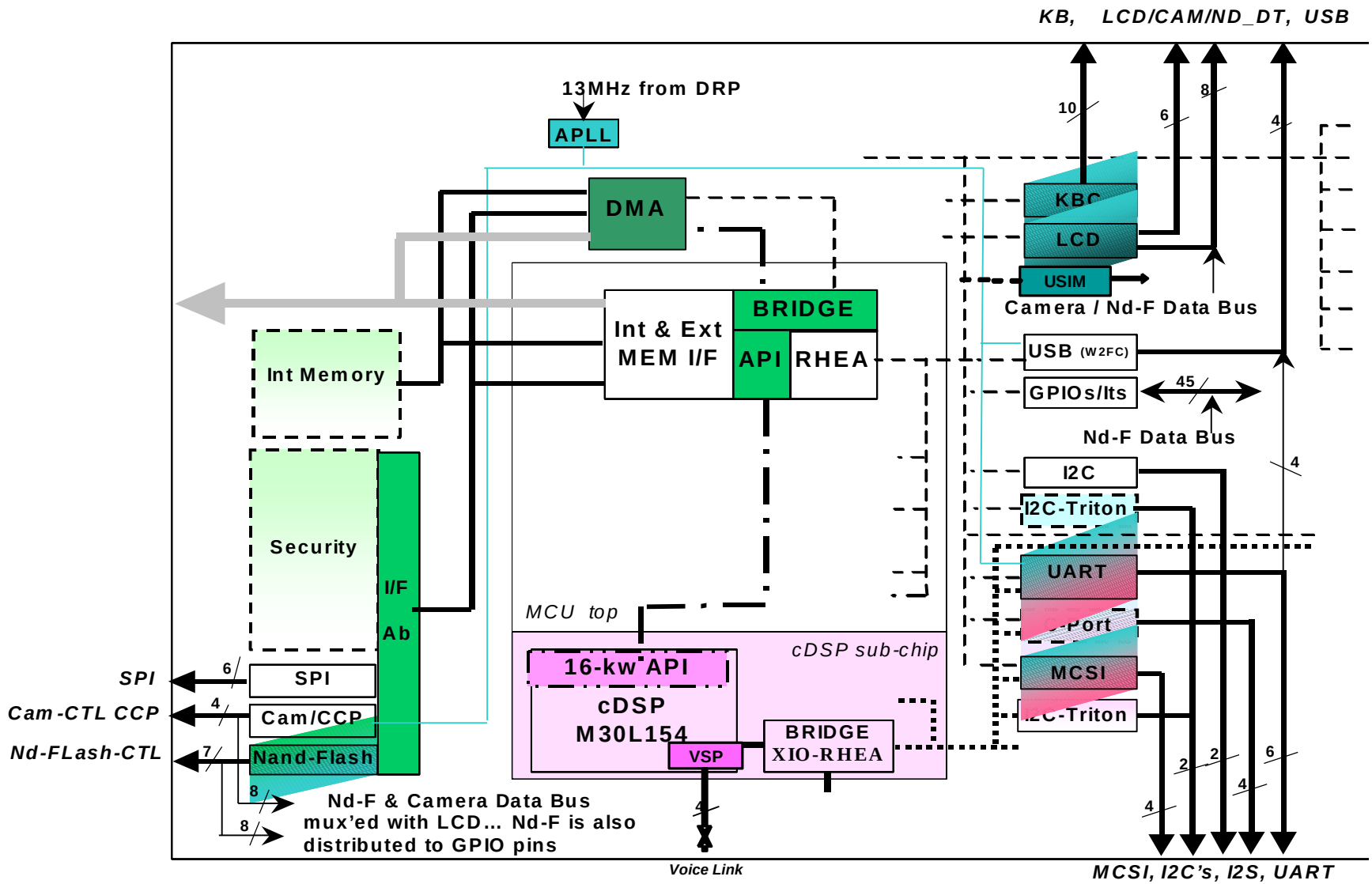
EXTERNAL I/F BLOCK DIAGRAM



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SCANNED KEYBOARD

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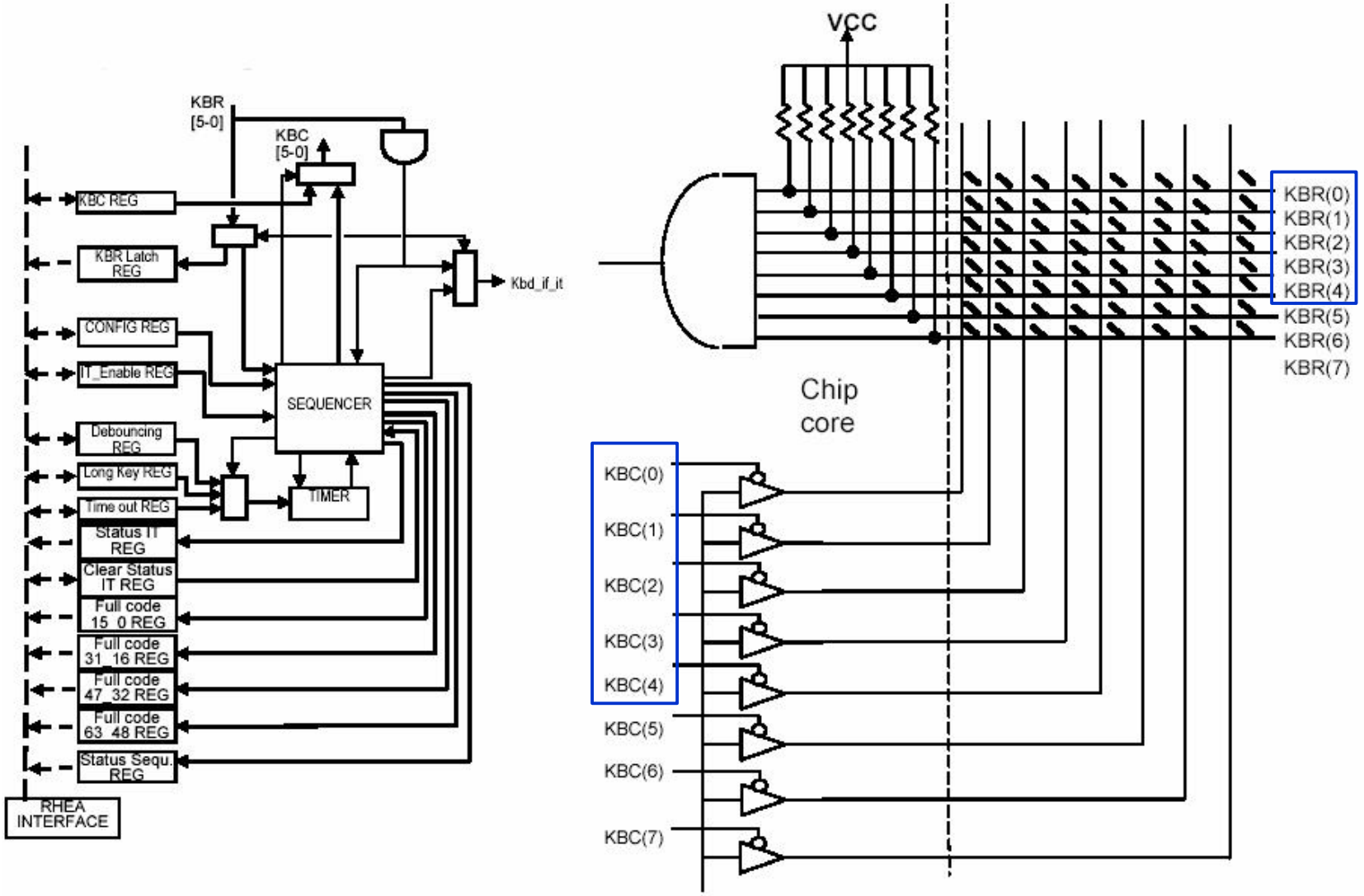
SCANNED KEYBOARD DIAGRAM



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SCANNED KEYBOARD FEATURES

- Works on 32kHz main clocks
- Debouncing time programmable
- Support of multi-configurations keyboard, up to 8 columns * 8 rows. But Locosto is only 5*5.
- Multi keys press detection and decoding (2 keys fully compliant but more than 2 with some limitations).
- Each ARM interrupt enabled or disabled by register configuration.
- Module generates an overrun if CPU reads register to late.
- Interrupts generated on level
- Each key coded on one bit in four 16 bits registers.

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MCSI
(Multi-Channel Serial Interface)

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MCSI FEATURES

- Serial Interface with a Multi-Channels transmission capability.
- Support the audio link with an external Bluetooth baseband IC device.
- All transmission parameters are configurable to cover the maximum number of operating conditions:
  - Ø MASTER or SLAVE clock control (transmission clock and frame synchronization pulse)
  - Ø Programmable transmission clock frequency from 5KHz to 6MHz (Reference clock 13MHz)
  - Ø Single (1 channel per frame) or Multi (x16) channels frame structure
  - Ø Programmable word length : 3 to 16 bits
  - Ø Full-duplex transmission
  - Ø Programmable frame configuration
  - Ø Programmable interrupts occurrence time (TX and RX)
  - Ø Error detection with interrupt generation on wrong frame length
- Support of GSM DAI operating modes.

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UART Modem / IrDA

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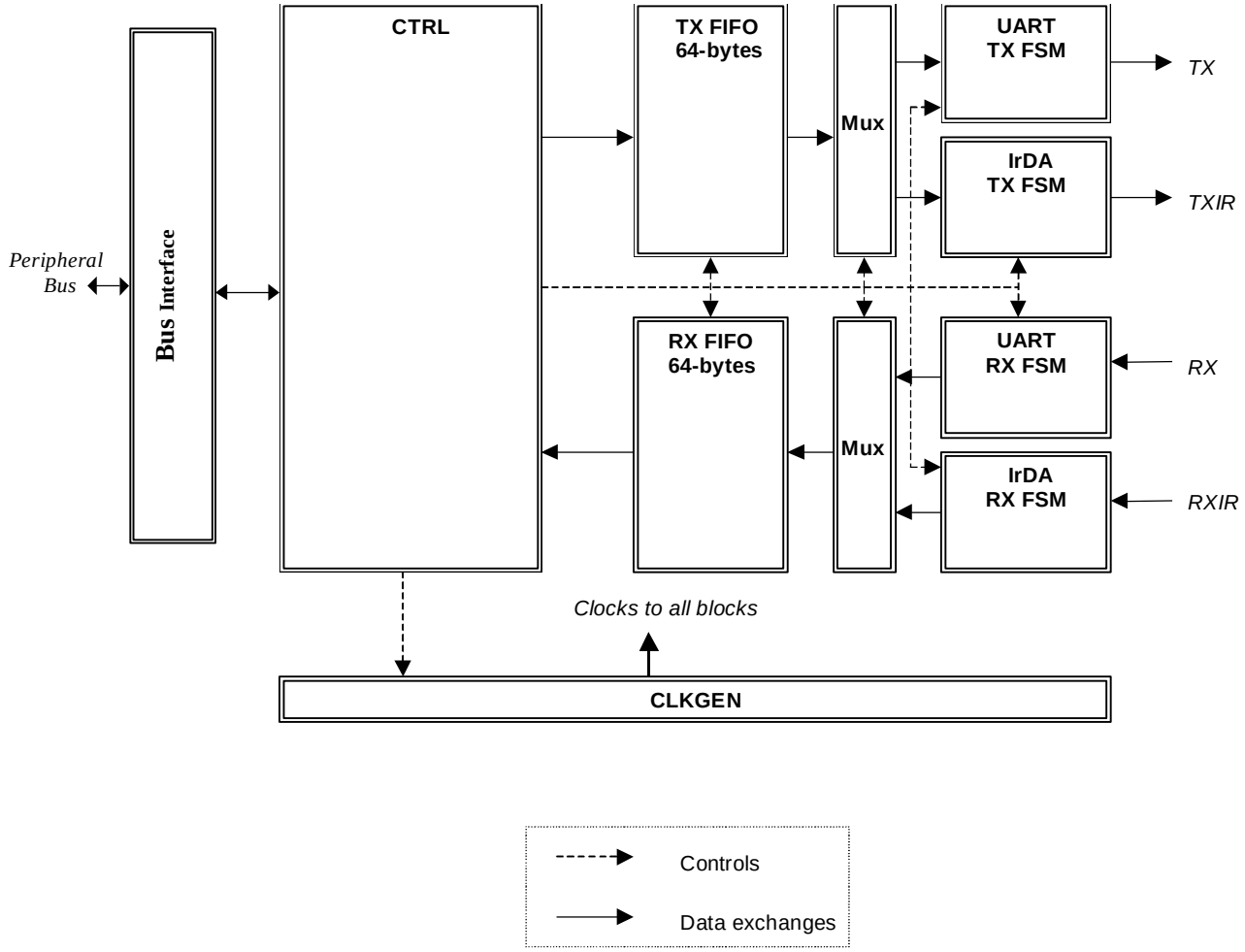
UART MODEM / IRDA BLOCK DIAGRAM



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UART MODEM / IRDA FEATURES

- ***UART Modem Functions***
  - Baud-rate from 300 bits/s up to 3.6864 Mbits/s
  - Auto-baud between 1200 bits/s and 115.2 Kbits/s
  - Software/Hardware flow control
  - Programmable serial interface characteristics

- ***IrDA Functions***
  - Slow infrared (SIR up to 115.2 KBAUD)
  - medium infrared (MIR 0.576 MBAUD & 1.152MBAUD)
  - fast infrared (FIR 4.0 MBAUD) operations (very fast infrared (VFIR) is not supported)

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LOCOSTO-IC EXTERNAL PERIPHERALS

I²C

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MULTI-MASTER I²C

- Main features of the I2C controller are:
  - Compliant to Philips I2C specification version 2.1
  - Standard (100 Kbits/s) and fast modes (400 Kbits/s)
  - 7-bit and 10-bit device addressing modes
  - H/W asserted Start/Stop conditions, Ack/Nack; S/W control for Repeated-Start
  - Multi-master Arbitration & clock synchronization
  - Built-in FIFO for buffered read or write; 2 x 16-bit word
  - 16-bit wide access to maximize bus throughput
  - Module enable/disable capability
  - Programmable clock generation
  - Two DMA channels:
    - Receive-channel: Synchronously reads received data into the FIFO
    - Transmit-channel: Writes data to be transmitted into the FIFO
  - Six interrupt sources, grouped to one CPU's IRQ-line

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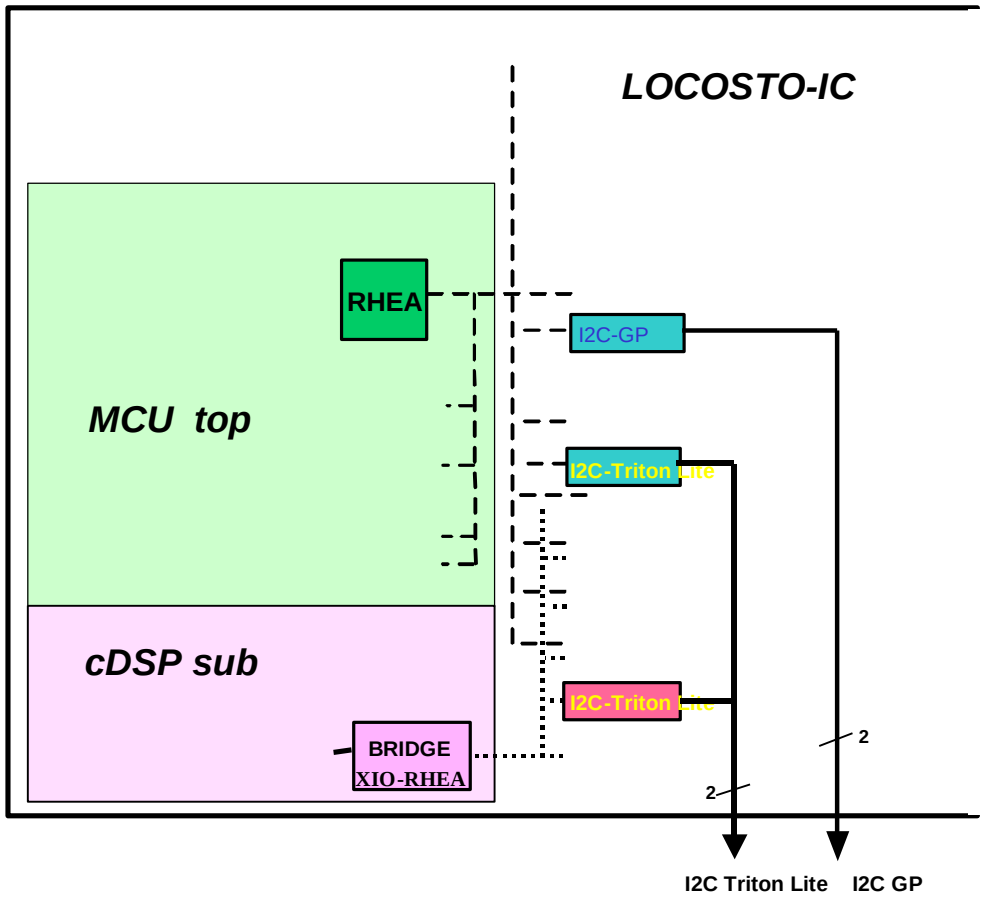
MULTI-MASTER I²C BUS



- **I2C-TriTon Lite** for controlling
  - Ø TriTon Lite-ABB
    - ü from the DSP (Voice, Stereo-Audio)
    - ü from the MCU (LDO's, MADC, RTC…)
  - Ø Additional Slave-only components.
- **I2C-GP** for multi-master system.

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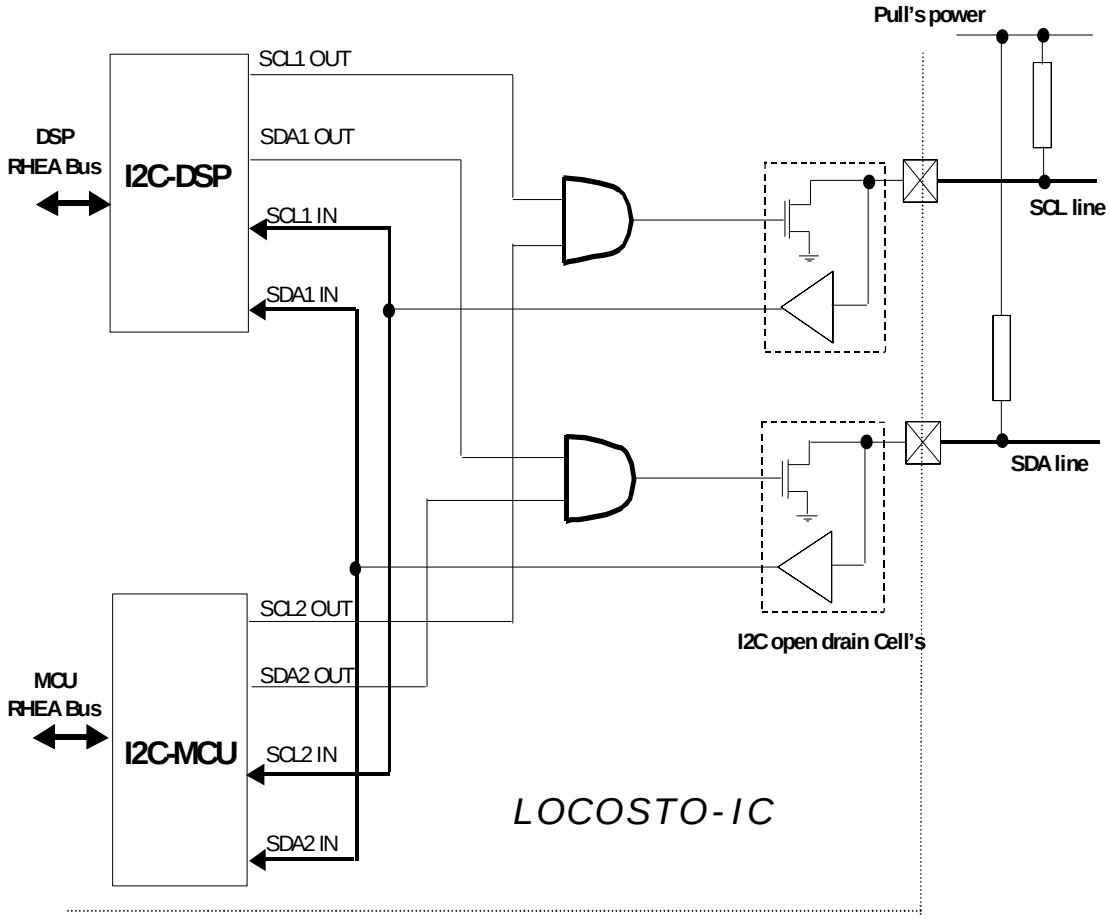
I2C TRITON Lite BUS



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USIM INTERFACE (Universal Subscriber Identity Module)

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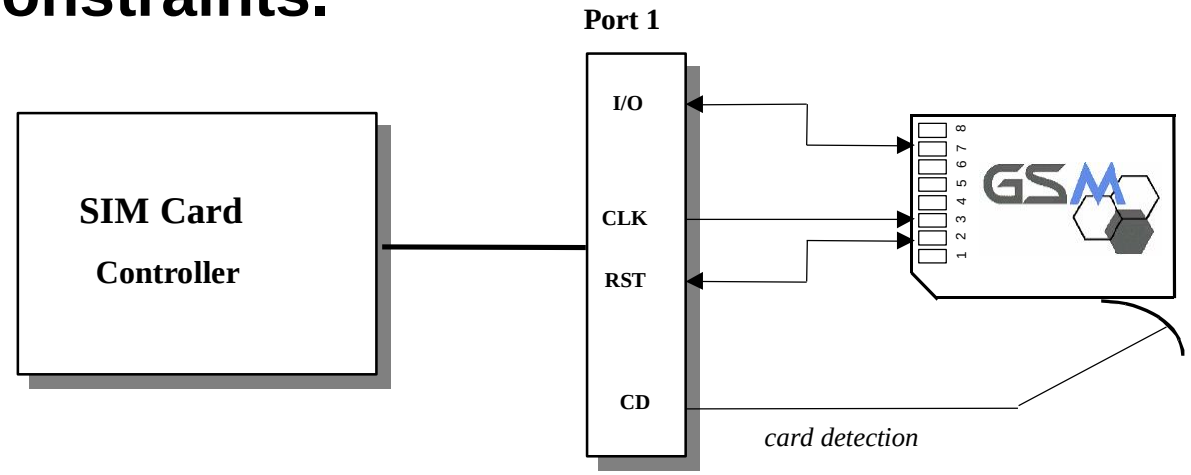
USIM

- **Designed to support many simultaneous smart-card applications such as SIM (GSM), USIM (3GPP), banking (EMV) and loyalty application.**
- **Implements:**
  - **the hardware interfaces to the Smart Card**
  - **a sequencer that manages the transmission protocols T-0 and T-1, defined in the ISO7816.3 standard, thus freeing the MCU of the real-time constraints.**



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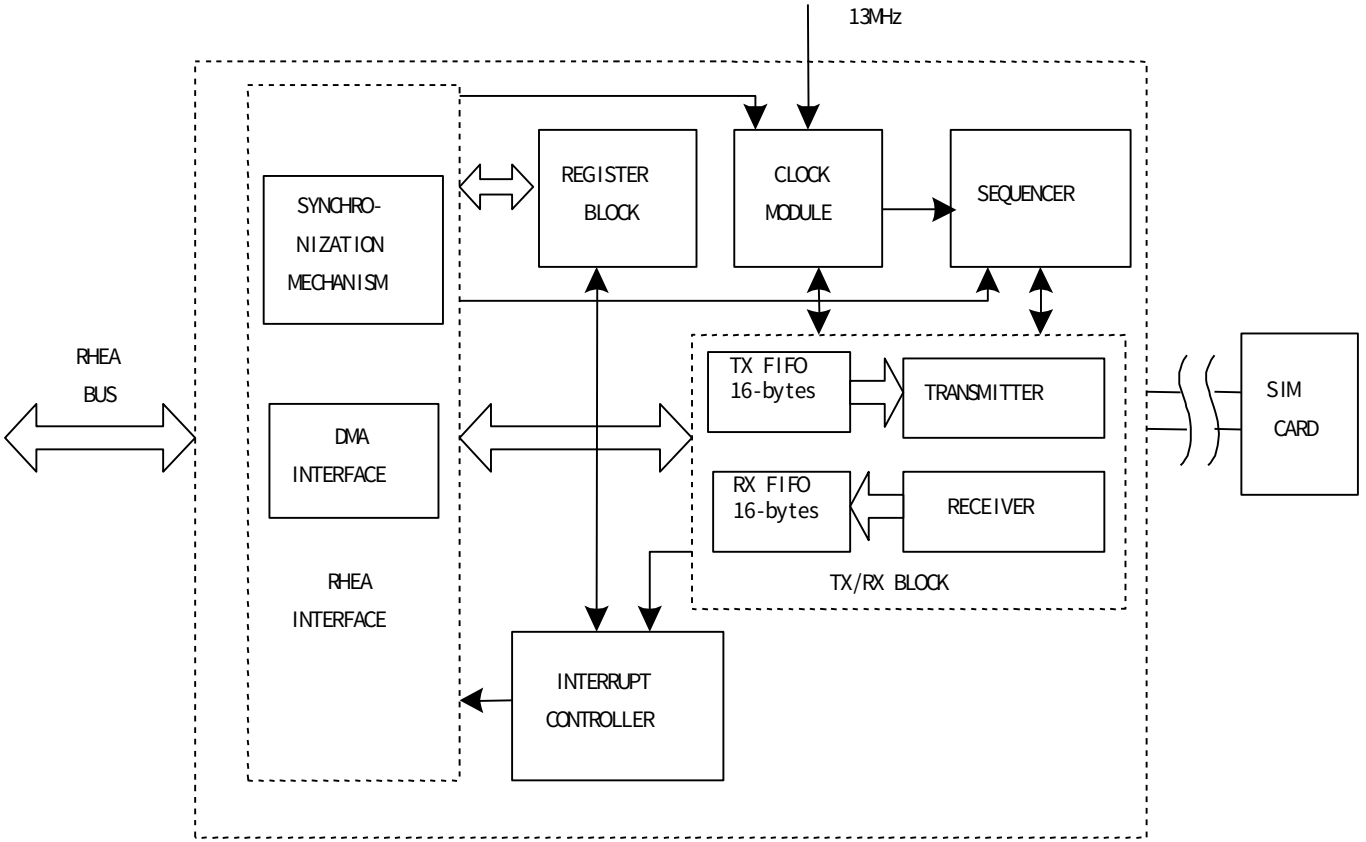
USIM BLOCK DIAGRAM



CARD PRESENCE DETECTION is done in TRITON Lite.

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C-PORT
(Codec Port Interface)

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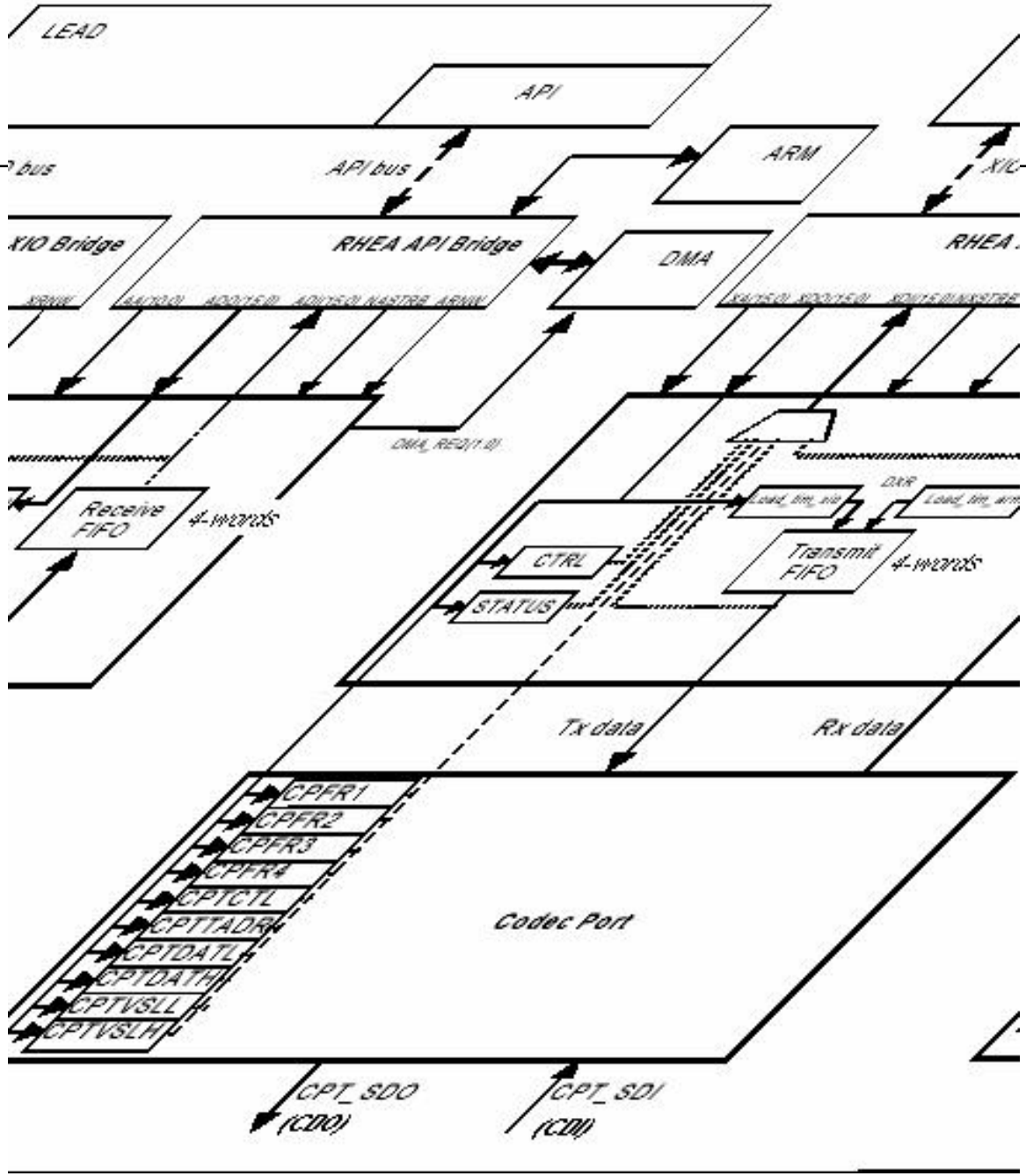

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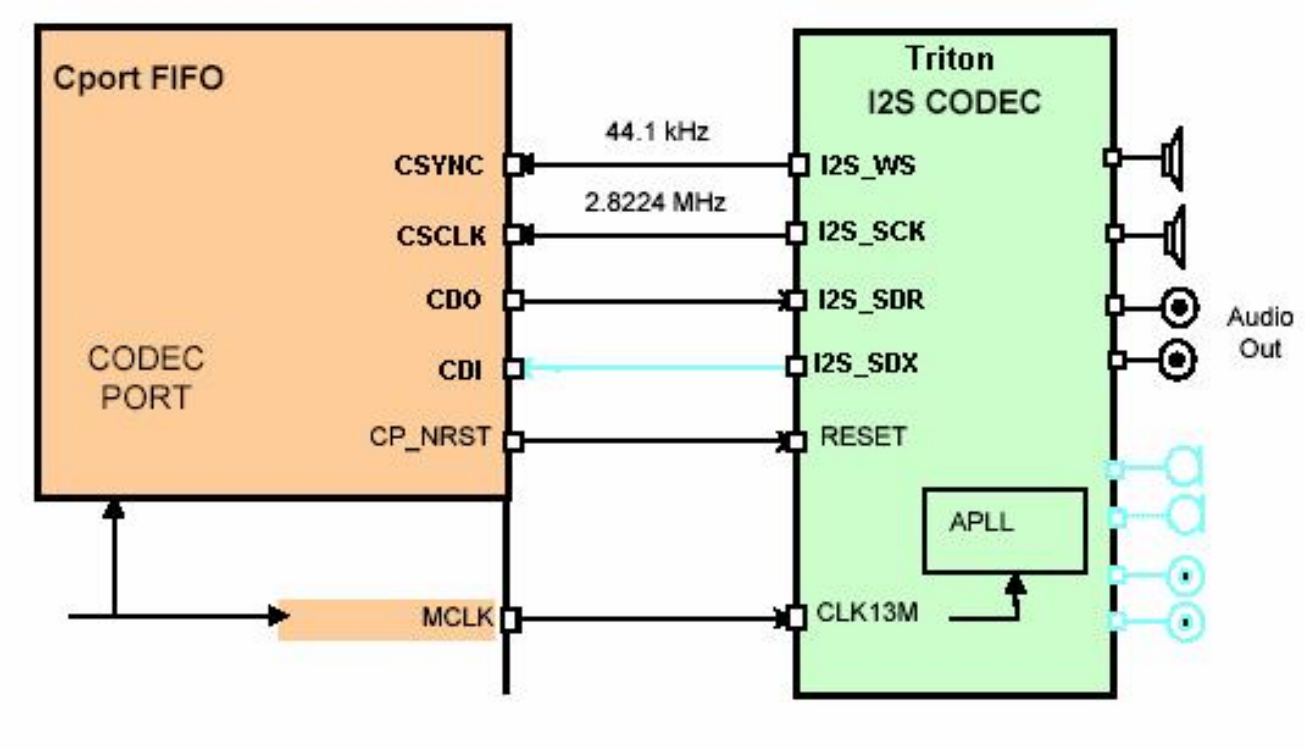
C-PORT



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EXTERNAL PERIPHERALS

USB

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USB FEATURES

- **USB_W2FC module: USB 1.1 client full speed (12Mbps)**
- **Interface between the MCU and the USB device and handles USB transactions with minimal MCU intervention**
- **Requires a 48MHz clock generated by APLL upon request**
- **Locosto chip does not integrate the transceiver (differential drivers) that are available in TriTon Lite ABB chip; the USB_W2FC interface is supplied at 1.8v.**
- **2 USB Modes**
  - Ø **DAT_SE0 for single-ended transactions with the USB controller (DBB chip) (3-pins),**
  - Ø **VP_VM for differential communications with the USB controller (4-pins).**

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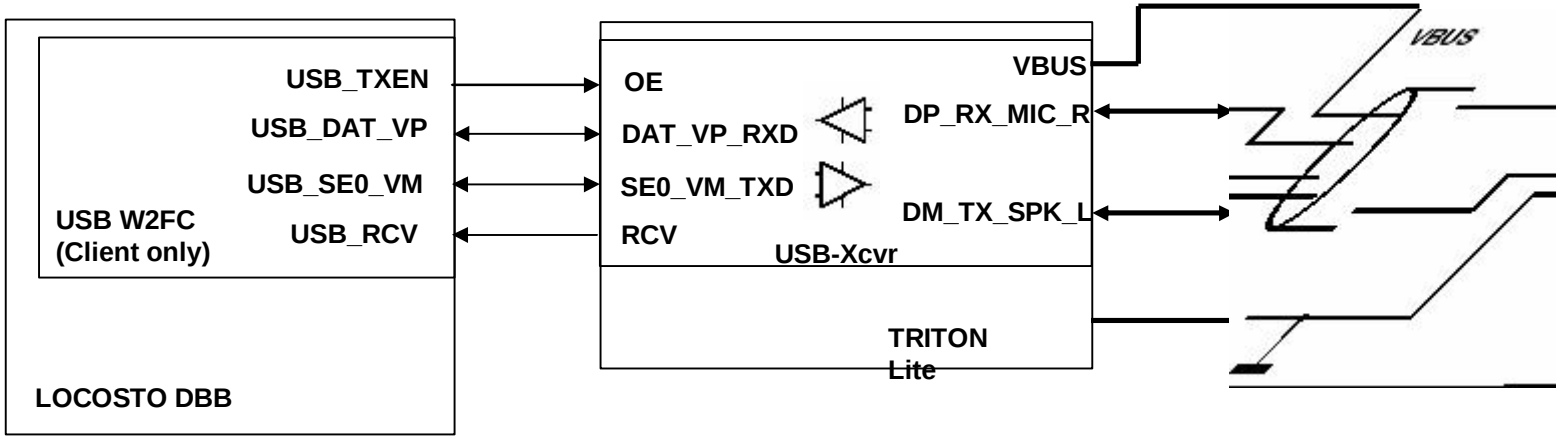
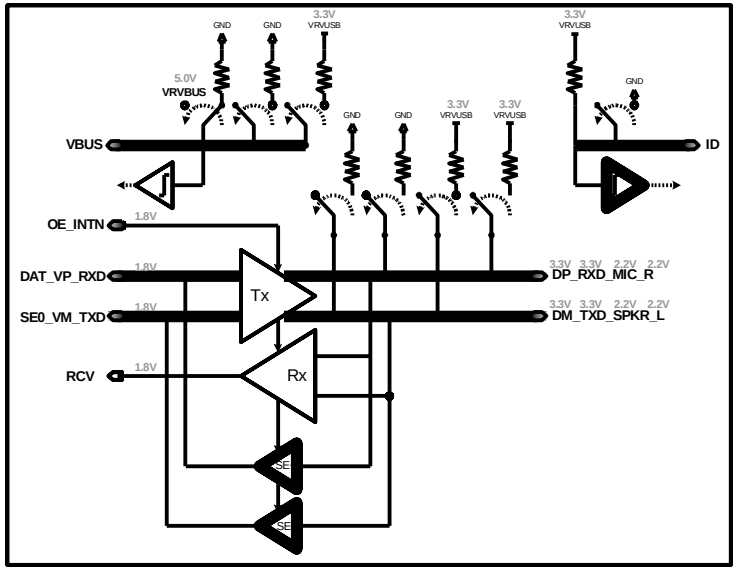
USB CONNECTIONS



MCU USB I/F: 4 pins – VDDIO power domain (1v8) – Multiplexed with UART		
USB_RCV	IN	USB Differential Receiver input; not used in 3 pins DAT_SE0 mode.
USB_SE0_VM	IN/OUT	- USB SE0 in 3 pins bi-dir DAT_SE0 mode - VM function in 4 pins bi-dir VP_VM mode
USB_DAT_VP	IN/OUT	- DAT function in 3 pins bi-dir DAT_SE0 mode - VP function in 4 pins bi-dir VP_VM mode
USB_TXEN	OUT	USB Transmit Enable



TRITON Lite USB Transceiver

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SECURE ENVIRONMENT

SECURE ENVIRONMENT

- Secure hardware
- PRRM (Protected Resource Reset Management)
- Cryptography
- EMPU (Enhanced Memory Protection Unit)

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GENERAL INTRODUCTION ON SECURITY

What do we try to achieve with a secure system?

- Protection against firmware Modification
- Secure Download of the firmware
- Protection Against Cloning Between Mobile
- Secure Confidential Data Encryption/Decryption
- Protection Against Reverse Engineering

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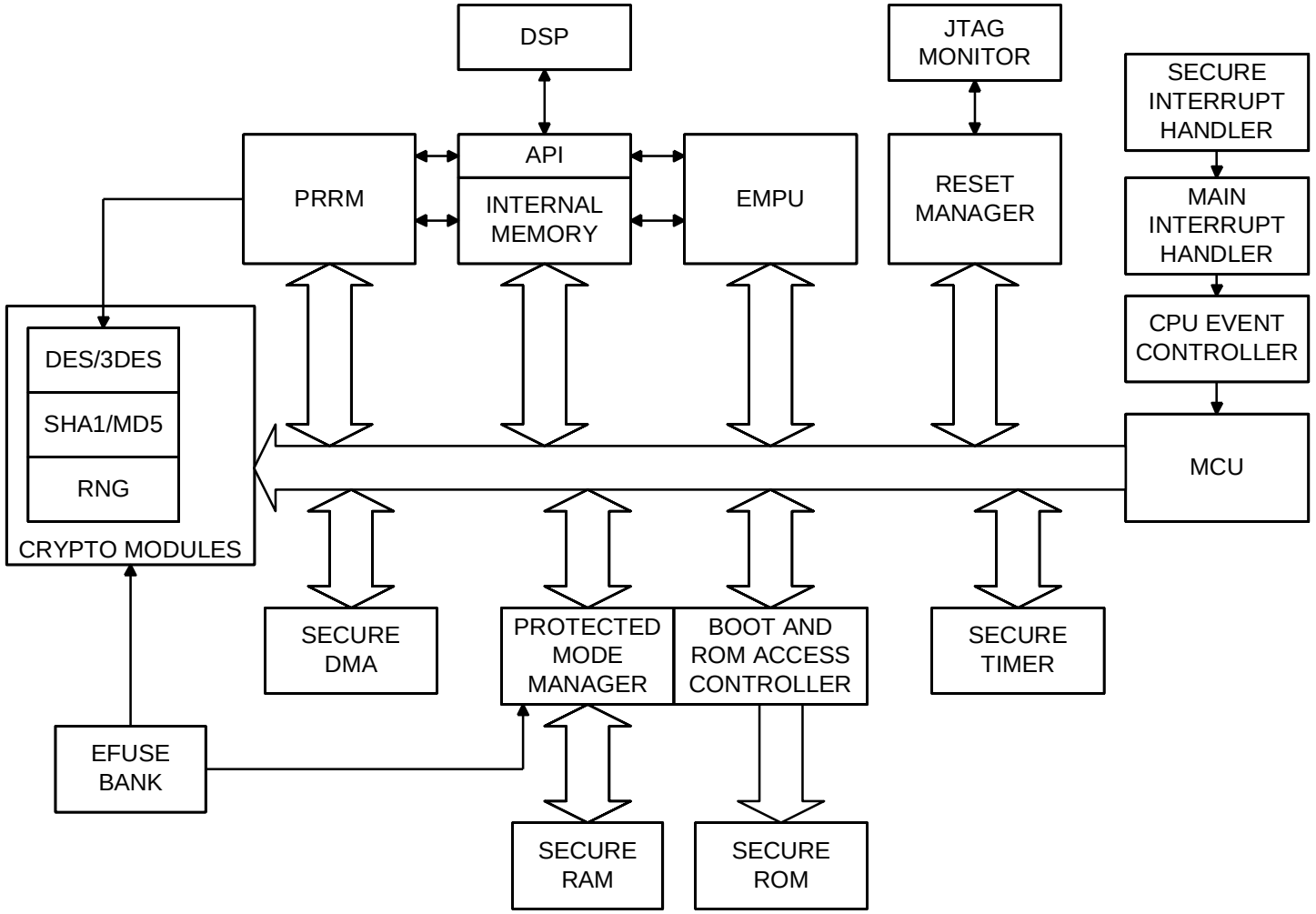
SECURE ENVIRONMENT ARCHITECTURE



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SECURE ENVIRONMENT

SECURE HARDWARE

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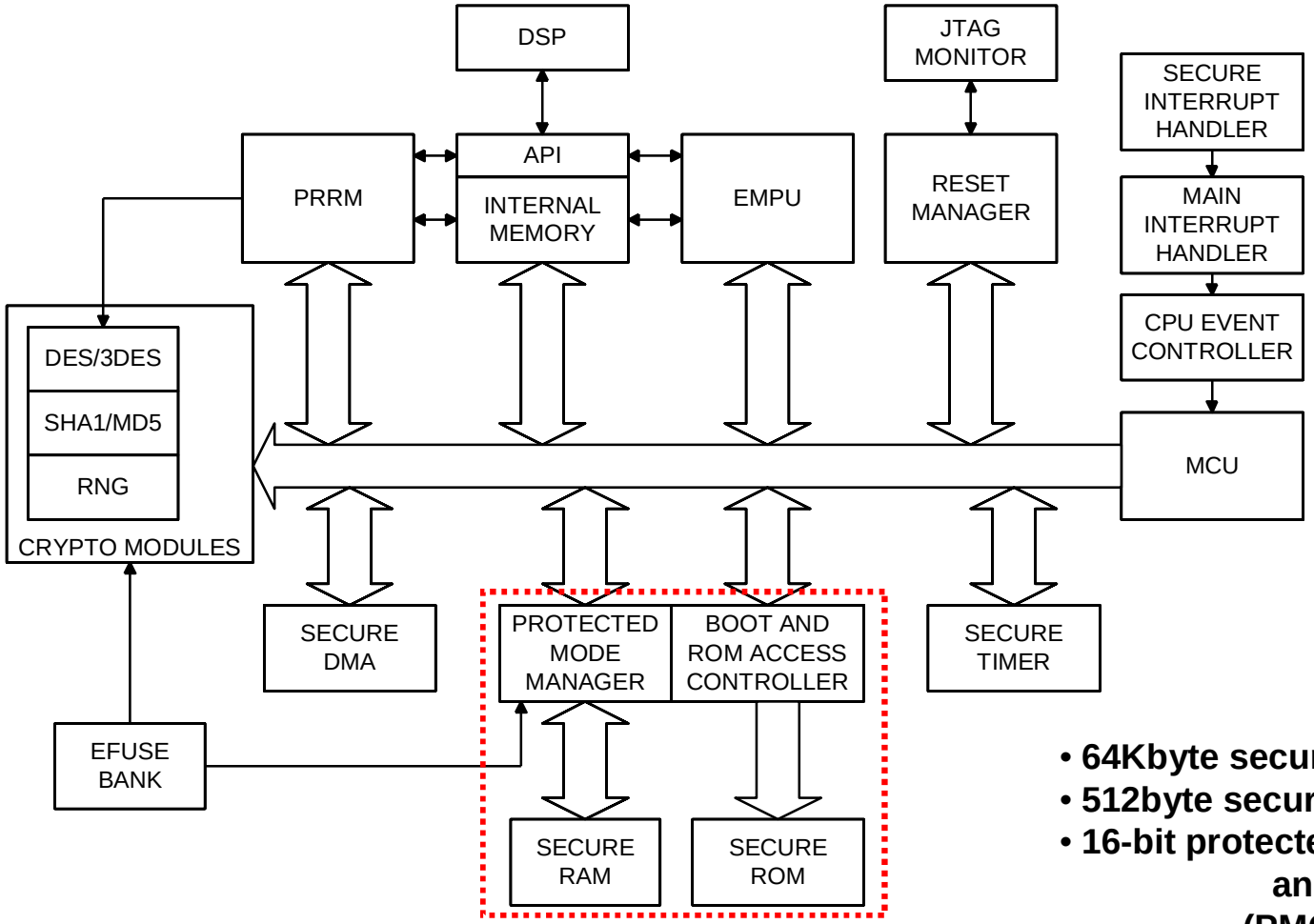
SECURE HARDWARE



- **64Kbyte secure boot ROM**
- **512byte secure RAM**
- **16-bit protected mode control and status register (PMCTLST register).**
- **Secure Access Controller**

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SECURE BOOT ROM (Overview)

- **Content (64kBytes):**
- **Secure ROM content cannot be read/dumped**
- **Any access to the secure code from outside the Secure-ROM or in emulation is denied.**
- **It cannot be interrupted or bypassed.**
- **It is not dependant on the OS.**

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SECURE RAM

- 512 bytes (128x32-bit)
- Dedicated SRAM used for secure context stack operations and short data/variables storage.
- DMA accesses are not serviced.
- Reserved for secure-ROM code execution
- Any access from outside the Secure-ROM code or in emulation is denied.
- Its content is cleared upon reset event

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SECURE ENVIRONMENT

PRRM

Protected Resource Reset Management

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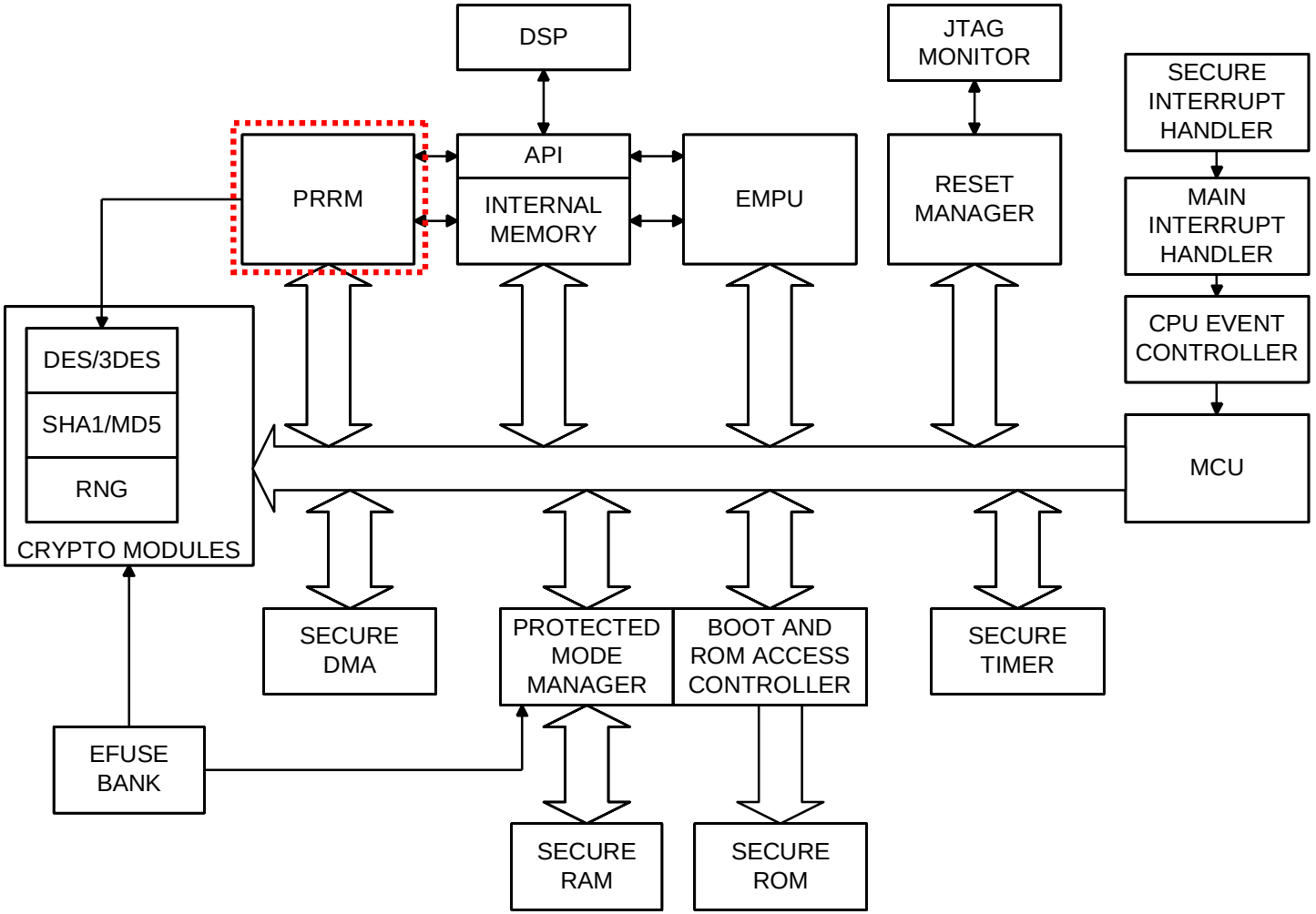
PRRM



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PRRM FEATURES

- The PRRM - “reset module” - can perform a reset on:
  - Ø the internal memory space,
  - Ø the API memory space,
  - Ø the protected resources (Secure RAM, RNG, DES, 3DES, …).
- It also can generate:
  - Ø a Global chip reset,
  - Ø a protected resource reset,
  - Ø an opcode prefetch abort.
- The PRRM reset is initiated on different reset sources:
  - Ø Global chip reset request,
  - Ø Protected resource reset request,
  - Ø Secure watchdog timer reset request,
  - Ø Soft reset.

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SECURE ENVIRONMENT

EMPU

Enhanced Memory Protection Unit

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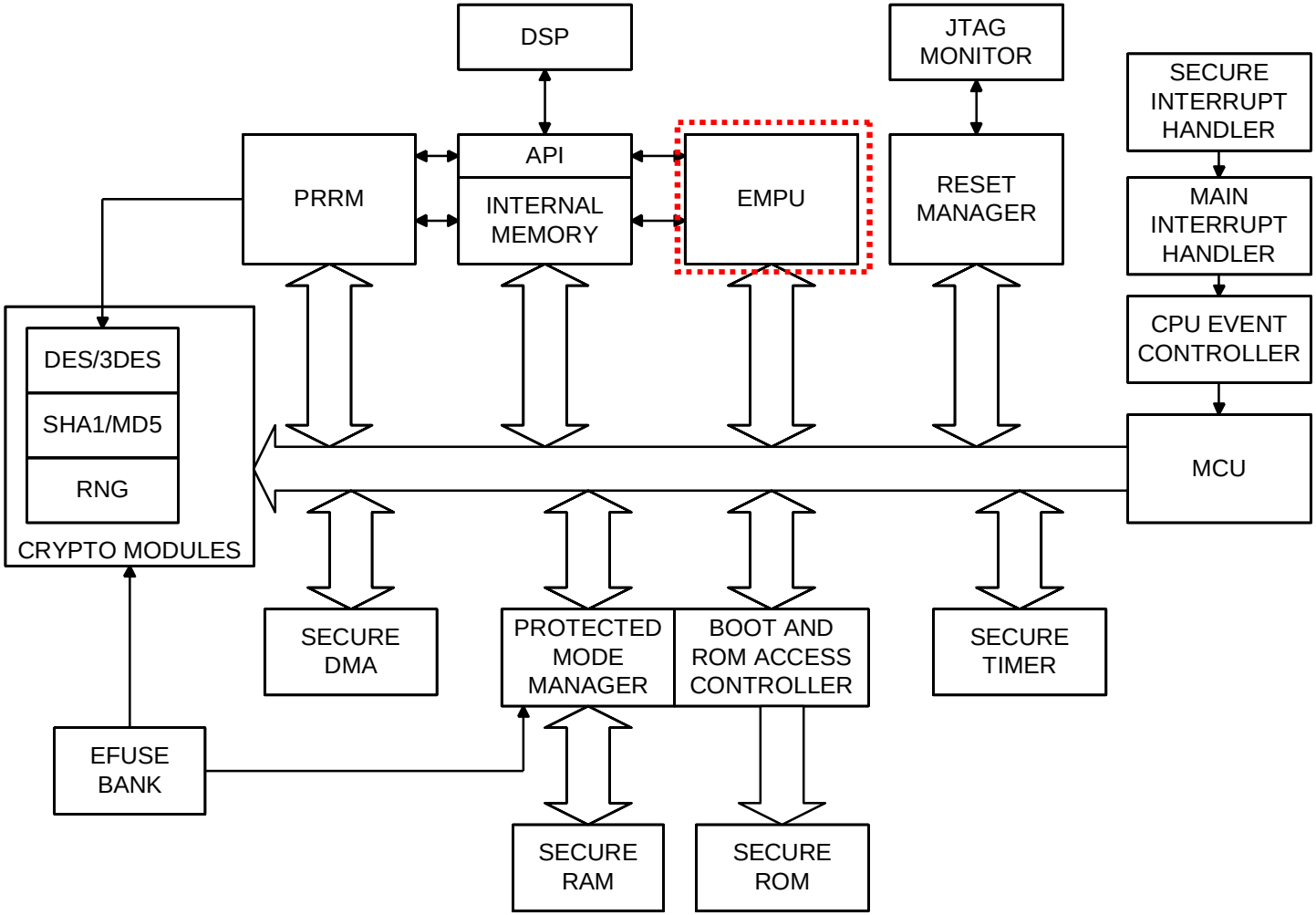

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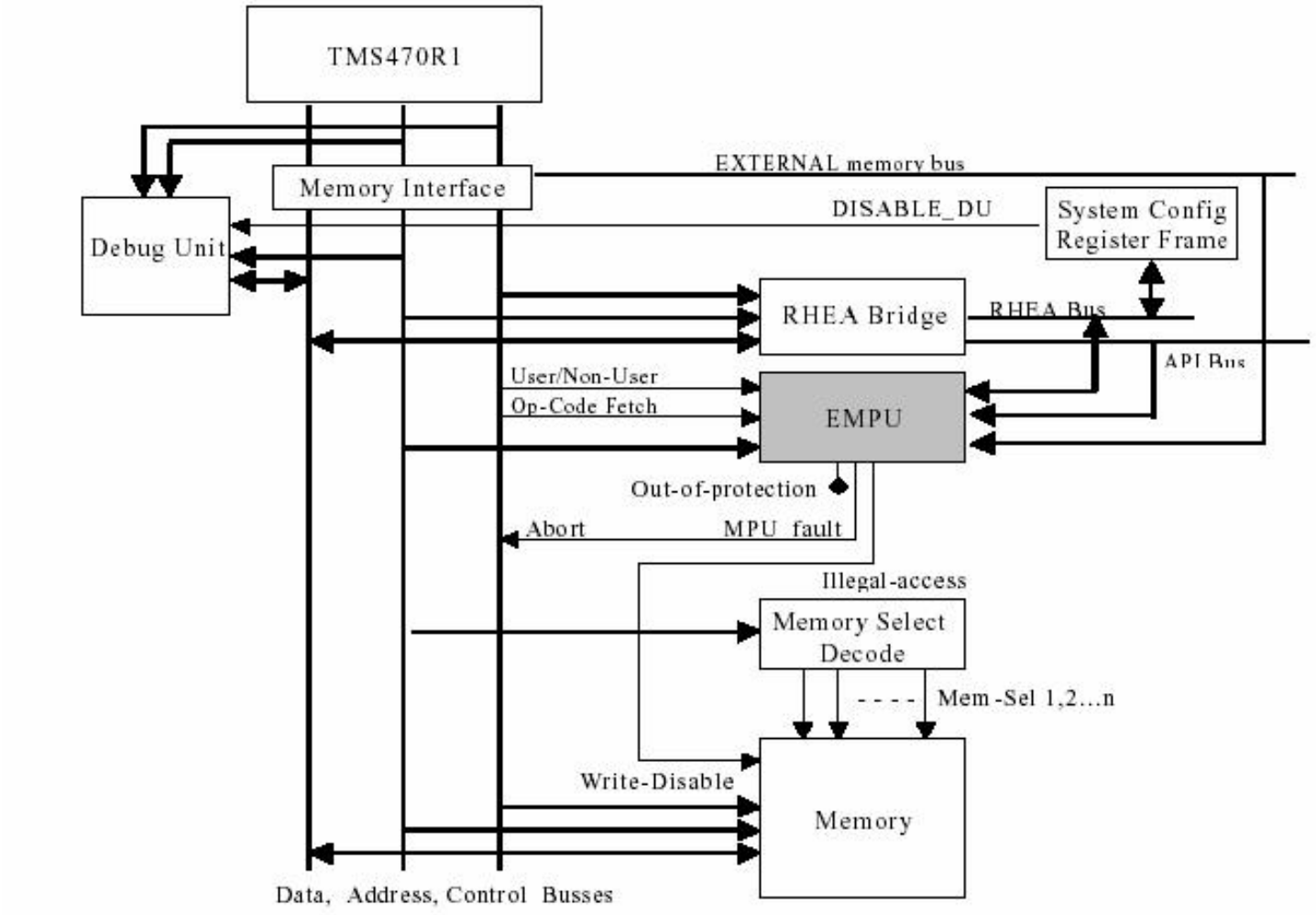

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EMPU FEATURES

- The EMPU allows defining internal-memory sub-regions, each having a separate protection attribute.
- This permits for partitioning the memory space into program instruction, system data, user data, stack …
- The address bus directly issued from the processor is monitored providing a real-time position of the memory region accessed. When a protection breach attempt occurs:
  - Ø the memory control signals are affected,
  - Ø no writing/reading into/from the memory,
  - Ø and the fault condition is indicated to the processor.
- The EMPU allows for controlling 3 different protected memory spaces shared by a Micro-controller and a Direct Memory Access (DMA):
  - Ø API memory space,
  - Ø External memory space,
  - Ø Internal memory space.

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EMPU INTERNAL MEMORY

- Up to 4 programmable protected regions within a maximum memory space of 256 k-byte
- A 64 k-byte maximum region size (256 k-byte for 4 regions).
- A minimum granularity of 8 bytes (minimum protected region size)
- 4 protection modes applied to the memory sub-region bounded by the starting/ending addresses:
  - § Non-User R/W,
  - § User Read-only,
  - § ROM,
  - § Privileged-region write
- Definition by region base address and starting/ending addresses within the protected memory region

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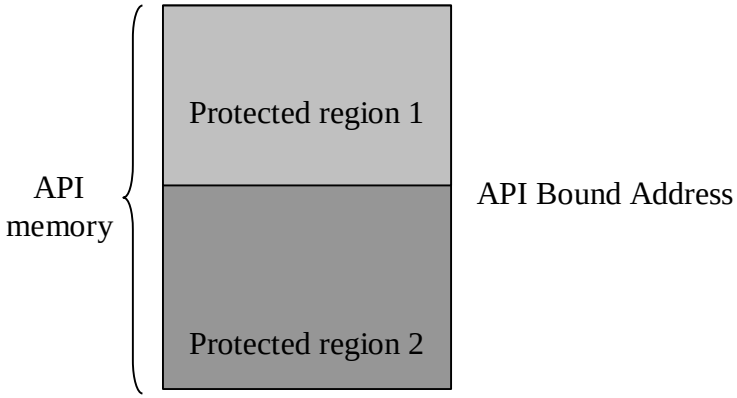
EMPU API

- 2 regions, programmable boundary API protected region
- A minimum granularity of 1 byte on the API
- 3 protection modes:
  - § Read protect,
  - § Write Protect,
  - § Read/Write protect



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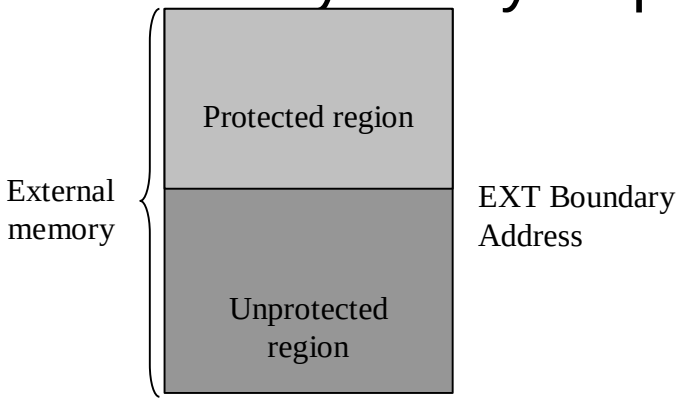
EMPU EXTERNAL MEMORY

- The protected region from the External memory base address within the system memory map to the limit of this region.
- A minimum granularity of 128 bytes on external memory
- Protection Mode enabled/disabled (protection type is internally hard coded to protected write)
- The protection enable bit is “write once” and is activated according to the External memory chip select defined in the control register. This feature allows protecting an external memory in any chip select configuration.



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EMPU

- The EMPU generates:
  - An illegal-access signal for each type of protected memory space (internal, external and API) if the application program attempts a non-authorized access to a memory region (i.e. User write access to a region programmed for User Read-only accesses).
  - A MPU-fault signal which is a logical function of the 3 protected spaces (internal, external and API) Illegal-access signals.
  - A fault indication (Illegal-access) flagged into the EMPU status register which is available to the processor for fault analyze.

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LOCOSTO-IC SECURE BOOT

LOCOSTO
VS
CALYPSO PLUS

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Making Wireless

HW DIFFERENCES

- Boot ROM size is now 64 KB as compared to 48 KB in Calypso plus.
- Only One UART Module in Locosto.
- USB Transceiver resides in Triton Lite
- Internal SRAM is reduced to 2.5 M-bit (320KB); Hence for flash programmer code, effectively only 1 M-bit of SRAM will be available (128 KB)
- Die-ID size is increased to 128 bits
- EMIF has changed from Calypso Plus – Permitting to have a maximum of 4 chip selects (CS0/1/2/3) with a maximum of 32 MB each. Also Burst mode access to external memory is added and Page mode access is removed.
- MCU Clock frequency in Locosto can go up to 104 MHz.

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