LOCOSTO PROGRAM

T3031
(Triton_Lite)
Datasheet

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1 DEVICE OVERVIEW

The T3031 (TRITON_LITE) chip is the analog and power management part of the Texas Instruments next generation Cellular System Solutions TCS2300/TCS2310. These GSM/GPRS platforms are also composed by a single chip embedding Digital Baseband and RT transceiver and offer different peripheral devices like a LCD panel, Camera, USB, Keypad, Vibrator and Bluetooth.

The purpose of T3031 device is to provide to platforms the following resources:

A power management system
Power supply resources
A voice and audio interface
A battery charger
A monitoring system
A real time clock resource
USB 2.0 Full speed transceiver with carkit detection
Three White-LEDs drivers
A vibrator driver
A SIM-Card detection system
A thermal shutdown
An I2C interface
A JTAG and boundary scan

2 PIN DIAGRAM

Pin Name	Supplies	I/O	Description	PU/PD
SIM-Card Interface (insertion / extraction detection function only) (1-pin)				
SIMDTC	VRIO/GND_PWR3	I	SIM-card insertion / extraction detection	PU/PD programmable (reg SIMDTCCTRL), PU enabled by default
Housekeeping (Monitoring ADC, M-ADC) (4-pins)				
ADCIN3	VRABB/GND_PWR5	I/O	Monitoring ADC input (# 3), plus current source (see bit THENSA in BCICTL1 register)	
ADCIN4	VRABB/GND_PWR5	I/O	Monitoring ADC input (# 4) plus current source output (Battery Type)	
ADCIN5	VRABB/GND_PWR5	I/O	Monitoring ADC input (# 5) current source output (Battery Temp)	
STARTADC	VRIO/GND_PWR3	I	Trigger to start synchronous conversion	
USB Interface (8-pins)				
OE_INTN / TEST1	VRIO/GND_PWR3	I/O	USB transceiver output enable (Input) USB transceiver interrupt line (output)	PD programmable (reg CFG_PU_PD_LSB), disabled by default, reset_off value Z
DAT_VP_RXD / TEST2	VRIO/GND_PWR3	I/O	USB driver data positive input / output UART Receive data	PD programmable (reg CFG_PU_PD_LSB), disabled by default, reset_off value Z
SE0_VM_TXD / TEST3	VRIO/GND_PWR3	I/O	USB driver data negative input / output UART Transmit data	PD programmable (reg CFG_PU_PD_LSB), disabled by default, reset_off value Z
RCV / TEST4	VRIO/GND_PWR3	I/O	USB logic data receiver output	reset_off value 0

DP_RXD_MIC_R	VRUSB/GND_PWR3(4)	I/O	USB data bus (positive terminal)	reset_off value Z
DM_TXD_SPKR_L	VRUSB/GND_PWR3(4)	I/O	USB data bus (negative terminal)	reset_off value Z
ID_USB	VRUSB/GND_PWR3(4)	I/O	USB connector identification	Reset_off Pull-up on VRRTC Pull-up on VRUSB (active mode)
VBUS	VBUS/GND_PWR3(4)	I/O	USB VBUS power supply line	reset_off value Z
Power Supply (24-pins)				
VCC1	VCC1	I	Input supply voltage for regulators	
VCC2	VCC2	I	Input supply voltage for regulators	
VCC3	VCC3	I	Input supply voltage for regulators	
VCC4	VCC4	I	Input supply voltage for regulators	
VCC5	VCC5	I	Input supply voltage for regulators	
VCC6	VCC6	I	Input supply voltage for regulators	
VRABB	VRABB/GND_PWR4	O	Output voltage for VRABB regulator	
GND_DBB	GND_ PWR3	I/O	Power regulator ground	
VRPLL	VRPLL/GND_PWR1	O	Output voltage for VRPLL regulator	
VRMEM	VRMEM/GND_ PWR3	O	Output voltage for VRMEM regulator	
VRIO	VRIO/GND_ PWR3	O	Output voltage for VRIO regulator	
VREXTH	VREXTH/GND_ PWR3	O	Output voltage for VREXTH regulator	
VREXTL	VREXTL/GND_ PWR3	O	Output voltage for VREXTL regulator	
VRRTC	VRRTC/GND_PWR1	O	Output voltage for VRRTC regulator	
VRSIM	VRSIM/GND_ PWR3	O	Output voltage for VRSIM regulator	
VRMMC	VRMMC/GND_ PWR3	O	Output voltage for VRMMC regulator	
GND_VBUS	GND_ PWR3	I/O	VBUS dedicated ground	
VRUSB	VRUSB/GND_ PWR3	O	Output voltage for VRUSB regulator	
VRWLED	VRWLED/GND_ PWR3	O	Output voltage for VRWLED regulator	
GND_PWR1	GND_PWR1	I/O	Power ground (# 1)	
GND_PWR2	GND_PWR2	I/O	Power ground (# 2)	
GND_PWR3	GND_PWR3	I/O	Power ground (# 3)	
GND_PWR4	GND_PWR4	I/O	Power ground (# 4)	
GND_PWR5	GND_PWR5	I/O	Power ground (# 5)	
Battery Charger Interface (BCI) & Control (10-bits)				
VAC	VAC/GND_PWR5	I	Battery charger input power supply	
PCHGAC	VAC/GND_PWR5	O	AC pre-charge output current	
PCHGUSB	VBUS/GND_PWR5	O	Car-kit pre-charge output current	
VCCS	VCCS/GND_PWR5	I	Charge current sense	
VBAT	VBAT/GND_PWR5	I	Main battery voltage sense	
VBATS	VCCS/GND_PWR5	I	Charge current sense	
ICTLUSB1	VBUS/GND_PWR5	O	USB external pass transistor control	
ICTLUSB2	VCCS/GND_PWR5	O	USB external pass transistor control	
ICTLAC1	VAC/GND_PWR5	O	AC external pass transistor control	
ICTLAC2	VCCS/GND_PWR5	O	AC external pass transistor control	

White-LEDs Drivers (3-pins)				
LED_A	VRWLED/GND_PWR2	I	Led A driver output (screen)	
LED_B	VRWLED/GND_PWR2	I	Led B driver output (key-pad)	
LED_C	VRWLED/GND_PWR2	I	Led C driver output (auxil-iary screen)	
Vibrator-Motor Driver (1-pin)				
VIBDR	VIBDR/GND_PWR3	O	Vibrator driver output	
Reference Voltage / Current (4-pins)				
VBG	VRABB/REFGND	O	Bandgap voltage	
IREF	VRABB/REFGND	I	Reference current genera-tion	
REFGND	REFGND	I	System reference ground	
VBACKUP	VBACKUP/GND_PWR3	I	Backup battery	
JTAG - Test (6-pins)				
TCK	VRIO/GND_PWR3	I	Scan test clock	PD programmable (reg CFG_PU_PD_LSB), enabled by default
TMS	VRIO/GND_PWR3	I	Test mode selection	PU programmable (reg CFG_PU_PD_LSB), enabled by default
TDI	VRIO/GND_PWR3	I	Scan path input	PU programmable (reg CFG_PU_PD_LSB), enabled by default
TDO	VRIO/GND_PWR3	O	Scan path output	3-state, reset value Z
TESTRESET	VRRTC/GND_PWR3	I	Input reset for test mode only	PD not programmable
TESTV	VBAT/GND_PWR5	O	LDO sense	Def. float
System Master Clocks (2-pins)				
MCLK1	VRIO/GND_PWR3	I	System clock input (from processor #1)	PD programmable (reg CFG_PU_PD_MSB), disabled by default
Control Serial Port (2-pins)				
SDA1	VRIO/GND_PWR3	I/O	I^2C # 1 bi-directional data signal	
SCL1	VRIO/GND_PWR3	I/O	I^2C # 1 bi-directional clock signal	
Boot Mode Select (1-pin)				
BM_SEL	VRRTC/GND_PWR3	I	Boot mode ('1': *Locosto* mode)	
Interrupt Handling (1-pins)				
P1_INT2	VRIO/GND_PWR3	O	Maskable interrupt to processor #1	Reset_off value 1
Power-On Reset (1-pins)				
ONNOFF	VRIO/GND_PWR3	O	Digital baseband reset (due to each switch-on)	PD not programmable
Power Control State Machine (4-pins)				
PWON	VCC2/GND_PWR3	I	External switch-on event (ON button) (with 32-kHz debouncing)	PU programmable (reg CFG_PU_PD_MSB), enabled by default
RPWON	VCC2/GND_PWR3	I	External switch-on event (Remote) (with 32-kHz debouncing)	PU programmable (reg CFG_PU_PD_MSB), enabled by default
WAKEUP1	VRIO/GND_PWR3	I	System switch-on event (processor #1)	PD programmable (reg CFG_PU_PD_MSB), disabled by default
PCLKREQ	VRIO/GND_PWR3	I	Peripheral clock request	PD programmable (reg CFG_PU_PD_MSB), enabled by default
Real Time Clock (3-pins)				
OSC32KIN	VRRTC/REFGND	I	Crystal oscillator	
OSC32KOUT	VRRTC/REFGND	O	Crystal oscillator	
CLK32KOUT	VRIO/GND_PWR3	O	32-kHz digital output clock	
Voice & Audio Resources (32-pins)				
MICIN	VRABB/REFGND	I	Microphone amplifier	

			negative input	
MICIP	VRABB/REFGND	I	Microphone amplifier positive input	
HSMIC	VRABB/REFGND	I	Headset microphone input	
MICBIAS	VRABB/REFGND	I	Microphone bias	
HSMICBIAS	VRABB/REFGND	I	Headset microphone bias	
AUXI_FMR	VRABB/REFGND	I	FM radio input (R channel) / SE Auxiliary	
FML	VRABB/REFGND	I	FM radio input (L channel)	
EARN	VRABB/GND_PWR4	O	Earphone amplifier negative output	
EARP	VRABB/GND_PWR4	O	Earphone amplifier positive output	
SPKPA	SPKVDD/SPKGND	O	8-Ω speaker amplifier positive output (A)	
SPKNA	SPKVDD/SPKGND	O	8-Ω speaker amplifier negative output (A)	
SPKPD	SPKVDD/SPKGND	O	8-Ω speaker amplifier positive output (D)	
SPKND	SPKVDD/SPKGND	O	8-Ω speaker amplifier negative output (D)	
SPKVDD	SPKVDD/SPKGND	I	8-Ω speaker amplifier power supply	
SPKGND	SPKGND	I	8-Ω speaker amplifier power ground	
HSOL	VRABB/GND_PWR4	O	Headset amplifier (left)	
HSOR	VRABB/GND_PWR4	O	Headset amplifier (right)	
HSOVMID	VRABB/GND_PWR4	O	Headset amplifier pseudo-ground	
AUDVMID	VRABB/GND_PWR4	I/O	Audio VMID filter	
FILTERAPLL	VRABB/REFGND	I/O	Audio PLL filter	
I2S_SCK	VRIO/GND_PWR3	O	Serial clock (I^2S serial port)	Reset_off value 0
I2S_SDR	VRIO/GND_PWR3	I	Serial data-in (I^2S serial port)	
I2S_SDX	VRIO/GND_PWR3	O	Serial data-out (I^2S serial port)	3-state, reset_off value Z
I2S_WS	VRIO/GND_PWR3	O	Word select (I^2S serial port)	Reset_off value 0
VSP_VCK	VRIO/GND_PWR3	O	Serial clock (VSP serial port)	3-state, reset_off value Z
VSP_VDR	VRIO/GND_PWR3	I	Serial data-in (VSP serial port)	
VSP_VDX	VRIO/GND_PWR3	O	Serial data-out (VSP serial port)	3-state, reset_off value Z
VSP_VFS	VRIO/GND_PWR3	O	Frame synchronization (VSP serial port)	3-state, reset_off value Z
General Purpose I/Os (2-pins)				
CKEN	VRIO/GND_PWR3	I/O	Clock resource enable	PD not programmable
REGEN	VCC5/GND_PWR3	I/O	External resource enable	PD not programmable
Headset Detection I/O (1-pin)				
HSDET	VBAT/GND_PWR4	I	Headset detection	PU programmable (reg CFG_PU_PD_MSB), enabled by default
Precharge Boot Mode Select (1-pin)				
BM_PRECH	VAC / GND_PWR3	I	Precharge boot mode	PU not programmable

Notes:

GND_PWR1, GND_PWR2, GND_PWR4, GND_PWR5 are connected together to build the clean ground, while GND_PWR3 is the dirty ground

Table 1 : Pin Description

3 PACKAGING INFORMATION

The T3031 chip is packaged in a MicroStar Junior Ball Grid Array (BGA) package, 0.5-mm pitch (125ZPH).

ORDERING NUMBER	VOLTAGE	T_A
T3031FZPH (R)	- 0.3 V to 7 V	- 30°C to 85°C

Table 2 : Operating Temperature

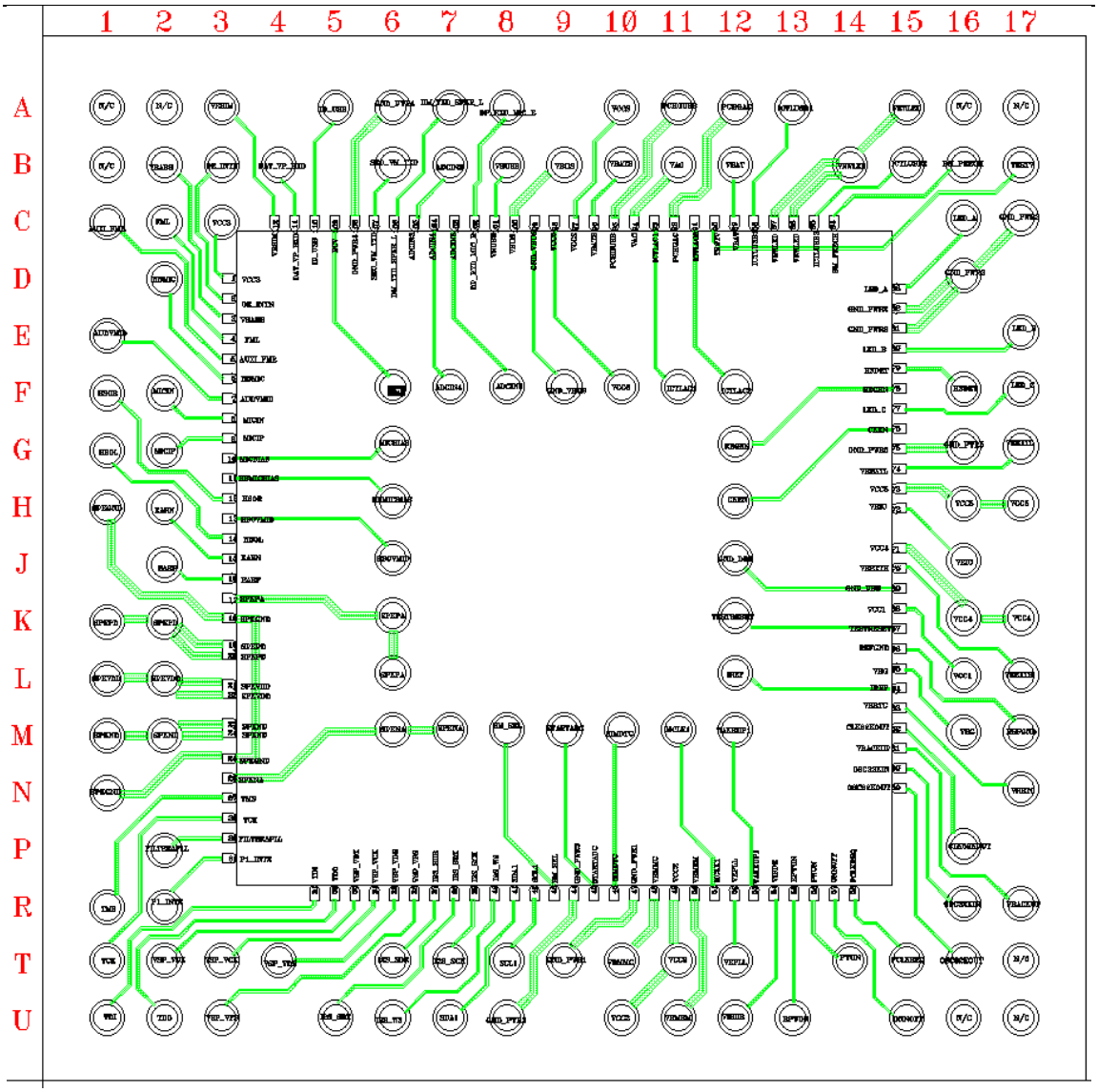


Figure 1 : Package of Triton_Lite

Dissipation rating table for a maximum T_J = 125°C (Model : Free air)					
Package	T_A < 30°C Power rating	Thermal resistance J-to-A Above T_A = 30°C	T_A = 50°C Power rating	T_A = 70°C Power rating	T_A = 85°C Power rating
125-ZPH	2.14W	44.3°C/W (2S2P)	1.69W	1.24W	0.90W

Note: The power dissipation of T3031 is strongly dependent on external current requirements, most of the overall power consumption of this device is due to the embedded regulators. If all the regulators are asked for the maximum current at the same time, the 125-ZPH package is not capable to dissipate the total power dissipation. Thus, the platform software must be capable to avoid a critical current requirement for T3031 device.
In addition, T3031 includes a over-temperature protection system that limits the on-chip junction temperature at 145°C nominal: if this threshold is overcome, T3031asks to the software close non-critical system applications or to limit their current requirements.

Table 2 : Dissipation Rating Table (for $T_{J\text{-}MAX}$ = 125°C)

Table 3 : Signal Name by Ball Number

Row	I/O name
A	**[1-17]**
A1	N/C
A2	N/C
A3	VRSIM
A4	-
A5	ID_USB
A6	GND_PWR4
A7	DM_TXD_SPKR_L
A8	DP_RXD_MIC_R
A9	-
A10	VCCS
A11	PCHGUSB
A12	PCHGAC
A13	ICTLUSB1
A14	-
A15	VRWLED
A16	N/C
A17	N/C

B	[1-17]
B1	N/C
B2	VRABB
B3	OE_INTN
B4	DAT_VP_RXD
B5	-
B6	SE0_VM_TXD
B7	ADCIN3
B8	VRUSB
B9	VBUS
B10	VBATS
B11	VAC
B12	VBAT
B13	-
B14	VRWLED
B15	ICTLUSB2
B16	BM_PRECH
B17	TESTV

C	[1-17]
C1	AUXI_FMR
C2	FML
C3	VCC3
C4	-
C5	-
C6	-
C7	-
C8	-
C9	-
C10	-
C11	-
C12	-
C13	-
C14	-
C15	-
C16	LED_A
C17	GND_PWR2

D	[1-17]
D1	-
D2	HSMIC
D3	-
D4	-
D5	-
D6	-
D7	-
D8	-
D9	-
D10	-
D11	-
D12	-
D13	-
D14	-
D15	-
D16	GND_PWR2
D17	-

E	[1-17]
E1	AUDVMID
E2	-
E3	-
E4	-
E5	-
E6	-
E7	-
E8	-
E9	-
E10	-
E11	-
E12	-
E13	-
E14	-
E15	-
E16	-
E17	LED_B

F	[1-17]
F1	HSOR
F2	MICIN
F3	-
F4	-
F5	-
F6	RCV
F7	ADCIN4
F8	ADCIN5
F9	GND_VBUS
F10	VCC6
F11	ICTLAC1
F12	ICTLAC2
F13	-
F14	-
F15	-
F16	HSDET
F17	LED_C

G	[1-17]
G1	HSOL
G2	MICIP
G3	-
G4	-
G5	-
G6	MICBIAS
G7	-
G8	-
G9	-
G10	-
G11	-
G12	REGEN
G13	-
G14	-
G15	-
G16	GND_PWR5
G17	VREXTL

H	[1-17]
H1	SPKGND
H2	EARN
H3	-
H4	-
H5	-
H6	HSMICBIAS
H7	-
H8	-
H9	-

H10	-
H11	-
H12	CKEN
H13	-
H14	-
H15	-
H16	VCC5
H17	VCC5

J	[1-17]
J1	-
J2	EARP
J3	-
J4	-
J5	-
J6	HSOVMID
J7	-
J8	-
J9	-
J10	-
J11	-
J12	GND_DBB
J13	-
J14	-
J15	-
J16	VRIO
J17	-

K	[1-17]
K1	SPKPD
K2	SPKPD
K3	-
K4	-
K5	-
K6	SPKPA
K7	-
K8	-
K9	-
K10	-
K11	-
K12	TESTRESET
K13	-
K14	-
K15	-
K16	VCC4
K17	VCC4

L	[1-17]
L1	SPKVDD
L2	SPKVDD
L3	-
L4	-
L5	-
L6	SPKPA
L7	-
L8	-
L9	-
L10	-
L11	-
L12	IREF
L13	-
L14	-
L15	-
L16	VCC1
L17	VREXTH

M	[1-17]
M1	SPKND
M2	SPKND
M3	-
M4	-
M5	-
M6	SPKNA
M7	SPKNA
M8	BM_SEL
M9	STARTADC
M10	SIMDTC
M11	MCLK1
M12	WAKEUP1
M13	-
M14	-
M15	-
M16	VBG
M17	REFGND

N	[1-17]
N1	SPKGND
N2	-
N3	-
N4	-
N5	-
N6	-
N7	-
N8	-
N9	-
N10	-
N11	-
N12	-
N13	-
N14	-
N15	-
N16	-
N17	VRRTC

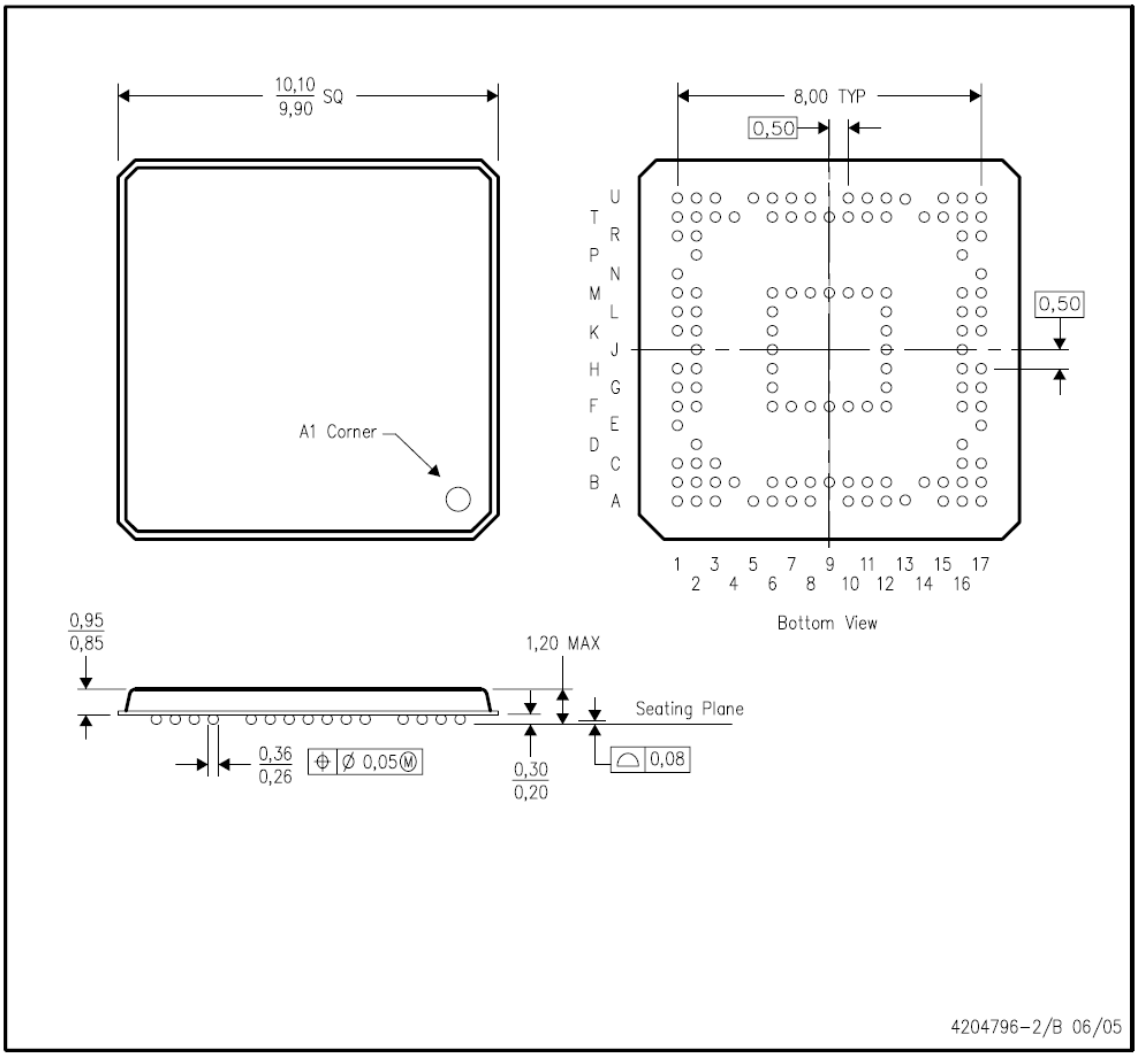
P	[1-17]
P1	-
P2	FILTERAPLL
P3	-
P4	-
P5	-
P6	-
P7	-
P8	-
P9	-
P10	-
P11	-
P12	-
P13	-
P14	-
P15	-
P16	CLK32KOUT
P17	-

R	[1-17]
R1	TMS
R2	P1_INT2
R3	-
R4	-
R5	-
R6	-
R7	-
R8	-
R9	-
R10	-
R11	-
R12	-
R13	-
R14	-
R15	-
R16	OSC32KIN
R17	VBACKUP

T	[1-17]
T1	TCK
T2	VSP_VDX
T3	VSP_VCK
T4	VSP_VDR
T5	-
T6	I2S_SDR
T7	I2S_SCK
T8	SCL1
T9	GND_PWR1
T10	VRMMC
T11	VCC2
T12	VRPLL
T13	-
T14	PWON
T15	PCLKREQ
T16	OSC32KOUT
T17	N/C

U	[1-17]
U1	TDI
U2	TDO
U3	VSP_VFS
U4	-
U5	I2S_SDX
U6	I2S_WS
U7	SDA1
U8	GND_PWR3
U9	-
U10	VCC2
U11	VRMEM
U12	VIBDR
U13	RPWON
U14	-
U15	ONNOFF
U16	N/C
U17	N/C

ZPH (S–PBGA–N125) **PLASTIC BALL GRID ARRAY**



NOTE: All the dimensions are in millimeter.

Figure 2 : Mechanical Dimensions for the ZPH Package

The T3031 device meets Texas Instruments standard requirements relative to the electrostatic discharge sensitivity (ESD).

The following list details the TWL3031 ESD performance relative to TI requirements:

ESD Method	Standard Reference	TWL3031 Performance	TI Standard Requirements
Human body model	EIA/JEDEC22-A114	2000 V	2000 V
Charge device model	EIA/JEDEC22-C101	500V	500V

4 PADS ELECTRICAL CHARACTERISTICS

Pad name	PU / PD	Min value (uA)	Typ value (uA)	Max value (uA)	Power domain
SIMDTC (PU)	PU / PD (programmable)	-10	-4.2	-2	VRIO
SIMDTC (PD)		2	4.5	10	
MCLK1	PD (programmable)	2	4.5	10	VRIO
OE_INTN	PD (programmable)	2	4.5	10	VRIO
DAT_VP_RXD	PD (programmable)	2	4.5	10	VRIO
SE0_VM_TXD	PD (programmable)	2	4.5	10	VRIO
TCK	PD (programmable)	2	4.5	10	VRIO
TMS	PU (programmable)	-10	-4.2	-2	VRIO
TDI	PU (programmable)	-10	-4.2	-2	VRIO
TESTRESET	PD	2	4.5	10	VRRTC
WAKEUP1	PD (programmable)	2	4.5	10	VRIO
PCLKREQ	PD (programmable)	2	4.5	10	VRIO
RPWON	PU (programmable)	-40	-31	-15	VBAT
PWON	PU (programmable)	-40	-31	-15	VBAT
HSDET	PU (programmable)	-40	-31	-15	VBAT

Table 4 : PD/PU current values

Digital inputs

PARAMETER	MIN	TYP	MAX	UNITS
pd7bufdincdm				
Related I/O's : HSDET, PWON, RPWON				
Low level input voltage VIL related to VBAT			0.3 VBAT	V
High level input voltage VIH related to VBAT	0.7 VBAT			V
pad3bufdincdm, ***pad3bufdiocdm2_inHF***				
Related I/O's : BM_SEL, STARTADC, SIMDTC, MCLK1, WAKEUP1, PCLKREQ, TESTRESET, TMS, TCK, TDI, VSP_VDR, I2S_SDR, OE_INTN, SE0_VM_TXD, RCV, DAT_VP_RXD				
Low level input voltage VIL related to VRIO or VRRTC			0.35 VR	V
High level input voltage VIH related to VRIO or VRRTC	0.65 VR			V
pd3bufdiocdm2i2cod (input)				
Related I/O's : SDA1, SCL1				
Low level input voltage VIL related to VRIO			0.3 VRIO	V
High level input voltage VIH related to VRIO	0.7 VRIO			V

Digital outputs

PARAMETER	MIN	TYP	MAX	UNITS
pad7budout				
Related I/O's : REGEN				
Low level input voltage VOL (I_{OL} = 10 uA)			0.3	V
High level input voltage VOH (I_{OH} = 10 uA)	0.8 VBAT			V
pd3bufdoutrisg_HF, ***pd3bufdout***, ***pad3bufdiocdm2_HF***				
Related I/O's : OE_INTN, SE0_VM_TXD, RCV, DAT_VP_RXD, CKEN, CLK32KOUT, ONNOFF, I2S_SDX, I2S_SCK, I2S_WS, VSP_FS, VSP_VDX, VSP_VCK, TDO, P1_INT2				
Low level input voltage VOL related to VRIO or VRRTC (I_{OL} = 2 mA)			0.3 VR	V
High level input voltage VOH related to VRIO or VRRTC (I_{OH} = 2 mA)	0.7 VR			V
pd3bufdiocdm2i2cod (output)				
Related I/O's : SDA1, SCL1				
Low level output voltage VOL related to VRIO @ 3mA (sink current)			0.2 VRIO	V
Output current			3	mA

Note: (1) VR = VRRTC, VRIO domains

Table 5 : PAD electrical characteristics

5 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE

Supply voltage range VBAT, VBACKUP …….……..…….…..... -0.3 V to 7 V

Supply voltage range VCHG…….……..…….…..... -0.3 V to 20 V

Supply voltage range VBUS…….……..…….…..... -0.3 V to 6 V

Voltage on any input……..-0.3 V to VDD +0.3 V

Peak output current on the VRUSB terminal…….……..…….…..... 15 mA

Peak output current on the VRWLED terminal…….……..……20 mA

Peak output current on the VRPLL terminal…….……..……10 mA

Peak output current on the VRABB terminal…….……..…….……80 mA

Peak output current on the VRRTC terminal…….……..……20 mA

Peak output current on the VREXTH terminal…….……..…200 mA

Peak output current on the VREXTL terminal…….……..……200 mA

Peak output current on the VRMMC terminal…….……..……100 mA

Peak output current on the VRSIM terminal…….……..……...15 mA

.

Peak output current on the VRIO terminal…….……..…….200 mA

Peak output current on the VRMEM terminal…….……..…….200 mA

Peak output current on the VCHG terminal…….……..…….200 mA

Peak output current on all other terminals…….…... -5 to 5 mA

Free-air temperature range…….…… -30ºC to 85ºC

Maximum junction temperature T_J …….……..……150ºC

Storage temperature range…….…….. -65ºC to 150ºC

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PARAMETER	MIN	TYP	MAX	UNIT
Main battery supply voltage In regulation, SPKVDD	3		5.5	V
Backup battery supply voltage VBACKUP, Main battery connected on VBACKUP			5.5	V
Battery charger supply voltage VCHG	4.8		20	V

Table 6 : Recommended operating conditions

6 FUNCTIONAL BLOCK DIAGRAM

This section describes the functional blocks embedded in the T3031 device.

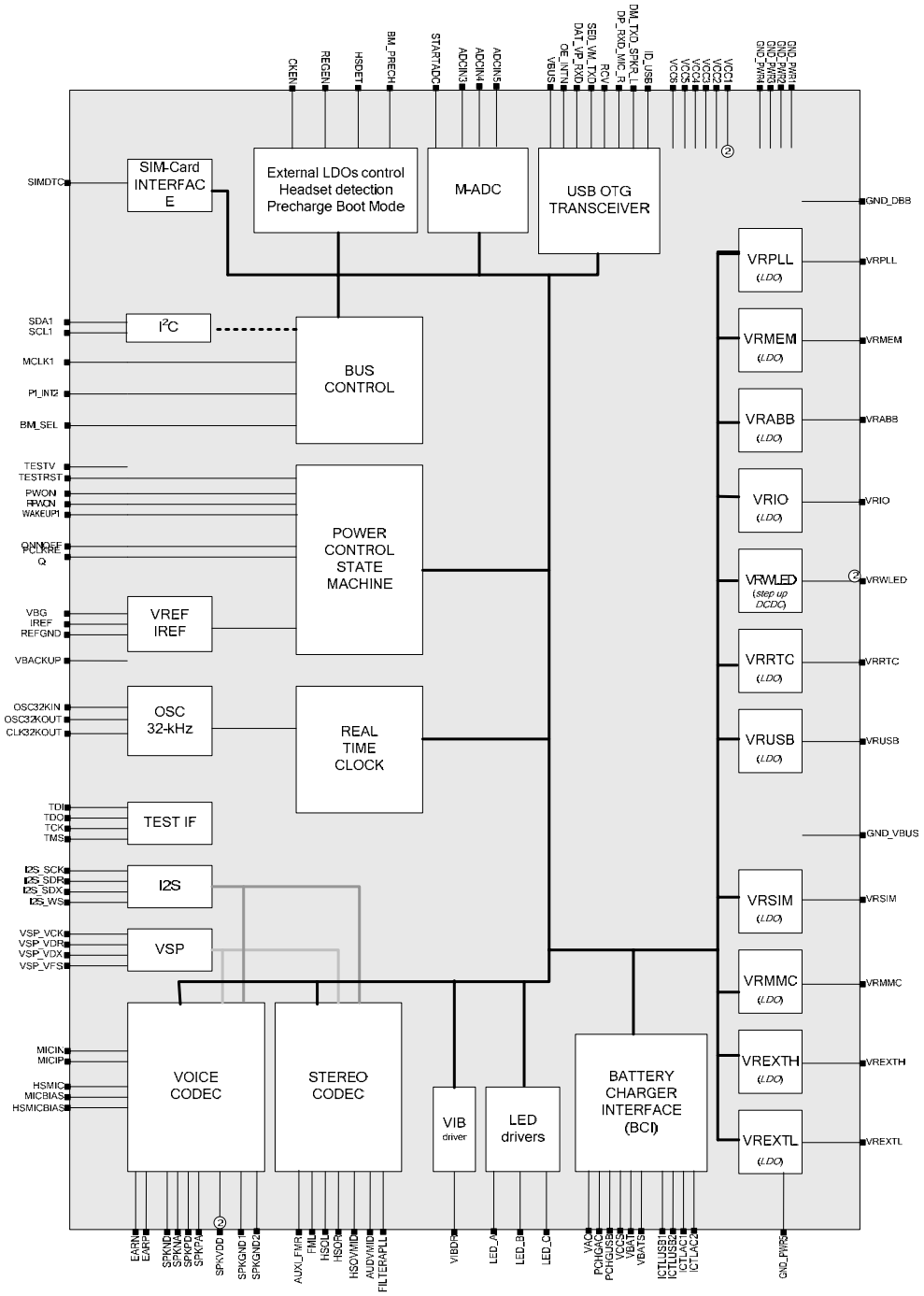


Figure 3 : Block Diagram of T3031

7 POWER RESOURCES

The power supply module of T3031 generates the different power supplies required by T3031, the processors and the external peripherals.

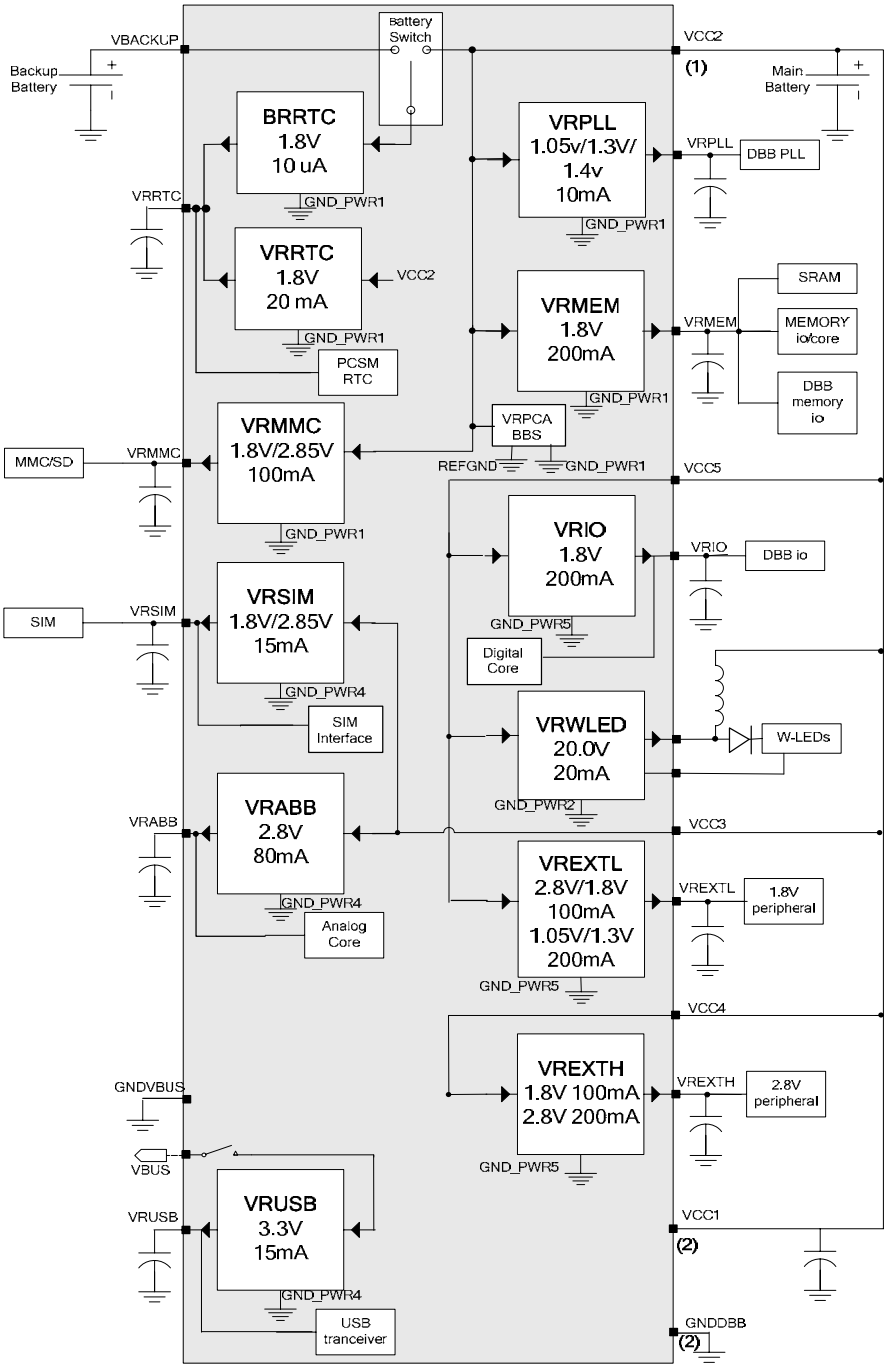


Figure 4 : Block Diagram of the Regulators

7.1 VRUSB LDO

The VRUSB voltage regulator is a Low Dropout linear voltage regulator supplying the USB module (3.3V/ 15mA).

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRUSB to GNDD	-	1	-	µF
Filtering capacitor ESR		0	-	300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}	ON mode, in regulation, VBUS_VRUSB=1 USB precharge mode, VBAT=0v	4.4 4.4	VBUS VBUS	5.25 5.25	V
Output voltage V_{OUT}	ON mode USB precharge mode, VBAT=0v	3.1 3	3. 3 3.3	3.5 3.5	V
Rated output current I_{OUT}	ON mode	-	-	15	mA
DC Load regulation	ON mode, $I_{OUT} = I_{OUTmax}$ to 0	-	-	50	mV
DC Line regulation	ON mode, $V_{IN}=V_{Inmin}$ to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$	-	Get to	20	mV
Settling time	I_{OUT} steps from I_{OUT} max/2 to I_{OUT} max in 5us I_{OUT} steps from I_{OUT} max to I_{OUT} max/2 in 5us @ $V_{OUT} = V_{OUTfinal} \pm 3\%$	-	100	-	µs
Turn-on time	I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$	-	0.5	-	ms
Ripple rejection	f = 100Hz @ I_{OUTmax} f = 500kHz @ I_{OUTmax}	- -	55 35	- -	dB
Ground current	ON mode, I_{OUT} = 0 ON mode, $I_{OUT} = I_{OUTmax}$		0.07 0.07		mA

Table 7 : Electrical Characteristics of VRUSB

7.2 VRWLED DC-DC

The VRWLED voltage regulator is a step-up DC-DC converter supplying the White LEDs (20.0V/60mA). The regulated voltage depends on the number of series White-LEDs. The main battery directly supplies VRWLED.

7.3 VRPLL LDO

The VRPLL voltage regulator is a programmable Low Dropout linear voltage regulator supplying the PLLs (1.05V, 1.3V, 1.4V/ 10mA). The main battery directly supplies VRPLL.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRPLL to GNDA		1		µF
Filtering capacitor ESR		0		300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
DC Output voltage V_{OUT}	ON mode : VRPLLSEL<1 :0>=11 ON mode : VRPLLSEL<1 :0>=10 or 01 ON mode : VRPLLSEL<1 :0>=00	1.3 1.24 0.95	1.4 1.3 1.05	1.5 1.4 1.15	V
	LOW POWER mode : VRPLLSEL<1 :0>=11 LOW POWER mode : VRPLLSEL<1 :0>=10 or 01 LOW POWER mode : VRPLLSEL<1 :0>=00	1.3 1.24 0.95	1.4 1.3 1.05	1.5 1.4 1.17	
Rated output current I_{OUT}	ON mode LOW POWER mode			10 1	mA
DC Load regulation	ON mode, I_{OUT} = I_{OUTmax} to 0			100	mV
DC Line regulation	ON mode, V_{IN}=V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			100	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%		100		ms
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%		100		µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{INmax} @ I_{OUT} = I_{OUTmax} f = 500kHz V_{IN}=3.2v to V_{INmax} @ I_{OUT} = I_{OUTmax}		55 35		dB
Ground current	ON mode, I_{OUT} = 0 ON mode, I_{OUT} = I_{OUTmax} LOW POWER mode		0.062 0.7 0.017		mA

Table 8 : Electrical Characteristics of VRPLL

7.4 VRABB LDO

The VRABB voltage regulator is a Low Dropout linear voltage regulator supplying the T3031 analog part (2.8V/ 80mA). The main battery directly supplies VRABB.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRABB to GNDA	-	1	-	µF
Filtering capacitor ESR		0	-	300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode LOW POWER mode	2.7 2.7	2.8 2.85	2.9 2.95	V
Rated output current I_{OUT}	ON mode LOW POWER mode	- -	- -	80 1	mA
DC Load regulation	ON mode, $I_{OUT} = I_{OUTmax}$ to 0	-	-	100	mV
DC Line regulation	ON mode, $V_{IN}=V_{Inmin}$ to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$	-	-	100	mV
Turn-on time	I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$	-	100	-	µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$	-	100	-	µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$ f = 500kHz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$	- -	55 35	- -	dB
Ground current	ON mode, I_{OUT} = 0 ON mode, $I_{OUT} = I_{OUTmax}$, V_{IN}>3.2v LOW POWER mode		0.055 1.4 0.017		mA

Table 9 : Electrical Characteristics of VRABB

7.5 VRRTC & BRRTC LDO

The VRRTC voltage regulator is a programmable Low Dropout linear voltage regulator supplying the embedded 32 kHz real time clock. VRRTC is also the supply voltage of the power management system. VRRTC is supplied from the main or backup battery, depending of the system state. VRRTC is always supplied, as long as a valid energy source is present.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRRTC to GNDD		1		µF
Filtering capacitor ESR		0		300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}	ON mode BACKUP mode, VBAT=0v BACKUP mode, VBACKUP=0v	2.5 1.9 1.9	VCC2 VBACKUP VCC2	5.5 5.5 3.0	V
DC Output voltage V_{OUT}	ON mode, 3.0<V_{IN}<5.5v BACKUP mode, VBAT=0v, 2.3v ≤ V_{IN} ≤ 5.5v, BACKUP mode, VBACKUP=0v, 2.3v ≤ V_{IN} ≤ 2.6v	1.65 1.65	1.8 1.8 1.8	1.95 1.95	V
Rated output current I_{OUT}	ON mode BACKUP mode			20 0.03	mA
DC Load regulation	ON mode, I_{OUT} = I_{OUTmax} to 0 BACKUP mode, VBAT=0v, I_{OUT} = I_{OUTmax} to 0			100 100	mV
DC Line regulation	ON mode, V_{IN}=3.0v to V_{INmax} @ I_{OUT} = I_{OUTmax} BACKUP mode, VBAT=0v, V_{IN}=2.3v to 5.5v @ I_{OUT} = I_{OUTmax}			100 100	mV
Turn-on time	V_{IN} =0v to 3.6v, VBACKUP =0v, I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%		5000		us
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3% From Backup to ON mode, I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%		100 100		µs
Ripple rejection	ON mode, f = 100Hz V_{IN}=2.5v to V_{INmax} @I_{OUT}=I_{OUTmax} ON mode, f = 500kHz V_{IN}=2.5v to V_{INmax} @I_{OUT}=I_{OUTmax}		55 35		dB
Ground current	ON mode @ I_{OUT} = 0 BACKUP mode		23 3		µA

Table 10 : Electrical Characteristics of VRRTC & BRRTC

7.6 VREXTH LDO

The voltage regulator VREXTH is a programmable Low Dropout linear voltage regulator supplying an external peripheral (1.8V/ 200mA, 2.8V/ 100mA). The main battery directly supplies VREXTH.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VREXTH to GND	-	1	-	µF
Filtering capacitor ESR		0	-	300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode : VREXTHSEL=1 ON mode : VREXTHSEL=0	2.7 1.65	2.8 1.8	2.9 1.95	V
	LOW POWER mode: VREXTHSEL=1 LOW POWER mode: VREXTHSEL=0	2.7 1.65	2.8 1.8	2.95 1.95	
Rated output current I_{OUT}	ON mode, V_{OUT}=2.8v ON mode, V_{OUT}=1.8v LOW POWER mode	- - -	- - -	100 200 1	mA
DC Load regulation	ON mode, I_{OUT} = I_{OUTmax} to 0, V_{OUT}=2.8v ON mode, I_{OUT} = I_{OUTmax} to 0, V_{OUT}=1.8v	- -	- -	100 50	mV
DC Line regulation	ON mode, V_{IN}=V_{Inmin} to V_{Inmax} @ I_{OUT} = I_{OUTmax}, V_{OUT}=2.8v ON mode, V_{IN}=V_{Inmin} to V_{Inmax} @ I_{OUT} = I_{OUTmax}, V_{OUT}=1.8v	- -	- -	100 50	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%	-	100	-	µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%	-	100	-	µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ I_{OUT} = I_{OUTmax} f = 500kHz V_{IN}=3.2v to V_{Inmax} @ I_{OUT} = I_{OUTmax}	- -	55 35	- -	dB
Ground current	ON mode, I_{OUT} = 0 ON mode, I_{OUT} = I_{OUTmax}, V_{OUT} = 1.8v ON mode, I_{OUT} = I_{OUTmax}, V_{OUT} = 2.8v LOW POWER mode		0.06 2 1.3 0.017		mA

Table 11 : Electrical Characteristics of VREXTH

7.7 VREXTL LDO

The voltage regulator VREXTL is a programmable Low Dropout linear voltage regulator supplying an external peripheral (2.8V, 1.8V/ 100mA). The main battery directly supplies VREXTL.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VREXTL to GNDD		1		µF
Filtering capacitor ESR		0		300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode, VREXTLSEL=11 ON mode, VREXTLSEL=10 ON mode, VREXTLSEL=01 ON mode, VREXTLSEL=00	2.7 1.65 1.24 0.95	2.8 1.8 1.3 1.05	2.9 1.95 1.4 1.15	V
	LOW POWER mode, VREXTLSEL=11 LOW POWER mode, VREXTLSEL=10 LOW POWER mode, VREXTLSEL=01 LOW POWER mode, VREXTLSEL=00	2.7 1.65 1.24 0.95	2.8 1.8 1.3 1.05	2.95 1.95 1.42 1.17	V
Rated output current I_{OUT}	ON mode, V_{OUT}=2.8v/1.8v ON mode, V_{OUT}=1.3v/1.05v			100 200	mA
	LOW POWER mode			1	
DC Load regulation	ON mode, I_{OUT} = I_{OUTmax} to 0, V_{OUT}=2.8v ON mode, I_{OUT} = I_{OUTmax} to 0, V_{OUT}=1.8v			100 50	mV
DC Line regulation	ON mode, V_{IN}=V_{Inmin} to V_{Inmax} @ I_{OUT} = I_{OUTmax}, V_{OUT}=2.8v ON mode, V_{IN}=V_{Inmin} to V_{Inmax} @ I_{OUT} = I_{OUTmax}, V_{OUT}=1.8v			100 50	mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%		100		µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ V_{OUT} = $V_{OUTfinal}$ ± 3%		100		µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ I_{OUT} = I_{OUTmax} f = 500kHz V_{IN}=3.2v to V_{Inmax} @ I_{OUT} = I_{OUTmax}		55 35		dB
Ground current	ON mode, I_{OUT} = 0 ON mode, I_{OUT} = I_{OUTmax} LOW POWER mode		0.06 2 0.015		mA

Table 12 : Electrical Characteristics of VREXTL

7.8 VRMMC LDO

The voltage regulator VRMMC is a programmable Low Dropout linear voltage regulator supplying an external MMC device (1.8V, 2.85V/ 100mA). The main battery directly supplies VRMMC.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRMMC to GNDD	-	1	-	µF
Filtering capacitor ESR		0	-	300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode : VRMMCSEL=1, ON mode : VRMMCSEL=0,	2.7 1.65	2.85 1.8	2.95 1.95	V
	LOW POWER mode : VRMMCSEL=1, LOW POWER mode : VRMMCSEL=0,	2.7 1.65	2.85 1.8	2.95 1.95	
Rated output current I_{OUT}	ON mode LOW POWER mode			100 1	mA
DC Load regulation	ON mode, $I_{OUT} = I_{OUTmax}$ to 0			100	mV
DC Line regulation	ON mode, $V_{IN}=V_{Inmin}$ to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$			100	mV
Turn-on time	I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$ f = 500kHz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$		55 35		dB
Ground current	ON mode, I_{OUT} = 0 ON mode, $I_{OUT} = I_{OUTmax}$ LOW POWER mode		0.06 1.3 0.017		mA

Table 13 : Electrical Characteristics of VRMCC

7.9 VRSIM LDO

The voltage regulator VRSIM is a programmable Low Dropout linear voltage regulator supplying the SIM-card and the SIM-card driver (1.8V, 2.85V/ 15mA). The main battery directly supplies VRSIM.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRSIM to GNDD		670 (1)		nF
Filtering capacitor ESR		0		300	mΩ

Note: (1) 670nF capacitors are built with 470nF close to VRSIM output , 100nF close to the Digital Baseband USIM supply and 100nF close to Sim Card socket

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode : VRSIMSEL=1, ON mode : VRSIMSEL=0,	2.7 1.65	2.85 1.8	2.95 1.95	V
	LOW POWER mode : VRSIMSEL=1, LOW POWER mode : VRSIMSEL=0,	2.7 1.65	2.85 1.8	2.95 1.95	
Rated output current I_{OUT}	ON mode LOW POWER mode			15 1	mA
DC Load regulation	ON mode, $I_{OUT} = I_{OUTmax}$ to 0			100	mV
DC Line regulation	ON mode, $V_{IN}=V_{Inmin}$ to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$			100	mV
Turn-on time	I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$ f = 500kHz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$		55 35		dB
Ground current	ON mode, I_{OUT} = 0 ON mode, $I_{OUT} = I_{OUTmax}$ LOW POWER mode		0.06 0.85 0.017		mA

Table 14 : Electrical Characteristics of VRSIM

7.10 VRIO LDO

The voltage regulator VRIO is a Low Dropout linear voltage regulator supplying the I/Os of the system (1.8V/ 200mA). The main battery directly supplies VRIO.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRIO to GNDD		1		µF
Filtering capacitor ESR		0		300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode LOW POWER mode	1.7 1.65	1.8 1.85	1.9 1.95	V
Rated output current I_{OUT}	ON mode LOW POWER mode			200 1	mA
DC Load regulation	ON mode, $I_{OUT} = I_{OUTmax}$ to 0			100	mV
DC Line regulation	ON mode, $V_{IN}=V_{Inmin}$ to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$			100	mV
Turn-on time	I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$ f = 500kHz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$		55 35		dB
Ground current	ON mode, I_{OUT} = 0 ON mode, $I_{OUT} = I_{OUTmax}$ LOW POWER mode		0.06 1.75 0.017		mA

Table 15 : Electrical Characteristics of VRIO

7.11 VRMEM LDO

The voltage regulator VRMEM is a Low Dropout linear voltage regulator supplying the external SRAM, Flash memories (1.8V/ 200mA). The main battery directly supplies VRMEM.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VRMEM to GNDD	-	1	-	µF
Filtering capacitor ESR		0	-	300	mΩ

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}		3.0	3.6	5.5	V
Output voltage V_{OUT}	ON mode LOW POWER mode	1.7 1.65	1.8 1.85	1.9 1.95	V
Rated output current I_{OUT}	ON mode LOW POWER mode	- -	- -	200 1	mA
DC Load regulation	ON mode, $I_{OUT} = I_{OUTmax}$ to 0	-	-	50	mV
DC Line regulation	ON mode, $V_{IN}=V_{Inmin}$ to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$	-	-	50	mV
Turn-on time	I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$	-	100	-	µs
Wake-up time	LOW POWER to ON mode, I_{OUT} = 0, @ $V_{OUT} = V_{OUTfinal} \pm 3\%$	-	100	-	µs
Ripple rejection	f = 100Hz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$ f = 500kHz V_{IN}=3.2v to V_{Inmax} @ $I_{OUT} = I_{OUTmax}$	- -	55 35	- -	dB
Ground current	ON mode, I_{OUT} = 0 ON mode, $I_{OUT} = I_{OUTmax}$ LOW POWER mode		0.06 1.75 0.017		mA

Table 16 : Electrical Characteristics of VRMEM

7.12 REFERENCE VOLTAGE AND BIAS CURRENT

The band–gap voltage reference is filtered by using an external capacitor connected across the VREF output and the analog ground REFGND. The VREF voltage is distributed and buffered inside the device. The band–gap is started in fast mode and is set automatically in slow mode , there is less noise after a switch on. The bias currents of the analog blocks of T3031 are generated in using an external resistor connected across IREF and the analog ground REFGND. The current flowing through this resistor is then multiplied and distributed across the device.

Output load condition

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Filtering capacitor	Connected from VREF to GNDREF		100		nF
Biasing resistor	Connected from IREF to GNDREF		120k		Ω

Electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage V_{IN}	ON mode	2.5	3.6	5.5	V
Output Reference voltage (VREF terminal)	ON mode LOW POWER mode	1.16	1.18 1.2	1.2	V
Output voltage on IREF terminal	ON mode LOW POWER mode		VREF 0		V
Internal Low Reference voltage	Measured through TESTV terminal, ON mode LOW POWER mode		 0.85 0.85		V
PORZ/Backup VRTC Internal Reference voltage	Measured through TESTV terminal, BACKUP mode		 1.2		V

Table 17 : Electrical Characteristics of Reference Voltage and Bias Current

7.13 BACKUP BATTERY

The backup battery can be recharged from the main battery. A programmable voltage regulator powered by the main battery allows recharging the backup battery. The backup battery charge starts when the following conditions are met:
Backup battery charge is enabled by a control bit
Main Battery voltage > Backup Battery voltage
Main battery > 2.8V
Note: If the backup battery is not present , the backup battery pin is connected to main battery pin

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VBACKUP to MADC input attenuation	VBACKUP from 2.4 V to 5.5 V	0.2	0.25	0.35	V/V
Backup battery charging current	VBACKUP = 2.8 V, BBCHEN = 1	350	500	900	µA
	VBACKUP = 0 V, BBCHEN = 1	350	500	900	µA
End backup battery charging voltage: VBBCHGEND	$I_{VBACKUP}$ = -10 µA , BBSEL = 00	3.0	3.1	3.2	V
	$I_{VBACKUP}$ = -10 µA , BBSEL = 01	3.1	3.2	3.3	
	$I_{VBACKUP}$ = -10 µA , BBSEL = 10	2.9	3.0	3.1	
	$I_{VBACKUP}$ = -10 µA , BBSEL = 11	VBAT-0.2	VBAT		

Table 18 : Electrical Characteristics of Backup battery

7.14 BATTERY MONITORING AND DETECTION THRESHOLD

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main Battery Charged Threshold VMBCH	Measured on VBAT terminal	3	3.2	3.5	V
Main Battery Low Threshold VMBLO	VBACKUP=3.2v, measured on VBAT terminal (monitored on terminal ONNOFF)	2.6	2.75	2.9	V
Main Battery High Threshold VMBHI	Measured on terminal VBAT, VBACKUP=0v	2.5	2.65	3.0	V
	Measured on terminal VBAT, VBACKUP=3.2v	2.5	2.85	3.0	
Batteries Not Present Threshold VBNPR	Measured on terminal VBACKUP with VBAT=0v, Measured on terminal VBAT with VBACKUP =0v, (monitored on terminal VRRTC)	1.9	2.1	2.3	V

Table 19 : Power ON/Power OFF and Backup Conditions

7.15 POWER CONSUMPTION

All current consumption measurements are performed with RBIAS=120kΩ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF mode (1)	VBAT=3.6v, CK32K ON		43	65	µA
BACKUP mode (1)	VBAT=0v, VBACKUP=3.2v, CK32K ON VBAT= 2.4v, VBACKUP=0v, CK32K ON		8.5 16	12 22	µA

(1) programming Power Digital software patches: PB_CLK_CFG=00

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Audio Voiceband Codec (VBC)	WBA=0, MICAMP and EARAMP on, See Note (3) WBA=1, MICAMP and EARAMP on		3.8 5.3		mA
Audio Stereo Codec (AUSC)	SRW=010, AUFS=44.1kHz, HSOAMPL&R on		7.75		mA
Vibrator (VIB)			0.05		mA
Monitoring ADC (MADC)			0.275		mA

(3) Measurements are for blocks in power up mode without transmit or receive activity. System clock is running on 13 MHz.The consumption is given for a stand alone block. To have the total consumption, add the current describe in Section *Device ON/OFF Modes*.

Table 20 : Power Consumption

8 AUDIO AND VOICE INTERFACE

The T3031 device provides to the platform voice and audio resources

- A voice path
- A audio stereo path.

The voice path processes the analog audio signals in the uplink path and transmits the converted data to the DSP speech coder through the Voice Serial Port VSP. In the downlink path, the voice path converts the digital samples of speech data received from the DSP via the VSP into analog audio signals. The voice path supports a 8 kHz (default narrowband mode) or a 16 kHz (wideband mode) sampling frequency.
The Stereo path converts the audio digital samples received from the I^2S serial interface into analog audio signals. It supports all the standard frequencies from 8kHz to 48kHz (allowed frequencies: 8, 11.025, 12, 22.05, 24, 32, 44.1 and 48 kHz).
Two included PLLs provide the suitable system clocks to the voice and stereo circuitry (ADC, DAC, Digital Filters, Digital interfaces).

Features

- Handset Microphone biasing
- Headset Microphone biasing
- Headset Plug/Unplug detection
- Headset Hook detection (call answer/end button on equiped Headset microphone device)
- High output dynamic differential Earphone mode, using Headset outputs
- Two gain modes (high & low power) on 8Ω Handfree driver to be compatible with dual mode Ear/Handfree single speaker device
- Pop Noise attenuation circuitry implemented for all single-ended output stages
- Mono Voice memo capability: Voice memo function is supported for both 8kHz Narrowband and 16kHz Wideband by routing the Voice uplink samples to the audio interface (I2S) transmit path.

External inputs

- Voice serial port (VDR pin)
- Audio serial port (SDR pin)
- FM stereo (FML pin, FMR/AUXI pin)
- FM mono (FMR/AUXI pin only)
- Handset microphone input (MICIN,MICIP pins)
- Headset microphone input (HSMIC pin)
- Car kit microphone (D+ pin)

Outputs

- Handset earphone outputs (EARP, EARN pins)
- Handfree 8Ω speaker outputs (SPKPA, SPKPD, SPKNA, SPKND pins)
- Headset 32Ω stereo outputs (HSOL, HSOR pins)
- USB car kit stereo outputs (D+, D- pins)
- USB car kit mono output (D- pin)
- Voice serial port (VDX)
- Audio serial port (SDX)

SOURCE: EXT ⇒ / INT ⇒ / OUT ⇓	MIC	HSMIC	D+ (CARKIT MIC)	FMR/ FM MONO/ AUXI (5)	FML (5)	VDR VOICE	INVERTED VOICE (4)	SDR L	SDR R	SDR MONO (2)
Earphone						X		(*)		X(2)
Handfree (8 Ohms)				X		X		(*)		X(2)
Headset L					X	X(3)(4)		X		X(2)
Headset R				X		X(3)	X(4)		X	X(2)
USB D+ (Carkit R speaker)									X	X(2)
USB D- (Carkit L speaker)						X		X		X(2)
VDX	X(1)	X(1)	X(1)	X(1)						
SDX	X(1)	X(1)	X(1)	X(1)						

Table 21 : Multiplexing and Mixing Capabilities for the Available Outputs

Important Notes:

EXT: External analog or digital inputs
INT: Inputs which can be generated internally and used as inputs

X: indicates a possible path connection

(1):
The VDX output can be routed to the SDX output.

(2): **Built internally:**
A mono conversion SDR MONO = SDRL + SDRR is done in the audio digital control.
The propagation of the Audio Mono signal to a Mono output stage is done in using the Left DAC channel only
(*):This connectivity allows to route the Audio Left signal to each Mono output

(3):
The VDR signal is a mono signal and can be routed to Headset Left and Right speakers of a Stereo Headset device.

(4): **Built internally:**
The VDR signal is converted in the analog domain by a DAC converter and amplified.
The voice DAC out signal can be inverted in the analog domain, before amplification.
These signals can be connected to the Headset L and R amplifiers to built a differential output stage and increase the output dynamic range and SNR.

(5):
- If the FM input is a stereo signal, the FML input corresponds to the FM left channel input and the FMR/AUXI input corresponds to the FM right channel input.
- If the FM input is a mono signal, the FMR/AUXI input has to be used only.

The grey colored boxes on the same row show that signals from corresponding sources which can be mixed in the analog domain before being output , the output is given in the same row. Maximum 2 signals can be mixed together.

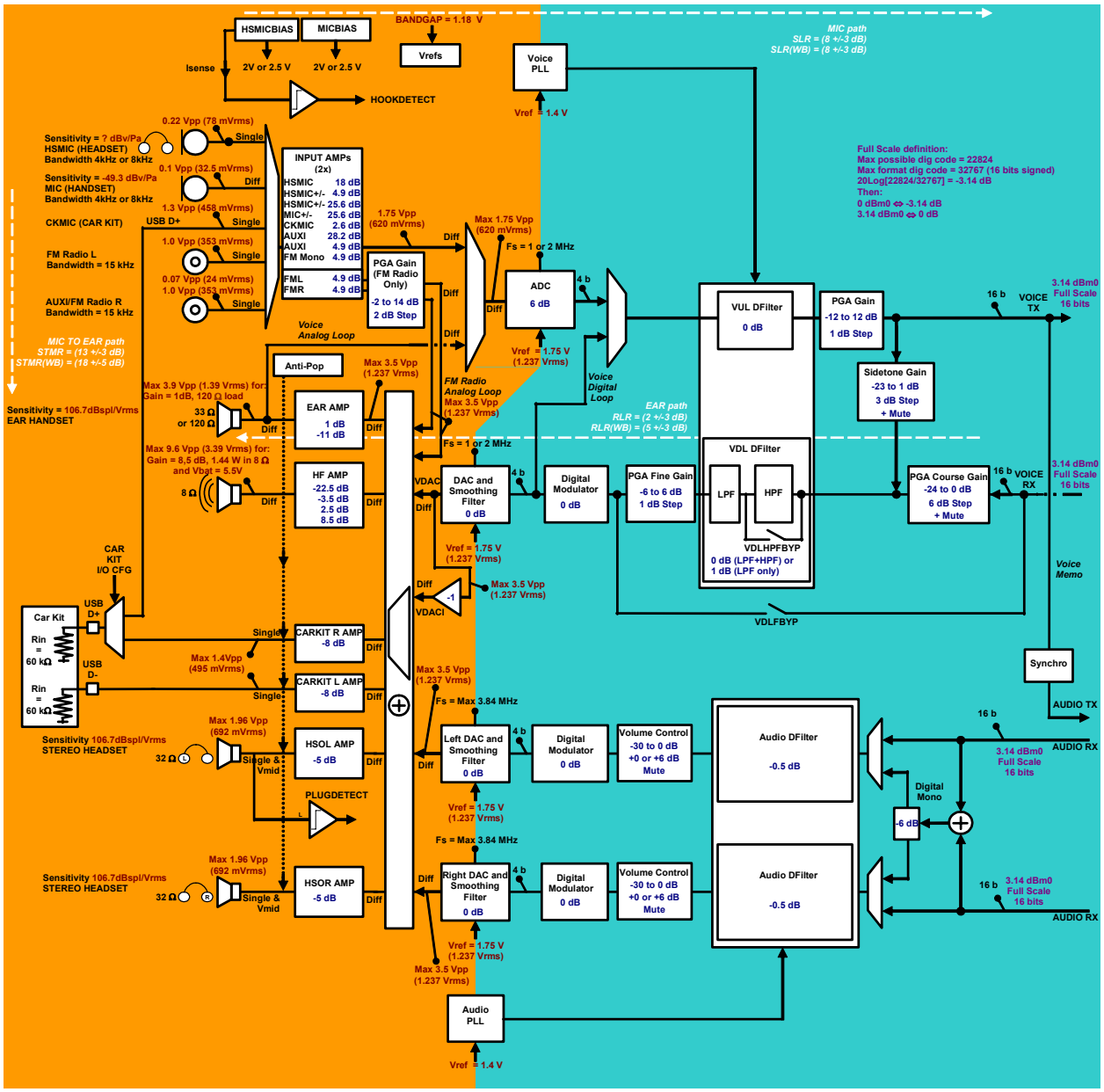


Figure 5 : Audio and Voice Block Diagram

8.1 VOICE UPLINK PATH

The voice uplink path includes a first amplification stage dedicated to inputs

The handset differential inputs MICIP and MICIN can be amplified by the differential handset microphone amplifier. This amplifier has a gain of 25.6 dB and a bias generator MICBIAS provides an external voltage of 2 V or 2.5 V to bias the microphone.

The headset differential inputs HSMIC and AUXI can be amplified by the differential handset microphone amplifier. This amplifier has two different gains 4.9 dB or 25.6 dB and a bias generator HSMICBIAS provides an external voltage of 2 V or 2.5 V to bias the microphone.

The auxiliary input AUXI (AUXI - VMID) can be amplified by the auxiliary amplifier. This amplifier has two different gains 4.9 dB or 28.2 dB. VMID is an internal reference.

The headset single input HSMIC (HSMIC - VMID) can be amplified by the auxiliary amplifier. This amplifier has a gain of 18 dB and a bias generator HSMICBIAS provides an external voltage of 2 V or 2.5 V to bias the microphone.

The car kit microphone input USB D+ (USB D+ - VMID) can be amplified by the auxiliary amplifier. This amplifier has a gain of 2.6 dB.

The mono FM input (mono FM - VMID) can be amplified by the auxiliary amplifier. This amplifier has a gain of 4.9 dB.

The stereo FM inputs can be amplified, the FM right channel is amplified by the auxiliary amplifier (FM R - VMID). and the left channel by the handset microphone amplifier (FM L - VMID), the gains are of 4.9 dB. This output is not connected to the ADC input, like the other outputs, but to an audio output stage through a logarithmic PGA gain stage.

Analog–to–digital conversion is performed by a third–order Σ–Δ modulator with a sampling rate of 1MHz/2MHz. Output of the ADC is fed to a speech digital filter, which performs the decimation down to 8kHz/16kHz and band–limits the signal with both low–pass and high–pass transfer functions. Programmable gain can be set digitally from -12 dB to +12 dB in 1 dB steps and is programmed with the VULPG bits of the VULGAIN register. The speech samples are then transmitted to the DSP via the voice serial interface (VSP) at a rate of 8kHz /16kHz. The uplink voice path can be powered down with the VULR bit of the TOGB register.

Headset Plug/Unplug detection:

- 2 modes:
  - Triton Lite already ON (Battery connected, VRIO ON) and plug event;
  - Triton Lite OFF and plug event: the plug detection will be effective once VRIO is set ON;
- A plug detection will set the status bit HEADSETSTATUS to ‘0’ state (register AUDINTSTS) and generate an INT2_P1 interrupt to be acknowledged;
- An unplug detection will set the status bit HEADSETSTATUS to ‘1’ state (register AUDINTSTS) and generate another INT2_P1 interrrupt to be acknowledged.
- Plug and unplug detections are digitally debounced (debouncing time = 8ms).

- The jack plug detection feature is addressed through the HSDET pin. The integrated pull up, connected to the pin, forces a high level (VBAT) when the headset load is not connected. At jack insertion headset load connection (32 Ohms) imposes a low level on that node (Headset left channel): as an exemple HSDET = 1mV after jack plug for VBAT = 4V.
- Input comparator threshold voltages are defined as VTlow = VBAT/2 – 100mV and VThigh = VBAT/2 + 100mV, VBATmin = 3.2V. The plug and unplug detection remains functional if there is no signal from HSOL amplifier output (stereo path is OFF) or if there is a signal from HSOL

(stereo path is ON): maximum level on HSOL when the stereo path is ON is 1 Vp which stays far enough from the comparator threshold levels VBATmin/2 – 100mV and VBATmin/2 + 100mV.

- Jack plug detection is functional if a plug event occurs before the power up of Triton Lite or if the plug event occurs after the power up of Triton Lite: analog detection part is always active if the battery is connected; Detection interrupts will be generated once the VRIO regulator is power up during the Triton Lite power up sequence.
- A level change on HSDET pin is sensed by a Schmitt trigger to provide a jack detection signal to the audio digital control. The audio digital control receives the detection signal and proceeds to a digital debouncing (time: 8ms = 256 * 32 kHz clock periods) before sending an INT2 interrupt signal to the interrupts handler, indicating that an plug event happened on the jack connector.
- In order to be able to detect jack unplug the same I/O is configured to generate an interrupt on the opposite level transition of its input voltage once insertion interrupt has been acknowledged.
- A status bit HEADSETSTATUS (bit #0 in AUDINTSTS register) is available to reflect to detection state: '1' state means there is no plug, '0' state means that there is a plug insertion.

Headset Hook detection (call answer/end button on equipped Headset microphone device):

- Only a push button event will generate an INT2_P1 interrupt. A push button detection will set the HOOKSTATUS bit to '0' state (register AUDINTSTS);
- A Hook button release will not generate any interrupt, but the status bit HOOKSTATUS (register AUDINTSTS) will be set to '1' state;
- Usage:
  - HSMICBIAS power ON:
    - Set HSMICBIAS value (2V or 2.5V): set bit #5 MICBIASLVL in CTRL2 register;
    - Set VULON: set bit #1 VULS ='1' in TOGB register;
    - Select HSMICBIAS: set bit #4 MICBIASSEL = '1' in CTRL2 register;
  - Wait HSMICBIAS power on settling time;
  - Set bit #4 HOOKEN = '1' in CTRL5 register to enable the Hook detection circuitry.
- Analog debouncing: depends on external components choice.
- When disabling headset HOOK detection: HOOKEN bit MUST be set to '0', before any VULOFF (bit #0 VULR ='1' in TOGB register).

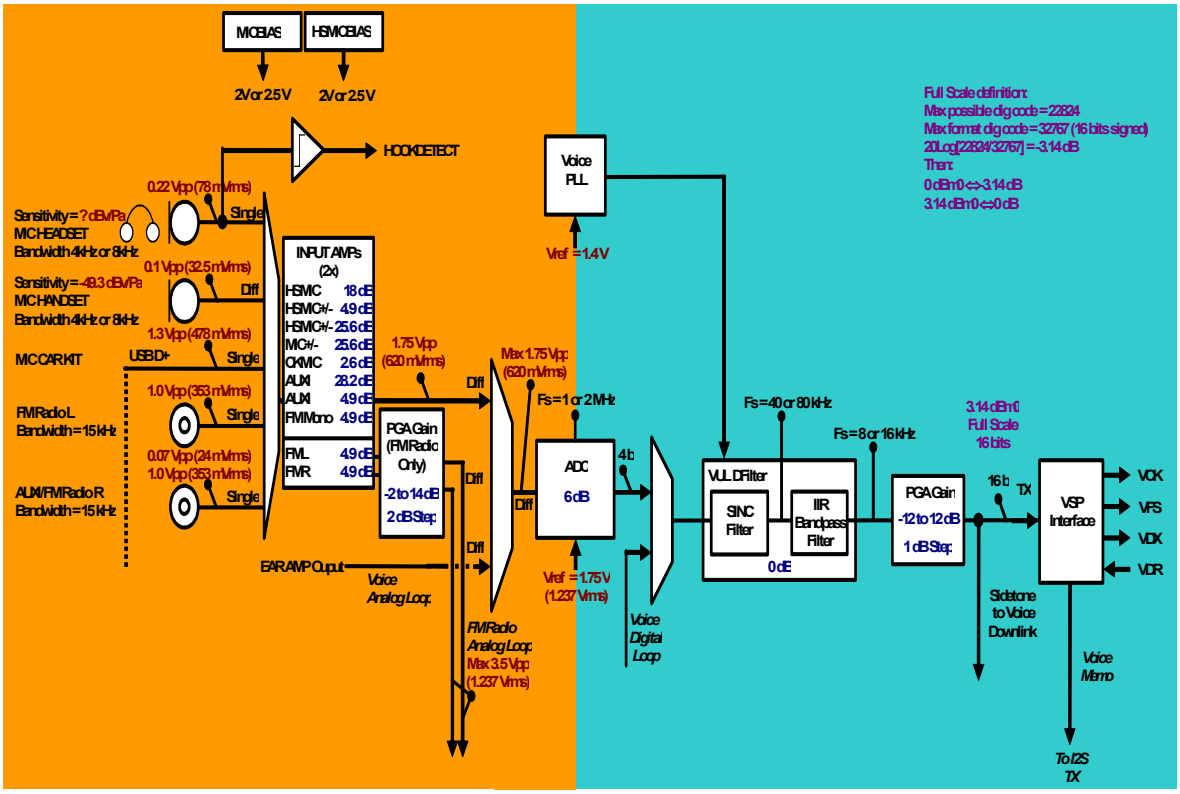


Figure 6 : Voice Uplink Path

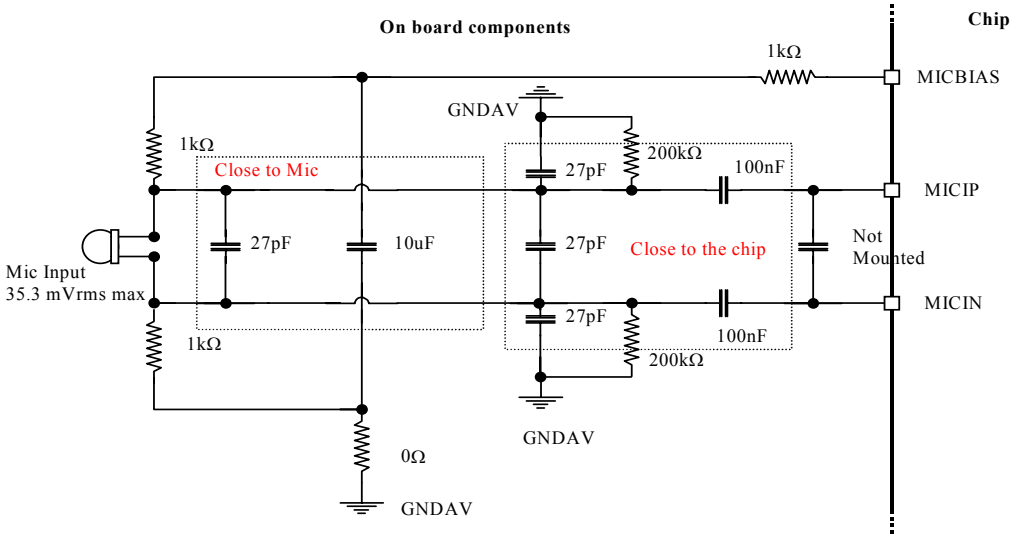


Figure 7 : Handset Microphone differential Inputs

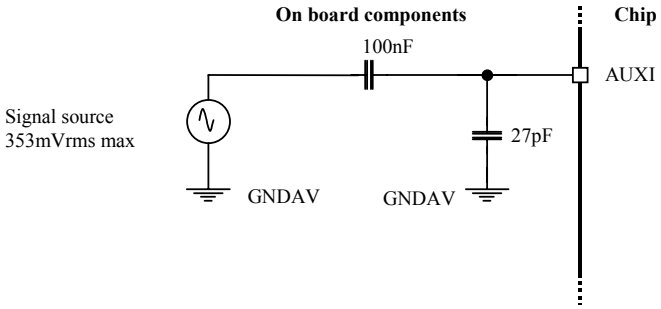
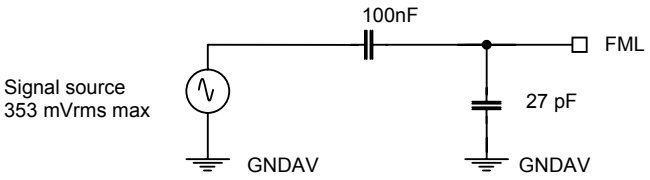


Figure 8 : Auxiliary Input



And

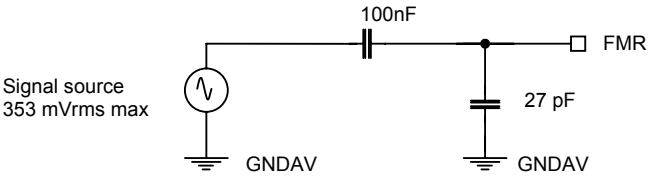


Figure 9 : FM Radio Stereo Inputs

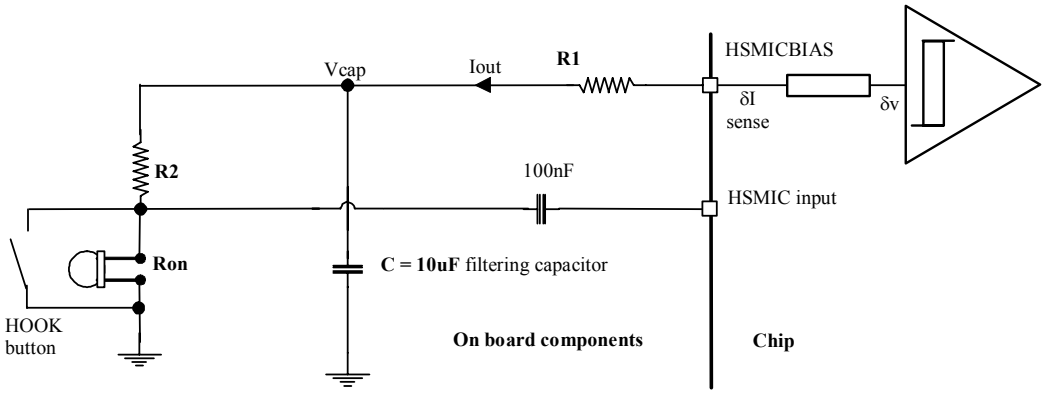


Figure 10 : Headset Microphone single input, Hook Detection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HSMICBIAS current (Iout) for open switch	HSMICBIAS = 2 V			450	uA
HSMICBIAS current (Iout) for close switch	HSMICBIAS = 2 V	1050			
HSMICBIAS current (Iout) for open switch	HSMICBIAS = 2.5 V			600	
HSMICBIAS current (Iout) for close switch	HSMICBIAS = 2.5 V	1200			

Note: Figure 11 shows the allowed ranges for Iout (open and close switch). Hook detection is not guaranteed if Iout does not follow the ranges reported in the Table 22.

Table 22 : Hook Detection Current Threshold

The external R1, R2 (and Ron) resistances values in the HSMIC biasing schematic need to be chosen to allow the correct biasing of the HSMIC microphone and to allow the hook detection when the HSMIC microphone is shorted during a push button event.

Components should be chosen using following formulas:

OPEN SWITCH:

R1 + R2 + Ron > HSMICBIAS / Iout

For HSMICBIAS = 2V, R1 + R2 + Ron > 4.44kOhms
For HSMICBIAS = 2.5V, R1 + R2 + Ron > 4.17kOhms

CLOSE SWITCH:

R1 + R2 < HSMICBIAS / Iout

For HSMICBIAS = 2V, R1 + R2 < 1.9kOhms
For HSMICBIAS = 2.5V, R1 + R2 < 2.08kOhms

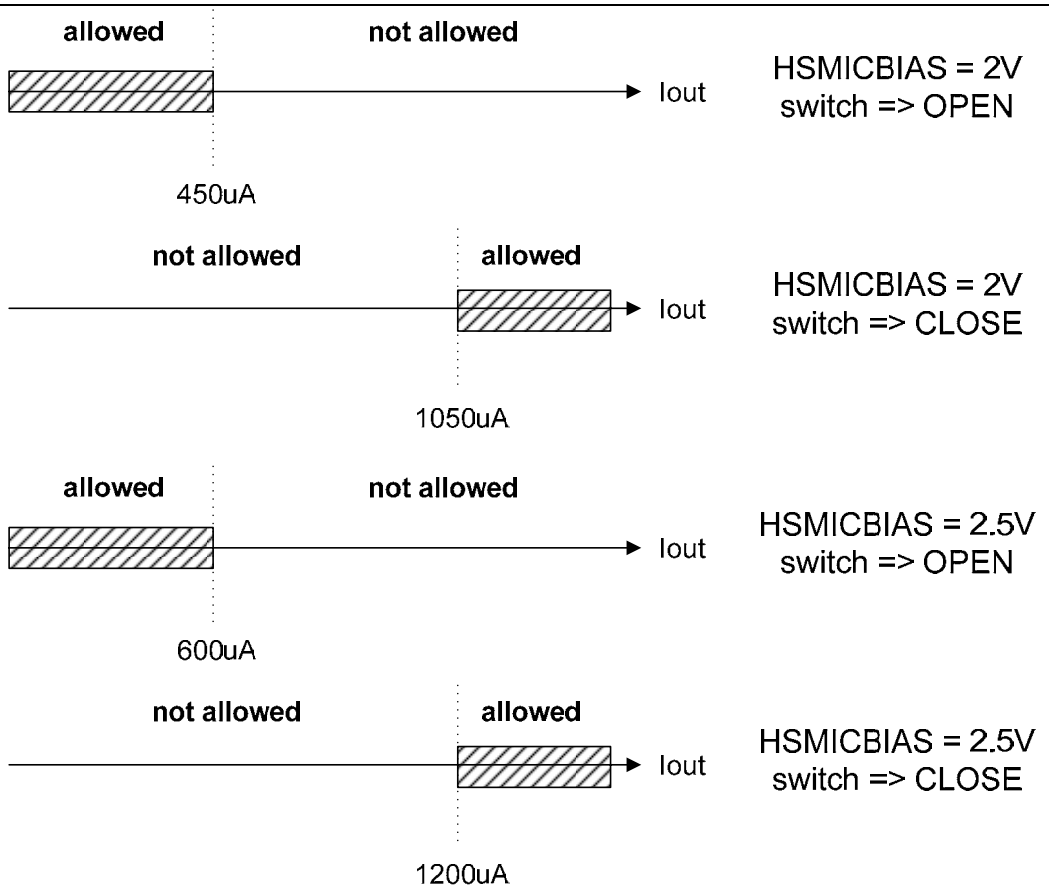


Figure 11 : Allowed regions for Iout current

$$Vcap = \left(Vhsmicbias \Big/ \left(1 + \left(\frac{R1}{R2 + Ron}\right)\right)\right) \times \left(1 - e^{\frac{-t}{\tau}}\right) \qquad \tau = \left(R1 \times C \Big/ \left(1 + \left(\frac{R1}{R2 + Ron}\right)\right)\right)$$

Vcap and Iout nominal values are reached at 99% at t = 5τ.

It is mandatory to wait 5τ between HSMICBIAS power ON and HOOK enable to avoid parasitic push button detection.

PARAMETER	TEST CONDITIONS	TYP	UNITS
Settling time = 5τ	HSMICBIAS = 2V or 2.5V, R1 = R2 = Ron = 1kΩ and C = 10pF.	33.3	ms

Table 23 : Settling Time between HSMICBIAS power ON and HOOK , Single Input HSMIC

$$Vcap = \left(Vhsmicbias \Big/ \left(1 + \left(\frac{R1}{R2}\right)\right)\right) \times \left(1 - e^{\frac{-t}{\tau}}\right) \qquad \tau = \left(R1 \times C \Big/ \left(1 + \left(\frac{R1}{R2}\right)\right)\right)$$

PARAMETER	TEST CONDITIONS	TYP	UNITS
Time constant = τ	HSMICBIAS = 2V or 2.5V, Ron = 1kΩ and C = 10pF: Typ: nominal R1 = R2 = 1kΩ	5	ms

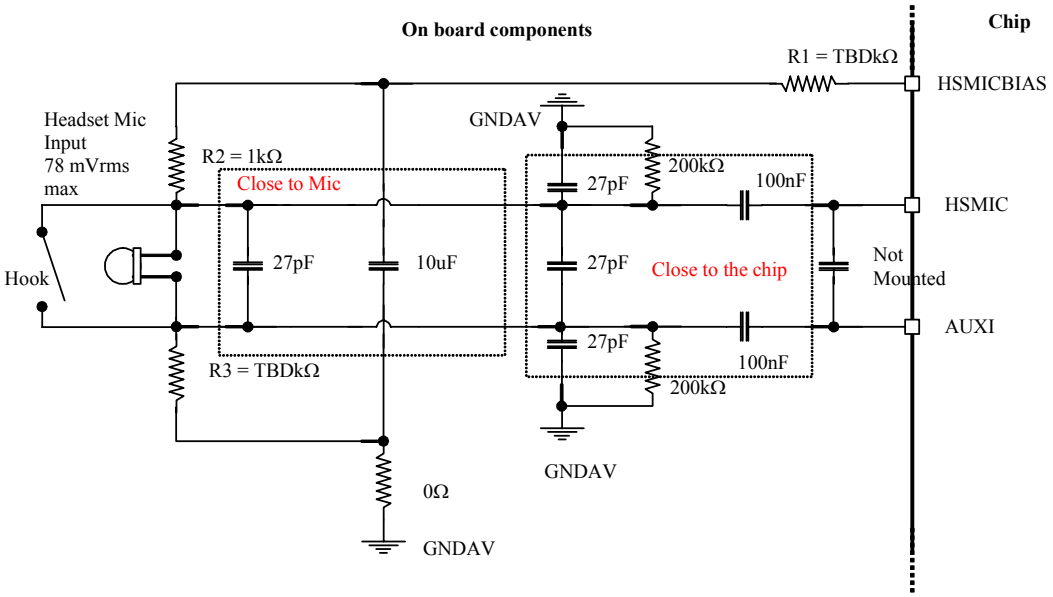
Table 24 : Time Constant After A HooK button push Event , Single Input HSMIC

$$Vcap = \left(Vhsmicbias \Big/ \left(1 + \left(\frac{R1}{R2 + Ron}\right)\right)\right) \times \left(1 - e^{\frac{-t}{\tau}}\right) \qquad \tau = \left(R1 \times C \Big/ \left(1 + \left(\frac{R1}{R2 + Ron}\right)\right)\right)$$

PARAMETER	TEST CONDITIONS	TYP	UNITS
Time constant = τ	HSMICBIAS = 2V or 2.5V, Ron = 1kΩ and C = 10pF: Typ: nominal R1 = R2 = 1kΩ	6.6	ms

Table 25 : Time Constant After A HooK button Release Event , Single Input HSMIC

Note: serial resistances values between HSMICBIAS, HSMIC and GNDAV have to be choosen **to bias** correctly **the microphone** and **respect the hook detection threshold current**.



Settling Time between HSMICBIAS power ON and HOOK

$$Vcap = \left(Vhsmicbias \Big/ 1 + \left(\frac{R1}{R2 + R3 + Ron} \right) \right) \times \left(1 - e^{\frac{-t}{\tau}} \right) \quad \tau = \left(R1 \times C \Big/ 1 + \left(\frac{R1}{R2 + R3 + Ron} \right) \right)$$

Vcap and Iout nominal values are reached at 99% at t = 5τ.

It is mandatory to wait 5τ between HSMICBIAS power ON and HOOK enable to avoid parasitic push button detection.

Time Constant After A Hook button Push Event (R1 + R2 + R3 = 2kΩ, Ron = 1kΩ)

$$Vcap = \left(Vhsmicbias \Big/ 1 + \left(\frac{R1}{R2 + R3} \right) \right) \times \left(1 - e^{\frac{-t}{\tau}} \right) \qquad \tau = \left(R1 \times C \Big/ 1 + \left(\frac{R1}{R2 + R3} \right) \right)$$

Time Constant After A Hook Button Release Event

$$Vcap = \left(Vhsmicbias \Big/ 1 + \left(\frac{R1}{R2 + R3 + Ron} \right) \right) \times \left(1 - e^{\frac{-t}{\tau}} \right) \quad \tau = \left(R1 \times C \Big/ 1 + \left(\frac{R1}{R2 + R3 + Ron} \right) \right)$$

Figure 12 : Headset Microphone differential inputs, Hook Detection

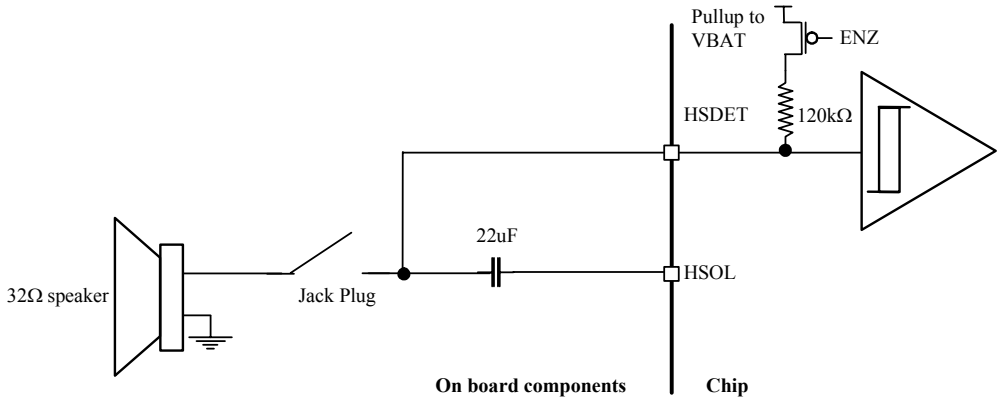


Figure 13 : Headset Plug and Unplug Detection

8.2 VOICE DOWNLINK PATH

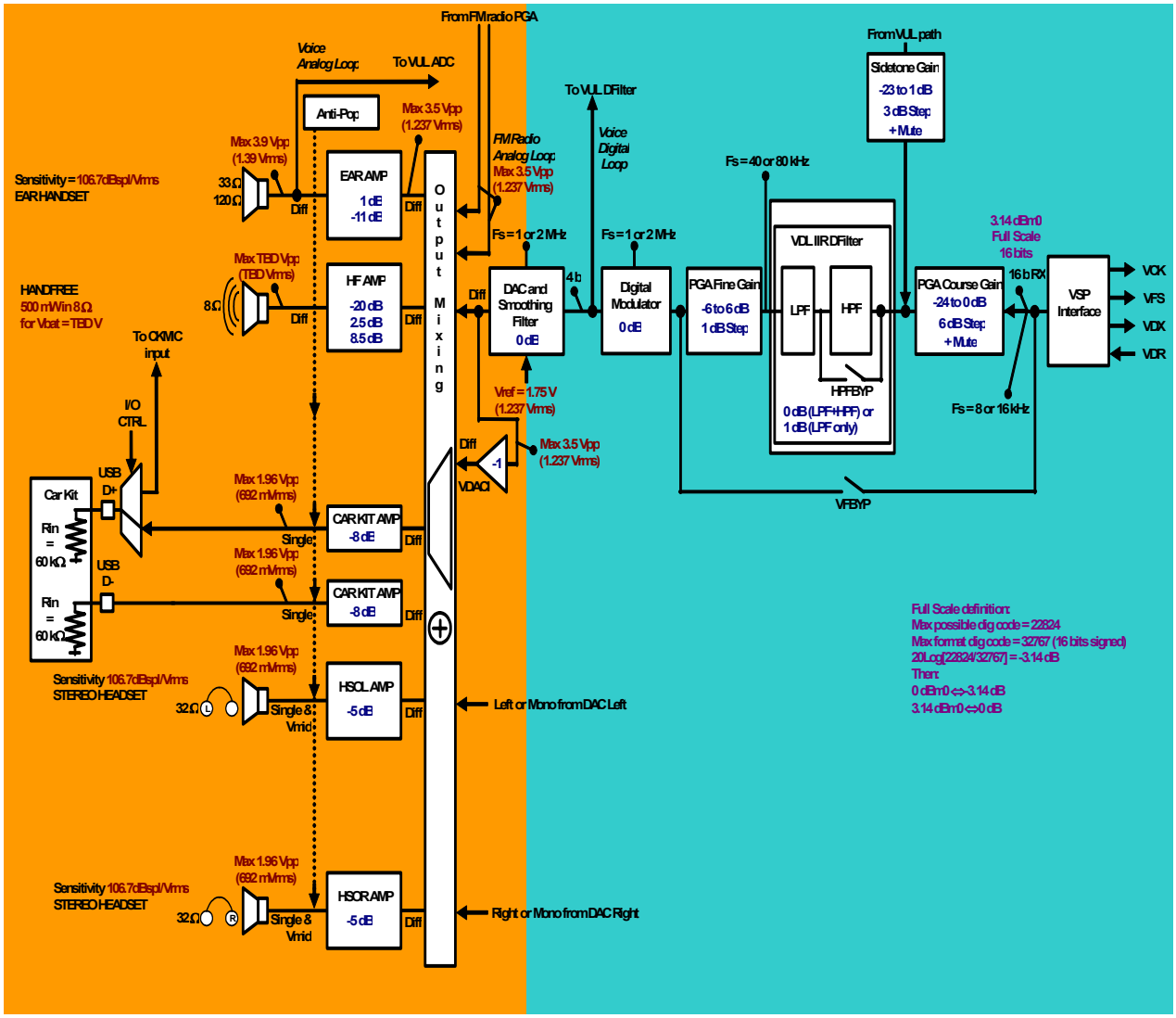


Figure 14 : Voice Downlink Path

The voice downlink path receives speech samples at the rate of 8 kHz/16kHz from the DSP via the voice serial interface VSP and converts them to analog signals to drive the external transducers.

The digital speech coming from the DSP is first fed to a speech digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate from 8kHz/16kHz up to 40kHz/80kHz to allow the digital–to–analog conversion to be performed by an over-sampling digital modulator. The second function is to band–limit the speech signal with both low–pass and high–pass transfer functions. The filter and PGA gain can be bypassed by programming the VDLFBYP bit in the CTRL1 register. The high-pass of the speech downlink filter can be bypassed using the VDLHPFBYP bit of the CTRL1 register.

The interpolated and band–limited signal is fed to a second order Σ–Δ digital modulator sampled at 1MHz/2MHz to generate a 4–bit (9 levels) over-sampled signal. This signal is then passed through a dynamic element matching block and then to a 4–bit digital–to–analog converter DAC.

Due to the over-sampling conversion, the analog signal obtained at the output of the 4–bit DAC is mixed with a high frequency noise. A first–order RC filter included in the output stage is enough to filter this noise.

The volume control and the programmable gain are performed in the RX digital filter. Volume control is performed in steps of 6 dB from 0 dB to -24 dB. In mute state, attenuation is higher than 40 dB. A fine adjustment of gain is possible from -6 dB to +6 dB in 1dB steps to calibrate the system depending on the earphone characteristics. This configuration is programmed with the VDLGAIN register.

The earphone amplifier provides a full differential signal on the terminals EARP and EARN (Earphone), and each output amplifier provides a single signal on terminals D+ and D- (USB Car Kit), Headset Right and Left (Headset). The 8 Ohms speaker amplifier provides a differential signal on the terminals SPKPA, SPKPD and SPKNA, SPKND (Handfree).

The downlink voice path can be powered down with the VDLR bit of the TOGB register.

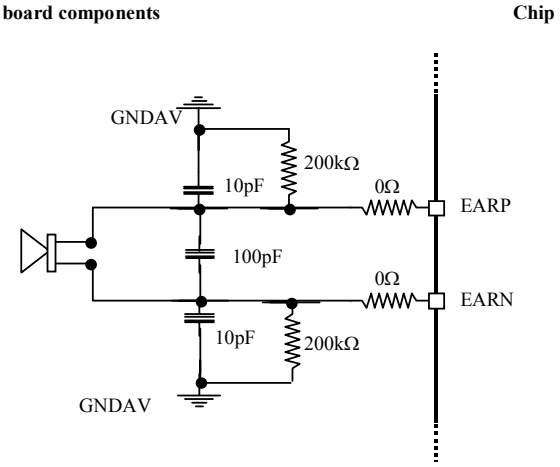
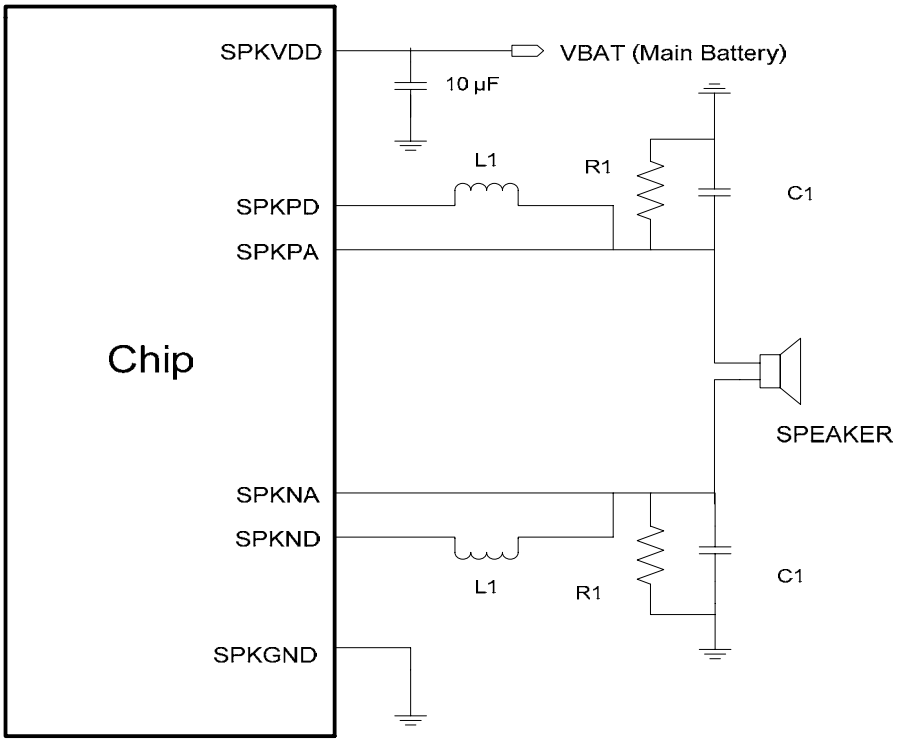


Figure 15 : Earphone Output



Note: Recommended values are in Table 31

The 10 µF capacitor between VBAT and ground has to filter the VBAT variations.
The 8 Ohms speaker and inductance must be connected as close as possible of the SPK outputs to avoid dynamic loss in connections.

Figure 16 : 8 Ohms Handfree Speaker Output

8.3 STEREO AUDIO PATH

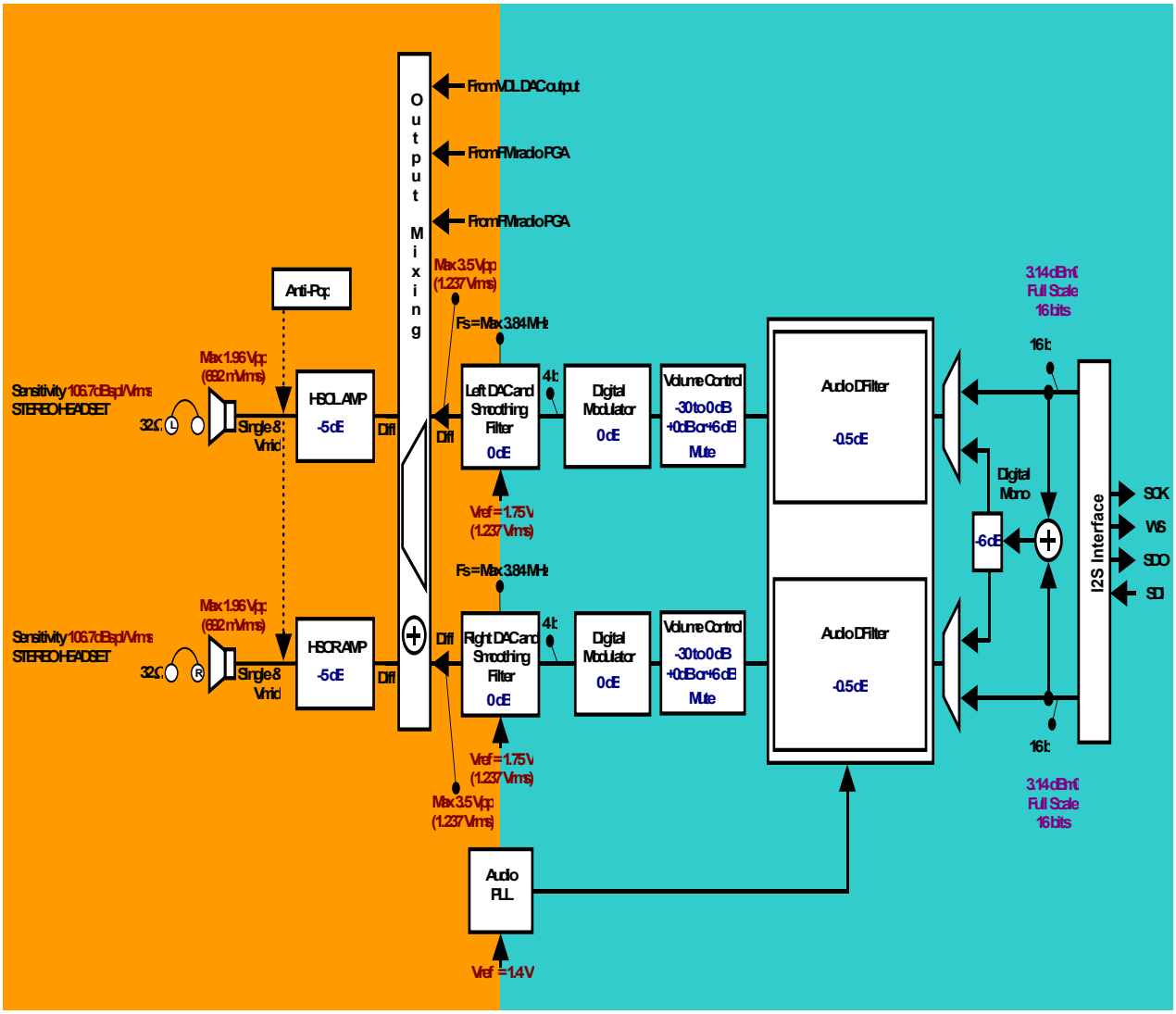


Figure 17 : Stereo Audio Path

The stereo audio path receives Left and right signal samples at the rate of a programmable frequency, from 8kHz to 48kHz, via the I2S serial interface and converts them to analog signals to drive the external audio signal or speech transducers.

The digital audio signal is first fed to an audio digital filter that has two functions. The first function is to interpolate the input signal and to increase the sampling rate to allow the digital–to–analog conversion to be performed by an over-sampling digital modulator. The second function is to band–limit the audio signal with a low–pass transfer functions. The interpolated and band–limited signal is fed to a second order Σ–Δ digital modulator sampled at f_{S1} frequency to generate a 4–bit (9 levels) over-sampled signal. This signal is then passed through a dynamic element matching block and then to a 4–bit digital–to–analog converter DAC.

Due to the over-sampling conversion, the analog signal obtained at the output of the 4–bit DAC is mixed with a high frequency noise. A first–order RC filter included in the output stage is enough to filter this noise.

The volume control is performed in the audio digital filter. Volume control is performed in steps of 1 dB from 0 dB to -30 dB. In mute state, attenuation is higher than 40 dB. The gain is independently programmable on the Left and Right channels, using the registers AUDLGAIN abd AUDRGAIN. A common adjustment of gain is possible at 0dB or +6dB (bit AUGA in CTRL4 register). A digital Left/Right adder and -6dB attenuator allows output of a mono audio path.

The left and right headset amplifiers provide the stereo signal on terminals HSOL and HSOR. A pseudo ground is provided on terminal HSOVMID to eliminate external capacitors. The mono audio signal can be provided on the Right or the Right and Left headset outputs. The mono audio signal can be added to the speech signal and provided on the Auxiliary, Earphone and/or 8 Ohms Speaker outputs. The Audio Stereo/Mono path can be powered down and configured with the TOGB, CTRL1, CTRL2, CTRL3, CTRL4, CTRL5 and CTRL6 registers.

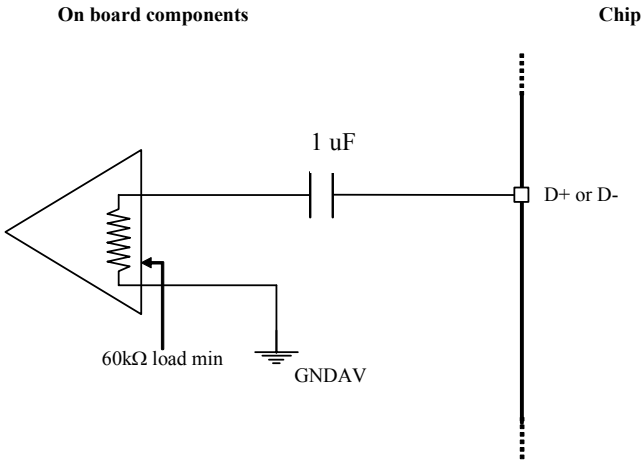


Figure 18 : Car Kit Outputs: Stereo mode (USB D+, D-) or Mono mode (USB D-)

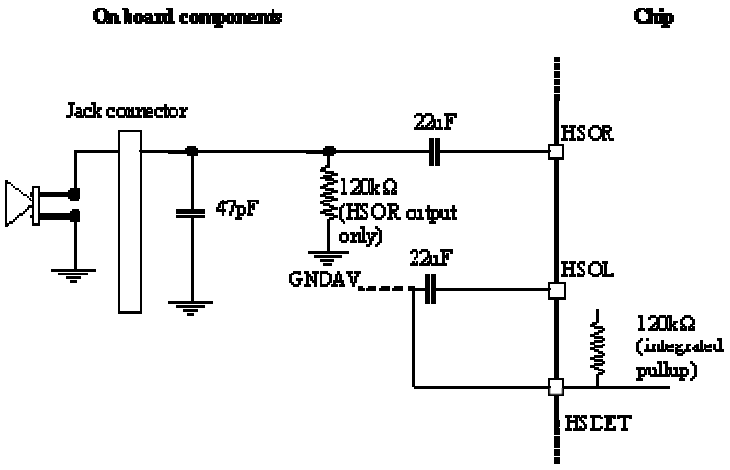


Figure 19 : Headset Stereo Speaker

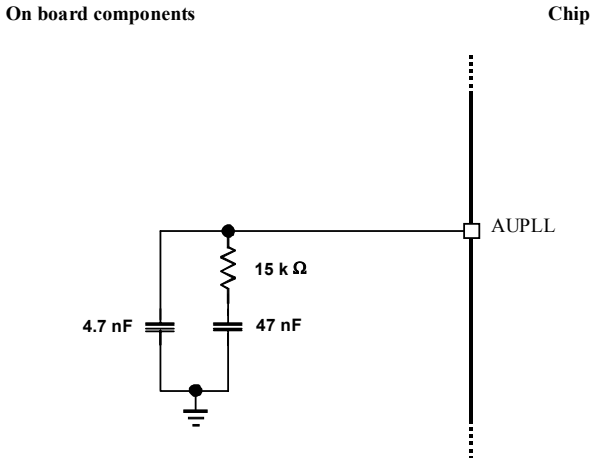


Figure 20 : Audio PLL External Filter

8.4 ANTI-POP

The Pop noise is due to the audio output amplifier which is switched on. The speaker is AC coupled through an external capacitor, the sharp rise time given by the activation of the bias causes a large 'spike' to propagate to the 32Ω earpiece which is uncomfortable to the user.

Pop cancellation is achieved through a pre-charge, and a discharge of the external coupling capacitor. Possible range for this charge and discharge timing considering process, temperature and supply variations is between 7 ms and 20 ms for charge.

The anti-pop system was implemented for every T3031 output except for the Handfree 8 ohms speaker.

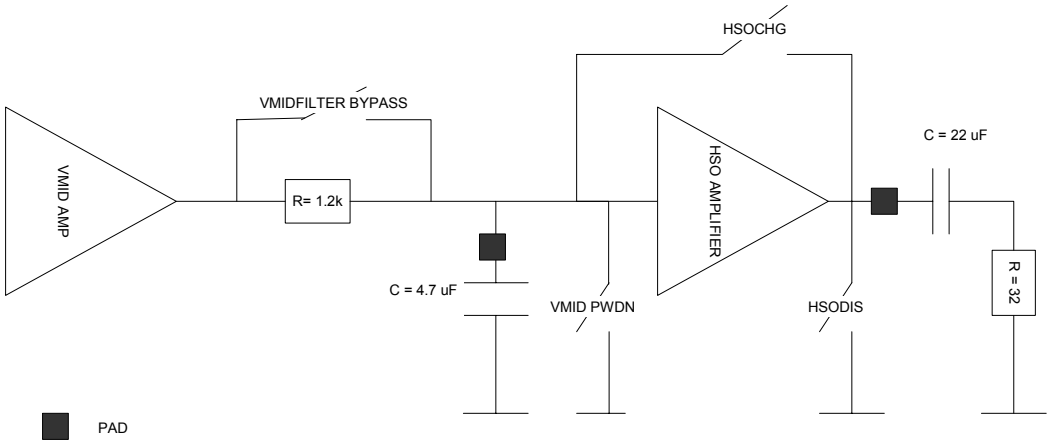


Figure 21 : Headset Anti-pop System

The principle is the charge of the external capacitor directly to the common mode voltage VMID with non audible frequencies avoiding the POP noise. For this system, the VMID amplifier with a low pass RC filter is used to load the external capacitor bypassing the Headset Amplifier. The external and filtering capacitors can be discharged and the anti-pop system can be started again.

This filtering functionality can be bypassed for the other amplifier.

8.5 VOICE SERIAL PORT

The Voice Serial Port (VSP) is a bi-directional (TX / RX) configurable serial port. It consists of four terminals:
VSP_VDX ➔ Data transmit
VSP_VDR ➔ Data receive
VSP_VFS ➔ Frame synchronization signal
VSP_VCK ➔ Clock signal
The format is a 16bit data packet with a frame synchronization.

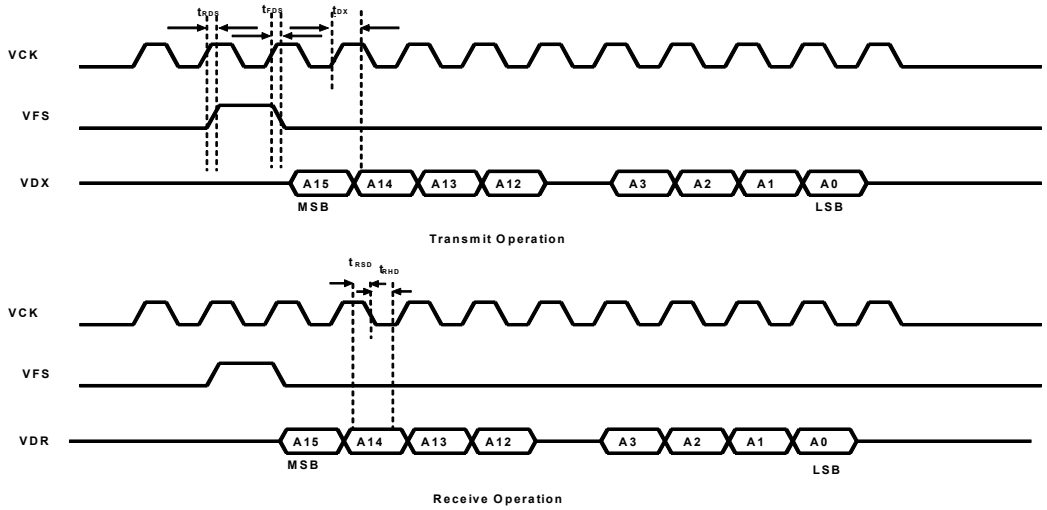


Figure 22 : Voice Serial Port Operations

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCK signal frequency	VSPCK=0		MCLK1/26		MHz
	VSPCK=1, WBA=0		MCLK1/13		
	VSPCK=1, WBA=1		2		
VCK signal jitter	VSPCK=0		+/- 2		us
	VSPCK=1, WBA=0		+/- 2		
	VSPCK=1, WBA=1		+/- 2		
VCK duty cycle	VSPCK=0		50		%
	VSPCK=1, WBA=0				
	VSPCK=1, WBA=1				
VFS signal frequency	WBA=0		8		kHz
	WBA=1		16		
Voice PLL lock time	Voice PLL ON		50		us

Table 26 : Voice Serial Port Timings

8.6 STEREO AUDIO SERIAL PORT

T3031 supports I2S audio interface master mode (T3031 provides the data clock SCK and the frame synchronization WS).

Two formats are available (selection bit: I2SLRJ in CTRL5 register):

- Right justified (default mode at reset): I2SLRJ = '0':

  20 bits word size (for each Left and Right word): 4 padding bits at '0' state and 16 bits data (MSB first);

- Left justified: set I2SLRJ to '1' state:

  20 bits word size (for each Left and Right word): 16 bits data (MSB first) and 4 padding bits at '0' state.

For each format: one bit shift: for a word of 20 bits, the first bit is available on the second rising edge of SCK, after the falling edge of WS (SCK = continuous serial clock, WS = word select, SDR = serial data to receive, SDX = serial data to transmit).

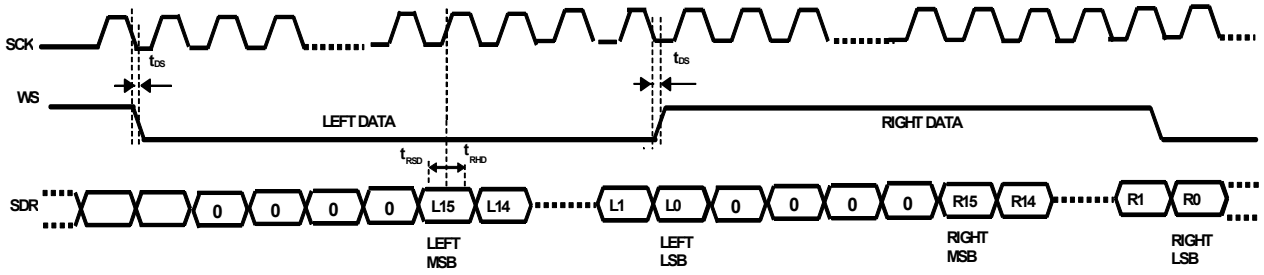


Figure 23 : Right Justified Format , Audio Serial Port

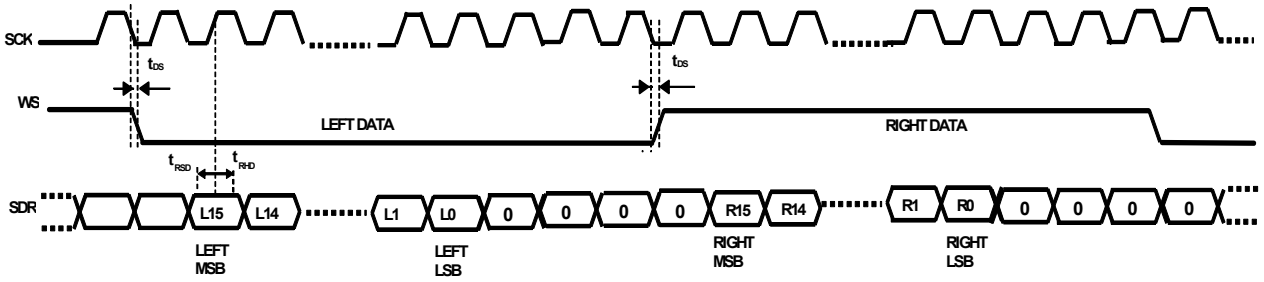


Figure 24 : Left Justified Format , Audio Serial Port

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Left/Right N bits to receive			16		Bit
Total data to receive (Left + Right) = 2x(N+4)			40		Bit
SCK clock frequency = 1/T			40*WS		kHz
SCK duty cycle			50		%
Signal frequency	others		48		kHz
Default configuration ⇒	SRW [3:0] = 1000		48		
	SRW[3:0] = 0111		44.1		
	SRW[3:0] = 0110		32		
	SRW[3:0] = 0101		24		
	SRW[3:0] = 0100		22.05		
	SRW[3:0] = 0011		16		
	SRW[3:0] = 0010		12		
	SRW[3:0] = 0001		11.025		
	SRW[3:0] = 0000		8		
WS duty cycle			50		%
Stereo Audio PLL lock time			10		ms

Table 27 : Audio Serial Port Timings

8.7 REGISTERS

8.7.1 TOGB

Register	TOGB							
Page	0	Address	Dec # 208	Hex 0xD0				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	STS	STR	VDLS	VDLR	VULS	VULR
Read/Write	R	R	W	W	W	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 6)	Reserved bits
STS	Writing '1' in this bit clears the STON bit of the PWRONSTATUS register to '1'
STR	Writing '1' in this bit clears the STON bit of the PWRONSTATUS register to '0'
VDLS	Writing '1' in this bit clears the VDLON bit of the PWRONSTATUS register to '1'
VDLR	Writing '1' in this bit clears the VDLON bit of the PWRONSTATUS register to '0'
VULS	Writing '1' in this bit clears the VULON bit of the PWRONSTATUS register to '1'
VULR	Writing '1' in this bit clears the VULON bit of the PWRONSTATUS register to '0'

8.7.2 PWRONSTATUS

Register	PWRONSTATUS							
Page	0	Address	Dec # 209	Hex 0xD1				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	RSVRD	SPKON	STON	VDLON	VULON
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 4)	Reserved bits
SPKON	This bit is set to '1' when the Hands-free speaker amplifier is powered on, that is to say when SPK(2:0) bits in OUTEN3 register are set to a value between "001" and "110".
STON	When this bit is cleared to '0', the Stereo downlink path STEREO DIG FILTER + STEREO DAC is in power-down mode. This bit is set to '1' by the STS bit and reset by the STR bit of toggle bits register TOGB
VDLON	When this bit is cleared to '0', the Voiceband downlink path VSP + DIG FILTER + VOICE DAC is in power-down mode. This bit is set to '1' by the VDLS bit and reset by the VDLR bit of toggle bits register TOGB
VULON	When this bit is cleared to '0', the Voiceband uplink path VSP + DIG FILTER + VOICE DAC is in power-down mode. This bit is set to '1' by the VULS bit and reset by the VULR bit of toggle bits register TOGB

8.7.3 CTRL1

Register	CTRL1							
Page	0	Address	Dec # 210		Hex 0xD2			
Bit	7	6	5	4	3	2	1	0
Name	VALOOP	VDLHPFBYP	VDLFBYP	VSPCK	VSYNC	VCLKMODE	BOOST	WBA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

VALOOP	When this bit is set to 1, the internal analog loop of the output samples is sent to the input of the audio ADC. To avoid saturation of the analog path in this mode you must set: PGA downlink = -6 dB, PGA uplink = 0 dB, Volume = 0 dB, and SideTone = MUTE
VDLHPFBYP	Voice speech digital high pass filter bypass (active if VDLHPFBYP=1)
VDLFBYP	When this bit is set to 1, the whole Voice Downlink digital filter is bypassed.
VSPCK	VSPCK= 0: set the VCK frequency to 500-kHz VSPCK= 1, WBA= 0: set the VCK frequency to 1MHz, VSPCK= 1, WBA= 1: set the VCK frequency to 2MHz
VSYNC	When this bit is set to 1, the digital modulator, the digital voice serial port, and the digital filter are reset. At the reset using VDR, the filter will set VSYNC to 0.
VCLKMODE	When this bit is cleared to 0, this bit allows selection of the VCK in burst mode. When this bit is set to 1, this bit allows selection of the VCK in continuous mode.
BOOST	Increase (BOOST= 1) the drive capability of Voice up-link input amplifier stages. It is recommended to set this bit at '1' state in Wideband mode.
WBA	Voice Speech path operating with Wide Band (8-kHz bandwidth, WBA=1) or narrow band (4kHz bandwidth, WBA= 0)

8.7.4 CTRL2

Register	CTRL2							
Page	0	Address	Dec # 211		Hex 0xD3			
Bit	7	6	5	4	3	2	1	0
Name	VMIDSEL	VMIDRBYP	MICBIASLVL	MICBIASSEL	FMG_3	FMG_2	FMG_1	FMG_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

VMIDSEL	When this bit is set to 1, Audio output VMID is set to 1.5 V, else output VMID is set to 1.35 V.
VMIDRBYP	If VMIDRBYP='1': bypass the internal resistance R of the VMID low-pass RC filter (external C connected to AUVMID terminal) (the audio VMID is an internal reference).
MICBIASLVL	When this bit is cleared to 0, the analog bias for the electric microphone and external decoupling is driven to 2 V. When this bit is set to 1, the bias is driven to 2.5 V.
MICBIASSEL	When this bit is set to 1, HSMICBIAS is active else MICBIAS is active. MICBIAS/HSMICBIAS is powered on if VULON is set to '1' and INMODE(3:0) ≠ "0000".
FMG [3:0]	FM Radio analog programmable relative gain (absolute gain at mic/auxi amp out = 4.9 dB + relative gain)

FMPG3	FMPG2	FMPG1	FMPG0	Rel. Gain	Abs. Gain
0	0	0	0	0 dB	4.9 dB
0	0	0	1	2 dB	6.9 dB
0	0	1	0	4 dB	8.9 dB
0	0	1	1	6 dB	10.9 dB

	0	1	0	0	8 dB	12.9 dB
	0	1	0	1	10 dB	14.9 dB
	0	1	1	0	12 dB	16.9 dB
	0	1	1	1	14 dB	18.9 dB
	1	0	0	0	-2 dB	2.9 dB
	Others				0 dB	4.9 dB

Notes:
- FM Radio analog gains are relative to the default MIC and AUXI amplifiers gain (4.9 dB) in FM Radio mode (FMG = "0000" at reset);
- FM Radio analog programmable gains are not available when the chosen INMODE (see CTRL3 register) is not Stereo FM Radio (INMODE = "0100" for FM Radio).

8.7.5 CTRL3

Register	**CTRL3**							
Page	**0** Address		**Dec # 212**		**Hex 0xD4**			
Bit	7	6	5	4	3	2	1	0
Name	SPKDIGON	SPKG_2	SPKG_1	SPKG_0	INMODE_3	INMODE_2	INMODE_1	INMODE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

SPKDIGON	If set to '0': Handfree Class D part is off. If PWDNSPK = '0', Class AB part is on; If set to '1': Handfree Class D part is on. If PWDNSPK = '0', Class AB part is on when the Voice PLL is activated. (See ***)
SPKG [2:0]	000: SPKAMP gain is +8.5 dB 001: SPKAMP gain is +2.5 dB 010: SPKAMP gain is +2.5 dB 011: SPKAMP gain is -3.5 dB (Handfree performance not guaranteed) 100: SPKAMP gain is -22.5 dB (Handfree performance not guaranteed)
INMODE [3:0]	0000: No input selected (See **) 0001: MIC IN (diff): Selected inputs: MICIP, MICIN. Amplifier: MIC AMP, Gain = 25.6 dB 0010: HSMIC IN (diff): Selected inputs: HSMIC, AUXI/FMR. Amplifier: MIC AMP, Gain = 4.9 dB 0011: HSMIC IN (diff): Selected inputs: HSMIC, AUXI/FMR. Amplifier: MIC AMP, Gain = 25.6 dB 0100: FM IN Stereo (2x single): Selected inputs: FML, AUXI/FMR. Amp(s): MIC & AUXI AMPS, Gain = 4.9 dB 0101: HSMIC IN (1x single): Selected input: HSMIC. Amplifier: AUXI AMP, Gain = 18 dB 0110: AUXI IN (1x single): Selected input: AUXI/FMR. Amplifier: AUXI AMP, Gain = 4.9 dB 0111: AUXI IN (1x single): Selected input: AUXI/FMR. Amplifier: AUXI AMP, Gain = 28.2 dB 1000: FM IN Mono (1x single): Selected input: FMR. Amplifier: AUXI AMP, Gain = 4.9 dB 1001: CAR KIT IN MONO (1x single): Selected input: USB D+. Amplifier: AUXI AMP, Gain = 2.6 dB (See *)

Notes:
(*): D+ analog input is enabled and AUXI amplifier powered on if INMODE = 1001 AND CARKITMICEN = 1;
(**): MICBIAS/HSMICBIAS is powered on if VULON is set to '1' and INMODE(3:0) ≠ "0000";
(***): PWDNSPK is internally generated from SPK(2:0) bits (see register OUTEN3): if SPK(2:0) ≠ "000" or ≠ "111", the Hands-free speaker amp is used and PWDNSPK is set to '0'.

8.7.6 CTRL4

Register	**CTRL4**							
Page	**0** Address		**Dec # 213**		**Hex 0xD5**			
Bit	7	6	5	4	3	2	1	0
Name	VMEMO	I2SON	MONOL	MONOR	AUGA	SFTVOL	SFTVOL	RSVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

VMEMO	When this bit is set to 1, the Voice digital uplink samples (transmit VDX) are routed to the I2S interface, transmit AUDX port. Only 8kHz and 16kHz Audio mode are supported. No merge from Voice uplink samples to Audio mono data path. The Voice transmit samples through the I2S transmit path can be used for Voice memo application.
I2SON	Set the power on of the I2S serial Interface (I2SON=1) if STON already set to '1'.
MONOL †	Convert Stereo signal to mono signal and transmit on left channel (MONOL=1)
MONOR †	Convert Stereo signal to mono signal and transmit on right channel (MONOR=1)
AUGA †	Audio Stereo Left & Right channels Digital Volume control: AUGA — Relative Gain 0 — 0 dB 1 — +6 dB
SFTVOL [1:0] †	Audio Stereo/Mono Soft volume control : SFTVOL1 — SFTVOL0 — Data format 0 — 0 — 1/FS×512 0 — 1 — 1/FS×128 1 — 0 — 1/FS×8 1 — 1 — 1/FS×1/2
RSVD	Reserved.
† The value of this control bits should not be changed when STON='1' (PWONSTATUS register).	

8.7.7 CTRL5

Register	CTRL5							
Page	0	Address	Dec # 214	Hex 0xD6				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	I2SLRJ	EARG	HOOKEN	SRW_3	SRW_2	SRW_1	SRW_0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7)	Reserved bits
I2SLRJ	I2S word data Left or Right justification: 0: Right justified 1: Left justified
EARG	When this bit is set to: 0: EARAMP gain is –11 dB 1: EARAMP gain is 1 dB
HOOKEN††	Hook detection enable bit (defaut state = disabled): must be set to '1' state after the settling time needed by the HSMICBIAS power on.
SRW [3:0] †	Stereo Audio Sampling rate frequency SRW3 — SRW2 — SRW1 — SRW0 — Sampling frequency (AUCK freq. = 40*FS) 1 — 0 — 0 — 0 — 48 kHz 0 — 1 — 1 — 1 — 44.1 kHz 0 — 1 — 1 — 0 — 32 kHz 0 — 1 — 0 — 1 — 24 kHz 0 — 1 — 0 — 0 — 22.05 kHz 0 — 0 — 1 — 1 — 16 kHz 0 — 0 — 1 — 0 — 12 kHz 0 — 0 — 0 — 1 — 11.025 kHz 0 — 0 — 0 — 0 — 8 kHz others — Not used

† The value of this control bits should not be changed when STON='1' (PWONSTATUS register).
†† Warning: the HOOKEN bit must be set to '1' after programming MICBIASSEL (CTRL2 register) at '1':
Application sequence:

- Set HSMICBIAS value (2V or 2.5V): set bit #5 MICBIASLVL in CTRL2 register;
- Set VULON: set bit #1 VULS ='1' in TOGB register;

- Select HSMICBIAS: set bit #4 MICBIASSEL = '1' in CTRL2 register;
- Wait HSMICBIAS power on settling time
- Set bit #4 HOOKEN = '1' in CTRL5 register.

To Disable HOOK feature: HOOKEN bit must be set to '0', before any VULOFF (VULR='1' in TOGB register).

8.7.8 CTRL6

Register	CTRL6							
Page	0	Address	Dec # 215	Hex 0xD7				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	STPLL SPEEDUP	STPLL PCHGZ	VPLL PCHGZ	STPLLON	VPLLON
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 5)	Reserved bits
STPLLSPEEDUP	Audio Stereo PLL speed-up (settling time) (active high)
STPLLPCHGZ	Audio Stereo PLL pre-charge (active low).
VPLLPCHGZ	Voice PLL pre-charge (active low).
STPLLON	Audio stereo PLL power up (active high).
VPLLON	Voice PLL power up (active high).

8.7.9 POPMAN

Register	POPMAN							
Page	0	Address	Dec # 216	Hex 0xD8				
Bit	7	6	5	4	3	2	1	0
Name	CARKIT DHG	CARKIT CHG	RSVRD	RSVRD	EARDHG	EARCHG	HSODHG	HSOCHG
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

x-DHG † (bits: 7-5-3-1)	Enable the discharge of the external capacitor connected to AUVMID. This bit has NO effect when xCHG is set to '1' or when VDLON (or STON) is set to '0' or when corresponding audio output is set on
x-CHG † (bits: 6-4-2-0)	Enable the charge of the internal VMID through the external capacitor connected to AUVMID terminal. During this phase, the amplifier x output(s) is short-circuited to the internal VMID. This bit has NO effect when VDLON (or STON) is set to '0' or when AUTOMATIC MODE is running

† x is EAR for Earphone EAR outputs, HSO for HSOL and HSOR for headset outputs or CARKIT for CARKITL and CARKITR outputs

Important note: car kit anti-pop control (Manual or Automatic mode):

- CARKITCHG and CARKITDHG controls are effective for left car kit amplifier only if USBCARKITLEN = '1';
- CARKITCHG and CARKITDHG controls are effective for right car kit amplifier only if USBCARKITREN = '1';
- USBCARKITLEN, USBCARKITREN description: see OUTEN2 register;
- This hardware protection avoids to use the anti-pop system during an USB data transmission on D+ and D- pins, and then avoid to loose data.

8.7.10 POPAUTO

Register	POPAUTO							
Page	0	Address	Dec # 217		Hex 0xD9			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	RSVRD	CARKITAUTO	RSVRD	EARAUTO	HSOAUTO
Read/Write	R	R	R	R	R/W	R	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 4)	Reserved bits
x-AUTO †	'1' means that xCHG functionality runs in AUTOMATIC mode '0' in MANUAL mode AUTOMATIC Mode: xCHG (with VMIDRBYP='1') control bit is set automatically to '1' when VDLON (or STON) rise. This bit is cleared automatically to '0' when the corresponding audio output is set on MANUAL Mode: xCHG control bit bit has NO effect when the corresponding audio output is set on

† x is EAR for Earphone EAR outputs, HSO for HSOL and HSOR for headset outputs or CARKIT for CARKITL and CARKITR outputs

8.7.11 SIDETONE

Register	SIDETONE							
Page	0	Address	Dec # 218		Hex 0xDA			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	RSVRD	VST_3	VST_2	VST_1	VST_0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 4)	Reserved bits
VST [3:0]	Side tone levels:

VST3	VST2	VST1	VST0	Relative Gain
1	1	0	1	-23 dB
1	1	0	0	-20 dB
0	1	1	0	-17 dB
0	0	1	0	-14 dB
0	1	1	1	-11 dB
0	0	1	1	-8 dB
0	0	0	0	-5 dB
0	1	0	0	-2 dB
0	0	0	1	1 dB
0	1	0	1	1 dB
1	0	0	0	Mute
1	0	0	1	Mute
1	0	1	0	Mute
1	0	1	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

8.7.12 VULGAIN

Register	VULGAIN							
Page	0	Address	Dec # 219		Hex 0xDB			
Bit	7	6	5	4	3	2	1	0
Name	RSVD	RSVD	DXEN	VULPG_4	VULPG_3	VULPG_2	VULPG_1	VULPG_0

Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVD (bit 7 – bit 6)	Reserved bits
DXEN	When this bit is set to 1, the VDX signal is in mute mode. If this bit is cleared to 0, the VDX signal is in normal mode.
VULPG [4:0]	Voice uplink digital programmable gain: **VULPG4 / VULPG3 / VULPG2 / VULPG1 / VULPG0 / Relative Gain** 1 0 0 0 0 -12 dB 1 0 1 1 1 -11 dB 1 1 0 0 0 -10 dB 1 1 0 0 1 -9 dB 1 1 0 1 0 -8 dB 1 1 0 1 1 -7 dB 0 0 0 0 0 -6 dB 0 0 0 0 1 -5 dB 0 0 0 1 0 -4 dB 0 0 0 1 1 -3 dB 0 0 1 0 0 -2 dB 0 0 1 0 1 -1 dB 0 0 1 1 0 0 dB 0 0 1 1 1 1 dB 0 1 0 0 0 2 dB 0 1 0 0 1 3 dB 0 1 0 1 0 4 dB 0 1 0 1 1 5 dB 0 1 1 0 0 6 dB 1 0 0 0 1 7 dB 1 0 0 1 0 8 dB 1 0 0 1 1 9 dB 1 0 1 0 0 10 dB 1 0 1 0 1 11 dB 1 0 1 1 0 12 dB

8.7.13 VDLGAIN

Register	VDLGAIN							
Page	0	Address	Dec # 220	Hex 0xDC				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	VOLCTL_2	VOLCTL_1	VOLCTL_0	VDLPG_3	VDLPG_2	VDLPG_1	VDLPG_0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7)	Reserved bit
VOLCTL [2:0]	Volume control (PGA Course gain) **VOLCTL2 / VOLCTL1 / VOLCTL0 / Relative Gain** 0 1 0 0 dB 1 1 0 -6 dB 0 0 0 -12 dB 1 0 0 -18 dB 0 1 1 -24 dB 1 0 1 Mute 0 0 1 Mute 1 1 1 Mute
VDLPG [3:0]	Voice downlink digital programmable gain (PGA fine gain) **VDLPG3 / VDLPG2 / VDLPG1 / VDLPG0 / Relative Gain** 0 0 0 0 -6 dB 0 0 0 1 -5 dB 0 0 1 0 -4 dB

	0	0	1	1	-3 dB
	0	1	0	0	-2 dB
	0	1	0	1	-1 dB
	0	1	1	0	0 dB
	0	1	1	1	1 dB
	1	0	0	0	2 dB
	1	0	0	1	3 dB
	1	0	1	0	4 dB
	1	0	1	1	5 dB
	1	1	0	0	6 dB
	1	1	0	1	-6 dB
	1	1	1	0	-6 dB
	1	1	1	1	-6 dB

8.7.14 OUTEN1

Register	**OUTEN1**							
Page	**0**	Address	**Dec # 221**		**Hex 0xDD**			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	HSOL_2	HSOL_1	HSOL_0	HSOR_2	HSOR_1	HSOR_0	HSOVMID
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVD (bit 7)	Reserved bit
HSOL [2:0]	HSOL AMP Audio output control **HSOL2** / **HSOL 1** / **HSOL0** / **output signal** 0 0 0 none (HSOL amp powered down) 0 0 1 Voice Speech 0 1 0 Audio Left / Audio Mono 0 1 1 FM Left from VUL FM PGA (FML input) 1 0 0 Voice Speech + Audio Left / Audio Mono 1 0 1 Voice Speech + FM Left 1 1 0 Audio Left / Audio Mono + FM Left 1 1 1 Voice Speech
HSOR [2:0]	HSOR AMP Audio output control **HSOR2** / **HSOR 1** / **HSOR 0** / **output signal** 0 0 0 none (HSOR amp powered down) 0 0 1 Voice Speech 0 1 0 Audio Right / Audio Mono 0 1 1 FM Right from VUL FM PGA (FMR/AUXI inp.) 1 0 0 Voice Speech + Audio Right / Audio Mono 1 0 1 Voice Speech + FM Right 1 1 0 Audio Right / Audio Mono + FM Right 1 1 1 Inverted Voice Speech
HSOVMID	When this bit is set to 1, HSOVMID is powered up (if VDLON or STON = 1), else HSOVMID is powered down

Note: OUTEN1 register contains enable bits to select the channels to amplify and power on the suitable amplifiers.

8.7.15 OUTEN2

Register	**OUTEN2**							
Page	**0**	Address	**Dec # 222**		**Hex 0xDE**			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	CARKIT_1	CARKIT_0	RSVRD	RSVRD	EAR_1	EAR_0
Read/Write	R	R	R/W	R/W	R	R	R/W	R/W

Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD	Reserved bit
CARKIT [1:0]	CAR KIT AMP Audio output control **CARKIT 1** **CARKIT 0** **output signal** 0 0 none (CAR KIT L & R amps powered down) 0 1 Voice Speech on Left amp (D-) (*) 1 0 Audio Stereo on Left & Right amps (D-, D+) (*)(**) 1 1 Voice Speech + Audio Mono on Left amp (D-) (*)
RSVRD	Reserved bit
EAR [1:0]	EAR AMP Audio output control **EAR 1** **EAR** **output signal** 0 0 none (EAR amp powered down) 0 1 Voice Speech 1 0 Audio Mono (from Left channel) 1 1 Voice Speech + Audio Mono

Notes:

- OUTEN2 register contains enable bits to select the channels to amplify and power on the suitable amplifiers;
- Car Kit output drivers are also controlled by dedicated signals from the USB digital control: USBCARKITLEN and USBCARKITREN:
  - These signals are active if CARKIT(1-0) is not “00”;
  - **(*)** If USBCARKITLEN = ‘1’, Car Kit Left amplifier can be used in three configurations: CARKIT(1:0) = “01” , “10” or “11”;
  - **(**)** If USBCARKITREN = ‘1’, Car Kit Right amplifier can be used in one configuration: CARKIT(1:0) = “10”. USBCARKITREN must be at ‘0’ state for the other CARKIT(1:0) cases.
  - **Car Kit Decoding table:**
    - When CARKIT(1:0) = “01”: if USBCARKITLEN = ‘1’ **and** USBCARKITREN = ‘0’ then: Voice speech on Car Kit Left amplifier;
    - When CARKIT(1:0) = “10”: if USBCARKITLEN = ‘1’ **and** USBCARKITREN = ‘1’ then: Audio Left on Car Kit Left amplifier, Audio Right on Car Kit Right amplifier;
    - When CARKIT(1:0) = “11”: if USBCARKITLEN = ‘1’ **and** USBCARKITREN = ‘0’ then: Voice speech + Audio Mono on Car Kit Left amplifier.
  - Car Kit Left amplifier output is connected to the DN pin (USB D-);
  - Car Kit Right amplifier output is connected to the DP pin (USB D+);
- USBCARKITLEN and USBCARKITREN signals are built from the USB toggle registers called CTRL_3_SET and CTRL_3_CLR:
  - Bits 5 & 4: status bits; Bits 3 & 2: Set and Reset bits.

8.7.16 OUTEN3

Register	**OUTEN3**							
Page	**0** Address	**Dec # 223**	**Hex 0xDF**					
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVD	RSVD	RSVD	SPK_2	SPK_1	SPK_0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 3)	Reserved bits
SPK [2:0]	HANDFREE AMP Audio output control **SPK2** **SPK1** **SPK0** **output signal**

	0	0	0	none (SPK amp powered down)
	0	0	1	Voice Speech
	0	1	0	Audio Mono (from Left channel)
	0	1	1	FM Mono from VUL FM PGA (FMR/AUXI inp.)
	1	0	0	Voice Speech + Audio Mono
	1	0	1	Voice Speech + FM Mono
	1	1	0	Audio Mono + FM Mono
	Others			none (SPK amp powered down)

Note: OUTEN3 register contains enable bits to select the channels to amplify and power on the suitable amplifiers.

8.7.17 AUDLGAIN

Register	AUDLGAIN							
Page	0	Address	Dec # 224	Hex 0xE0				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	AULGA_4	AULGA_3	AULGA_2	AULGA_1	AULGA_0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 5)	Reserved bits					
AULGA [4:0]	Audio Stereo Left channel Volume control					
	AULGA4	**AULGA3**	**AULGA2**	**AULGA1**	**AULGA0**	**Rel. Gain**
	0	0	0	0	0	0 dB
	0	0	0	0	1	-1 dB
	0	0	0	1	0	-2 dB
	0	0	0	1	1	-3 dB
	0	0	1	0	0	-4 dB
	0	0	1	0	1	-5 dB
	0	0	1	1	0	-6 dB
	0	0	1	1	1	-7 dB
	0	1	0	0	0	-8 dB
	0	1	0	0	1	-9 dB
	0	1	0	1	0	-10 dB
	0	1	0	1	1	-11 dB
	.	.	.	.	.	.
	.	.	.	.	.	.
	.	.	.	.	.	.
	1	1	1	0	1	-29 dB
	1	1	1	1	0	-30 dB
	1	1	1	1	1	Mute

8.7.18 AUDRGAIN

Register	AUDRGAIN							
Page	0	Address	Dec # 225	Hex 0xE1				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	AURGA_4	AURGA_3	AURGA_2	AURGA_1	AURGA_0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 5)	Reserved bits					
AURGA [4:0]	Audio Stereo Right channel Volume control					
	AURGA4	**AURGA3**	**AURGA2**	**AURGA1**	**AURGA0**	**Rel. Gain**
	0	0	0	0	0	0 dB
	0	0	0	0	1	-1 dB
	0	0	0	1	0	-2 dB
	0	0	0	1	1	-3 dB

	0	0	1	0	0	-4 dB
	0	0	1	0	1	-5 dB
	0	0	1	1	0	-6 dB
	0	0	1	1	1	-7 dB
	0	1	0	0	0	-8 dB
	0	1	0	0	1	-9 dB
	0	1	0	1	0	-10 dB
	0	1	0	1	1	-11 dB
	.	.	.	.	.	.
	.	.	.	.	.	.
	.	.	.	.	.	.
	1	1	1	0	1	-29 dB
	1	1	1	1	0	-30 dB
	1	1	1	1	1	Mute

8.7.19 AUDINTSTS

Register	AUDINTSTS							
Page	0	Address	Dec # 234		Hex 0xEA			
Bit	7	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	HOOK STATUS	HEADSET STATUS
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	1	1

Register bits description

RSVD (bit 7 to bit 2)	Reserved bits
HOOK STATUS	Status bit which reflects the hook push button detection status: default state = 1 means button release state (button switch open). 1: Unhook 0: Hook
HEADSET STATUS	Status bit which reflects the headset plug detection status: default state = 1 means an unplug state. 1: Unplug 0: Plug

8.7.20 HFTEST1

Register	HFTEST1							
Page	0	Address	Dec # 232		Hex 0xE8			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	SPKALLZB
Read/Write	R	R	R	R	R	R	R	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 1)	Reserved bits (Note: don't modify RSRVD bits default values)
SPKALLZB	If set to '0', the Class D outputs are in HighZ when SPKDIGON = '0' If set to '1': - the Class D outputs are connected to ground when SPKDIGON = '0' and SPKPMOSALLON = '0' (to measure the on resistance of the Nmos bridge or to discharge the inductance current); - the Class D outputs are connected to VBAT when SPKDIGON = '0' and SPKPMOSALLON = '1' (tp measure the on resistance of the Pmos bridge).

8.8 ELECTRICAL CHARACTERISTICS

Audio Inputs Characteristics

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum differential input range (MICIP-MICIN)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *MICAMP* gain = 25.6dB, Differential MIC			32.5	mVrms
Maximum input range (AUXI)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *AUXAMP* gain=28.2dB, Single AUXI			24	mVrms
Maximum input range (AUXI)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *AUXAMP* gain=4.9dB, Single AUXI			353	mVrms
Maximum input range (HSMIC)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *AUXAMP* gain = 18dB, Single HSMIC			78	mVrms
Maximum differential input range (HSMIC-AUXI)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *MICAMP* gain = 25.6dB, Differential HSMIC			32.5	mVrms
	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *MICAMP* gain = 4.9dB, Differential HSMIC			353	mVrms
Maximum input range FML	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *MICAMP* gain=4.9dB, Single FML			353	mVrms
Maximum input range FMR (= AUXI)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *AUXAMP* gain=4.9dB, Single FMR (AUXI)			353	mVrms
Maximum input range CKMIC (= USB D+)	Inputs 3 dBm0 (Maximum digital sample amplitude with PGA gain set to 0 dB), *AUXAMP* gain=2.6dB, Single CKMIC (USB D+)			478	mVrms
Nominal reference level (MICIP-MICIN)	Differential MIC		-10		dBm0
Nominal reference level at (AUXI/FMR)	Single AUXI/FMR		-10		dBm0
Nominal reference level at (HSMIC)	Single HSMIC		-10		dBm0
Nominal reference level at (HSMIC-AUXI)	Differential HSMIC		-10		dBm0
Nominal reference level at FML	Single FML		-10		dBm0
Nominal reference level at CKMIC	Single CKMIC		-10		dBm0
Differential input resistance (MICIP-MICIN)	Differential MIC, *MICAMP* gain = 25.6 dB (INMODE = 0001)		36		kΩ
Differential input resistance (HSMIC-AUXI)	Differential HSMIC, *MICAMP* gain = 4.9 dB (INMODE = 0010)		261		kΩ
	Differential HSMIC, *MICAMP* gain = 25.6 dB (INMODE = 0011)		36		kΩ
Micro amplifier gain for (MICIP-MICIN) input	Differential MIC (INMODE = 0001)		25.6		dB
Micro amplifier gain for (HSMIC-AUXI) input	Differential HSMIC (INMODE = 0010)		4.9		dB
	Differential HSMIC (INMODE = 0011)		25.6		dB
Micro amplifier gain for FML input	Single FML input for FM Stereo (INMODE = 0100)		4.9		dB
Auxiliary amplifier gain for AUXI/FMR input	Single AUXIFMR input for FM Stereo (INMODE = 0100)		4.9		dB
	Single AUXI input, low gain (INMODE = 0110)		4.9		dB
	Single AUXI input, high gain (INMODE = 0111)		28.2		dB
Auxiliary amplifier gain for HSMIC input	Single HSMIC input (INMODE = 0101)		18		dB
Auxiliary amplifier gain for CKMIC input	Single AUXI input (INMODE = 1001), CARKITMICEN = 1		2.6		dB

Input resistance at AUXI/FMR	Single AUXI input, *AUXAMP* gain = 4.9 dB (INMODE = 0110)	130.5		kΩ
	Single AUXI input, *AUXAMP* gain = 28.2 dB (INMODE = 0111)	13.5		kΩ
	FM Mono (INMODE = 1000), *AUXAMP* gain = 4.9 dB	130.5		kΩ
	FM Stereo (INMODE = 0100), *AUXAMP* gain from 2.9 dB to 18.9 dB	36		kΩ
Input resistance at HSMIC	HSMIC single input, *AUXAMP* gain = 18 dB (INMODE = 0101)	40.5		kΩ
Input resistance at FML	FM Stereo (INMODE = 0100), *MICAMP* gain from 2.9 dB to 18.9 dB	36		kΩ
Input resistance at DP (Car Kit Mic input)	Single AUXI input, *AUXAMP* gain = 2.6 dB (INMODE = 1001, CARKITMICEN = '1')	195		kΩ
DC level at MICBIAS	MICBIASLVL bit = 0, $I_{MICBIAS}$ = 0 to 2 mA	1.9	2.1	V
	MICBIASLVL bit = 1, $I_{MICBIAS}$ = 0 to 2 mA	2.4	2.6	V
DC level at HSMICBIAS	MICBIASLVL bit = 0, $I_{MICBIAS}$ = 0 to 2 mA	1.9	2.1	V
	MICBIASLVL bit = 1, $I_{MICBIAS}$ = 0 to 2 mA	2.4	2.6	V
Current capability at MICBIAS			2	mA
Current capability at HSMICBIAS			2	mA
SPK common mode value		SPKV DD/2		V

Table 28 : Audio Inputs Characteristics

Voiceband Uplink Path Characteristics

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PGA absolute gain	VULPGA code 10000 -12 dB		-12		dB
	VULPGA code 10111 -11 dB		-11		
	VULPGA code 11000 -10 dB		-10		
	VULPGA code 11001 -9 dB		-9		
	VULPGA code 11010 -8 dB		-8		
	VULPGA code 11011 -7 dB		-7		
	VULPGA code 00000 -6 dB		-6		
	VULPGA code 00001 -5 dB		-5		
	VULPGA code 00010 -4 dB		-4		
	VULPGA code 00011 -3 dB		-3		
	VULPGA code 00100 -2 dB		-2		
	VULPGA code 00101 -1 dB		-1		
	VULPGA code 00110 0 dB		0		
	VULPGA code 00111 1 dB		1		
	VULPGA code 01000 2 dB		2		
	VULPGA code 01001 3 dB		3		
	VULPGA code 01010 4 dB		4		
	VULPGA code 01011 5 dB		5		
	VULPGA code 01100 6 dB		6		
	VULPGA code 10001 7 dB		7		
	VULPGA code 10010 8 dB		8		
	VULPGA code 10011 9 dB		9		
	VULPGA code 10100 10 dB		10		
	VULPGA code 10101 11 dB		11		
	VULPGA code 10110 12 dB		12		

	Others cases		-6		
Power supply rejection from VBAT	0 Hz to 100 kHz		40		dB

Frequency response **4kHz bandwidth**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency response relative to reference gain at 1.015 kHz	≤ 100 Hz			-20	dB
	100 Hz to 200 Hz			-10	
	300 Hz to 400 Hz	-2	0	+1	
	400 Hz to 3300 Hz	-1	0	+1	
	3300 Hz to 3400 Hz	-2	0	+1	
	4000 Hz to 4600 Hz			-17	
	4600 Hz to 6000 Hz			-40	
	≥ 6000 Hz			-45	

Frequency response **8kHz bandwidth (wideband)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency response relative to reference gain at 2.031kHz	≤ 100 Hz			-11	dB
	200 Hz to 300 Hz			-3	
	300 Hz to 400 Hz	-7	0	+1	
	800 Hz to 1000 Hz	-3	0	+1	
	1400 Hz to 6600 Hz	-1	0	+1	
	6600 Hz to 6800 Hz	-2	0	+1	
	8000 Hz to 9200 Hz			-17	
	9200 Hz to 12000 Hz			-40	
	≥ 12000 Hz			-45	

Psophometric TSNR **8KHz bandwidth**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Psophometric TSNR (Harmonic Distortion + SNR)	3 dBm0 (Maximum Digital Code)	**35**	48		dB
2.031kHz Tone (WBA=1)	0 dBm0	**40**	66		
	-10 dBm0	**45**	67		
	-50 dBm0	**20**	26		
Maximum idle channel noise				-72	dBm0
Crosstalk with the downlink path	Downlink path loaded at 33 Ω			-66	dB

Gain characteristics **8KHz bandwidth**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute gain error (1)	At 0 dBm0	-1		1	dB
1.015kHz or 2.031kHz Tone (WBA=1)	At -10 dBm0	-11		-9	
Gain tracking error	3 dBm0	-0.25		0.25	dB
	0 dBm0	-0.25		0.25	
	-10 dBm0 (reference)		0		
	-50 dBm0	-0.50		0.50	

Note: (1) for Carkit output stage, absolute gain error is [-2; 2 dB] at 0 dBm0 and [-12; -8 dB] at –10 dBm0.

Table 29 : Voice Uplink Path Characteristics

Audio Outputs Characteristics

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Minimum resistive load between EARP and EARN: Zload			120		Ω
			33		Ω
Differential Maximum capacitor load between EARP and EARN:				100	pF
Common mode Minimum resistive load at EARP or EARN			200		kΩ
Common mode Maximum capacitor load at EARP or EARN				50	pF
Minimum output resistive load at D+: Zload	CARKIT = 1	60			kΩ
Minimum output resistive load at D-: Zload	CARKIT = 1	60			kΩ
Minimum resistive load at HSOL and HSOR: Zload			32		Ω
Maximum capacitor load at HSOL and HSOR:				100	pF
Maximum capacitor load at HSOVMID				200	pF
Capacitor load at AUVMID			4.7		µF

Table 30 : Loads and External Components Values

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Minimum resistive load between SPKP and SPKN: Zload		6	8		Ω
Common mode Minimum resistive load at SPKP and SPKN (R1) Figure 16			220		kΩ
Filtering common mode capacitor on SPKAN and SPKAP (C1) Figure 16			220		nF
Serial filtering inductance on SPKDN and SPKDP (L1) Figure 16 ±20%		22			µH
Saturation current of the L1 inductance		350			mA
Serie resistance of the L1 inductance				1.3	Ω

Note : A 6 ohms speaker +/- 10% load can be connected on the spkd_p/n output and that does not represent any risk for the amplifier itself, however the electrical characteristics are guaranteed for 8 Ohms load. The Class A/B does not support Hand Free mode alone.

Table 31 : External Components Values for the Class AD Amplifier

Global characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Earphone output swing at EARP-EARN	distortion ≤ 2% and 120 Ω, VSP input level = +3 dBm0, amp gain = -11 dB		0.98		V_{PP}
	distortion ≤ 2% and 33 Ω, VSP input level = -5.34 dBm0, amp gain = -11 dB		0.38		
	distortion ≤ 2% and 120 Ω, I2S input level = +3 dBm0, amp gain = -11 dB		0.93		
	distortion ≤ 2% and 120 Ω, VSP input level = +3 dBm0, amp gain = 1 dB	3.1	3.92		
	distortion ≤ 2% and 33 Ω, VSP input level = -5.34 dBm0, amp gain = 1 dB	1.2	1.5		
	distortion ≤ 2% and 120 Ω, I2S input level = +3 dBm0, amp gain = 1 dB	2.96	3.7		
Earphone amplifier gain	EARG = 1		1		dB
	EARG = 0		-11		dB
Earphone amplifier state in power down			High Z		
Earphone amplifier power supply rejection	1 kHz, 100 mVpp		50		dB
Car kit output swing at D+ and D-	distortion ≤ 2% and 1 kΩ, VSP input level = +3 dBm0, bit VMIDSEL = '0' or '1' (Internal Vmid = 1.35 V or 1.5 V)	1.15	1.4		V_{PP}

Car Kit Output amplifier gain (Left/Right)			-8		dB
Car Kit amplifier state in power down			High Z		
Car kit amplifier power supply rejection	1 kHz, 100 mVpp		50		dB
Headphone output swing at (HSOL/R)	distortion ≤ 2% and 32 Ω, VSP input level = +3 dBm0	1.6	1.96		V_{PP}
	distortion ≤ 2% and 32 Ω, I2S input level = +3 dBm0	1.48	1.85		
Headphone L/R amplifier gain			-5		dB
HSOL/R amplifier state in power down			High Z		
HSOL/R amplifier Power supply rejection	1 kHz, 100 mVpp		50		dB
Hands-free speaker output swing at SPKP-SPKN (differential output), SPKVDD = VBAT	distortion ≤ 1% and 8 Ω, SPKVDD = 4.2 V, Pout = 340 mW, SPKG = 001 (2.5 dB), VSP input level = +3 dBm0,		4.65		V_{PP}
Hands-free speaker output swing at SPKP-SPKN (differential output), SPKVDD = VBAT	distortion ≤ 1% and 8 Ω, SPKVDD = 4.2 V, Pout = 680 mW, SPKG = 000 (8.5 dB), VSP input level = 0 dBm0,		6.6		V_{PP}
Speaker amplifier gain	000		+8.5		dB
	001		+2.5		
	010		+2.5		
	011 (*)		-3.5		
	100 (*)		-22.5		
Speaker amplifier state in power down			High Z		
Speaker amplifier power supply rejection	1 kHz, 100 mVpp		80		dB
DC level at HSOVMID		1.2	1.35	1.5	V
DC level at AUVMID	VMIDSEL = 0		1.35		V
	VMIDSEL = 1		1.5		

Note: (*) The performances of the hands-free speaker are not guaranteed for these gains.

Table 32 : Audio Outputs Characteristics

Voiceband Downlink Path Characteristics

Volume Control Gain

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Default and reference	VOCTL code 010		0		dB
	VOCTL code 110		-6		
	VOCTL code 000		-12		
	VOCTL code 100		-18		
	VOCTL code 011		-24		
Mute	VOCTL code 101, 001, 111			-40	dB

PGA Gain Step

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Default	VDLPGA code 0000 -6 dB		-6		dB
	VDLPGA code 0001 -5 dB		-5		
	VDLPGA code 0010 -4 dB		-4		
	VDLPGA code 0011 -3 dB		-3		
	VDLPGA code 0100 -2 dB		-2		
	VDLPGA code 0101 -1 dB		-1		
Reference	VDLPGA code 0110 0 dB		0		dB
	VDLPGA code 0111 1 dB		1		
	VDLPGA code 1000 2 dB		2		
	VDLPGA code 1001 3 dB		3		

	VDLPGA code 1010	4 dB		4	
	VDLPGA code 1011	5 dB		5	
	VDLPGA code 1100	6 dB		6	
	Other cases			-6	

Sidetone Gain Step

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference	VDLST code 1101	-23 dB		-23		dB
	VDLST code 1100	-20 dB		-20		
	VDLST code 0110	-17 dB		-17		
	VDLST code 0010	-14 dB		-14		
	VDLST code 0111	-11 dB		-11		
	VDLST code 0011	-8 dB		-8		
	VDLST code 0000	-5 dB		-5		
	VDLST code 0100	-2 dB		-2		
	VDLST code 0001	1 dB		1		
	VDLST code 0101	1 dB		1		
	VDLST code 1000	Mute			-66	
	Other cases	Mute			-66	

Frequency response **4kHz bandwidth**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency response relative to reference gain at 1 kHz	≤ 50 Hz			-10	dB
	50 Hz to 160 Hz			-3	
	300 Hz to 400 Hz	-2	0	1	
	400 Hz to 3300 Hz	-1	0	1	
	3300 Hz to 3400 Hz	-2	0	1	
	4000 Hz to 4600 Hz			-17	
	4600 Hz to 6000 Hz			-40	
	≥ 6000 Hz			-45	

Frequency response **8kHz bandwidth (WBA=1)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Frequency response relative to reference gain at 2.031kHz	≤ 100 Hz			-11	dB
	200 Hz to 300 Hz			-3	
	300 Hz to 400 Hz	-7	0	+1	
	800 Hz to 1000 Hz	-3	0	+1	
	1400 Hz to 6600 Hz	-1	0	+1	
	6600 Hz to 6800 Hz	-2	0	+1	
	8000 Hz to 9200 Hz			-17	
	9200 Hz to 12000 Hz			-40	
	≥ 12000 Hz			-45	

Psophometric TSNR & ICN **8kHz bandwidth**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Psophometric TSNR (Harmonic Distortion + SNR)	3 dBm0 (Maximum Digital Code)		35		dB
Measured with psophometric filter	0 dBm0	45	78		
2.031kHz Tone (WBA=1)	-10 dBm0	57	73		
Measured at: EARP-EARN (load = 120 Ω), Carkit, Headset	-30 dBm0	50	55		
	-40 dBm0	40	45		
	-50 dBm0	30	35		
Maximum idle channel noise (EAR, Carkit, Headset) Measured with psophometric filter				-86	dBm0

TSNR (Harmonic Distortion + SNR) Measured with psophometric filter 2.031kHz Tone (WBA=1) Measured at: SPKP-SPKN @2.5dB, Load = 8 Ω, L = 22 uH, 220nF	3 dBm0 (Maximum Digital Code)	35	dB
	0 dBm0	50	
	-10 dBm0	56	
	-20 dBm0	47	
	-30 dBm0	37	
	-40 dBm0	27	
	-50 dBm0	17	
	-60 dBm0	7	
	-70 dBm0	0	
Maximum idle channel noise (Handfree SPK output) Measured with psophometric filter		-80	dBm0
Crosstalk with the uplink path		-66	dB

Gain characteristics **8kHz bandwidth**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute gain error 2.031kHz Tone (WBA=1)	At 0 dBm0	-1	0	1	dB
	At 0 dBm0, HPFBYP=1	0	1	2	
	At -10 dBm0	-11	-10	-9	
Gain tracking error Measured at: EARP-EARN (load = 120 Ω), Carkit, Headset	3 dBm0	-0.3		0.3	dB
	0 dBm0	-0.25		0.25	
	-10 dBm0 (reference)		0		
	-50 dBm0	-0.50		0.50	
Class AD Gain tracking error Measured at: SPKP-SPKN @2.5dB, Load = 8 Ω, L = 22 uH, C = 220nF	3 dBm0	-0.3		0.3	dB
	0 dBm0	-0.25		0.25	
	-10 dBm0 (reference)		0		
	-50 dBm0	-1.50		1.50	

Table 33 : Voice Downlink Path Characteristics

Audio Stereo Path Characteristics

Right/Left Audio Volume Control Gain Step

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Right and Left Gain	AUGA=1, AULGA/AURGA = 00000		+6		dB
Default and Reference	AUGA=0, AULGA/AURGA = 00000		0		dB
Right or Left Gain	AUGA=0, AULGA/AURGA = 00001		-1		dB
	AUGA=0, AULGA/AURGA = 00010		-2		
	AUGA=0, AULGA/AURGA = 00011		-3		
	AUGA=0, AULGA/AURGA = 00100		-4		
	AUGA=0, AULGA/AURGA = 00101		-5		
	AUGA=0, AULGA/AURGA = 00110		-6		
	AUGA=0, AULGA/AURGA = 00111		-7		
	AUGA=0, AULGA/AURGA = 01000		-8		
	AUGA=0, AULGA/AURGA = 01001		-9		
	AUGA=0, AULGA/AURGA = 01010		-10		
	AUGA=0, AULGA/AURGA = 01011		-11		
	…		…		
	AUGA=0, AULGA/AURGA = 11101		-29		
	AUGA=0, AULGA/AURGA = 11110		-30		
Right or Left Mute	AUGA=0, AULGA/AURGA = 11111			-40	dB

Frequency response (relative to reference gain at 1 kHz)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Passband			0.42*Fs †		Hz
Passband gain	In region 0 to 0.42*Fs	-1		1	dB
Stopband			0.65*Fs		Hz
Stopband Attenuation	In region 0.65*Fs to 8*Fs	60	75		dB
Group Delay			12.625/ Fs		µs
-3dB attenuation		0.47*Fs	0.48*Fs	0.49*Fs	Hz

† Fs is the sampling frequency (8/11.025/12/16/22.05/24/32/44.1/48kHz).

Audiometric TSNR

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Audiometric TSNR (Harmonic Distortion + SNR) (1) 1.015kHz Tone Measured at: HSOL/R	3 dBm0, Fs = 44.1kHz, BW: 20Hz-20kHz	35	59		dB
	0 dBm0, Fs = 44.1kHz, BW: 20Hz-20kHz	45	61		
	-10 dBm0	57	62		
	-50 dBm0	25	27		
Maximum idle channel noise (1)				-78	dBm0
Intermodulation Distortion	At 0 dBm0 and 1 kHz		-60		dB
Inband Spurious	At 0 dBm0 and 1 kHz, 300 to 0.4*Fs		-50		dB

Note: All performance measurements done with an Audiometric filter (A-weighted filter). Failure to use such a filter results in higher THD+N and lower SNR and dynamic range readings than shown in electrical characteristics. The Audiometric filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Gain characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute gain error	At 0 dBm0 and 1 kHz	-1.5	-0.5	0.5	dB
	At -10 dBm0 and 1 kHz	-11.5	-9.5	-8.5	
L/R Gain Mismatch	At 0 dBm0 and 1 kHz, gain setting @ 0 dB	-1	0.2	1	dB
Gain tracking error	3 dBm0	-0.25		0.25	dB
	0 dBm0	-0.25		0.25	
	-10 dBm0 (reference)		0		
	-50 dBm0	-0.50		0.50	

Table 34 : Audio Stereo Path Characteristics

9 USB 2.0 FULL SPEED TRANSCEIVER

9.1 FUNCTIONAL DESCRIPTION

T3031 includes a Universal Serial Bus (USB) transceiver with a carkit detection, able to support USB 12 Mb/s Full-Speed (FS) and USB 1.5 Mb/s Low-Speed (LS) . When a USB cable is plugged into the Mini-B receptacle, the transceiver detects the cable's presence on VBUS (>1.8V) and ID (≠ float) pins, even if the phone is switched off. The transceiver can charge the phone's battery when connected to a power device. The transceiver is fully operational only in phone's Active mode, and when the automatic precharge is disabled. It is impossible to use the transceiver in normal operations when the precharge is activated. The precharge must be deactivated first.

T3031 device's car kit is developed based on CEA-936-A rev.39 – Nov. 24th 2004 specification . T3031 device doesn't not support other updated versions of this specification .
Compared to the CEA-936-A rev.39 – Nov. 24th 2004 specification, the carkit implementation in the T3031 device does not support

- a full implemented hardware Phone State Machine
- the relative interrupts and registers for the proper behavior of the Phone State machine
- the Data-During-Audio signaling mode
- the analog carkit comparator (CR_INT interrupt).

- USB transceiver full compliant (modes and registers)
- 3-pins or 4-pins bidirectional port with the USB controller (DBB chip) (DAT_SE0 / VP_VM),
- Can transmit and receive USB data at LS / FS rates
- Supports data line ($D^{+/-}$) and V_{BUS} pulsing session request (SRP)
- Supports UART signaling (From 9.6 kbaud up to 115.2 kbaud)
- Supports AUDIO (MONO / STEREO) signaling
- Triton Lite's transceiver does not support USB High Speed (HS) mode signaling
- USB, charger and carkit precharges are impossible during normal transceiver operations

The following diagram presents the relevant modules embedded in Triton Lite, in order to operate the USB transceiver. The I^2C bus is used to access the digital section of the USB.

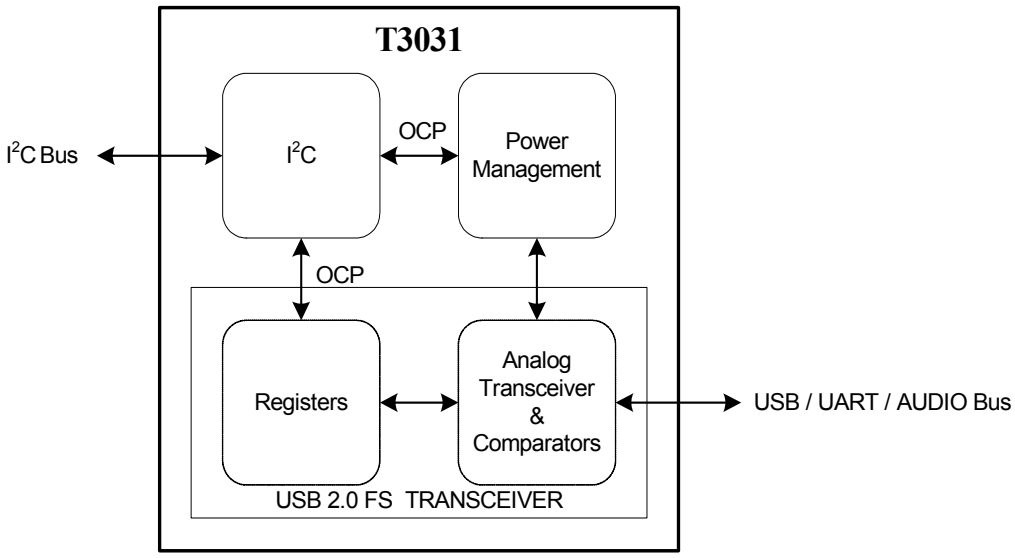


Figure 25 : USB 2.0 FS Transceiver

USB CONTROLLER INTERFACE

To transmit and receive USB information, it is needed 3 or 4 pins towards the USB controller embedded in the DBB chip. In USB mode, the transceiver is allowed to transmit data on the differential bus $D^{+/-}$ when the output enable pin OE_INTN is cleared to 0. Therefore, DAT_VP and SE0_VM are the inputs of the differential driver and the RCV pin is irrelevant (when SUSPEND is cleared to 0, the RCV line is always giving the status of the differential data line DP/DM). When OE_INTN is set to 1, the USB controller is receiving in single-ended or differential data encoding on DAT_VP and SE0_VM pins, and RCV is the output of the differential input receiver.

Note: In a 3-pins port configuration, the RCV pin is not used. (even if it works exactly the same as the 4 pins configuration). The output of the differential receiver is multiplexed on DAT_VP.

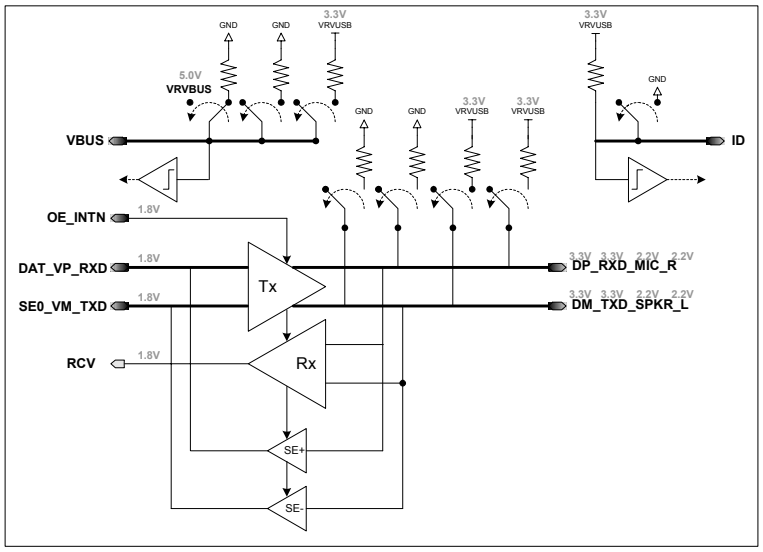


Figure 26 : USB Transceiver Block Diagram

NAME	BALL	TYPE	RESET	DESCRIPTION
T3031 – USB PORT INTERFACE				
VBUS	A6	Analog I/O	USB-A Off High-Z USB-A On PD	5v-tolerant power Supply V_{BUS} line; The transceiver drives the line if the regulator is on and the VBUS_DRV bit is set; The V_{BUS} line may also be pulled-up to VRUSB or pulled-down when VBUS_CHRG or VBUS_DISCHRG register bits are asserted; Place an external decoupling capacitor (C_{OTG_VBUS}) close to this pin.
DP_RXD_MIC_R	A5	Analog I/O	USB-A Off High-Z USB-A On PD	5v-tolerant data plus pin in USB modes; Receive function in UART; Microphone or right speaker in AUDIO; The data line may be pulled-up or pulled-down with the bits DP_PULLUP, DP_PULLDOWN; Place an external capacitor C_{INUB} (22pF) closed to this pin. (Optional)
DM_TXD_SPKR_L	A3	Analog I/O	USB-A Off High-Z USB-A On PD	5v-tolerant data minus pin in USB modes; Transmit function in UART; Monaural speaker or left speaker in AUDIO; The data line may be pulled-up or pulled-down with the bits DM_PULLUP, DM_PULLDOWN; As D^+, place the C_{INUB} capacitor closed to this pin. (Optional)
ID	D4	Analog I/O	USB-A Off PU (on VRRTC) USB-A On PU (on VRUSB)	5v-tolerant ID line, it defines the type of device connected to the phone's USB port; And also the default state (host / device) at the cable connection; With the 5-wire interface, ID line is used to signal interrupts; The transceiver senses the voltage of this pin to determine if the pin is either floating, grounded or resistively connected to ground (102kΩ, 200kΩ, 440kΩ); The transceiver can short this pin to ground by asserting the ID_GND_DRV bit, in order to generate an interrupt.
GND	B7/C7	Power	Gnd	Ground line of the cable connected to the T3031 digital ground.
DBB CHIP (USB CONTROLLER) – T3031 INTERFACE				
OE_INTN	E4	Digital I/O	High-Z / PD	When this pin is configured as an input, It controls the direction of DAT_VP, SE0_VM, DP and DM; When it is set as an output, it is an interrupt active low; Its function is directly related to the status of the SUSPEND and OE_INT_EN register bits; When it is not configured as an interrupt line, USB interrupts are transmitted through the general T3031 P1_INT2 pin; Bidirectional; three-state output.
DAT_VP_RXD	C3	Digital I/O	OE_INTN=0 High-Z / PD OE_INTN=1 0	DAT function in DAT_SE0 mode; VP in VP_VM mode; RXD function in UART mode; USB and UART functions depend of the SUSPEND, UART_EN, DAT_SE0 register bits and the input pin OE_INTN; Bidirectional; three-state output.
SE0_VM_TXD	C4	Digital I/O	OE_INTN=0 High-Z / PD OE_INTN=1 0	SE0 function in DAT_SE0 mode; VM in VP_VM mode; TXD function in UART; USB and UART functions depend of the SUSPEND, UART_EN, DAT_SE0 register bits and the input pin OE_INTN; Bidirectional; three-state output.
RCV	A2	Digital I/O	0	Differential receiver output for USB LS / FS; It reflects the differential value of DP and DM, in any mode (DAT_SE0 / VP_VM) and in any direction (transmission and reception).

Table 35 : I/Os of the USB

9.2 MODES OF THE TRANSCEIVER

9.2.1 Power Modes

Active Mode
In Active mode, the USB transceiver is fully operational: both differential driver and receiver are turned on.

Suspend Mode
In Suspend mode, only the USB differential driver and receiver are turned off. The digital section and the analog comparators are still working, as well as the drivers for the UART and AUDIO. VRUSB needs to be kept powered on, principally for the UART and AUDIO functions, the ID comparators and the pull-ups / pull-downs.

Power Down Mode
In the Power Down mode, the overall transceiver in turned off, except the V_{BUS} comparators for SRP, which are supplied on VRABB and the wake-up comparators supplied on VRRTC and VBUS. So, even if the phone is in Off mode, once a USB device is attached, an interrupt signal generated on VBUS or ID lines releases the ONnOFF signal.

Precharge Mode
By default, the transceiver is used by the BCI in order to detect a powered device on the USB port. The precharge via USB can be requested at any moment. The software has to disable the precharge if the transceiver is needed for normal operations.

9.2.2 Data Signaling Modes

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USB Modes
Two modes exist for the USB transceiver:

- DAT_SE0 for single-ended transactions with the USB controller (DBB chip) (3-pins),
- VP_VM for differential communications with the USB controller (4-pins).

When the SUSPEND bit is cleared, the USB mode is activated. If another data signaling mode was already selected (UART or AUDIO), setting SUSPEND to 0 will turn off the UART and AUDIO drivers for the USB signaling.

Next are detailed the truth tables of the I/Os, for both modes, during the transmissions and receptions:

USB MODE (SUSPEND=0)	INPUTS		OUTPUTS		
	DAT_VP	SE0_VM	D^+	D^-	RCV
DAT_SE0	0	0	0	1	0 (RCV)
DAT_SE0	1	0	1	0	**1 (RCV)**
DAT_SE0	0	1	0	0	Latch (RCV)
DAT_SE0	1	1	0	0	Latch (RCV)
VP_VM	0	0	0	0	Latch (RCV)
VP_VM	1	0	1	0	**1 (RCV)**
VP_VM	0	1	0	1	**0 (RCV)**
VP_VM	1	1	1	1	Latch (RCV)

Table 36 : USB Transmission Signal Encoding

USB MODE	SUSPEND	INPUTS		OUTPUTS		
		D^+	D^-	DAT_VP	SE0_VM	RCV
DAT_SE0	0	0	0	Latch (RCV)	1 ($SE^{+/-}$)	Latch (RCV)
DAT_SE0	0	1	0	**1 (RCV)**	0 ($SE^{+/-}$)	**1 (RCV)**
DAT_SE0	0	0	1	**0 (RCV)**	0 ($SE^{+/-}$)	**0 (RCV)**
DAT_SE0	0	1	1	Latch (RCV)	0 ($SE^{+/-}$)	Latch (RCV)
DAT_SE0	1	0	0	0 (SE^{+})	1 ($SE^{+/-}$)	0
DAT_SE0	1	1	0	1 (SE^{+})	0 ($SE^{+/-}$)	0
DAT_SE0	1	0	1	0 (SE^{+})	0 ($SE^{+/-}$)	0
DAT_SE0	1	1	1	1 (SE^{+})	0 ($SE^{+/-}$)	0
VP_VM	0	0	0	0 (SE^{+})	0 (SE^{-})	Latch (RCV)
VP_VM	0	1	0	1 (SE^{+})	0 (SE^{-})	**1 (RCV)**
VP_VM	0	0	1	0 (SE^{+})	1 (SE^{-})	**0 (RCV)**
VP_VM	0	1	1	1 (SE^{+})	1 (SE^{-})	Latch (RCV)
VP_VM	1	0	0	0 (SE^{+})	0 (SE^{-})	0
VP_VM	1	1	0	1 (SE^{+})	0 (SE^{-})	0
VP_VM	1	0	1	0 (SE^{+})	1 (SE^{-})	0
VP_VM	1	1	1	1 (SE^{+})	1 (SE^{-})	0

Table 37 : USB Reception Signal Encoding

UART Mode

When the UART_EN bit is enabled, UART transactions can be achieved through the transceiver. During this mode, the transceiver can be considered as simple levels translators. When UART_EN is set to 1, it automatically switched off the other USB and AUDIO drivers.

UART DATA PATH	FROM	TO
TRANSMISSION	SE0_VM_**TXD**	DM_**TXD**_SPKR_L
RECEPTION	DP_**RXD**_MIC_R	DAT_VP_**RXD**

Table 38 : UART Pins Configuration

AUDIO Modes

It is possible to select between the MONO and STEREO signaling modes. When enabling the AUDIO drivers, the USB and UART drivers are turned off. Several AUDIO register access have to be performed in order to configure properly the uplink and downlink audio paths.

AUDIO SIGNALING	MONO	STEREO
TRANSMISSION	DM_TXD_**SPKR**_L	DP_RXD_MIC_**R** DM_TXD_SPKR_**L**
RECEPTION	DP_RXD_**MIC**_R	-

Table 39 : AUDIO Pins Configuration

9.3 ANALOG – DIGITAL INTERFACE

There are two kinds of signals at the analog - digital interface: Those coming from the digital, which are the transceiver control signals, and those generated by the analog module after electrical detections on the USB port.

9.3.1 Control Signals

This section describes the signals coming from the digital module toward the USB transceiver , AUDIO drivers and the USB regulators. These signals may be directly controlled by software via the implemented registers

USBA_EN
When USBA_EN = 1, it enables the overall analog section of the transceiver and the digital pads towards the USB controller. USBA_EN has no effect on the automatic precharge the comparators dedicated for V_{BUS} SRP and the wake-up interrupts on both V_{BUS} and ID lines. USBAS enables (USBAR disables) the USB analog transceiver. Also, there is a dedicated enable for the digital section of the USB. USBDS enables (USBDR disables) the USB digital transceiver.

SPEED
SPEED configures the USB driver for LS or FS operations.

SUSPEND
SUSPEND controls the power consumption inside the transceiver in USB mode. The differential driver and receiver are powered-down and their outputs are tri-stated when SUSPEND = 1. Extra logic has been added in order to avoid conflicts on $D^{+/-}$ between USB, UART and AUDIO modes.

DAT_SE0
During USB transactions, DAT_SE0 selects single-ended or differential signaling mode at the T3031 - DBB chip interface. Single-ended mode is selected when DAT_SE0 = 1, otherwise VP_VM differential transfer is used.

OE_INT_EN
When OE_INT_EN bit is asserted the OE_INTN pin becomes an output and is driven low when a USB interrupt occurs. Also, in UART and AUDIO modes, when this bit is set, an interrupt can be sent. When OE_INT_EN =1 and SUSPEND = 0, USB signaling is still possible but the interrupts are generated through the T3031 P1_INT2 pin.

UART_EN
When UART_EN = 1, this signal allows the transceiver to work in UART signaling mode. In that case, DM driver and VP receiver are used as transmitter TXD and receiver RXD. During this mode, the drivers DP, RCV and VM are turned-off. Asking for USB or AUDIO signaling will set UART_EN to 0.

DP_PULLUP
DP_PULLUP controls the pull-up R_{PU} resistor to VRUSB power supply on the DP line. The pull-up is applied when DP_PULLUP = 1. Setting DP_PULLDOWN = 1 forces DP_PULLUP to 0.

DM_PULLUP
DM_PULLUP controls the pull-up R_{PU} resistor to VRUSB power supply on the DM line. The pull-up is applied when DM_PULLUP = 1. Setting DM_PULLDOWN = 1 forces DM_PULLUP to 0.

DP_PULLDOWN
DP_PULLDOWN controls the pull-down R_{PD} resistor to ground on the DP line. The pull-down is applied when DP_PULLDOWN = 1. Setting DP_PULLUP = 1 forces DP_PULLDOWN to 0.

DM_PULLDOWN
DM_PULLDOWN controls the pull-down R_{PD} resistor to ground on the DM signal. The pull-down is applied when DM_PULLDOWN = 1. Setting DP_PULLUP = 1 or DM_PULLUP = 1 forces DM_PULLDOWN to 0.

ID_GND_DRV
This signal forces the ID pin to ground. Named as ID_GND, this signal has been renamed to avoid confusion with the USB interrupt ID_GND.

VBUS_DISCHRG
VBUS_DISCHRG enables a pull-down resistor on the V_{BUS} line to discharge the bus. This pull-down is sized such that the maximum discharge current is limited to $I_{B\_DSCHG\_IN}$. This translates to a resistor of a size $R_{B\_SRP\_DWN}$. The bus is discharged when VBUS_DISCHRG = 1. Setting VBUS_DISCHRG clears VBUS_DRV and VBUS_CHRG.

VBUS_CHRG
When acting as a B-device, the transceiver can request a session using the V_{BUS} pulsing method of the SRP. V_{BUS} is pulsed by connecting a resistance of $R_{B\_SRP\_UP}$ (VBUS_CHRG = 1) between V_{BUS} and the VRUSB regulator. Setting VBUS_CHRG clears VBUS_DRV and VBUS_DISCHRG.

VBUS_VRUSB
This signal selects the input voltage of the VRUSB regulator. When VBUS_VRUSB = 1, the VBUS line is the input of the regulator. This bit must be set to 1.

SPKR_L_BIAS_EN
This signal allows the VOICE to enable the speaker driver on DM line.

SPKR_R_BIAS_EN
This signal allows the VOICE to enable the speaker driver on DP line.

MIC_BIAS_EN
This signal allows the VOICE to enable the microphone receiver on DP line.

9.3.2 Detection Signals

This section describes the signals from the analog transceiver towards the digital module.

VA_VBUS_VLD
A comparator is provided to allow an A-device to determine whether or not the voltage on V_{BUS} is at a valid level for correct operations. The minimum threshold for this comparator is given by $V_{A\_VBUS\_VLD}$. Any voltage below $V_{A\_VBUS\_VLD}$ min is detected as a low-voltage condition. This comparator output should be ignored during power-up. VA_VBUS_VLD = 1 when the $V_{A\_VBUS\_VLD}$ threshold (4.4V – 4.55V – 4.75V) is exceeded. The four VBUS comparators outputs are detecting a specific voltage threshold. In order to limit the number of interrupts generated, a cable debounce time can be set.

VA_SESS_VLD
A comparator is provided to allow an A device to determine when V_{BUS} is high enough to start a session. VA_SESS_VLD = 1 when the $V_{A\_SESS\_VLD}$ threshold (0.8V – 1.1V – 1.4V) is exceeded. When VBUS reached 2.1V, the interrupt is detected as a VB_SESS_VLD interrupt.

DP_HI
DP_HI is set to 1 when the single-ended DP receiver detects DP above V_{IH} (2.0V). The comparator's threshold is defined in [0.8V – 2.0V] range.

ID_GND
A comparator is used to determine when the ID pin has been shorted to ground through a resistance of less than $R_{A\_PLUG\_ID}$ (<10Ω) when the ID pin is biased to V_{ID_HI} (3.3V) via $R_{XC\_ID\_DET\_HI}$ (100kΩ). The ID_GND signal is set to 1 when this is true.

DM_HI
DM_HI is set to 1 when the single-ended DM receiver detects DM above V_{IH} (2.0V). The comparator's threshold is defined in [0.8V – 2.0V] range.

ID_FLOAT
A comparator is used to determine when the ID pin has been terminated to ground through a resistance of more than 560kΩ, when the ID pin is biased to V_{ID_HI} (3.3V) via $R_{XC\_ID\_DET\_HI}$ (100kΩ). The ID_FLOAT signal is set to 1 when this condition is met.

CR_INT
When D^+ pin is below the $V_{PH\_DP\_LO}$ [0.4V – 0.5V – 0.6V] carkit interrupt threshold, the CR_INT bit is set to 1. The carkit comparator has to be enabled first.

VB_SESS_END
VB_SESS_END signal is set to 1 if the V_{BUS} line is lower than the $V_{B\_SESS\_END}$ threshold (0.2V – 0.5V – 0.8V).

VB_SESS_VLD
VB_SESS_VLD signal is set to 1 if the V_{BUS} line is higher than the $V_{B\_SESS\_VLD}$ threshold (2.1V – 2.4V – 2.7V). Once VBUS reached 4.4V, the interrupt is detected as a VA_VBUS_VLD interrupt.

STRESS
STRESS is set to 1 when the VRUSB regulator voltage is higher than 3.6V.

ID_RES_100K

Two comparators are used for detecting the accessory / charger resistors. Due to important mismatch between the internal $R_{XC\_ID\_DET\_HI}$ (100kΩ) and the external resistor inside the peripheral device, the detection range has been enlarged from 50kΩ to 150kΩ. The first comparator detects resistors higher than 50kΩ. The second comparator detects resistors lower than 150kΩ. ID_RES_100K signal is set to 1 when a resistor of 102kΩ (1%) is detected on ID pin.

ID_RES_200K

As detailed above for the 102kΩ resistor, the detection range of the 200kΩ resistor has been implemented between 150kΩ and 320kΩ with two comparators. ID_RES_200K signal is set to 1 when a resistor of 200kΩ (1%) is detected on ID pin.

ID_RES_440K

The detection range of the 440kΩ resistor has been defined with two comparators, between 320kΩ and 560kΩ. ID_RES_440K signal is set to 1 when a resistor of 440kΩ (1%) is detected on ID pin.

9.4 APPLICATION BOARD

Some external components need to be placed between the T3031 device and the USB receptacle. The C_{OTG_VBUS} capacitor is mandatory. The C_{INUB} capacitors are optional.

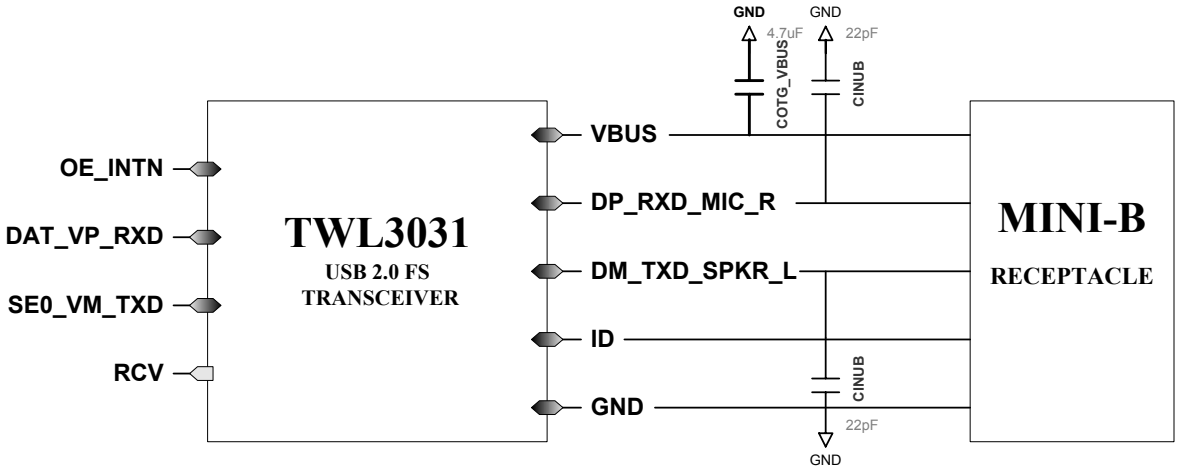


Figure 27 : USB Application Board

The T3031 device must be closed to the Mini-B receptacle. the maximum delay authorized on the data lines is 3ns. DP & DM lines are differential.

9.5 LIST OF REFERENCES

For more details please refer to the official documents, directly available on the www.usb.org and www.ce.org websites.

"*Universal Serial Bus Specification, Rev. 2.0*", April 27th, 2000.
"*USB ECN: Pull-Up / Pull-Down Resistors*", May 7th, 2002.
"*On-The-Go Supplement to the USB 2.0 Specification, Rev. 1.2RC3*", May 20th, 2004.
"*CEA-2011 R0V1 - OTG Transceiver Interface Specification*", July 2nd, 2003.
"*OTG Carkit Transceiver Specification, Rev. 0.64*", October 1st, 2004.
"*CEA-936 rAv39 - Mini-USB Analog Carkit Interface*", November 24th, 2004.
"*USB Compliance Checklist: Peripheral Silicon, Rev. 1.8*", December 18th, 2001.
"*USB Compliance Checklist: On-The-Go Devices, Rev. 1.0*", August 2003.
"*USB Compliance Test Procedures, Rev. 1.3*", February 2004.

Table 40 : Official Related Documents

9.6 REGISTERS

9.6.1 VENDOR_ID_LSB

Register	VENDOR_ID_LSB							
Page	0/2	Address	Dec # 0		Hex 0x00			
Bit	7	6	5	4	3	2	1	0
Name	VENDOR_ID_7	VENDOR_ID_6	VENDOR_ID_5	VENDOR_ID_4	VENDOR_ID_3	VENDOR_ID_2	VENDOR_ID_1	VENDOR_ID_0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	1	0	1	0	0	0	1

Register bits description

VENDOR_ID [7:0]	Texas Instruments Vendor ID (8 LSBs) – Default value: 51 HEX

9.6.2 VENDOR_ID_MSB

Register	VENDOR_ID_MSB							
Page	0/2	Address	Dec # 1		Hex 0x01			
Bit	7	6	5	4	3	2	1	0
Name	VENDOR_ID_15	VENDOR_ID_14	VENDOR_ID_13	VENDOR_ID_12	VENDOR_ID_11	VENDOR_ID_10	VENDOR_ID_9	VENDOR_ID_8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	1	0	0

Register bits description

VENDOR_ID [15:8]	Texas Instruments Vendor ID (8 MSBs) – Default value: 04 HEX

9.6.3 PRODUCT_ID_LSB

Register	PRODUCT_ID_LSB							
Page	0/2	Address	Dec # 2		Hex 0x02			
Bit	7	6	5	4	3	2	1	0
Name	PRODUCT_ID_7	PRODUCT_ID_6	PRODUCT_ID_5	PRODUCT_ID_4	PRODUCT_ID_3	PRODUCT_ID_2	PRODUCT_ID_1	PRODUCT_ID_0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	1

Register bits description

PRODUCT_ID [7:0]	T3031 product ID (8 LSBs) – Default value: 01 HEX

9.6.4 PRODUCT_ID_MSB

Register	PRODUCT_ID_MSB							
Page	0/2	Address	Dec # 3		Hex 0x03			
Bit	7	6	5	4	3	2	1	0
Name	PRODUCT_ID_15	PRODUCT_ID_14	PRODUCT_ID_13	PRODUCT_ID_12	PRODUCT_ID_11	PRODUCT_ID_10	PRODUCT_ID_9	PRODUCT_ID_8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	1	1	0	0	0	0	0	0

Register bits description

PRODUCT_ID [15:8]	T3031 product ID (8 MSBs) – Default value: C0 HEX

9.6.5 CTRL_1_SET

Register	CTRL_1_SET							
Page	0/2	Address	Dec # 4		Hex 0x04			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	UART_EN	OE_INT_EN	RSVRD	RSVRD	DAT_SE0	SUSPEND	SPEED
Read/Write	R	R/S/C	R/S/C	R	R	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	1	1	1

Register bits description

RSVRD (bit 7)	Reserved bit
UART_EN	0: Suspend / USB / AUDIO 1: UART
OE_INT_EN	0: USB Interrupts on the P1_INT2 pin 1: Interrupts on the OE_INTN pin (USB interrupts on the P1_INT2 pin)
RSVRD (bit 4 to bit 3)	Reserved bits
DAT_SE0	0: VP/VM 1: DAT/SE0
SUSPEND	0: Active 1: Suspend
SPEED	0: LS 1: FS

9.6.6 CTRL_1_CLR

Register	CTRL_1_CLR							
Page	0/2	Address	Dec # 5		Hex 0x05			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	UART_EN	OE_INT_EN	RSVRD	RSVRD	DAT_SE0	SUSPEND	SPEED
Read/Write	R	R/S/C	R/S/C	R	R	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	1	1	1

Register bits description

RSVRD (bit 7)	Reserved bit
UART_EN	0: Suspend / USB / AUDIO 1: UART
OE_INT_EN	0: USB Interrupts on the P1_INT2 pin 1: Interrupts on the OE_INTN pin (USB interrupts on the P1_INT2 pin)
RSVRD (bit 4 to bit 3)	Reserved bits
DAT_SE0	0: VP/VM 1: DAT/SE0
SUSPEND	0: Active 1: Suspend
SPEED	0: LS 1: FS

9.6.7 CTRL_2_SET

Register	CTRL_2_SET							
Page	0/2	Address	Dec # 6		Hex 0x06			
Bit	7	6	5	4	3	2	1	0
Name	VBUS_CHRG	VBUS_DISCHRG	RSVRD	ID_GND_DRV	DM_PULLDOWN	DP_PULLDOWN	DM_PULLUP	DP_PULLUP
Read/Write	R/S/C	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	1	1	0	0

Register bits description

VBUS_CHRG	0: normal operations 1: VBUS charged
VBUS_DISCHRG	0: normal operations 1: VBUS discharged
RSVRD (bit 5)	Reserved bit
ID_GND_DRV	0: ID pulled-up 1: ID grounded
DM_PULLDOWN	0: not asserted 1: asserted
DP_PULLDOWN	0: not asserted 1: asserted
DM_PULLUP	0: not asserted 1: asserted
DP_PULLUP	0: not asserted 1: asserted

9.6.8 CTRL_2_CLR

Register	CTRL_2_CLR							
Page	0/2	Address	Dec # 7		Hex 0x07			
Bit	7	6	5	4	3	2	1	0
Name	VBUS_CHRG	VBUS_DISCHRG	RSVRD	ID_GND_DRV	DM_PULLDOWN	DP_PULLDOWN	DM_PULLUP	DP_PULLUP
Read/Write	R/S/C	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	1	1	0	0

Register bits description

VBUS_CHRG	0: normal operations 1: VBUS charged
VBUS_DISCHRG	0: normal operations 1: VBUS discharged
RSVRD (bit 5)	Reserved bit
ID_GND_DRV	0: ID pulled-up 1: ID grounded
DM_PULLDOWN	0: not asserted 1: asserted
DP_PULLDOWN	0: not asserted 1: asserted
DM_PULLUP	0: not asserted 1: asserted
DP_PULLUP	0: not asserted 1: asserted

9.6.9 INT_SRC

Register	INT_SRC	Status of the signals that can generate an interrupt							
Page	0/2	Address	Dec # 8		Hex 0x08				
Bit	7	6	5	4	3	2	1	0
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)
VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.10 INT_LATCH_SET

Register	INT_LATCH_SET	This register indicates which sources have generated an interrupt							
Page	0/2	Address	Dec # 10		Hex 0x0A				
Bit	7	6	5	4	3	2	1	0
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD
Read/Write	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)
VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.11 INT_LATCH_CLR

Register	INT_LATCH_CLR	This register indicates which sources have generated an interrupt							
Page	0/2	Address	Dec # 11		Hex 0x0B				
Bit	7	6	5	4	3	2	1	0
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD
Read/Write	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)
VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.12 INT_EN_LO_SET

Register	INT_EN_LO_SET	This register enables interrupts on transitions from high to low						
Page	0/2	Address	Dec # 12	Hex 0x0C				
Bit	7	6	5	4	3	2	1	0
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD
Read/Write	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)
VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.13 INT_EN_LO_CLR

Register	INT_EN_LO_CLR	This register enables interrupts on transitions from high to low						
Page	0/2	Address	Dec # 13	Hex 0x0D				
Bit	7	6	5	4	3	2	1	0
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD
Read/Write	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)

VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.14 INT_EN_HI_SET

Register	INT_EN_HI_SET	This register enables interrupts on transitions from low to high							
Page	0/2	Address	Dec # 14		Hex 0x0E				
Bit	7	6	5	4	3	2	1	0	
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD	
Read/Write	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)
VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.15 INT_EN_HI_CLR

Register	INT_EN_HI_CLR	This register enables interrupts on transitions from low to high							
Page	0/2	Address	Dec # 15		Hex 0x0F				
Bit	7	6	5	4	3	2	1	0	
Name	CR_INT	RSVRD	ID_FLOAT	DM_HI	ID_GND	DP_HI	VA_SESS_VLD	VA_VBUS_VLD	
Read/Write	R/S/C	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

CR_INT	Carkit pulses of 200 ns to 500 ns are not detected (32 kHz clock). Only low levels of DP line < 0.5 V for at least 1 clock period are detected.
RSVRD (bit 6)	Reserved bit
ID_FLOAT	ID line is floating
DM_HI	DM line is high
ID_GND	ID line is grounded
DP_HI	DP line is high
VA_SESS_VLD	VBUS higher than VA_SESS_VLD (enable high), lower than VA_SESS_VLD (enable low)
VA_VBUS_VLD	VBUS higher than VA_VBUS_VLD (enable high), lower than VA_VBUS_VLD (enable low)

9.6.16 USB_POWER_SET

Register	USB_POWER_SET	USB power configuration register							
Page	0/2	Address	Dec # 16		Hex 0x10				
Bit	7	6	5	4	3	2	1	0	
Name	VBUS_VRUSB	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	
Read/Write	R/S/C	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

VBUS_VRUSB	1: VBUS input of VRUSB, VBUS_VRUSB needs to be set to 1 for powering up the VRUSB regulator
RSVRD (bit 6 – bit 0)	Reserved bits

9.6.17 USB_POWER_CLR

Register	USB_POWER_CLR	USB power configuration register						
Page	0/2	Address	Dec # 17	Hex 0x11				
Bit	7	6	5	4	3	2	1	0
Name	VBUS_VRUSB	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD
Read/Write	R/S/C	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

VBUS_VRUSB	1: VBUS input of VRUSB, VBUS_VRUSB needs to be set to 1 for powering up the VRUSB regulator
RSVRD (bit 6 – bit 0)	Reserved bits

9.6.18 CTRL_3_SET

Register	CTRL_3_SET							
Page	0/2	Address	Dec # 26	Hex 0x1A				
Bit	7	6	5	4	3	2	1	0
Name	MIC_EN	MIC_BIAS_EN	SPKR_RIGHT_EN	SPKR_LEFT_EN	SPKR_R_BIAS_EN	SPKR_L_BIAS_EN	RSVRD	RSVRD
Read/Write	R	R/S/C	R	R	R/S/C	R/S/C	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

MIC_EN	Not used
MIC_BIAS_EN	0: Input disabled 1: Input enabled
SPKR_RIGHT_EN	Not used
SPKR_LEFT_EN	Not used
SPKR_R_BIAS_EN	0: output disabled 1: output enabled
SPKR_L_BIAS_EN	0: output disabled 1: output enabled
RSVRD (bit 1 – bit 0)	Reserved bits

9.6.19 CTRL_3_CLR

Register	CTRL_3_CLR							
Page	0/2	Address	Dec # 27	Hex 0x1B				
Bit	7	6	5	4	3	2	1	0
Name	MIC_EN	MIC_BIAS_EN	SPKR_RIGHT_EN	SPKR_LEFT_EN	SPKR_R_BIAS_EN	SPKR_L_BIAS_EN	RSVRD	RSVRD
Read/Write	R	R/S/C	R	R	R/S/C	R/S/C	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

MIC_EN	Not used
MIC_BIAS_EN	0: Input disabled 1: Input enabled
SPKR_RIGHT_EN	Not used
SPKR_LEFT_EN	Not used
SPKR_R_BIAS_EN	0: output disabled 1: output enabled
SPKR_L_BIAS_EN	0: output disabled 1: output enabled
RSVRD (bit 1 – bit 0)	Reserved bits

9.6.20 INT_SRC_2

Register	INT_SRC_2	This register indicates the current state of the signals that can generate an interrupt							
Page	2	Address	Dec # 160		Hex 0xA0				
Bit	7	6	5	4	3	2	1	0	
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	Not used
ID_RES_200K	Not used
ID_RES_100K	Not used
STRESS	Not used
VB_SESS_VLD	Not used
VB_SESS_END	Not used

9.6.21 INT_LATCH_2_SET

Register	INT_LATCH_2_SET	This register indicates which source has generated an interrupt							
Page	2	Address	Dec # 161		Hex 0xA1				
Bit	7	6	5	4	3	2	1	0	
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END	
Read/Write	R	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	440-kΩ resistor connected to ID line
ID_RES_200K	200-kΩ resistor connected to ID line
ID_RES_100K	100-kΩ resistor connected to ID line
STRESS	Stress condition detected
VB_SESS_VLD	VBUS higher than VB_SESS_VLD (enable high), lower than VB_SESS_VLD (enable low)
VB_SESS_END	VBUS higher than VB_SESS_END (enable high), lower than VB_SESS_END (enable low)

9.6.22 INT_LATCH_2_CLR

Register	INT_LATCH_2_CLR	This register indicates which source has generated an interrupt						
Page	2	Address	Dec # 162	Hex 0xA2				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END
Read/Write	R	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	440-kΩ resistor connected to ID line
ID_RES_200K	200-kΩ resistor connected to ID line
ID_RES_100K	100-kΩ resistor connected to ID line
STRESS	Stress condition detected
VB_SESS_VLD	VBUS higher than VB_SESS_VLD (enable high), lower than VB_SESS_VLD (enable low)
VB_SESS_END	VBUS higher than VB_SESS_END (enable high), lower than VB_SESS_END (enable low)

9.6.23 INT_EN_LO_2_SET

Register	INT_EN_LO_2_SET	This register enables interrupts on transitions from high to low						
Page	2	Address	Dec # 163	Hex 0xA3				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END
Read/Write	R	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	440-kΩ resistor connected to ID line
ID_RES_200K	200-kΩ resistor connected to ID line
ID_RES_100K	100-kΩ resistor connected to ID line
STRESS	Stress condition detected
VB_SESS_VLD	VBUS higher than VB_SESS_VLD (enable high), lower than VB_SESS_VLD (enable low)
VB_SESS_END	VBUS higher than VB_SESS_END (enable high), lower than VB_SESS_END (enable low)

9.6.24 INT_EN_LO_2_CLR

Register	INT_EN_LO_2_CLR	This register enables interrupts on transitions from high to low						
Page	2	Address	Dec # 164	Hex 0xA4				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END
Read/Write	R	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	440-kΩ resistor connected to ID line
ID_RES_200K	200-kΩ resistor connected to ID line
ID_RES_100K	100-kΩ resistor connected to ID line

STRESS	Stress condition detected
VB_SESS_VLD	VBUS higher than VB_SESS_VLD (enable high), lower than VB_SESS_VLD (enable low)
VB_SESS_END	VBUS higher than VB_SESS_END (enable high), lower than VB_SESS_END (enable low)

9.6.25 INT_EN_HI_2_SET

Register	INT_EN_HI_2_SET	This register enables interrupts on transitions from low to high						
Page	2	Address	Dec # 165	Hex 0xA5				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END
Read/Write	R	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	440-kΩ resistor connected to ID line
ID_RES_200K	200-kΩ resistor connected to ID line
ID_RES_100K	100-kΩ resistor connected to ID line
STRESS	Stress condition detected
VB_SESS_VLD	VBUS higher than VB_SESS_VLD (enable high), lower than VB_SESS_VLD (enable low)
VB_SESS_END	VBUS higher than VB_SESS_END (enable high), lower than VB_SESS_END (enable low)

9.6.26 INT_EN_HI_2_CLR

Register	INT_EN_HI_2_CLR	This register enables interrupts on transitions from low to high						
Page	2	Address	Dec # 166	Hex 0xA6				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	ID_RES_ 440K	ID_RES_ 200K	ID_RES_ 100K	STRESS	VB_SESS_ VLD	VB_SESS_ END
Read/Write	R	R	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ID_RES_440K	440-kΩ resistor connected to ID line
ID_RES_200K	200-kΩ resistor connected to ID line
ID_RES_100K	100-kΩ resistor connected to ID line
STRESS	Stress condition detected
VB_SESS_VLD	VBUS higher than VB_SESS_VLD (enable high), lower than VB_SESS_VLD (enable low)
VB_SESS_END	VBUS higher than VB_SESS_END (enable high), lower than VB_SESS_END (enable low)

9.6.27 CABLE DEBOUNCE

Register	CABLE DEBOUNCE	Debounce time before generating any VBUS and ID interrupt on INT_LATCH(_2). 32-kHz 8-bit counter. Default value: 5-ms (160)						
Page	2	Address	Dec # 186	Hex 0xBA				
Bit	7	6	5	4	3	2	1	0
Name	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7	CABLE_DE BOUNCE_7
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	1	0	1	0	0	0	0	0

Register bits description

CABLE_DEBOUNCE [7:0]	Debounce time (Dec 160 , Bin 10100000)

Notes:

Depending on the configuration of OE_INT_EN and SUSPEND bits, the USB interrupts are generated on either OE_INTN or P1_INT2 pins:

- OE_INT_EN=0 and SUSPEND=X readdresses the interrupts on P1_INT2 line,
- OE_INT_EN=1 and SUSPEND=0 readdresses the interrupts on P1_INT2 line,
- OE_INT_EN=1 and SUSPEND=1 readdresses the interrupts on OE_INTN line.

ID and VBUS interrupts are emitted after the cable debounce time.

Precharge bit (PREUSBOFF) must be disabled for USB applications.

USB-D bit controls the outputs towards the analog section. Once cleared, the outputs are reset to the default values of the registers.

r = read, w = write

s = set

c = clear

Once VRUS regulator is turned on through the power bus, the level shifter resets are enabled after the next access to the power bus. In particular, the LVS_USB2IO_AUTO bit does not work when the regulator is turned on via the I2C instructions. It is possible to manually release the reset signal by setting LVS_USB2IO_EN bit after disabling LVS_USB2IO_AUTO bit.

9.7 ELECTRICAL CHARACTERISTICS

Note:
(1) Not tested on production line.
(2) Not characterized.
(3) Not validated in laboratory.

5V-Tolerant Transceiver

Voltage

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
VRUSB Stress Clamp Voltage	V_{STRESS}		3.40	3.67	3.90	V
VRUSB Output Voltage In Stressed Conditions	V_{RUSB_STRESS}		3.40	3.67	3.90	V

Current

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
VRUSB Stress Return Current	I_{STRESS}		10	30	50	mA

ID

Termination

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone I_D Pull-Up To $V_{PH\_ID\_UP}$ Pull-Up Resistance On I_D Pin	$R_{PH\_ID\_UP}$ R_{XC_ID}		70	100	286	kΩ

Voltage

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone I_D Pull-Up Voltage I_D Pull-Up Voltage	$V_{PH\_ID\_UP}$ V_{ID_HI}	Connected to VRUSB	2.7	3.30	4.5	V
Phone I_D Pull-Down Voltage	$V_{PH\_ID\_DWN}$		-10	10	20	V

V_{BUS}

Termination

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
A-Device V_{BUS} Input Impedance To G_{ND}	$R_{A\_BUS\_IN}$	SRP (V_{BUS} Pulsing) capable A-device not driving V_{BUS}	10	70	100	kΩ
B-Device V_{BUS} SRP Pull-Down	$R_{B\_SRP\_DWN}$	5.25V / 8mA	656			Ω
B-Device V_{BUS} SRP Pull-Up	$R_{B\_SRP\_UP}$	(5.25V – 3V) / 8mA Pull-up voltage = 3V	281			Ω

Capacitance

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
On-The-Go Device V_{BUS} Bypass Capacitance (1) (2) (3)	C_{OTG_VBUS}	Component placed on board, Close to V_{BUS} pin	1.0	4.7	6.5	µF

Voltage

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone V_{BUS} Voltage Out V_{BUS} A-Device Output Voltage Low-Power Port	$V_{PH\_VBUS\_OUT}$ $V_{A\_VBUS\_OUT}$ V_{BUS}	$0 \le I_{VBUS} \le I_{A\_VBUS\_OUT} < 100$ mA Phone powered accessory (3V - 5.25V)	2.7	5.0	5.25	V

Current

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
B-Device (SRP Capable) Discharge Current (1) (2)	$I_{B\_DSCHG\_IN}$	$0 V \le V_{BUS} \le 5.25$			8	mA
B-Device (SRP Capable, Peripheral-Only) Unconfigured Average Current	$I_{B\_PO\_UNCFG}$	$0 V \le V_{BUS} \le 5.25$ V T_{AVG} = 1 ms			8	mA

Valid Input Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
A-Device V_{BUS} Valid	$V_{A\_VBUS\_VLD}$	For B-device proper operation	4.40	4.65		V
B-Device Session Valid	$V_{B\_SESS\_VLD}$ $V_{B\_SESS\_VLD}$		2.1	2.4	2.7	V

Phone Session Vld Threshold A-Device Session Valid	$V_{PH\_SESS\_VLD}$ $V_{A\_SESS\_VLD}$ $V_{A\_SESS\_VLD}$		0.8	1.1	1.4	V
B-Device Session End	$V_{B\_SESS\_END}$	Implemented, but can also use pull-down resistor to discharge V_{BUS}	0.2	0.5	0.8	V

Data-Line $D^{+/-}$

Terminations

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone $D^{+/-}$ Pull-Down A & B - Devices Data Line Pull-Down Bus Pull-Down Resistor On Downstream Port	$R_{PH\_DP\_DWN}$ $R_{PH\_DM\_DWN}$ R_{PD} R_{PD}		14.250	18	24.800	kΩ
Phone D^+ Pull-Up D^+ Pull-Up Resistance Bus Pull-Up Resistor On Upstream Port (Idle Bus) Bus Pull-Up Resistor On Upstream Port (Receiving)	$R_{PH\_DP\_UP}$ R_{DP_UP} R_{PUI} R_{PUA}	USB certification waiver	0.900	1.1	1.575	kΩ
Input Impedance Exclusive Of Pull-Up / Pull-Down	Z_{INP}		300			kΩ

Voltage

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone D^+ Pull-Up Voltage Carkit D^- Pull-Up Voltage Termination Voltage For Upstream Facing Port Pull-Up	$V_{PH\_DP\_UP}$ $V_{CR\_DM\_UP}$ V_{TERM}		3.0	3.3	3.6	V

Current

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Transceiver $D^{+/-}$ Leakage Current	$I_{XC\_DAT\_LKG}$		-2		2	µA

USB

Input Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Differential Common Mode Range	V_{CM}		0.8		2.5	V
Differential Input Sensitivity	V_{DI}		0.2			V
High (Driven)	V_{IH}		2.0			V
High (Floating)	V_{IHZ}		2.7		3.6	V
Low	V_{IL}				0.8	V

Output Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Output Signal Crossover Voltage	V_{CRS}	USB certification waiver	1.1	1.65	2.0	V
High (Driven)	V_{OH}		2.8	3.3	3.6	V
Low	V_{OL}		0.0	0.1	0.3	V

Ls Driver

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Fall Time	T_{LF}		75	150	300	ns
Rise Time	T_{LR}		75	150	300	ns
Rise & Fall Time Matching	T_{LRFM}		80	100	120	%

Ls Data Timings

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Width Of S_{E0} Interval During Differential Transition (1)	T_{LST}				210	ns
Upstream Facing Port Source Driver Jitter (Next) (1) (2)	T_{USDJ1}		-25	0	25	ns
Upstream Facing Port Source Driver Jitter (Paired) (1) (2)	T_{USDJ2}		-10	0	10	ns

Fs Driver

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Fall Time	T_{FF}		4	15	20	ns
Rise Time	T_{FR}		4	15	20	ns
Rise & Fall Time Matching	T_{FRFM}	USB certification waiver	80	100	110	%
Driver Output Resistance	Z_{DRV} / R_S	With internal resistors	28	36	44	Ω

Fs Data Timings

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Width Of S_{E0} Interval During Differential Transition	T_{FST}			4	14	ns
Source Driver Jitter To Next Transition (1) (2)	T_{SDJ1}		-2	0	2	ns
Source Driver Jitter For Paired Transitions (1) (2)	T_{SDJ2}		-1	0	1	ns

UART

Input Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Serial Interface Input High R_{XD} Input High On D^+	V_{IH_SER} $V_{IH\_RXD\_DAT}$		2.0			V
Serial Interface Input Low R_{XD} Input Low On D^+	V_{IL_SER} $V_{IL\_RXD\_DAT}$				0.8	V

Output Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Serial Interface Output High T_{XD} Output High On D^-	V_{OH_SER} $V_{OH\_TXD\_DAT}$	I_{SOURCE} = 4mA	2.4	3.3	3.6	V
Serial Interface Output Low T_{XD} Output Low On D^-	V_{OL_SER} $V_{OL\_TXD\_DAT}$	I_{SINK} = -4mA	0.0	0.1	0.4	V

Timings

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone UART Edge Rates (1)	$T_{PH\_UART\_EDGE}$	10% to 90%			1	µs

AUDIO

Terminations

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone Microphone Input Impedance	$Z_{PH\_MIC\_IN}$	Freq = 1kHz	10			kΩ
Phone Speaker Output Impedance	$Z_{PH\_SPKR\_OUT}$	Freq = 1kHz			200	Ω

Current

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone Speaker Source Current	$I_{PH\_SPKR\_SRC}$	$D^{+/-}$ grounded			20	mA

Input Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone Microphone Input Range	$V_{PH\_MIC\_IN}$		1.0		2.2	V

Output Levels

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone Speaker Output Bias	$V_{PH\_SPKR\_BIAS}$		0.7		1.6	V
Phone Speaker Output Range	$V_{PH\_SPKR\_OUT}$				2.2	V

CARKIT

Interrupts

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Phone D^+ Low Threshold	$V_{PH\_DP\_LO}$		0.4	0.5	0.6	V

OTHERS

USB Differential Receiver

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Propagation delay (1) DP / DM -> RCV	$DEL_{DP\_DM\_RCV}$	Driver's outputs unloaded	10	40	70	ns
Skew between RCV & VP (1)	$SKW_{RCV\_VP\_VM}$	Driver's outputs unloaded	-8	0	8	ns
Differential Receiver Hysteresis (1)	V_{RXD_HYS}		45	75	100	mV

USB Single-Ended Receivers

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Propagation delay (1) DP -> VP & DM -> VM	DEL_{DP_VP} DEL_{DM_VM}	Driver's outputs unloaded	10	40	70	ns
Single-Ended Hysteresis (1)	V_{SE_HYS}		100	250	400	mV
Switching Threshold	V_{TH}		0.8		2.0	V

USB Differential Driver

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
FS Propagation delay VP -> DP (1) VM -> DM (1)	$DEL_{FS\_VP\_DP}$ $DEL_{FS\_VM\_DM}$	Pull-downs R=15kΩ on both DP & DM / Pull-up R=1.5kΩ @ 3.6V on DP only (VP tr=tf=3ns)	10	20	40	ns
LS Propagation delay VP -> DP (1) VM -> DM (1)	$DEL_{LS\_VP\_DP}$ $DEL_{LS\_VM\_DM}$	Pull-downs R=15kΩ on both DP & DM / Pull-up R=1.5kΩ @ 3.6V on DM only (VP tr=tf=3ns)	25	100	175	ns

VBUS Wake-Up Comparator

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
VBUS Wake-Up Threshold	$V_{VBUS\_WK\_UP}$		1.6	1.8	2.0	V

ID Wake-Up Comparator

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
ID Wake-Up Threshold	$V_{ID\_WK\_UP}$		140	280	420	mV

VBUS Comparators

PARAMETER	SYMBOL	COMMENTS	MIN	TYP	MAX	UNIT
Hysteresis Voltage (1)	V_{VBUS_HYS}			200		mV

Table 41 : USB Transceiver Electrical Characteristics

10 BATTERY CHARGER

10.1 BATTERY CHARGER INTERFACE

The charging device can be either a charger with a low–output impedance regulated or non-regulated voltage source of 20V absolute maximum or a device plugged in the USB wall outlet. The device plugged in the USB wall outlet can be either a USB driver with a low-output impedance dc voltage source from 4.4V to 5.25V or a carkit with a low-output impedance dc voltage source from 4.75V to 5.25V. Two external PMOS power transistors, driven by ICTLAC2 and ICTLUSB2 of the T3031 device, control the choice between the charger input and the USB input. Their role is also to prevent reverse leakage current from the main battery in case of one of the two charging devices is connected to the mobile phone without delivering any voltage at its output. Two external PMOS power transistors driven by ICTLAC1 and ICTLUSB1 of the T3031 device, control the current flowing from the charging device to the main battery.

The main function of the battery charger interface is the charging control of both 1–cell Li–Ion battery or 3–series Ni–MH/Ni–Cd cell battery with the support of an external µC. The external µC enables the charge by forcing the programming bit CHEN to 1. The external µC select the charging device either by forcing the programming bit ACPATHEN to 1 for a charge with a charger or by forcing the programming bit USBPATHEN to 1 for a charge with the USB. The hardware forbidden having ACPATHEN and USBPATHEN forced to 1 in the same time.

The charging scheme for the Li–Ion battery is constant current first (typical current is 1xC) followed by constant voltage charging once a certain voltage threshold is reached (4.2 V typical). Charging is stopped when the charging current at constant voltage has decreased down to C/20 (typical). Because the BCI works in the linear mode, the power dissipation around the external components must be taken into account.

The charging scheme for the Ni–MH/Ni–Cd is constant current only. Charging is stopped when ΔV across battery terminals versus time inverts from positive to slightly negative (typically, a few mV per cell) or by any other criteria involving battery voltage or battery temperature. Ni–MH/Ni–Cd 3–cell battery voltage can reach 5.5 V at the end of a charge cycle.

In case of power dissipation problems around the external components, pulsed charge with a charger is also supported. The external µC enables the pulsed charge by forcing the programming bit PWMEN to 1. The hardware forbidden having the pulsed charge and the linear charge enable in the same time. A Pulsed Width-Modulated signal controls the externals PMOS transistors driven by ICTLAC1 and ICTLAC2 of the T3031 device. The frequency of the PWM signal is 1Hz typical.

In addition to the above charging schemes, the pre-charge is systematically applied when a battery charger or a carkit is connected to a switched–off mobile phone: a constant charging current (typically C/20) is applied automatically to the battery from PCHGAC or PCHGUSB of the T3031 device when the battery voltage is lower than 3.6 V. A specific pre-charge mode enables a full charge with the charger when the battery voltage is higher than 2.0V.

The BCI can also supply active portable accessory devices without any own supply by forcing the programming bit ACCSUPEN to 1. In this mode, the two external PMOS transistors driven by ICTLAC1 and ICTLAC2 works like two closed switches that connect the battery voltage to the device plugged into the charger wall outlet. The hardware forbidden having the accessory supply mode and the charge or pre-charge mode enable in the same time. When a charger is plug, the hardware disables automatically the accessory supply mode.

A watch-dog timer, using the CK32K clock, allows to automatically stop the battery charge after a programmable delay. The automatic stop is done by forcing CHEN or PWMEN programming bits to 0. An INT2 interrupt is generated when the automatic stop appears. The software can enable the watch-dog by forcing the BCI watch-dog key register BCIWDKEY to the dedicated value.

The watch-dog protection is automatically enabled when CHEN or PWMEN is forced to 1. In this case, the delay is set to 4.0s. The software can disable this protection by forcing the BCI watch-dog key register BCIWDKEY to WDKEY6.

10.2 CHARGING WITH A CHARGER

The magnitude of the reference charging current is set using the 8 bits CHGIREG register (1). A 8–bit DAC convert the content of this register. The magnitude of the reference charging voltage is set using the 10 bits CHGVREG register (2). A 10–bit DAC converts the content of this register. Both DAC outputs set the reference input of the analog charge loop. An error amplifier drives the gate of the external PMOS device via the terminal ICTLAC1 of the T3031 device.

For Li–Ion rechargeable batteries, when the battery voltage measured at terminal VBAT by the MADC reaches 4.2 V ±30 mV, the µC sets the charging control loop into constant voltage mode by changing the CHIV programming bit from 1 to 0. MESBAT programming bit should be forced to 1 to allow the battery voltage measure and the constant voltage charge mode.

During the constant voltage charge phase, the battery charge current is continuously monitored by the µC through the use of the MADC. When this current goes below a certain limit (C/20) the battery is declared fully charged and the µC terminates the charge by forcing the programming bit CHEN to 0.

The end of charge current threshold can be detected automatically by using the 8 bits CHGIREG register. A comparator allows, forcing PROCTL0, PROCTL1 and PROEN programming bits to the dedicated values, to switch off the charging current when the charging current fall below the threshold given by CHGIREG. The switch off is done by forcing CHEN programming bit to 0. PROCTL0, PROCTL1 and PROEN are forced using the 8 bits BCISKEY key register. An INT2 interrupt is generated when the comparator detects the programmed threshold.

During the constant current charge phase, a battery over voltage or battery over temperature threshold can be set using the 10 bits CHGVREG. A comparator allows, forcing PROCTL0, PROCTL1 and PROEN programming bits to the dedicated values, to switch off the charging current when the battery voltage or battery temperature reaches the threshold given by CHGVREG. The switch off is done by forcing CHEN programming bit to 0. PROCTL0, PROCTL1 and PROEN are forced using the 8 bits BCISKEY key register. An INT2 interrupt is generated when the comparator detects the programmed threshold.

The over voltage protection is automatically enabled when CHEN programming bit is forced to 1. In this case, the voltage threshold is set to a value relative to a VBAT pin of the T3031 device equal to 4.5V typical. The software can disable this protection by forcing BCISKEY key register to SKEY6.This protection have to be disabled during the constant voltage charge phase

An external µC should monitor the battery and control the charge loop via the I2C serial interface.

(1) : $CHGIREG\_code(dec) = \frac{2^8 - 1}{1.75} \times (Charging\_Current \times gain \times Rs + offset)$

with Rs = 0.22 Ohms, offset = OFFSN[1:0] and gain = CGAIN4 (BCICTL2 register).

(2) : $CHGVREG\_code(dec) = \frac{2^{10} - 1}{1.75} \times Charging\_Voltage \times (\text{VBAT to MADC input attenuation})$

10.3 CHARGING WITH A USB DEVICE OR A CARKIT

The charge with a USB device or a carkit is done using the same analog charge loop as the charge with a charger. The reference registers, the DAC and the error amplifier are the same. The error amplifier drives the gate of the external PMOS device via the terminal ICTLUSB1 of the T3031 device.

The automatics switch off coming from the end of charge current threshold or the battery over voltage or battery over temperature threshold can also be programmed during a charge with a USB device or a carkit.

Using the USB-protocol, an external µC should detect what is the maximum charge current to be set.

Taking into account the specifications of VBUS input of the T3031 device minimum voltage and the main battery maximum voltage, it might be not enough to charge the battery completely.

An external µC should monitor the battery and control the charge loop via the I2C serial interface.

10.4 BATTERY PRE-CHARGE

If the battery voltage is lower than 3.2 V (battery partially discharged or fully discharged), the charging scheme to be applied is the pre-charge. Pre-charge with a charger (AC pre-charge) or pre-charge with any USB accessory(a carkit, an USB device or USB charger) are supported. The mobile phone is not started until the battery gets sufficiently recharged up to 3.2 V; when this happens, the μC is started to control the fast charge cycle of the main battery, and the C/20 current can be switched off forcing PREACOFF or PREUSBOFF programming bits to 1. In case the μC did not stop the pre-charge, it is automatically stopped when the battery voltage is higher than 3.6V.

The selection between the AC pre-charge and the USB pre-charge is done automatically by hardware depending on the charger and the VBUS detection status. If the battery voltage is lower than 0.5 V typical, as soon as a charger or a USB accessory is detected, each correspondent pre-charge is started. If the battery voltage is higher than 0.5 V typical, the AC pre-charge is priority. In this case, if the charger device is present the AC pre-charge is started and if the charger device is not present but a USB accessory is present the USB pre-charge is started.

To detect a charger, VAC input of the T3031 device is sensed. If VAC is raising 400mV typical upper the battery voltage, STS_CHG status bit is forced to 1. STS_CHG is then forced to 0 when VAC is falling below the battery voltage typical. An INT2 interrupt is generated when the comparator detect the plug or unplug of the charger.

To avoid periodic plug and unplug detection when a non-regulated charger is used, STS_CHG is de-bounced. STS_CHG status bit is forced to 1 when the charger is plug and STS_CHG is forced to 0 32ms after the charger unplug.

To detect an USB accessory, the protocol used comes directly from the carkit specification CEA_936.

A comparator senses VBUS input of the T3031 device. If VBUS is higher than 4.4V, VBUSSTS status bit is forced to 1. An INT2 interrupt is generated when the comparator detect the VBUS voltage. If we are in ACTIVE mode, the software has to disable the pre-charge to be able to use the device connected to the USB port.

If VBUSSTS is forced to 1, the precharge start.

The electrical characteristics of the carkit detection are specified in the T3031 USB transceiver specification.

If the μC is started and a USB device is plugged, the software has to stop the USB pre-charge to be able to use the USB port for an other function.

The pre-charge currents are calculated with the relations below. The pre-charge currents are limited to 100mA for the AC pre-charge and 100mA for the USB pre-charge.

IVACprech = (VAC – VBAT)/(Rprech+Ron+Rloss)

IVBUSprech = (VBUS – VBAT)/(Rprech+Ron+Rloss)

A fast AC pre-charge could be programmed forcing BM_PRECH pin of the T3031 device to 0. BM_PRECH has to be floating to stay in the previous pre-charge mode.

If BM_PRECH pin is forced to 0 and the main battery voltage is higher than 2.0V, an fast AC pre-charge is set tightens ICTLAC1 and ICTLAC2 pins to 0. As for the previous mode, in case the μC did not stop the pre-charge, it is automatically stopped when the battery voltage is higher than 3.6V. In this mode, the charger device has to limit itself the charge current.

In the fast AC pre-charge mode, the hardware avoids having a main charge (linear or pulsed) and an fast AC pre-charge in the same time. So the fast AC pre-charge is automatically stopped when CHEN or PWMEN programming bits are forced to 1.

10.5 PULSED CHARGING SCHEME

The duty cycle of the 1Hz Pulsed Width-Modulated signal is set using the 10 bits PWMDTYCY register. A digital block converts the content of the register. The resulting one bit PWM signal that can be

read into the registers controls the externals PMOS transistors driven by ICTLAC1 and ICTLAC2 of the T3031 device.

This mode is only supported for charges with a charger. The charger device has to limit itself the charge current.

The battery charge current and the battery voltage are continuously monitored by the μC through the use of the MADC.

The automatics switch off coming from the battery over voltage or battery over temperature threshold can be programmed during a PWM charge. The over voltage protection is automatically enabled when PWMEN programming bit is forced to 1. In this case, the voltage threshold is set to a value relative to a VBAT pin of the T3031 device equal to 4.5V typical. The software can disable this protection by forcing BCISKEY key register to SKEY6.

An external μC should monitor the battery and control the duty cycle via the I2C serial interface.

10.6 CHARGING DEVICE DETECTION

The charger device detection is done by a comparison relative to VBAT level (see electrical characteristics). To ensure a good functionality of the detection, the voltage drop between VBAT level and the charger level must be greater than 100mV during all the functional mode (precharge , AC fast-precharge, charge).
Voltage drop = (Rsense + Ron external power mosfet+ Rloss) * I charge.

The USB device or carkit device detection in precharge mode is done by a comparison to fix level (see electrical characteristics 4.4V max). The VBUS unplug can be detected during the battery charge by making regular VBUS measurements via MADC.

10.7 ACCESSORY SUPPLY

Before entering this mode, an external μC should detect the accessory device plugged in the the AC outlet or the USB outlet.

The accessory supply mode can be enable only when the charger status bit STS_CHG is forced to 0 and the pre-charge disable programming bits PREACOFF and PREUSBOFF are forced to 1.

When ACCSUPEN is forced to 1, ICTLAC1 and ICTLAC2 or ICTLUSB1 and ICTLUSB2 pins are tight to 0 and the two external PMOS transistors connected to ICTLAC1 and ICTLAC2 or ICTLUSB1 and ICTLUSB2 works like two closed switches that connect the battery voltage to to the charger outlet input or the USB outlet input.

The external μC select the charging device either by forcing the programming bit ACPATHEN to 1 for an accessory connected to the AC outlet or by forcing the programming bit USBPATHEN to 1 for an accessory connected to the USB outlet. The hardware forbidden having ACPATHEN and USBPATHEN forced to 1 in the same time.

MESVAC programming bit should be forced to 0 to avoid a leakage current on the resistor ratio connected to VAC pin.

An over current protection threshold can be set using the 8 bits CHGIREG register. A comparator allows, forcing PROCTL0, PROCTL1, PROEN and LIMITEN programming bit bits to the dedicated values, to switch off the accessory supply when the supply current reach the threshold given by CHGIREG. The switch off is done by forcing ACCSUPEN programming bit to 0. PROCTL0, PROCTL1, PROEN and LIMITEN are forced using the 8 bits BCISKEY key register. An INT2 interrupt is generated when the comparator detects the programmed threshold.

10.8 BATTERY MONITORING

Battery monitoring is performed by the multiplexed 10–channel 10–bit ADC MADC used to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage and the backup battery voltage. The signals are converted into digital 10–bit words, stored in auxiliary ADC output registers and transmitted to an external μC.

Battery charging current is sensed using a 220–mΩ external resistor connected across terminals VCCS and VBATS of the T3031 device. The battery voltage value is measure using the VBAT terminal of the T3031 device.

In order to measure the temperature and identify the type of the battery, the BCI includes dc current sources that provide a bias current through the ADCIN4 and ADCIN5 or ADCIN3 input pins of the MADC. These three terminals should be connected to the thermal sensing devices (thermistor) and to the battery type resistor and the resulting voltages can be measured using the MADC. For power consumption saving, these current sources are active only in switched–on mode when a measurement is required. The current source on ADCIN5 or ADCIN3 is programmable (3 bits) in the 10–μA to 80–μA ranges. The current source on ADCIN4 is arbitrarily set to 10 μA.

The THEN programming bit enables the thermistor current source. The THSIGN programming bit set the sign of the current source. The THSENS(0-2) programming bits set the current magnitude between 10 and 80 μA. The THENSA programming bit allows the use of ADCIN5 or ADCIN3 input for thermal sensing. The battery type current source has a fixed value 10 μA and is enabled by the TYPEN programming bit.

A calibration routine storing the voltage across thermal sensor at two temperatures is necessary to compensate for dispersions of voltage across thermal sensor terminals.

10.9 MODES OF OPERATION

The following table gives the functions that could be programmed in the different modes of operation.

		Modes of operation			
		Main Charge	Pulsed Width Modulation	Accessory Supply	Pre-charge
Functions	Battery over voltage protection	Enable by default VBAT=4.5V	Enable by default VBAT=4.5V	X	Automatic switch-off VBAT=3.8V
	Battery over temperature protection	X (1)	X	X	
	Li Ion end of charge detection	X	X		
	Reverse current limitation			X	
	Watch dog	Enable by default 4s	Enable by default 4s	X	
	Battery type measurement	X	X	X	
	Battery temperature measurement	X	X	X	

(1) "X" Means that the function could be programmed in this mode of operation

The following table gives the enable and configuration signals associated to the different modes of operation.

		Modes of operation			
		Main Charge	Pulsed Width Modulation	Accessory Supply	Pre-charge
Control	Enable	CHEN=1	PWMEN=1 & ACPATHEN=1	ACCSUPEN=1	Enable by default and disable by PREACOFF=1 PREUSBOFF=1
	Configuration	CHIV ACPATHEN USBPATHEN CHGV CHGI CGAIN4 OFFSEN OFFSN(1:0) MESBAT	PWMDTYCY	ACPATHEN USBPATHEN	BM_PRECH (pin)

Table 42 : Operation Modes of Battery Charger

10.10 HARDWARE CONTROL PROTECTIONS

The Hardware control protections are integrated in the T3031 battery charger. Each protection is implemented to avoid a software error that could damage the T3031 device or the external components.

The following table list the hardware control protections implemented.

Protection	Explication	Example		
Priority between main charge, PWM mode and accessory supply mode	If CHEN or PWMEN or ACCSUPEN is enabling, a second bit could not be enable.	Write CHEN=1 Write PWMEN=1 Write ACCSUPEN=1	=> => =>	CHEN=1, PWMEN=0, ACCSUPEN=0 CHEN=0, PWMEN=1 ACCSUPEN=0 CHEN=0, PWMEN=0, ACCSUPEN=1
	If CHEN, PWMEN, ACCSUPEN are enabling at the same time, CHEN has the priority on PWMEN and ACCSUPEN, PWMEN has the priority on ACCSUPEN.	Write CHEN=1, PWMEN=1 and ACCSUPEN=1	=>	CHEN=1, PWMEN=0, ACCSUPEN=0
Priority between ACPATHEN and USBPATHEN	If ACPATHEN or USBPATHEN is enabling, the other bit could not be enable.	Write ACPATHEN=1 Write USBPATHEN=1	=> =>	ACPATHEN=1, USBPATHEN=0 ACPATHEN=0 USBPATHEN=1
	If ACPATHEN and USBPATHEN are enabling at the same time, ACPATHEN has the priority on USBPATHEN.	Write ACPATHEN=1 and USBPATHEN=1	=>	ACPATHEN=1, USBPATHEN=0
Security between LIMITEN and CHEN	LIMITEN could not be enable when CHEN=1	Write CHEN=1 Write SKEY5	=> =>	CHEN=1, LIMITEN=0 CHEN=1, PROEN=1, LIMITEN=0
Security between VRVBUS enable and carkit pre-charge	If VRVBUS is enable, the carkit pre-charge is stopped	 Write VRVBUS_EN=1	 =>	VRVBUS_EN=0, PREUSBOFF=0 VRVBUS_EN=1, PREUSBOFF=1
Security between STS_CHG and accessory supply mode	If STS_CHG rise, the accessory supply mode is stopped	Write ACCSUPEN=1 STS_CHG=1	=> =>	ACCSUPEN=1 ACCSUPEN=0
Over voltage protection automatically stated in Main charge and PWM mode	If CHEN=1 or PWMEN=1, the over voltage protection is stated			
Watch-dog automatically stated in Main charge and PWM mode	If CHEN=1 or PWMEN=1, the watch-dog is stated			
Charger status signal de-bouncing	STS_CHG is debounced before entering in the register	Charger plug Charger unplug	=> =>	STS_CHG=1 after 62.5µs STS_CHG=0 after 32ms

Table 43 : Hardware Control Protections

10.11 BATTERY CHARGER BLOCK DIAGRAM

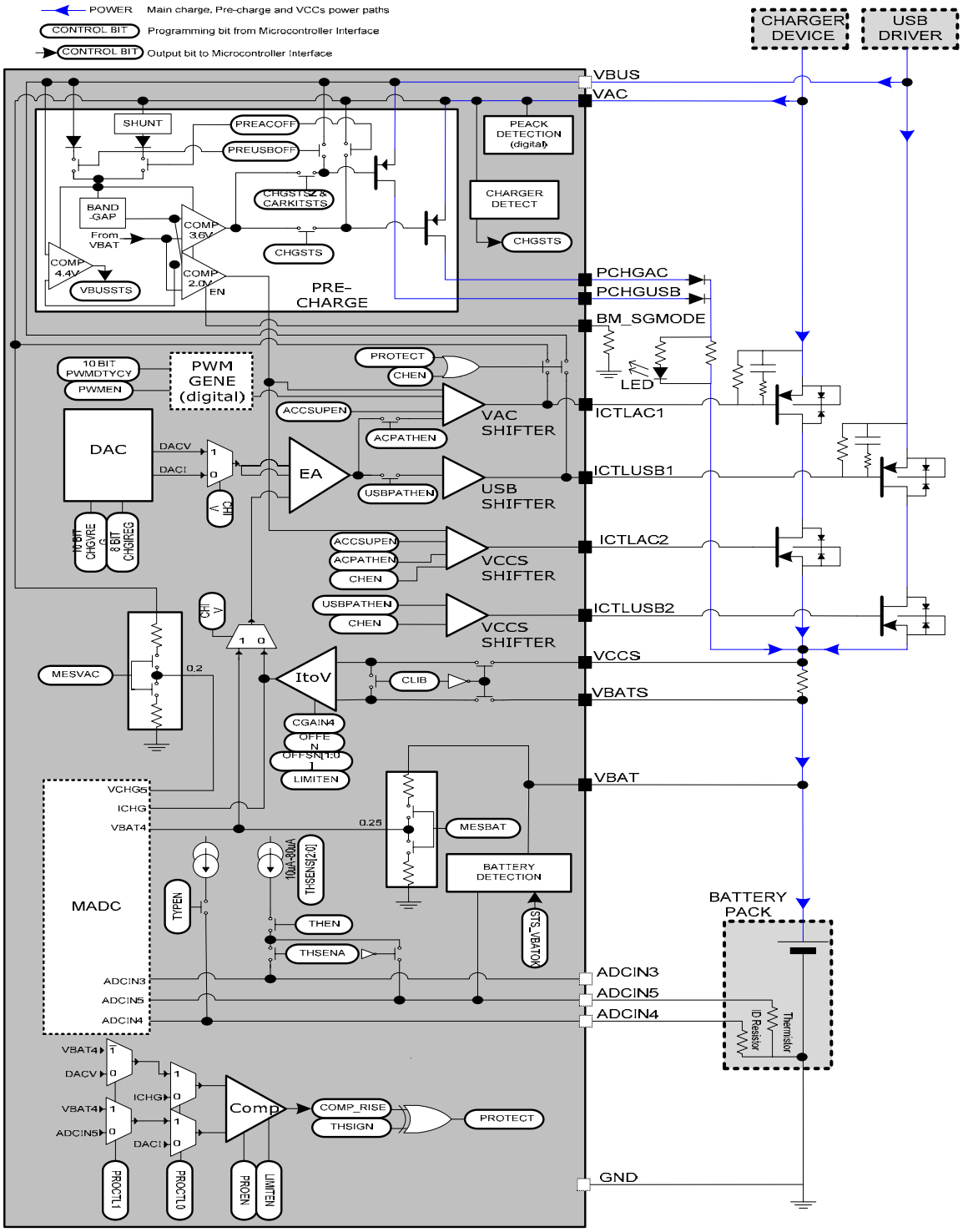


Figure 28 : Battery Charger Block Diagram

10.12 REGISTERS

10.12.1 CHGVREG2

Register	CHGVREG2							
Page	0	Address	Dec # 119		Hex 0x77			
Bit	7	6	5	4	3	2	1	0
Name	CHGV_1	CHGV_0	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD
Read/Write	R/W	R/W	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CHGV [1:0]	LSB of the 10–bit DAC register for setting a voltage for main battery charging or fixing the battery over voltage protection or the temperature protection
RSRVD (bit 5 – bit 0)	Reserved bits

10.12.2 CHGVREG1

Register	CHGVREG1							
Page	0	Address	Dec # 120		Hex 0x78			
Bit	7	6	5	4	3	2	1	0
Name	CHGV_9	CHGV_8	CHGV_7	CHGV_6	CHGV_5	CHGV_4	CHGV_3	CHGV_2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CHGV [9:2]	MSB for 10–bit DAC register for setting a voltage for main battery charging or fixing the battery over voltage protection or the temperature protection (formula used in section 10.2). **Note:** CHGV is automatically programmed at 1010010010 (4.5V) when CHEN or PWMEN is write at 1

10.12.3 CHGIREG

Register	CHGIREG							
Page	0	Address	Dec # 121		Hex 0x79			
Bit	7	6	5	4	3	2	1	0
Name	CHGI_7	CHGI_6	CHGI_5	CHGI_4	CHGI_3	CHGI_2	CHGI_1	CHGI_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CHGI [7:0]	8–bit DAC register for setting a current for main battery charging or fixing the end of charge current detection (formula used in section 10.2).

10.12.4 BCISECU

Register	BCISECU							
Page	0	Address	Dec # 122		Hex 0x7A			
Bit	7	6	5	4	3	2	1	0
Name	PROCTL_1	PROCTL_0	THSIGN	PROEN	LIMITEN	PROTECT	RSVRD	RSVRD
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

PROCTL [1:0]	BCI comparator configuration: PROCTL(1:0) = 00 : comparator power down, with PROEN=0 PROCTL(1:0) = 01 : battery temperature sensing, with PROEN=1 PROCTL(1:0) = 10 : end of charge current sensing, with PROEN=1 PROCTL(1:0) = 11 : battery voltage sensing, with PROEN=1
THSIGN	Negative Thermistor measure THSIGN= 0 : battery temperature with positive coefficient sensing, with PROEN=1 THSIGN= 1 : battery temperature with negative coefficient sensing, with PROEN=1
PROEN	Enable (PROEN= 1) the over temperature, over voltage or End of Charge current, comparator.
LIMITEN	Enable reverse current limitation.
PROTECT	Status of over-voltage, over-temperature or LiIon end of charge detection (PROTECT='1': protection comparator rises). **Note 1**: When PROTECT rises, CHEN, PWMEN and ACCSUPEN are automatically forced to 0 and an acknowledge is needed to write them again (see Application paragraph) **Note 2**: When PROTECT rises, an INT2 (INT2PRTCTZ) is automatically generated **Note 3**: PROTECT bit is a real time status bit reflecting the actual state of the protection. This protection is automatically released when it is no more needed. Therefore, in some cases (Current Limitation) the PROTECT bit can be read as "0" (protection released after it was triggered) whereas an interrupt has occurred (on INT2 line) indicating that the protection was triggered. In order to have a correct interrupt status, ONLY the status bit associated to the interrupt line 1 (BCI_PROTECT), in the interrupt register INT2_P1_STS_A, bit_0 must be used. The PROTECT bit MUST NOT be used as a status bit for the interrupt generation.
RSRVD (bit 1 - bit 0)	Reserved bits

10.12.5 BCISKEY

Register	**BCISKEY**							
Page	**0** Address	**Dec # 123**	**Hex 0x7B**					
Bit	7	6	5	4	3	2	1	0
Name	SKEY_7	SKEY_6	SKEY_5	SKEY_4	SKEY_3	SKEY_2	SKEY_1	SKEY_0
Read/Write	W	W	W	W	W	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

SKEY [7:0]	Key code of the security bits writing, following key values should be written before their corresponding bit is write : "SKEY1" : 10101010: battery over temperature protection (battery with positive thermistor) : PROCTL(1:0) = 01; THSIGN = 0; PROEN = 1; LIMITEN = 0 "SKEY2" : 01010101: battery over temperature protection (battery with negative thermistor) : PROCTL(1:0) = 01; THSIGN = 1; PROEN = 1; LIMITEN = 0 "SKEY3" : 11011011: LiIon end of charge detection (current sensing) : PROCTL(1:0) = 10; THSIGN = 0; PROEN = 1; LIMITEN = 0 "SKEY4" : 10111101: battery over voltage protection

	: PROCTL(1:0) = 11; THSIGN = 0; PROEN = 1; LIMITEN = 0 "SKEY5" : 11100011: reverse current limitation for accessory supply mode : PROCTL(1:0) = 10; THSIGN = 0; PROEN = 1; LIMITEN = 1 "SKEY6" : 00011010: comparator power down and PROTECT acknowledge : PROCTL(1:0) = 00; THSIGN = 0; PROEN = 0; LIMITEN = 0 : Able CHEN, ACCSUPEN and PWM write after a PROTECT rise

10.12.6 BCICTL1

Register	BCICTL1							
Page	0	Address	Dec # 124	Hex 0x7C				
Bit	7	6	5	4	3	2	1	0
Name	THSENSA	TYPEN	THEN	THSENS_2	THSENS_1	THSENS_0	CHIV	CHEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

THSENSA	Select ADCIN5 (THENSA= 0) or ADCIN3 (THENSA= 1) for main battery temperature sensing.
TYPEN	Enables bias current for main battery type reading.
THEN	Enables bias current for main battery temperature sensing.
THSENS [2:0]	Sets eight possible values for thermal sensor bias current.
CHIV	Selects constant current (CHIV= 1) or constant voltage charging mode (CHIV= 0).
CHEN	Enables the main charge with charger or USB. **Note 1**: CHEN can be read only 62.5us after a write **Note 2**: When CHEN rises, the watch-dog and the over voltage protections are automatically started **Note 3**: CHEN automatically falls when the watch-dog overflow (WOVF) or the protect overflow (PROTECT) rise, CHEN needs an acknowledge (write WDKEY6 or SKEY6) before being raised again **Note 4**: CHEN could not be raised when PWMEN is equal to 1 or when ACCUPEN is equal to 1

10.12.7 BCICTL2

Register	BCICTL2							
Page	0	Address	Dec # 125	Hex 0x7D				
Bit	7	6	5	4	3	2	1	0
Name	OFFEN	OFFSN_1	OFFSN_0	CGAIN4	CLIB	ACCSUPEN	ACPATHEN	USBPATHEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

OFFEN	Enable offset settings for current to voltage conversion.
OFFSN [1:0]	Set 4 possible values for current to voltage conversion offset (CGAIN4=0): [1] 00 : + 100 mV [2] 10 : + 200 mV [3] 01 : + 300 mV [4] 11 : + 400 mV

CGAIN4	Reduce the gain of the current to voltage converter from 10 (CGAIN4=0) to 4 (CGAIN4= 1).
CLIB	Allows (CLIB= 1) a zero calibration routine to the I–to–V converter
ACCSUPEN	Enable (ACCSUPEN= 1) the Accessory Supply mode. **Note_1**: ACCSUPEN can be read only 62.5us after a write **Note_2**: ACCSUPEN automatically falls when the protect overflow (PROTECT) rises, ACCSUPEN needs an acknowledge (write SKEY6) before being raised again **Note_3**: ACCSUPEN could not be raised when PWMEN is equal to 1, when CHEN is equal to 1 or when STS_CHG is equal to 1
ACPATHEN	Enable (ACPATHEN=1) the AC power path. **Note**: ACPATHEN could not be raised when USBPATHEN is equal to 1
USBPATHEN	Enable (USBPATHEN=1) the USB power path. **Note**: ACPATHEN could not be raised when USBPATHEN is equal to 1

10.12.8 BCIPWM2

Register **BCIPWM2**
Page **0** Address **Dec # 126** **Hex 0x7E**

Bit	7	6	5	4	3	2	1	0
Name	PWMDTYCY_1	PWMDTYCY_0	PWMEN	PWM	RSRVD	RSRVD	RSRVD	RSRVD
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

PWMDTYCY [1:0]	10-Bit register for setting PWM duty cycle (2 LSBs) PWMDTYCY[9:0] = 0x000 the PWM duty cycle for BCI pulsed charging mode will be 0. (0/1023) PWMDTYCY[9:0} = 0x3FF the PWM duty cycle for BCI pulsed charging mode will be 1.
PWMEN	Enable and start (PWMEN=1) the PWM signal generation. **Note_1**: PWMEN can be read only 62.5us after a write **Note_2**: ACPATHEN have to be set to 1 to activate PWM mode **Note_3**: When PWMEN rises, the watch-dog and the over voltage protections are automatically started (see Application paragraph) **Note_4**: PWMEN automatically falls when the watch-dog overflow (WOVF) or the protect overflow (PROTECT) rise, PWMEN needs an acknowledge (write WDKEY6 or SKEY6) before being raised again (see Application paragraph) **Note_5**: PWMEN could not be raised when CHEN is equal to 1 or when ACCUPEN is equal to 1
PWM	PWM signal.

10.12.9 BCIPWM1

Register **BCIPWM1**
Page **0** Address **Dec # 127** **Hex 0x7F**

Bit	7	6	5	4	3	2	1	0
Name	PWM DTYCY_9	PWM DTYCY_8	PWM DTYCY_7	PWM DTYCY_6	PWM DTYCY_5	PWM DTYCY_4	PWM DTYCY_3	PWM DTYCY_2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

PWMDTYCY [9:2]	10-Bit register for setting PWM duty cycle (8 MSBs) PWMDTYCY[9:0] = 0x000 the PWM duty cycle for BCI pulsed charging mode will be 0. (0/1023) PWMDTYCY[9:0} = 0x3FF the PWM duty cycle for BCI pulsed charging mode will be 1.

10.12.10 BCIWDKEY

Register	BCIWDKEY							
Page	0	Address	Dec # 128		Hex 0x80			
Bit	7	6	5	4	3	2	1	0
Name	WDKEY_7	WDKEY_6	WDKEY_5	WDKEY_4	WDKEY_3	WDKEY_2	WDKEY_1	WDKEY_0
Read/Write	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Register bits description

WDKEY [7:0]	Key code of the Watch-Dog timer, following key values should be written before their corresponding delay is reached : "**WDKEY1**" : 10101010: 1s (and WEN forced to 1) "**WDKEY2**" : 01010101: 2s (and WEN forced to 1) "**WDKEY3**" : 11011011: 4s (and WEN forced to 1) "**WDKEY4**" : 10111101: 8s (and WEN forced to 1) "**WDKEY5**" : not used "**WDKEY6**" : 00110011: Disable Watch-Dog protection.

10.12.11 BCIWD

Register	BCIWD							
Page	0	Address	Dec # 129		Hex 0x81			
Bit	7	6	5	4	3	2	1	0
Name	WOVF	WEN	WSTS_1	WSTS_0	RSRVD	RSRVD	RSRVD	RSRVD
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	1	0	0	0	0	0

Register bits description

WOVF	Watch-dog over flow when WOVF=1. **Note_1**: When WOVF rises, CHEN and PWMEN are automatically forced to 0 and an acknowledge is needed to write them again **Note_2**: When WOVF rises, an INT2 (INT2WOVFZ) is automatically generated
WEN	Enable and start (WEN=1) the Watch-dog timer. **Note**: WEN can be read only 62.5us after a WKEY write
WSTS [1:0]	Watch-dog status: WSTS = 00 : 1s count is on-going WSTS = 01 : 2s count is on-going WSTS = 10 : 4s count is on-going WSTS = 11 : 8s count is on-going
RSRVD (bit 3 - bit 0)	Reserved bits

10.12.12 BCICTL3

Register	BCICTL3							
Page	0	Address	Dec # 131		Hex 0x83			
Bit	7	6	5	4	3	2	1	0
Name	PREACOFF	PREUSBOFF	MESBAT	MESVAC	RSRVD	RSRVD	VBUSSTS	RSRVD
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

PREACOFF	Disable (PREACOFF=1) the AC pre-charge.
PREUSBOFF	Disable (PRESUBOFF=1) the carkit pre-charge.
MESBAT	Connects resistive divider to main battery. **Note**: MESBAT is automatically raised when CHEN or PWMEN is write at 1
MESVAC	Connects resistive divider charger input.
RSRVD (bit 3 - bit 2)	Reserved bits
VBUSSTS	Status of VBUS presence check (VBUSSTS='0': no VBUS detected). **Note**: When VBUSSTS rises, an INT2 (INT2VBUSZ) is automatically generated
RSRVD (bit 0)	Reserved bit

10.13 ELECTRICAL CHARACTERISTICS

VBAT = 3.6 V, R_S = 0.22 Ω, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VAC input voltage range (1)		4.8		20	V
VAC slew rate				5	V/µs
VBUS input voltage range (external)		4.4	5	5.25	V
VBUS input voltage range (internal)		3	5	5.25	V
AC Pre-charge Ron	Measured between VAC and PCHGAC, VBAT=0.5v VAC=6.8v & 20v $IVAC_{PRECH}$ = 100 mA	1	4	10	Ω
Car kit Pre-charge Ron	Measured between VBUS and PCHGUSB, VBAT=0.5v VBUS=5.0v $IVBUS_{PRECH}$ = 100 mA	1	4	10	Ω
PCHGAC pin leakage	Pre-charge OFF, VAC=5V, PCHGAC = 0V			+/- 1	µA
Current–to–voltage conversion slope (2)	(VCCS-VBATS) rising from 0.1 V to 0.17 V: CGAIN4=0	1.76	2.2	2.64	mV/mA
	(VCCS-VBATS) rising from 0.25 V to 0.425 V: CGAIN4=1	0.704	0.88	1.056	
ICTLAC1 output voltage swing (ACPATHEN=1)	$I_{ICTLAC1}$ =-10 µA, CHEN =1, PWMEN=1, PWMDTYCY=0x000	VAC-0.3			V
	$I_{ICTLAC1}$ =+10 µA, CHEN =1, PWMEN=1, PWMDTYCY=0x3FF			0.35	
	$I_{ICTLAC1}$ =+5 µA, CHEN =1, MESBAT=1, CHGVREG=0x3FF			0.8	
	$I_{ICTLAC1}$ =-5 µA, CHEN =1, MESBAT =1, CHGVREG=0x000			0.35	
	$I_{ICTLAC1}$ =-10 µA, BM_PRECH=0, VBAT=3.2V	VAC-0.3			
	$I_{ICTLAC1}$ =+10 µA, BM_PRECH=0, VBAT=3.2V			0.35	
ICTLUSB1 output voltage swing (USBPATHEN=1)	$I_{ICTLUSB1}$ =+5 µA, CHEN =1, MESBAT=1, CHGVREG=0x3FF			0.8	
	$I_{ICTLUSB1}$ =-5 µA, CHEN =1, MESBAT =1, CHGVREG=0x000			0.35	
ICTLAC2 output voltage swing (ACPATHEN=1)	$I_{ICTLAC2}$ =-10 µA, CHEN =1, PWMEN=1, PWMDTYCY=0x000	VCCS-0.3			
	$I_{ICTLAC2}$ =+10 µA, CHEN =1, PWMEN=1, PWMDTYCY=0x3FF			0.35	
ICTLUSB2 output voltage swing	$I_{ICTLAC2}$ =-10 µA, CHEN =1, USBPATHEN=0	VCCS-0.3			
	$I_{ICTLAC2}$ =+10 µA, CHEN =1, USBPATHEN=1			0.35	
AC Pre-charge switch-off time	VAC=6.8V, Rprech=100Ω, VBAT threshold=3.8V		75	100	µs
USB Pre-charge switch-off time	VBUS=5.0V, Rprech=100Ω, VBAT threshold=3.8V		30	50	µs
AC Pre-charge switch-off time in AC fast pre-charge mode	VAC=6.8V, C=22nF and R=1.5Ω connected to ICTLAC1, VBAT threshold=3.8V		60	160	µs
AC Constant Voltage Charge over-voltage switch-off time	VAC=6.8V, C=22nF and R=1.5Ω connected to ICTLAC1, 600mA constant current programmed, VBAT threshold=4.5V		60	160	µs
USB Constant Voltage Charge over-voltage switch-off time	VBUS=5.0V, C=22nF and R=1.5Ω connected to ICTLUSB1, 600mA constant current programmed, VBAT threshold=4.5V		85	130	µs
AC Constant Voltage Charge over-voltage switch-off time	VAC=6.8V, C=22nF and R=1.5Ω connected to ICTLUSB1, 500mA charge current, VBAT=4.2V		190	300	µs
USB Constant Voltage Charge over-voltage switch-off time	VBUS=5.0V, C=22nF and R=1.5Ω connected to ICTLUSB1, 500mA charge current, VBAT=4.2V		190	300	µs
Battery voltage at pre-charge end	VBAT input, Max current depends on external resistor	3.6	3.8	4.0	V
Battery voltage threshold to start AC fast pre-charge	VBAT input		2.0		V
VAC to MADC input attenuation	VAC from 4.8 V to 6.8 V	0.15	0.20	0.30	V/V
VBAT to MADC input attenuation	VBAT from 3.0 V to 5.5 V	0.2	0.25	0.35	V/V
Current–to–voltage conversion offset	OFFEN=1, OFFSN(1:0)=00, CGAIN4=0, LIMITEN=0		100		mV
	OFFEN=1, OFFSN(1:0)=01, CGAIN4=0, LIMITEN=0		300		mV
	OFFEN=1, OFFSN(1:0)=10, CGAIN4=0, LIMITEN=0		200		mV
	OFFEN=1, OFFSN(1:0)=11, CGAIN4=0, LIMITEN=0	300	400	500	mV
Current–to–voltage conversion offset in reverse mode	OFFEN=1, OFFSN(1:0)=00, CGAIN4=1, LIMITEN=1		0.24		V
	OFFEN=1, OFFSN(1:0)=01, CGAIN4=1, LIMITEN=1		0.71		V
	OFFEN=1, OFFSN(1:0)=10, CGAIN4=1, LIMITEN=1		0.51		V
	OFFEN=1, OFFSN(1:0)=11, CGAIN4=1, LIMITEN=1		0.95		V

Current–to–voltage conversion offset in reverse mode	OFFEN=1, OFFSN(1:0)=00, CGAIN4=0, LIMITEN=1		0.61		V
	OFFEN=1, OFFSN(1:0)=01, CGAIN4=0, LIMITEN=1		1.77		V
	OFFEN=1, OFFSN(1:0)=10, CGAIN4=0, LIMITEN=1		1.26		V
	OFFEN=1, OFFSN(1:0)=11, CGAIN4=0, LIMITEN=1		2.36 (3)		V
Charge Voltage DAC linear range	CHIV=0	0AF		352	hex
Charge Current DAC linear range	CHIV=1	2C		FF	hex
Temperature sensing DAC resolution			3		Bit
Temperature sensing DAC LSB	R(IREF) = 120 kΩ, ADCIN5=ADCIN3 = 1V, THENSA=0/1 THSENS[2-0]=000	8	10	12	µA
Temperature sensing DAC INL/DNL	R(IREF) = 120 kΩ, ADCIN5=ADCIN3 = 1V, THENSA=0/1			0.2	LSB
ADCIN4 dc current source for battery identification	R_{IREF} = 120 kΩ, ADCIN4 = 1 V, TYPEN=1	8	10	12	µA
Main Battery presence detect threshold	CHEN =0, measured through ADCIN5 rising voltage and sourced current, monitoring STS_VBATOK value, VAC=4.8 V & 20 V	0		100	kΩ

NOTES: 1. The maximum voltage value of the charging device is 20 V (process limitation). The minimum voltage value of the charging device is: VBATMAX + diode drop + 0.2 Ω resistor drop + VDC drop.
Where VBATMAX is the maximum voltage value of the battery (4.2 V for Li–ion battery). For example to charge Li–ion battery with 1–A fast current charge, the minimum voltage value of the charging device must be 5.1 V.
2. MADC output code = (VCCS - VBATS) * 10 + offset with CGAIN4=0
MADC output code = (VCCS - VBATS) * 4 with CGAIN4 = 1, OFFSEN = 0
3. 2.4V is too high compared to MADC input range (1.75V) so this value cannot be tested

VBAT = 3.6 V, VAC=4.8 V unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Positive over temperature threshold	PROCTL(1:0)=01, THSIGN=0, CHVREG(9:0)=0x3FF	1.65	1.75	1.85	V
	PROCTL(1:0)=01, THSIGN=0, CHVREG(9:0)=0x0AF	0.2	0.3	0.4	
	CHIV=1, CGAIN4=1, CHGIREG(7:0)=0xFF, VCCS=VBATS=VBAT, measured through ADCIN5 rising voltage, monitoring ICTLAC1				
Negative over temperature threshold	PROCTL(1:0)=01, THSIGN=1, CHVREG(9:0)=0x3FF	1.65	1.75	1.85	V
	PROCTL(1:0)=01, THSIGN=1, CHVREG(9:0)=0x0AF	0.2	0.3	0.4	
	CHIV=1, CGAIN4=1, CHGIREG(7:0)=0xFF, VCCS=VBATS=VBAT, measured through ADCIN5 rising voltage, monitoring ICTLAC1				
Falling End of Charge Current threshold (4)	PROCTL(1:0)=10, OFFEN=0, CHGIREG(7:0)=0xFF, CGAIN4=0, CHEN =1, MESBAT=1, CHIV=0, measured through MADC, (VCCS-VBATS) falling voltage, monitoring ICTL	165	175	185	mV
Over voltage threshold when default value (5)	PROCTL(1:0)=11, MESBAT=1, CHIV=1, CGAIN4=1, CHGIREG(7:0)=0xFF, VCCS=VBATS=VBAT measured through MADC, VBAT rising voltage, monitoring ICTL	4.4	4.5	4.6	V

4. MADC output code = VBAT * 0.25, 5. Can be change by programming CHGVREG register

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Charger presence detect threshold	VBAT=3.6V, rising edge	VBAT +0.2	VBAT +0.4	VBAT +0.65	V
Charger unplug detect threshold	VBAT=3.6V, falling edge	VBAT	VBAT +0.05	VBAT +0.1	V
Carkit detection consumption	VBUS=5.0V			500	µA
VBUS detection threshold		4	4.25	4.4	V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Watch-dog delay (6)	KEY[7:0] = 10101010		32000*T		(7)
	01010101		64000*T		
	11011011		128000*T		
	10111101		256000*T		

6. Enable by default at when CHEN=1, 7. T : 1/CK32K clock.

Table 44 : Battery Charger Electrical Characteristics

11 POWER MANAGEMENT SYSTEM

11.1 SYSTEM OVERVIEW

The power management T3031 (Triton_Lite) chip controls the power up, power down and power transitions of other devices associated to a specific functionality. Each one of those devices is capable through different means of generating a request of power state transition to the T3031 chip.
The T3031 chip manages the power of the Locosto, RF and Peripheral devices.
The Locosto device is a digital base band processor, the RF device is the RF transmission reception stage. The peripheral device may be a Bluetooth device. All the devices are supplied by two batteries, the main battery MB and the backup battery BB.
At the first valid main battery insertion, the internal reset is released and the VRRTC power domain rises up providing the supply to the 32 kHz oscillator. The VRRTC low dropout linear voltage regulator supplies the embedded real time clock 32 kHz and also the power management state machines.
The T3031 chip is ready to accept global hardware requests of power transitions, in this state the power bus is still in the slave mode and the 32 kHz clock is not provided externally. The power bus is in the master mode when a global hardware request of power state transition is detected. The T3031 chip actives the reference resources, next the power resources and finally the ON_nOFF reset signal and the CLK_ENable signal. Those signals active the power resources for both T3031 and the external devices and enable the RF clock signal. The 32 kHz clock is now provided externally.
The power state change requests are
The global hardware inputs HW :

- the detection of valid ON/OFF button press PWON
- the detection of accessory insertion RPWON
- the detection of charger insertion CHG
- the detection of USB insertion USB
- the detection of RTC ALARM event, RTC (internal signal)

The single hardware WAKEUP input

- WAKEUP1 is the digital base band processor request, the VRIO regulator supplying the I/Os has to be enabled
- PCLKREQ is the peripheral request or WAKEUP2, the VRIO regulator supplying the I/Os has to be enabled

The software inputs SW, the processor has to be supplied.

- these requests are sent to the T3031 chip through the I2C bus

The power management of T3031 can independently drive three subsystems or different groups of external devices in parallel P1,P2, P3
P1 is associated to the digital base band processor or modem
P2 is associated to the application processor
P3 is associated to the peripherals
There are three concurrent state machines of power management, each one associated to P1,P2, P3.

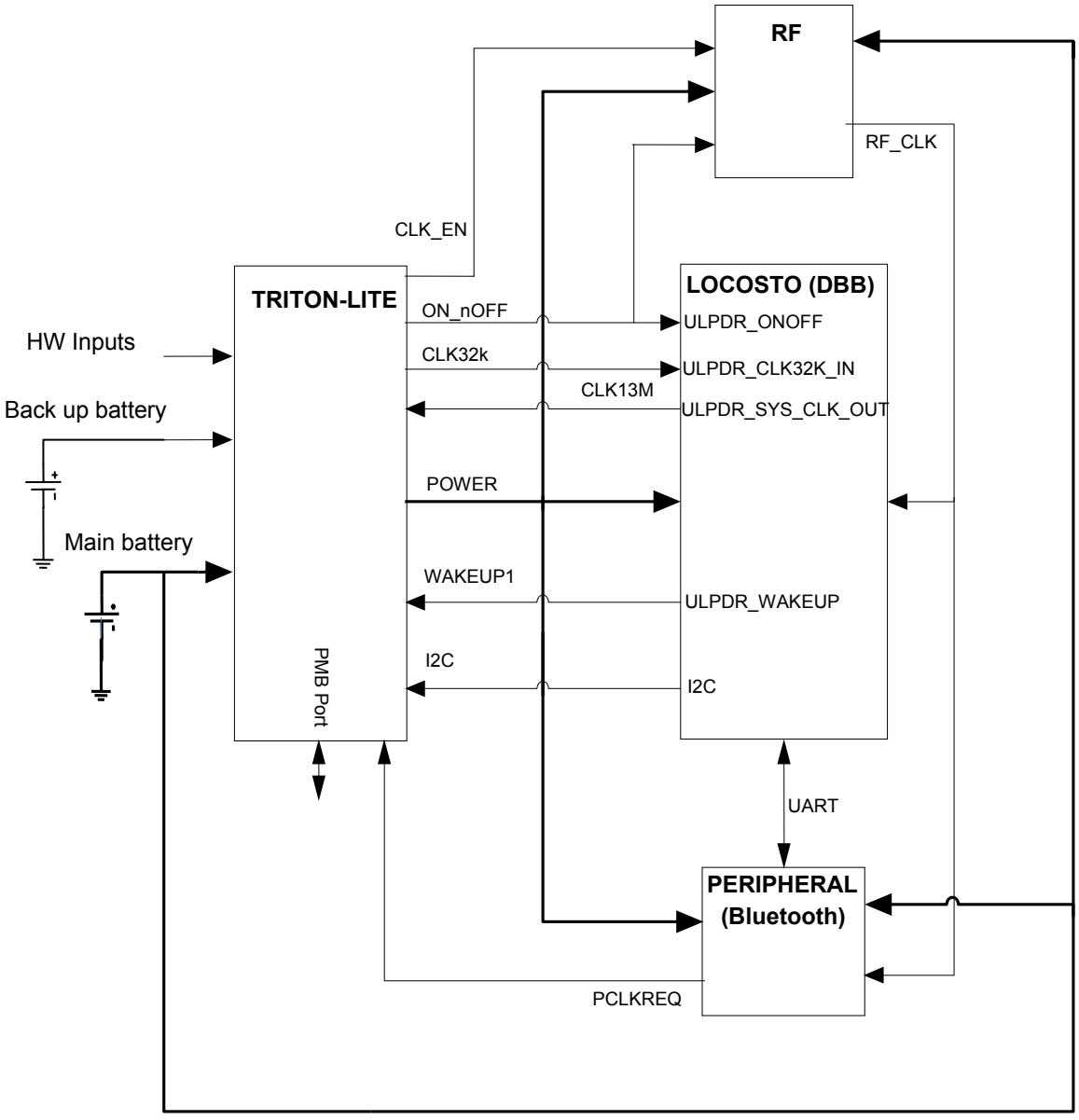


Figure 29 : Power Management Schematic

11.2 SIGNALS PLAYING A ROLE IN SYSTEM POWER STATES CHANGES

The P1,P2,P3 subsystems have got three states, OFF, ACTIVE, SLEEP.
The global system has got two states SUPPLY, BACKUP linked at the voltage of the batteries.
In the NO SUPPLY state, the system isn't powered by any battery.
In the BACKUP state, the system is powered only with the backup battery, it maintains only the VRRTC supply.
In the OFF state, the P1,P2,P3 subsystem is powered by the main battery, it maintains only the VRRTC supply, it is able to accept the power state change global hardware requests.
In the ACTIVE state, the P1,P2,P3 subsystem is powered by the main battery, the selected supplies are enabled in full consumption.
In the SLEEP state, the P1,P2,P3 subsystem is powered by the main battery, the selected supplies are enabled but in low consumption.
The P1,P2,P3 states can differ
SW inputs : the software inputs are only valid when the P1 subsystem is in the ACTIVE state. The 3.2 V main battery comparator and the main battery presence comparator can be enabled or disabled to check a valid Off to Active transition.

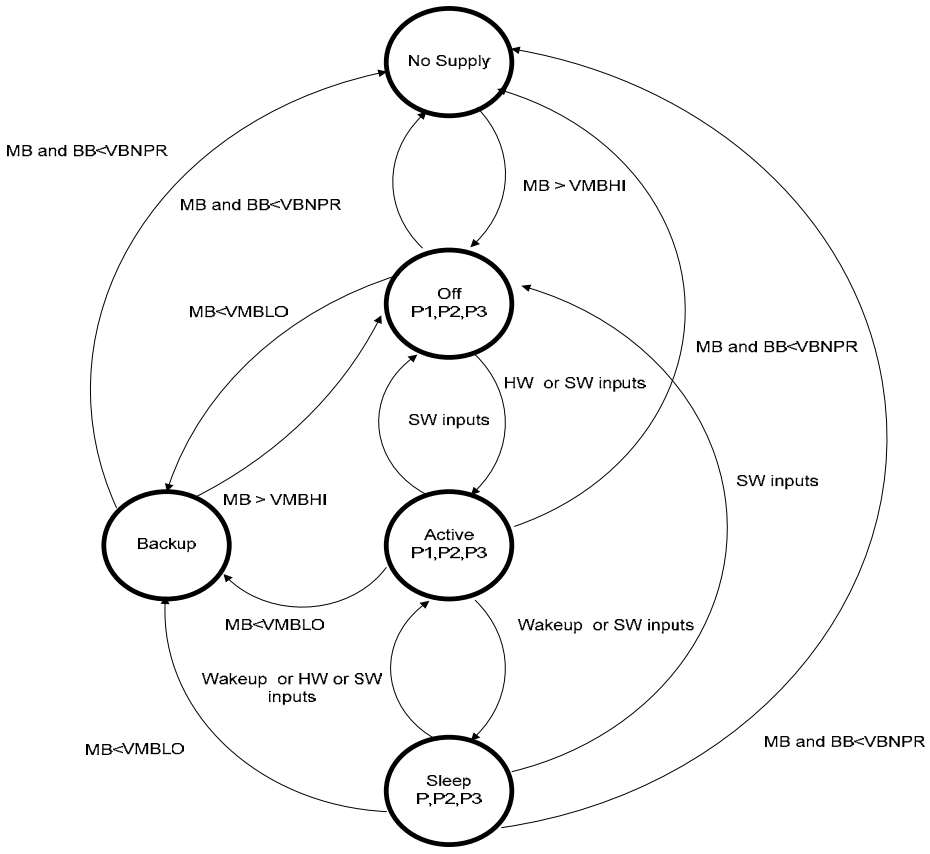


Figure 30 : P1,P2,P3 Power Management State Machines

Transition	PWON_N	RPWON_N	CHG	USB	RTC ALARM	WAKE UP1	WAKE UP2	WAKE UP3
P1_all to off	-	-	-	-	-	-	-	-
P1_off to act	-/0	-/0/E	-/1	-/1	-/R	-	-	-
P1_slp to act	-/0	-/0/E	-/1	-/1	-/R	R/1	-	-
P1_act to slp	-	-	-	-	-	-/0	-	-
P2_all to off	-	-	-	-	-	-	-	-
P2_off to act	-/0	-/0/E	-/1	-/1	-/R	-	-	-
P2_slp to act	-/0	-/0/E	-/1	-/1	-/R	-	R/1	-
P2_act to slp	-	-	-	-	-	-	-/0	-
P3_all to off	-	-	-	-	-	-	-	-
P3_off to act	-/0	-/0/E	-/1	-/1	-/R	-	-	-
P3_slp to act	-/0	-/0/E	-/1	-/1	-/R	-	-	R/1
P3_act to slp	-	-	-	-	-	-	-	-/0

Transition	P1_ DEVOFF	P1_ DEVSLP	P1_ DEVACT	P2_ DEVOFF	P2_ DEVSLP	P2_ DEVACT	P3_ DEVOFF	P3_ DEVSLP	P3_ DEVACT
P1_all to off	R	-	-	-	-	-	-	-	-
P1_off to act	-	-	R	-	-	-	-	-	-
P1_slp to act	-	-	R	-	-	-	-	-	-
P1_act to slp	-	R	-	-	-	-	-	-	-
P2_all to off	-	-	-	R	-	-	-	-	-
P2_off to act	-	-	-	-	-	R	-	-	-
P2_slp to act	-	-	-	-	-	R	-	-	-
P2_act to slp	-	-	-	-	R	-	-	-	-
P3_all to off	-	-	-	-	-	-	R	-	-
P3_off to act	-	-	-	-	-	-	-	-	R
P3_slp to act	-	-	-	-	-	-	-	-	R
P3_act to slp	-	-	-	-	-	-	-	R	-

	Functionnality depends on registers bit
R	Rising Edge sensitivity
F	Falling Edge sensitivity
E	Rising or Falling Edge sensitivity
0	Level sensitivity – Active on low level
1	Level sensitivity – Active on high level
-	No effect

Table 45 : Edge/level Sensitivity of the Power Management Input Signals

11.3 THE POWER MANAGEMENT STATE MACHINE

The FSM input block allows the control and the configuration of the inputs for the three States change generator blocks. The main task of this block consists re-synchronizing the state change requests on the 32 kHz clock. Its outputs are sent to each States change generator block to start the power states transitions.

The States change generator blocks map the state change request to sequencers generating the appropriate state transition commands. It allows the association of a power state change request to a subsystem. The outputs of these blocks are under the format of four commands

OFF to ACTIVE
ACTIVE to OFF
ACTIVE to SLEEEP
SLEEP to ACTIVE

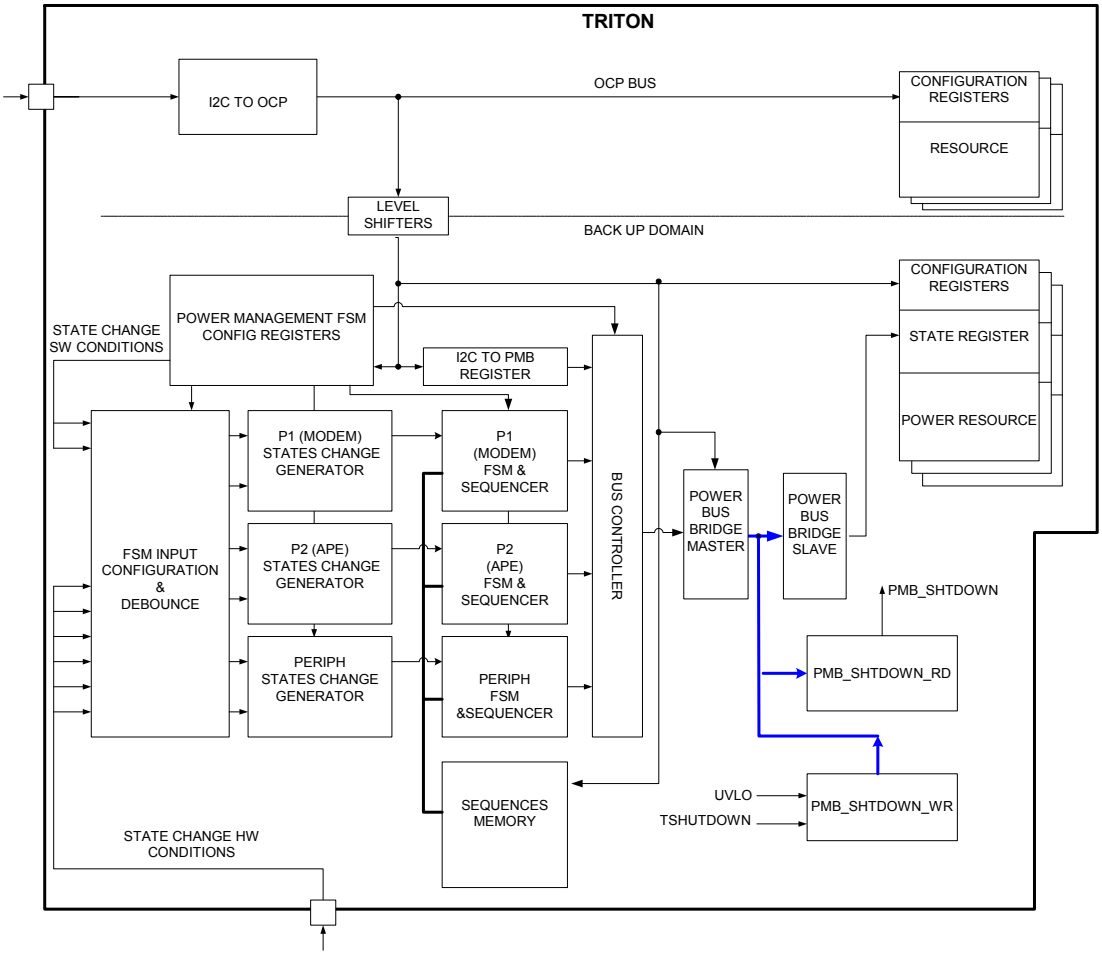


Figure 31 : Power Management Block Diagram

The FSM & sequencer blocks provide the required power sequence by the states change generator blocks. The sequencer fetches instructions from the sequences memory.

- It extracts the delay to insert before generating the power broadcast message to the power management bus controller
- It extracts the address of the next instruction
- It sends the power broadcast message to the PMB controller adding the associated device group information
- Waits for the delay to be terminated
- It jumps to the next instruction

The three sequencers run in parallel, in case of identical addresses , a parallel access to the same memory location is allowed for all sequencers.

The switch on (OFF to ATIVE) and switch off (ALL to OFF) transitions are executed synchronously for all the subsystems in the case of a allowed system. This is possible thanks to the synchronization capability of all the sequencers by default enabled at boot.

Modem			Application			Peripherals			State	Comments
OFF	SLEEP	ACTIVE	OFF	SLEEP	ACTIVE	OFF	SLEEP	ACTIVE		
■			■			■			Off	Allowed
■			■				■		peripheral idle	not allowed
■			■					■	Peripheral active	not allowed
■				■		■			Wait appli	not allowed
■				■			■		Wait appli	not allowed
■				■				■	Wait appli + Periph activity	not allowed
■					■	■			Application running	not allowed
■					■		■		Application running	not allowed
■					■			■	Application running + Peripheral activity	not allowed
	■		■			■			Modem paging	not allowed
	■		■				■		Modem paging + peripheral idle	not allowed
	■		■					■	Modem paging + peripheral active	not allowed
	■			■		■			Mobile paging, application wait	fail safe IO
	■			■			■		Mobile paging, application wait and peripheral idle	Allowed
	■			■				■	Modem paging application wait and peripheral active	Allowed
	■				■	■			Modem paging application active	fail safe IO
	■				■		■		Modem paging application active peripheral idle	allowed
	■				■			■	Modem paging application active peripheral active	allowed
		■	■			■			Modem active	not allowed
		■	■				■		Modem active peripheral idle	not allowed
		■	■					■	Modem active peripheral active	not allowed
		■		■		■			Modem active application wait	fail safe IO
		■		■			■		Modem active, application wait peripheral idle	allowed
		■		■				■	Modem active application wait peripheral active	allowed
		■			■	■			Modem active application active	fail safe IO
		■			■		■		Modem active application active peripheral idle	allowed
		■			■			■	All active	Allowed

Table 46 : System Configurations

When several transition requests occur at the same time, the sequencers have to define priority. Here are the rules to apply for each sequencer.

Filter 1	Rules	
	1	Clear the condition that occurs a transition, as soon as coming out of a stable state

Filter 2	Rules		**Priority**
	1	In ACTIVE clear couple (act to slp & slp to act when true together)	1 – Highest
	2	Priority is 1-OFF 2-ACTIVE 3-SLEEP	2
	3	Clear transitions that go in same state	3 – Lowest
	4	In SLEEP : all off to act condition are cleared	1 – Highest
	5	In OFF : clear all act to slp or slp to act	1 – Highest
	6	In OFF : clear all to off if off to act is set	1 – Highest

Example

	ACTIVE				FILTER conditions				NEXT	Rules
	Off to act	All to off	Act to slp	Slp to act		Off to act	All to off	Act to slp	Slp to act		
	0	0	0	0		0	0	0	0	ACTIVE	
	0	0	0	1		0	0	0	0	ACTIVE	3
	0	0	1	0		0	0	1	0	ACTIVE to SLEEP	
	0	0	1	1		0	0	0	0	ACTIVE	1
	0	1	0	0		0	1	0	0	ACTIVE to OFF	
	0	1	0	1		0	1	0	0	ACTIVE to OFF	2
=>	0	1	1	0	=>	0	1	0	0	ACTIVE to OFF	2
	0	1	1	1		0	1	0	0	ACTIVE to OFF	1
	1	0	0	0		0	0	0	0	ACTIVE	3
	1	0	0	1		0	0	0	0	ACTIVE	3
	1	0	1	0		0	0	1	0	ACTIVE to SLEEP	3
	1	0	1	1		0	0	0	0	ACTIVE	1,3
	1	1	0	0		0	1	0	0	ACTIVE to OFF	2
	1	1	0	1		0	1	0	0	ACTIVE to OFF	3
	1	1	1	0		0	1	0	0	ACTIVE to OFF	2,3
	1	1	1	1		0	1	0	0	ACTIVE to OFF	1,3

Table 47 : Transition Rules

The power transition sequences are hard-coded in ROM

The bus controller arbitrates the three sequencers toward the power bus interface

- It associates to each sequencer the header of the belonging device group
- It checks the inputs coming from the three sequencers and in case of parallel access generates a single power broadcast message
- It grants a priority to the three sequencers through a mechanism of turning listening windows associated to each sequencer.

The power management FSM configuration registers allow the configuration of the T3031 power management

11.4 POWER RESOURCES

In a complex system including a modem processor P1, an application processor P2 and some peripherals P3, the power resources need to be shared in order to achieve the most efficient power supply scheme avoiding redundancies.
The power resources of T3031 are the power providers PP, the power references PR and the power reset and control RC.
In the T3031 case the power resources of T3031 are shared between P1, P2, P3 at the reset as described in the following table
The values for RES_GRP and RES_TYP are hard coded

TRITON-LITE			
	DEV_GRP	RES_GRP	RES_TYP
VRPLL	P1 (1)	PP (1)	5(PWR_CORE_2ND)
VREXTL	P1 (1)	PP (1)	5(PWR_CORE_2ND)
VRMEM	P1 (1)	PP (1)	7(PWR_LDO_PRI)
VRABB	P1 (1)	PP (1)	7(PWR_LDO_PRI)
EXT_REGEN	P3 (4)	PP (1)	7(PWR_LDO_PRI)
VREXTH	P1 (1)	PP (1)	10(PWR_LDO_2ND)
VRIO	P1/P3 (5)	PP (1)	10(PWR_LDO_2ND)
VRSIM	NONE	PP (1)	16(SW_LDO)
VRMMC	NONE	PP (1)	16(SW_LDO)
VRUSB	NONE	PP (1)	16(SW_LDO)
LBG Voltage Reference	P1/P2/P3 (7)	PR (4)	2
MBG Voltage Reference	P1/P2/P3 (7)	PR (4)	3
Bias Current	P1/P2/P3 (7)	PR (4)	4
Comparator BAT32	P1/P2/P3 (7)	PR (4)	25
TH Shutdown	P1/P2/P3 (7)	PR (4)	6
STATE_MNGT	P1/P2/P3 (7)	RC (2)	26
CLK_EN	P1/P3 (5)	RC (2)	27
SLEEP_MNGT	P1 (1)	RC (2)	26
TR_PRE	P1/P2/P3 (7)	PR (4)	30
BAT_PRES_CHECK	P1/P2/P3 (7)	PR (4)	25

Table 48 : T3031 Power Resources

Each resource can be remapped to belong to different device groups.

The SW controlled resources are not controlled by a power up sequence but by programming the resource configuration register, T3031 resources belonging to this type are VRMMC, VRSIM, VRUSB, and VRWLED.

The enable of the system clock function, in T3031 it is associated to the CLK_EN output signal on the VRIO power domain.

STATE_MNGT manages the generation of the system reset signal associated to the output pin ON_nOFF and of the internal information of SLEEP mode to be propagated to the chip's modules.

Comparator BAT32 provides to T3031 information about 3.2V battery state for the valid switch on battery threshold.

Bias current provides the reference current for all the T3031 blocks.
LBG provides the voltage reference to all the blocks need to be active in OFF mode as the backup battery charge block.
MBG provides the reference voltage for all the T3031 power suppliers.

Thermal shutdown manages the enable of the thermal shutdown security feature.

TR_PRE allows the emission of a broadcast message to the system indicating the T3031 presence.

BAT_PRES_CHECK manages the main battery presence check.

Two types of registers are associated to the power resources:

- Configuration registers
- State register

DEV_GRP[2:0]	Device group identification: This field indicates to which group of devices is associated the power resource.(All, Modem, Application, Peripherals).This field is used by the resource to decode the power bus commands.
SLEEP_STATE[3:0]	This bits field indicates the state to be taken by the resource in case of a system SLEEP transition.
OFF_STATE[3:0]	This bits field indicates the state to be taken by the resource in case of a system OFF transition.
RES_STATE[3:0]	This field indicates the current state of the resource, it is a read only field
RES_ID[7:0]	This field indicates the resource identificator. Each resource has associated at reset a different identificator, nevertheless this field could be modified by SW to provide the flexibility of differentiating identical devices by I2C access. This unique ID has to be shared among all the system resources there is a special coding rule that has to be followed at design level to choose the initial reset value for those fields: The RES_ID can be considered as composed by a CLUSTER_ID field and a RES_NUMB field. RES_NUMB is hard-coded and unique to each resource, the CLUSTER_ID can be programmable in some of its bits locations: In the T3031 case 2x16 resources clusters has been adopted and the RES_ID field of each resource is 0 0 0 0 x x x x or 0 0 1 0 x x x x. bit 6 and 5 programmable
RES_DEDICATED1[6:0]	This bits field is dedicated to the specific configuration of the resource

Table 49 : Resource Registers

11.5 THE POWER MANAGEMENT BUS

The Power Management Bus PMB is implemented as a standard SPI interface, PMB messages may have four main different formats. Three out of the four are based on a synchronous mono-master SPI protocol (clock,data,enable) with a data length variable between 16 and 32 bits. The fourth is totally asynchronous and allows multi-master messages.

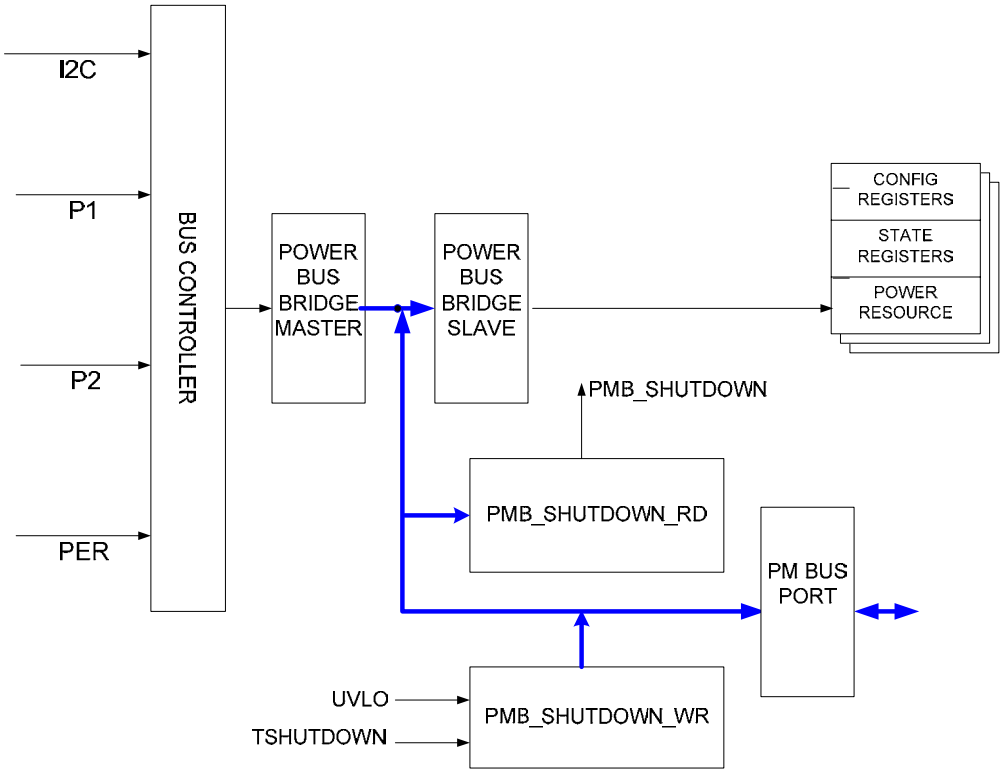


Figure 32 : Power Management Bus Block Diagram

Broadcast messages 16 bits

All the power resources connected on the PMB will decode this message accordingly to their DEV_GRP, RES_GRP and RES_TYP fields'configuration. Broadcast messages are discriminated by singular messages through the value assumed by the MT bit. Generally the broadcast messages are issued by the sequencers P1,P2,P3. Nevertheless the application SW has the capability of writing a broadcast message through the I2C to PMB bridge.

MSB

DEV_GRP[2:0]	MT	RES_GRP[2:0]	RES_TYP[4:0]	RES_STATE[3:0]

DEV_GRP[2:0]	Device group broadcast address: This field indicates to which device group (sub-system) is directed the power bus message. Each Power resource is associated to one of those groups 000 = Other (data cargo) 001 = Modem group (processor1) 010 = Application group (processor2) 100 = Peripheral group 011 = Processor1 & Processor2 101 = Peripherals & Processor1 110 = Peripherals & Processor 2 111 = All device groups
MT	Message Type 0=Singular, 1=Broadcast. **[1]**
RES_GRP[2:0]	Resource group: This field indicates, among the groups indicated by DEV_GRP field, which group of power resource is addressed. 000 = Reserved for further use 001 = Power provider 010 = Reset and control 100 = Power Reference 011 = Power Provider and Reset and Control 101 = Power Provider and Power Reference 110 = Reset and control and Power Reference 111 = All resources groups
RES_TYP[4:0]	Resource group: This field indicates which specific power resource is addressed. Up to a maximum of 30 different resource types per resource group could be addressed by broadcast messages. 00000 = Reserved 00001 = Resource1 ……. 11110 = Resource30 11111 = All
RES_STATE[3:0]	State to be assumed by the addressed power resource 1110 = ACTIVE …... 0000 = OFF

Table 50 : Broadcast Messages

Singular messages 16 bits

The singular messages are usually issued by a processor through the I2C to PMB bridge.

DEV_GRP[2:0]	MT	RES_ID[7:0]	RES_STATE[3:0]

DEV_GRP[2:0]	Device group broadcast address: This field indicates to which device group is directed the power bus message. Each Power resource is associated to one of those groups 000 = Other (data cargo) 001 = Modem group (processor1) 010 = Application group (processor2) 100 = Peripheral group 011 = Processor1 & Processor2 101 = Peripherals & Processor1 110 = Peripherals & Processor 2 111 = All device groups
MT	Message Type 0=Singular, 1=Broadcast **[0]**
RES_ID[7:0]	Resource id: This field indicates, the identification number of the resource Up to 256 singular resources can be addressed.
RES_STATE[3:0]	State to be assumed by the addresses power resource 1110 = ACTIVE ……. 0000 = OFF

Table 51 : Single Messages

Data transfer 16 to 32 bits

The 16 LSB data are sent first, then the 16 MSB data.

DEV_GRP[2:0]	DATA28..0]

DEV_GRP[2:0]	Code corresponding to a data transfer through power bus (this options is mainly used for test and debug purposes) **[000]**
DATA[28:0]	Data cargo

Table 52 : Data Transfer

In a complex system other external chips could implement circuitry detecting emergency conditions such as the low battery condition UVLO or the overheating of the device TSHUTDOWN.Those emergency conditions have to be propaged to the rest of the system and induce actions on the power management resources. The PMB is the appropriate vehicle for those kinds of emergency messages.
The PMB_SHUTDOWN_WR block has the capability of asynchronously forcing the system shutdown command.. The PMB_SHUTDOWN_RD block read the PMB status and generates a shutdown command whether a shutdown condition is detected on the PMB. Each device managed through the PMB integrates those two blocks. The detected shutdown condition forces a reset and an OFF state on all power resources managed by the PMB.

At the first power up the shutdown condition is presented on the PMB in order to reset all the devices connected on the bus, all resources are forced to their OFF state with a default configuration. The PMB is in the IDLE condition waiting for messages to be transmitted and listening for other device shutdown messages. The delay between two consecutive PMB messages is programmable and can assume two values, 1 period of 32 kHz clock (default) or 6 periods of 32 kHz clock. The PM_C behavior is also configurable , PM_C can be a free running clock (default) or valid for the length of the transmission plus 3/15/31 periods after the PM_F rise. In order to avoid generation of spurious

PMB_SHUTDOWN conditions on the bus at transmit time, data on the PM_D signal must be output only when the PM_F signal is already at the low logical level. For the same reason at the end of the transmission the PM_D signal has to be to the high logical level before PM_F signal.

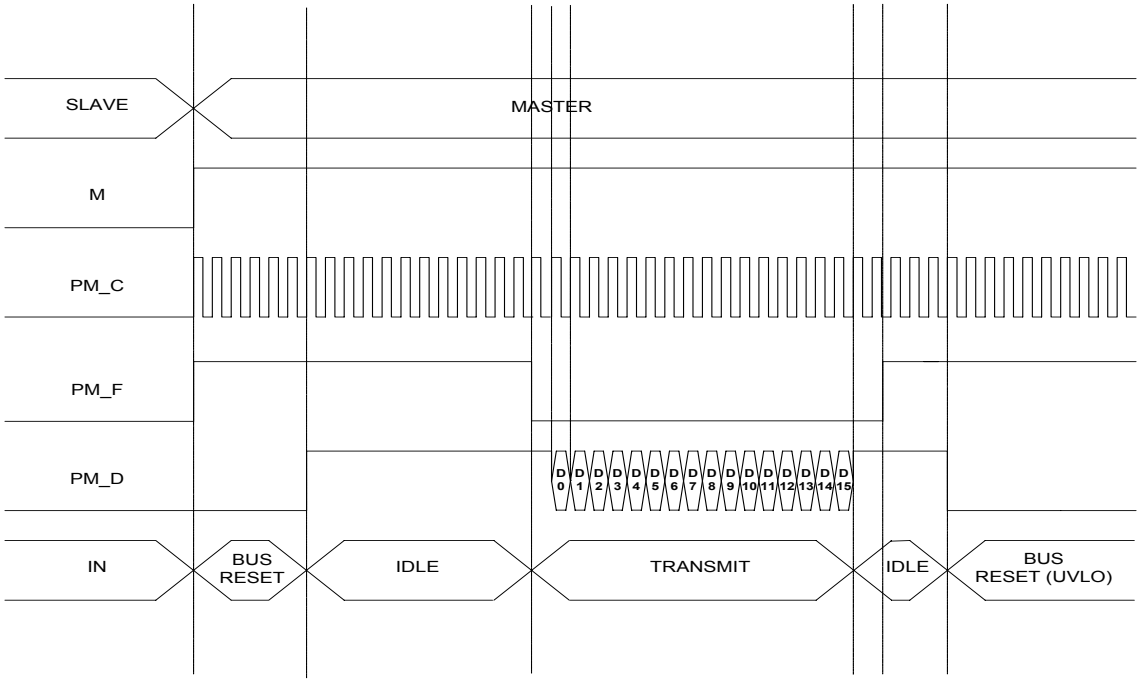


Figure 33 : Serial Transmission of the Power Management Bus

The registers in T3031 can be set or reset by four kind of reset

The reset_tst has the highest priority and is generated by the input TESTRESET.
The reset_por has the second highest priority and is generated by :
- either an internal VRRTC comparator
- or pressing the power on key more than 8.2s

The reset_bck has the third highest priority and is generated by the PMB_SHUTDOWN output.
The reset_off has the lowest priority and is generated by the ON_nOFF output.

reset_por = (low battery AND low back-up) OR (manual PWON press for 8.2s)
reset_bck = (low battery) OR (thermal shutdown)

State / Reset Type	No Supply state	Backup state	Off state	Active state
Reset_off	Applied	Applied	Applied	-
Reset_bck	Applied	Applied	-	-
Reset_por	Applied	-	-	-
Reset_tst	-	Only applied in HW event on testreset input		

Table 53 : Types of Reset

11.6 POWER MANAGEMENT PROGRAMMING MODEL

A power state transition can be seen as a sequence of severals steps. Each step corresponding to a specific power resource type enabled or disabled.
The system resources are of three kinds PR, RC and PP. Each power transition sequence could be considered as the appropriate concatenation of the three resources groups as illustrated in the diagram.

PP: Power providers
PR: Power references
RC: Reset and control

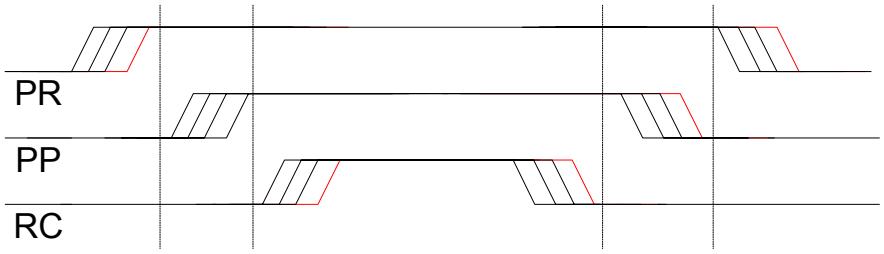


Figure 34 : Power Resources Sequencing

The sequences will remain valid only if the system will not enter in the NO SUPPLY state. In this case the adopted sequences will be the default ones.

		OFF 2 ON SEQUENCE	DIVISOR	TIMER	DELAY (ms)
step	0	Indicate to PMB resource Triton-Lite presence	0	6	0.794
step	1	Enable first level of battery check (Triton-Lite 2.8V comp ACTIVE, LBG ACTIVE)	0	4	0.58
step	2	Enable reference voltage (Triton-Lite MBG in ACTIVE_FAST mode)	2	1	3.48
step	3	Enable reference current (Triton-Lite Bias block in ACTIVE mode)	0	2	0.58
step	4	Enable second level of battery check (Triton-Lite BAT_PRES_CHECK and BAT32 comparator)	1	2	1.526
step	5	Enable Triton-Lite mode in External Power resources	1	6	2.502
step	6	Enable Triton-Lite VREXTL,VRPLL + Enable External Power resources IO's DCDC	1	6	2.502
step	7	Enable Primary LDO's (Triton-Lite VRMEM, VRABB, REGEN + External Power resources)	1	0	1.038
step	8	Enable Secondary LDO's (Triton-Lite VREXTH, VRIO + External Power resources) step A	1	0	1.038
step	9	Enable Secondary LDO's (External Power resources) step B (1)	1	0	1.038
step	10	ACTIVE state Broadcast for all PP	1	4	2.014
step	11	PR ACTIVE broadcast (Triton-Lite MBG in ACTIVE accurate mode, BAT32 OFF, BAT_PRES_CHECK OFF)	2	4	4.944
step	12	State management ACTIVE (Triton-Lite release the ON_nOFF and its internal reset)	0	1	0.58
step	13	Clock management ENABLE (Triton-Lite enable the clock function CLK_EN high)	0	1	0.58
step	14	ACTIVE state Broadcast for all subsystems	0	1	0.58

(1) At this moment a dedicated logic will enable level shifter between VRIO and VRRTC allowing the 32K generation on the VRIO domain

Table 54 : Default OFF to ACTIVE Sequence

		ON TO OFF SEQUENCE	DIVISOR	TIMER	DELAY (ms)
step	1	Clock management DISABLE (Triton-Lite disable the clock function, CLK_EN low)	0	1	0.58
step	2	System Reset (Triton-Lite force ON_nOFF and its internal reset to its active states)	0	1	0.58
step	3	OFF state Broadcast for all subsystems	0	1	0.58

Table 55 : Default ACTIVE to OFF Sequence

		ACTIVE to SLEEP sequence	DIVISOR	TIMER	DELAY (ms)
step	1	Clock management DISABLE (Triton-Lite disable the clock function, CLK_EN low)	0	1	0.58
step	2	SLEEP BROADCAST for PP	0	1	0.58
step	3	SLEEP BROADCAST for PR	0	1	0.58
step	4	SLEEP state Broadcast for all subsystems	0	1	0.58

Table 56 : Default ACTIVE to SLEEP Sequence

		SLEEP to ACTIVE SEQUENCE	DIVISOR	TIMER	DELAY (ms)
step	1	WAKEUP BROADCAST for PR	0	4	0.58
step	2	ACTIVE BROADCAST for PP	1	2	1.526
step	3	ACTIVE state Broadcast for all subsystems	0	1	0.58

Table 57 : Default SLEEP to ACTIVE Sequence

RES_STATE	LDO's	REGEN	DC/DC	MBG	BAT_PRES_CHECK	TR_PRE	LBG	BAT32	BIAS	TH_SHUT	SLEEP_MNGT	STATE_MNGT	CLK_EN
1111(15) BOOT	ACTIVE	ACTIVE	ACTIVE	ON FAST	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1110(14) ACTIVE	ACTIVE	ACTIVE	ACTIVE	ON ACCURATE	OFF	ACTIVE	ACTIVE	OFF	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1101(13)	ACTIVE	ACTIVE	ACTIVE	ON ACCURATE	OFF	ACTIVE	ACTIVE	OFF	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1100(12)	ACTIVE	ACTIVE	ACTIVE	ON ACCURATE	OFF	ACTIVE	ACTIVE	OFF	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1011(11) WAKEUP	ACTIVE	ACTIVE	ACTIVE	ON FAST	OFF	ACTIVE	ACTIVE	OFF	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1010(10)	ACTIVE	ACTIVE	ACTIVE	ON FAST	OFF	ACTIVE	ACTIVE	OFF	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1001(9)	ACTIVE	ACTIVE	ACTIVE	ON FAST	OFF	ACTIVE	ACTIVE	OFF	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1000(8) SLEEP	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0111(7)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0110(6)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0101(5)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0100(4)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0011(3)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0010(2)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0001(1)	SLEEP	SLEEP	SLEEP	SLEEP	OFF	ACTIVE	ACTIVE	OFF	SLEEP	SLEEP	SLEEP	SLEEP	SLEEP
0000(0) OFF	OFF	OFF	OFF	OFF	OFF	ACTIVE	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Power Providers
Reset and Control
Power Reference

Table 58 : RES_STATE multi states

OFF to ACTIVE 15 steps

	DEV_GRP	MT	RES_GRP	RES_TYP	RES_STATE
Step01 F9EF	111	1	100	11110	1111
Step02 F82F	111	1	100	00010	1111
Step03 F83F	111	1	100	00011	1111
Step04 F84F	111	1	100	00100	1111
Step05 F99F	111	1	100	11001	1111
Step06 F21E	111	1	001	00001	1110
Step07 F25E	111	1	001	00101	1110
Step08 F27E	111	1	001	00111	1110
Step09 F2AE	111	1	001	01010	1110
Step10 F2BE	111	1	001	01011	1110
Step11 F3FE	111	1	001	11111	1110
Step12 F9FE	111	1	100	11111	1110
Step13 F5AE	111	1	010	11010	1110
Step14 F5BE	111	1	010	11011	1110
Step15 FFFE	111	1	111	11111	1110

ACTIVE to OFF 3 steps

	DEV_GRP	MT	RES_GRP	RES_TYP	RES_STATE
Step01 F5B0	111	1	010	11011	0000
Step02 F5A0	111	1	010	11010	0000
Step03 FFF0	111	1	111	11111	0000

ACTIVE to SLEEP 4 steps

	DEV_GRP	MT	RES_GRP	RES_TYP	RES_STATE
Step01 F5B8	111	1	010	11011	1000
Step02 F3F8	111	1	001	11111	1000
Step03 F9F8	111	1	100	11111	1000
Step04 FFF8	111	1	111	11111	1000

SLEEP to ACTIVE 3 steps

	DEV_GRP	MT	RES_GRP	RES_TYP	RES_STATE
Step01 F9FB	111	1	100	11111	1011
Step02 F3FE	111	1	001	11111	1110
Step03 FFFE	111	1	111	11111	1110

Table 59 : Power bus words for standard sequences

11.7 MASTER REGISTERS

11.7.1 CFG_PU_PD_MSB

Register	CFG_PU_PD_MSB							
Page	1	Address	Dec # 24	Hex 0x18				
Bit	7	6	5	4	3	2	1	0
Name	CPWON PU7VZ	CRPWON PU7VZ	CHSDET PU7VZ	CWAKEUP2 PD	CWAKEUP1 PD	CPCLKREQ PD	RSRVD	CMCLK1 PD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset_por	0	0	0	1	0	1	0	0

Register bits description

CPWONPU7VZ	Pull-Up (active low) of PWON pin
CRPWONPU7VZ	Pull-Up (active low) of RPWON pin
CHSDETPU7VZ	Pull-Up (active low) of HSDET pin
CWAKEUP2PD	Pull-Down (active high) of WAKEUP2 pin
CWAKEUP1PD	Pull-Down (active high) of WAKEUP1 pin
CPCLKREQPD	Pull-Down (active high) of PCLKREQ pin
RSRVD (bit 1)	Reserved bit
CMCLK1PD	Pull-Down (active high) of MCLK1 pin

11.7.2 CFG_PU_PD_LSB

Register	CFG_PU_PD_LSB							
Page	1	Address	Dec # 25	Hex 0x19				
Bit	7	6	5	4	3	2	1	0
Name	CTCK PD	CTMS PUZ	CTDI PUZ	COEINTN PD	CDATVPRXD PD	CSE0VMTXD PD	RSRVD	CPM PUZ
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset_por	1	0	0	0	0	0	0	0

Register bits description

CTCKPD	Pull-Down (active high) of TCK pin
CTMSPUZ	Pull-Up (active low) of TMS pin
CTDIPUZ	Pull-Up (active low) of TDI pin
COEINTNPD	Pull-Down (active high) of OE_INTN pin
CDATVPRXDPD	Pull-Down (active high) of DAT_VP_RXD pin
CSE0VMTXDPD	Pull-Down (active high) of SE0_VM_TXD pin
RSRVD (bit 1)	Reserved bit
CPMPUZ	Pull-Up (active low) of PM_D and PM_F pins

11.7.3 P1_CFG_TRANSITION

Register	P1_CFG_TRANSITION							
Page	1 Address	Dec # 26	Hex 0x1A					
Bit	7	6	5	4	3	2	1	0
Name	P1_LVL_WAKEUP	Not Used	Not Used	P1_MSK_ RTC	P1_MSK _USB	P1_MSK _CHG	P1_MSK _RPWON	P1_MSK _PWON
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset_off	0	-	-	-	-	-	-	-
Reset_por	0	0	0	1	1	1	1	1

Register bits description

P1_LVL_WAKEUP	When '0' : WAKEUP1 rising edge affects P1_SLP2ACT transition When WAKEUP1 = '0' : does not affects P1_ACT2SLP transition When '1' : WAKEUP1 active on level When WAKEUP1 = '0' : P1_ACT2SLP transition occurs When WAKEUP1 = '1' : P1_SLP2ACT transition occurs
P1_MSK_RTC	When '0' : RTC does not affect P1_OFF2ACT or P1_SLP2ACT transition When '1' : RTC does affect P1_OFF2ACT or P1_SLP2ACT transition
P1_MSK_USB	When '0' : USB does not affect P1_OFF2ACT or P1_SLP2ACT transition When '1' : USB does affect P1_OFF2ACT or P1_SLP2ACT transition
P1_MSK_CHG	When '0' : CHG does not affect P1_OFF2ACT or P1_SLP2ACT transition When '1' : CHG does affect P1_OFF2ACT or P1_SLP2ACT transition
P1_MSK_RPWON	When '0' : RPWON does not affect P1_OFF2ACT or P1_SLP2ACT transition When '1' : RPWON does affect P1_OFF2ACT or P1_SLP2ACT transition
P1_MSK_PWON	When '0' : PWON does not affect P1_OFF2ACT or P1_SLP2ACT transition When '1' : PWON does affect P1_OFF2ACT or P1_SLP2ACT transition

11.7.4 P2_CFG_TRANSITION

Register	P2_CFG_TRANSITION							
Page	1 Address	Dec # 27	Hex 0x1B					
Bit	7	6	5	4	3	2	1	0
Name	P2_LVL_WAKEUP	Not Used	Not Used	P2_MSK_ RTC	P2_MSK _USB	P2_MSK _CHG	P2_MSK _RPWON	P2_MSK _PWON
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset_off	0	-	-	-	-	-	-	-
Reset_por	0	0	0	1	1	1	1	1

Register bits description

P2_LVL_WAKEUP	When '0' : WAKEUP2 rising edge affects P2_SLP2ACT transition When WAKEUP2 = '0' : does not affects P2_ACT2SLP transition When '1' : WAKEUP2 active on level When WAKEUP2 = '0' : P2_ACT2SLP transition occurs When WAKEUP2 = '1' : P2_SLP2ACT transition occurs
P2_MSK_RTC	When '0' : RTC does not affect P2_OFF2ACT or P2_SLP2ACT transition When '1' : RTC does affect P2_OFF2ACT or P2_SLP2ACT transition
P2_MSK_USB	When '0' : USB does not affect P2_OFF2ACT or P2_SLP2ACT transition When '1' : USB does affect P2_OFF2ACT or P2_SLP2ACT transition
P2_MSK_CHG	When '0' : CHG does not affect P2_OFF2ACT or P2_SLP2ACT transition When '1' : CHG does affect P2_OFF2ACT or P2_SLP2ACT transition
P2_MSK_RPWON	When '0' : RPWON does not affect P2_OFF2ACT or P2_SLP2ACT transition When '1' : R PWON does affect P2_OFF2ACT or P2_SLP2ACT transition
P2_MSK_PWON	When '0' : PWON does not affect P2_OFF2ACT or P2_SLP2ACT transition When '1' : PWON does affect P2_OFF2ACT or P2_SLP2ACT transition

11.7.5 P3_CFG_TRANSITION

Register	P3_CFG_TRANSITION							
Page	1 Address	Dec # 28	Hex 0x1C					
Bit	7	6	5	4	3	2	1	0
Name	P3_LVL_WAKEUP	Not Used	Not Used	P3_MSK_ RTC	P3_MSK _USB	P3_MSK _CHG	P3_MSK _RPWON	P3_MSK _PWON
Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Reset_off	0	-	-	-	-	-	-	-
Reset_por	0	0	0	1	1	1	1	1

Register bits description

P3_LVL_WAKEUP	When '0' : WAKEUP3 rising edge affects P3_SLP2ACT transition When WAKEUP3 = '0' : does not affects P3_ACT2SLP transition When '1' : WAKEUP3 active on level When WAKEUP3 = '0' : P3_ACT2SLP transition occurs When WAKEUP3 = '1' : P3_SLP2ACT transition occurs
P3_MSK_RTC	When '0' : RTC does not affect P3_OFF2ACT or P3_SLP2ACT transition When '1' : RTC does affect P3_OFF2ACT or P3_SLP2ACT transition
P3_MSK_USB	When '0' : USB does not affect P3_OFF2ACT or P3_SLP2ACT transition When '1' : USB does affect P3_OFF2ACT or P3_SLP2ACT transition
P3_MSK_CHG	When '0' : CHG does not affect P3_OFF2ACT or P3_SLP2ACT transition When '1' : CHG does affect P3_OFF2ACT or P3_SLP2ACT transition
P3_MSK_RPWON	When '0' : RPWON does not affect P3_OFF2ACT or P3_SLP2ACT transition When '1' : RPWON does affect P3_OFF2ACT or P3_SLP2ACT transition
P3_MSK_PWON	When '0' : PWON does not affect P3_OFF2ACT or P3_SLP2ACT transition When '1' : PWON does affect P3_OFF2ACT or P3_SLP2ACT transition

11.7.6 P123_CFG_TRANSITION

Register	P123_CFG_TRANSITION							
Page	1 Address	Dec # 29	Hex 0x1D					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	P123_LVL_RPWON
Read/Write	R	R	R	R	R	R	R	R/W
Reset_por	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 1)	Reserved bits
P123_LVL_RPWON	When 0 ➔ RPWON edge event only affect P[123]_SLP2ACT and P[123]_OFF2ACT When 1 ➔ RPWON active level only affect P[123]_SLP2ACT and P[123]_OFF2ACT

11.7.7 STS_HW_CONDITIONS

Register	STS_HW_CONDITIONS							
Page	1 Address	Dec # 30	Hex 0x1E					
Bit	7	6	5	4	3	2	1	0
Name	STS_ VBATOK	STS_ WAKEUP3	STS_ WAKEUP2	STS_ WAKEUP1	STS_USB	STS_CHG	STS_ RPWON	STS_ PWON
Read/Write	R	R	R	R	R	R	R	R
Reset_por	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Register bits description

STS_VBATOK	Level status of VBATOK comparator, '1' means VBAT is correct (VBAT voltage comparator and VBAT presence checker are ok) STS_VBATOK = (VBAT_CMP or SEQ_MSK_VBAT_CMP) and (VBAT_PRE or SEQ_MSK_VBAT_PRE)
STS_WAKEUP3	Level status of WAKEUP3 pad (active high)
STS_WAKEUP2	Level status of WAKEUP2 pad (active high)
STS_WAKEUP1	Level status of WAKEUP1 pad (active high)
STS_USB	Level status of USB port , '1' means USB is plugged , '0' unplugged
STS_CHG	Level status of CHARGER , '1' means charger is plugged , '0' unplugged
STS_RPWON	Level status of RPWON button (active high) , after debouncing (31.25 ms)
STS_PWON	Level status of PWON button (active high) , after debouncing (31.25 ms)
Note: VBAT_CMP and BAT32 are the same comparator.	

11.7.8 SEQ_P123_STATE

Register	SEQ_P123_STATE							
Page	1	Address	Dec # 31	Hex 0x1F				
Bit	7	6	5	4	3	2	1	0
Name	Not Used	Not Used	SEQ_P3_ STATE_1	SEQ_P3_ STATE_0	SEQ_P2_ STATE_1	SEQ_P2_ STATE_0	SEQ_P1_ STATE_1	SEQ_P1_ STATE_0
Read/Write	R	R	R	R	R	R	R	R
Reset_por	0	0	0	0	0	0	0	0

Register bits description

SEQ_P3_STATE [1:0]	Current state of sequencer P3
SEQ_P2_STATE [1:0]	Current state of sequencer P2
SEQ_P1_STATE [1:0]	Current state of sequencer P1
Note: state are coded as follows: 00 ➔ OFF 11 ➔ ACTIVE 10 ➔ SLEEP 01 ➔ Reserved code	

11.7.9 SEQ_CFG_MODE

Register	SEQ_CFG_MODE							
Page	1	Address	Dec # 32	Hex 0x20				
Bit	7	6	5	4	3	2	1	0
Name	STS_P123 _STATE _STABLE	STS_P1_ STATE _STABLE	STS_P2_ STATE _STABLE	STS_P3_ STATE _STABLE	SEQ_MSK _VBAT _PRE	SEQ_MSK _VBAT _CMP	SEQ_ FREEZE	SEQ_OFF SYNC
Read/Write	R/P	R/P	R/P	R/P	R/W/P	R/W/P	R/W/P	R/W/P
Reset_por	0	0	0	0	0	0	0	1

Register bits description

STS_P123_STATE_STABLE	Status of P123 state machine. 0: A transition is on-going on one of the state machines. 1: No transition is on-going on the state machines.
STS_P1_STATE_STABLE	Status of P1 state machine. 0: A transition is on-going on the state machine. 1: No transition is on-going on the state machine.
STS_P2_STATE_STABLE	Status of P2 state machine. 0: A transition is on-going on the state machine. 1: No transition is on-going on the state machine.

STS_P3_STATE_STABLE	Status of P3 state machine. 0: A transition is on-going on the state machine. 1: No transition is on-going on the state machine.
SEQ_MSK_VBAT_PRE	When 0 : Vbat presence comparator is used to check a valid OFF to ACTIV transition When 1 : Vbat presence comparator is not used to check a valid OFF to ACTIV transition, the comparator status is seen as equal to 1
SEQ_MSK_VBAT_CMP	When 0 : Vbat voltage comparator is used to check a valid OFF to ACTIV transition When 1 : Vbat voltage comparator is not used to check a valid OFF to ACTIV transition, the comparator status is seen as equal to 1
SEQ_FREEZE	Freeze all sequencer in their current state, all sequencer finish its own current transition if one is on going.
SEQ_OFFSYNC	All sequencer wait each other before any - P[123]_ACT2OFF transition Any write in P[123]_DEVOFF write also the value in P[123]_DEVOFF - P[123]_OFF2ACT transition Any switch-on on one sequencer is applied on all sequencer. (Has priority on switch-on mask condition)

11.7.10 PB_CFG

Register	PB_CFG							
Page	1	Address	Dec # 34	Hex 0x22				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	PB_PMF_DLY	PB_CLK_CFG_1	PB_CLK_CFG_0	PB_P123_BW_1	PB_P123_BW_0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	1	1	0	0

Register bits description

RSRVD (bit 7 – bit 5)	Reserved bits
PB_PMF_DLY	When '1' : PMF is kept 6 PMC clock between each Power Bus write Access When '0' : PMF is kept 1 PMC clock between each Power Bus write Access
PB_CLK_CFG [1:0]	00 : PB_CLK is only valid when PB_F=0 and 3 clock pulse after PB_F rise 01 : PB_CLK is only valid when PB_F=0 and 15 clock pulse after PB_F rise 10 : PB_CLK is only valid when PB_F=0 and 31 clock pulse after PB_F rise 11 : PB_CLK is a free running clock
PB_P123_BW [1:0]	00 : P1, P2 , P3 have each band width equity (33% or 25%) 01 : P1 has 50% Power Bus band width, others shared 50% Band width with equity 10 : P2 has 50% Power Bus band width, others shared 50% Band width with equity 11 : P3 has 50% Power Bus band width, others shared 50% Band width with equity

11.7.11 PB_CFG_I2C

Register	PB_CFG_I2C							
Page	1	Address	Dec # 35	Hex 0x23				
Bit	7	6	5	4	3	2	1	0
Name	STS_PB_I2C_BUSY	RSRVD	RSRVD	RSRVD	RSRVD	PB_I2C_LGHT_1	PB_I2C_LGHT_0	PB_I2C_BWEN
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

STS_PB_I2C_BUSY	1 : word PB_I2C_WORD_[ABCD] is queued and has not been send on power bus 0 : buffer empty / ready to send a word on power bus
RSRVD (bit 6 – bit 3)	Reserved bits
PB_I2C_LGHT [1:0]	00 : 16 bits lenght 01 : 24 bits lenght 10 : 32 bits lenght 11 : 32 bits lenght
PB_I2C_BWEN [1:0]	When '0' : I2C has no access on Power Bus When '1' : I2C has access to Power Bus (Reduce Band width for P[123] that have not the 50% band width)

11.7.12 PB_CFG_TEST

Register	PB_CFG_TEST							
Page	1	Address	Dec # 36	Hex 0x24				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	SETUP_ DONE_B	SETUP_ DONE	RSRVD	PB_MASTER_ EXT	PB_MSK_MA STER_AUTO	RSRVD	RSRVD
Read/Write	R	R/W/P	R/W/P	R	R/W/P	R/W/P	R	R
Reset_por	0	0	0	0	0	1	0	0
Reset_bck	-	0	-	-	-	-	-	-

Register bits description

RSRVD (bit 7)	Reserved bit
SETUP_DONE_B	1 : PMC configuration is done 0 : PMC configuration not done
SETUP_DONE	1 : PMC configuration is done 0 : PMC configuration not done
RSRVD (bit 4)	Reserved bit
PB_MASTER_EXT	When PB_MSK_MASTER_AUTO=1 (HW) PB_MASTER is read only PB_MASTER is clear and unlock by internal reset_bck Is lock to 0 if the first PB_F falling edge event is driven by external device Is lock to 1 if the first PB_F falling edge event is driven by T3031 device. This lock to 1 has priority on lock to 0. When PB_MSK_MASTER_AUTO=0 (SW) PB_MASTER is read and write When '0' : Master on Power bus is an external device When '1' : Master on Power bus is T3031 device
PB_MSK_MASTER_AUTO	Select AUTOMATIC (HW) master selection on PowerBus or Software (SW) selection
RSRVD (bit 1 – bit 0)	Reserved bits

11.7.13 PROTECT_PKEY

Register	PROTECT_PKEY							
Page	1	Address	Dec # 45	Hex 0x2D				
Bit	7	6	5	4	3	2	1	0
Name	PKEY_7	PKEY_6	PKEY_5	PKEY_4	PKEY_3	PKEY_2	PKEY_1	PKEY_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

PKEY [7:0]	READ access : Read 0x00 if a no-valid PKEY has been written Read 0x11 if a valid PKEY has been written WRITE access : Write 0xE3 to write a valid PKEY

11.7.14 P1_DEV

Register	P1_DEV							
Page	1	Address	Dec # 48	Hex 0x30				
Bit	7	6	5	4	3	2	1	0
Name	Not Used	Not Used	Not Used	Not Used	Not Used	P1_DEVACT	P1_DEVSLP	P1_DEVOFF
Read/Write	R	R	R	R	R	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

P1_DEVACT	Write '1' will start a P1_OFF2ACT or P1_SLP2ACT transition This bit is clear automatically , one period of CK32K after.
P1_DEVSLP	Write '1' will start a P1_ACT2SLP transition This bit is clear automatically , one period of CK32K after.
P1_DEVOFF	Write '1' will start a P1_ACT2OFF or P1_SLP2OFF transition This bit is clear automatically , one period of CK32K after.

11.7.15 P2_DEV

Register	P2_DEV							
Page	1	Address	Dec # 49	Hex 0x31				
Bit	7	6	5	4	3	2	1	0
Name	Not Used	Not Used	Not Used	Not Used	Not Used	P2_DEVACT	P2_DEVSLP	P2_DEVOFF
Read/Write	R	R	R	R	R	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

P2_DEVACT	Write '1' will start a P2_OFF2ACT or P2_SLP2ACT transition This bit is clear automatically , one period of CK32K after.
P2_DEVSLP	Write '1' will start a P2_ACT2SLP transition This bit is clear automatically , one period of CK32K after.
P2_DEVOFF	Write '1' will start a P2_ACT2OFF or P2_SLP2OFF transition This bit is clear automatically , one period of CK32K after.

11.7.16 P3_DEV

Register	P3_DEV							
Page	1	Address	Dec # 50	Hex 0x32				
Bit	7	6	5	4	3	2	1	0
Name	Not Used	Not Used	Not Used	Not Used	Not Used	P3_DEVACT	P3_DEVSLP	P3_DEVOFF
Read/Write	R	R	R	R	R	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

P3_DEVACT	Write '1' will start a P3_OFF2ACT or P3_SLP2ACT transition This bit is clear automatically , one period of CK32K after.
P3_DEVSLP	Write '1' will start a P3_ACT2SLP transition

P3_DEVOFF	This bit is clear automatically , one period of CK32K after. Write '1' will start a P3_ACT2OFF or P3_SLP2OFF transition This bit is clear automatically , one period of CK32K after.

11.7.17 PB_I2C_WORD_A

Register **PB_I2C_WORD_A**
Page **1** Address **Dec # 51** **Hex 0x33**

Bit	7	6	5	4	3	2	1	0
Name	PB_I2C_WORD_A_7	PB_I2C_WORD_A_6	PB_I2C_WORD_A_5	PB_I2C_WORD_A_4	PB_I2C_WORD_A_3	PB_I2C_WORD_A_2	PB_I2C_WORD_A_1	PB_I2C_WORD_A_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	1	1	1	1	1	1	1	1

Register bits description

PB_I2C_WORD_A [7:0]	

11.7.18 PB_I2C_WORD_B

Register **PB_I2C_WORD_B**
Page **1** Address **Dec # 52** **Hex 0x34**

Bit	7	6	5	4	3	2	1	0
Name	PB_I2C_WORD_B_7	PB_I2C_WORD_B_6	PB_I2C_WORD_B_5	PB_I2C_WORD_B_4	PB_I2C_WORD_B_3	PB_I2C_WORD_B_2	PB_I2C_WORD_B_1	PB_I2C_WORD_B_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	1	1	1	1	1	1	1	1

Register bits description

PB_I2C_WORD_B [7:0]	

11.7.19 PB_I2C_WORD_C

Register **PB_I2C_WORD_C**
Page **1** Address **Dec # 53** **Hex 0x35**

Bit	7	6	5	4	3	2	1	0
Name	PB_I2C_WORD_C_7	PB_I2C_WORD_C_6	PB_I2C_WORD_C_5	PB_I2C_WORD_C_4	PB_I2C_WORD_C_3	PB_I2C_WORD_C_2	PB_I2C_WORD_C_1	PB_I2C_WORD_C_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	1	1	1	1	1	1	1	1

Register bits description

PB_I2C_WORD_C [7:0]	

11.7.20 PB_I2C_WORD_D

Register **PB_I2C_WORD_D**
Page **1** Address **Dec # 54** **Hex 0x36**

Bit	7	6	5	4	3	2	1	0
Name	PB_I2C_WORD_D_7	PB_I2C_WORD_D_6	PB_I2C_WORD_D_5	PB_I2C_WORD_D_4	PB_I2C_WORD_D_3	PB_I2C_WORD_D_2	PB_I2C_WORD_D_1	PB_I2C_WORD_D_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	1	1	1	1	1	1	1	1

Register bits description

PB_I2C_WORD_D [7:0]	

11.8 SLAVE REGISTERS

11.8.1 BBSPOR_CFG

Register	BBSPOR_CFG							
Page	1	Address	Dec # 58	Hex 0x3A				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	BBCHGEN	BBSEL_1	BBSEL_0	MES_BB
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	1	0	0	0	0

Register bits description

RSRVD (bit 7 to bit 4)	Reserved bits
BBCHGEN	Back up battery charge enable
BBSEL [1:0]	Back up battery charge voltage selection: 00 ➔ 3.1V 01 ➔ 3.2V 10 ➔ 3.0V 11 ➔ VBAT
MES_BB	Enable resistor divider for Back Battery Voltage measure When SLEEPEN=1 this bit is force to '0' outside of the register

11.8.2 VRSIM_CFG_STS

Register	VRSIM_CFG_STS							
Page	1	Address	Dec # 69	Hex 0x45				
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to no device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.3 VRSIM_RES_ID

Register	VRSIM_RES_ID							
Page	1	Address	Dec # 70	Hex 0x46				
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	0	0	1	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 2

11.8.4 VRSIM_CFG_STATE

Register	VRSIM_CFG_STATE							
Page	1	Address	Dec # 71		Hex 0x47			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.5 VRSIM_CFG_DEDICATED

Register	VRSIM_CFG_DEDICATED							
Page	1	Address	Dec # 72		Hex 0x48			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	VSEL
Read/Write	R	R	R	R	R	R	R	R/W
Reset_off	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 1)	Reserved bits
VSEL	'1' : Output voltage is set to 2.8V '0' : Output voltage is set to 1.8V

11.8.6 VRMMC_CFG_STS

Register	VRMMC_CFG_STS							
Page	1	Address	Dec # 73		Hex 0x49			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to no device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.7 VRMMC_RES_ID

Register	VRMMC_RES_ID							
Page	1	Address	Dec # 74		Hex 0x4A			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	0	0	1	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0

	These bits are the same for all resources. RES_ID[3:0] : Default resource number is 3

11.8.8 VRMMC_CFG_STATE

Register	VRMMC_CFG_STATE							
Page	1	Address	Dec # 75	Hex 0x4B				
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.9 VRMMC_CFG_DEDICATED

Register	VRMMC_CFG_DEDICATED							
Page	1	Address	Dec # 76	Hex 0x4C				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	VSEL
Read/Write	R	R	R	R	R	R	R	R/W
Reset_off	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 to bit1)	Reserved bits
VSEL	'1' : Output voltage is set to 2.8V '0' : Output voltage is set to 1.8V

11.8.10 VREXTH_CFG_STS

Register	VREXTH_CFG_STS							
Page	1	Address	Dec # 77	Hex 0x4D				
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.11 VREXTH_RES_ID

Register	VREXTH_RES_ID							
Page	1	Address	Dec # 78	Hex 0x4E				
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	0	1	0	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 4

11.8.12 VREXTH_CFG_STATE

Register	VREXTH_CFG_STATE							
Page	1	Address	Dec # 79	Hex 0x4F				
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.13 VREXTH_CFG_DEDICATED

Register	VREXTH_CFG_DEDICATED							
Page	1	Address	Dec # 80	Hex 0x50				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	VSEL
Read/Write	R	R	R	R	R	R	R	R/W
Reset_off	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 1)	Reserved bits
VSEL	'1' : Output voltage is set to 2.8V '0' : Output voltage is set to 1.8V

11.8.14 VRPLL_CFG_STS

Register	VRPLL_CFG_STS							
Page	1	Address	Dec # 81	Hex 0x51				
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.15 VRPLL_RES_ID

Register	VRPLL_RES_ID							
Page	1	Address	Dec # 82	Hex 0x52				
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	0	1	0	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 5

11.8.16 VRPLL_CFG_STATE

Register	VRPLL_CFG_STATE							
Page	1	Address	Dec # 83	Hex 0x53				
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.17 VRPLL_CFG_DEDICATED

Register	VRPLL_CFG_DEDICATED							
Page	1	Address	Dec # 84	Hex 0x54				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	VSEL_1	VSEL_0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset_bck	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 2)	Reserved bits
VSEL [1:0]	“11” : Output voltage is 1.4V “10” or “01” : Output voltage is 1.3V “00” : Output voltage is 1.05V

11.8.18 VRIO_CFG_STS

Register	VRIO_CFG_STS							
Page	1	Address	Dec # 85	Hex 0x55				
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM and DEV_GRP_PERIPH device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.19 VRIO_RES_ID

Register	VRIO_RES_ID							
Page	1	Address	Dec # 86		Hex 0x56			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	0	1	1	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 6

11.8.20 VRIO_CFG_STATE

Register	VRIO_CFG_STATE							
Page	1	Address	Dec # 87		Hex 0x57			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.21 VRMEM_CFG_STS

Register	VRMEM_CFG_STS							
Page	1	Address	Dec # 89		Hex 0x59			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.22 VRMEM_RES_ID

Register	VRMEM_RES_ID							
Page	1	Address	Dec # 90		Hex 0x5A			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	0	1	1	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 7

11.8.23 VRMEM_CFG_STATE

Register	VRMEM_CFG_STATE							
Page	1	Address	Dec # 91		Hex 0x5B			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.24 VRUSB_CFG_STS

Register	VRUSB_CFG_STS							
Page	1	Address	Dec # 93		Hex 0x5D			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to no device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.25 VRUSB_RES_ID

Register	VRUSB_RES_ID							
Page	1	Address	Dec # 94		Hex 0x5E			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	1	0	1	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 10

11.8.26 VRUSB_CFG_STATE

Register	VRUSB_CFG_STATE							
Page	1	Address	Dec # 95		Hex 0x5F			
Bit	7	6	5	4	3	2	1	0
Name	OFF_STATE_3	OFF_STATE_2	OFF_STATE_1	OFF_STATE_0	SLEEP_STATE_3	SLEEP_STATE_2	SLEEP_STATE_1	SLEEP_STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.27 VRUSB_CFG_DEDICATED

Register	VRUSB_CFG_DEDICATED							
Page	1	Address	Dec # 96		Hex 0x60			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	LVS_USB2IO_EN	LVS_USB2IO_AUTO
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset_bck	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 2)	Reserved bits
LVS_USB2IO_EN	Enable Level Shifter between VRUSB and VRIO Bit is update to 0/1 reflecting level shifter status when LVS_USB2IO_AUTO is set to '1'
LVS_USB2IO_AUTO	'0' : Level shifter enable is controlled by LVS_USB2IO_EN bit '1' : Level shifter are enable/disable by detecting VRUSB and VRIO activities

11.8.28 VRABB_CFG_STS

Register	VRABB_CFG_STS							
Page	1	Address	Dec # 97		Hex 0x61			
Bit	7	6	5	4	3	2	1	0
Name	DEV_GRP_2	DEV_GRP_1	DEV_GRP_0	RSRVD	RES_STATE_3	RES_STATE_2	RES_STATE_1	RES_STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.29 VRABB_RES_ID

Register	VRABB_RES_ID							
Page	1	Address	Dec # 98		Hex 0x62			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	1	0	1	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 11

11.8.30 VRABB_CFG_STATE

Register	VRABB_CFG_STATE							
Page	1	Address	Dec # 99		Hex 0x63			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.31 VRABB_CFG_DEDICATED

Register	VRABB_CFG_DEDICATED							
Page	1	Address	Dec # 100		Hex 0x64			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	LVS_ ABB2IO_EN	LVS_ ABB2IO_AUTO	BIASABB _EN	BIASABB _AUTO
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	0	1	0	1

Register bits description

RSRVD (bit 7 – bit 4)	Reserved bits
LVS_ABB2IO_EN	Enable Level Shifter between VRABB and VRIO Bit is update to 0/1 reflecting level shifter status when LVS_ABB2IO_AUTO is set to '1'
LVS_ABB2IO_AUTO	'0' : Level shifter enable is controlled by LVS_ABB2IO_EN bit '1' : Level shifter are enable/disable by detecting VRABB and VRIO activi-ties
BIASABB_EN	Enable Bias for module connected on VRABB Bit is update to 0/1 reflecting bias enable status when BIASABB_AUTO is set to '1'
BIASABB_AUTO	'0' : Bias enable is controlled by BIASABB_EN bit '1' : Bias is enable/disable by detecting VRABB activities

11.8.32 VREXTL_CFG_STS

Register	VREXTL_CFG_STS							
Page	1 Address Dec # 105 Hex 0x69							
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.33 VREXTL_RES_ID

Register	VREXTL_RES_ID							
Page	1 Address Dec # 106 Hex 0x6A							
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	1	1	0	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 13

11.8.34 VREXTL_CFG_STATE

Register	VREXTL_CFG_STATE							
Page	1 Address Dec # 107 Hex 0x6B							
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.35 VREXTL_CFG_DEDICATED

Register	VREXTL_CFG_DEDICATED							
Page	1 Address Dec # 108 Hex 0x6C							
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	SLEEP _VSEL_1	SLEEP _VSEL_0	ACTIVE _VSEL_1	ACTIVE _VSEL_0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset_bck RMODE = 0	0	0	0	0	1	0	1	0
Reset_bck RMODE = 1	0	0	0	0	0	1	0	1

Note: RMODE is a Resource control. It is a Reset mode (select between 2 values at reset for some register bits). The pad is called BM_SEL.

Register bits description

RSRVD (bit 7 – bit 4)	Reserved bits
SLEEP_VSEL [1:0]	Voltage used in SLEEP mode '00' : Output voltage is 1.05V '01' : Output voltage is 1.3V '10' : Output voltage is 1.8V '11' : Output voltage is 2.8V
ACTIVE_VSEL [1:0]	Voltage used in ACTIVE mode '00' : Output voltage is 1.05V '01' : Output voltage is 1.3V '10' : Output voltage is 1.8V '11' : Output voltage is 2.8V

11.8.36 EXT_REGEN_CFG_STS

Register	EXT_REGEN_CFG_STS							
Page	1 Address Dec # 109 Hex 0x6D							
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	0	0	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_PERIPH device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.37 EXT_REGEN_RES_ID

Register	EXT_REGEN_RES_ID							
Page	1 Address Dec # 110 Hex 0x6E							
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	0	0	1	1	1	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 0 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 14

11.8.38 EXT_REGEN_CFG_STATE

Register	EXT_REGEN_CFG_STATE							
Page	1 Address Dec # 111 Hex 0x6F							
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.39 CBAT32_CFG_STS

Register	CBAT32_CFG_STS							
Page	1	Address	Dec # 112	Hex 0x70				
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	1	1	1	0

Register bits description

DEV_GRP [2:0]	Owns to all device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.40 CBAT32_RES_ID

Register	CBAT32_RES_ID							
Page	1	Address	Dec # 113	Hex 0x71				
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	0	0	0	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 1

11.8.41 CBAT32_CFG_STATE

Register	CBAT32_CFG_STATE							
Page	1	Address	Dec # 114	Hex 0x72				
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset_bck	1	1	1	0	1	1	1	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 1110
SLEEP_STATE [3:0]	Option disable

11.8.42 BGAP_CFG_STS

Register	BGAP_CFG_STS							
Page	1	Address	Dec # 118		Hex 0x76			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to all device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.43 BGAP_RES_ID

Register	BGAP_RES_ID							
Page	1	Address	Dec # 119		Hex 0x77			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	0	0	1	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 3 MBG

11.8.44 BGAP_CFG_STATE

Register	BGAP_CFG_STATE							
Page	1	Address	Dec # 120		Hex 0x78			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.45 BGSLP_CFG_STS

Register	BGSLP_CFG_STS							
Page	1	Address	Dec # 122		Hex 0x7A			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	1	1	1	1

Register bits description

DEV_GRP [2:0]	Owns to all device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.46 BGSLP_RES_ID

Register	BGSLP_RES_ID							
Page	1	Address	Dec # 123		Hex 0x7B			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	0	1	0	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 4 LBG

11.8.47 BGSLP_CFG_STATE

Register	BGSLP_CFG_STATE							
Page	1	Address	Dec # 124		Hex 0x7C			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset_bck	1	1	1	1	1	1	1	1

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 1111
SLEEP_STATE [3:0]	Option disable

11.8.48 TSHUTDOWN_CFG_STS

Register	TSHUTDOWN_CFG_STS							
Page	1	Address	Dec # 125		Hex 0x7D			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to all device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.49 TSHUTDOWN_RES_ID

Register	TSHUTDOWN_RES_ID							
Page	1	Address	Dec # 126		Hex 0x7E			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	0	1	0	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 5

11.8.50 TSHUTDOWN_CFG_STATE

Register	TSHUTDOWN_CFG_STATE							
Page	1	Address	Dec # 127		Hex 0x7F			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	1	1	1

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1111

11.8.51 TSHUTDOWN_CFG_DEDICATED

Register	TSHUTDOWN_CFG_DEDICATED							
Page	1	Address	Dec # 128		Hex 0x80			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	THERM_ HD	THERM_ TS	RSRVD	THERM_ HDSEL_1	THERM_ HDSEL_0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset_bck	0	0	0	0	0	0	1	1

Register bits description

RSRVD (bit 7 to 5)	Reserved bits
THERM_HD	Hot die detector output
THERM_TS	Thermal shutdown detector output
RSRVD (bit 2)	Reserved bit
THERM_HDSEL [1:0]	Temperature selection for Hot Die detector: 00 : Low temperature threshold … 11 : High temperature threshold

11.8.52 BIAS_CFG_STS

Register	BIAS_CFG_STS							
Page	1	Address	Dec # 129		Hex 0x81			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to all device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.53 BIAS_RES_ID

Register	BIAS_RES_ID							
Page	1	Address	Dec # 130		Hex 0x82			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	0	1	1	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 6

11.8.54 BIAS_CFG_STATE

Register	BIAS_CFG_STATE							
Page	1	Address	Dec # 131		Hex 0x83			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.55 CLKON_CFG_STS

Register	CLKON_CFG_STS							
Page	1	Address	Dec # 132		Hex 0x84			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM and DEV_GRP_PERIPH device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.56 CLKON_RES_ID

Register	CLKON_RES_ID							
Page	1	Address	Dec # 133		Hex 0x85			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	0	1	1	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 7

11.8.57 CLKON_CFG_STATE

Register	CLKON_CFG_STATE							
Page	1	Address	Dec # 134		Hex 0x86			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option available – By default SLEEP_STATE = 1000

11.8.58 STATE_MNGT_CFG_STS

Register	STATE_MNGT_CFG_STS							
Page	1	Address	Dec # 135		Hex 0x87			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM and DEV_GRP_PERIPH device groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.59 STATE_MNGT_RES_ID

Register	STATE_MNGT_RES_ID							
Page	1	Address	Dec # 136		Hex 0x88			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	1	0	0	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 8

11.8.60 STATE_MNGT_CFG_STATE

Register	STATE_MNGT_CFG_STATE							
Page	1	Address	Dec # 137		Hex 0x89			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset_bck	0	0	0	0	1	1	1	1

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option disable

11.8.61 SLEEP_MNGT_CFG_STS

Register	SLEEP_MNGT_CFG_STS							
Page	1	Address	Dec # 138		Hex 0x8A			
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	1	0	0	0	0

Register bits description

DEV_GRP [2:0]	Owns to DEV_GRP_MODEM device group
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.62 SLEEP_MNGT_RES_ID

Register	SLEEP_MNGT_RES_ID							
Page	1	Address	Dec # 139		Hex 0x8B			
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	1	0	1	1

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 11

11.8.63 SLEEP_MNGT_CFG_STATE

Register	SLEEP_MNGT_CFG_STATE							
Page	1	Address	Dec # 140	Hex 0x8C				
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset_bck	0	0	0	0	1	0	0	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 0000
SLEEP_STATE [3:0]	Option disable

11.8.64 BAT_PRES_CHECK_CFG_STS

Register	BAT_PRES_CHECK_CFG_STS							
Page	1	Address	Dec # 144	Hex 0x90				
Bit	7	6	5	4	3	2	1	0
Name	DEV_ GRP_2	DEV_ GRP_1	DEV_ GRP_0	RSRVD	RES_ STATE_3	RES_ STATE_2	RES_ STATE_1	RES_ STATE_0
Read/Write	R/W	R/W	R/W	R	R	R	R	R
Reset_bck	1	1	1	1	1	1	1	0

Register bits description

DEV_GRP [2:0]	Owns to all groups
RSRVD (bit 4)	Reserved bit
RES_STATE [3:0]	This field indicates the current state of the resource, it is a read only field

11.8.65 BAT_PRES_CHECK_RES_ID

Register	BAT_PRES_CHECK_RES_ID							
Page	1	Address	Dec # 145	Hex 0x91				
Bit	7	6	5	4	3	2	1	0
Name	RES_ID_7	RES_ID_6	RES_ID_5	RES_ID_4	RES_ID_3	RES_ID_2	RES_ID_1	RES_ID_0
Read/Write	R	R/W	R/W	R	R	R	R	R
Reset_bck	0	0	1	0	1	0	1	0

Register bits description

RES_ID [7:0]	RES_ID[7]=0 : Use a 16 resources cluster RES_ID[6:4]=0 : Default cluster has number 2 These bits are the same for all resources. RES_ID[3:0] : Default resource number is 10

11.8.66 BAT_PRES_CHECK_CFG_STATE

Register	BAT_PRES_CHECK_CFG_STATE							
Page	1	Address	Dec # 146		Hex 0x92			
Bit	7	6	5	4	3	2	1	0
Name	OFF_ STATE_3	OFF_ STATE_2	OFF_ STATE_1	OFF_ STATE_0	SLEEP_ STATE_3	SLEEP_ STATE_2	SLEEP_ STATE_1	SLEEP_ STATE_0
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R
Reset_bck	1	1	1	0	1	1	1	0

Register bits description

OFF_STATE [3:0]	Option available – By default OFF_STATE = 1110
SLEEP_STATE [3:0]	Option not available

Note:

P: Bit protected by PKEY

W: Write
R: Read

12 INTERRUPTS

12.1 INTERRUPT SOURCES

One interrupt signal (P1_INT2) is generated for the modem processor.

When the INT2_P1_STS register is not zero, the INT2_ P1 output is set to active low, indicating that an interrupt has occurred and that the status register is ready to be read.

When an I2C write access is made to the INT2_P1_STS register, it is cleared and the INT2_P1 output is set to high.

For each INT2_P1 there is a masking bit associated to each individual interrupt, INT2_P1_MSK.

When INT2_P1_MSK [i] bit is set to 1, the associated interrupt is masked. This means that if a interrupt event occurs, the interrupt is not generated.

INT2 sources	Section	Block	Description
1	AUX	BCI	Charge-stop event
2	AUX	BCI	VBUS pre-charge detection
3	AUX	BCI	Watchdog overflow
4	AUX	M-ADC	Monitoring ADC end of conversion (SW #1)
5	AUX	M-ADC	Monitoring ADC end of conversion (SW #2)
6	AUX	USB	USB/Carkit ID VBUS D+/D- detection
7	AUX	SIM-card	SIM-card plug / un-plug detection
8	PM	PM control	Falling-edge on PWON
9	PM	PM control	Event on RPWON
10	PM	PM control	Battery charger detection
11	PM	PM control	RTC event
12	PM	PM control	Low-battery detection
13	PM	PM control	USB ID / V_{BUS} detection
14	PM	Thermistor	Hot-Die condition detection
15	AUDIO	Audio/Voice	Audio Send / End detection (Hook-detect)
16	AUDIO	Audio/Voice	Headset plug / un-plug detection

Note1: AUX section contains the interrupts from the auxiliary functions (BCI, M-ADC, USB, SIM-Card), PM sections contains the interrupts related to the Power Management (PM) and the thermistor, AUDIO section contains the interrupts from the audio/voice section.

Note2: ONLY one write access to any of the 2 interrupt status registers (INT2_P1_STS_A and INT2_P1_STS_B) is necessary to clear BOTH registers and to release the P1_INT2 signal.

Table 60 : Interrupt Sources Table

12.2 REGISTERS

12.2.1 INT2_P1_STS_A

Register	INT2_P1_STS_A							
Page	0	Address	Dec # 244		Hex 0xF4			
Bit	7	6	5	4	3	2	1	0
Name	INT2_P1_STS_7	INT2_P1_STS_6	INT2_P1_STS_5	INT2_P1_STS_4	INT2_P1_STS_3	INT2_P1_STS_2	INT2_P1_STS_1	INT2_P1_STS_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

INT2_P1_STS [7:0]	Status of interrupt number 0 to 7. INT2_P1_STS[i] is set to 1 when the associated interrupt number i event is detected All bits are cleared to 0 when a WRITE access (data 0 or 1) occurs on this register.

12.2.2 INT2_P1_STS_B

Register	INT2_P1_STS_B							
Page	0	Address	Dec # 245		Hex 0xF5			
Bit	7	6	5	4	3	2	1	0
Name	INT2_P1_STS_15	INT2_P1_STS_14	INT2_P1_STS_13	INT2_P1_STS_12	INT2_P1_STS_11	INT2_P1_STS_10	INT2_P1_STS_9	INT2_P1_STS_8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

INT2_P1_STS [15:8]	Status of interrupt number 8 to 15. INT2_P1_STS[i] is set to 1 when the associated interrupt number i event is detected All bits are cleared to 0 when a WRITE access (data 0 or 1) occurs on this register.

12.2.3 INT2_P1_MSK_A

Register	INT2_P1_MSK_A							
Page	0	Address	Dec # 246		Hex 0xF6			
Bit	7	6	5	4	3	2	1	0
Name	INT2_P1_MSK_7	INT2_P1_MSK_6	INT2_P1_MSK_5	INT2_P1_MSK_4	INT2_P1_MSK_3	INT2_P1_MSK_2	INT2_P1_MSK_1	INT2_P1_MSK_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

INT2_P1_MSK [7:0]	Mask of interrupt number 0 to 7. When INT2_P1_MSK[i] is set to 1, the associated interrupt number i is masked, no INT2_P1 is generated, INT2_P1_STS[i] is not updated and the internal interrupt i is cleared and acknowledged. When INT2_P1_MSK[i] is set to 0 , the associated interrupt number i is enabled : INT2_P1 is generated, INT2_P1_STS[i] is updated and internal interrupt i is cleared and acknowledged.

12.2.4 INT2_P1_MSK_B

Register	INT2_P1_MSK_B							
Page	0	Address	Dec # 247		Hex 0xF7			
Bit	7	6	5	4	3	2	1	0
Name	INT2_P1_MSK_15	INT2_P1_MSK_14	INT2_P1_MSK_13	INT2_P1_MSK_12	INT2_P1_MSK_11	INT2_P1_MSK_10	INT2_P1_MSK_9	INT2_P1_MSK_8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

INT2_P1_MSK [15:8]	Mask of interrupt number 8 to 15. When INT2_P1_MSK[i] is set to 1, the associated interrupt number i is masked, no INT2_P1 is generated, INT2_P1_STS[i] is not updated and the internal interrupt i is cleared and acknowledged. When INT2_P1_MSK[i] is set to 0 , the associated interrupt number i is enabled : INT2_P1 is generated, INT2_P1_STS[i] is updated and internal interrupt i is cleared and acknowledged.

13 REAL TIME CLOCK

13.1 FUNCTIONALITIES

The functionalities of the RTC block are:

- Time informations (seconds/minutes/hours) directly in BCD code
- Calendar Informations (Day/Month/Year/ Day of the week) directly in BCD code up to year 2099
- Interrupts generation, periodically (1s / 1m / 1h / 1d period) or at a precise time of the day (alarm function)
- 30s time correction
- oscillator frequency calibration

13.2 BLOCKS DIAGRAM

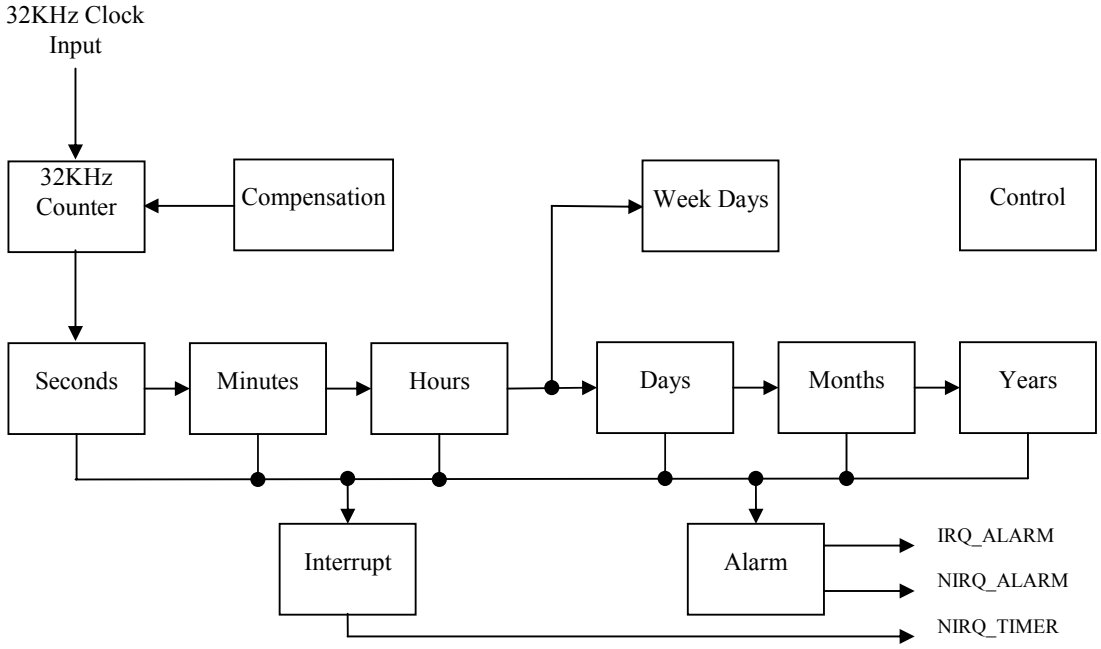


Figure 35 : RTC Digital Section Block Diagram

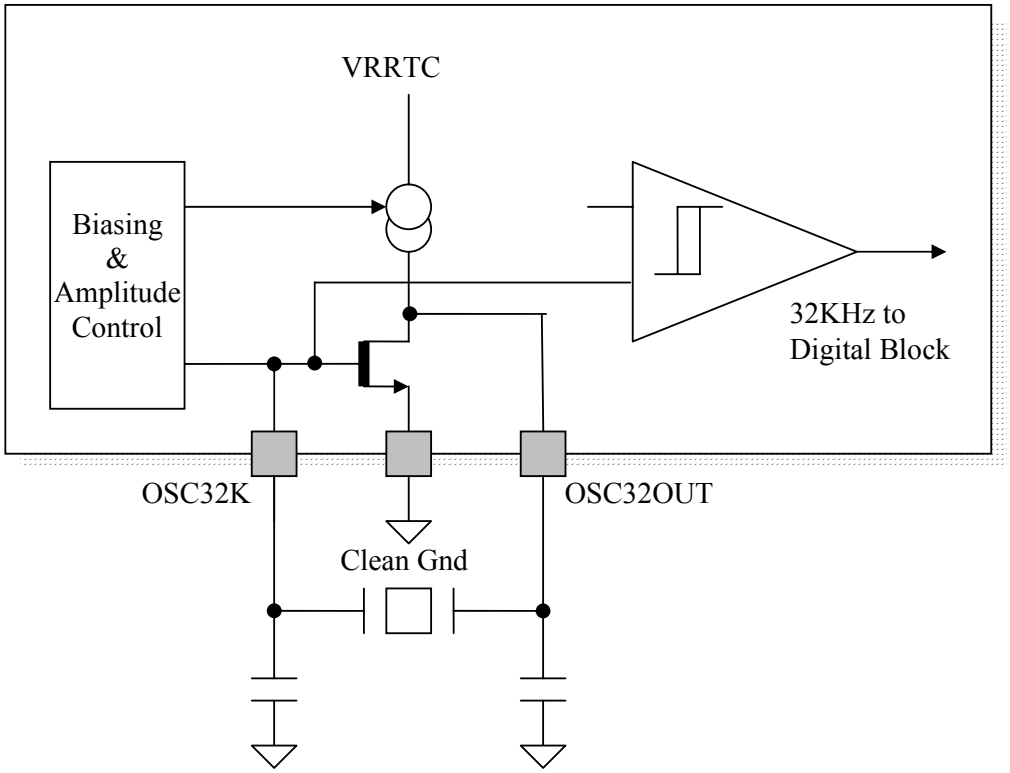


Figure 36 : Block Diagram of the Analog Cell

13.3 TYPES OF REGISTERS

There are three types of registers:

1. TC and TC alarm registers
2. General registers
3. Compensation registers

TC Registers

All the time and calendar informations are available in these dedicated registers, called TC registers. The TC registers values are written in BCD code (Binary Coded Decimal).

1. Year data ranges from 00 to 99
   - Leap Year = Year divisible by four (2000, 2004, 2008, 2012, …).
   - Common Year = other years
2. Month data ranges from 01 to 12
3. Day value ranges from:
   - 1 to 31 when months are 1,3,5,7,8,10,12
   - 1 to 30 when months are 4,6,9,11
   - 1 to 29 when month is 2 and year is a leap year
   - 1 to 28 when month is 2 and year is a common year
4. Week value ranges from 0 to 6

5. Hour value ranges from 00 to 23 in 24 hour mode and ranges from 1 to 12 in AM/PM mode
6. Minutes value ranges from 0 to 59
7. Seconds value ranges from 0 to 59

To modify the current time, the micro-controller writes the new time into TC registers in order to fix the time/calendar information. micro-controller can write into TC registers without stopping the RTC.
Also, the micro-controller can stop the RTC by clearing STOP_RTC bit of the control register and check the RUN bit of the status to be sure that the RTC is frozen. Then update TC values, and then re-start the RTC by setting STOP_RTC bit.

Example: Time is 10H54M36S PM (PM_AM mode set), the 5th of September 97 previous registers values will be:

SECONDS_REG	0x36
MINUTES_REG	0x54
HOURS_REG	0x90
DAYS_REG	0x05
MONTHS_REG	0x09
YEARS_REG	0x97

You can round to the closest minute, by setting ROUND_30S bit of the control register; TC values are set to the closest minute value at the next second. ROUND_30S bit will be automatically cleared when rounding time is performed.

Example: if current time is 10H59M45S, round operation will change time to 11H00M00S.
if current time is 10H59M29S, round operation will change time to 10H59M00S.

General Registers

The micro-controller can access to the STATUS_REG and to the CTRL_REG at any time (excepted for the CTRL_REG[5] bit which must be changed only when the RTC is stopped).

Compensation Registers

The COMP_MSB_REG and COMP_LSB_REG must respected the available access period. These registers should be updated before each compensation, before each hours and one second.
For example, the micro-controller could load the compensation value into these registers after each hour event, during an available access period.

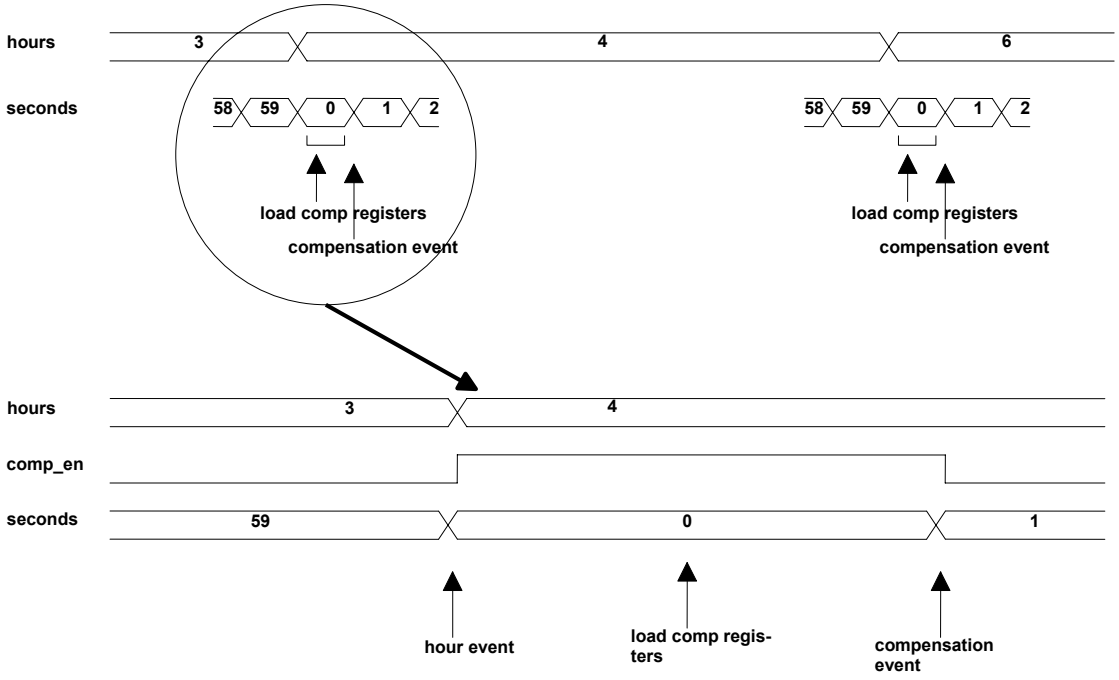


Figure 37 : Compensation Scheduling

In order to compensate any inaccuracy of the 32 kHz oscillator, it is possible to balance this drift. The micro-controller should perform a calibration of the oscillator frequency, calculate the drift compensation versus one time hour period; and then the micro-controller should load the compensation registers with the drift compensation value. Indeed, if the AUTO_COMP_EN bit in the RTC_CTRL_REG is enabled, the COMP_REG value (in 2 complement) is added to the RTC 32 kHz counter at each hour and one second. When COMP_REG is added to RTC 32 kHz counter, the duration of the current second becomes (32768 - COMP_REG) / 32768 s; so, it is possible to compensate the RTC with a 1/32768 s time unit accuracy by hour.

13.4 RTC INTERRUPTS

RTC can generate interrupts. The timer interrupt, and the alarm interrupt.

Timer Interrupt

Timer interrupt can be generated periodically, either every second, or every minute, or every hour, or every day (RTC_INTERRUPTS_REG[1:0]). This interrupt is enabled by the IT_TIMER bit of the interrupts register. It is a negative edge sensitive interrupt (low level pulse duration = 15 µs). The RTC_STATUS_REG[5:2] are only updated at each new interrupt and show what events have happened.

Alarm Interrupt

Alarm interrupt can be generated when the time set into TC ALARM registers is exactly the same as in the TC registers. This interrupt is then generated if the IT_ALARM bit of the interrupts register is set. This interrupt is low level sensitive, RTC_STATUS_REG[6] indicates that Alarm interrupt occurred. This interrupt is disable by writing ‘1’ into the RTC_STATUS_REG[6].

13.5 REGISTERS

13.5.1 SECONDS_REG

Register	SECONDS_REG							
Page	1	Address	Dec # 0	Hex 0x00				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	SEC1_2	SEC1_1	SEC1_0	SEC0_3	SEC0_2	SEC0_1	SEC0_0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7)	Reserved bit
SEC1 [2:0]	Second digit of seconds (range is 0 up to 5)
SEC0 [3:0]	First digit of seconds (range is 0 up to 9)

13.5.2 MINUTES_REG

Register	MINUTES_REG							
Page	1	Address	Dec # 1	Hex 0x01				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	MIN1_2	MIN1_1	MIN1_0	MIN0_3	MIN0_2	MIN0_1	MIN0_0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7)	Reserved bit
MIN1 [2:0]	Second digit of minutes (range is 0 up to 5)
MIN0 [3:0]	First digit of minutes (range is 0 up to 9)

13.5.3 HOURS_REG

Register	HOURS_REG							
Page	1	Address	Dec # 2	Hex 0x02				
Bit	7	6	5	4	3	2	1	0
Name	PM_nAM	RSRVD	HOUR1_1	HOUR1_0	HOUR0_3	HOUR0_2	HOUR0_1	HOUR0_0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

PM_nAM	Only used in PM_AM mode (otherwise it is set to 0) 0 ➔ AM 1 ➔ PM
RSRVD (bit 6)	Reserved bit
HOUR1 [2:0]	Second digit of hours (range is 0 up to 2)
HOUR0 [3:0]	First digit of hours (range is 0 up to 9)

13.5.4 DAYS_REG

Register	DAYS_REG							
Page	1	Address	Dec # 3	Hex 0x03				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	DAY1_1	DAY1_0	DAY0_3	DAY0_2	DAY0_1	DAY0_0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
DAY1 [2:0]	Second digit of hours (range is 0 up to 3)
DAY0 [3:0]	First digit of hours (range is 0 up to 9)

13.5.5 MONTHS_REG

Register	MONTHS_REG							
Page	1	Address	Dec # 4	Hex 0x04				
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	MONTH1_0	MONTH0_3	MONTH0_2	MONTH0_1	MONTH0_0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	1

Register bits description

RSVRD (bit 7 – bit 5)	Reserved bits
MONTH1	Second digit of months (range is 0 up to 1)
MONTH0 [3:0]	First digit of months (range is 0 up to 9)

Note: usual notation is taken for month value, that is:
01 ➔ January (default value)
02 ➔ February
…
12 ➔ December

13.5.6 YEARS_REG

Register	YEARS_REG							
Page	1	Address	Dec # 5	Hex 0x05				
Bit	7	6	5	4	3	2	1	0
Name	YEAR1_3	YEAR1_2	YEAR1_1	YEAR1_0	YEAR0_3	YEAR0_2	YEAR0_1	YEAR0_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

YEAR1 [3:0]	Second digit of years (range is 0 up to 9)
YEAR0 [3:0]	First digit of years (range is 0 up to 9)

13.5.7 WEEKS_REG

Register	WEEKS_REG							
Page	1	Address	Dec # 6		Hex 0x06			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	WEEK_2	WEEK_1	WEEK_0
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 3)	Reserved bits
WEEK [2:0]	First digit of days in a week (range is 0 up to 6)

13.5.8 ALARM_SECONDS_REG

Register	ALARM_SECONDS_REG							
Page	1	Address	Dec # 8		Hex 0x08			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	ALARM_ SEC1_2	ALARM_ SEC1_1	ALARM_ SEC1_0	ALARM_ SEC0_3	ALARM_ SEC0_2	ALARM_ SEC0_1	ALARM_ SEC0_0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7)	Reserved bit
ALARM_SEC1 [2:0]	Second digit of seconds (range is 0 up to 5)
ALARM_SEC0 [3:0]	First digit of seconds (range is 0 up to 9)

13.5.9 ALARM_MINUTES_REG

Register	ALARM_MINUTES_REG							
Page	1	Address	Dec # 9		Hex 0x09			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	ALARM_ MIN1_2	ALARM_ MIN1_1	ALARM_ MIN1_0	ALARM_ MIN0_3	ALARM_ MIN0_2	ALARM_ MIN0_1	ALARM_ MIN0_0
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7)	Reserved bit
ALARM_MIN1 [2:0]	Second digit of seconds (range is 0 up to 5)
ALARM_MIN0 [3:0]	First digit of seconds (range is 0 up to 9)

13.5.10 ALARM_HOURS_REG

Register	ALARM_HOURS_REG							
Page	1	Address	Dec # 10		Hex 0x0A			
Bit	7	6	5	4	3	2	1	0
Name	ALARM_ PM_nAM	RSRVD	ALARM_ HOUR1_1	ALARM_ HOUR1_0	ALARM_ HOUR0_3	ALARM_ HOUR0_2	ALARM_ HOUR0_1	ALARM_ HOUR0_0
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

ALARM_PM_nAM	0 ➔ AM Only used in PM_AM mode (otherwise it is set to 0) 1 ➔ PM
RSRVD (bit 6)	Reserved bit
ALARM_MIN1 [2:0]	Second digit of seconds (range is 0 up to 5)
ALARM_MIN0 [3:0]	First digit of seconds (range is 0 up to 9)

13.5.11 ALARM_DAYS_REG

Register	ALARM_DAYS_REG							
Page	1	Address	Dec # 11		Hex 0x0B			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	ALARM_ DAY1_1	ALARM_ DAY1_0	ALARM_ DAY0_3	ALARM_ DAY0_2	ALARM_ DAY0_1	ALARM_ DAY0_0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
ALARM_DAY1 [1:0]	Second digit of days (range is 0 up to 3)
ALARM_DAY0 [3:0]	First digit of days (range is 0 up to 9)

13.5.12 ALARM_MONTHS_REG

Register	ALARM_MONTHS_REG							
Page	1	Address	Dec # 12		Hex 0x0C			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	ALARM_ MONTH1_0	ALARM_ MONTH0_3	ALARM_ MONTH0_2	ALARM_ MONTH0_1	ALARM_ MONTH0_0
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	1

Register bits description

RSRVD (bit 7 – bit 5)	Reserved bits
ALARM_MONTH1 [1:0]	Second digit of months (range is 0 up to 1)
ALARM_MONTH0 [3:0]	First digit of months (range is 0 up to 9)

13.5.13 ALARM_YEARS_REG

Register	ALARM_YEARS_REG							
Page	1	Address	Dec # 13		Hex 0x0D			
Bit	7	6	5	4	3	2	1	0
Name	ALARM_ YEAR1_3	ALARM_ YEAR1_2	ALARM_ YEAR1_1	ALARM_ YEAR1_0	ALARM_ YEAR0_3	ALARM_ YEAR0_2	ALARM_ YEAR0_1	ALARM_ YEAR0_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

ALARM_YEAR1 [3:0]	Second digit of years (range is 0 up to 9)
ALARM_YEAR0 [3:0]	First digit of years (range is 0 up to 9)

13.5.14 RTC_CTRL_REG

Register	RTC_CTRL_REG							
Page	1	Address	Dec # 16		Hex 0x10			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	SET_32_ COUNTER	TEST_ MODE	MODE_ 12_24	AUTO_ COMP	ROUND_ 30S	STOP_ RTC
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
SET_32_COUNTER	0 => No action 1 => set the 32 KHz counter with comp_reg value (See note)
TEST_MODE	0=> functional mode 1 => test mode (Auto compensation is enable when the 32 KHz counter reaches at its end)
MODE_12_24	0 => 24 hours mode (See note) 1 => 12 hours mode (PM-AM mode)
AUTO_COMP	0 => No auto compensation 1 => Auto compensation enabled
ROUND_30S	0 => No update 1 => When a one is written, the time is rounded to the closest minute (See note)
STOP_RTC	0 => RTC is frozen 1 => RTC is running

Note: A dummy read of this register is necessary before each I2C read in order to update the ROUND_30S bit value.
SET_32_counter must only be used when the RTC is frozen.
ROUND_30S bit is a toggle bit, the micro-controller can only write '1', RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller will read '1' until the rounded to the closet minute is perform at the next second.
MODE_12_24 : it is possible to switch between the two mode at any time without disturbed the RTC, read or write are always performed with the current mode.

13.5.15 RTC_STATUS_REG

Register	RTC_STATUS_REG							
Page	1	Address	Dec # 17		Hex 0x11			
Bit	7	6	5	4	3	2	1	0
Name	POWER_UP	ALARM	1D_EVENT	1H_EVENT	1M_EVENT	1S_EVENT	RUN	RSRVD
Read/Write	R/W	R/W	R	R	R	R	R	R
Reset_por	1	0	0	0	0	0	0	0

Register bits description

POWER_UP	Indicates that a reset occurred
ALARM	Indicates that an alarm interrupt has been generated
1D_EVENT	One day has occurred
1H_EVENT	One hour has occurred
1M_EVENT	One minute has occurred
1S_EVENT	One second has occurred
RUN	0 => RTC is frozen 1 => RTC is running

RSRVD (bit 0)	Reserved bit

Note:

A dummy read of this register is necessary before each I^2C read in order to update the status register value.
The alarm interrupt keeps its low level, until the micro-controller write '1' in the ALARM bit of the RTC_STATUS_REG register.
The timer interrupt is a low level pulse (15 µs duration).
RUN bit show the real state of the RTC, indeed because of STOP_RTC signal was resynchronized on 32 KHz clock, the action of this bit is delayed.
POWER_UP is set by a reset, is cleared by writing '1' in this bit.

13.5.16 RTC_INTERRUPTS_REG

Register	RTC_INTERRUPTS_REG							
Page	1 Address	Dec # 18	Hex 0x12					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	IT_ALARM	IT_TIMER	EVERY_1	EVERY_0
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers) by the TC registers
IT_TIMER	Enable periodic interrupt 0 => interrupt disabled 1 => interrupt enabled
EVERY [1:0]	Interrupt period 00 => every second 01 => every minute 10 => every hour 11 => every day

13.5.17 RTC_COMP_LSB_REG

Register	RTC_COMP_LSB_REG							
Page	1 Address	Dec # 19	Hex 0x13					
Bit	7	6	5	4	3	2	1	0
Name	RTC_COMP_LSB_7	RTC_COMP_LSB_6	RTC_COMP_LSB_5	RTC_COMP_LSB_4	RTC_COMP_LSB_3	RTC_COMP_LSB_2	RTC_COMP_LSB_1	RTC_COMP_LSB_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RTC_COMP_LSB [7:0]	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [LSB]

13.5.18 RTC_COMP_MSB_REG

Register	RTC_COMP_MSB_REG							
Page	1 Address	Dec # 20	Hex 0x14					
Bit	7	6	5	4	3	2	1	0
Name	RTC_COMP_MSB_7	RTC_COMP_MSB_6	RTC_COMP_MSB_5	RTC_COMP_MSB_4	RTC_COMP_MSB_3	RTC_COMP_MSB_2	RTC_COMP_MSB_1	RTC_COMP_MSB_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RTC_COMP_MSB [7:0]	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [MSB]

Note: This register must be written in 2 complement.
This means that to add one 32 KHz oscillator period every hour, micro-controller needs to write 'FFFF' into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG.
To remove one 32 KHz oscillator period every hour, micro-controller needs to write '0001' into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG.
The '7FFF' value is forbidden.

13.5.19 RTC_RES_PROG_REG

Register	RTC_RES_PROG_REG							
Page	1	Address	Dec # 21		Hex 0x15			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	SW_RES_PROG_5	SW_RES_PROG_4	SW_RES_PROG_3	SW_RES_PROG_2	SW_RES_PROG_1	SW_RES_PROG_0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset_por	0	0	1	0	0	1	1	1

Register bits description

RSRVD (bit 7 – bit 6)	Reserved bits
SW_RES_PROG [5:0]	Value of the oscillator resistance

13.5.20 RTC_RESET_STATUS_REG

Register	RTC_RESET_STATUS_REG							
Page	1	Address	Dec # 22		Hex 0x16			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RESWON_STATUS
Read/Write	R	R	R	R	R	R	R	R/W
Reset_por	0	0	0	0	0	0	0	0

Register bits description

RSRVD (bit 7 – bit 1)	Reserved bits
RESWON_STATUS	Indicates if a respwon has been done. This bit is cleared by RESPWON pin. It is write once.

13.6 ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Comment
Operational temperature range	-35		85	°C	
Storage temperature	-65		+125	°C	
Operating voltage range	1.6	1.8	2.0	V	
Supply current			3	µA	
Crystal Frequency		32.768		kHz	@ specified load capacitor value
Crystal tolerance			+/- 20	ppm	
Crystal frequency change versus temperature range			-200	ppm	
Max crystal series resistor to be use R1			100	kΩ	@ Fundamental frequency.
Crystal load capacitor	6		12.5	pF	According to crystal data sheet
Load crystal oscillator Cosin ,Cosout	12		25	pF	parallel mode Including parasitic PCB capacitor
Oscillator capacitor ratio COSC32KIN / COSC32KOUT		1			
Frequency Temperature coefficient.		+/-0.5		Ppm/°C	Oscillator contribution (not including crystal variation)
Voltage coefficient		+/- 2		ppm/V	
Duty cycle (CK32KOUT)	40		60		Logic output signal
Logic output external load			40	pF	
Startup time			2	S	On power on

Table 61 : Electrical Characteristics of the Oscillator

14 MONITORING ADC

14.1 FUNCTIONAL DESCRIPTION

The monitoring ADC (MADC) consists of a 10–bit analog–to–digital converter (ADC) combined with a 9–input analog multiplexer. The ADC implementation consists of a successive approximation conversion. Five of the eleven inputs are available externally (ADCIN3, ADCIN4, ADCIN5), and the remaining six inputs are dedicated to die temperature measurement, main battery voltage, backup battery voltage, charger voltage, charger current monitoring and USB Vbus voltage. One external input (ADCIN3) is a standard input. The two others inputs (ADCIN4 and ADCIN5) which are associated with current sources, are intended for battery temperature and battery type measurements.

T3031 MADC is designed to work in a multiprocessor environment. In T3031, the resource “generic analog to digital conversion” is used by Modem (P1) processor.

Uses of the MADC resource done by the P1 processor are different and mostly related to the need of real time constraints for the conversion.

Real Time Conversion Request (STARTADC from P1 only)
In the modem case, in order to be able to monitor battery voltage under heavy current sink, the capability of starting the conversion in a well-defined position with respect to the transmitting burst is often required.
The MADC is activated when **STARTADC** is asserted. When this occurs, the MADC digital control fetches the real time selection register to determine which channels should be sampled and converted. A sequence of conversion will consist from 1 to 9 channels to convert and will process all queued selected channels one after one, starting with channel #1, ending with channel #9. At the end of each conversion, the MADC writes the conversion result into the corresponding results register. An **INT2_P1** interrupt could also be generated at the end of the whole sequence of conversions.

Asynchronous Conversion Request (SP1 from P1)
Modem processor may also require conversions asynchronously with respect to the TDMA frame for general purpose use. These conversion cases are not critical in terms of start of conversion positioning unless the measured value is not the main battery.
General purpose conversions do not require a result granularity in time lower than the duration of three all channels conversion sequences.
While requiring a general purpose conversion, there is no need of specifying on which channel, all channels will be converted.

14.2 ANALOG INPUT CHANNEL DESCRIPTION

Chan-nel	1	2	3	4	5	6	7	8	9
Type	External	External	External	Internal	Internal	Internal	Internal	Internal	Internal
Name	ADCIN3	BT ADCIN4	BTEMP ADCIN5	USBVBUS	VBKP	ICHG	VCHG	VBAT	HOTDIE

- Six internal analog values:
  - Die temperature sensing: HOTDIE
  - Battery voltage: VBAT
  - Battery charger voltage: VCHG
  - Current charger (current–to–voltage (I–to–V) converter): ICHG
  - Backup battery voltage: VBKP
  - USB Vbus voltage

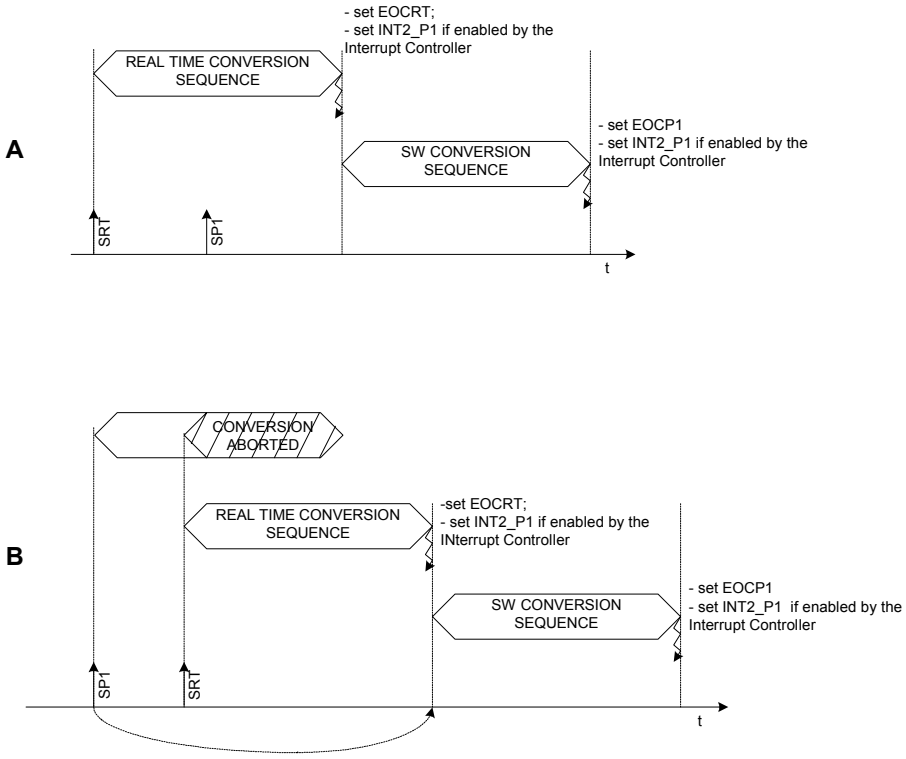
- Three external analog values:
  - Battery temperature: BTEMP = ADCIN5
  - Battery type: BT = ADCIN4
  - ADCIN3

14.3 CONVERSIONS REQUEST SCENARIOS

Modem Processor P1 Request
- SRT: STARTADC IO coming from the modem processor implies real time constraints;
- SP1: a write access (SW) to the toggle bit SP1 in the MADC control register does not imply any real time constraint: this kind of request is called asynchronous or general purpose request.

Possible Scenarios
Given the non-synchronization of the two processors in term of MADC resource sharing, all the combination of those start conditions can be possible. An INT2_P1 interrupt will be sent to the Modem processor **P1** after a real time conversion sequence and after a completed SP1 SW conversion sequence.

The logic control will manage those occurrences using the following rules:



The control logic will manage those occurrences using the following rule:

- STARTADC initiated conversion (SRT) has a higher priority than the SW initiated conversions

Two possible cases to manage:

Case A: Asynchronous SW Request During A Real Time Sequence

If a SW request (SP1) occurs while a STARTADC initiated sequence (SRT) is already running:

- The SW request will be hold and the on going real time sequence will continue until its whole completion and converted data stored in the real time dedicated Ram. Then an INT2_P1 interrupt will be generated and sent to the Modem processor.
- The digital control will execute the SW request after the completion of the real time sequence of conversions. Then, an INT2_P1 interrupt will be generated.

Case B: Real Time STARTADC Request During An Asynchronous Sequence

If a STARTADC real time request occurs while a SW (request SP1) initiated conversion sequence is already running, the on going SW conversion is aborted, the real time conversion sequence is started and a new SW initiated conversion is re-scheduled at the end of the STARTADC sequence.
Then, in terms of conversion time, a SW initiated sequence can reach a maximum of three complete sequences to obtain the conversion results.

14.4 REGISTERS

14.4.1 RTSELECT_LSB

Register	RTSELECT_LSB							
Page	0	Address	Dec # 40	Hex 0x28				
Bit	7	6	5	4	3	2	1	0
Name	CH6	CH5	CH4	CH3	CH2	CH1	RSRVD	RSRVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CH [6:1]	These bits become read-only bits during real-time conversion. When the bit CH[i] is set, MADC channel i is inserted in the conversion sequence started by a real-time request through STARTADC.

14.4.2 RTSELECT_MSB

Register	RTSELECT_MSB							
Page	0	Address	Dec # 41	Hex 0x29				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	CH9	CH8	CH7
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

CH [9-7]	These bits become read-only bits during real-time conversion. When the bit CH[i] is set, MADC channel i is inserted in the conversion sequence started by a real-time request through STARTADC.

14.4.3 CTRL_P1

Register	CTRL_P1							
Page	0	Address	Dec # 42	Hex 0x2A				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	SP1	EOCRT	EOCP1	BUSY
Read/Write	R	R	R	R	W	R	R	R
Reset_off	0	0	0	0	0	1	1	0

Register bits description

SP1	**Start Processor 1.**Toggle bit used by the processor 1 to start an all channel conversion. Writing logical '0' in this bit has no effect.
EOCRT	**End Of Conversion Real Time.** When this bit is set MADC indicates that conversion with real time constraints required by processor 1 is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical '0'.
EOCP1	**End Of Conversion Processor 1**. When this bit is set MADC indicates that conversion required by processor 1 is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical '0'.
BUSY	When this bit is set MADC is running its sequence of conversions.

	Note: this read only bit is common with the CTRL_P2 register, bit 0 (same signal).

14.4.4 RTCH1_LSB

Register	RTCH1_LSB	Channel 1 RT Conversion Result Register (ADCIN3)							
Page	0	Address	Dec # 48	Hex 0x30					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 1 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (i.e. during a Real Time conversion), the read value is H00

14.4.5 RTCH1_MSB

Register	RTCH1_MSB	Channel 1 RT Conversion Result Register (ADCIN3)							
Page	0	Address	Dec # 49	Hex 0x31					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04.
Bit [9:8]	Channel 1 result of conversion (2 MSBs)

14.4.6 RTCH2_LSB

Register	RTCH2_LSB	Channel 2 RT Conversion Result Register (ADCIN4 = BT)							
Page	0	Address	Dec # 50	Hex 0x32					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 2 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.7 RTCH2_MSB

Register	RTCH2_MSB	Channel 2 RT Conversion Result Register (ADCIN4 = BT)							
Page	0	Address	Dec # 51	Hex 0x33					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 2 result of conversion (2 MSBs)

14.4.8 RTCH3_LSB

Register	RTCH3_LSB	Channel 3 RT Conversion Result Register (ADCIN5 = BTEMP)							
Page	0	Address	Dec # 52	Hex 0x34					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 3 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.9 RTCH3_MSB

Register	RTCH3_MSB	Channel 3 RT Conversion Result Register (ADCIN5 = BTEMP)							
Page	0	Address	Dec # 53	Hex 0x35					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 3 result of conversion (2 MSBs)

14.4.10 RTCH4_LSB

Register	RTCH4_LSB	Channel 4 RT Conversion Result Register (USBVBUS)							
Page	0	Address	Dec # 54	Hex 0x36					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 4 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.11 RTCH4_MSB

Register	RTCH4_MSB	Channel 4 RT Conversion Result Register (USBVBUS)							
Page	0	Address	Dec # 55	Hex 0x37					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 4 result of conversion (2 MSBs)

14.4.12 RTCH5_LSB

Register	RTCH5_LSB	Channel 5 RT Conversion Result Register (VBKP)							
Page	0	Address	Dec # 56	Hex 0x38					
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 5 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.13 RTCH7_MSB

Register	RTCH5_MSB	Channel 5 RT Conversion Result Register (VBKP)							
Page	0	Address	Dec # 57	Hex 0x39					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 5 result of conversion (2 MSBs)

14.4.14 RTCH6_LSB

Register	RTCH6_LSB	Channel 6 RT Conversion Result Register (ICHG)							
Page	0	Address	Dec # 58	Hex 0x3A					
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 6 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.15 RTCH6_MSB

Register	RTCH6_MSB	Channel 6 RT Conversion Result Register (ICHG)							
Page	0	Address	Dec # 59	Hex 0x3B					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 6 result of conversion (2 MSBs)

14.4.16 RTCH7_LSB

Register	RTCH7_LSB	Channel 7 RT Conversion Result Register (VCHG)							
Page	0	Address	Dec # 60	Hex 0x3C					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 7 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.17 RTCH7_MSB

Register	RTCH7_MSB	Channel 7 RT Conversion Result Register (VCHG)							
Page	0	Address	Dec # 61	Hex 0x3D					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 7 result of conversion (2 MSBs)

14.4.18 RTCH8_LSB

Register	RTCH8_LSB	Channel 10 RT Conversion Result Register (VBAT)							
Page	0	Address	Dec # 62	Hex 0x3E					
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 8 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.19 RTCH8_MSB

Register	RTCH8_MSB	Channel 8 RT Conversion Result Register (VBAT)							
Page	0	Address	Dec # 63	Hex 0x3F					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 8 result of conversion (2 MSBs)

14.4.20 RTCH9_LSB

Register	RTCH9_LSB	Channel 9 RT Conversion Result Register (HOTDIE)							
Page	0	Address	Dec # 64	Hex 0x40					
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 9 result of conversion (8 LSBs). If COLLISION_RT bit is at '1' state (ie during a Real Time conversion), the read value is H00

14.4.21 RTCH9_MSB

Register	RTCH9_MSB	Channel 9 RT Conversion Result Register (HOTDIE)							
Page	0	Address	Dec # 65	Hex 0x41					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_RT	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_RT	**Collision Read Real Time:** this bit is set at '1' state when a Read operation occurs during an on going real time sequence of conversions (EOCRT control bit at '0' state): If COLLISION_RT is at '1' state, the read value is H04
Bit [9:8]	Channel 9 result of conversion (2 MSBs)

14.4.22 GPCH1_LSB

Register	GPCH1_LSB	Channel 1 GP Conversion Result Register (ADCIN3)							
Page	0	Address	Dec # 70	Hex 0x46					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 1 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (i.e. during an Asynchronous conversion), the read value is H00

14.4.23 GPCH1_MSB

Register	GPCH1_MSB	Channel 1 GP Conversion Result Register (ADCIN3)							
Page	0	Address	Dec # 71	Hex 0x47					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 1 result of conversion (2 MSBs)

14.4.24 GPCH2_LSB

Register	GPCH2_LSB	Channel 2 GP Conversion Result Register (ADCIN4 = BT)							
Page	0	Address	Dec # 72	Hex 0x48					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 2 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.25 GPCH2_MSB

Register	GPCH2_MSB	Channel 2 GP Conversion Result Register (ADCIN4 = BT)							
Page	0	Address	Dec # 73	Hex 0x49					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 2 result of conversion (2 MSBs)

14.4.26 GPCH3_LSB

Register	GPCH3_LSB	Channel 3 GP Conversion Result Register (ADCIN5 = BTEMP)							
Page	0	Address	Dec # 74	Hex 0x4A					
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 3 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.27 GPCH3_MSB

Register	GPCH3_MSB	Channel 3 GP Conversion Result Register (ADCIN5 = BTEMP)							
Page	0	Address	Dec # 75	Hex 0x4B					
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 3 result of conversion (2 MSBs)

14.4.28 GPCH4_LSB

Register	GPCH4_LSB	Channel 4 GP Conversion Result Register (USBVBUS)							
Page	0	Address	Dec # 76	Hex 0x4C					
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 4 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.29 GPCH4_MSB

Register	GPCH4_MSB	Channel 4 GP Conversion Result Register (USBVBUS)							
Page	0	Address	Dec # 77	Hex 0x4D					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 4 result of conversion (2 MSBs)

14.4.30 GPCH5_LSB

Register	GPCH5_LSB	Channel 5 GP Conversion Result Register (VBKP)							
Page	0	Address	Dec # 78	Hex 0x4E					
Bit	7	6	5	4	3	2	1	0	
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

Bit [7:0]	Channel 5 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.31 GPCH5_MSB

Register	GPCH5_MSB	Channel 5 GP Conversion Result Register (VBKP)							
Page	0	Address	Dec # 79	Hex 0x4F					
Bit	7	6	5	4	3	2	1	0	
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8	
Read/Write	R	R	R	R	R	R	R	R	
Reset_off	0	0	0	0	0	0	0	0	

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 5 result of conversion (2 MSBs)

14.4.32 GPCH6_LSB

Register	GPCH6_LSB	Channel 6 GP Conversion Result Register (ICHG)						
Page	0	Address	Dec # 80	Hex 0x50				
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 6 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.33 GPCH6_MSB

Register	GPCH6_MSB	Channel 6 GP Conversion Result Register (ICHG)						
Page	0	Address	Dec # 81	Hex 0x51				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 6 result of conversion (2 MSBs)

14.4.34 GPCH7_LSB

Register	GPCH7_LSB	Channel 7 GP Conversion Result Register (VCHG)						
Page	0	Address	Dec # 82	Hex 0x52				
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 7 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.35 GPCH7_MSB

Register	GPCH7_MSB	Channel 7 GP Conversion Result Register (VCHG)						
Page	0	Address	Dec # 83	Hex 0x53				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCRT control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 7 result of conversion (2 MSBs)

14.4.36 GPCH8_LSB

Register	GPCH8_LSB	Channel 8 GP Conversion Result Register (VBAT)						
Page	0	Address	Dec # 84	Hex 0x54				
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 8 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.37 GPCH8_MSB

Register	GPCH8_MSB	Channel 8 GP Conversion Result Register (VBAT)						
Page	0	Address	Dec # 85	Hex 0x55				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 8 result of conversion (2 MSBs)

14.4.38 GPCH9_LSB

Register	GPCH9_LSB	Channel 9 GP Conversion Result Register (HOT-DIE)						
Page	0	Address	Dec # 86	Hex 0x56				
Bit	7	6	5	4	3	2	1	0
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

Bit [7:0]	Channel 9 result of conversion (8 LSBs). If COLLISION_GP bit is at '1' state (ie during an Asynchronous conversion), the read value is H00

14.4.39 GPCH9_MSB

Register	GPCH9_MSB	Channel 9 GP Conversion Result Register (HOT-DIE)						
Page	0	Address	Dec # 87	Hex 0x57				
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	COLLISION_GP	Bit9	Bit8
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

COLLISION_GP	**Collision Asynchronous:** this bit is set at '1' state when a Read operation occurs during an on going asynchronous sequence of conversions (EOCP1 or EOCP2 control bit at '0' state): If COLLISION_GP is at '1' state, the read value is H04
Bit [9:8]	Channel 9 result of conversion (2 MSBs)

14.5 ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		-	10	-	Bit
MADC voltage reference		-	1.75	-	V
Differential nonlinearity		-2	-	2	LSB
Integral nonlinearity	Best fitting	-2	-	2	LSB
Input range		0	-	1.75	V
STARTADC pulse minimum duration	MADC period = T = 1/F	-	1*T	-	µs

PARAMETER		MIN	TYP	MAX	UNITS
Running frequency F		-	1	-	MHz
Clock period T = 1/F (duty cycle = 50/50)		-	1	-	µs
N = number of analog inputs to convert in a single sequence		0		10	
Tstart (depends on re-synchronization)	SP1 or SP2 asynchronous request	5*T	-	6*T	µs
	Real time STARTADC request	4*T	-	5*T	
Tsettling time is the time to wait before sampling a stale analog input. Tsettling is calculated from the max((Rs + Ron)*Cbank) of the 11 possible input sources (internal or external inputs). Ron is the resistance of the selection analog input switch.		-	16.5*T	-	µs
Tadc time is the ADC conversion time (3 phases: successive approximation operations, write converted data in register and auto reset)		-	9.5*T	-	µs
Tstop		2*T	-	3*T	µs
Total Sequence Conversion Time General Formula		Tstart + N*(tsettling +tadc)+Tstop			µs
Conversion Time: Sequence Of Only One conversion (N=1)		-	-	35*T	µs
Conversion Time: Full Sequence Of Conversions (N=11)		-	-	269*T	µs

PARAMETER	MIN	TYP	MAX	UNITS
Input capacitor Cbank	-	12	-	pF
Max Source Input Resistance Rs (for all 11 internal or external inputs)	-	-	100	kΩ
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
Power on consumption, Running frequency F = 1MHz		0.5		mA

Note: the consumption is given for a stand alone block.

Table 62 : Electrical Characteristics of the M-ADC

15 HOT-DIE FUNCTION AND THERMAL SHUTDOWN

T3031 contains a two-levels control and protection system capable to monitor the on-chip temperature and prevent the overall device from an uncontrolled increase of the junction-temperature (T_J).

15.1 HOT-DIE FUNCTION

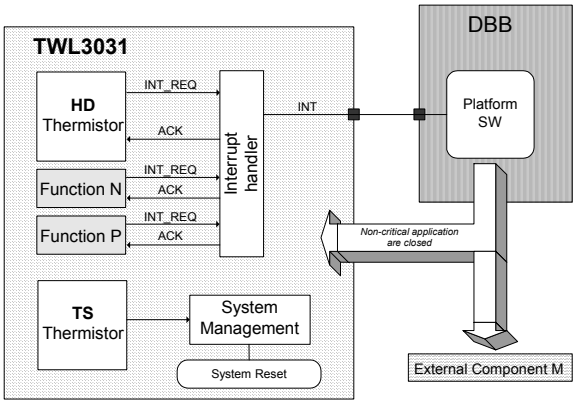
The Hot-Die function generates an interrupt to send to the modem processor through terminal P1_INT2. The junction-temperature threshold, which generates the interrupt, can be selected via register thus improving the flexibility of the system. The Hot-Die signal is a request to the software managing the platform to close non-critical applications in order to reduce the IC internal temperature thus preventing on-chip critical conditions.
The Hot-Die function integrated within T3031 provides host power management software with an early warning over-temperature condition. This monitoring system is connected to the interrupt controller and is capable to send an interrupt.
When an interrupt is triggered by the monitor, the hosts' power management software should take immediate action to reduce the amount of power drawn from T3031 device. If corrective action is not taken into account and die temperature still climbs, the second level of protection (thermal shutdown) will reset the device (if 170ºC junction temperature, nominal is reached, see below)

T3031 allows programming four different thresholds in order to increase the flexibility of the system: in nominal conditions, the threshold triggering the interrupt can be set from 145°C up to 160°C with 5°C-steps. The Hot-Die hysteresis is 10°C in typical conditions.

15.2 THERMAL SHUTDOWN

The Thermal Shutdown monitor function is integrated in T3031 to generate an immediate, unconditional reset to the T3031 device when an over-temperature condition exists. This function should not be confused with the early warning provided to software by the Hot-Die monitor function.
In T3031, the threshold (T_J rising) of the Thermal Shutdown is 170°C, nominal. The Thermal Shutdown hysteresis is 10°C in typical conditions.

Figure 38 : Hot-Die (HD) Function and Thermal Shutdown (TS)



15.3 THERMAL CHARACTERISTICS

Hot-Die Characteristics

THERM_HDSEL[1:0]	Threshold (nominal)
00 (1st Hot-Die threshold)	*Rising temp*: 152 deg
	Falling temp: 142 deg
01 (2nd Hot-Die threshold)	*Rising temp*: 158 deg
	Falling temp: 148 deg
10 (3rd Hot-Die threshold)	*Rising temp*: 162 deg
	Falling temp: 152 deg
11 (4th Hot-Die threshold)	*Rising temp*: 168 deg
	Falling temp: 157 deg

Thermal Shutdown Characteristics

Threshold (nominal)
Rising temp: 178 deg
Falling temp: 168 deg

Table 63 : Thermal Characteristics of the Hot-Die Function and the Thermal Shutdown

16 SIM-CARD DETECTION

16.1 FUNCTIONAL DESCRIPTION

T3031 provides the regulated supply voltage VRSIM for the SIM-card and the circuitry to detect the insertion or extraction of the SIM-Card in or from the mobile.
When the SIM-card is inserted, a mechanical contact connected on T3031 device terminal SIMDTC is tripped and after debouncing, an interrupt is generated. The SIM-card presence detection logic must be active even when the system is in idle mode. Thus, the debouncing logic is based on the 32-kHz low-activity clock. The debouncing time is programmable. The signal from SIMDTC is pre-processed depending on the detection system and on the internal pull-up/pull-down configuration.

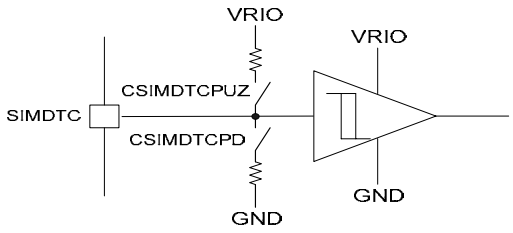


Figure 39 : SIM-card Detection System

16.2 REGISTERS

16.2.1 TOGGLE1

Register	TOGGLE1							
Page	0	Address	Dec # 104		Hex 0x68			
Bit	7	6	5	4	3	2	1	0
Name	SIMS	SIMR	USBDS	USBDR	VIBS	VIBR	MADCS	MADCR
Read/Write	W	W	W	W	W	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

SIMS	SIM-Card set signal (SIM-Card detection system enabled)
SIMR	SIM-Card reset signal (SIM-Card detection system disabled)
USBDS	USB (digital) set signal (USB digital enabled)
USBDR	USB (digital) reset signal (USB digital disabled)
VIBS	Vibrator driver set signal (Vibrator driver enabled)
VIBR	Vibrator driver reset signal (Vibrator driver disabled)
MADCS	M-ADC set signal (M-ADC enabled)
MADCR	M-ADC reset signal (M-ADC disabled)

16.2.2 PWDNSTATUS

Register	PWDNSTATUS							
Page	0	Address	Dec # 106		Hex 0x6A			
Bit	7	6	5	4	3	2	1	0
Name	USBA_ EN	WLEDC_ EN	WLEDB_ EN	WLEDA_ EN	SIM_ EN	USBD_ EN	VIB_ EN	MADCON
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

USBA_EN	USB (analog) enable status (active high)
WLEDC_EN	W-LEDC driver enable status (active high)
WLEDB_EN	W-LEDB driver enable status (active high)
WLEDA_EN	W-LEDA driver enable status (active high)
SIM_EN	SIM-Card driver enable status (active high)
USBD_EN	USB (digital) enable status (active high)
VIB_EN	Vibrator driver enable status (active high)
MADCON	M-ADC enable status (active high)

.

16.2.3 SIMDEBOUNCING

Register	SIMDEBOUNCING							
Page	0	Address	Dec # 139		Hex 0x8B			
Bit	7	6	5	4	3	2	1	0
Name	SINS_ DEB_3	SINS_ DEB_2	SINS_ DEB_1	SINS_ DEB_0	SEXT_ DEB_3	SEXT_ DEB_2	SEXT_ DEB_1	SEXT_ DEB_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

SINS_DEB [3:0]	SIM-card insertion de-bouncing time Code 0000: de-bouncing time 0.5ms (default state); Code 0001: de-bouncing time 1ms;

	… Code 1111: de-bouncing time 8ms. **Note**: insertion de-bouncing step is 0.5ms.
SEXT_DEB [3:0]	SIM-card extraction de-bouncing time Code 0000: de-bouncing time 0.5ms (default state); Code 0001: de-bouncing time 1ms; … Code 1111: de-bouncing time 8ms. **Note**: insertion de-bouncing step is 0.5ms.

16.2.4 SIMDTCCTRL

Register	SIMDTCCTRL							
Page	0	Address	Dec # 140		Hex 0x8C			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	SW_FC	CSIMDTC PUZ	CSIMDTC PD
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

SW_FC	SW_FC bit allows to configure the internal circuitry at the varying of the external mechanical contact: 0: insertion corresponds to an open-state of the external mechanical contact; 1: insertion corresponds to a close state of the external mechanical contact.
CSIMDTCPUZ	Pull-up enabled active low (mechanical contact between SIMDTC I/O and ground).
CSIMDTCPD	Pull-down enabled active high (mechanical contact between VRIO and SIMDTC I/O).

16.3 ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Debouncing time (SIM-card insertion)		0.5	-	8	ms
Time unit (SIM-card insertion)		-	0.5	-	ms
Debouncing time (SIM-card extraction)		0.5	-	8	ms
Time unit (SIM-card extraction)		-	0.5	-	ms
Pull-down resistor (resistor + resistive switch)		-	345	-	kΩ
Pull-up resistor (resistor + resistive switch)		-	475	-	kΩ

Table 64 : Electrical Characteristics of the SIM-Card

17 VIBRATOR MOTOR DRIVER

17.1 FUNCTIONAL DESCRIPTION

A LDO based vibrator motor driver has been embedded to drive an external vibrator motor. The output voltage of this regulator is programmable, based on a nominal 4-Hz cycle.
The output voltage level, which is controlled via register, can be 1.2V, 1.3V, 1.4V and 2.7V. The vibrator driver is capable to provide up to 75 mA.
The duty-cycle of the nominal 4-Hz frequency is controlled via register and can be 25%, 50%, 75% and 100%. This vibrator driver allows a soft turn-on (500µs max) and turn-off (2ms max).

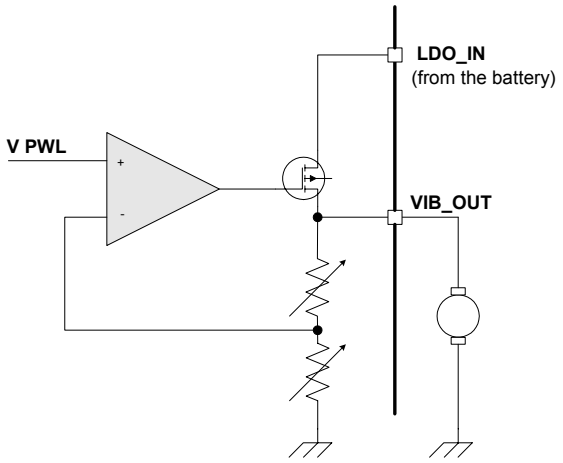


Figure 40 : Vibrator Motor Driver Block Scheme

17.2 REGISTERS

17.2.1 TOGGLE1

Register	TOGGLE1							
Page	0	Address	Dec # 104		Hex 0x68			
Bit	7	6	5	4	3	2	1	0
Name	SIMS	SIMR	USBDS	USBDR	VIBS	VIBR	MADCS	MADCR
Read/Write	W	W	W	W	W	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

SIMS	SIM-Card set signal (SIM-Card detection system enabled)
SIMR	SIM-Card reset signal (SIM-Card detection system disabled)
USBDS	USB (digital) set signal (USB digital enabled)
USBDR	USB (digital) reset signal (USB digital disabled)
VIBS	Vibrator driver set signal (Vibrator driver enabled)
VIBR	Vibrator driver reset signal (Vibrator driver disabled)
MADCS	M-ADC set signal (M-ADC enabled)
MADCR	M-ADC reset signal (M-ADC disabled)

17.2.2 PWDNSTATUS

Register	PWDNSTATUS							
Page	0	Address	Dec # 106		Hex 0x6A			
Bit	7	6	5	4	3	2	1	0
Name	USBA_ EN	WLEDC_ EN	WLEDB_ EN	WLEDA_ EN	SIM_ EN	USBD_ EN	VIB_ EN	MADCON
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

USBA_EN	USB (analog) enable status (active high)
WLEDC_EN	W-LEDC driver enable status (active high)
WLEDB_EN	W-LEDB driver enable status (active high)
WLEDA_EN	W-LEDA driver enable status (active high)
SIM_EN	SIM-Card driver enable status (active high)
USBD_EN	USB (digital) enable status (active high)
VIB_EN	Vibrator driver enable status (active high)
MADCON	M-ADC enable status (active high)

17.2.3 VIBCTRL

Register	VIBCTRL							
Page	0	Address	Dec # 109		Hex 0x6D			
Bit	7	6	5	4	3	2	1	0
Name	Not used	RSRVD	RSRVD	RSRVD	VSEL_1	VSEL_0	D_SEL_1	DSEL_0
Read/Write	-	R	R	R	R/W	R/W	R/W	R/W
Reset_off	-	0	1	1	1	1	1	1

Register bits description

RSVRD (bit 6 – bit 4)	Reserved bits
VSEL [1:0]	Output voltage level: 00: 1.2V (if VIB_EN is high) 01: 1.3V (if VIB_EN is high) 10: 1.4V (if VIB_EN is high)

	11: 2.7V (if VIB_EN is high) (default mode)
DSEL [1:0]	Duty-cycle selection for the internally derived 4-Hz clock: 00: duty-cycle=100% 01: duty-cycle=75% 10: duty-cycle=50% 11: duty-cycle=25% (default mode)

17.3 ELECTRICAL CHARACTERISTICS

VIB_ENABLE | VIB_VSEL[1:0]	Vout (nominal)	Iout (max)	Iddq (max)
000	0 (Off)	0	1µA
001	0 (Off)	0	1µA
010	0 (Off)	0	1µA
011	0 (Off)	0	1µA
100	Vout = 1.2V	75mA	20µA
101	Vout = 1.3V	75mA	20µA
110	Vout = 1.4V	75mA	20µA
111	Vout = 2.7V	75mA	20µA

VIB_DSEL[1:0]	Hardware Mode	Vout (nominal)
00	L_100	VIB duty cycle = 100%: When Vout>0, vibrator is on continuously
01	L_75	VIB duty cycle = 75%: When Vout>0, vibrator is on for 0.1875 seconds of every 0.25 seconds
10	L_50	VIB duty cycle = 50%: When Vout>0, vibrator is on for 0.125 seconds of every 0.25 seconds
11	L_25	VIB duty cycle = 25%: When Vout>0, vibrator is on for 0.0625 seconds of every 0.25 seconds

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Input Voltage (V_{IN})				2.9		4.2	V
Output Voltage	$2.9 < V_{IN} < 4.2V$ $0 < I_O < 75mA$	VIB_VSEL=	11 10 01 00		2.7 1.4 1.3 1.2		V
Output Voltage Accuracy				-3		+3	%
Ground Current (I_Q)	OFF ON, I_O=75mA max					1 20	µA
Output Current (I_O)	Normal Mode			0		75	mA
Short Circuit Current (Ios)	$V_{IN} = V_{MAX}$					250	mA
Load Regulation	V_{IN} = 3.6V, $0 < I_O <$ Imax					50	mV
Line Regulation	$2.9V < V_{IN} < 4.2V$, I_O = Imax					20	mV
T on, OFF to ON	VOUT = 2.7 V (within 5% of V_{OUT}) VOUT = 1.2 V (within 5% of V_{OUT})				15 7		µs
T off, ON to OFF	Output regulated voltage @ 2.7 V Output regulated voltage @ 1.2 V				0.5 0.2		ms
Vibrator load inductance					70		µH
Vibrator load resistance					40		ohm

Table 65 : Electrical Characteristics of the Vibrator Motor Driver

18 WHITE-LEDs DRIVERS

18.1 FUNCTIONAL DESCRIPTION

Three white-LEDs drivers are embedded within T3031.
The first one LED_A is dedicated for the screen backlight and can drive up to four white-LEDs in series.
The second one LED_B is dedicated for the keypad and can drive up to four white-LEDs in series.
The third one LED_C is dedicated for the auxiliary display and can drive up to four white-LEDs, but in typical conditions it drives two white-LEDs in series.
The three white-LEDs drivers series are fed by a dedicated DCDC step-up regulator VRWLED.

LED_A, LED_B and LED_C can drive from 1 up to 4 WLEDs in series (with the current limitations reported in Table 68). The drivers are capable to drive also other kind of LEDs.
The output power will be always **Pout = (N_leds x V_forward_MAX) x I_programmed**. Pout must respect the limitations reported in Table 67.
It is worth noting that the output regulated voltage is not constant: this voltage changes at the varying of (a) the LEDs number, (b) their forward voltage and (c) the programmed current.

The maximum current delivered by this white-LEDs drivers is 63.75mA, in order to have an average maximum current within each white-LED of 21.25mA . The 63.75mA are switched among the three series of LEDs as described in Figure 41 , the corresponding timing scheme is reported in Figure 42. Thus, each series of LEDs has a maximum average current per frame of 21.25mA (63.75mA/3). The frame period is $3 \times T_{CK}$. T_{CK} can be programmed via a register between 2ms and 6ms.

The current delivered to each series of white-LEDs is obtained from a dedicated 8-bit DAC-based system. The DAC does not present a classical structure, the current contribution related to the 4-MSBs is generated in a different mode compared to the one of the 4-LSBs. This approach allows to strongly reduce the area of the DAC. The current contribution related to the 4-MSBs is provided by a standard 4-bit current-mode DAC, while the 4-LSBs contribution is generated starting from a PWM signal that modulates a 4mA current level as indicated in Figure 43. Figure 44 shows the typical current shape during a generic conversion period.

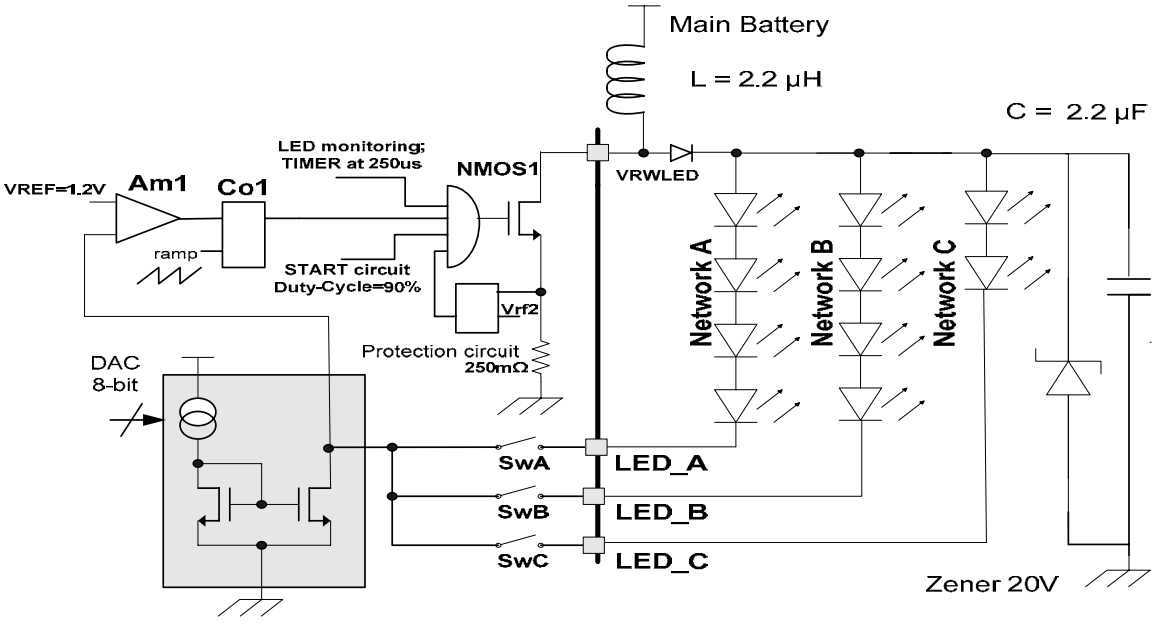


Figure 41 : White-LEDs Drivers (typical use-case, 4+4+2 white-LEDs)

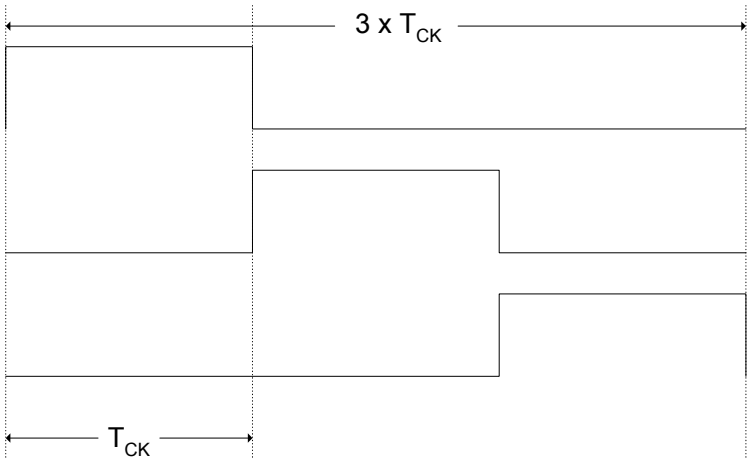


Figure 42 : Timing Scheme of the System

Input code number	Input code	Average current
255 (MAX)	11111111	21.25mA
254	11111110	21.17mA
…	…	…
240	11110000	20mA
239	11101111	19.92mA
…	…	…
15	00001111	1.25mA
14	00001110	1.17mA
13	00001101	1.08mA
12	00001100	1.00mA
11	00001011	0.92mA
10	00001010	0.83mA
9	00001001	0.75mA
8	00001000	0.67mA
7	00000111	0.58mA
6	00000110	0.50mA
5	00000101	0.42mA
4	00000100	0.33mA
3	00000011	0.25mA
2	00000010	0.17mA
1	00000001	0.83mA
0 (MIN)	00000000	0mA

Note: the values reported in this table correspond to the sum of the contributions of the 4-MSBs and of the 4-LSBs. As it will be detailed in the following, because of the particular architecture of the embedded DAC, the 4-MSBs will be specified with the related voltage levels (classical approach), while the 4-LSBs will be specified by construction providing the voltage level and the duty-cycles of the digital signal modulating the voltage level.

Table 66 : White-LEDs Drivers 8-bit DAC Input code , Output current

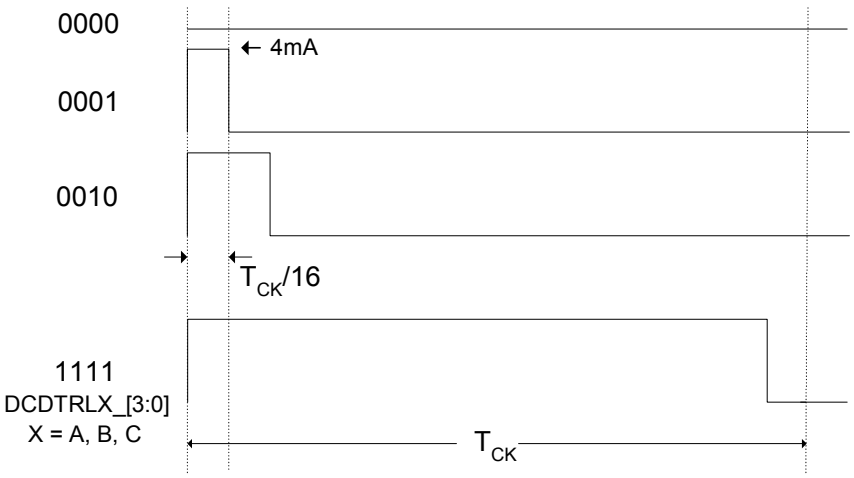


Figure 43 : PWM Signal (I_L contribution)

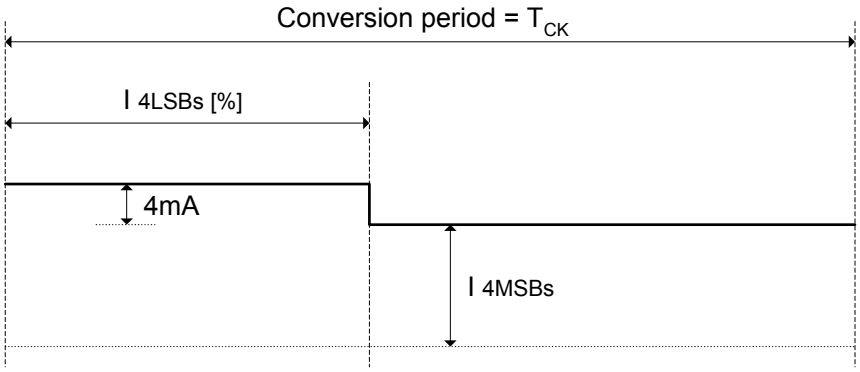


Figure 44 : Current Shape (I_M + I_L) During a Generic Conversion Period

The DCDC step-up is based on a control loop, which is composed of a start-up circuit and an amplifier Am1 in series with a comparator Co1, which is used when the wanted output voltage level is approximately achieved.
The current flowing in the white-LEDs networks is provided by the 8-bit DAC described in the previous paragraph.
The start-up circuit works with a 90%-duty-cycle of a 1-MHz clock to boost the VRWLED regulated voltage up to about 18V (4-white-LEDs case) or 10V (2-white-LEDs case) in about 500µs. The current drawn from the battery is limited at 400mA (in typical conditions) by a dedicated circuit, which is capable to sense the current flowing through power NMOS transistor (Max: 460 mA). This solution allows to limit current peaks on the battery during the start-up phase and each refresh period (when the leg to feed changes).The system is limited on $Pout_{max}$ Table 67 for different white-Leds numbers. The limitation of the max current through the legs at the varying of the Leds number (VBAT = 3.6V) is reported in Table 68

Another dedicated logic is capable to sense if one of the three white-LEDs series does not work properly (open circuit): this logic prevents the divergence of the circuit, forcing a low-voltage level on the gate of the power NMOS transistor in this case. During the normal operation, the NMOS transistors drivers which are part of the feedback system of the boost remain saturated with a nominal drain-to-source voltage closed to 1.2V.

VBAT	Pout 2 LEDs(mW)	Pout 3 LEDs(mW)	Pout 4 LEDs(mW)
5.5	586.5	873.3	824
5.4	586.5	831.6	834.24
5.2	586.5	812.5	767.97
5	586.5	799.8	710.73
4.8	586.5	755.22	645.84
4.6	586.5	683.2	572.76
4.4	586.5	637.2	523.26
4.2	586.5	606.9	487.92
4	586.5	583.1	457.8
3.8	586.5	535.5	424.65
3.6	586.5	468	377.4
3.4	586.5	425.5	330.75
3.3	586.5	401.082	304.5

Table 67 : White-LEDs , maximal output power

	Max current		
VBAT (V)	**2 LEDs (mA)**	**3 LEDs (mA)**	**4 LEDs (mA)**
3.6	Max (64)	40	25.5

Table 68 : White-LEDs , maximal current, VBAT = 3.6 V

Note: The performances of the white-LEDs driver are strongly dependent of the employed white-LEDs. All the data here reported has been obtained using NSCW310 white-LEDs (3.5 x 2.8 mm white-LEDs)

18.2 REGISTERS

18.2.1 TOGGLE2

Register	TOGGLE2							
Page	0	Address	Dec # 105		Hex 0x69			
Bit	7	6	5	4	3	2	1	0
Name	USBAS	USBAR	WLEDCS	WLEDCR	WLEDBS	WLEDBR	WLEDAS	WLEDAR
Read/Write	W	W	W	W	W	W	W	W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

USBAS	USB (analog) set signal (USB analog enabled)
USBAR	USB (analog) reset signal (USB analog disabled)
WLEDCS	W-LEDC driver set signal (W-LEDC driver enabled)
WLEDCR	W-LEDC driver reset signal (W-LEDC driver disabled)
WLEDBS	W-LEDB driver set signal (W-LEDB driver enabled)
WLEDBR	W-LEDB driver reset signal (W-LEDB driver disabled)
WLEDAS	W-LEDA driver set signal (W-LEDA driver enabled)
WLEDAR	W-LEDA driver reset signal (W-LEDA driver disabled)

18.2.2 PWDNSTATUS

Register	PWDNSTATUS							
Page	0	Address	Dec # 106		Hex 0x6A			
Bit	7	6	5	4	3	2	1	0
Name	USBA_ EN	WLEDC_ EN	WLEDB_ EN	WLEDA_ EN	SIM_ EN	USBD_ EN	VIB_ EN	MADCON
Read/Write	R	R	R	R	R	R	R	R
Reset_off	0	0	0	0	0	0	0	0

Register bits description

USBA_EN	USB (analog) enable status (active high)
WLEDC_EN	W-LEDC driver enable status (active high)
WLEDB_EN	W-LEDB driver enable status (active high)
WLEDA_EN	W-LEDA driver enable status (active high)
SIM_EN	SIM-Card driver enable status (active high)
USBD_EN	USB (digital) enable status (active high)
VIB_EN	Vibrator driver enable status (active high)
MADCON	M-ADC enable status (active high)

18.2.3 WLEDCTRL_LEDA

Register	WLEDCTRL_LEDA							
Page	0	Address	Dec # 113		Hex 0x71			
Bit	7	6	5	4	3	2	1	0
Name	DACINA_3	DACINA_2	DACINA_1	DACINA_0	DC CTRLA_3	DC CTRLA_2	DC CTRLA_1	DC CTRLA_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

DACINA [3:0]	4-MSBs of the 8-bit DAC for the LED A driving current (I_M) DACINA_[3:0]= 0000: 0-mA DACINA_[3:0]= 0001: 4-mA …

	DACINA_[3:0]= 1111: 60-mA
DCCTRLA [3:0]	4-LSBs of the 8-bit DAC for the LED A driving current (I_L): Duty-Cycle control DCCTRLA_[3:0]= 0000: 0% (0 of 1 MSB) 0 mA DCCTRLA_[3:0]= 0001: 6.25% (1/16 of 1 MSB) 0.25 mA … DCCTRLA_[3:0]= 1111: 93.75% (15/16 of 1 MSB) 3.75 mA

18.2.4 WLEDCTRL_LEDB

Register	WLEDCTRL_LEDB							
Page	0 Address	Dec # 114		Hex 0x72				
Bit	7	6	5	4	3	2	1	0
Name	DACINB_3	DACINB_2	DACINB_1	DACINB_0	DC CTRLB_3	DC CTRLB_2	DC CTRLB_1	DC CTRLB_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

DACINB [3:0]	4-MSBs of the 8-bit DAC for the LED B driving current (I_M) DACINB_[3:0]= 0000: 0-mA DACINB_[3:0]= 0001: 4-mA … DACINB_[3:0]= 1111: 60-mA
DCCTRLB [3:0]	4-LSBs of the 8-bit DAC for the LED B driving current (I_L): Duty-Cycle control DCCTRLB_[3:0]= 0000: 0% (0 of 1 MSB) 0 mA DCCTRLB_[3:0]= 0001: 6.25% (1/16 of 1 MSB) 0.25 mA … DCCTRLB_[3:0]= 1111: 93.75% (15/16 of 1 MSB) 3.75 mA

18.2.5 WLEDCTRL_LEDC

Register	WLEDCTRL_LEDC							
Page	0 Address	Dec # 115		Hex 0x73				
Bit	7	6	5	4	3	2	1	0
Name	DACINC_3	DACINC_2	DACINC_1	DACINC_0	DC CTRLC_3	DC CTRLC_2	DC CTRLC_1	DC CTRLC_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

DACINC [3:0]	4-MSBs of the 8-bit DAC for the LED C driving current (I_M) DACINC_[3:0]= 0000: 0-mA DACINC_[3:0]= 0001: 4-mA … DACINC_[3:0]= 1111: 60-mA
DCCTRLC [3:0]	4-LSBs of the 8-bit DAC for the LED C driving current (I_L): Duty-Cycle control DCCTRLC_[3:0]= 0000: 0% (0 of 1 MSB) 0 mA DCCTRLC_[3:0]= 0001: 6.25% (1/16 of 1 MSB) 0.25 mA … DCCTRLC_[3:0]= 1111: 93.75% (15/16 of 1 MSB) 3.75 mA

18.2.6 WLEDCTRL

Register	WLEDCTRL							
Page	0	Address	Dec # 116		Hex 0x74			
Bit	7	6	5	4	3	2	1	0
Name	WLED SWFREQ_ 1	WLED SWFREQ_ 0	DAC_IREF _CTRL	TIMER_ CTRL_3	TIMER_ CTRL_2	TIMER_ CTRL_1	TIMER_ CTRL_0	RSRVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset_off	1	0	0	0	1	0	0	0

Register bits description

WLEDSWFREQ[1:0]	These two bits set the switching frequency of the current flowing through the WLEDs. Code 11: Reserved code Code 10: current switched any 2ms (default mode) ➔ 168-Hz Code 01: current switched any 3ms ➔ 112-Hz Code 00: current switched any 6ms ➔ 56-Hz
DAC_IREF_CTRL	It sets the path of the reference current for the 8-bit DAC. 0: Reference current is generated by the on-chip current reference generator (based on the external reference resistor at node IREF 1: Reference current is generated by a dedicated V-to-I converter (reference input voltage is the on-chip bandgap reference)
TIMER_CTRL [3:0]	White-LEDs monitoring timer control bits: they control the status of each WLEDs network. In case the circuit has not properly started (after the programmed time), this timer stops driving the network that does not work correctly. This action is taken after the time programmed in the register (see the following values). Code 0000: 125μs (MIN value) Code 0001: 125 μs + 31 μs (MIN value + step) Code 0100: 250 μs (default code) Code 1111: 593 μs (MAX value)
RSRVD (bit 0)	Reserved bit, must remain always at the reset value 0.

Note: If the bit 0 is set to a value different from the reset status, the overall consumption of T3031 can increase and the IC can be permanently damaged.

18.3 ELECTRICAL CHARACTERISTICS

L = 2.2 µH ± 20% RDC max = 100 mΩ, C = 2.2 µF ± 20% , Zener 20V Iz typ = 5mA (min: 4mA, max: 10mA) Pd typ = 0.3W (min: 0.25W, max: 0.5W)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
WLED current related to the 4-MSBs	code: 00000000		0		mA
Code 00000000 : MIN 4-MSBs code	code: 00010000		4		mA
Code 00010000 : 4-MSBs step	code: 11110000		60		mA
Code 11110000 : MAX 4-MSBs code	0000 (0/16)		0		mA
	0001 (1/16)		0.25		
	0010 (2/16)		0.5		
	0011 (3/16)		0.75		
	0100 (4/16)		1		
	0101 (5/16)		1.25		
	0110 (6/16)		1.5		
	0111 (7/16)		1.75		
	1000 (8/16)		2		
	1001 (9/16)		2.25		
	1010 (10/16)		2.5		
	1011 (11/16)		2.75		
	1100 (12/16)		3		
	1101 (13/16)		3.25		
	1110 (14/16)		3.5		
	1111 (15/16)		3.75		

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LED A,B,C output level when selected			1.2		V
Matching of the current among the three drivers					
Driver *i* – Driver *j* (*i*, *j* = A, B, C)	4 WLEDs in both network *i* and *j*		1.5%		
Driver *i* – Driver *j* (*i*, *j* = A, B, C)	4 WLEDs in network *i(j)*, 2 WLEDs in network *j(i)*		2.8%		

Tantal capacitor: 2.2 µF ± 20% , VR = 25 V (rated voltage ≤ 85ºC) , VC = 17 V (category voltage ≤ 125ºC), Temperature range: -40ºC ≤ T ≤ 125ºC

Table 69 : Electrical Characteristics of the White-LEDs Drivers

19 REGISTER MAP DESCRIPTION

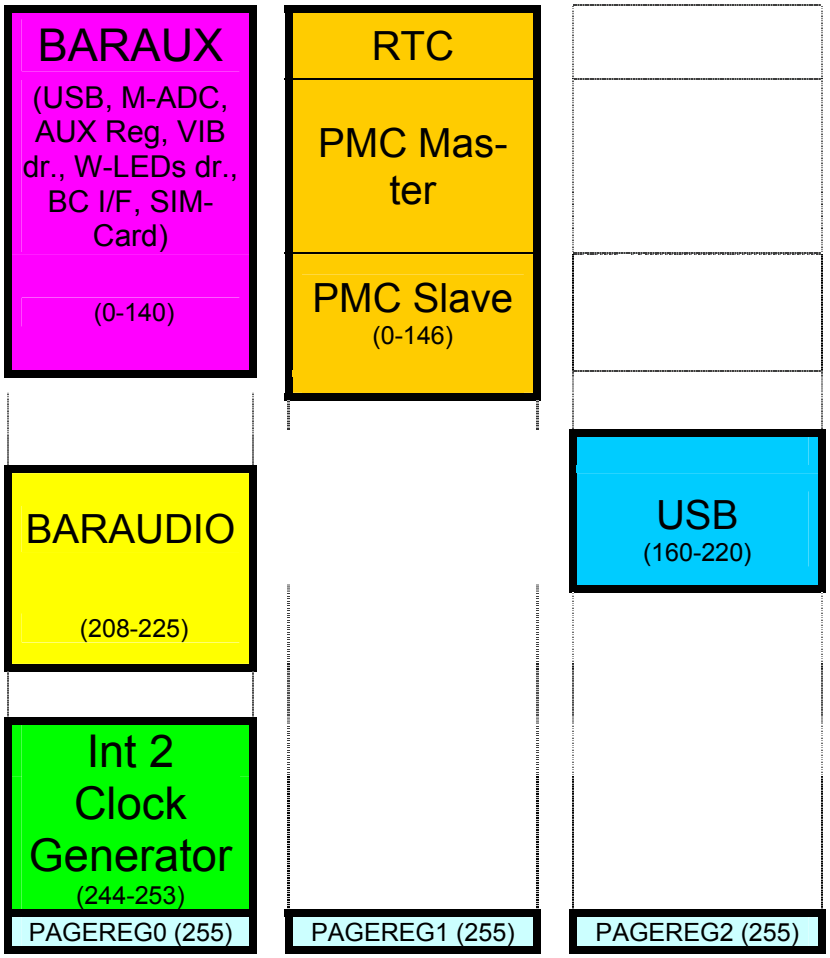


Figure 45 : Register Map

PAGEREG(0123)

Register	**PAGEREG**							
Page	**0/1/2/3**	Address	**Dec # 255**		**Hex 0xFF**			
Bit	7	6	5	4	3	2	1	0
Name	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	RSVRD	PAGE_ BIT_1	PAGE_ BIT_0
Read/Write	R	R	R	R	R	R	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0

Register bits description

RSVRD (bit 7 – bit 2)	Reserved bits
PAGE_BIT [1:0]	These bits define the current page following the table: 00 ➔ Page 0 01 ➔ Page 1 10 ➔ Page 2 11 ➔ Reserved

20 I²C

20.1 T3031 DATA FORMAT

Within T3031, all registers are “byte addressed”. Each byte has its own address. T3031 I²C address is hardcoded to **0x2D.**

The internal memory is organized in 4 pages that can be selected using a dedicated PAGE register. Each page contains 256 bytes and thus T3031 holds a maximum of 1024 addressable bytes.

8bits registers are accessed through the I²C providing the address byte first then the data byte.
16 bits registers are considered as two 8 bits registers. However they can be accessed trough the I²C using 1 single address , the one of the LSByte, the address of the MSByte will be generated internally automatically.

20.2 WRITE OPERATION

Write operations are initiated by a START condition, controlled by the master. Data transfers are composed of minimum 3 bytes (for 8bits registers). The first byte being sent by the master is the device address. When detecting a match with its own address (address of T3031 I²C interface), T3031 will generate an acknowledge (ACK bit) meaning that T3031 is in active mode. Following this byte, the master sends another address byte, which is this time, the address of the internal register being accessed. Then, the master sends 1 data byte containing the register data and ends the transmission by generating a STOP condition. All bytes being sent are acknowledged by TRITON Lite.

If, during a write access, the internal OCP bus is busy, the interface will force the connected host in wait state by pulling down the SCL line until the bus is freed up. This clock stretching technique is part of the I²C protocol.

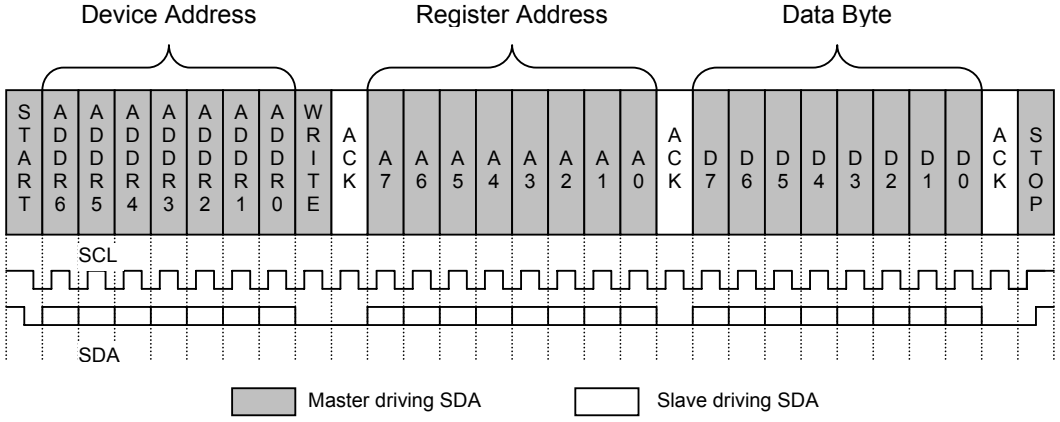


Figure 46 : I²C 8bits Write Access

16 bits write accesses are handled internally as 2 consecutive 8 bits accesses except that the address for the 2nd data byte is generated automatically. Indeed, the data LSByte is written at the address (@) provided by the *Register Address* byte of the I²C access and the MSByte is written at the address (@+1) (which is generated internally). There is no need to provide a second *Register Address* byte for the MSByte of data. Each internal access (write to register) is done during the ACK phase of the I²C. Therefore, for a 16bits write access, there will be 2 internal write accesses, one during the ACK phase of the LSByte, and the other during the ACK phase of the MSByte.

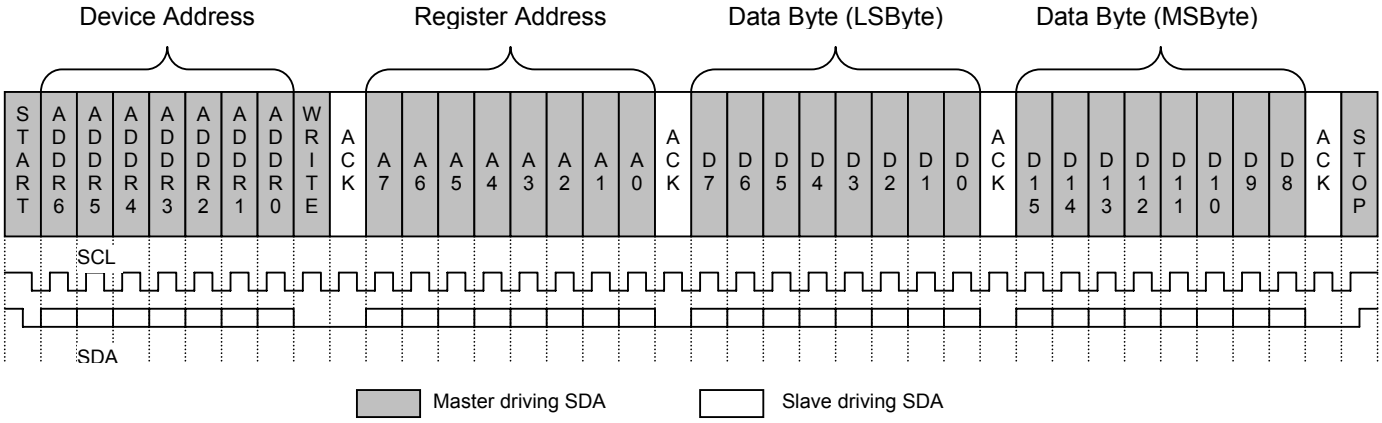


Figure 47 : I²C 16bits Write Access

T3031 also supports write burst accesses with a maximum of 256 consecutives bytes (maximum possible without having to change the internal page). First byte will be written at the address (@) provided by the *Register Address* byte of the I²C access, and the following data bytes will be written at the addresses (@+n) where *n* corresponds to the position of the data byte within the I²C frame. Each new incoming data byte gets its internal destination address generated automatically by incrementing the previous address by 1. When reaching 256 (maximum address range within 1 single page) the internally generated address will loop back to 0, remaining on the same page. Each internal access (write to register) is executed during the ACK phase of the I²C frame.

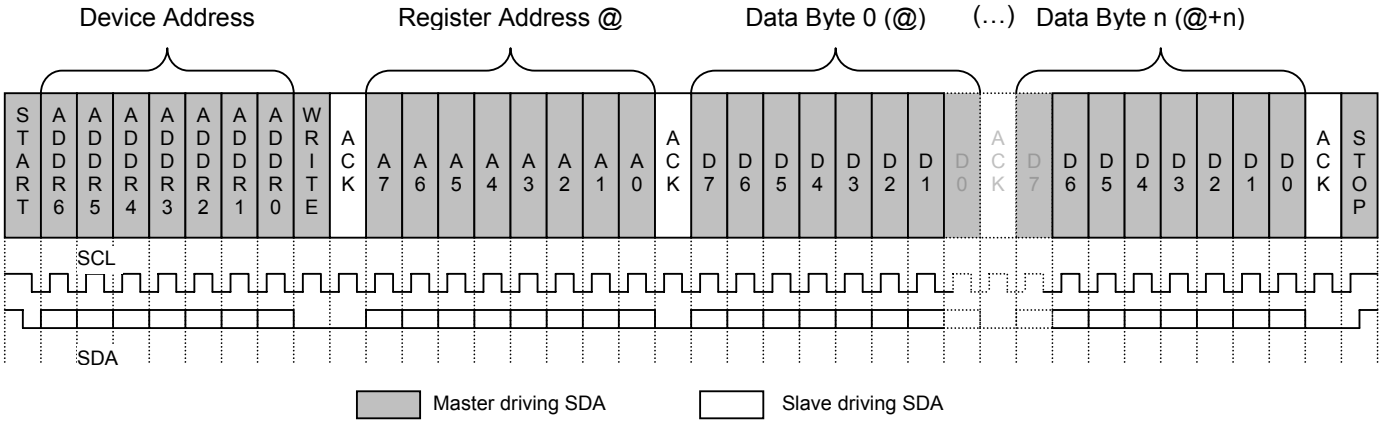


Figure 48 : I²C Burst Write Access

20.3 READ OPERATION

Read operations are composed of 2 consecutive accesses including a Repeat START condition. Since registers are identified through the pair "Device Address + Register Address", a simple read access to the Device Address only would not reach the desired register. Therefore, T3031 needs to have a first (write) access where the Register Address is specified in order to fill-in the read output buffer. Then, on the following read access, the read value is returned on the SDA line. Read operation can be viewed as a write operation without data followed by a read operation.
It is important that the 2 consecutives operations are not separated (do not use a "START STOP START STOP" sequence instead of a START Repeat_START STOP sequence). This condition is mandatory to avoid re-arbitration of the I^2C bus in the middle of a read operation.
After the third ACK bit, when retrieving the data from the register, T3031 might put the master in wait-state by pulling down the SCL line in order to have enough time to fetch the data from the register before loading the output buffer (specially in case where the OCP bus is busy).

For 8 bits read accesses, the data byte being output, following the 2nd *Device Address* byte corresponds to the data hold (read) in the register specified by the *Register Address* byte

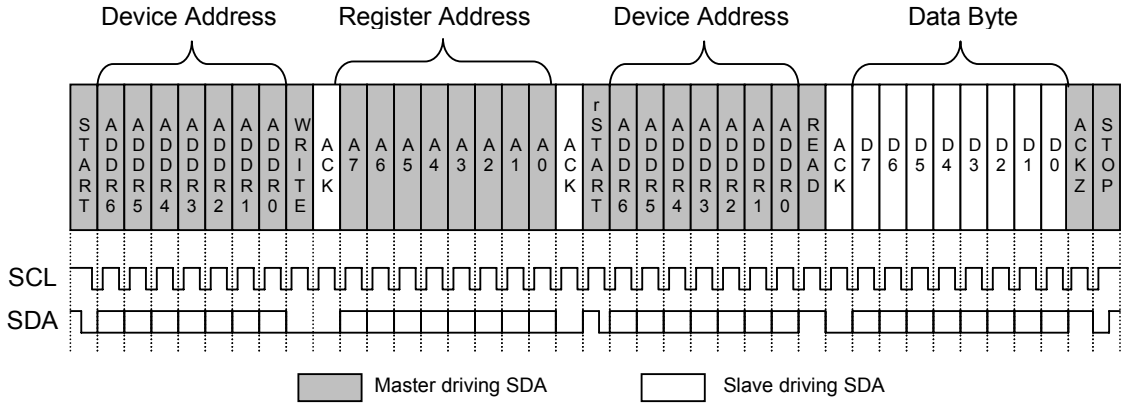


Figure 49 : I^2C 8bits Read Access

For 16 bits read accesses, the first data byte being output corresponds to the data hold (read) in the register specified by the *Register Address* byte (@). The 2nd data byte corresponds to the register located at the address (@+1).

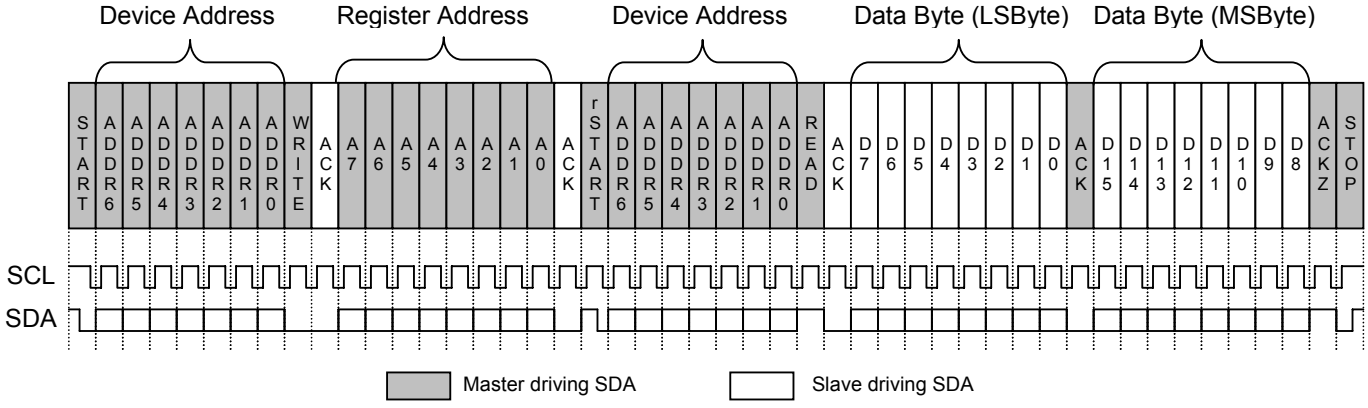


Figure 50 : I^2C 16bits Read Access

T3031 also supports burst read accesses with a maximum of 256 consecutives bytes (maximum possible without having to change the internal page). First byte will be read at the address (@) provided by the *Register Address* byte of the I²C access, and the following data bytes will be read at the addresses (@+n) where *n* corresponds to the position of the data byte within the I²C frame. Each new output data byte gets its internal address generated automatically by incrementing the previous address by 1. When reaching 256 (maximum address range within 1 single page) the internally generated address will loop back to 0, remaining on the same page. Each internal access (read to register) is executed during the ACK phase of the I²C frame.

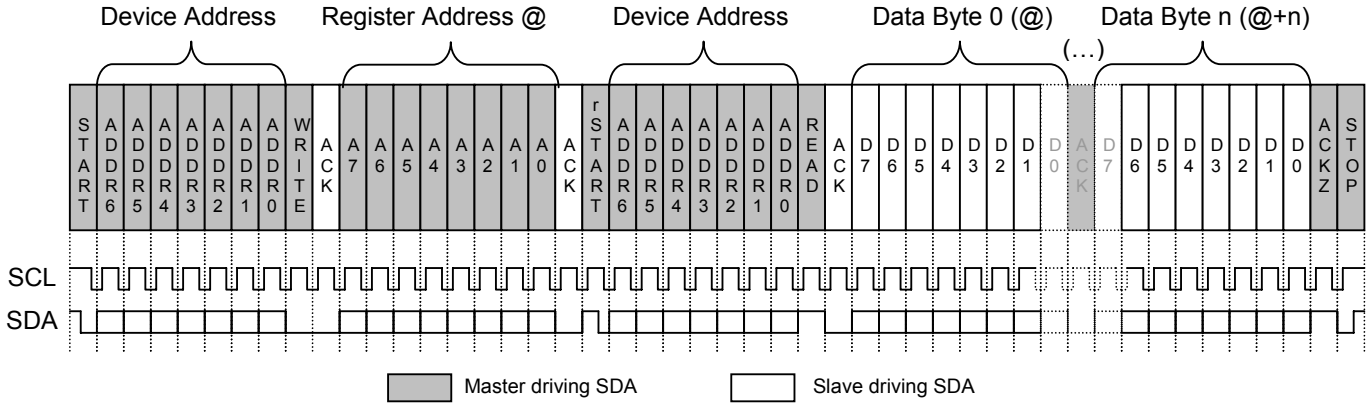


Figure 51 : I²C Burst Read Access

20.4 I²C DEVICE ADDRESS CONFIGURATION

T3031 I²C device address (0x2D) cannot be changed using a hardware external pull-up or pull-down. However there is the possibility to change this device address using the following custom General Call access:

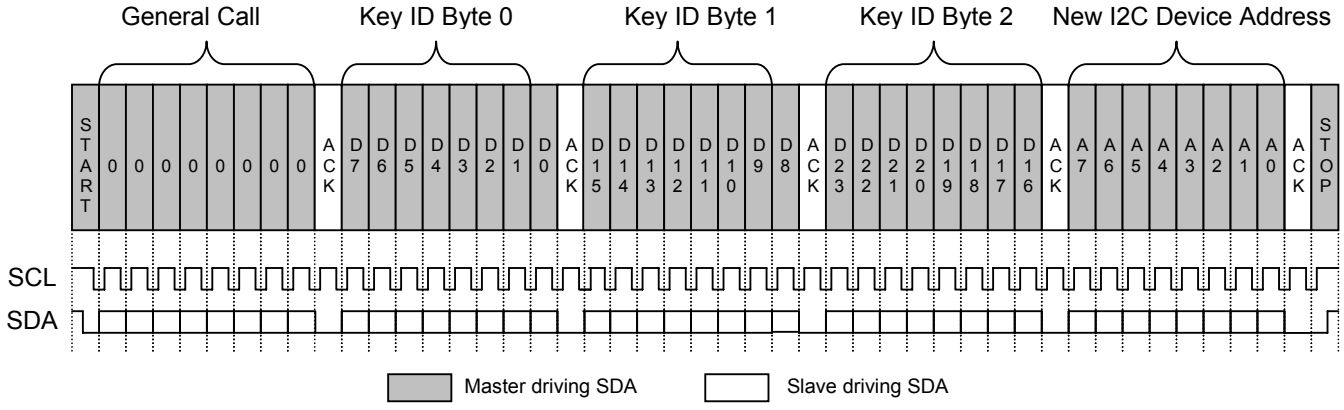


Figure 52 : I²C Device address configuration

The 24-bits key is composed of the 16bits Part Number (Byte 1 and Byte 2) and the 8 LSBits (Byte 0) of the 11bits Manufacturer Identity of the JTAG IDCODE. When this 24-bits key matches the JTAG IDCODE values, then the internal I²C device address is updated with the next byte being input on the interface

20.5 TIMINGS CHARACTERISTICS

Parameter	STANDARD Mode		FAST Mode		Units
	Min	Max	Min	Max	
SCL Clock Frequency	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	0.6	-	µs
LOW period of the SCL clock	4.7	-	1.3	-	µs
HIGH period of the SCL clock	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	4.7	-	0.6	-	µs
Data hold time	0 [2]	3.45 [3]	0 [2]	0.9 [3]	µs
Data set-up time	250	-	100 [4]	-	ns
Rise time of both SDA and SCL signals	-	1000	$20 + 0.1C_b$ [1]	300	ns
Fall time of both SDA and SCL signals	-	300	$20 + 0.1C_b$ [1]	300	ns
Set-up time for STOP condition	4.0	-	0.6	-	µs
Bus free time between a STOP and a START condition	4.7	-	1.3	-	µs
Capacitive load for each bus line (C_b)	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including Hysteresis)	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
Noise margin at the HIGH level for each connected device (including Hysteresis)	$0.2V_{DD}$	-	$0.2V_{DD}$	-	V

(1) C_b = capacitance of the bus line in pF.
(2) T3031 must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(3) The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(4) A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does not stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,MAX} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification).

Table 70 : I^2C Timing Characteristics

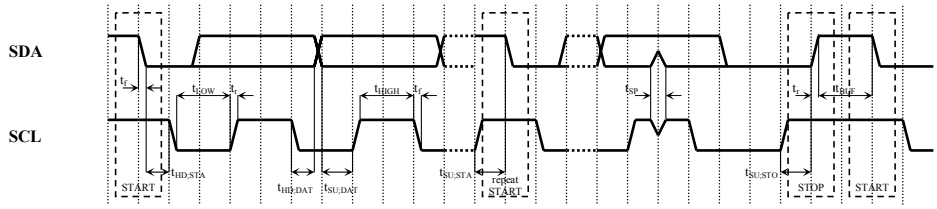


Figure 53 : I^2C Fast and Standard Mode Timing Diagram

21 JTAG

21.1 GENERAL DESCRIPTION

This interface uses the four dedicated I/O's pins TMS, TCK, TDI and TDO. The inputs TMS, TCK and TDI contain a pull-up device, which makes their state high when they are not driven. The output TDO is a 3-state output, which is Hi-Z except when data are shifted between TDI and TDO.

- TCK is the test clock signal.
- TMS is the test mode select signal.
- TDI is the scan path input.
- TDO is the scan path output.

The JTAG operations are controlled by a state machine that follows the JTAG state diagram. This state machine is reset by T3031 internal POR. A test mode is selected by writing a 6-bit word (Instruction) into the instruction register and then accessing the related data register.

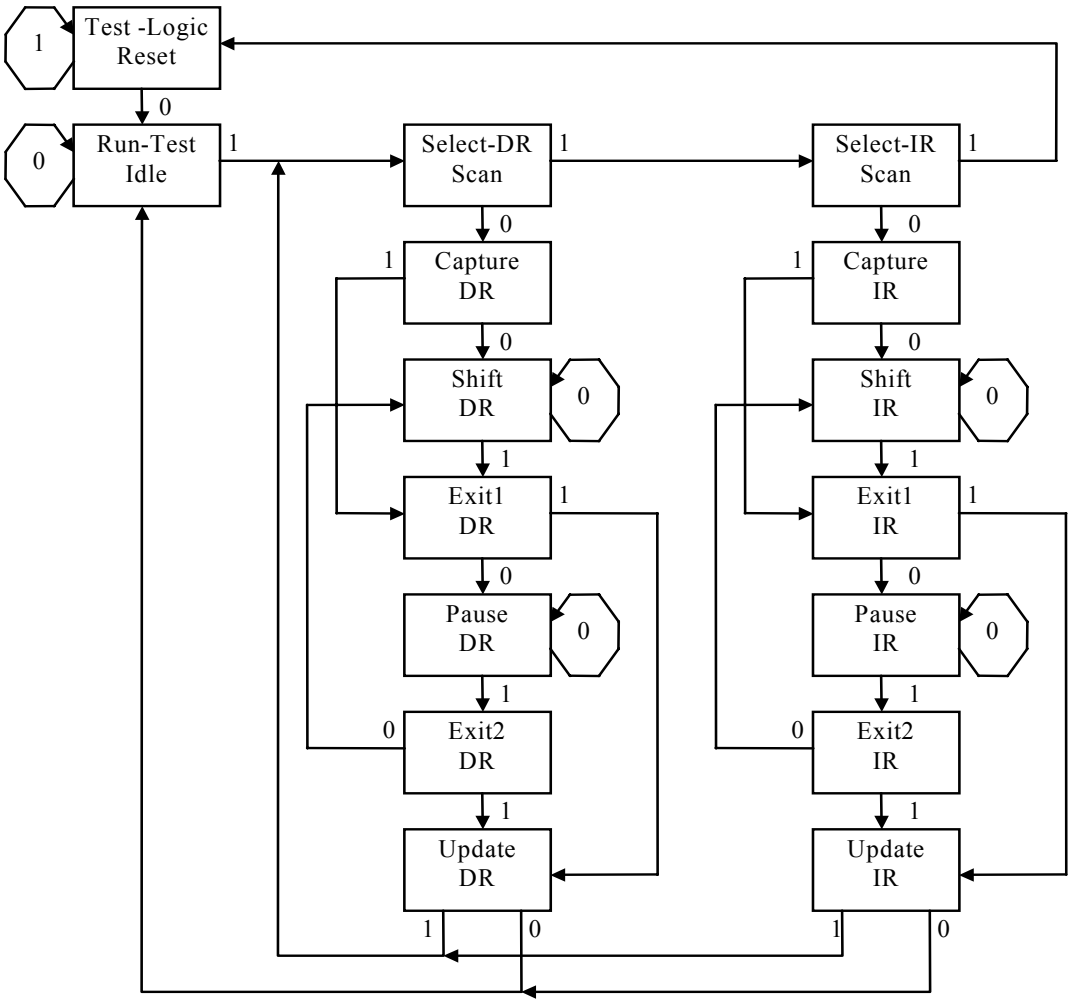


Figure 54 : JTAG State Diagram

The write operation to the instruction register (IRREG) is achieved through the following steps:
The instruction shift register is connected between TDI and TDO pins. Therefore, in order to shift-in an instruction, a correct bit stream must be input on TMS pin, to change the JTAG FSM state to SIR (Shift Instruction Register). And then shift-in the 6-bit instruction through TDI input. The instruction register (IRREG) is updated (parallel load from the instruction shift register to the instruction register) during the UPIR state (Update Instruction Register). Then a data register (DRREG) is selected and via the same protocol is written to actually enable the test mode.

21.2 PUBLIC INSTRUCTIONS

As defined in IEEE Std1149.1a the TAP contains the public instructions, which are described in the following table:

NAME	OPCODE	DESCRIPTION
BYPASS	111111	Connects the by-pass register between TDI and TDO
SAMPLE/ PRELOAD	000010	Connects the boundary scan register between TDI & TDO. This mode allows capturing a snapshot of the state of the I/O's of the device.
EXTEST	000000	Connects the boundary scan register between TDI & TDO. This mode allows to capture the state of the inputs pins and to force the state of the output pins. (For example it can be used for printed circuit board connections test)
IDCODE	000001	Connects the identification register between TDI and TDO. This is the default configuration at reset. The identification register's content is **0x5008D02F**.
INTEST	001001	Connects the boundary scan register between TDI & TDO. This mode allows to force the internal system input signals via the parallel latches of the boundary register and to capture internal system outputs. (This mode can be used for device internal test independently of the state of its input pins).
HIGHZ	000100	Forces all outputs and/or inouts in highz state
CLAMP	000011	Connects bypass register between TDI & TDO while maintaining previous state on boundary (i.e. PRELOAD)

Table 71 : Public Instructions

Once the test mode is selected among the standard public instructions it then involves 3 scan registers:

- The boundary scan register is inserted between the physical boundary (pins) and the system boundary (internal signals). It is mainly intended for test at board level, allowing capture of input pin state, force of output pin state, force of internal input signal and capture of internal output signals (depending on the selected test mode: SAMPLE / PRELOAD, EXTEST or INTEST). These features allow to check board connectivity between devices (EXTEST) or to activate internally the device, independently of the state of its input pins (INTEST).

- The identification register contains the 32-bit Identification code of the device.

- The bypass register is used to access to test data registers in other components on a board-level test data path.

These scan registers are reset by T3031 internal POR, and/or during the 'Test-Logic-Reset' state from the state machine.

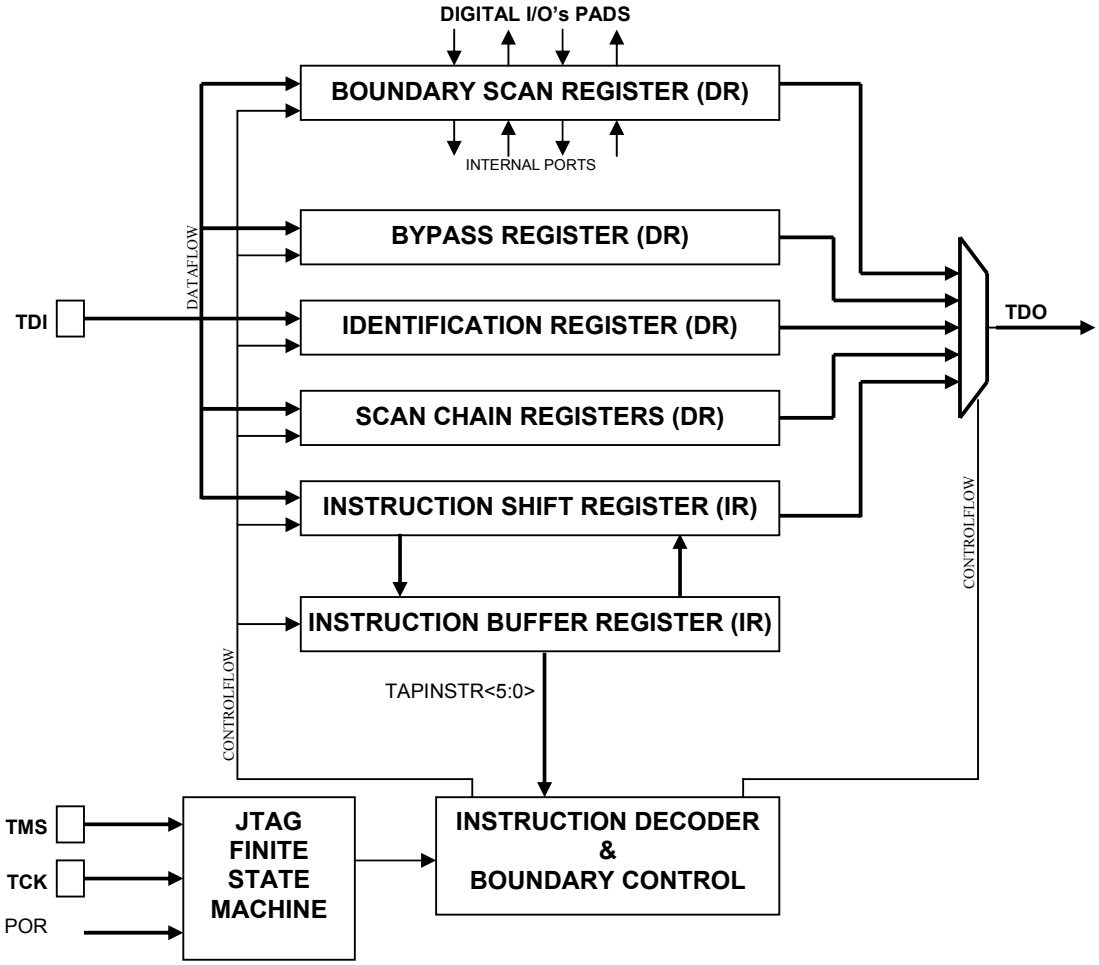


Figure 55 : TAP Block Diagram

21.3 BOUNDARY SCAN

Boundary scan chain is accessed through TDI-TDO using the following instructions:

- Sample/Preload
- Intest
- Extest

VSP_VDX is the last cell of the scan chain (just before TDO), and P1_INT2 is the first cell of the scan chain, right after TDI.

Cells named "*" are control cells for tri-state output. They refer to the previous cell in the scan chain. For example, cell number 1 is the control cell for output pin VSP_VDX (cell number 0).

Cells described as observe_only are just capture cells (Input/Output cannot be controlled).

Cell Number	Cell Name	Cell Description	Pin Type
0	VSP_VDX	Output (tri-state)	Digital
1	*	Control	Digital
2	VSP_VCK	Output (tri-state)	Digital
3	*	Control	Digital
4	VSP_VDR	Input	Digital
5	VSP_VFS	Output (tri-state)	Digital
6	*	Control	Digital
7	I2S_SDR	Input	Digital
8	I2S_SDX	Output (tri-state)	Digital
9	*	Control	Digital
10	I2S_SCK	Output	Digital
11	I2S_WS	Output	Digital
12	SDA1	Input	Digital
13	SDA1	Output	Digital
14	SCL1	Input	Digital
15	SCL1	Output	Digital
16	BM_SEL	Input (observe_only)	Digital
17	STARTADC	Input	Digital
18	SIMDTC	Input	Digital
19	MCLK1	Input	Digital
20	Not Connected	Input	Digital
21	WAKEUP1	Input	Digital
22	ONNOFF	Output	Digital
23	Not Connected	Output	Digital
24	Not Connected	Input	Digital
25	PCLKREQ	Input	Digital
26	Not Connected	InOut (observe_only)	Digital
27	CLK32KOUT	Output	Digital
28	TESTRESET	Input (observe_only)	Digital
29	Not Connected	Output (observe_only)	Digital
30	Not Connected	InOut (observe_only)	Digital

31	CKEN	Output	Digital
32	REGEN	Output (observe_only)	Digital
33	ICTLUSB2	Output (observe_only)	Digital
34	ICTLAC2	Output (observe_only)	Digital
35	ADCIN5	InOut (observe_only)	Analog
36	ADCIN4	InOut (observe_only)	Analog
37	ADCIN3	InOut (observe_only)	Analog
38	Not Connected	InOut (observe_only)	Analog
39	Not Connected	InOut (observe_only)	Analog
40	SE0_VM_TXD	Input	Digital
41	SE0_VM_TXD	Output	Digital
42	*	Control	Digital
43	RCV	Input	Digital
44	RCV	Output	Digital
45	*	Control	Digital
46	DAT_VP_RXD	Input	Digital
47	DAT_VP_RXD	Output	Digital
48	*	Control	Digital
49	OE_INTN	Input	Digital
50	OE_INTN	Output	Digital
51	*	Control	Digital
52	FML	Input (observe_only)	Analog
53	AUXI_FMR	Input (observe_only)	Analog
54	HSMIC	Input (observe_only)	Analog
55	AUDVMID	InOut (observe_only)	Analog
56	MICIN	Input (observe_only)	Analog
57	MICIP	Input (observe_only)	Analog
58	MICBIAS	Output (observe_only)	Analog
59	HSMICBIAS	Output (observe_only)	Analog
60	HSOR	Output (observe_only)	Analog
61	HSOVMID	Output (observe_only)	Analog
62	HSOL	Output (observe_only)	Analog
63	Not Connected	Output (observe_only)	Analog
64	EARN	Output (observe_only)	Analog
65	EARP	Output (observe_only)	Analog
66	Not Connected	Output	Digital
67	P1_INT2	Output	Digital

Table 72 : Boundary Scan

21.4 REGISTERS

21.4.1 JTAGVERNUM

Register	JTAGVERNUM							
Page	0	Address	Dec # 252		Hex 0xFC			
Bit	7	6	5	4	3	2	1	0
Name	RSRVD	RSRVD	RSRVD	RSRVD	VERNUMBER(3:0)			
Read/Write	-	-	-	-	R	R	R	R
Reset_off	-	-	-	-	x	x	x	x

Register bits description

RSRVD (bit 7 - 4)	Reserved bits
VERNUMBER[3:0]	Value depending version number

21.4.2 TESTUNLOCK

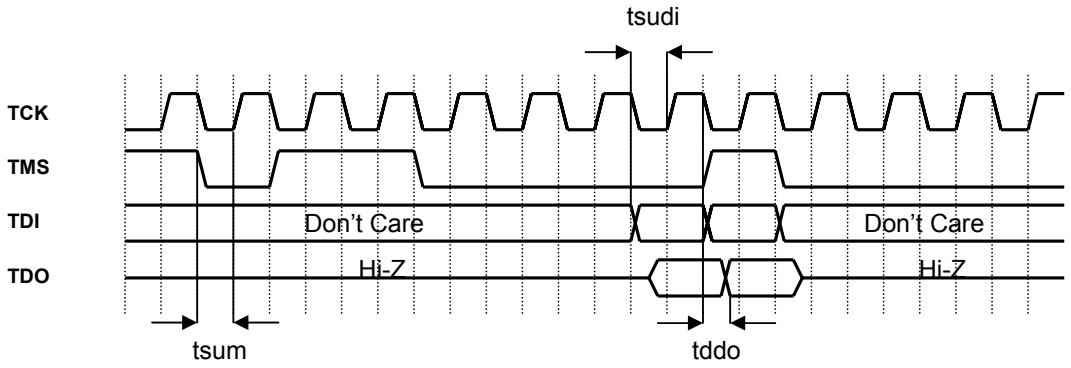
Register	TESTUNLOCK							
Page	0	Address	Dec # 254		Hex 0xFE			
Bit	7	6	5	4	3	2	1	0
Name	TEST_ UNLOCK_ KEY_7	TEST_ UNLOCK_ KEY_6	TEST_ UNLOCK_ KEY_5	TEST_ UNLOCK_ KEY_4	TEST_ UNLOCK_ KEY_3 **enable 32k BCI clock in deep sleep**	TEST_ UNLOCK_ KEY_2	TEST_ UNLOCK_ KEY_1	TEST_ UNLOCK_ KEY_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset_off	0	0	0	0	0	0	0	0
Unlock key	1	0	1	1	0	1	1	0

Register bits description

TEST_UNLOCK_KEY [7:0]	Code to un-lock all the test registers in T3031 (0xB6)
TEST_UNLOCK_KEY[3]	When set to 1, it disables fix for WEBS 20. TEST_UNLOCK[3]=1 then BCI 32KHz clock is always ON TEST_UNLOCK[3]=0 then BCI 32KHz clock is switched OFF when going to SLEEP mode

21.5 TIMINGS CHARACTERISTICS

The Test Access Port of T3031 follows the timings specified in the IEEE Std1149.1a Figure 56. The following timing diagram is only used to provide information about T3031 setup and hold times on the input/output pins.



Parameter	Conditions	Min	Typ	Max	Units
TCK frequency		--	--	5	MHz
tsums Setup time TMS to TCK ↑		15	20	--	ns
tsudi Setup time TDI to TCK ↑		15	20	--	ns
Tddo Delay time TDO from TCK ↓		10*	19*	28*	ns

*: Values from Powermill simulations (Weak, Typical, Strong).

Figure 56 : TAP Timings Characteristics

Appendices

A. Acronyms

ADC	Analog-to-Digital Converter
BCI	Battery-Charger-Interface
BG	Band Gap
BT	BlueTooth
D^-	Data Minus
D^+	Data Plus
DAC	Digital-to-Analog Converter
DBB	Digital BaseBand
DS-WCDMA	Direct Sequence/Spread Wideband Code Division Multiple Access
FS	Full Speed
FSM	Finite State Machine
GPIO	General purpose I/O
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Group Speciale Mobile / Global System for Mobile Communications
HNP	Host Negotiation Protocol
HS	High Speed
I2C	Inter Integrated Circuit
I^2S	Inter-IC Sound Bus
JTAG	Joined Test Action Group
LCD	Liquid Crystal Display
LDO	Linear Drop-Out
LED	Light Emitting Diode

LS	Low Speed
MIC	Microphone
MMC	Multi Media Card
OTG	On-The-Go
PD	Pull-Down
PER	Peripherals
PMB	Power Management Bus
PP	Power Provider resource group (DCDC, LDO..)
PU	Pull-Up
PR	Power Reference resource group (BG,BIAS,BAT28…)
PSM	Phone State Machine
PWM	Pulse Width Modulation
RC	Reset and Control resource group (Clock enable signal, reset…)
RTC	Real Time Clock
SCL	Serial Clock Line
SDA	Serial Data Line
SE0	Single-Ended Zero
SE1	Single-Ended One
SIM	Subscriber Identity Module
SOF	Start Of Frame
SPI	Serial Peripheral Interface
SPKR	Speaker
SRP	Session Request Protocol
TAP	Test Access Port
TBC	To Be Confirmed
TBD	To Be Determined
TTL	Transistor – Transistor Logic
USB	Universal Serial Bus
VRPC	Voltage Reference / Power Control
VSP	Voice Serial Port

B. Glossary

International Mobile Telecommunication 2000 (IMT-2000/ITU-2000)	Formerly referred to as FPLMTS (Future Public Land-Mobile Telephone System), this is the ITU's specification/family of standards for 3G. This initiative provides a global infrastructure through both satellite and terrestrial systems, for fixed and mobile phone users. The family of standards is a framework comprising a mix/blend of systems providing global roaming. <URL: http://www.imt-2000.org/>