System Hardware Implementation LOCOSTO

and LOCOSTO-LITE

Specification

VER:1.6

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Department: R&D Cellular Systems WTBU organization Texas Instruments Nice

	Originator
Name	Jean PETENA
Created Date	October 4th, 2004

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HISTORY

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1.5	June 15th, 2005	Jean PETENA	Updated USB connector,	Christophe Labaume, Eric Balard,	8

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NOTES:

1. Creation

2. Update with final system schematic and components choices.

3. Changes : _ Charger schematic.
   _ CP1b feedbacks review included.
   _ Irda signal directions changed.
   _ UART and BT ball changed.

4. Changes : _ VGA ST CCP camera removed because not compatible with or without coprocessor.
   _ Debug capability chapter added.
   _ Added Global boot sequence.
   _ Added chap : system mode and system application
   _ ST CCP Camera 1.0Mp + co-processor added.
   _ System and Locosto Modes and transitions added.
   _ Detailed DM290 implementation included.

5. LocostoLite added and DM290 chapter reviewed and updated.

6. LocostoLite chapter updated to follow the LocostoLite definition changes.

7. Added Annex A : Stereo headset specification.
   Added Optional MMC/SD card connection on SPI interface.

8. Updated USB connector, updated Locosto-Lite def.

9. Triton changed to Triton-lite in the Locosto and Locosto + system. Updated Locosto-Lite chapter.

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1 Glossary

AES	Advanced Encryption Standard

BIST	Built In System Test
CCP	Compact Camera Port
CE	Cellular Engine
CRC	Cyclic Redundancy Check
CTS	Cleat To Send
DCXO	Digitally Controlled Crystal Oscillator
DBB	Digital Base Band
DRP 2	Digital Radio Processor 2
DVS	Dynamic Voltage scaling
EMIFS	External Memory Interface Slow
FIFO	First In First Out memory
FPS	Frame Per Second
GPS	Global Positioning System
GPRS	General Packet Radio Service
GS	GPS Sensor
HZ	High Impedance
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LS	Location Server
MMGPS	Multi-mode GPS
MS	Memory Stick
MS	Mobile Station
NFC	Nand Flash Controller
PIO	Programmable I/O
PLL	Phase-Locked Loop
PPS	Pulse Per Second
RAM	Random Access Memory
RF	Radio Frequency
RTC	Real Time Clock
RTS	Request To Send
SCCB	Serial Camera Control Bus
SD	Secure digital
SDIO	Secure digital I/O
UART	Universal Asynchronous Receiver/Transmitter
WIFI	Wireless Fidelity
WPA	Wireless Fidelity Protected Access

2 Introduction

This document explains how to properly integrate the LOCOSTO processor with other specific application ICs. Each chipset/application/interface is first described from a system point of view; lower level schematics are then given with design guidelines for integration of the various chips. Control signals, clocks, power plans, design, layout and routing constraints are fully detailed, allowing for an easy and fast product development cycle.

➔ *This document concentrates on the implementation of the Texas Instruments GPRS modem solution based on the **LOCOSTO** processor and the **TRITON LITE** companion chip for the audio, the USB connections and the power domain. Additional chipsets are also dealt with that support wireless communications: a-GPS, Bluetooth, FM and infrared.*

IC name	Application	Device ID	Package	Provider	Note
LOCOSTO	Processor	TSC2300		Texas Instruments Inc	
Triton Lite	Power management	TWL3031		Texas Instruments Inc	
aGPS	a-GPS	GPS5002		Texas Instruments Inc	
Island 2	Bluetooth	BRF6150		Texas Instruments Inc	
AGILENT	Infrared	HSDL3220		Agilent	
DM290	Image Signal Processor And video accelerator	DM290		Texas Instruments Inc	

IC name	Source of information	Revision
LOCOSTO	Locosto2004doc\hardware\specs\lcost_soc.doc	1.2
TRITON Lite	Top level Power supplies Digital modules specs Real time clock USB Pin out Ball mapping VRPC power management	1.1 2.0 0.2 0.1 0.1 14.01.2005 14.01.2005 1.0
aGPS	Data sheet	0.981
Island 2 (BRF6150)	BT-DS-0022 BRF6150 Product Preview Island2 Power Management SDP-BT-Spec	0.1 0.31 1.0
DM290	System spec DM290 External Host Interface Analysis	R2.0 Ver: 1.2
HSDL3220	HSDL3220 Data sheet	0.83

2.1 System schematic

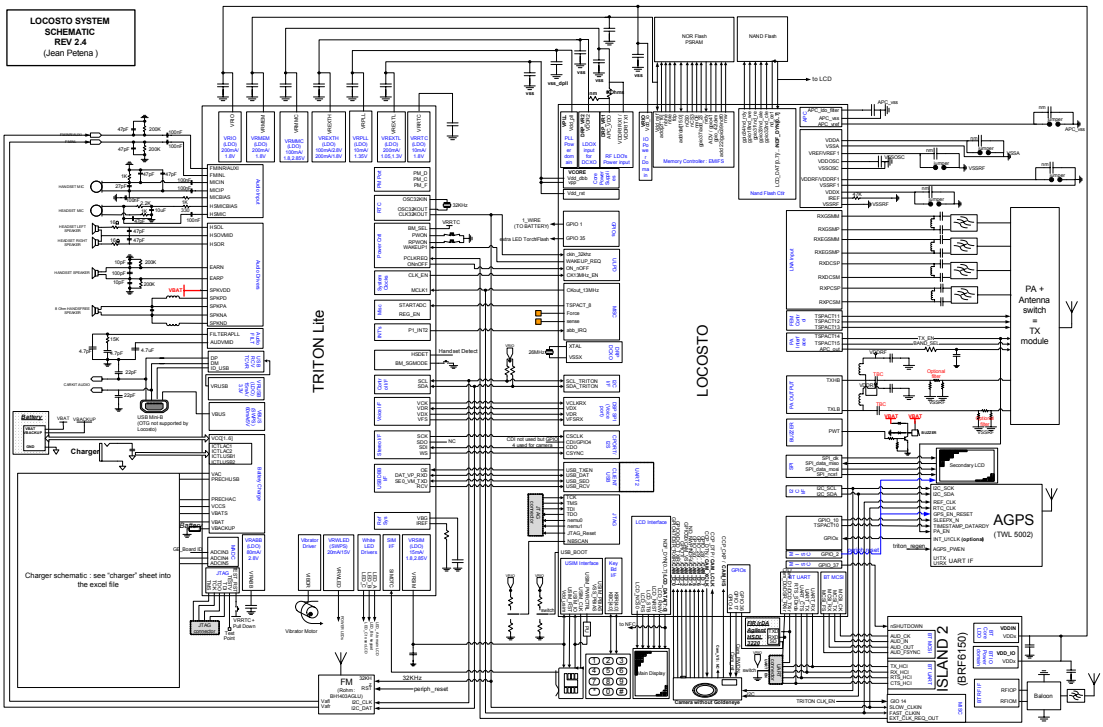


Figure 1 : Global System schematic

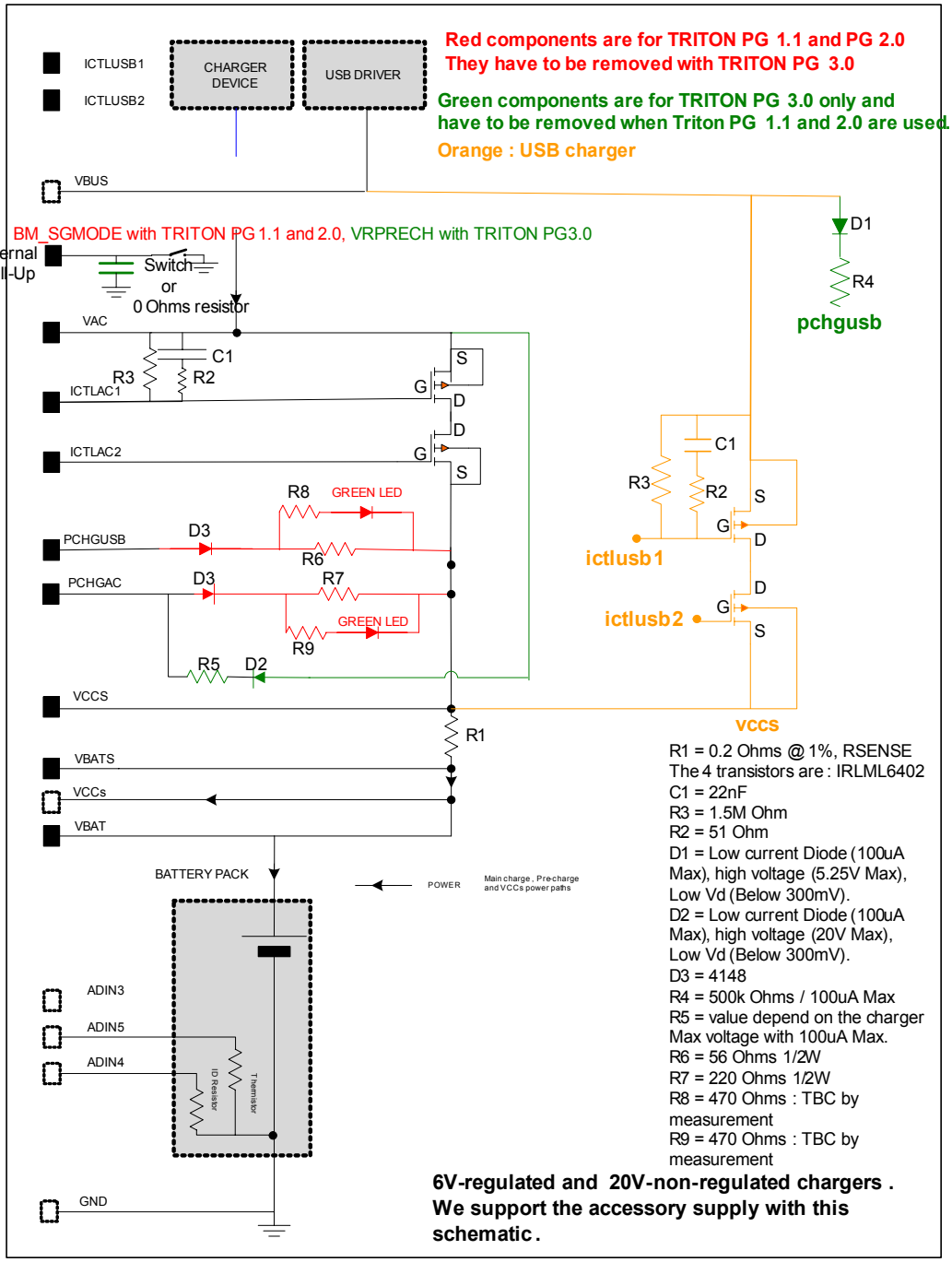


Figure 2 : charger schematic, compatible Triton lite PG 1.1, 2.0, 3.0 depending of component loading.

2.2 Overall system view

Application	Function	Chipset
Resources management	Battery management	[BAT]
	Power management	Triton Lite
	Clocks management	Xtal 26MHz : NDK NX3225DA W-191-735 Xtal 32KHz : Seiko Instruments : SSP-T7
Memories	NOR memory	Spansion S29NS064J
	PSRAM memory	Micron MT45W4MW16BFB
	NAND memory	Toshiba TC58DYM92A2XGJ5 or Samsung K9F1G08QOA
	Or MCP (NOR/PSRAM)	Spansion S71NS128JA0
RF	SAW GSM850	Murata SAFEB881MFL0F00
	SAW GSM900	Murata SAFEB942MFL0F00
	SAW DCS	Murata SAFEB1G84FA0F00
	SAW PCS	Murata SAFEB1G96FA0F00
	TX MODULE	RFMD 3178G
Wireless	Bluetooth	TI BRF6150 (Island 2), Island 3 will be also used in a second step.
	IrDA	Agilent FIR 3220
Navigation	AGPS	TI TWL 5002
Cameras	Parallel camera	Agilent ADCM2700
	Serial camera	ST VS6650
	Camera coprocessor	TI DM290
Displays	Main display	LCD Philips LPH8754-2 + controller Hitachi HD66774
	Sub display	LCD TFS 128*128 + Driver Sitronix ST7541
Audio	Handset	[HST]
	Headset	[HS]
	Car kit	[CKIT]
	Handfree	[HFREE]
	FM radio	Rohm BH1403AGLU
Cards	SIM card	[SIM]
USB	USB transceiver	Triton Lite : TI TWL3031
User interfaces	Keypad	5*5 Keypad

Application	Function	Chipset
	Vibrator	[VIB]
	Leds	Torch Flash / 3 back-light LEDs
	Buzzer	[BUZZER]
Debug capabilities	JTAG connector	JTAG Connector
	Monitoring	UART Connector
	Trace	Test port
	Other debug	NBSCAN

Table 1 : System described

2.2.1 Brief chipset description

2.2.1.1 Processor chipset

The system chipset is based on the DBB processor IC (LOCOSTO) and the power management IC (TRITON LITE).

➢ The LOCOSTO Integrated Circuit (IC) is a Digital Base Band (DBB) processor, cDSP/ARM7 @104MHz based, merged with the Digital Radio Processor 2 (DRP 2). The Locosto IC is integrated on a 90nm process (1218C027.0) based on the GS50 Standard Cells macro library.
The core runs at 1.3V nominal while the interface is specified at 1.8V nominal (except USIM, Reset, DRP & APC I/Os).
The DBB supports the processing of GSM radio signals in switching circuit mode and packet data mode (GPRS) for up to class 12, including evolution such as SAIC & localization system (A-GPS…) in compliance with the ETSI specification.
In addition the DBB can process, in a secure environment, messaging & multimedia services, such as EMS/MMS, WAP-browsing, Audio-players, Camera-functions, JAVA-based downloaded application…
The TCR3.2 software layer that controls the radio function as well as applications is based on and includes all features of TCR 3.1 plus additional specific components.
The DBB H/W function is based on the Calypso-Plus device and as such maintains the computing performance as well as the security levels, whereas system connectivity is down graded however still enabled for supporting system such as TI-Bluetooth, TI-AGPS &/ Camera systems. LoCosto-IC compared to CalypsoPlus embeds a reduced & re-partitioned memory system. Locosto target is to provide a low-cost solution and keep a high processing capability.
The supported operating system by Locosto is Nucleus.

➢ TRITON LITE (TWL3031) is an integrated power management specifically designed for integration with NEPTUNE or LOCOSTO, providing all the required power supplies and management functions. Power supplies are delivered through 11 LDO and 3 biases to the digital base-band and the interfaces (memories, PLL, IO, RTC, SIM, MMC, VBUS, USB, LED, and RF). Power management functions include dynamic voltage scaling, state machine control, modem power-up and power management sharing (power management port). System management is done through an I2C serial interface, allowing host to access the IC configuration registers, and the ability to interrupt the host. Voice and audio capabilities are controlled through both an I2S and a VSP serial interface, and include microphone, headset microphone, FM radio inputs, earplug, analog/digital speakers, and headset amplifier outputs. Additional hook detection input and auxiliary audio output are possible. Transceiver/driver functions include SIM detection, USB/UART interface, 3 White led drivers and vibrator driver. Housekeeping functions are done through 5 A/D converters. TRITON LITE provides also RTC functions, JTAG test, and a complete battery charger and control interface.
Triton lite is a 125zph socket.

2.2.1.2 Bluetooth Chipset

- ISLAND2 (BRF6150) chip is a highly integrated single-chip CMOS (H035) Bluetooth device that forms a complete standalone Bluetooth wireless communication system. The BRF6150 is the second generation of TI Single Chip succeeding the BRF6100 device. This device implements an advanced solution for the Bluetooth protocol with easy interfacing to a host system. The BRF6150 comprises: Digital Radio Processor (DRP), embedded Bluetooth point-to-multipoint hardware core for highly optimized execution of the Bluetooth protocol according to Bluetooth Specification 1.1 and 1.2, on-chip ROM and RAM, embedded ARM7TDMIE Microprocessor. The firmware running in ARM7TDMIE processor includes the low layers of the Bluetooth Protocol up to the Host Controller Interface (Link Controller, Link Manager, HCI and HCI Transport Layer). These functions combined with several on-chip peripherals enable easy integration with a variety of applications.
In a second step Island 3 will be used instead of Island 2.

2.2.1.3 aGPS chipset

- GPS5002 GPS system is a Multi-Mode Global Positioning System chip consisting of a highly parallel GPS receiver, a control processor and a set of peripherals. The heart of the GPS receiver is a set of eight parallel matched filter processors, called a fast convolution engine, which, during initial acquisition, can fully search in parallel all code phases of up to 8 received GPS signals (a total of 8184 chips). Alternative modes of acquisition and tracking allow the processing capability of the engine to be divided between a large number of frequency and time channels. For example, in one mode each filter processor may, in parallel, process a different set 64 different Doppler frequency bins, each over a different restricted code phase interval. This parallel processing affords reduced acquisition time by a factor of 100 or more over previously available hardware based solutions.

2.2.1.4 Image processor chipset and video accelerator

- DM290 is a low-power, highly integrated, combined hardware and programmable Camera Image Signal-Processing (ISP) platform. It is designed to offer camera module manufacturers the ability to produce affordable camera. Module products with high picture quality, the DM290 combines hardware and programmable image processing capability and highly integrated imaging peripheral set. Internal processing includes dead pixel correction, black level compensation, CFA interpolation, white balancing, Gamma correction, color space conversion and scaling. The interface is flexible enough to support various types of CCD and CMOS sensors, signal conditioning circuits, power management, and SDRAM, shutter, iris and auto-focus motor controls. The DM290 also enables seamless interface to TI application or baseband processors.

- CMOS SENSOR (ADMC4852) Ultra compact CMOS camera module is an advanced, low-power 2-mega-pixel camera component for embedded application as cellular phone. It combines an AGILENT CMOS image sensor and image –processing pipeline with a high quality, Auto-focus 3 element lens system and IR cut filter to deliver images in JPEG and data formats ready for storage or transmission.

- CCP SENSOR (VS6650) is a 1.0 mega-pixel camera module for use across a range of mobile phone platforms. It can generate 1 Mega-pixel images up to 30 fps. The VS6650 3-element lens design ensures high quality image capture while maintaining low module height. The overall optical stack, including lens system, IR filter, and sensor optical structures is developed by ST.

2.2.2 Block diagram

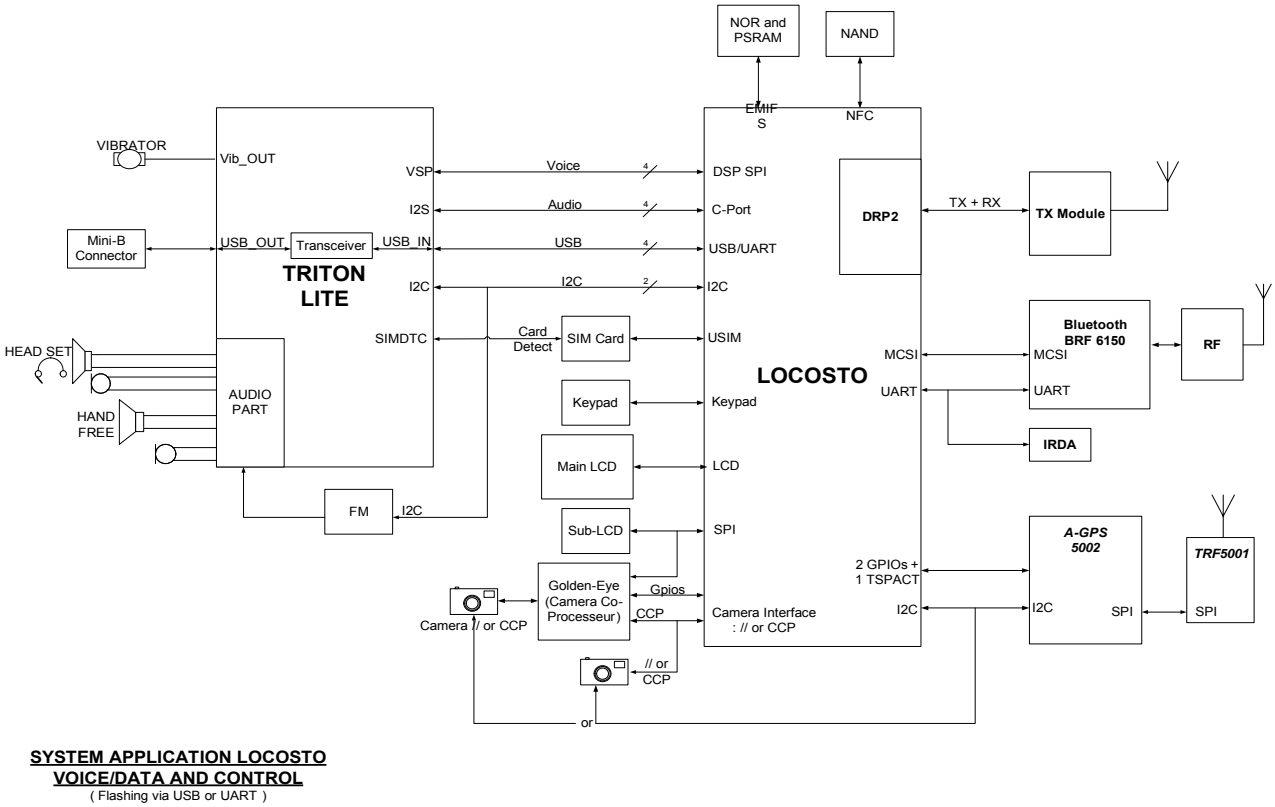


Figure 3 : Synoptic system schematic

An I2C (multi-master) bus is used for configuration access and control of the devices: LOCOSTO to TRITON LITE. Interrupts lines are used to request actions from the processors: Triton Lite to Locosto. Data are exchanged between LOCOSTO and TRITON LITE using two interfaces: a VSP interface for voice data, and an I2S interface for audio data. Triton Lite is the analog audio transceiver. It sends and receives voice data to/from LOCOSTO, and audio data to/from LOCOSTO through these two separate interfaces. Triton Lite also includes the USB transceiver: the only one USB input interface of this system. LOCOSTO can access the USB connector through TRITON LITE.

LOCOSTO accesses Triton Lite configuration and state registers using the I2C bus. Triton Lite interrupts LOCOSTO using the auxiliary processor dedicated P1_INT2 pin, and can signal up to 13 events such as USB detection, headset detection, battery monitoring, battery end of charge, etc. LOCOSTO has no internal USB transceiver and must make use of Triton Lite's transceiver capability to access an external USB device. Triton Lite includes a single USB OTG dual-role transceiver compatible with the "Universal Serial Bus Specification Revision 2.0 April 27, 2000" (HS no supported) and "On-The-Go Supplement to the USB 2.0 Specification Revision 1.0 Dec 18, 2001".
The Locosto-Triton Lite solution DOES NOT support OTG because Locosto do not support OTG feature (Locosto is slave only). Triton Lite USB interface works in 4 pin bi-directional modes. This selection is made through an internal configuration register.

LOCOSTO makes use of Triton Lite's extensive audio capabilities to record (MIC line, FM input, Headset) or playback music (speakers, EAR plug, and headset). Data exchange is done through a digital audio link (I2S standard), where LOCOSTO is the master and Triton Lite the slave.

Locosto makes use of Triton Lite's extensive audio capabilities to get (MIC line, Headset MIC) or playback voice data (speakers, EAR plug, headset speakers). Data exchange is done through a digital voice link, where Locosto is the master and Triton Lite the slave.

3 System Interconnect description

3.1 Locosto DRP2 and RF interface IMPLEMENTATION

3.1.1 Introduction

Locosto Radio Interface is a quadruple band transceiver sub-module suitable for GSM850, E-GSM900, DCS1800 and PCS1900 GPRS Class 12 applications.
Locosto Radio Interface is based on the DRP2.0 module. This module integrates a receiver based on a near zero IF architecture and a transmitter based on an ADPLL synthesizer which has a phase/frequency modulation capability. The receiver LO generation is performed by the ADPLL synthesizer.

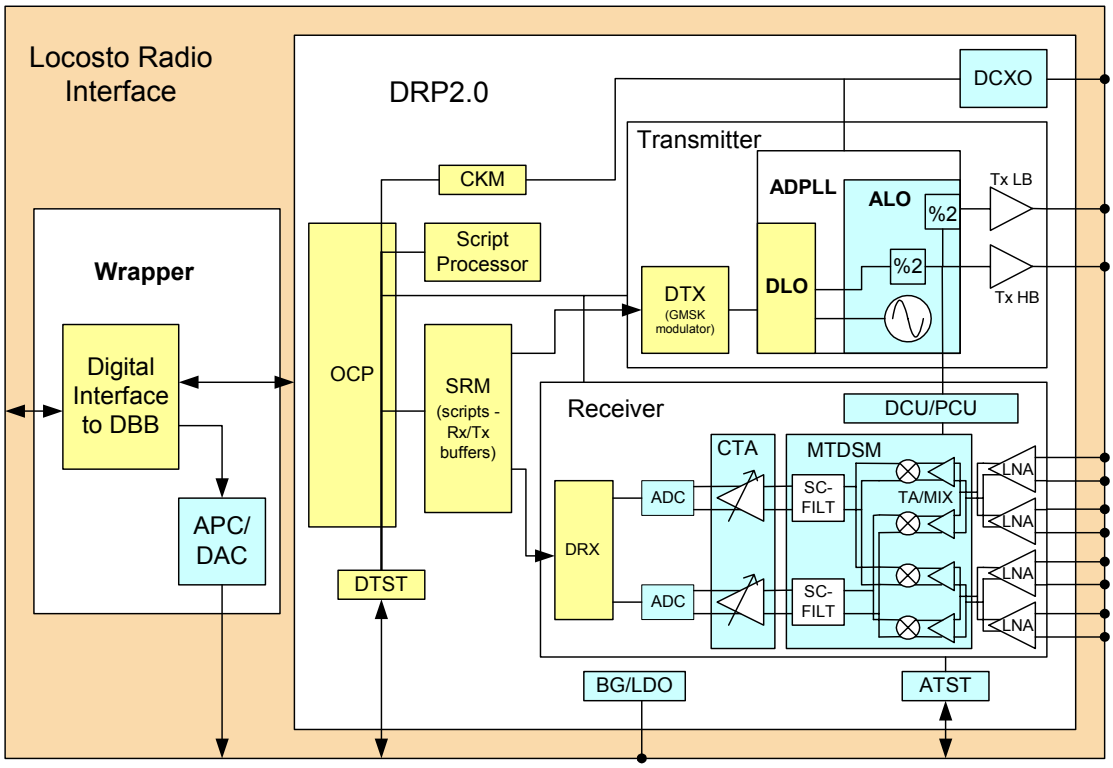


Figure 4 Locosto Radio Interface Block Diagram

The Locosto Radio Interface is based on the DRP2.0 module. This module integrates:

- A frequency synthesizer implemented as an All Digital PLL (ADPLL) which has a phase/frequency modulation capability (DTX).
- A receiver based on a near zero IF architecture. The receiver LO generation is performed by the ADPLL synthesizer. The receiver chain is constituted by 4 LNAs followed by MTDSM (Multi taps Direct Sampling Mixer), a continuous time amplifier (CTA), an analog to digital converter and a digital block DRX.

- A CKM module that generates clocking signals for the RF part and permits DBB system clock re-synchronization.
- A Script Processor to manage the sequencing and calibration of the transceiver.
- A DCXO generating the reference frequency for the ADPLL.
- DTST and ATST blocks for digital and analog test.
- OCP module as communication path to DBB.

The wrapper section of Locosto Radio Interface manages the connection between the DRP2 sub-module and the DBB. It also implements the APC functionality and power, reset and clock system management.

For more information see the “lcost_radio_interface.doc” documents.

3.1.2 RF schematic :

Please refer to reference design or validation platform for complete detailed RF interface schematic.

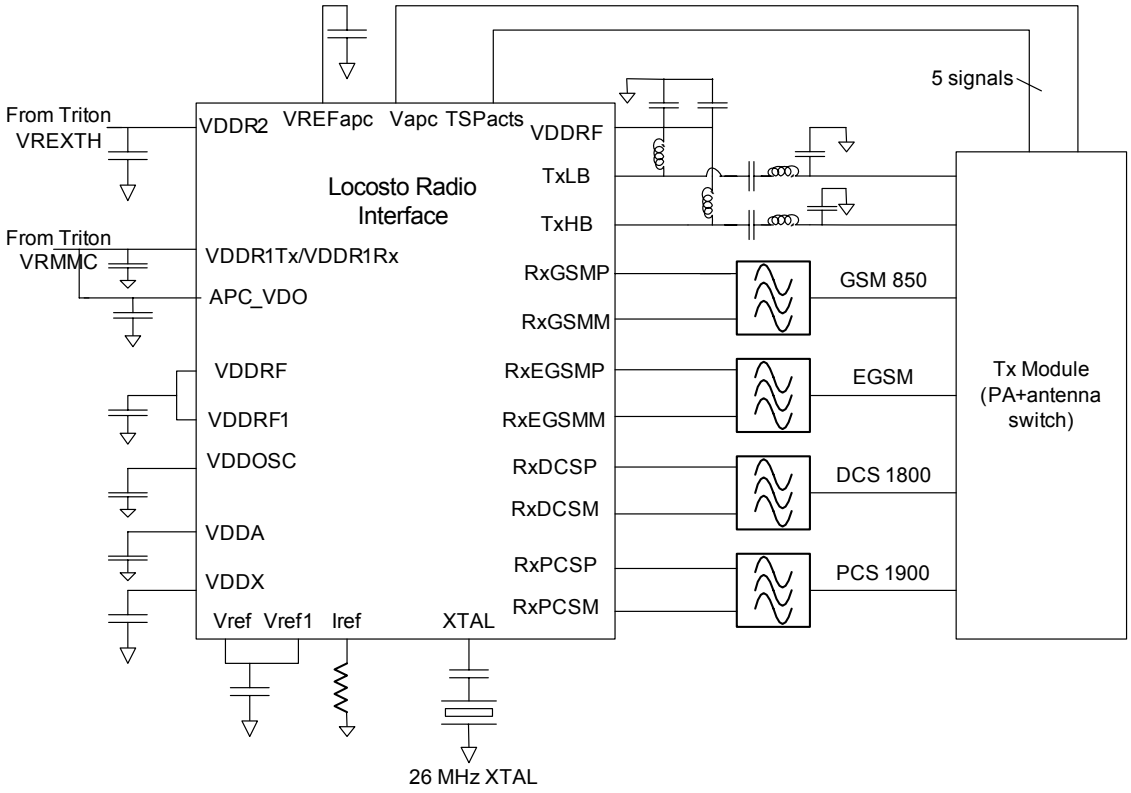


Figure 5 Application Board Functional Diagram

3.1.3 Components references :

The TX module reference is **RFMD RF3178G**

The chosen SAW filters are : Murata :
_ GSM850 : SAFEC881MFL0F00
_ GSM900 : SAFEC942MFL0F00
_ DCS : SAFEC1G84FA0F00

_ PCS : SAFEC1G96FA0F00

3.1.4 Connections :

LOCOSTO						SAW filter GSM850 : SAFEB881MFL0F00				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
RXGSMM	N17	0	I	VDDR1RX1	←	Output 2	4	O	NA	
RXGSMP	M17	0	I		←	Output 1	3	O		
LOCOSTO						SAW filter GSM900 : SAFEB942MFL0F00				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
RXEGSMM	M16	0	I	VDDR1RX1	←	Output 2	4	O	NA	
RXEGSMP	L16	0	I		←	Output 1	3	O		
LOCOSTO						SAW filter DCS : SAFEB1G84FA0F00				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
RXDCSM	K17	0	I	VDDR1RX1	←	Output 1	3	O	NA	
RXDCSP	L17	0	I		←	Output 2	4	O		
LOCOSTO						SAW filter PCS : SAFEB1G96FA0F00				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
RXPCSP	K16	0	I	VDDR1RX1	←	Output 2	4	O	NA	
RXPCSM	J16	0	I		←	Output 1	3	O		
LOCOSTO PA output						TX module : RFMD RF3178G				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
TXHB	G17	0	O	VDDR1TX1	→	DCS/PCS_IN	9	I	VDDR1TX1	
TXLB	F17	0	O		→	GSM850/GSM900	2	I		
LOCOSTO : Other RF signals						TX module : RFMD RF3178G				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
TSPACT11	F12	0	O	VDD_IO	→	B3	6	I	VDD_IO	
TSPACT12	H10	0	O		→	Not used				
TSPACT13	C14	0	O		→	B1	3	I		
TSPACT14 (TX_EN)	E12	0	O		→	TX_ENABLE	7	I		
TSPACT15 (BAND_SEL)	G10	0	O		→	B2	4	I		
APC_OUT	M11	0	O	APC_VDO	→	VRAMP	8	I		
SAW filter GSM850 : SAFEB881MFL0F00						TX module : RFMD RF3178G				**N**
Signal	**Pin**		**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
Input	1		I	VDDR1RX1	→	RX 850	13	O	VDDR1RX1	
SAW filter GSM900 : SAFEB942MFL0F00						TX module : RFMD RF3178G				**N**
Signal	**Pin**		**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
Input	1		I	VDDR1RX1	→	RX 900	14	O	VDDR1RX1	
SAW filter DCS : SAFEB1G84FA0F00						TX module : RFMD RF3178G				**N**
Signal	**Pin**		**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
Input	1		I	VDDR1RX1	→	RX 1800	15	O	VDDR1RX1	
SAW filter PCS : SAFEB1G96FA0F00						TX module : RFMD RF3178G				**N**
Signal	**Pin**		**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
Input	1		I	VDDR1RX1	→	RX 1900	16	O	VDDR1RX1	

Table 2 : RF interface connections

The reference clock is based on a Digitally-Controlled-Crystal-Oscillator (DCXO) architecture. The oscillator uses an external 26 MHz crystal. The AFC is done by programming the corresponding register through the control interface. The frequency correction is done by switching the oscillator capacitors in a digital manner.

3.1.5 External Crystal

Parameters	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Nominal Frequency				26		MHz
Frequency tolerance	at 25ºC ±3ºC				±10.0	ppm
Temperature characteristics	in reference to +25ºC over –20ºC ~+75ºC				±10.0	ppm
Aging 1st year after 5 years					 ±1.0 ±2.5	 ppm ppm
Dips vs. temperature	–20ºC ~ +75ºC				0.3	ppm/°C
Frequency versus temperature slope at 25°C	at 25° C ± 7°C		-0.5		0	ppm/°C
Equivalent Series Resistance					50	Ω
Standard load capacitance				12.5		pF
Shunt capacitance			1.0	1.2	1.4	pF
Series capacitance			4.3	5	5.7	fF
Drive level				50	100	µW

Table 3 Xtal requirements

3.1.6 Power considerations :

The SAW does not need external supply as they are passive filters. The TX module is supplied
directly by VBAT and the power consumption can be up to 2 to 3 A.

3.1.7 Current Consumption :

Power Mode	Test conditions	Typical operating current on VR1	Typical operating current on VR2	Typical operating current on VDDCORE
OFF Mode	All blocks off VDDCORE is off	Tbd uA	Tbd uA	Tbd uA
DEEP SLEEP Mode	All blocks off VDDCORE is on	15 uA	5 uA	TBD uA
IDLE1 Mode	All blocks off VDDCORE is on DCXO and Bandgap are ON	15 uA	2.8 mA	TBD uA
IDLE2 Mode	All blocks off VDDCORE is on DCXO and Bandgap are ON Regulators are ON	1.3 mA	2.8 mA	TBD uA

RECEIVE Mode

Module				
LNA/Mixer/CTA/ADC		35.5 mA		
DRX				6.3 mA
All-Digital PLL (including DCO)		24.6 mA	2.8 mA	15.4 mA
TOTAL		**60.1 mA**	**2.8 mA**	**21.3 mA**

TRANSMIT Mode

Module				
All-Digital PLL (including DCO)		23.6 mA	2.8 mA	15.6 mA
PA DAC		TBD		
PA Buffer		15.1 mA		
TOTAL		**38.7 mA**	**2.8 mA**	**15.6 mA**

3.1.8 Layout considerations :

_ The following lines must be 50 Ω :

- The 4 lines between the 4 SAW and the TX module.
- The 2 TX lines between Locosto and the TX module.
- The Antenna line : between the TX module and the antenna.

_ The VBAT supply to the TX module being 2-3 A the line must be very large and reduce the voltage drop-out as much as possible.

_ A special care must be taken for the Locosto RF GND : 3 GND separate islands must be done in the top layer for RF balls, RF analog balls, and RF digital balls. These 3 separate GND islands must be then connected together internally, through vias, to the main GND.

_ A special care must be taken for the APC_out line that must be routed to reduce the noise on this line as much as possible.

_ the 8 RX lines between the 4 SAW and Locosto must have : same length, same impedance,
routing that reduce noise.

_ At a component placement point of view all the RF lines must be as short as possible, so the SAWs and the TX module must be placed the nearest possible to Locosto. Especially, the 4 SAWs and its adaptation filters must be placed very near the Locosto balls.

3.2 Locosto to Triton Lite connection

LOCOSTO						TRITON LITE				Comments
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
TSPACT 8	N9	1	O	VDD_IO	→	STARTADC	M6	I	VRIO	
ABB_IRQ	P8	0	I		←	P1_INT2	M1	O		
SCL_TRITON	N7	0	IO		↔	SCL	M5	IO		
SDA_TRITON	R6	0	IO		↔	SDA	J6	IO		
VCLKRX	R7	0	I		←	VCK	L3	O		Voice
VDX	T6	0	O		→	VDR	L4	I		
VDR	M8	0	I		←	VDX	M2	O		
VFSRX	K9	0	I		←	VFS	M3	O		
CDI/GPIO4	R9	1	I		←	SDO (SDX)	H6	O		Can be left not connected, use the GPIO 4 instead.
CSCLK	P9	0	I		←	SCK	M4	O		Audio
CDO	T9	0	O		→	SDI (SDR)	K5	I		
CSYNC	M9	0	I		←	WS	L5	O		
USB_TXEN	M7	0	O		→	OE	E4	I		USB
USB_DAT	R5	0	O		→	DAT_VP_RXD	C3	I		
USB_SEO	L8	0	O		→	SEO_VM_TXD	C4	I		
USB_RCV	T4	0	I		←	RCV	A2	O		

Table 4 Locosto to Triton Lite connection

3.3 LOCOSTO MEMORY IMPLEMENTATION

3.3.1 EMIF (FLASH) memory interface

LOCOSTO EMIF supports PSRAM, NOR, ADD/DATA multiplexed, protocols. The data bus is 1.8V, 16-bit or 8-bit and runs up to 52 MHz (Burst clock).
The EMIF can control up to 4 memory devices, with 4 Chip Select signals, for a total address range up to 124-Mbyte (1 * 28-Mbyte + 3 * 32Mbyte). The CS3 (bootable) will be on the NOR Flash then the CS0 on the PSRAM. The CS1 and CS2 are accessible for optional added flash memory devices.

Supported device types
8bit and 16bit address and data multiplexed NOR Flash device
8bit and 16bit address and data multiplexed PSRAM device

The flash memory interconnection described is based on the following device :

Reference: NOR : S29NS016J/S29NS064J/S29NS128J
Type: Read/Write Burst Mode flash memory
A/D: muxed
Size: 16 / 64 / 128 Mbits
Data bus: 16 bits
Manufacturer: Spansion
Power supply: 1V8

Reference: NOR : M58WR016FU
Type: Read/Write Burst Mode flash memory
A/D: muxed
Size: 16 Mbits
Data bus: 16 bits
Manufacturer: ST Microelectronics
Power supply: 1V8

Reference: NOR : RD38F3050L0YBQ1S
Type: Read/Write Burst Mode flash memory
A/D: muxed
Size: 64 Mbits
Data bus: 16 bits
Manufacturer: Intel
Power supply: 1V8

Reference: PSRAM : MT45W4MW16BFB
Type: Read/Write Burst Mode flash memory
A/D: non muxed
Size: 64 Mbits
Data bus: 16 bits
Manufacturer: Micron
Power supply: 1V8

Reference: MCP : S71NS128JA0 (128Mb Spansion NOR / 64Mb Micron PSRAM)
Type: Read/Write Burst Mode flash memory
A/D: muxed
Size: (128Mb Spansion NOR / 64Mb Micron PSRAM)
Data bus: 16 bits
Manufacturer: Spansion (Micron PSRAM)
Power supply: 1V8

LOCOSTO						S29NS064J				N
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
Control signals										
ADV	J7	0	O		→	nAVD	B4	I		
nCS_0	E3	0	O		→					
nCS_1	D2	1	O		→					
nCS_2	F5	1	O		→					
nCS_3	L5	0	O		→	nCE	B9	I		
ckm	L6	1	IO		↔	CLK	A4	IO		
NMOE	M1	0	O	VDD_MIF	→	nOE	C10	I	VRMEM	
NRDY	M3	0	I		←	RDY	A1	O		
NBHE	L3	0	O		→					
NBLE	M2	0	O		→					
NFWP	G6	1	O		→	nWP	B7	I		
FDP	K6	0	O		→	nRESET	B6	I		
RNW	L1	0	O		→	nWE	A6	I		
Address signals										
ADD_16	G3	0	O		→	A16	B2	I		
ADD_17	F1	0	O		→	A17	A9	I		
ADD_18	F2	0	O		→	A18	B8	I		
ADD_19	H6	0	O		→	A19	A8	I		
ADD_20	J8	0	O	VDD_MIF	→	A20	B3	I	VRMEM	
ADD_21	F3	0	O		→	A21	A2	I		
ADD_22	G5	1	O		→	A22	A10	I		
ADD_23	H7	1	O		→					
Data/Address signals										
ADD_DAT_0	K4	0	IO		↔	A/DQ0	D10	IO		
ADD_DAT_1	L2	0	IO		↔	A/DQ1	D9	IO		
ADD_DAT_2	K5	0	IO		↔	A/DQ2	C7	IO		
ADD_DAT_3	K3	0	IO		↔	A/DQ3	C6	IO		
ADD_DAT_4	K2	0	IO		↔	A/DQ4	D5	IO		
ADD_DAT_5	J5	0	IO		↔	A/DQ5	D4	IO		
ADD_DAT_6	J3	0	IO		↔	A/DQ6	C3	IO		
ADD_DAT_7	J2	0	IO		↔	A/DQ7	C2	IO		
ADD_DAT_8	J4	0	IO	VDD_MIF	↔	A/DQ8	C9	IO	VRMEM	
ADD_DAT_9	J6	0	IO		↔	A/DQ9	C8	IO		
ADD_DAT_10	H2	0	IO		↔	A/DQ10	D7	IO		
ADD_DAT_11	H3	0	IO		↔	A/DQ11	D6	IO		
ADD_DAT_12	H5	0	IO		↔	A/DQ12	C5	IO		
ADD_DAT_13	G2	0	IO		↔	A/DQ13	C4	IO		
ADD_DAT_14	G1	0	IO		↔	A/DQ14	D2	IO		
ADD_DAT_15	H4	0	IO		↔	A/DQ15	D1	IO		

Table 5 EMIF interface connection

Layout considerations :

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W.
- The memory bus must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.3.2 NFC (NAND) memory interface

The NAND Flash interface allows connecting NAND Flash as an external mass storage facility. The interface implements a 8 bits parallel data bus in addition to the control signals for selecting chip, writing/reading, command and address latching, ready/busy status.

The interconnection described is based on the following devices :

Reference: TC58DYM92A2XGJ5
Type: NAND
Size: 512M-bits
Data bus: 8 bits
Manufacturer: TOSHIBA
Power supply: 1V8

Reference: K9F5608QOC
Type: NAND
Size: 512M-bits
Data bus: 8 bits
Manufacturer: SAMSUNG
Power supply: 1V8

Reference: K9F1G08QOA
Type: NAND
Size: 1G-bits
Data bus: 8 bits
Manufacturer: SAMSUNG
Power supply: 1V8

LOCOSTO						TC58DYM92A2XGJ5				**N**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
Control signals										
ND_RDY	C2	1	I	VDD_IO	←	RY/nBY	C8	O	VRIO	
ND_WE	A6	1	O		→	nWE	C7	I		
ND_RE	C3	1	O		→	nRE	D4	I		
ND_ALE	H8	1	O		→	ALE	C4	I		
ND_CLE	F6	1	O		→	CLE	D5	I		
ND_CE1	D3	0	O		→	nCE	C6	I		
Data signals										
NDF_0	E9	3	IO	VDD_IO	↔	I/O1	H4	IO	VRIO	
NDF_1	B8	3	IO		↔	I/O2	J4	IO		
NDF_2	C8	3	IO		↔	I/O3	K4	IO		
NDF_3	E8	3	IO		↔	I/O4	K5	IO		
NDF_4	B7	3	IO		↔	I/O5	K6	IO		
NDF_5	D8	3	IO		↔	I/O6	J7	IO		
NDF_6	C7	3	IO		↔	I/O7	K7	IO		
NDF_7	B6	3	IO		↔	I/O8	J8	IO		

Table 6 NFC interface connection

The Nand interface is multiplexed with the LCD interface in the default configuration but the Nand data bus is also accessible on other balls (optional configuration), see Locosto pinout modes for detailed informations about this optional nand data bus access.

Layout considerations :

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W.
- The memory bus must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.4 CAMERA MODULE IMPLEMENTATION

3.4.1 Direct Locosto-Camera connection

3.4.1.1 Parallel camera

The following parallel VGA 1.8v interface cameras are currently under validation. Cost and technical compatibility with the Locosto camera interface has been checked on specification :

- ESS : ES2199M
- ESS : ES2120M
- ST : ST6524.

But full validation of the Locosto camera interface will be performed with the Agilent ADCM2700 camera as the software is already developed and tested.

The Agilent ADCM2700 parallel camera module, color 640*480 landscape VGA resolution, is a 2.8V I/Os CMOS image sensor. As the Locosto camera interface is 1.8V it will need a level shifter to interface. We will use SN74AVCBH164245 and SN74TVC3306 bi directional level shifter.
The Agilent ADCM2700 incorporating a CCIR 656-compatible 8-bit parallel interface, or a RGB or YCbCr interface (serial or parallel), the ADCM2700 support industry-leading data resolutions. Support any image formats 640*480 or smaller.
The proposed level shifters are for description only, more suitable level shifters can be chosen. Please refer to reference design to have a more detailed implementation.
Frame Rate: 15 fps at VGA resolution **Input system clock:** 13Mhz

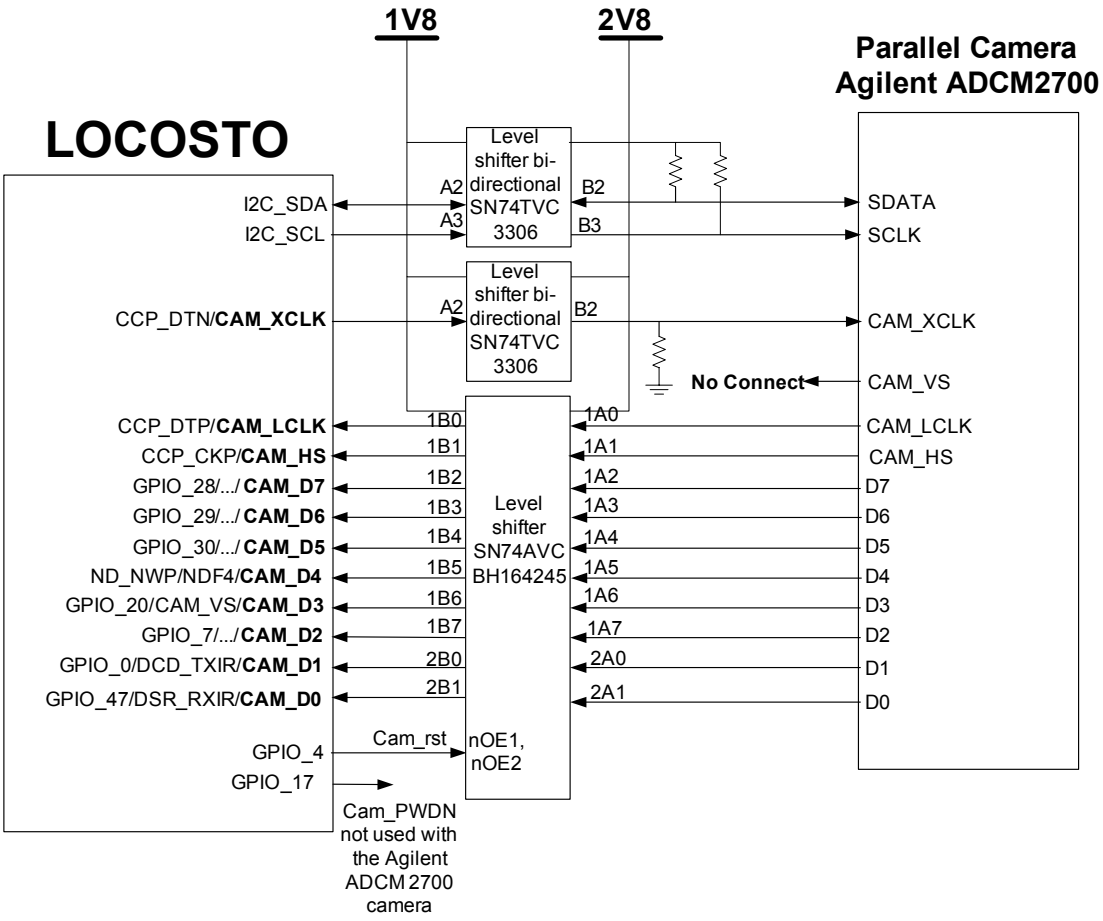


Figure 6 : Camera // connection

- Locosto GPIO_4 (PU at reset) is dedicated to Cam_rst function, but the Agilent ADCM2700 does not have reset pin so the GPIO_4 is used as Output Enable active low for all the level shifters.
- If we need to use a level shifter Output Enable active High instead of active low or we want to use a 1.8V I/Os camera using a reset active Low we can use the GPIO_2 (main peripheral resets) for that.
- The level shifters, when not enabled, must let the Locosto Camera bus in HZ mode because Cam_D0 and Cam_D1 signals are multiplexed, on Locosto, with UART signals that we can use when camera is not used.
- As the Agilent ADCM2700 camera do not have Reset and PowerDown signals so the Cam_Xclk must be fixed (Pull-Down) to avoid any uncontrolled behavior of the camera when not used.
- In the case we use a 1.8V I/Os camera with Locosto we must ensure that the Camera bus is let HZ when the camera Reset is active, in order to be able to use the UART bus.

IRDA/Camera are exclusive and dynamically switched when active !

The Locosto multiplexing gives IRDA signals RDS_Rxir and DCD_Txir muxed with the Cam_D0 and Cam_D1 signals. So, at reset, the camera must be under reset and the camera bus must be in HZ (High Impedance) to let the lines free for UART for boot
We can have this camera bus in HZ under reset using level shifters or a camera that has its bus HZ under reset.

GPIO4 (PU at reset) can be used for nEN for level shifter or for camera nReset. Or,
GPIO 2 (PD at reset, main peripheral reset) can be used for EN for level shifter or for camera Reset.

3.4.1.1.1 Interconnect Description

The camera module connection described below concerns specifically a dedicated AGILENT product, ADCM-2700 in 8 bits mode. Due to its I/O voltage (2.5 to 3.3v), we need to insert external level shifter between LOCOSTO module and the ADCM-2700 camera. Here after is shown the main connection system of a camera module

3.4.1.1.2 LOCOSTO to Level Shifter connection description

LOCOSTO						Level shifter : SN74AVCBH164245				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signals**	**Ball**	**I/O**	**Power**	**Comments**
CAM_D_0	N5	2	I	VDD_IO (on Triton VRIO)	←	2B1	14	O	VRIO	
CAM_D_1	M6	2	I		←	2B0	13	O		
CAM_D_2	G6	5	I		←	1B7	12	O		
CAM_D_3	E7	2	I		←	1B6	11	O		
CAM_D_4	E5	2	I		←	1B5	9	O		
CAM_D_5	B3	3	I		←	1B4	8	O		
CAM_D_6	G7	3	I		←	1B3	6	O		
CAM_D_7	C4	3	I		←	1B2	5	O		
CAM_LCLK	A5	1	I		←	1B0	2	O		
CAM_HS	F8	1	I		←	1B1	3	O		
GPIO_4 (CAM_RST)	R9	0	O		→	nOE1, nOE2	48, 25	I		

LOCOSTO						Level shifter : SN74TVC3306				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signals**	**Pin**	**I/O**	**Power**	**Comments**
CAM_XCLK	C6	1	O	VDD_IO (on Triton VRIO)	→	A2	3	I	VRIO	
GPIO_17 (CAM_PWDN)	B9	0	O		→	NC				

LOCOSTO						Level shifter : SN74TVC3306				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signals**	**Pin**	**I/O**	**Power**	**Comments**
I2C_SDA	N6	0	I/O	VDD_IO (on Triton VRIO)	←→	A2	3	IO	VRIO	
I2C_SCL	R4	0	O		→	A3	4	I		

Table 7 Camera // interface connection

3.4.1.1.3 Level Shifters to ADCM-2700 Camera connection description

Level shifter : SN74AVCBH164245					ADCM-2700 connector				
Signal	**Pin**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
2A1	35	I	2.8V	←	D0	4	O	2.8V	
2A0	36	I		←	D1	5	O		
1A7	37	I		←	D2	6	O		

1A6	38	I		←	D3	7	O	
1A5	40	I		←	D4	8	O	
1A4	41	I		←	D5	9	O	
1A3	43	I		←	D6	10	O	
1A2	44	I		←	D7	11	O	
1A1	46	I		←	CAM_HS	13	O	
No connect				←	CAM_VS	3	O	
1A0	47	I		←	CAM_LCLK	12	O	

Level shifter : SN74TVC3306					**ADCM-2700**				
Signal	**Pin**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
B2	6	IO	2.8V	←→	SDATA	16	I/O	2.8V	PU
B3	5	O		→	SCLK	15	I		PU
Level shifter : SN74TVC3306					**ADCM-2700**				
B2	6	O	2.8V	→	CAM_XCLK	2	I	2.8V	PD

The ADCM-2700 camera module is provided by Agilent on a connector, the ball described into the table above are the pin number associated to each signal.

3.4.1.1.4 ADCM-2700 CAMERA Power consideration :

Supply voltage requirements : 2.65 to 3.1V (we will take 2.8V). 50mV Max noise within 0-1MHz

Power consumption (@ 13Mhz CLK) :

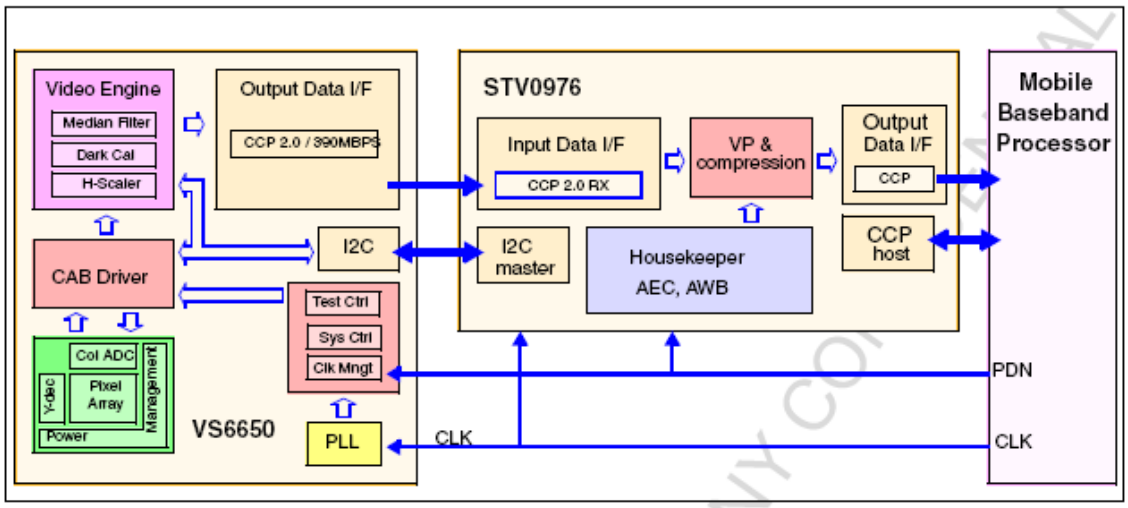
- Normal mode, typical : 42mA.
- Low power mode (Vcc = 2.8V, CLK stopped), typical : 500uA.
- Leakage (Vcc = 0V) : 1.5uA.

3.4.1.1.5 Layout consideration

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W.
- The camera bus must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.4.2 CCP camera connection

The ST Microelectronics VS6650 camera sensor is a 1.0 Megapixel SMIA camera sensor CCP 2.0 serial video 1.8V interface. It has to be used with the ST Microelectronics STV0976 co-processor that connects to Locosto CCP interface. The STV0976 co-processor will provide Locosto compatible protocol : YUV 4:2:2 , RGB 5:6:5 , RGB 4:4:4 , JPEG.



With the co-processor system the clock is sent by host to both the VS6650 and the co-processor.

The high-speed clock for the co-processor is supplied from the VS6650. It is generated using the VS6650 PLL and is provided as the continuous data qualification clock.

Figure 7 block schematic

3.4.2.1 Connections considerations

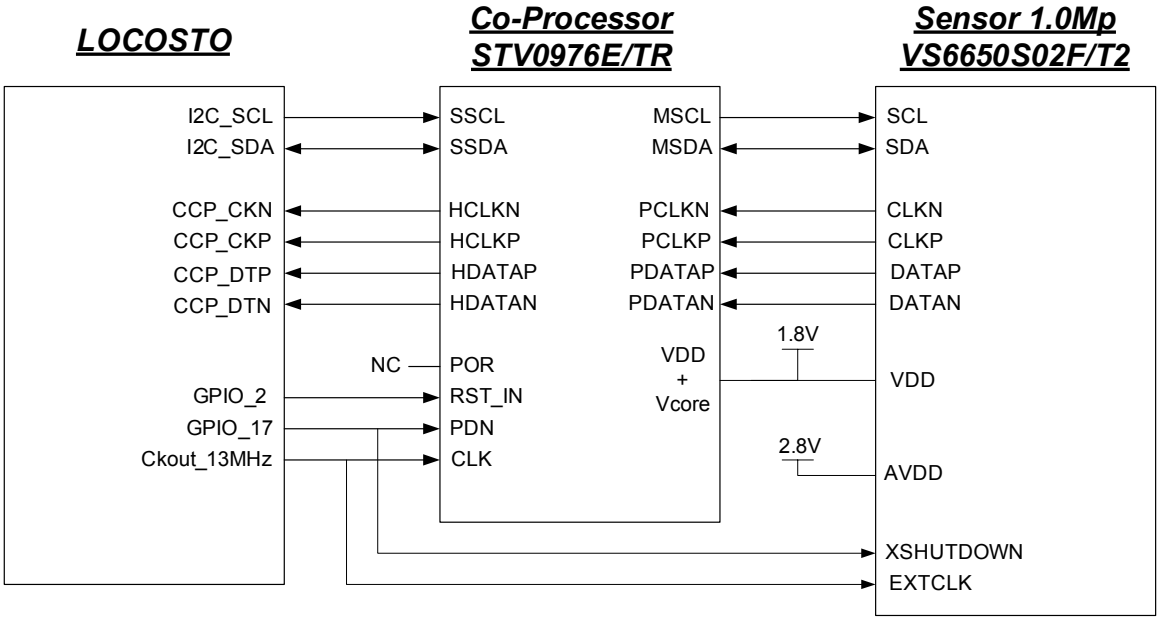


Figure 8 connections schematic

LOCOSTO					STV0976 co-processor					
Signal	**Ball**	**modes**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
CCP_DTP	A5	1	I	VRIO (1.8V)	←	HDATAP	C3	O	VDD/ Vcore	
CCP_DTN	C6	1	I		←	HDATAN	D3	O		

CCP_CKP	F8	1	I		←	HCLKP	C1	O		
CCP_CKN	E7	1	I		←	HCLKN	D1	O		
I2C_SDA	N6	0	I/O		←→	SSDA	D10	IO		
I2C_SCL	R4	0	O		→	SSCL	C10	I		
GPIO_17	B7	0	O		→	PDN	C8	I		
GPIO_2	T3	0	O		→	RST_IN	A5	I		
CLKout_13MHz	N8	0	O		→	CLK	E8	I		

STV0976 co-processor				**Sensor 1.0Mp VS6650**					
Signal	**Ball**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
PCLKP	F1	I	VDD/ Vcore	←	CLKP	10	O	VDD	
PCLKN	G1	I		←	CLKN	9	O		
PDATAP	F3	I		←	DATAP	13	O		
PDATAN	G3	I		←	DATAN	12	O		
MSCL	F8	O		→	SCL	6	I		
MSDA	G8	IO		←→	SDA	7	IO		
POR	A6	NA			No Connect				

LOCOSTO					**Sensor 1.0Mp VS6650**					
Signal	**Ball**	**modes**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
GPIO_17	B7	0	O	VRIO (1.8V)	→	XSHUTDOWN	4	I	VDD	
GPIO_2	T3	0	O		→	EXTCLK	5	I		

Table 8 Locosto to CCP camera connection

Onto the Locosto ballout the CCP pins are internally muxed with the parallel camera control signals (on the same signal mode).

3.4.2.2 Power considerations

STV0976 coprocessor : need 1.8V / 90mA on VDD and Vcore.

Sensor VS6650 : need 1.8V on VDD and 2.8V on AVDD. Total current = 28mA (following ST datasheets)

3.4.2.3 Layout considerations

A special care must be taken for the CCP bus : the frequency being high (208MHz) the following recommendations are mandatory :

- Match the 4 wire length. Line length being as short as possible (less than 4 cm is strongly recommended)
- The lines must be routed in “differential mode” : the two lines routed on the same layer, the distance between the two lines being unchanged all length of the line routing, the distance between the two lines being calculated to have the “differential impedance” required.
- The lines must have controlled impedance.
- Of course avoid multiple impedance break as VIA or connectors.

- The CCP bus must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.5 IRDA IMPLEMENTATION

IRDA interface short description

This interface is described with an Agilent module: The HSDL-3220 IRDA transceiver. It is a low profile (2.5/8/3mm) fast infrared (SIR, MIR and FIR) transceiver that provides interface between 1.8volt logic and IR signals for through-air, serial, half-duplex data link. It is fully compliant to IRDA data physical layer specifications v1.4 fast infrared (up to 4Mbps) and IEC825-Class Eye Safe.

IRDA/Camera are exclusive and dynamically switched when active !

The Locosto multiplexing gives IRDA signals RDS_Rxir and DCD_Txir muxed with the Cam_D0 and Cam_D1 signals. So, at reset, the camera must be under reset and the camera bus must be in HZ (High Impedance) to let the lines free for UART for boot
We can have this camera bus in HZ under reset using level shifters or a camera that has its bus HZ under reset.
GPIO4 (PU at reset) can be used for nEN for level shifter or for camera nReset. Or,
GPIO 2 (PD at reset, main peripheral reset) can be used for EN for level shifter or for camera Reset.

3.5.1 Block diagram

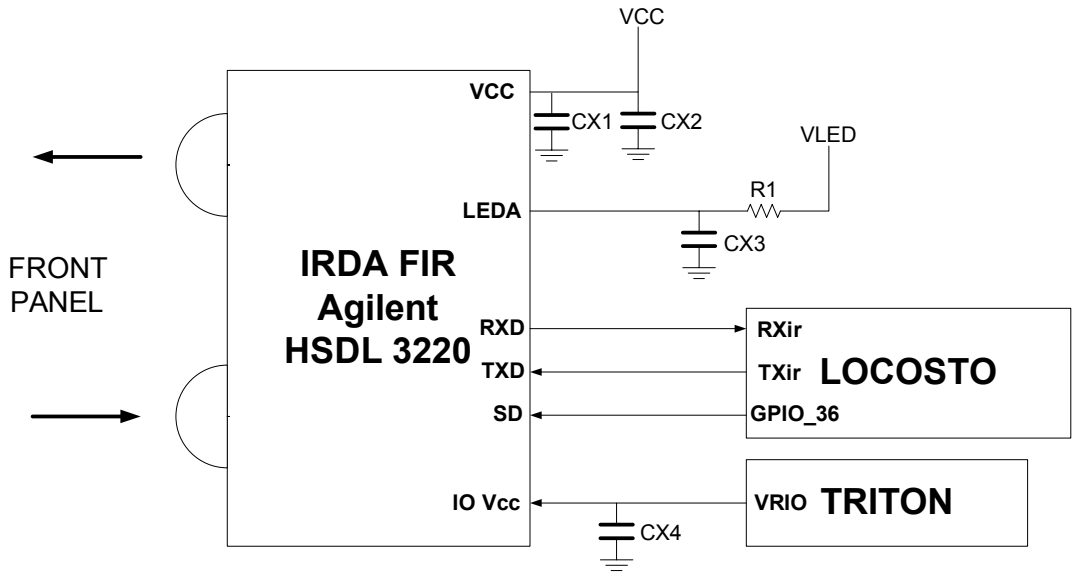


Figure 9 : IRDA connection

3.5.2 Interconnect Description

The IRDA transceiver module can be directly connected to LOCOSTO processor through UART irda interface. LOCOSTO can completely shutdown the transceiver (I/O and diode) through the SD I/O to reduce the power consumption when this link is unused.

The Agilent HSDL-3220 SD pin is connected to the Locosto GPIO36. We chose this solution because the RTS_SDirda Locosto signal is used as UART line for the UART bus and the BT connection. But, if a designer does not use the UART interface for UART bus or BT connection then the RTS_SDirda can be used to connect to Agilent HSDL-3220 SD pin.

3.5.2.1 Connections between LOCOSTO and HSDL3220

LOCOSTO						HSDL3220				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
TXir	M6	1	O	Vdd_io	→	TXD	3	I	VRIO	
RXir	N5	1	I		←	RXD	4	O		
GPIO_36	D2	0	O		→	SD	5	I		

Table 9 : IRDA interface

3.5.3 Power management

The input power supply to the **HSDL3220** is divided in two parts

- VLED and CORE supply 2.7v to 5.5v
- I/O supply 1.8v

HSDL3220						
Power plan	**Power rail Name**	**Pin**	**Nominal voltage**	**tolerance (min – max)**	**Estimated sink current**	**Comments**
Core power	VCC	6	2.8v	2.7 – 3.3	3mA	Shutdown current = 1uA
LED Anode	LEDA	1	3.6v	VBAT	150mA	Supplied via a serial 5.6Ω resistor
I/O ring	IOVCC	7	1.8v	1.8 – 3.6	10uA	

Table 10 : IRDA power consumption

3.5.4 Layout consideration

The following PCB layout guidelines provided by the vendor should be followed to obtain good electrical performance and Electro-magnetic immunity.

- A ground plane should be continuous under and near the part (same layer) except the shield trace.
- The shield trace is connected with a wide, low inductance trace to underneath system ground layer.
- Data signals should be wired on the third layer between two ground layers.

All these physical design requirements are described in AGILENT application note:
http://literature.agilent.com/litweb/pdf/5988-9321EN.pdf

3.6 Main LCD IMPLEMENTATION

Main LCD interface short description

The description of this interface is based on a driver IC from RENESAS : the HD66774 is a gate-driver IC for systems with color-TFT-liquid-crystal dot-matrix graphic displays. It incorporates a circuit for driving 240 channels of TFT gate-line driving all the power-supply circuits that are required for liquid crystal displays.

LCD Philips chipset main features

The LPH8754-2 display has both a microprocessor and video interface. The microprocessor interface is used to select and modify operating conditions. Video data can be written at a frame rate of 60 Hz using the dedicated video interface. For the LPH8754-2 module the preferred micro processor interface is the 80-system. The preferred video interface mode is the RGB interface.

- 8 or 9 bit LCD interface
- Active matrix 2.2" color 176RGB-by-220 TFT LCD module

3.6.1 Block diagram

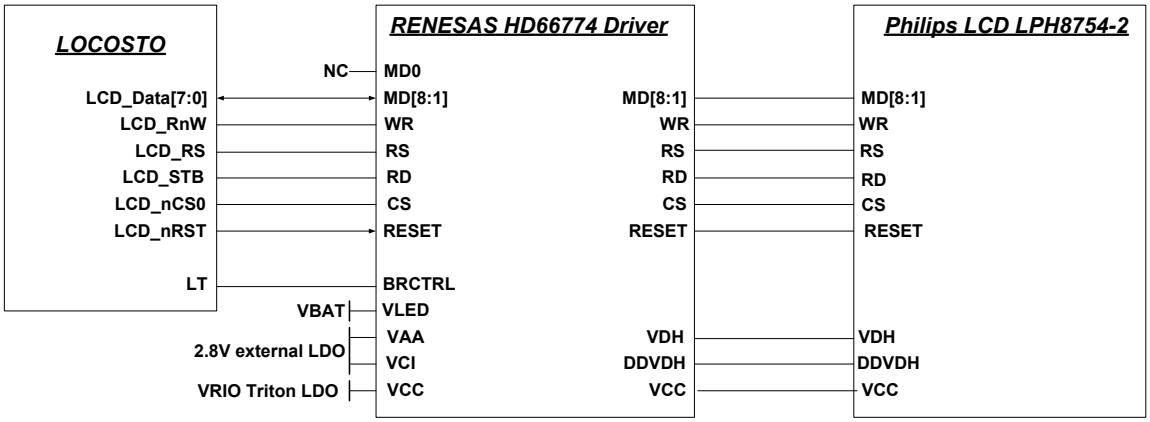


Figure 10 : main LCD connection

3.6.2 Interconnect Description

3.6.2.1 Connections between LOCOSTO and HD66774

The HD66774 module can be directly connected to LOCOSTO processor through its LCD interface. The data for display MD (8..1) are written according to the values of the Chip Select and Reset signals in synchronization with WR, RD and RS signals.

LOCOSTO						HD66774				
Signal	Ball	Mode	I/O	Power	Dir.	Signal	Pin on connector	I/O	Power	Comments
LCD_D0	E9	0	O	VDD_IO	→	MD1	50	I	VRIO	

LCD_D1	B8	0	O		→	MD2	51	I		
LCD_D2	C8	0	O		→	MD3	52	I		
LCD_D3	E8	0	O		→	MD4	53	I		
LCD_D4	B7	0	O		→	MD5	54	I		
LCD_D5	D8	0	O		→	MD6	55	I		
LCD_D6	C7	0	O		→	MD7	56	I		
LCD_D7	B6	0	O		→	MD8	57	I		
LCD_RnW	F9	0	O		→	WR	47	I		
LCD_RS	D9	0	O		→	RS	46	I		
LCD_STB	B10	0	O		→	RD	48	I		
LCD_nCS0	E10	1	O		→	CS	45	I		
LCD_nRST	C10	0	O		→	RESET	58	I		

Table 11 : Main LCD interface

3.6.3 Power management

The display chipset power management is divided in two parts

- HD66774 driver.
- TFT LCD panel power supply.

Philips gives the following numbers as power consumption for the whole solution (driver + LCD) :

_ Active mode : 27mW
_ Standby mode : 30uW
_ Sleep mode : 90uW.

Those numbers have to be confirmed, by Philips, with samples measurements.

3.6.4 Layout consideration

No available information from Philips but the usual following rules are applicables :

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W.
- The LCD bus must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.7 Secondary LCD IMPLEMENTATION

Secondary LCD interface short description

A “Secondary LCD”, physically placed on the top of a clamshell mobile phone is connected to the LOCOSTO SPI 1.8V interface.

The chosen secondary LCD is the TFS (Three-Five System) LCD : this module consists of transflective positive-image FSTN 128x128 black/white monochrome LCD, with a flex interface for insertion in a ZIF connector, JAE FF0115SA2 or equivalent. An integral LED lightguide is also provided. The LEDs, yellow-green, are on the customer's PCB.
This LCD must be connected to the Sitronix ST7541 driver, SPI 4 lines interface.
This solution is 2.8V I/Os so we have to use level shifters to connect to Locosto.

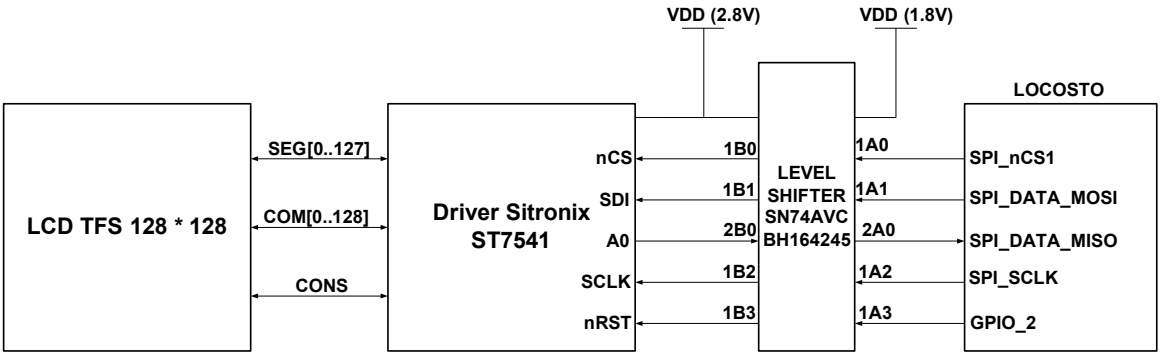


Figure 11 : Secondary LCD connection

3.7.1 Interconnect Description

The LCD TFS 128*128 + ST7541 Sitronix driver module can be directly connected to LOCOSTO on SPI interface.
The SPI CS0 can disable the Sec-LCD to save power when not used.
The SPI CS1 is used by the DM290 TI Camera coprocessor when used. So the SPI bus is shared between the secondary LCD and the DM290 camera co-processor.

LOCOSTO						Level shifters				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
SPI_clk	G9	1	O	Vdd_io	→	1A2	44	I	VRIO	
SPI_data_miso	F7	1	I		←	2A0	36	O		
SPI_data_mosi	C5	1	O		→	1A1	46	I		
SPI_ncs1	G8	1	O		→	1A0	47	I		
GPIO_2	T3	0	O		→	1A3	43	I		

Driver Sitronix ST7541					Level shifters				
Signal	**pin**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
SCLK	7	I	Vdd_io	→	1B2	5	O	2.8V	
A0	5	O		→	2B0	13	I		
SDI	8	I		←	1B1	3	O		
nCS	1	I		←	1B0	2	O		
nRST	3	I		←	1B3	6	O		

Table 12 : Secondary LCD interface

Power considerations :

The power supply need is : 2.8V. Imax normal mode is 500uA. I sleep mode is TBD.

3.8 FM IMPLEMENTATION

The Rohm BH1403AGLU FM stereo radio receiver IC is a build in front end, IF amplifier, FM detector, FM stereo demodulator, and PLL frequency synthesizer. It doesn't need external IF filter and external phase shifter for FM detector. For complete detailed implementation see Annex A. Standby mode and power down of stereo demodulation block by software operation.

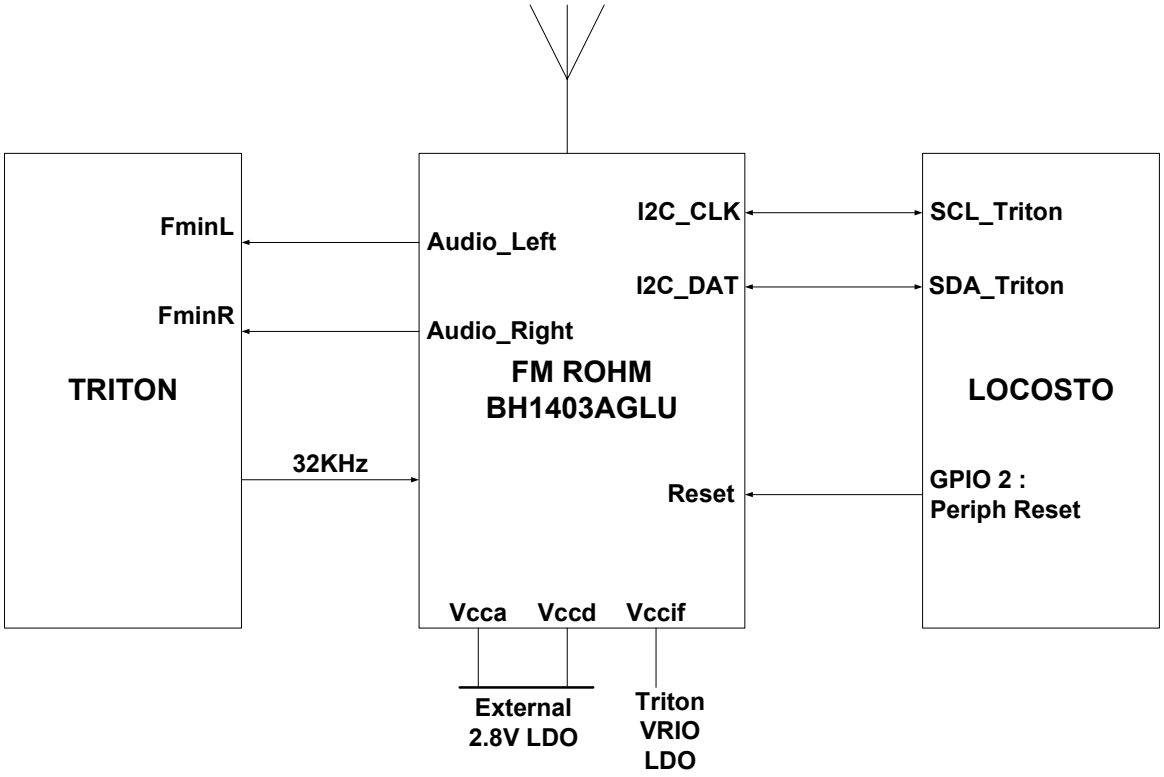


Figure 12 : FM connection

TRITON LITE						FM ROHM				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
FminL (FML)	D3		I	VRIO	←	Audio_Left	27	O	VRIO	
FminR (Auxi_FMR)	C2		I		←	Audio_Right	28	O		
32KHz	K11		O		→	32KHz	18	I		

LOCOSTO						FM ROHM				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
SCL_TRITON	N7	0	IO	VRIO	↔	I2C_CLK	10	IO	VRIO	
SDA_TRITON	R6	0	IO		↔	I2C_DAT	9	IO		
GPIO 2 (Periph Reset)	T3	0	O		→	Reset	15	I		

Table 13 : FM interface

Power supply considerations :

The Rohm BH1403AGLU FM IC must be supplied by :
- _ Vcca (analog) : 2.8V : external 2.8V LDO.
- _ Vccd (digital) : 2.8V : external 2.8V LDO.
- _ VCCif (Interface) : 1.8V : Triton LDO : VRIO.

Rohm is providing the following power consumption informations :
- _ Full system power consumption in active mode : 15mA
- _ in sleep mode : 50uA.
- _ in power down mode :1uA (leakage).

3.9 SIM IMPLEMENTATION

The LOCOSTO Universal Subscriber Identity Module Interface is designed to support many simultaneous smart-card applications such as SIM (GSM), USIM (3GPP), banking (EMV) and loyalty application. This module implements the hardware interfaces to the Smart Card and a sequencer that manages the transmission protocols T-0 and T-1, defined in the ISO7816.3 standard, thus freeing the MCU of the real-time constraints.

In a LoCosto Chip-Set environment, the USIM I/F is restricted for controlling the GSM SIM-card

This Locosto USIM interface can be 1.8V or 3V.
USIM_PBIAS has to be connected to Vdd_USIM through a (100nF : TBC) decoupling Capacitor (non mounted today, the value and the decision to be mounted will be made after tests).
The VSS_Pbias has to be connected to the main VSS.
The SIM card power is coming from the TRITON LITE VRSIM LDO and the SIM card detection pin is connected to the TRITON LITE SIMDTC signal.

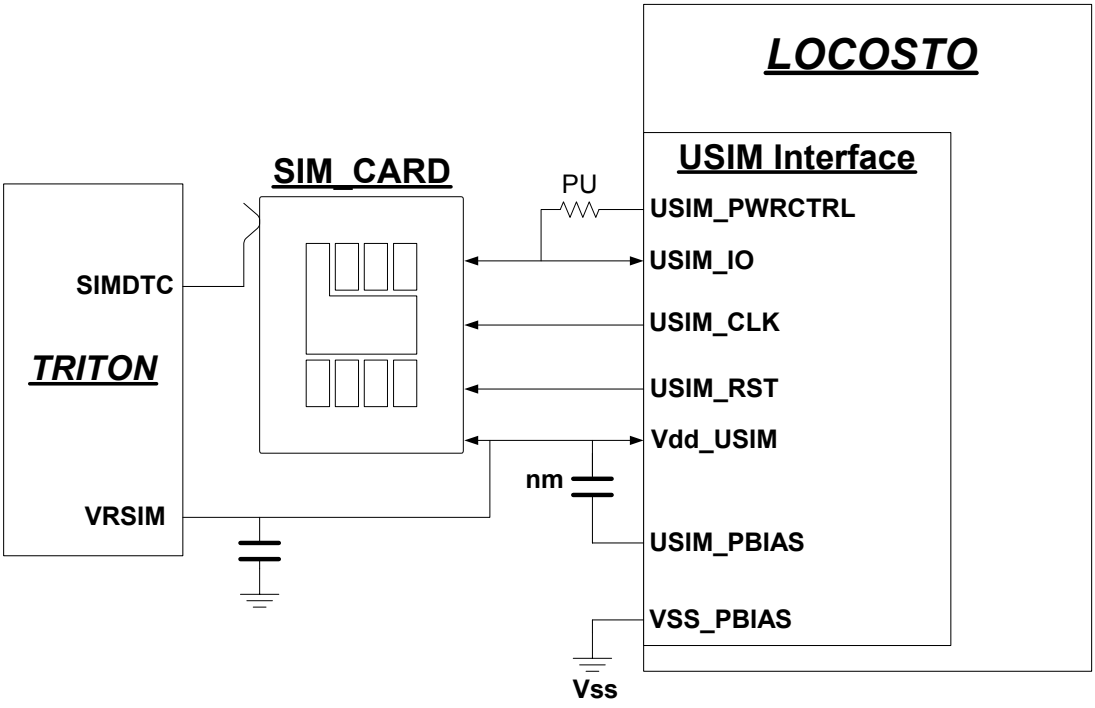


Figure 13 : SIM connection

LOCOSTO						SIM connector				N
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
SIM card										
USIM_IO	R11	0	IO	VDD_USIM	↔	IO	7	IO	VRSIM	
USIM_CLK	P10	0	O		→	CLK	3	I		
USIM_RST	N11	0	O		→	RST	2	I		
USIM_PWRCTRL	M10	0			→	IO	7	IO		1
USIM_PBIAS	T11	0								
VSS_PBIAS	U11	0								
TRITON LITE						**SIM connector**				**N**
SIMDTC	J7			VDD_USIM		SIM DETECT				

Table 14 : SIM interface

Note 1: SIM_PWRCTRL connected to SIM_IO through a resistor

3.10 BLUETOOTH IMPLEMENTATION

Bluetooth interface short description

This interface principally contains the BRF6150 module (Island 2), in a second step we will use Island 3 instead of Island 2. It is a highly integrated Bluetooth device that forms a complete standalone BT wireless communications system. The system battery can directly power it. It integrated a 2.4Ghz radio transceiver needing only an external BALUN and an antenna.

This device implements an advanced solution for the Bluetooth protocol with easy interfacing to the LOCOSTO processor. The firmware running in an ARM7TDMIE processor includes the low layers of the BT protocol up to Host controller interface. A “shut-down” input allows minimizing power consumption when Bluetooth function is not used.

BRF6150 Bluetooth module main features

- Digital radio processor.
- Bluetooth hardware according to BT specification 1.1 and 1.2.
- On chip ROM / RAM.
- Embedded ARM7TDMIE.
- Minimum external components
- Small size package: 4.5x4.5mm, BGA 0.5mm ball pitch package.
- Supports 12 to 40 MHz sine wave fast clock
- Supports Class 2 applications (10meters)
- Supports Class 1 applications (100meters) using an external Power amplifier (not supported by this system description)

3.10.1 Block diagram

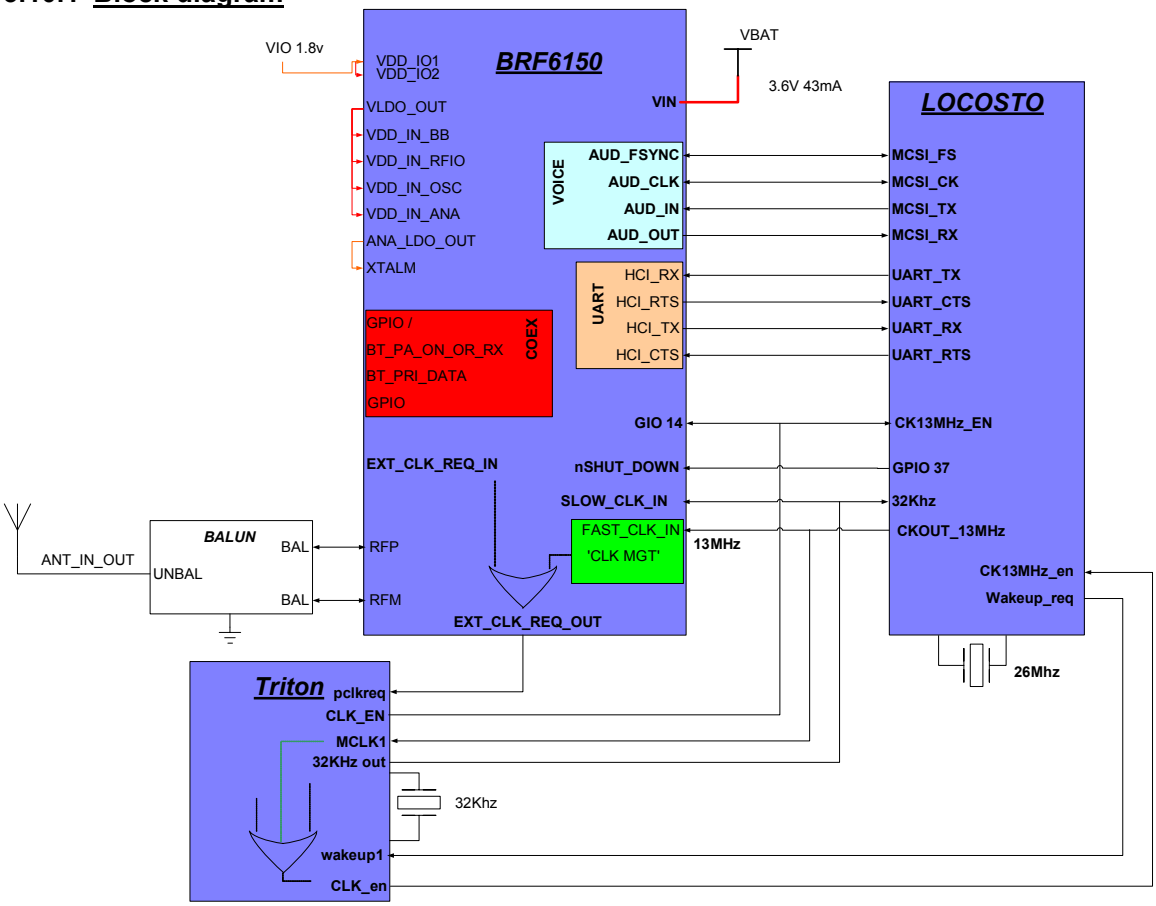


Figure 14 : BlueTooth connection

3.10.2 Interconnect Description

3.10.2.1 Connections between LOCOSTO and BRF6150

DATA: the BRF6150 incorporates one UART module dedicated to the host controller interface (HCI) transport layer. It's a four lines standard UART connection. Voltage levels of signals should match the voltage supplied to VDD_IO power input.
VOICE: The CODEC interface is a fully dedicated programmable serial port that provides the necessary logic, to use MCSI interface to the LOCOSTO processor. In master mode the BRF6150 device provides the clock and the frame synchronization to the processor.
Synchro : To synchronize the BRF6150 scan activity to the Locosto wake-up events the BT IC use the Triton Lite CLK_EN signal (connected on BT GIO 14). This mechanism allows to save power consumption.

LOCOSTO						BRF6150				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
VOICE										
MCSI_FS	M5	1	IO	VDD_IO	↔	AUD_FSYNC	A7	I/O	VDD_IO1 VDD_IO2	
MCSI_CLK	N3	1	IO		↔	AUD_CLK	B6	I/O		
MCSI_TX	K7	1	O		→	AUD_IN	C5	I		

MCSI_RX	P2	1	I		←	AUD_OUT	C7	O		
DATA										
UART_TX	P3	0	O	VDD_IO	→	HCI_RX	E4	I	VDD_IO1 VDD_IO2	
UART_CTS	R2	0	I		←	HCI_RTS	E7	O		
UART_RX	L7	0	I		←	HCI_TX	E5	O		
RTS_SDirda	R3	0	O		→	HCI_CTS	E8	I		
CONTROL										
GPIO_37	H7	0	O	VDD_IO	→	nSHUT_DOWN	E3	I	VDD_IO1 VDD_IO2	A pull down is present into BT IC.

BRF6150					**TRITON LITE**				
Signal	**Ball**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
EXT_CLK_REQ_OUT	D7	O	VDD_IO	→	PCLKREQ	M12	I	VRIO	

Note1: EXT_REF_CLK_OUT enable in shutdown mode.

BRF6150					**LOCOSTO**				
Signal	**Ball**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
FAST_CLK_IN	E2	I	VDD_IO	←	CKOUT_13MHz	N8	O	VDD_IO	

BRF6150					**TRITON LITE**				
Signal	**Ball**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
SLOW_CLK_IN	F6	I	VDD_IO	←	32KOUT	K11	O	VRIO	

BRF6150					**TRITON LITE**				
Signal	**Ball**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
IO_14	B4	I	VDD_IO	←	CLKEN	D10	O	VRIO	

Table 15 : BlueTooth interface

RADIO INTERFACE

BRF6150 ONLY needs two external components to achieve this function: a BALUN and an Antenna.

BRF6150					**BALUN**				
Signal	**Ball**	**I/O**	**Power**	**Dir.**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
RFP	H1	I/O	VDD_IO	←→	Balance	3	I/O	--	Ref. clock request to the EXT_CLK_REQ_OUT – PCLKREQ interface
RFM	H2	I/O		←→	Balance	4	I/O	--	

CLOCK MANAGEMENT

1_ TRITON LITE provides 32Khz slow clock to the processor (LOCOSTO) and its peripherals.

2_ Fast clock (13MHz from a 26MHz Xtal) is provided by LOCOSTO and shared between TWL5002 (AGPS), BRF6150 (BT) and Triton Lite.

3_ BT (EXT_CLK_REQ_OUT pin) can request the fast clock to Triton Lite module (pclkreq pin).

4_ BT clock request is gated (OR) in Triton Lite power IC and directly sent to LOCOSTO chip/module to enable the 13MHz clock generation.

3.10.3 Power management

The BRF6150 device requires two kinds of power source:

- System battery directly supplies CORE through the power management island. This part of the module integrated LDO to power supply core, RFIO and analog parts of the module.
- TRITON LITE I/O DCDC (1.8v voltage level) supplies I/O interface

The regulated outputs of all the on-chip regulators are available on external pins and should be routed on the application PCB to other respective blocks power supply pins of the BRF6150. Except Power off, power management can put the device in following modes:

1. **SHUTDOWN :** All circuits are shut down and the device is not functional.
2. **DEEP SLEEP :** The only active portion of the device is the slow clock digital part and the digital LDO.

3.10.3.1 BRF6150 Power requirements

Following table shows Power supply needed connections.

BRF6150						
Plan	**Power rail Name**	**BALL**	**Nominal voltage**	**tolerance (min – max)**	**Max sink current**	**Comments**
POWER						
All LDO	VBAT	H6	3.6V	-0.5v – 5.4v	52mA	Supplied by Main Battery
I/O ring	VDD_IO	D8, G7, A3	1.8v	1.65 – 3.6	20mA	Supplied by TRITON LITE
CORE + LDO	VLDO_OUT	G5	1.8v			Supplied by an internal LDO
SLOW CLOCK	VDD_IN_BB		1.8v			Supplied by an internal LDO (VLDO_OUT)
Keep Alive	KA_OUT	G6				Not used.
GROUND						
Digital GND	VSS	Digital ground		B8, G8, H7, A5, A2		
Analog GND	VSSA	Analog GND		F4, H4, D1, G1, G2, F3		

Table 16 : BlueTooth power consumption

BLUETOOTH interface is powered by

- TRITON LITE module, described in the "TRITON LITE" paragraph
- The Main Battery described in the "Battery" paragraph of the Global system description. Click on the Blue link to get more information.

Routing considerations :

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W.
- The buses must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.11 A-GPS IMPLEMENTATION

Here is shown a global connection system of aGPS function. ***The AGPS HW connection described herebelow is supported by the HW but not supported by the SW so for a full AGPS feature support some software adaptation has to be done.***
As it is described on the diagram below, the main function of the aGPS is ensured by a TI component, GPS5002, but this aGPS function needs also GPS RF receiver, which is a TI component, TRF5101. A power management and a GPS signals filter complete this diagram.
The GPS receiver can, during initial acquisition, fully search in parallel all code phases of up to 8 received GPS signals.
The TRF5101 needs a 2.8V LDO separated of Triton Lite 2.8V LDO due to noise constraints.
The chip supports the three assistance modes of operation:
Totally autonomous
Semi-autonomous:
In semi-autonomous operation, the navigation solution is computed in the chip using information from an auxiliary communication system, such as a cell phone—this greatly improves system sensitivity and acquisition time.
Wireless-assisted operation:
In wireless assisted operation, the chip computes code phases and other measurements using information from an auxiliary communication system and provides this data to a remote server for a final position calculation. Assisted modes provide greatly improved sensitivity, accuracy and acquisition performance.

3.11.1 Block diagram

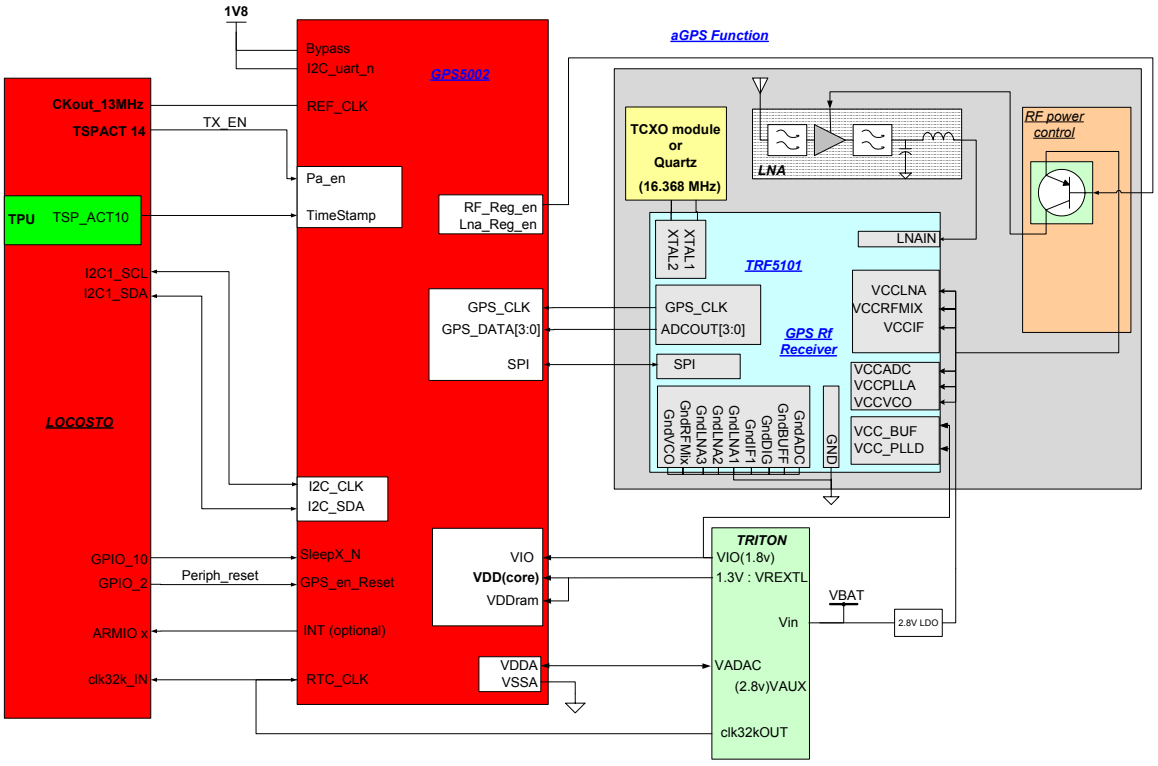


Figure 15 : AGPS connection

3.11.2 Interconnect Description

3.11.2.1 Connections between LOCOSTO and GPS5002

It controls GPS5002 module through an I2C bus.
To correctly start the aGPS function, after Core power on, the “SLEEP_N” has to be driven high at least 4ms before “GPS_EN_RESET” signals. Under reset these pins are configured with a low level disabling the start or the sleep modes of the GPS module. After the correct power up system, these pins are put in GPIO mode to control the GPS function.

LOCOSTO						GPS5002				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
Configuration and control										
GPIO_10	C11	1	O	VDD_IO	→	SLEEPX_N	C1	I	VRIO	Pull down at reset Time
GPIO_2 (Periph_Reset)	T3	0	O		→	GPS_EN_RESET	D2	I		
ARMIO_X	TBD		I		←	INT_U1CLK	F1	O		Optional
Data										
I2C_SDA	N6	0	IO	VDD_IO	↔	I2C_SDA	B1	I/O	VRIO	
I2C_SCL	R4	0	O		→	I2C_CLK	A1	I		

The GPS5002 “Timestamp” signals have to be controlled by an Locosto TPU interface, due to the system accuracy needed.

LOCOSTO						GPS5002				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
TSP_ACT10	B11	2	O	VRIO	→	TIMESTAMP	E2	I	VRIO	

The power amplifier information (PA_EN) is directly given by LOCOSTO DRP2 module through its TSPACT 14 signal (TX_EN). This “External blanking” function is used to eliminate processing data during transmission of a co-located communication transmitter (DRP).
LOCOSTO provides the 13Mhz system clock from a 26MHz Xtal. An AGPS internal clock Slicer, that allows the sine wave clock conversion in an internal logical clock, must be bypassed using a pull-up resistor on the bypass pin.

LOCOSTO						GPS5002				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
TSPACT 14	E12	0	O	VRIO	→	PA_EN	A2	I	VRIO	Indicates when cellular PA is on (TX_EN)
CKout_13MHz	N8	0	O		→	REF_CLK	G1	I		Reference clock

Table 17 : AGPS interface

3.11.2.2 Connections between TRITON LITE and GPS5002

TRITON LITE module only provides the Real time clock, shared with LOCOSTO, AGPS, BT modules. It is a 32,768 KHz slow clock with a 1v8 logical level.

TRITON LITE						GPS5002				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**Comments**
CLK32OUT	K11	--	O	VRRTC	→	RTC_CLK	A3	I	VRIO	32K sleep clock

3.11.2.3 GPS Reference clocks

- There is a High-speed VCTCXO clock on the AGPS module directly, known as GPSCLK, at a frequency of 16.368 MHz. This temperature-compensated VCXO is required for optimal AGPS performance when the accuracy of the input High-speed reference clock REFCLK is known to (or is determined to be) less than the accuracy of the GPSCLK (TCXO). Such situations exist when the Modem is powered on but not locked to the network, when the Modem is powered off, or when the SDP Big-board clock feeds the AGPS module.
  The AGPS module TCXO is specified to have an accuracy of 1 PPM.
- The High-speed (e.g. 13 MHz) reference clock (REFCLK) in this system is nominally sourced by the Modem. The performance specification of the REFCLK at the AGPS input is as follows: +/-1.5 PPM initial, +/-4 PPM with aging, +/-0.5 PPM when locked to network. The latter spec relates to the accuracy achievable from the specific air interface when the Modem is locked to the network base station, and may in practice achieve 0.1-PPM level.
-

3.11.2.4 GPS5002 Power requirements

The **VDDCORE** and the **VDDRAM** (internal memory power) need an external 1V3 power supply.
The **VDDIO** and **VDDA** (clock slicer power) need an external 1V8 power supply.
The core supply should be powered up at the same time as, or prior to the IO power supply. Similarly the core supply must be powered down after the IO power supply. The VBAT power supply is used as the input voltage. GPS5002 I/Os are not failsafe, they must be powered by the same source than Locosto I/Os : TRITON LITE VRIO.

GPS5002						
Plan	**Power rail Name**	**BALL**	**Nominal voltage**	**tolerance (min – max)**	**Max sink current**	**Comments**
POWER						
I/O ring	VDDIO	B6, C2, C7, G4, G6	1.8v	1.71– 1.89	6mA	
Analog Macro	VDDA	G2	1.8v	1.71– 1.89	400uA	
RAM	VDD	B7, E7	1.3v	1.235– 1.418	14mA	
CORE	VDDCORE	B3, B5, D7, F2, G3, G5	1.3v	1.235– 1.418		
GROUND						
Digital GND	VSS	Digital ground		C3, C4, C5, C6, D4, D5, D6, E3, E4, E5, E6, F5, F6		
Analog GND	VSSA	Analog GND		H1		

Table 18 : AGPS power consumption

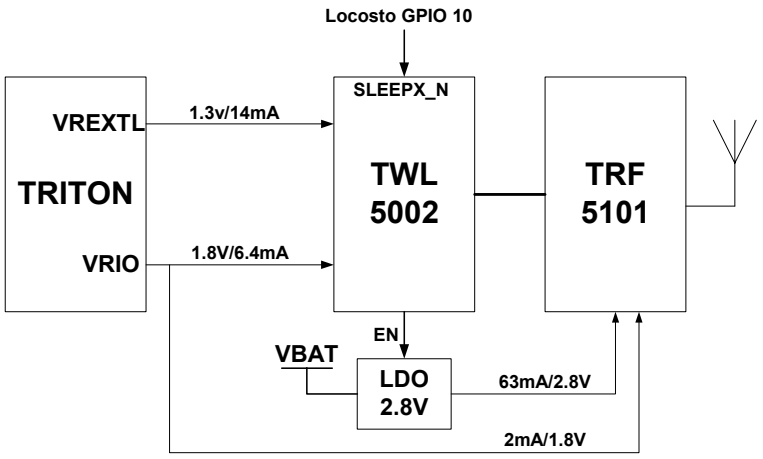


Figure 16 : AGPS power connection

3.11.2.5 GPS RF Receiver (TRF5101) power requirements

As for the GPS5002 chip, there is a power-up and power-down sequencing to take into account for a right function. See the datasheet manual for more details.
The diagram below shows the different power sections to be supplied. To achieve that, three power supplies are used:

- ✓ The same 1V8 source used for the VDDIO of aGPS module is also connected to the VCC_BUF and VCC_PLLD pins.
- ✓ An external 2.8V LDO is dedicated to the remaining analog power pin : VCC_LNA, VCC_Mix, VCC_IF, VCC_ADC, VCC_PLLA and VCC_VCO.
  Low noise amplifier regulator enable is used to power off the LNA when the RF acquisition is not active to reduce system power consumption and is software controlled. This function uses the I2C bus between the GPS5002 chip and LOCOSTO.

This power system based on the control of the different power supplies sources, will allow a global control of the aGPS section by the LOCOSTO. It will improve the power consumption control.

TRF5101 + RF						
IC	**Power rail Name**	**BALL**	**Nominal voltage**	**tolerance (min – max)**	**Max sink current**	**Comments**
	VBAT		3.6v			Supplied by Main Battery
TRF5101	VCCPLLA	A7	3.0	2.7-3.3	63mA	Supplied by 2V8 LDO
	VCCVCO	A3, A5				
	VCCLNA	B1				
	VCCRFMIX	E1				
	VCCIF	F1				
	VCCADC	F2				
	VCC_BUF	E6	1.8v	1.71-1.89	2mA	Supplied by TRITON VRIO
	VCC_PLLD	D6				
GROUND						
Low noise amplifier grounds	GNDLNA1	C1				
	GNDLNA2	D2				
	GNDLNA3	C2				
digital Grounds	GND GNDDIG	C4, C5, C6, D3, D4, D5, E3, E4, E5, F5				
Other grounds	GNDVCO	B2				
	GNDRFMIX	E2				
	GNDF	F3				
	GNDADC	F4				
	GNDBUFF	F6				

Table 19 : AGPS power connection

aGPS interface and attached RF are powered by

- TRITON LITE module, described in the "TRITON LITE" paragraph
- The Main Battery described in the "Battery" paragraph of the Global system description. Click on the Blue link to get more information.

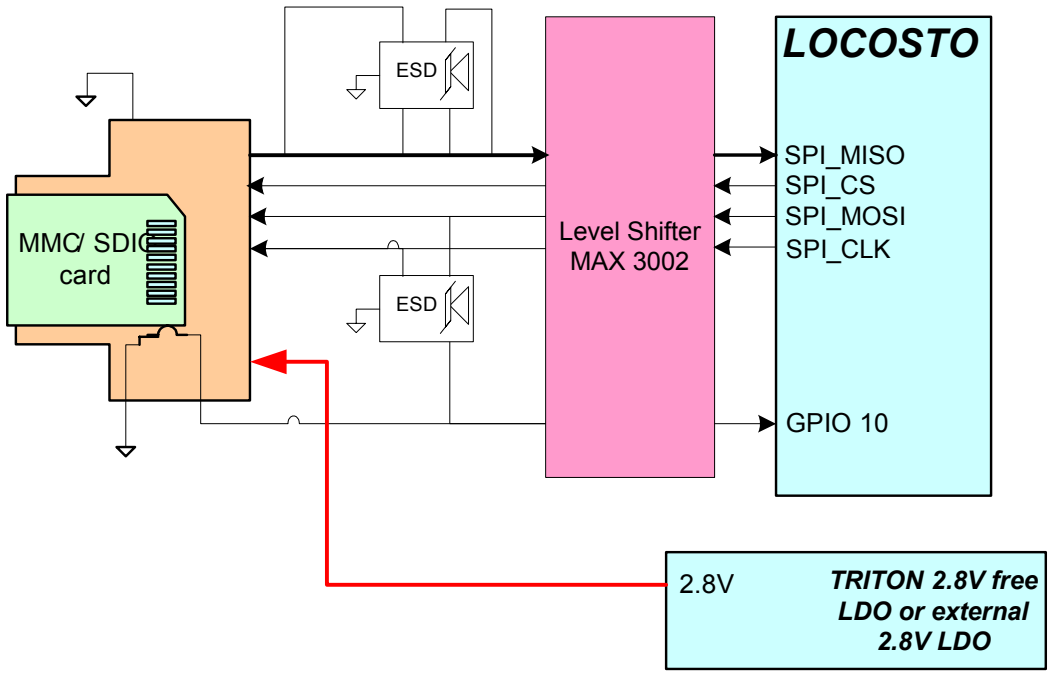
Routing considerations :

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W.
- The buses must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

3.12 Optional MMC/SD card on SPI bus

Locosto doesn't have a dedicated MMC/SD interface, but a MMC/SD card can still be connected to the SPI bus on the CS0 or CS1 or CS2.
The Locosto SPI interface is 1.8V I/O voltage, so can be connected directly to a 1.8V MMC/SDIO card. But, as the market today is more 3.3V I/O card, I've descrived the connection Locosto SPI to a 3.3V MMC/SD card *THROUGH a level shifter*.

3.12.1 Block Diagram



The MMC/SD card need a 2.8v power supply (up to 100mA). This power can come from a free Triton Lite LDO or from an external added LDO depending of the customer implementation.

3.12.2 Interconnect description

When a card is inserted in the connector, a switch detects its presence and grounds the corresponding card detect signal of Locosto.
Locosto then try to access read or write the present memory.
We don't have the possibility to make a mechanical distinction between MMC and SD card presence. This action is processed by Locosto software. It tries to access to the card with a MMC protocol first. If the card doesn't rightly answer the module try a SD protocol access.
The connector described in the block diagram is an SMK 3-in-1 connector.

3.12.3 Connections between Locosto SPI and MMC/SD connector

Locosto						Connector				
Signal	**Ball**	**Mode**	**I/O**	**Power**	**Dir.**	**Signal**	**Pin**	**I/O**	**Power**	**Comments**
SPI_CLK	G9	1	O	VDDIO	→	CLK	5	I	2.8V	
SPI_MISO	F7	1	I		←	D0/DAT0	7	O		
SPI_MOSI	C5	1	O		→	DI/CMD	2	I		
SPI_CS1	G8	1	O		→	CS/DAT3	1	I		
GPIO_10	C11	1	I/O		←→	Card Detect	NA	O		

The connection is done through a level shifter MAX3002 not described into the table.

3.12.4 Power requirements

MMC						
Power plan	**Power rail Name**	**PIN**	**Nominal voltage**	**tolerance (min – max)**	**Max sink current**	**Comments**
Power slot1	VRMMC	4	3.0v	2.7 – 3.6	Write: 33mA Read: 100mA	Maximum is reached by MMC card use.
Ground plan	**Power rail name**	**Definition**		**Pins list**		**Comments**
Slot1 GND	GND1	Connector ground		3, 6, 10, 19, 20, 21, 23, 25		

3.12.5 Layout consideration

For a reliable board design we must follow the following rules :

- Minimize and equilibrate all data and clock Wire length.
- Blend system clock (Strip line).
- Wire data and clock on separated layer (internal layer for clocks).

The connector will have to stand mechanical effort from the user plugging his card. Blended connector prevents two potential problems.

- Frequency transmission from high-speed logic as clock outside the system.
- Fragility of light connector especially on their connection with the card. A blended connector can be soldered.
- A separate ESD protection (exemple : Philips solutions) is required for each slot in order to adhere to IEC 61000-4-2 level 4 specification.

4 Global Power distribution implementation

For more complete detailed system power management description and explanation please see
the **" Locosto chipset power management_system_DAD_88_06_05_01795 "** document.

4.1 System power domain

Power generation and distribution for the global system is provided by the Triton Lite IC.
Moreover AGPS module (TWL5002) needs an additional 2.8V LDO to ensure a low noise supply. Additional power is also provided by an external 2.8V regulator (LDO) to peripheral devices.

This paragraph describes Locosto chip power domains and their estimated maximum current consumption. Locosto chip is intended to receive pre-regulated supplies by the means of the associated ABB chip (Triton Lite). Thus no direct connection with the main battery has to be supported by the Locosto chip.
Below a summary of addressed power domains:

Locosto specific (from Triton Lite)
DRP_CORE 1.3V
DRP_VR1 2.8V
DRP_VR2 2.8V
DBB_VDDCORE same as (DRP_CORE) 1.3V
DBB_RST same as (DRP_CORE) 1.3V
DBB_Vpp same as (DRP_CORE) 1.3V
DBB_VDDMEM (memory interface and memories) 1.8V
DBB_VDPLL 1.3V
DBB_APLL 1.3V
DBB_VDDIO 1.8V
DBB_VDDSIM 3V/1.8V
DBB_APC 2.8V

Application specific (from Triton Lite)
USBIO's driver 3.3V (Client only)
Analog Audio 2.8V
Charger 20V (to Triton)
Vibrator driver 2.7V
Main LCD 1.8V I/Os
Blue Tooth 1.8V I/Os
AGPS (TWL5002) 1.8V, 1.3V
IRDA 1.8V
Memories I/Os and core (NOR, PSRAM, NAND) 1.8V

Application specific (from VBAT)
Triton Lite
Hands free (Triton Lite)
Camera
Blue Tooth VBAT core
AGPS (TRF5101 : RF part) 2.8V
Main LCD 2.8V core
Secondary LCD VBAT
FM 2.8V
IRDA VBAT, 2.8V
Power Amplifier (PA)
Led

Here below the table describes the current consumption per voltage for each peripheral IC (based on manufacturer datasheets). This study allows estimating the current need per voltage for the full system then deciding the connection with the Triton Lite LDOs, also taking account of the noise constraints

	VBAT 3,6V (Active)	VBAT 3,6V (Stdby)	2,8V (Active)	2,8V (Stdby)	1,8V (Active)	1,8V (Stdby)	1,5V (Active)	1,3V (Active)	1,3V (Stdby)
BT ISLAND 2 (BRF6150)	52mA	17uA (sleep mode) 5uA (shutdown mode)			20mA	TBD			
AGPS TWL 5002					6,4mA	TBD		14mA	TBD
AGPS RF : TRF5101	Vbat supply an external 2,8V LDO (63mA) to supply the TRF5101 only.	TBD			2mA	TBD			
Main LCD : LCD Philips + Hitachi ctlr			11mA	TBD					
Sec LCD : TFS LCD + Sitronix driver			1,5mA	TBD					
FM : Rohm BH1402GLU			15,5mA	50uA (sleep mode)	not relevant	TBD			
Camera VGA Agilent ADCM-2700			42mA	500uA (if 2,8V active and CLK down) 1,5uA : @ 0V					
IRDA FIR Agilent HSDL3220	150mA	TBD	3mA	1uA	10uA	0			
	VBAT 3,6V (Active)	VBAT 3,6V (Stdby)	2,8V (Active)	2,8V (Stdby)	1,8V (Active)	1,8V (Stdby)	1,5V (Active)	1,3V (Active)	1,3V (Stdby)
Sum : I per V	265mA		73mA	551uA	28,4mA		G-E needs	14mA	
Locosto					45mA			140mA	
Triton Lite					30mA				
SUM	VBAT		need external LDO 2,8V/100mA		Triton Lite VRIO =28,4 +45 +30+70(memory IC's)+15 (Vdd_mif) = 188,4mA		LDO of 100mA when G-E	TRITON LITE VREXTL	

NOR Spansion : S29N5016J (Supplied from Triton Lite)	**40mA**	**9uA**
PSRAM Spansion S71NS064JA0 (Supplied from Triton)	**20mA**	**120uA**
NAND Samsung K9F1G08 (Supplied from Triton)	**10mA**	**10uA**
	70mA needed by the memories and supplied by Triton VRMEM	

Table 20 : System power distribution view (based on manufacturers data)

The scheme below represents the full system power connections, i.e. the Triton Lite LDOs + external LDOs and the Locosto and peripheral devices that are supplied by Triton Lite and the external LDOs.

Warning : The choice of the GPIOs used for the peripheral devices resets, power down, sleep, … are chosen taking care of their PU or PD state at Reset. For example GPIO 2 has been chosen as “periph reset“ because it is PD at reset so all the peripheral devices will be under reset during boot.

Remark : Concerning the RF supply, we have chosen : VR1 (Locosto) supplied by Triton Lite VRMMC and VR2 (Locosto) supplied by Triton VREXTH. This to reduce the risk of a noise pollution between the two parts of the RF. But another solution is currently under investigation and can be decided only after measurements. The solution that would allow removing the external 2.8V LDO, would be to use only one Triton Lite 2.8V LDO (VREXTH, VRMMC is not possible because it has to be enabled by SW that will work only if we have the 26MHz CLK that is supplied by VR2 …) for VR1, VR2 and DCXO.This solution will be confirmed after Power management measurement and characterization on Validation platform.

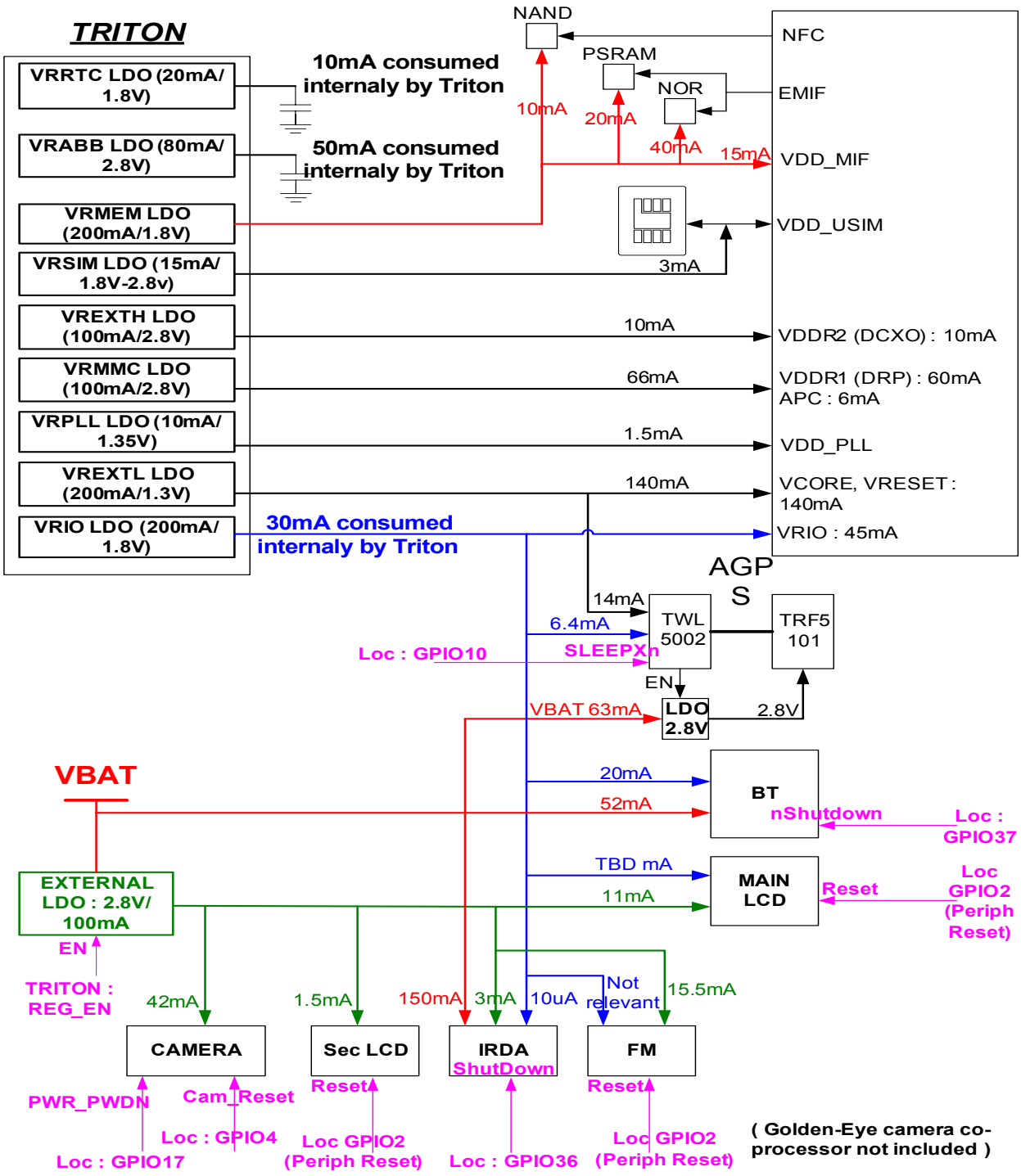


Figure 17 : Full system power domains connections

4.2 Global Power requirement

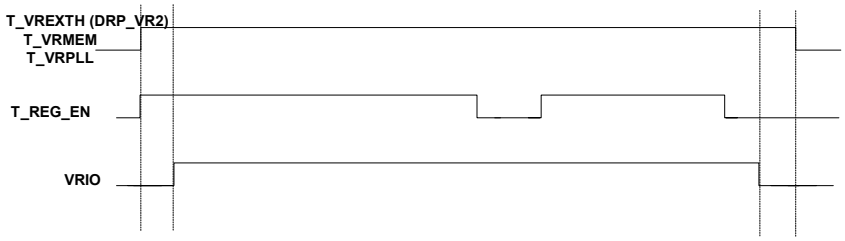
INTERFACE/ PERIPHERAL DEVICE	Signal name	Range value	Typical Value	Current Estimated	Voltage source	Voltage name	Comments
EMIF + NFC	VDD_MIF	1.7-1.95	1.8v	85mA	TRITON	VRMEM	
Tx module	VBAT	3.0 – 5.5	3.6V	2 to 3 A	Battery	VBAT	
Locosto Internal DCXO	VDDR2	2.7 – 2.95	2.8V	10mA	TRITON	VREXTH	
Locosto Internal DRP and APC	VDDR1 and APC_VDO	2.7 – 2.95	2.8v	DRP : 60mA APC : 6mA	TRITON	VRMMC	
SIM	VDD_USIM	2.7 – 2.95	2.8v	3mA	TRITON	VRSIM	
Locosto Internal PLL	VDD_PLL	1.24 – 1.365	1.35V	1.5mA	TRITON	VRPLL	
Locosto core	Vdd_dbb	1.24-1.365,	1.3V	140mA	TRITON	VREXTL	
	Vpp	2.0V max					
	Vdd_rst	1.0-1.89					
Locosto I/Os	VDD_IO	1.71-1.89	1.8V	45mA	TRITON	VRIO	
Main LCD	VCC	2.744-2.856	2.8V	11mA	External 2.8V LDO	LDO 2.8V output	
	VCCI	1.7-3.6	1.8V	TBD	TRITON	VRIO	
BRF6150	VBAT	-0.5 – 5.4	3.6V	52mA	Main battery	VBAT	
	VDD_IO1 VDD_IO2	1.65 – 3.6	1.8v	20mA	TRITON	VRIO	
GPS5002 + RF	VDDCORE	1.235– 1.418	1.3v	14mA	TRITON	VREXTL	
	VDDRAM	0.99-1.11	1.05v				
	VDDIO VDDA	1.71– 1.89	1.8v	6mA		VRIO	
	VDDA	1.71– 1.89	1.8v	400uA			
	VCCLNA VCCIF VCCPLLA VCCADC VCCVCO	2.7-3.3	2.8v	63mA	External AGPS 2.8V LDO	LDO 2.8V output	Generated from VBAT.
	VCC_BUF VCC_PLLD	1.71-1.89	1.8v	2mA	TRITON	VRIO	
	VDD.IO	1.65 - 1.95	1.8v	5mA			
Sub LCD	VDD	2.69-2.81	2.8v	1.5mA	External 2.8V LDO	LDO 2.8V output	
Camera	VDD	2.65-3.1	2.8V	42mA	External 2.8V LDO	LDO 2.8V output	
Irda	VDD I/Os	1.8-VDD1	1.8V	10uA	TRITON	VRIO	
	VDD1	2.7-3.6	2.8V	3mA	External 2.8V LDO	LDO 2.8V output	
	VDD2	NA	3.6V	150mA	Main battery	VBAT	
FM	VDD	2.4-4.0	2.8V	15.5mA	External 2.8V LDO	LDO 2.8V output	
	VDD IOs	1.7-4.0	1.8v	Not relevant	TRITON	VRIO	

Table 21 : Detailed system power consumption

4.3 Peripheral specific

- **External LDO**

Triton LDOs can be not sufficient to supply all the peripheral devices. This document is based on a components list that needs an external LDO 2.8V/100mA supplied by VBAT. But a different component list (less components or less power consuming components due to lower features) can carry out as no need of external LDO.
This external LDO is enabled by the Triton Lite REG-EN signal.
Triton Lite REG_EN goes up with VRMEM, VREXTH, VRPLL (before VRIO) then can be switched of if we want to cut the external LDO or then switched up to re-activate the external LDO.
This REG_EN signal is powered by VBAT, and not by VRIO, so its V_H is not 1.8V but Vbat.



Remark : the external LDOs can be enabled directly by VBAT in certain cases when the external LDO doesn't have to be put off.

- **Periph-Reset signal**

The Locosto GPIO 2 is chosen to be the "peripheral-reset" signal. That means that GPIO 2 will be connected to all the reset pins of the peripheral devices.

- **I2C topology**

Locosto embed two I2C buses :

- The first I2C bus can support master or slave devices connected to Locosto. On this bus we have Locosto (master), AGPS (master), Camera (slave).
- The second I2C can only support slaves devices connected to Locosto. On this bus we have Locosto (master), Triton Lite (slave), FM (Slave).

The devices connected onto the I2C buses haven't fail-safe I/Os, so the Triton Lite VRIO LDO, that supply Triton Lite/Locosto/peripheral devices I/Os, must be let ON even during the peripheral devices power switch off. This to avoid current leakage.

- **13MHz Clock**

The Locosto DBB IC provides a digital 1.8V square 13MHz clock to Triton Lite, BT and AGPS.
Locosto can drive up to 100pF as Triton Lite load is 12pF, BT and AGPS are about 30 pF each.

- **VBAT**

The battery provides the **VBAT** that can be **3.0V to 5.5V (3.6V typical)**. Several devices on the system (BT, AGPS, Sec LCD, IRDA in our example) are directly connected to VBAT thus the board designers have to take care that the devices input may not accept a VBAT range from 3.0V to 5.5V, so the boards designers have to add clamping diodes to do not break the devices supplied directly by VBAT.

- **Accepted batteries technologies**

Triton Lite device is able to manage supply coming from Li-Ion, Li-polymer and Ni-Mh batteries. Connection to a backup battery is optional.(In case of no backup battery, backup battery input will be connected to main battery).

- **I/Os fail safe**

" I/O fail safe definition :

_ If the peripheral device I/Os are Fail Safe so when the Locosto is supplied and the peripheral device is OFF (and its I/Os fail safe are also OFF = not supplied) so we will not have any current leakage.

_ If the peripheral device I/Os are NOT Fail Safe so when the Locosto is supplied and the peripheral device is OFF (and its I/Os fail safe are also OFF = not supplied) so we WILL HAVE current leakage.

So having a peripheral device with I/Os fail safe is better for power consuming point view. But if we have a peripheral device NOT I/Os fail safe we have to let the peripheral IC I/Os supply ON (VRIO) when the peripheral IC core is OFF (or in sleep mode), this to reduce the current leakage.

- **DC/DC not used**

Concerning Triton Lite schematic when DC/DC not used (Locosto configuration) :

_ the VCC1 input must be connected to Vbat (the DCDC is not used but some internal gates can use it anyway).

4.4 Power supplies available

4.4.1 BATTERIES Connection

Main Battery				BRF6150				
SIGNAL	Pin	I/O	POWER	SIGNAL	Ball	I/O	POWER	COMMENTS
VBAT	Output	O	3.6v	VBAT	H6	I	3.6v	

Main Battery				AGPS : GPS 5002				
SIGNAL	Pin	I/O	POWER	SIGNAL	BALL/ Pin	I/O	POWER	COMMENTS
VBAT	Output	O	3.6v	Specific 2.8V LDO		I	3.6v	

Main Battery				IRDA Agilent HSDL 3220 FIR				
SIGNAL	Pin	I/O	POWER	SIGNAL	Pin	I/O	POWER	COMMENTS
VBAT	Output	O	3.6v	LED A	1	I	3.6v	

Main Battery	TRITON LITE	

SIGNAL	Pin	I/O	POWER	SIGNAL	BALL	I/O	POWER	COMMENTS
VBAT	Output	O	3.6v	VBAT	A10	I	3.6v	
VBAT	Output	O	3.6v	Vcc1	H10, H11, H12	I	3.6v	
VBAT	Output	O	3.6v	Vcc2	L7, L8	I	3.6v	
VBAT	Output	O	3.6v	Vcc3	B2	I	3.6v	
VBAT	Output	O	3.6v	Vcc4	F11, F10	I	3.6v	
VBAT	Output	O	3.6v	Vcc5	E10, E11	I	3.6v	
VBAT	Output	O	3.6v	Vcc6	A7	I	3.6v	
VBAT	Output	O	3.6v	Vbats	D8	I	3.6v	

Main Battery				TX module RFMD RF3178G				
SIGNAL	Pin	I/O	POWER	SIGNAL	Pin	I/O	POWER	COMMENTS
VBAT	Output	O	3.6v	VBAT	5	I	3.6v	

Backup Battery				TRITON LITE				
SIGNAL	Pin	I/O	POWER	SIGNAL	BALL	I/O	POWER	COMMENTS
VBAT	Output	O	3.6v	VBACKUP	H8	I	3.6v	

Table 22 : Battery connections

4.4.2 TRITON LITE Description

Triton Lite is specifically designed to power the modem processor and its memories, peripherals, SIM and MMC cards, USB connectors and other devices. 2 step-down converters and 7 LDOs are available for that purpose; 3 other LDOs dedicated to internal functions should NOT be used for external purposes.

Inputs						
Power plan	**Power rail name**	**Operating condition**	**Nominal voltage**	**Tolerance (min - max)**	**Max sink (mA)**	**N**
Main supply	VBAT		3.6	2.5 – 5.5		
Backup supply	VBACKUP		3.6	2.5 – 5.5		
Ground plan	**Power rail name**	**Definition**	**Pins list**			
DCDC converters	GNDDBB	VRDBB ground	F8, F9, G9			
DCDC converters	GNDVBUS	VRVBUS ground	B7, C7			
MMC, MEM, PLL, vibrator	GNDPWR1	Power ground	K7			
LED	GNDPWR2	Power ground	B11			
Digital sections	GNDPWR3	Power ground	L6			
SIM, ABB, voice/audio	GNDPWR4	Power ground	B3			
EXT, IO, ADC, Charger	GNDPWR5	Power ground	D11			
System	REFGND	Analog ground	J12			

Output type	Output name	Dynamic range (V)	Tolerance (%)	Max drive (mA)	Typ tON time (us)	N
DCDC	VRDBB	0.95 – 1.4, 30mV step	+/- 5	850	300	1
DCDC	VRVBUS	5.0	+/- 5	60	100 ms max	2
LDO	VRUSB	3.3	+/- 5	15	100	3
LDO	VRABB	2.8	+/- 5	80	100	5
LDO	VRRTC	1.8	+/- 5	20	100	3
LDO	VRPLL	1.05/1.3	+/- 5	10/10	500	3
LDO	VRMEM	1.8	+/- 5	200	100	4
LDO	VRIO	1.8	+/- 5	200	100	5
LDO	VRSIM	1.8/2.85	+/- 5	15/15	100	3
LDO	VREXTH	1.8/2.8	+/- 5	200/100	100	4
LDO	VREXTL	1.05 – 1.3	+/- 5	200	100	5

LDO	VRMMC	1.8/2.85	+/- 5	100/100	100	3

Table 23 : Triton Lite Power description

1. Step-down operation at 1.0 MHz requires a LC filter on the output, L = 2.2 uH (125 mOhms at DC), C = 10 uF (ESR 50 mOhms at 1.0 MHz).
2. Step-down operation at 1.0 MHz requires a LC filter on the output, L = 4.7 uH (125 mOhms at DC), C = 15 uF (ESR 50 mOhms at 1.0 MHz).
3. Decoupling capacitor on output C = 1 uF (ESR 100 mOhms at 100 kHz).
4. Decoupling capacitor on output C = 10 uF (ESR 100 mOhms at 100 kHz).
5. Decoupling capacitor on output C = 4.7 uF (ESR 100 mOhms at 100 kHz).

For more information on the power supplies, please refer to Triton's documents.

4.4.3 TRITON LITE Interconnect

Triton Lite					**Locosto**				**N**
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
VRMMC	M7	O	2.8	→	APC_VD0	U13	I	2.8v	
VRMMC	M7	O	2.8	→	VDDR1RX1	T15	I	2.8v	
VRMMC	M7	O	2.8	→	VDDR1TX1	F16	I	2.8v	
VRIO	E12	O	1.8	→	VDD_IO	C9, U7, U3, A3	I	1.8	
VRSIM	A1	O	1.8	→	VDD_USIM	T12	I	1.8	
VRMEM	M8	O	1.8	→	VDD_MIF	E1, K1	I	1.8	
VREXTH	F12	O	2.8v	→	VDDR2	F15	I	2.8v	
VREXTL	D12	O	1.3v	→	Vdd_DBB	B15, A13, A11, A8, U6, B4, N1	I	1.3v	
VREXTL	D12	O	1.3v	→	Vpp	B17, A17	I	1.3v	
VREXTL	D12	O	1.3v	→	Vdd_RST	U10, R10	I	1.3v	
VRPLL	M9	O	1.3v	→	VDD_PLL	C13	I	1.35v	

Triton Lite					**BT : BRF6150**				**N**
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
VRIO	E12	I	1.8	→	VDD_IO_SF	H8, B3	I	1.8v	
VRIO	E12	I	1.8	→	VDD_IO	G7, A3, D8	I	1.8v	

Triton Lite					**AGPS : GPS 5002**				**N**
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
VRIO	E12	O	1.8	→	VDDIO	B6, C2, C7, G4, G6	I	1.8v	
VRIO	E12	O	1.8	→	VDDA	G2	I	1.8v	
VREXTL	D12	O	1.3	→	VDDCORE	B3, B5, D7, F2, G3, G5	I	1.3v	
VREXTL	D12	O	1.3	→	VDD	B7, E7	I	1.3v	

Triton Lite					**Main LCD : Philips LPH8754-2 + Hitachi driver HD66774**				**N**
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
VRIO	E12	I	1.8	→	Vcc1	72, 73	I	1.8	
VRIO	E12	I	1.8	→	Vcc2	76, 77	I	1.8	

Triton Lite					**FM : Rohm BH1403AGLU**				**N**
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
VRIO	E12	I	1.8	→	Vccif	8	I	1.8	

Triton Lite					**IRDA : Agilent FIR 3220**				**N**
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Pin**	**I/O**	**Power**	
VRIO	E12	I	1.8	→	IOVcc	7	I	1.8	

Table 24 : Triton Lite Power interconnect

Layout considerations :

_ The power traces from Triton Lite to Locosto must be large enough to supply the max current required by Locosto. Avoid thin traces on supply lines. Choose short and wide traces whenever possible.

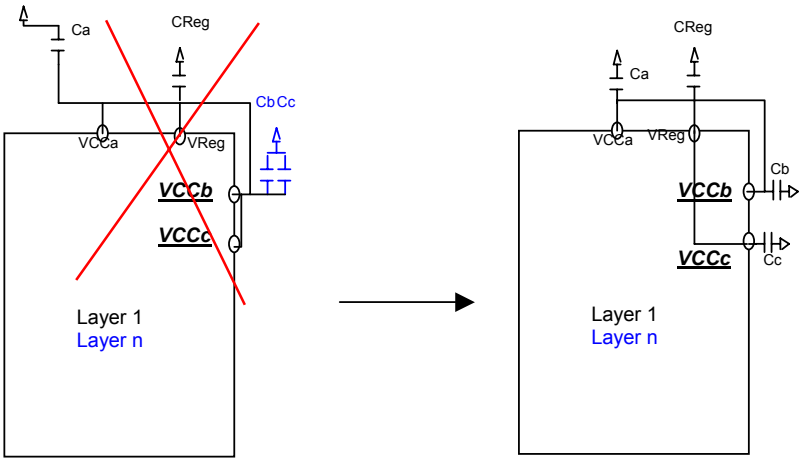
_ All digital, CLK, RF lines must be far from power traces to avoid any noise coupling effect.

_ Put via to GND very close to the GND pad of the decoupling capacitor (in the pad if possible).

_ The supply trace coming from Triton Lite must go first to the decoupling capacitor and then to the relevant Locosto VCC ball.

_ The decoupling capacitors must be placed as near as possible of the Triton Lite and Locosto power balls

_ Ideally, place the decoupling capacitor in the same layer as the chip, so as to avoid any additional parasitic inductor due to vias.



4.4.4 TPS79328YEQR Description

The TPS79328YEQR module is a low drop out 2.8V regulator 200mA.
The Input VBAT can be 3.0V min up to 5.5V max. Its standby current is less than 1uA. It is provided in YEQ package.

4.4.5 TPS79328YEQR Interconnect

TPS79328				Triton Lite				
SIGNAL	Ball	I/O	POWER	SIGNAL	BALL	I/O	POWER	COMMENTS
EN	A3	I	VBAT	REGEN	C11	O	VBAT	

TPS79328				Parallel Camera : Agilent ADCM2700			
SIGNAL	BALL	I/O	POWER	SIGNAL	Pin	I/O	POWER
OUT	C1	O	2.8v	vdd	17	I	2.8v / 42mA

TPS79328	Secondary LCD : TFS 128*128	

SIGNAL	BALL	I/O	POWER	SIGNAL	Pin	I/O	POWER	COMMENTS
OUT	C1	O	2.8v	VDD	9	I	2.8V	0.5 mA

TPS79328				Secondary LCD : Sitronix driver ST7541				
SIGNAL	BALL	I/O	POWER	SIGNAL	Pin	I/O	POWER	COMMENTS
OUT	C1	O	2.8v	VDD1, VDD2	231, 262 to 283, 313, 335, 339, 344	I	2.8V	1 mA

TPS79328				IRDA : Agilent FIR 3220				
SIGNAL	BALL	I/O	POWER	SIGNAL	Pin	I/O	POWER	COMMENTS
OUT	C1	O	2.8v	VCC	6	I	2.8V	3 mA

TPS79328				FM : Rohm BH1403AGLU				
SIGNAL	BALL	I/O	POWER	SIGNAL	BALL	I/O	POWER	COMMENTS
OUT	C1	O	2.8v	Vcca, Vccd	A7, A2, D2	I	2.8V	15.5 mA

TPS79328				Main LCD : Philips LPH8754-2 + Hitachi ctlr HD66774			
SIGNAL	BALL	I/O	POWER	SIGNAL	Pin	I/O	POWER
OUT	C1	O	2.8v	VAA, VCC, VCI	5,6,14,15,16,18,19,20	I	2.8V

Table 25 : 2.8V external LDO interconnect

5 Global Clock distribution implementation

5.1 System clock Block diagram

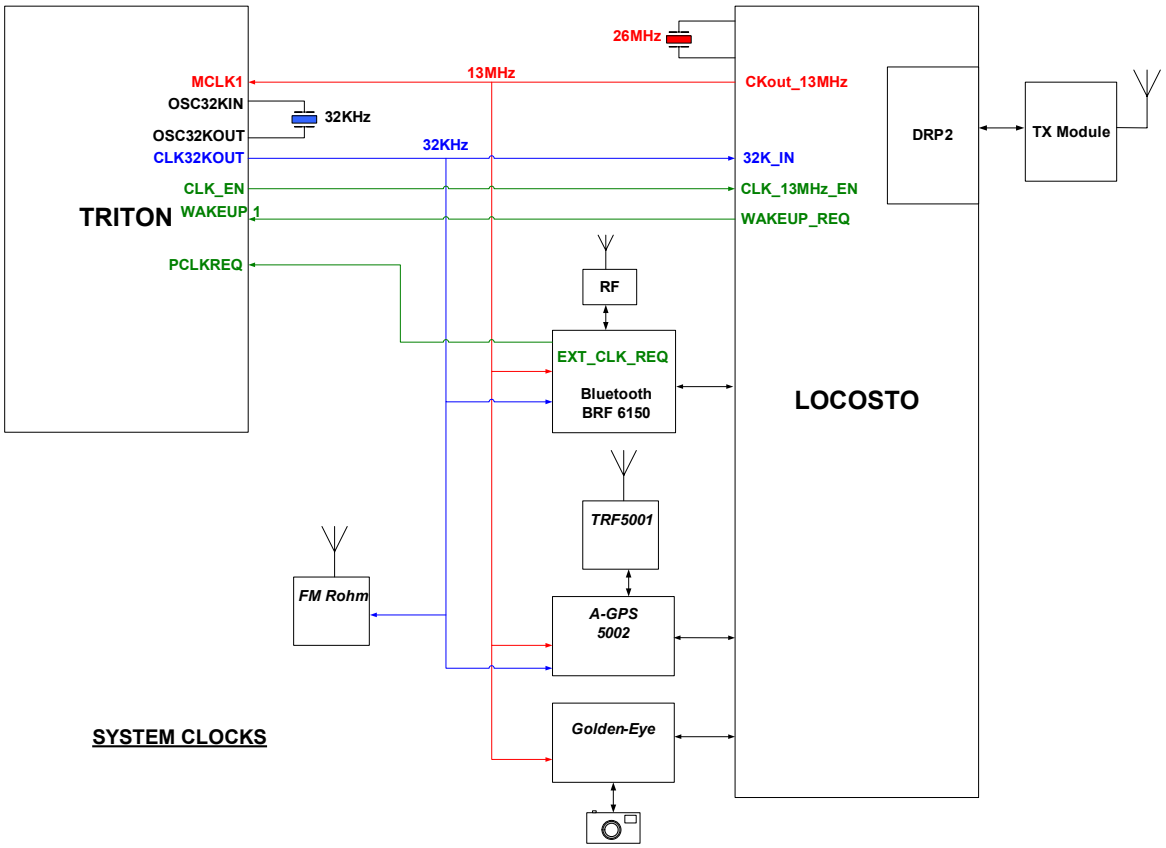


Figure 18 : System Clock block diagram

5.2 Description

The system clocking is divided in two main domains:

- 13Mhz Fast clock.
- 32.768Khz slow clock

5.3 Fast clock management

The 13Mhz reference clock is generated by a 26MHz crystal connected to LOCOSTO. Then the 26MHz is divided by two into LOCOSTO to provide a square 13MHz to the system.

The external 26Mhz crystal has a frequency stability of +/- 3ppm.

The enable signal CLK_EN is a digital signal provided by the Power IC (Triton Lite) to requests the Fast Clock to Locosto (CLK_13MHz_EN). Then Locosto will provide the 13MHz (CKout_13MHz) to the system : to Triton Lite (MCLK1), BT, AGPS and to the camera co-processor DM290.

The BT (BRF6150) device can also request (EXT_CLK_REQ) the fast clock to Triton Lite (PCLKREQ) that will request the fast clock to Locosto.

LOCOSTO can assert the wakeup_req signal to Triton Lite (wakeup1 pin) to request the fast clock and its associated powers (ACTIVE state) or to switch off the fast clock and its associated powers (SLEEP state).

5.3.1 Fast System clock interconnections

LOCOSTO					GPS5002				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
CKout_13MHz	N8 (Mode 0)	O	VDDIO	→	REF_CLK	G1	I	VRIO	

LOCOSTO					BRF6150				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
CKout_13MHz	N8 (Mode 0)	O	VDDIO	→	XTALP / FAST_CLK_IN	E2	I	VRIO	

LOCOSTO					TRITON LITE				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
CKout_13MHz	N8 (Mode 0)	O	VDDIO	→	MCLK1	J8	I	VRIO	

LOCOSTO					DM290				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
CKout_13MHz	N8 (Mode 0)	O	VDDIO	→	Source_CLK	TBD	I	VRIO	

TRITON LITE					BRF6150				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
PCLKREQ	M12	I	VDDIO	←	EXT_CLK_REQ_OUT	D7	O	VRIO	

LOCOSTO					TRITON LITE				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
CLK_13MHz_EN	T7 (Mode 0)	I	VDDIO	←	CLK_EN	D10	O	VRIO	

LOCOSTO					TRITON LITE				
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	**COMMENTS**
WAKEUP_REQ	R8 (mode 0)	O	VDDIO	→	WAKEUP 1	K9	I	VRIO	

Table 26 : Fast system Clock interconnect

5.4 Slow clock (RTC) management

32Khz slow clock is generated in TRITON LITE module from a dedicated crystal (+/-20 ppm frequency stability). This function is working immediately after the backup battery plug-in, available to the full system as soon as Triton Lite LDO VRIO output is stabilized to 1.8V; the 32KHz is alive in system in sleep mode. It is used in a RTC module giving time and calendar information directly accessible from the (I2C) control port interface. TRITON LITE module drives out this clock to LOCOSTO, BT (BRF6150) and AGPS (TWL5002).
TRITON LITE broadcasts it to LOCOSTO, BRF6150 AND TWL5002 modules only after VIO is power on and stabilized.

TRITON LITE					LOCOSTO					
Signal	**Ball**	**I/O**	**Power**	**DIR**	**Signal**	**Mode**	**Ball**	**I/O**	**Power**	**COMMENTS**
CLK32KOUT	K11	O	VRIO	→	32K_IN	0	T8	I	VDD_IO	

TRITON LITE					GPS5002					
Signal	**Pin**	**I/O**	**Power**	**DIR**	**Signal**	**MODE**	**Ball**	**I/O**	**Power**	**COMMENTS**
CLK32KOUT	K11	O	VRIO	→	RTC_CLK	--	A3	I	VRIO	

TRITON LITE					BLUETOOTH					
Signal	Ball	I/O	Power	DIR	Signal	MODE	Ball	I/O	Power	COMMENTS
CLK32KOUT	K11	O	VRIO	➔	SLOW_CLK_IN	--	F6	I	VDD_IN_BB *	Fail-safe input

TRITON LITE					FM Rohm BH1403AGLU					
Signal	Ball	I/O	Power	DIR	Signal	MODE	Pin	I/O	Power	COMMENTS
CLK32KOUT	K11	O	VRIO	➔	32KHz	--	38	I	VRIO	

Table 27 : Slow System CLOCK connection

VDD_IN_BB is powered by an internal LDO directly connected to VBAT

-

-

6 debug Capability

6.1 JTAG

LoCosto Test Access Port controller interfaces the standard IEEE JTAG serial protocol.

The chip integrates 5 x TAP/JTAG controllers to control respectively the LoCosto chip and the DRP2.0 Sub-Chip test hardware configurations, the Fuse-Farm controller, the ARM7TDMI MCU and the C54x DSP emulation's.

The JTAG Test Access Port (TAP) of the chip depending on "nBSCAN" pin value can be selected:

- To access the 2 processors on-chip emulators with a pseudo IEEE JTAG protocol for emulation purposes. A PC or workstation can be connected to the interface to set the bi-emulation mode with the ARM core linked to DSP core. The IceCrusher module supports the synchronization between the 2 cores.

- To dialog with embedded TAP/JTAG controller's, which instructions set is compliant with the IEEE 1149 standard for controlling Boundary Scan modes, Fuse-Farm activation, DRP's specific test configuration & the programming of the chip I/Os configuration (PMT modes, full-scan modes, memory-BIST modes…).

6.2 Nemu 0 & 1

Emulation mode. Refer to "LoCosto – Integrated Circuit System On Chip Specification" for more informations.

6.3 NBSCAN

Chip's test engineering as well as I/O 's Boundary Scan (PCB's test) is set by pulling "nBSCAN" pin to a low level. When the "nBSCAN" pin is high (on-chip pull-up) functional mode with emulation capability is set; emulation effective entry is defined from the "EMU" protected control bit.

7 Global Reset implementation

7.1 Block diagram

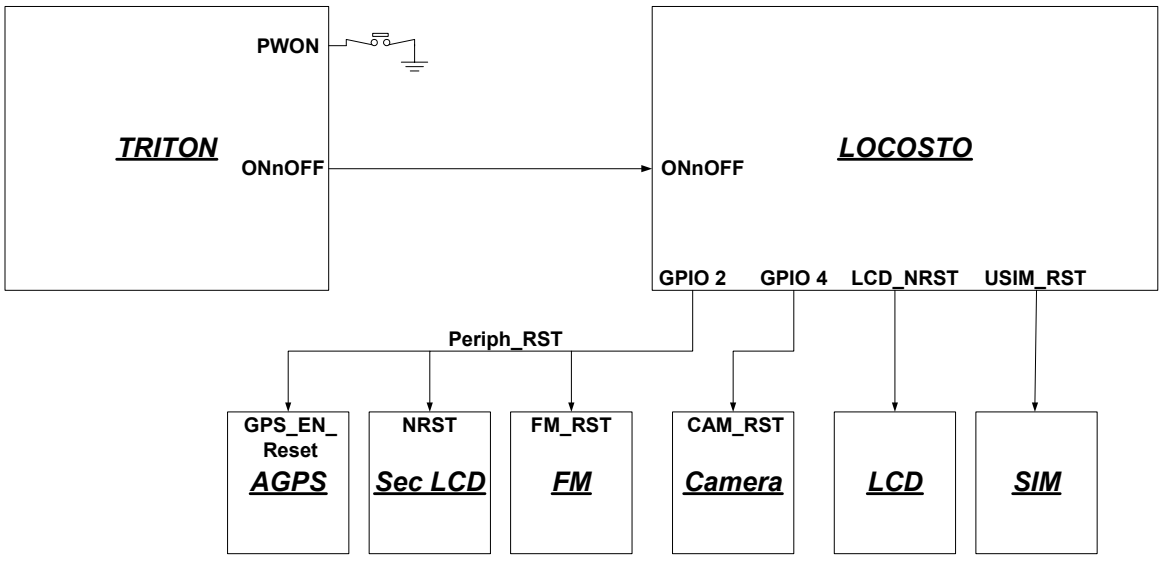


Figure 19 : Global Reset diagram

7.2 Interconnect

The main switch-on button (PWON) of the system starts Triton Lite power-up sequence (state machine). After completion of the TRITON LITE LDOs output ramp-ups LOCOSTO is started by TRITON LITE by the
ONnOFF signal. LOCOSTO starts in reset mode 0. LOCOSTO also drives the secondary LCD, A-GPS and FM reset through GPIO 2 used as periph_reset signal. LOCOSTO GPIO 4 is dedicated to Camera Reset and LOCOSTO is providing dedicated signals for LCD reset and SIM reset.

Triton Lite									N
Signal	Ball	I/O	Power		Signal	Ball	I/O	Power	
PWON	L10	I	PULL_DOWN	←	External button	n/a			1

1. Triton Lite can also be switched on from a remote device via RPWRON.

LOCOSTO					TRITON LITE				N
Signal	Ball	I/O	Power		Signal	Ball	I/O	Power	
ONnOFF	N10 (Mode 0)	I	VDD_RST	←	ONnOFF	M11	O	VRIO	

LOCOSTO						AGPS					N
Signal	Ball	Mode	I/O	Power		Signal	Mode	I/O	Power		
GPIO_2	T3	0	O	VDD_IO	→	GPS_EN_RESET	D2		I	VRIO	2, (PD @ Reset)

2. LOCOSTO GPIO_2 is dedicated to system peripherals reset.

LOCOSTO						Sec LCD				N
Signal	Ball	Mode	I/O	Power		Signal	pin	I/O	Power	
GPIO_2	T3	0	O	VDD_IO	→	NRST	3	I	VRIO	2

LOCOSTO						FM				N
Signal	Ball	Mode	I/O	Power		Signal	Pin	I/O	Power	
GPIO_2	T3	0	O	VDD_IO	→	FM_RST	15	I	VRIO	2

LOCOSTO						CAMERA				N
Signal	Ball	MODE	I/O	Power	Signal	Signal	pin	I/O	Power	
GPIO 4	R9	0	O	VDD_IO	→	CAM_RST	NA			

LOCOSTO						LCD				N
Signal	Ball	Mode	I/O	Power		Signal	Pin	I/O	Power	
LCD_NRST	C10	0	O	VDD_IO	→	RESET	58	I	VRIO	

LOCOSTO						SIM				N
Signal	Ball	Mode	I/O	Power		Signal	Pin	I/O	Power	
USIM_RST	N11	0	0	VDD_USIM	→	RESET	2	I	VRSIM	

Table 28 : Reset connections

8 System description

8.1 TRITON LITE Power up sequence

At battery plug-in, TRITON LITE starts its power on sequence and generates the 32Khz clock. It is master in this sequence. It directly drives Locosto power supply and enables the external LDO(s) with REG_EN signal.

We can divide this sequence in five main steps:

- **NO SUPPLY:** none battery is present.
- **BACKUP:** Only backup battery is present.
  Initially in manufacturing the backup battery plug-in generates a reset signal to the power control state machine and enables the 32-kHz oscillator.
- **OFF:** Main battery is present, backup battery present or not.
  All power supplies are in off state except VRTC.
  After power on reset sequence the power control state machine maintains a reset condition for the other blocks of Triton Lite and for external use. During this state control state machine is able to detect and process a switch on condition from an external event, ONNOFF signal is maintained low and will be released to high once switch-on sequence is complete.
- **ACTIVE:** Main battery is present, backup battery present or not.
  Power supplies are on.
- **SLEEP:** Main battery is present, backup battery present or not.
  Power supplies are in low power mode.

Transition of operating states:

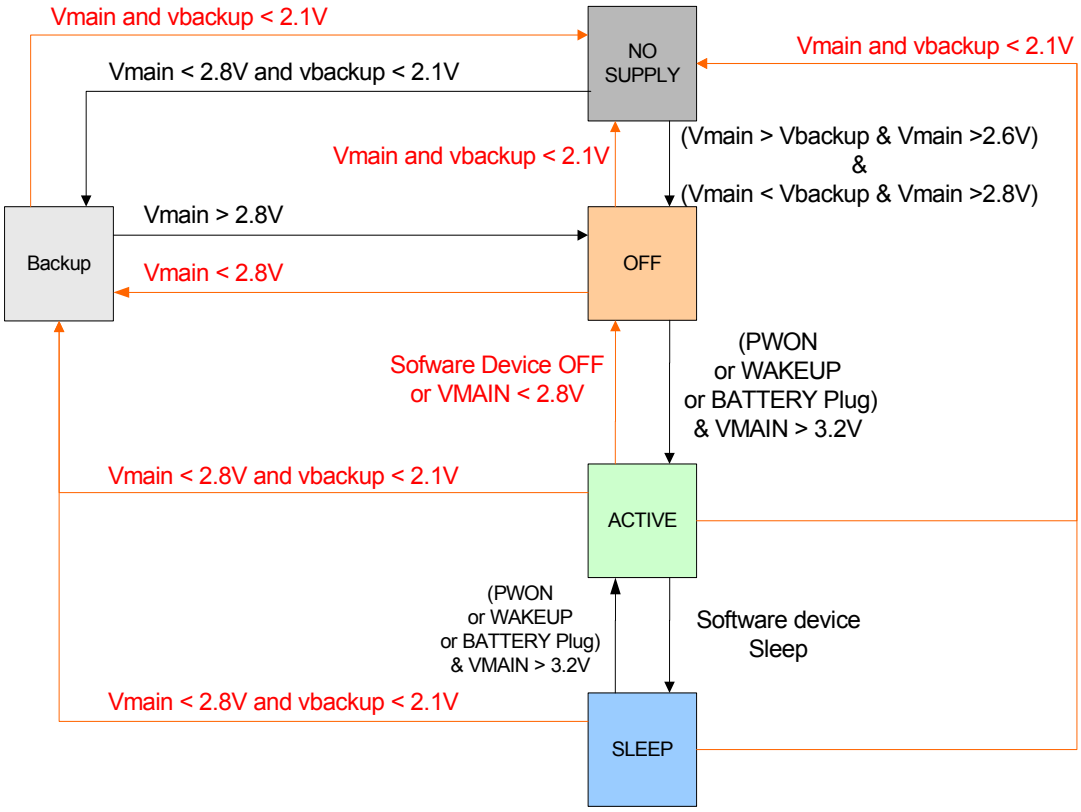


Figure 20 : Triton Lite operating states

Transitions	Conditions
No Supply to Off	Vmain > Vbackup and Vmain > 2.6V & Vmain < Vbackup and Vmain > 2.8V
Backup to No Supply	Vmain and Vbackup < 2.1V
Backup to Off	Vmain > 2.8V
Off to No Supply	Vmain and Vbackup < 2.1V
Off to Backup	Vmain < 2.8V
Off to Active	Pwon or Rpwon1 or RpWon1 or Wakeup or Battery plug. & Vmain > 3.2V
Active to No Supply	Vmain and Vbackup < 2.1V
Active to Backup	Vmain < 2.8V and Vbackup > 2.1V
Active to Off	Software Device Off or Vmain < 2.8V
Active to Sleep	Software Device Sleep
Sleep to no Supply	Vmain and Vbackup < 2.1V
Sleep to Backup	Vmain < 2.8V and Vbackup > 2.1V
Sleep to Active	Pwon or Rpwon1 or RpWon1 or Wakeup or Battery plug & Vmain > 3.2V

Table 29 : Triton Lite States transitions

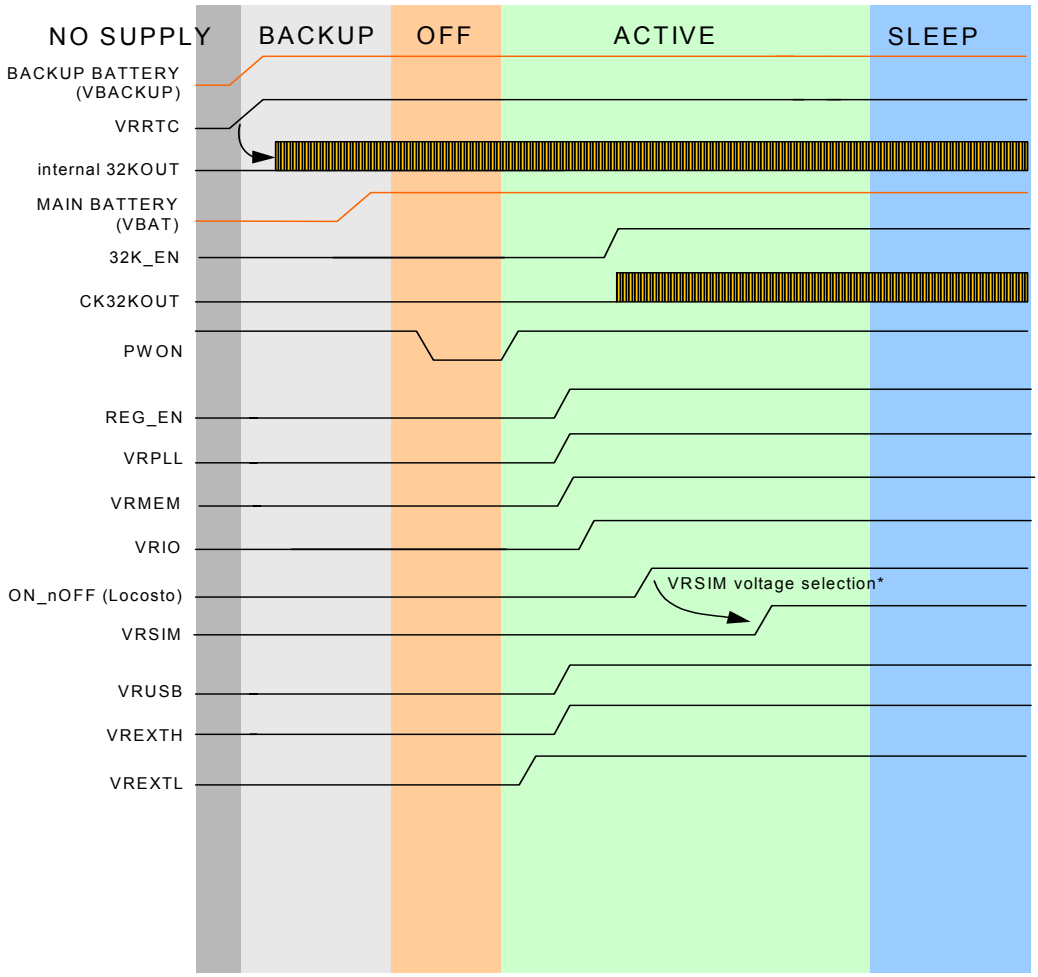


Figure 21 : Triton Lite power-up sequence

8.2 Global Boot sequence

8.2.1 BLOC DIAGRAM

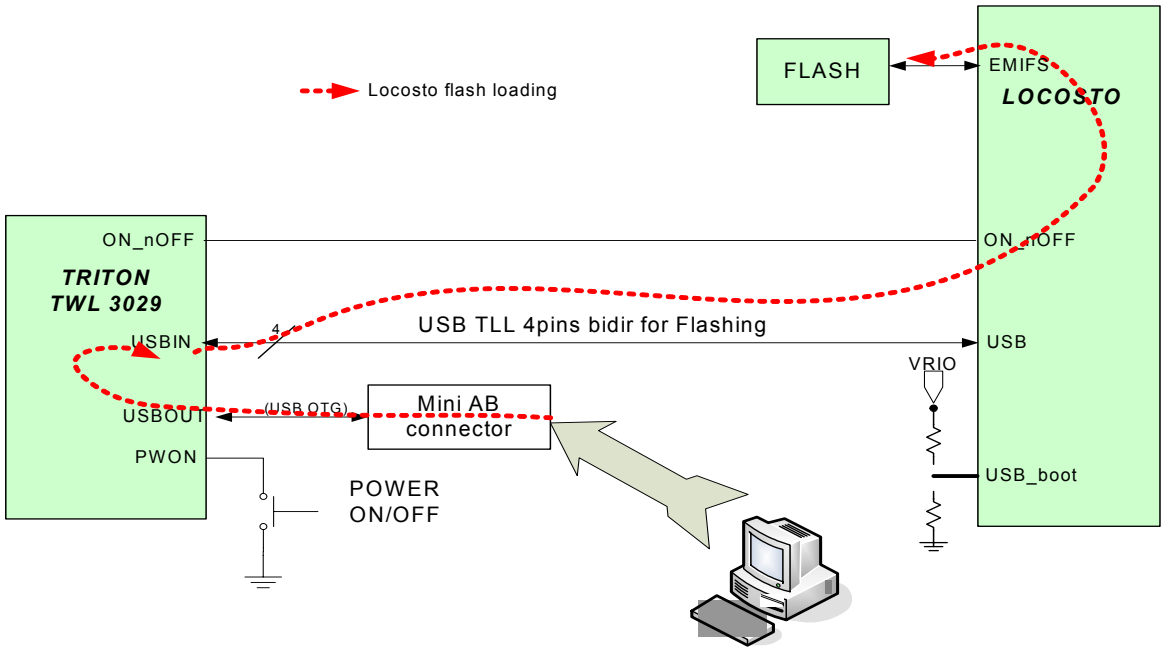


Figure 22: GLOBAL BOOT BLOC DIAGRAM

8.2.2 LOCOSTO BOOT SEQUENCE DESCRIPTION

- The main switch-on button starts Triton Lite ROM power-up sequence (state machine).
- Triton Lite simultaneously supplies peripherals.
- After completion of the ramp-ups TRITON LITE starts LOCOSTO by the asserting ON_nOFF signal.
- At the first power-on (in manufacturing environment) a basic ROM-CODE preprogrammed in Locosto allows the Flash loader code loading in the flash through the TRITON LITE USB transceiver.
- Locosto USB_boot pin, sampled at reset, selects the source interface (USB 4 pins TLL or UART) and begins the peripheral boot.
- They are also sampled at each warm reset to select firmware code location.

8.2.3 Security device

For Security Device, after having detected the flash to boot from, thanks to USB_boot signal, the ROM Code imports keys and Primary Protected Application and if present sub images to the secure ROM code.

The ROM Code MUST authenticates the sub image before execution. If the certificate authentication fails we reboot the system. Note that the certificate structure of executable image MUST be compliant with Locosto ones.
For ***Secure devices***, after each warm reset, the LOCOSTO processor MUST be able to configure the EMIF interface prior to any authentication and verification. In this case, USB TLL synchronization MUST be bypassed (Flashing bypass).

8.2.4 Peripheral Booting

In our configuration, Locosto flash contains the operational code. LOCOSTO is connected to the external world through the TRITON LITE USB transceiver for flashing.
After each power-on or on/off reset, the LOCOSTO ROM Code must download a FLASH loader and/or the configuration to be applied to the EMIF interface into LOCOSTO internal memory. The content of the flash loader is transparent for the ROM code, which is only in charge to download software at a specific address.
USB communication should always be present in order to allow FLASH configuration at each Power On Reset, and to have same ROM code.

8.2.5 Peripheral Reset

During the booting phase the Locosto GPIO 2 (Periph_reset) is Pull-Down so all the peripheral devices have their reset enabled. Then Locosto will disable Periph_reset and the peripheral devices will start running.

8.3 Global GPIO & TSPACTs management

Locosto GPIOs / TSPACTs						**Comments**
Signal	**Ball**	**Mode**	**I/O**	**Power**	**PU/PD at Reset**	
TSPACT 8	N9	1	O	VDD_IO	PD	Triton START ADC
TSPACT 10	B11	2	O	VDD_IO	PD	AGPS_TIMESTAMP
TSPACT 11	F12	0	O	VDD_IO		FEM control
TSPACT 12	H10	0	O	VDD_IO		FEM control
TSPACT 13	C14	0	O	VDD_IO		FEM control
TSPACT 14	E12	0	O	VDD_IO		TX_EN
TSPACT 15	G10	0	O	VDD_IO		Band_Select
GPIO 1	K8	0	IO	VDD_IO	PD	1_WIRE signal (PWT in option, function realized with Triton).
GPIO 17	B9	0	IO	VDD_IO	PU	1_ When DM290 : INT_GtoL 2_ When Camera : CAM_PWDN
GPIO 4	R9	0	IO	VDD_IO	PU	1_ When DM290 : INT_LtoG 2_ When Camera : CAM_RST
GPIO 10	C11	1	IO	VDD_IO	PU	AGPS_SLEEPX_N
GPIO 11	D10	1	IO	VDD_IO	PU	DM290 Sleep
GPIO 2	T3	0	IO	VDD_IO	PD	System periph reset (AGPS Reset, FM reset, DM290 reset when present)
GPIO 35	F5	0	IO	VDD_IO	PU	Extra LED for Torch/Flash
GPIO 36	D2	0	IO	VDD_IO	PU	IRDA SD
GPIO 37	H7	0	IO	VDD_IO	PD	BT shutdown

Table 30 : GPIOS and TSPACTs description

9 System mode

9.1 Mode description

Each subsystem (modem and peripherals) can be in either ACTIVE, SLEEP, or OFF state. Possible power configurations depend on device chip capability once in OFF mode to present to external world output signals grounded (logic ground has to be the inactive level) and input signals disconnected. This will avoid external device current leakage into non-supplied device. This is the intended meaning of failsafe IO's.

Locosto processor does not provide failsafe interconnection at its interfaces. Thus configurations in which, one of the two is in an OFF state while the other is in ACTIVE or SLEEP state are prohibited.

9.2 Locosto MODES

9.2.1 Locosto MODES DESCRIPTION

The Layer 1 sleep manager handles three global power modes: DEEP SLEEP, BIG SLEEP and AWAKE. The Layer 1 sleep manager manages the states of the system in each mode and performs transitions between the modes.

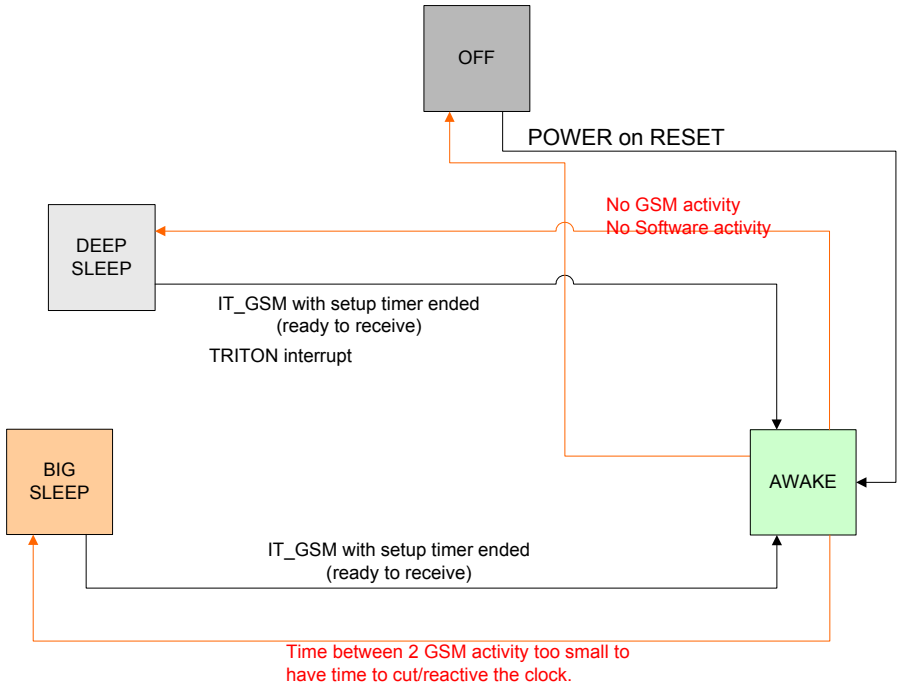


Figure 23: Locosto MODES DESCRIPTION

9.2.1.1 OFF mode

The module is not powered and waiting for power on and reset.

9.2.1.2 DEEP SLEEP mode

In DEEP SLEEP mode, only 32KHz is on in Locosto. This means that all internal clocks are inactive except the clk32k clock, which is the ULPD state machine clock.
The module can switch in low power mode.

9.2.1.3 BIG SLEEP mode

In BIG SLEEP mode, the clk32k clock is active and the system input clock (26Mhz) is active. At this time, GSM timer counter is equal to TDMA frame setup time.

9.2.1.4 AWAKE mode

In this mode, the module is active as well as any requested peripheral clocks. In this mode the clk32k clock is active. It is ready to receive TDMA frame. It can handle voice call and audio streaming from a network connection

9.2.2 LOCOSTO MODES TRANSITIONS

9.2.2.1 Transition from 'Power on' to 'AWAKE' mode

At power-up, when the power-up input signal ON_nOFF is asserted (high), the ULPD FSM enters Wake Up mode. In this case, IT_WAKEUP signal is switched to active state '1'.

9.2.2.2 Transition from DEEP SLEEP to AWAKE mode

Transition to awake mode occurs when:

- A GSM timer interrupt occurs from the ULPD.
- A wake-up request is initiated by TRITON LITE interrupt.

FSM leaves Deep Sleep mode and IT_WAKEUP is asserted high.

9.2.2.3 Transition from BIG SLEEP mode to AWAKE mode

Transition to awake mode occurs when:

- A GSM timer interrupt occurs from the ULPD.
- A wake-up request is initiated by TRITON LITE interrupt.

9.2.2.4 Transition from AWAKE mode to DEEP SLEEP mode

Transition to DEEP SLEEP state occurs when:

- No GSM activity during enough time to stop/reactive the clock

FSM enters in DEEP SLEEP mode and IT_WAKEUP goes to 0.

9.2.2.5 Transition from AWAKE mode to BIG SLEEP mode

Transition to BIG SLEEP state occurs when:

- No GSM activity during not enough time to stop/reactive the clock but several TDMA frames.

10 System application

10.1 Audio path

10.1.1 Schema block description

LOCOSTO processor is hosting the application engine that supports multimedia services, such as audio/video streaming, in a secure environment and JAVA based downloaded application. The Serial audio interface consists of a modem audio I2S codec interface, a modem voice interface, and a Bluetooth™[1] voice interface.
They are provided through following LOCOSTO peripherals: a VSP, a Cport and a MCSI.

- The voice serial port (VSP) is a bi-directional (transmit/receive) serial port that directly connects the Serial Port Interface (DSP SPI) to the voice CODEC of the ABB companion chip (Triton Lite).
- The CoDec port interface (C-port) is configured to support the Inter-IC sound (I2S) industry standard serial interface protocol.
- BT MCSI is a serial port interface to connect to Bluetooth external voice codec.

All Triton Lite (Analog Base Band IC) audio configurations are done through an I2C link.

The following diagram gives an overview of the chipset and connectivity involved in the AUDIO path.

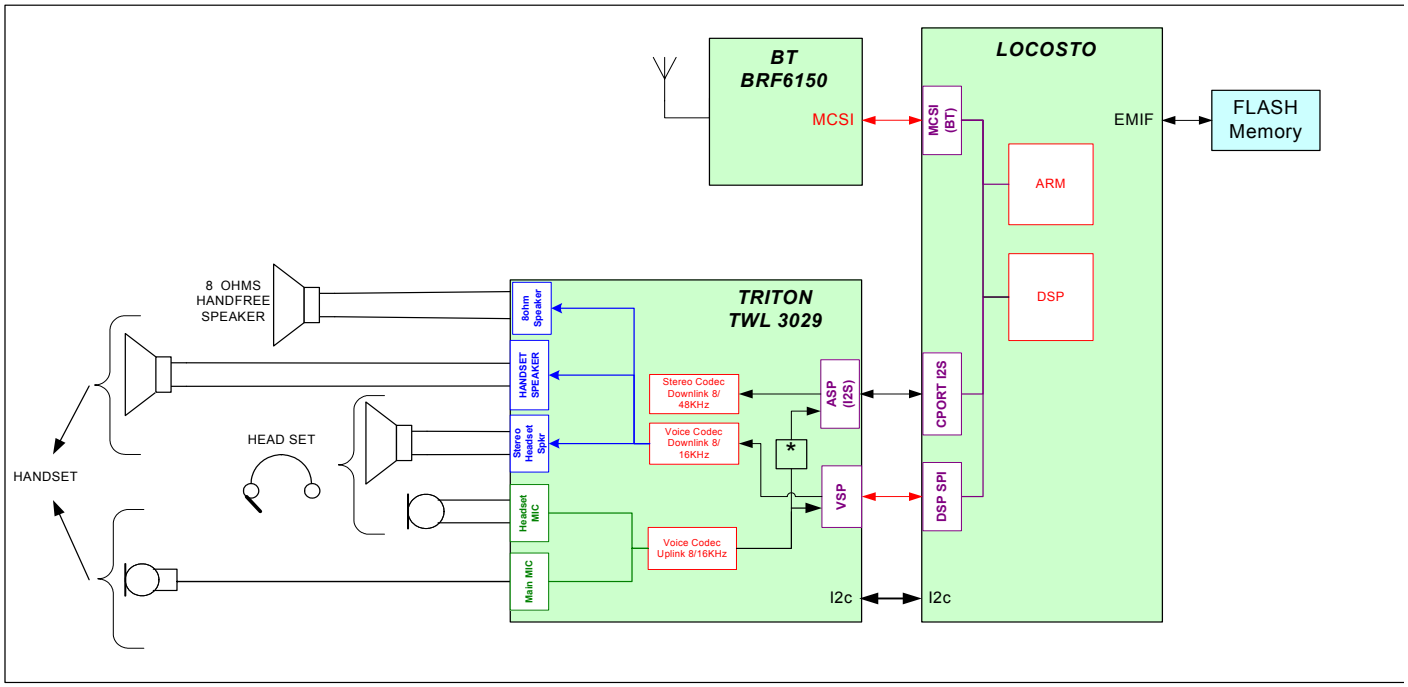


Figure 24: GLOBAL AUDIO PATH BLOC DIAGRAM

10.1.2 Audio/Voice data flow

10.1.2.1 Ring and Multimedia Streaming

This scenario applies for all multimedia codec running on the LOCOSTO. Audio data can come from different sources:

- Streaming from a network connection (dedicated channel). The data packets are buffered and sent by the RF module to LOCOSTO for decoding
- Streaming from a data storage memory such as Flash. LOCOSTO has firstly loaded the Flash from a PC or other storage source through USB or BT peripherals.
- The LOCOSTO that handles decoding, rate matching (if any), and send filtered samples to the Stereo Audio codec or BT device performs the multimedia codec.

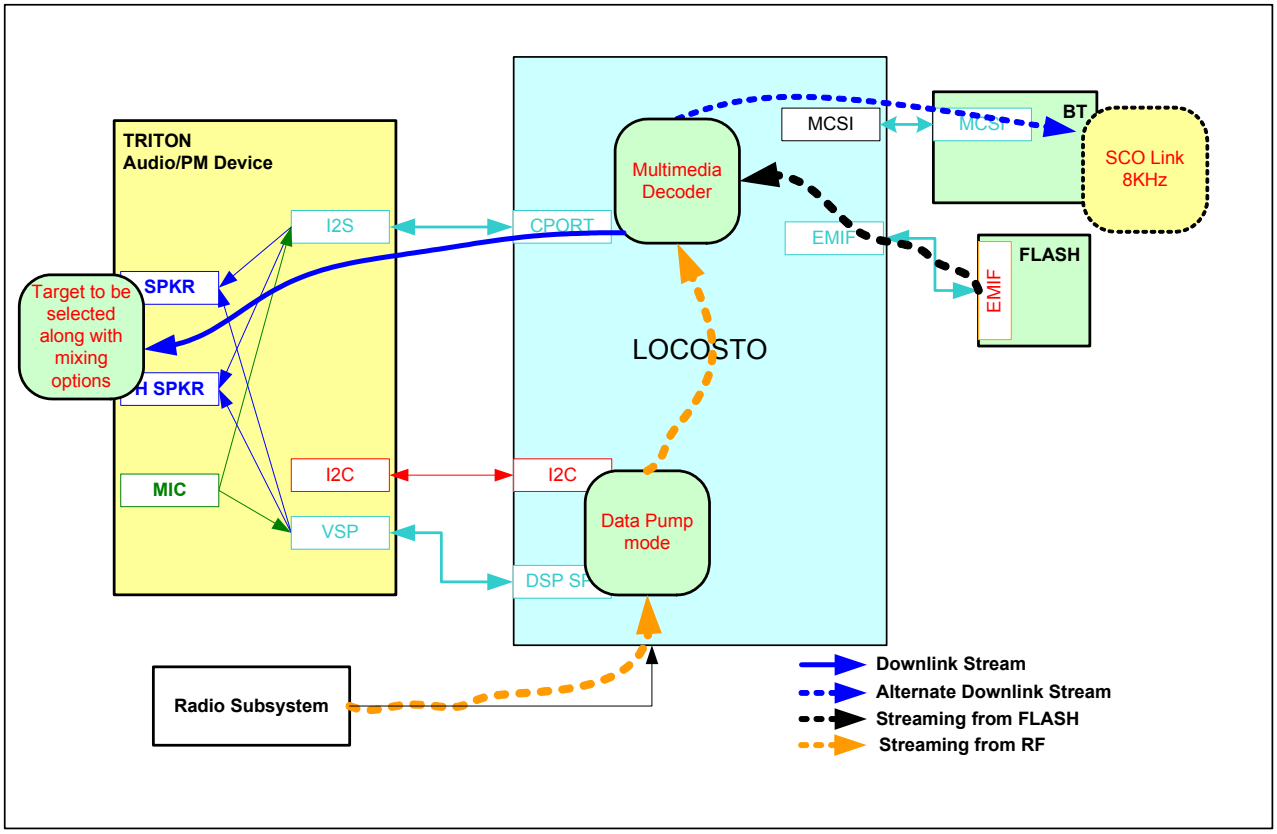


Figure 25: LOCOSTO Streaming Audio Flows

Without voice call, the LOCOSTO subsystem can be put in sleep. TRITON LITE device uses LOCOSTO 13Mhz clock to generate sampling frequency and serial port clocks.

10.1.2.2 Voice Call

This scenario applies when a dedicated voice channel is set on the modem. The LOCOSTO hosts the voice Codec as part of its modem functions and decode/encode voice uplink and downlink samples to and from the RF. LOCOSTO is needed for the Voice call application to handle BT Headset and/or Multimedia streaming over voice call as depicted below.

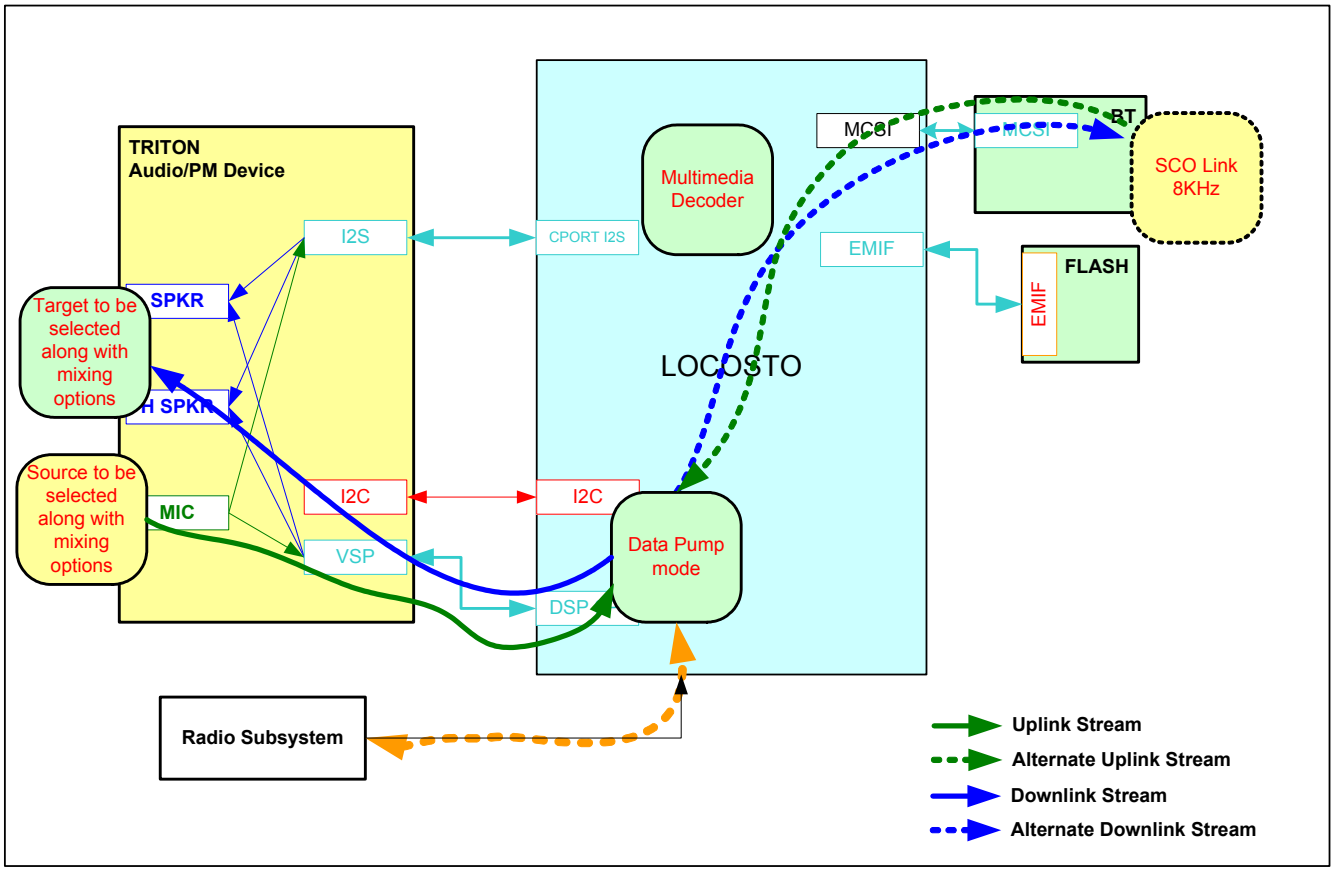


Figure 26: LOCOSTO Voice Call flows

The Voice call record application is performed in two different ways:

1. If a BT Headset is used, then the LOCOSTO is responsible to manage the PCM flows from the BT MCSI port and encode the stream while pass-through to the BT device.
2. If no BT headset is used, then the LOCOSTO sends the uplink and downlink PCM samples to TRITON LITE via the VSP interface. The LOCOSTO is then responsible to perform the encoding.

In the same manner, multimedia audio over the air depends if a BT headset is used.

1. If a BT headset is used, then the LOCOSTO sums (after decimation) the multimedia stream to the voice downlink path to the BT headset as well as the uplink path to be encoded and transmitted by the RF module.

2. If no BT headset is used, then the decimated multimedia flow is passed to the LOCOSTO that sums it to its uplink stream. The downlink is managed directly by analog mixing within the PM/Audio device.

10.1.2.3 Video Conferencing

This scenario applies for Video conferencing application. The LOCOSTO is acting as a data pump and the LOCOSTO hosts the voice codec as part of its MEPG4/AAC processing functions and decode/encode voice uplink and downlink samples to and from the RF.

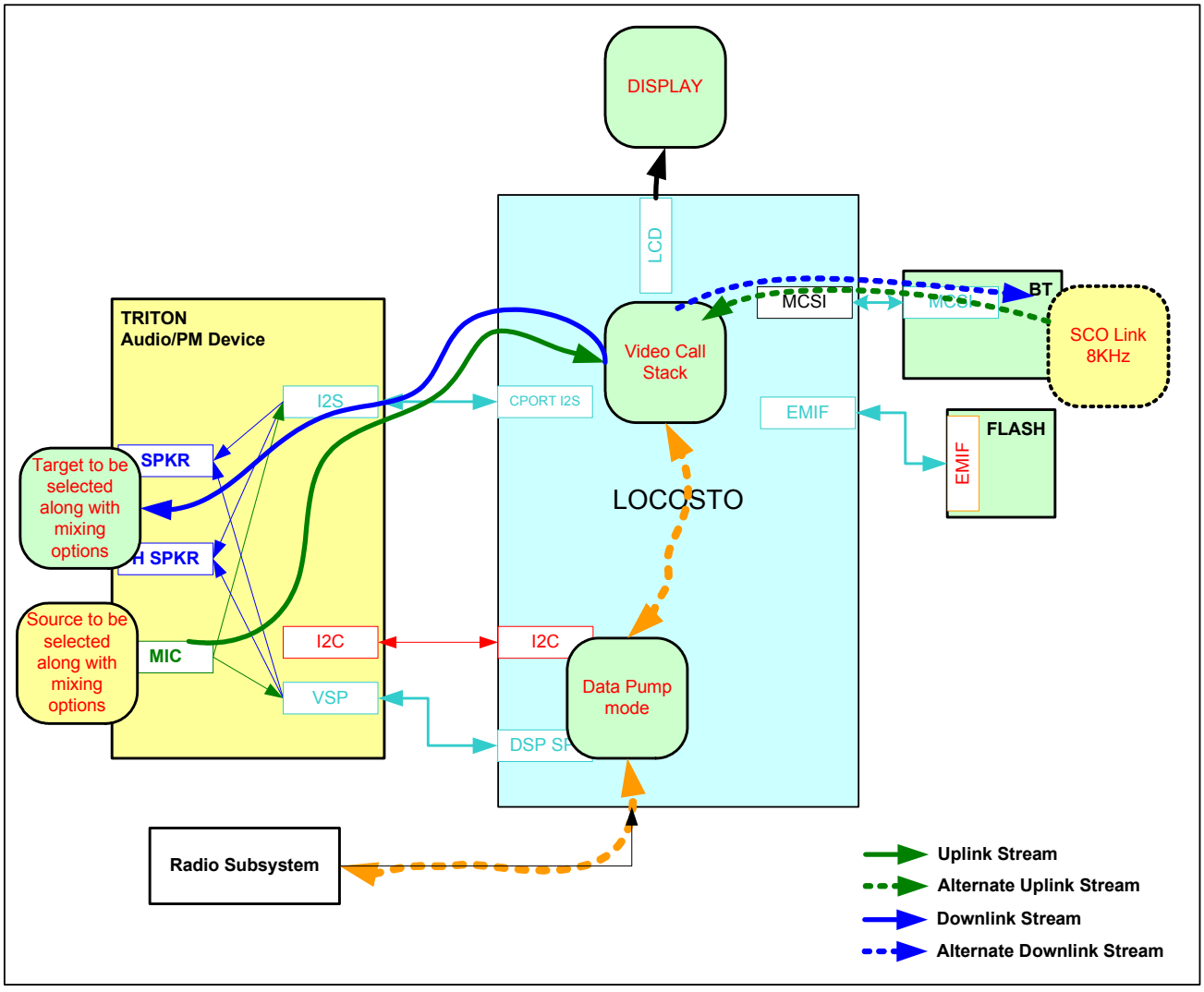


Figure 27: LOCOSTO Video Conference audio flows

10.1.2.4 Data Entry

This scenario applies for voice recognition, text-to-speech or voice memo applications where an audio uplink path to the LOCOSTO is necessary. The multimedia codec is running either on the MCU, DSP processor or accelerator. Audio data comes from a local source (microphone, headset or BT headset) and either directly processed or stored on a local memory.

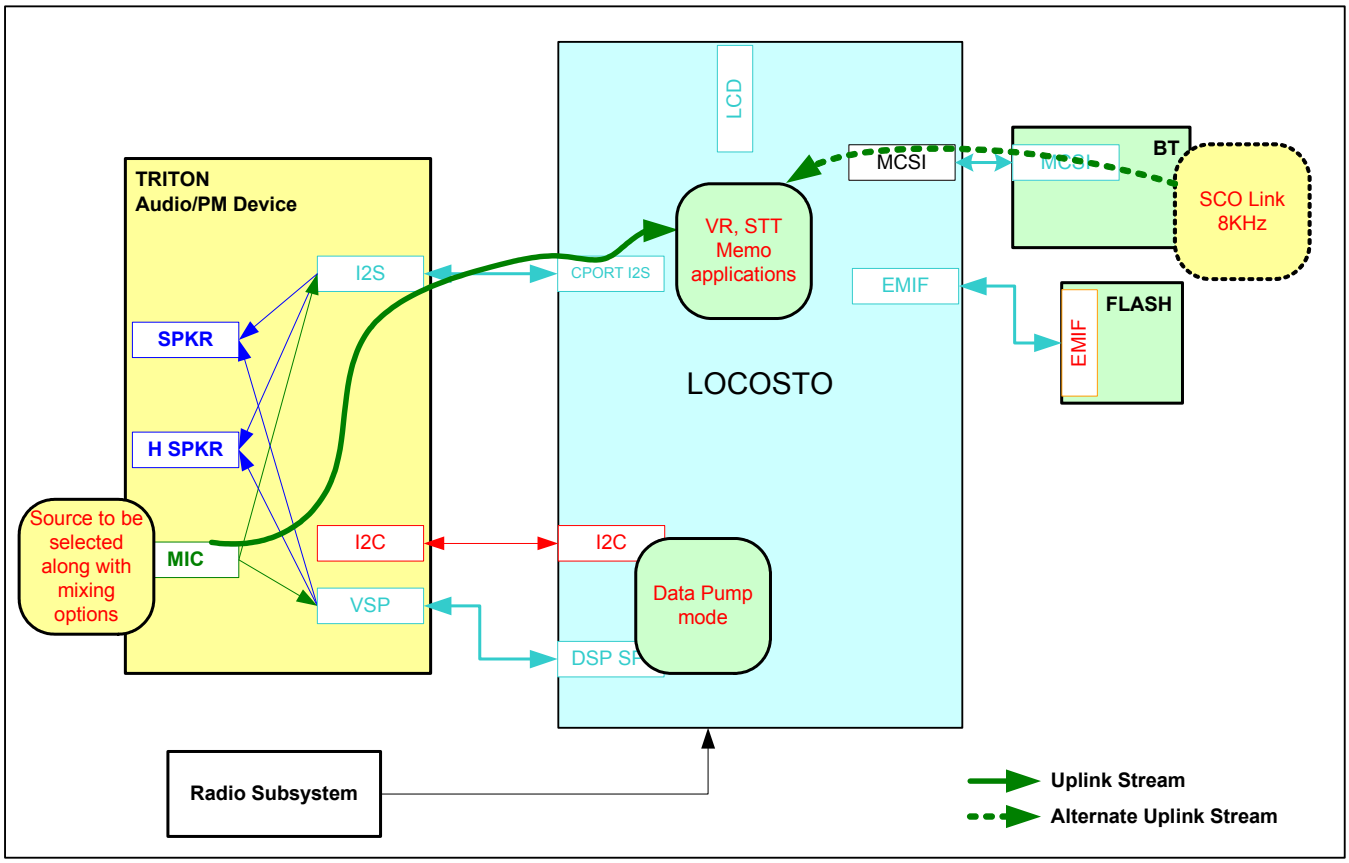


Figure 28: LOCOSTO Data entry flows

TRITON LITE device uses LOCOSTO 13Mhz clock to generate sampling frequency and serial port clocks.

10.1.2.5 BT Cordless

This scenario applies when handset is used like a home DECT phone using Bluetooth link to communicate with RTC network. LOCOSTO SW DSP can add acoustic treatment on uplink and downlink flows.

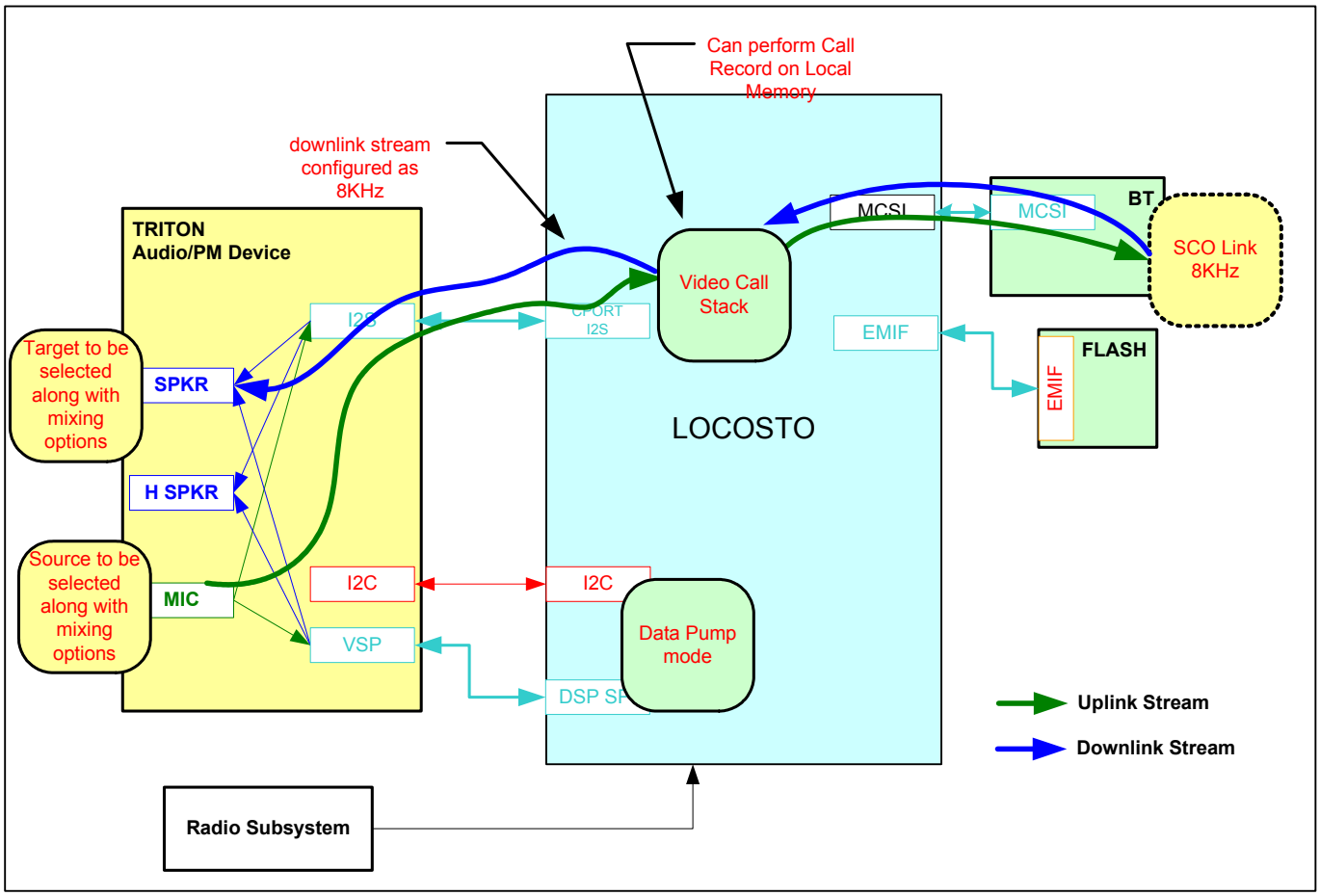


Figure 29: LOCOSTO BT Cordless flows

11 DM290

11.1 DM290 SUB-SYSTEM IMPLEMENTATION

DM290 interface short description

DM290 system is typically a CCD/CMOS camera front-end to a larger system. DM290 handles interfacing to raw CCD/CMOS data, then processes and possibly encodes this image data for subsequent display or use by the rest of the system.

DM290 module main features

- The performance target (using a SDRAM) is 5M pixels at under than 1 second processing time (SDRAM to SDRAM).
- No SDRAM processing supports up to 3M pixels capture (as we go for VGA only (300Kp) for Locosto standalone) : ***this implementation is the one chosen for Locosto system***
- It can interface CCD or CMOS sensor.
- Supports real time preview mode at CIF resolution with up to 30fps with Locosto.
- Thumbnail creation
- It enables H.263/MPEG4 video encoding up to CIF 30fps.

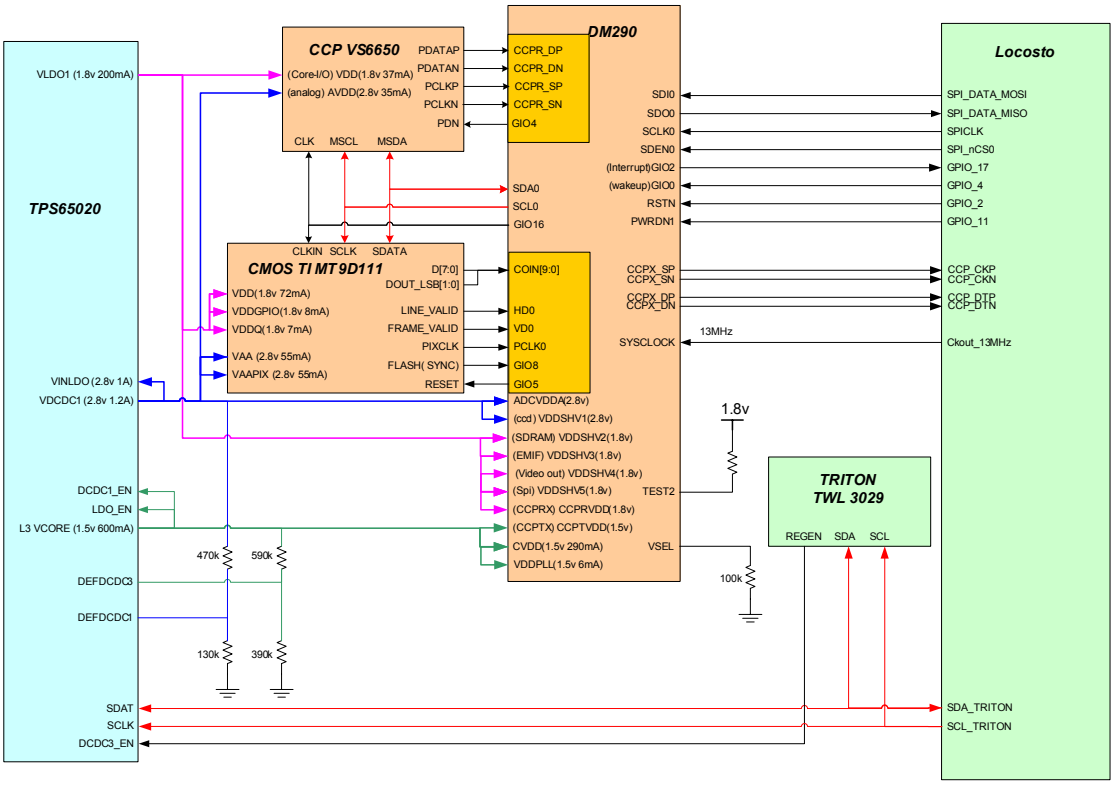


Figure 30 DM290 connection

The DM290 coprocessor data link to Locosto is performed with the 4 lines CCP interface, the SPI bus is used to configure the DM290. The DM290 proposes the Sleep feature, a reset signal and 2 GPIOs to synchronize with Locosto.

Onto the Locosto ballout the CCP pins are internally muxed with the parallel camera control signals (on the same signal mode).

11.2 LOCOSTO to DM290 connection description

LOCOSTO						DM290				
Signal name	**Ball**	**Mode**	**I/O**	**Power**	**DIR**	**Signals**	**Ball**	**I/O**	**Power**	**Comments**
SPI_DATA_MISO	F7	1	I	VDDIO	←	SDO0	C4	O	VDDSHV5	
SPI_DATA_MOSI	C5	1	O		→	SDI0	C5	I		DM290 internal pulldown
SPI_CLK	G9	1	O		→	SCLK0	D5	I		DM290 internal pulldown
SPI_nCS0	E6	1	O		→	SDEN0	B6	I		
GPIO_4	R9	0	O		→	GIO0	B7	I		DM290 wake-up with int. pull-up
GPIO_11	D10	1	O		→	PWRDN	B2	I		DM290 internal pulldown
GPIO_17	B7	0	I		←	GIO2	A7	O		DM290 interrupt with int. pull-dwn
GPIO_2	T3	0	O		→	RSTN	K2	I	VDDSHV1	
CCP_CKP	F8	1	I		←	CCPX_SP	E1	O	CCPTVDD	
CCP_CKN	E7	1	I		←	CCPX_SN	F1	O		
CCP_DTP	A5	1	I		←	CCPX_DP	C1	O		
CCP_DTN	C6	1	I		←	CCPX_DN	D1	O		
CKout_13MHz	N8	0	O		→	SYSCLK	A6	I	VDDSHV5	DM290 internal pulldown

Table 31: Locosto to DM290 connections

11.2.1 DM290 to CCP camera connection description

DM290					VS6650 CCP camera				
Signal name	**Ball**	**I/O**	**Power**	**DIR**	**Signals**	**Pin**	**I/O**	**Power**	**Comments**
CCPR_DP	J1	I	CCPRVDD	←	PDATAP	13	O	VDD	
CCPR_DN	K1	I		←	PDATAN	12	O		
CCPR_SP	L1	I		←	PCLKP	10	O		
CCPR_SN	M1	I		←	PCLKN	9	O		
SCL0	C6	O	VDDSHV5	→	MSCL	6	I		Note 1
SDA0	D6	I/O		↔	MSDA	7	I/O		
GIO16	L10	O	VDDSHV1	→	CLK	5	I		
GIO4	L7	O		→	PDN	4	I		

Table 32: DM290 to CCP camera connections

11.2.2 DM290 to CMOS sensor camera connection description

DM290					TI MT9D111				
Signal name	**Ball**	**I/O**	**Power**	**DIR**	**Signals**	**Pin**	**I/O**	**Power**	**Comments**
COIN0	P3	I	VDDSHV1	←	DOUT_LSB0	E2	O	VDDGPIO	Note 1
COIN1	L4	I		←	DOUT_LSB1	F2	O		
COIN2	M4	I		←	DOUT0	B3	O	VDDQ	
COIN3	N4	I		←	DOUT1	D3	O		
COIN4	P4	I		←	DOUT2	D2	O		
COIN5	L5	I		←	DOUT3	C2	O		
COIN6	M5	I		←	DOUT4	A2	O		
COIN7	N5	I		←	DOUT5	D1	O		
COIN8	P5	I		←	DOUT6	C1	O		

COIN9	L6	I		←	DOUT7	B1	O		
HD0	N6	I/O		←	LINE_VALID	B4	O		
VD0	P6	I/O		←	FRAME_VALID	A4	O		
PCLK0	M6	I		←	PIXCLK	C4	O		
GIO8	L8	I		←	FLASH	F1	O		
GIO16	L10	O	VDDSHV1	→	CLKIN	B8	I		
GIO5	M7	O		→	RESET	D7	I		
SCL0	C6	O		→	CLK	B5	I		
SDA0	D6	I/O	VDDSHV5	←→	SDATA	A5	I/O		
HSYNC	L13	I		←	HSYNC	18	O		
VSYNC	L12	I		←	VSYNC	17	O		
VCLK	M14	I		←	VCLK	20	O		
GIO8	L8	I	VDDSHV1	←	FLASH SYNC	22	O		
GIO16	L10	O		→	MCLK	21	I		
SCL0	C6	O	VDDSHV5	→	SCLK	19	I	VDD	Note 1
SDA0	D6	I/O		←→	SDATA	16	I/O		

Table 33: DM290 to CMOS sensor camera connections

11.3 Power management

11.3.1 DM290 Power requirements

DM290						
Power plan	**Power rail**	**PIN**	**Nominal voltage**	**tolerance (min – max)**	**Current (Max)**	**Comments**
CORE	CVDD		1.5	1.43 – 1.58	160mA	
CCP TX	CCPTVDD					
Oscillator	XVDD				6mA	
SDRAM interface I/O	VDDSHV2		1.8	1.71 – 1.89	30mA	
EMIF interface I/O	VDDSHV3					
Video interface I/O	VDDSHV4					
SPI interface I/O	VDDSHV5					
CCP RX	CCPRVDD					
Imager Analog Power	ADCVDDA		2.8	2.66 2.94	50mA	
PLL0	PLL0VDDA					
PLL1	PLL1VDDA					
CCD interface I/O	VDDSHV1					
Ground plan	**Power rail**	**Definition**		**Pins list**		**Comments**
Digital core	GND	Digital ground				

Table 34: DM290 power requirements

11.3.2 CCP camera Power requirements

VS6650						
Power plan	**Power rail**	**PIN**	**Nominal voltage**	**tolerance (min – max)**	**Current**	**Comments**
Analog power	AVDD	3	2.8v	2.4 – 2.9	37mA	
Core, I/O power	VDD	11	1.8v	1.7 – 1.9	35mA	
Power plan	**Power rail**	**PIN**	**Nominal voltage**	**tolerance (min – max)**	**Current**	**Comments**
Analog ground	AGND	2	--	--	--	
Digital ground	GND	8, 14				

Table 35: CCP camera power requirements

11.3.3 CMOS camera Power requirements

TI MT9D111						
Power plan	**Power rail**	**Ball**	**Nominal voltage**	**tolerance (min – max)**	**Current**	**Comments**
Digital power	VDD	A1, B2, G2, H1, C7, A8	1.8v	1.7 – 1.95	72mA	
Analog power	VAA	G7, H8	2.8v	2.5 – 3.1	55mA	
Pixel Array power	VAAPIX	H7,	2.8v	2.5 – 3.1	55mA	
GPIO power	VDDGPIO	H3, H6	1.8v	1.7 – 3.1	15mA	
I/O power	VDDQ	A3, A6	1.8v	1.7 – 3.1		
Power plan	**Power rail**	**Ball**	**Nominal voltage**	**tolerance (min – max)**	**Current**	**Comments**
Analog ground	AGND	E8, G8	--	--	--	
Digital ground	DGND	D4, E4, C3, F3, E1, D6, E6,F6, D5, E5, C8				

Table 36: CMOS camera power requirements

11.4 DM290 power distribution

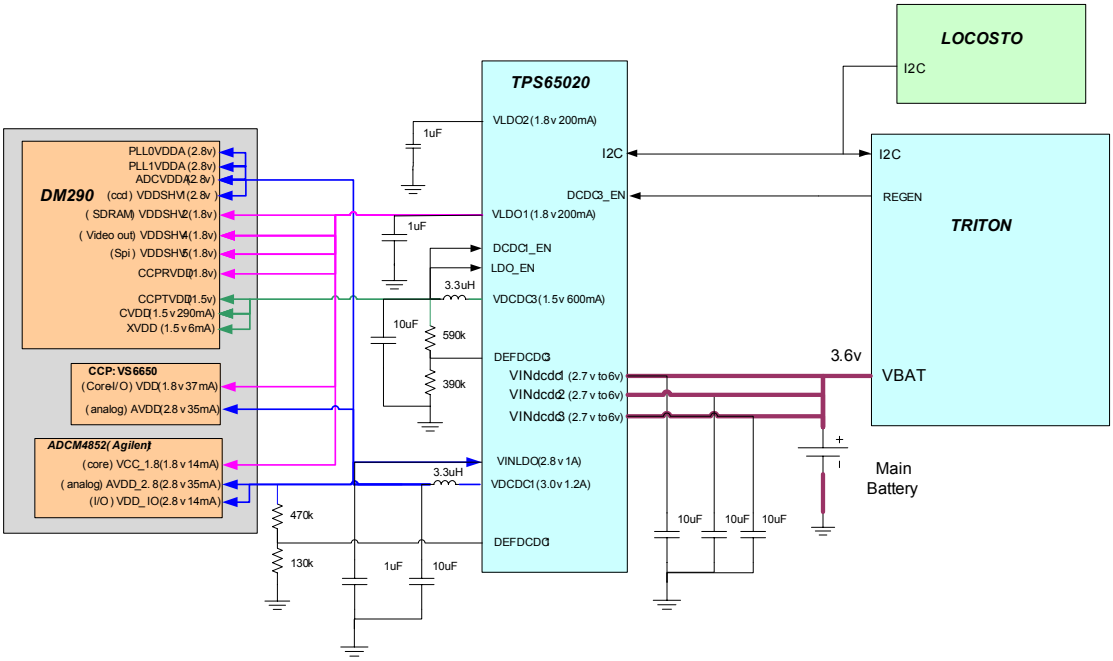


Figure 31 System Application Locosto to DM290 Power Distribution

The DCDC3_EN can be connected to Triton Lite REGEN or to a Locosto GPIO.

Power generation and distribution for the global system is divided between two power management ICs: TPS65020 provides power supplies mainly to the image processor DM290 while TRITON LITE generates the voltage sources necessary to the edge modem digital baseband Locosto. Triton Lite through DCDC3_EN controls TPS65020.

11.4.1 TPS65020 description

Output type	Output name	Dynamic range (V)	Tolerance (%)	Max drive (mA)	Typ tON time (us)	N
DCDC	VDCDC1	0.6 – VBAT	+/- 2	1200	750	1
DCDC	VDCDC2	0.6 – VBAT	+/- 2	1000	750	1
DCDC	VDCDC3	0.6 – VBAT	+/- 2	600	750	1
LDO	VLDO1	1.0 - 3.3	+/- 2	200	10	2
LDO	VLDO2	1.8	+/- 2	200	10	2
LDO	VRTC	3.0	+/- 2	20	10	2

1. Step-down operation at 1.5 MHz requires a LC filter on the output, L = 3.3 uH (125 mOhms at DC), C = 10 uF
2. Decoupling capacitor on output C = 10 uF (ESR 100 mOhms at 100 kHz).

Table 37: TPS65020 OUTPUTS

11.4.2 TPS65020 Interconnect

LOCOSTO					TPS65020				
Signal name	**Ball**	**I/O**	**Power**	**DIR**	**Signals**	**Pin**	**I/O**	**Power**	**Comments**
SDA_TRITON	R6	0	VDD_IO	←	SDAT	29	I/O	1.8v	
SCL_TRITON	N7	0		←	SCLK	30	I		
TRITON LITE					**TPS65020**				
Signal name	**Ball**	**I/O**	**Power**	**DIR**	**Signals**	**Pin**	**I/O**	**Power**	**Comments**
REGEN	C11	0	VBAT	←	DCDC3_EN	23	I	1.8v	

Table 38: TPS65020 to LOCOSTO power connections

TPS65020					DM290				N
Signal	**Pin**	**I/O**	**Power**	**DIR**	**Signal**	**Ball**	**I/O**	**Power**	
VLDO1	20	O	1.8v	→	VDDSHV2	E8, E9, E10	I	1.8v	
					VDDSHV3	D11, E11	I		
					VDDSHV4	K9, K10	I		
					VDDSHV5	E5, E6, E7	I		
VDCDC3	4	O	1.5v	→	CCPTVDD	F2	I	1.5v	
					CVDD	F6, F7, F8, F9, F10 G10, H10, J10	I		
					VDDPLL	G3, H3	I		
VDCDC1	7	O	3.0v	→	ADCVDDA	C2	I	2.8v	
					VDDSHV1	J4, K4, K5	I		

Table 39: TPS65020 to DM290 power connections

11.4.3 TPS65020 DM290 Power up sequence

- This sequence is started when the user starts using the camera. In this case the sequence starts at the 3rd step of the following description.

To properly sequence the power rails, it is important that core power comes up before the other voltage power supplies.

- At battery Plug-in TRITON LITE achieve its power on sequence. The TPS65020 wait for a power enable.
- TRITON LITE REGEN Enables the TPS65020 DCDC3.
- This DCDC3 supplies the DM290 core (1.5v) that needs to power on first. It also supplies the DCDC1 enable and the LDO enable.
- DCDC1 supplies TPS65020 LDO1, LDO2 and all DM290 subsystem high voltage (2.8v).
- LDO1 supplies all DM290 1.8v I/O ring

- LDO2 supplies the optional SDRAM

11.4.4 TPS65020 DM290 Power down sequence

This sequence is started by two possible causes
1. The user stops using the camera.
2. The user power down all the system during the camera use by inserting the power button.

It is important for core voltage to remain up until all other voltage rails on DM290 drop below the core voltage (CVDD) value. To reach this goal, we will use the TPS65020 registers to controls the power off sequence. LOCOSTO drives these control registers through the I2C bus.

1. Locosto drives low the REG_CTRL (1,2) to disable the LDOs to power down DM290 I/Os and SDRAM.
2. Locosto drives low the REG_CTRL (5) to disable the DCDC1 to power down DM290 subsystem high voltage (2.8v).
3. Locosto drives low the REG_CTRL (3) to disable the DCDC3 to power down DM290 core.
4. Locosto drives low the DCDC3 enable. The DCDC3 power down DM290 core, LDO enable and DCDC1 enable.
5. Locosto drives high the REG_CTRL (1,2,3,5) bits. Now TPS65020 is ready to perform a new DM290 power on sequence.

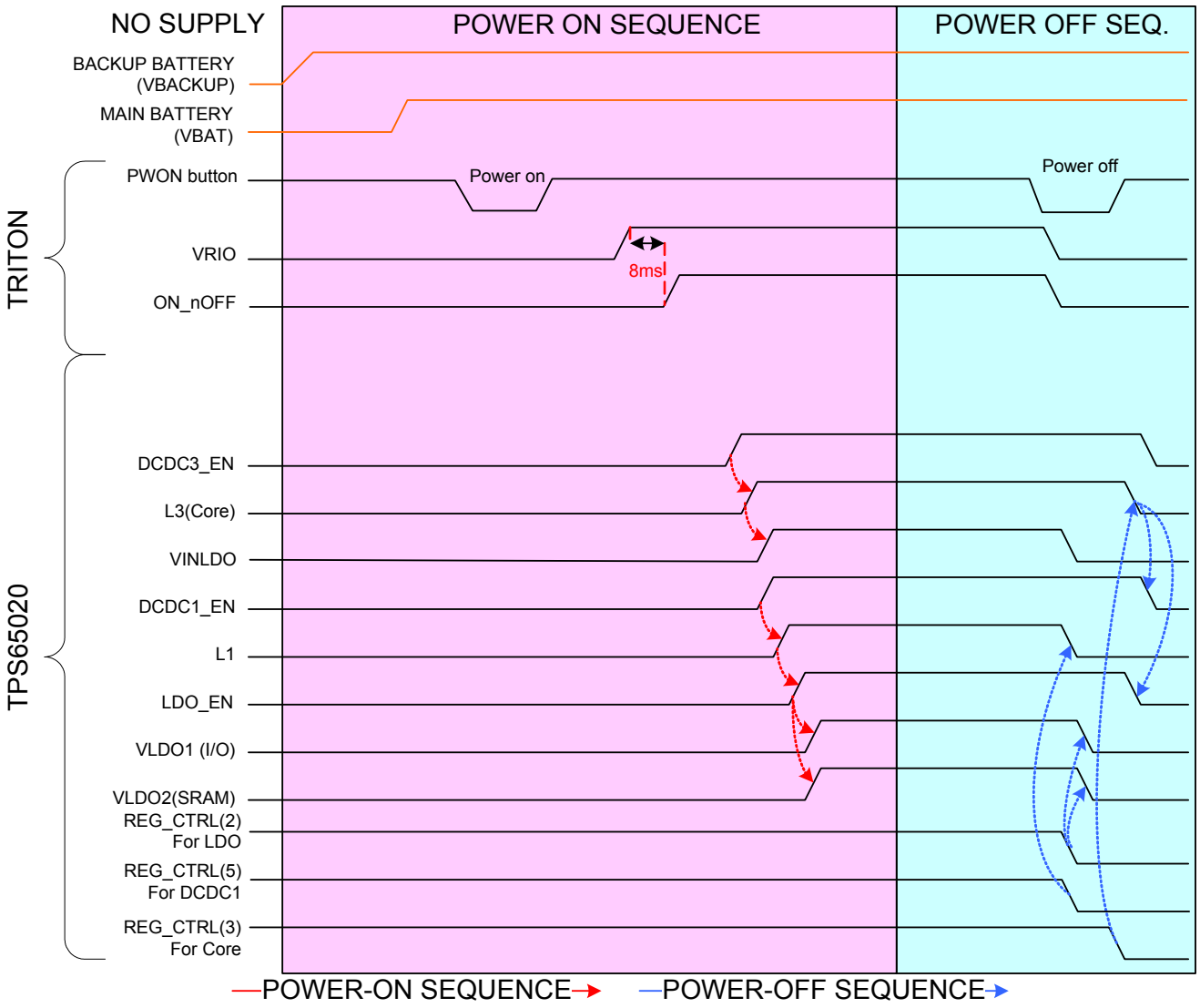


Figure 32 TPS65020 Power up/down sequence

11.5 DM290 BOOT SEQUENCE DESCRIPTION

DM290 provides three different Arm boot-up sequences:

- Self boot-up mode.
- Serial boot-up mode.

11.5.1 Serial boot-up mode

DM290 is externally downloadable through the SPI interface. After reset, Locosto can access to The ARM Internal Memory and write or overwrite boot code. This mode is selected with BTSEL1 input tied to low level and BTSEL0 input tied to high level.
DM290 is also externally downloadable through the I2C slave interface. This mode is selected with BTSEL1 input tied to high level and BTSEL0 input tied to low level.

11.6 DM290 POWER SAVING MODES

11.6.1 DM290 Power saving MODES DESCRIPTION

- **Power OFF MODE**
  The module is not powered and waiting for power on and reset.
- **DEEP Power down MODE**
  In Deep power down mode, all the logic is powered off, except I/O port to avoid failsafe problems.
- **Power down MODE**
  The oscillator is powered down so all internal clocks are OFF.
- **Sleep mode by Sleep mode register**
  Built-in PLL and all internal clock are stopped.
- **Sleep mode**
  Blocking the clock distribution (clock by clock) inside the module can partially or progressively stop the DM290.

11.6.2 DM290 MODES TRANSITIONS

- **Transition from Power off to Power down modes.**
  Not yet described
- **Transition from Power off to sleep modes.**
  When PWRDN is reset to 0, The FSM automatically switches from Power down mode to sleep mode.
- **Transition from sleep to active mode.**
  A negative pulse over than 2-system clock width on the GIO0 input brings the transition from sleep to active mode.
- **Transition from active to sleep modes.**
  Each clock module can be switch off independently by software through the MODx control register. To keep its content, the SDRAM (if used) must be set to self-refresh mode before stopping the SDRAM clock.
  All clocks can be turn off at the same time by software through the sleep mode register in the clock controller.
- **Transition from sleep to Power down modes.**
  In sleep mode, Pulling up PWRDN1 powers down the system clock oscillator.

11.7 Layout consideration

The CCP receive port is a set of differential pair signals going from the camera sensor to OMAP-DM290. This is a high-speed serial bus interface. Therefore, common mode voltage deviation should be minimized for maximum frequency operation (and maximum data throughput.) The traces for each differential pair should have equal lengths and matched impedance. Furthermore, the traces for each pair should be placed side by side so any high frequency crosstalk noise will be attenuated on both signals and thus cancelled out at the conversion from dual signal to single ended signal at the receiver end. The camera requires a source clock from OMAP-DM290. This clock is used to generate all the clocks internal to the camera as well as the CCP output port that sends data back to the OMAP-DM290. The trace for this clock should be as short as possible. A series termination resistor should be used (22 to 33ohms) to minimize the noise on the signal. The series termination resistor should be placed as close to OMAP-DM290 as possible.

All CCP signals should have a 100ohm series termination resistor at the source side of the trace (as close as possible to the output of the driver or to the input of the receiver.)

11.8 DM290 discrete power supply

11.8.1 Block Diagram

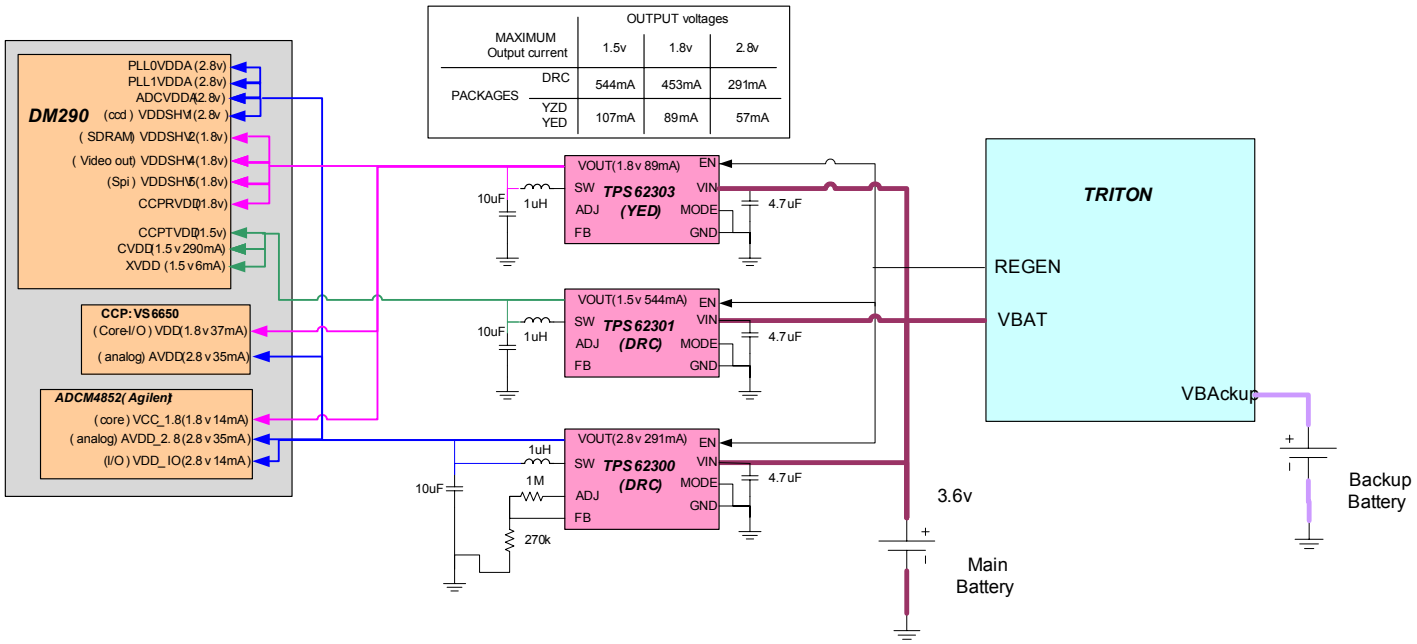


Figure 33: DM290 discrete power supply

11.8.2 Interconnection description

In this alternative solution Dm290 subsystem is powered by three discrete DCDC. The main advantage of this solution is the capacity to insert this logic groups in small-unused area. Triton Lite drives the core DCDC with REGEN and Locosto drive the 2 regulators for I/Os with GPIO 10, as the DM290 core must be up before its I/Os (ON sequence) and the DM290 core must go down after I/Os for OFF sequence. So power up and down sequences must be programmed in Locosto software code to meet the DM290 requirements. The table included in the bloc diagram describes the power limitation due each package dissipation capability. The solution size is thus limited by this constraint.

11.8.2.1 TPS62303 description

Output type	Output name	Dynamic range (V)	Tolerance (%)	Max drive (mA)	Typ tON time (us)	N
DCDC	VOUT	1.8v	-0.5/+1.3	89	250	

11.8.2.2 TPS62301 description

Output type	Output name	Dynamic range (V)	Tolerance (%)	Max drive (mA)	Typ tON time (us)	N
DCDC	VOUT	1.5v	-0.5/+1.3	544	250	

11.8.2.3 TPS62300 description

Output type	Output name	Dynamic range (V)	Tolerance (%)	Max drive (mA)	Typ tON time (us)	N
DCDC	VOUT	2.8v	-0.5/+1.3	291	250	

Table 40: TPS62303/62301/62300 OUTPUTS

11.8.2.4 Size comparison between centralized and discrete solutions

Solutions	Provider	Modules references	Package	Package size (mm)	Area (mm2)
DISCRETE SOLUTION					
DCDC for 1.8V 80mA	TI	TPS62303	YED	2x1	2
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 4.7uF 6.3v X5R	Murata	GRM21BF51A475ZA01	0805	2x1.25	2.5
Inductor 1uH 0.09Ohm 455mA	Taiyo Yuden	LQ LB2016T1R0M	0806	2x1.6	3.2
Total					10.2
DCDC for 1.5V 300mA	TI	TPS62301	DRC	3x3	9
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 4.7uF 6.3v X5R	Murata	GRM21BF51A475ZA01	0805	2x1.25	2.5
Inductor 1uH 0.09Ohm 455mA	Taiyo Yuden	LQ LB2016T1R0M	0806	2x1.6	3.2
Total					17.2
DCDC for 2.8V 90mA	TI	TPS62300	DRC	3x3	9
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 4.7uF 6.3v X5R	Murata	GRM21BF51A475ZA01	0805	2x1.25	2.5
Inductor 1uH 0.09Ohm 455mA	Taiyo Yuden	LQ LB2016T1R0M	0806	2x1.6	3.2
RESISTOR 1M 1%			0402	1x0.5	0.5
RESISTOR 270k 1%			0402	1x0.5	0.5
Total					17.7
Discrete solution Total area					45.10
POWER IC SOLUTION					
POWER IC		TPS65020		6x6	36
RESISTOR 590k 1%			0402	1x0.5	0.5
RESISTOR 390k 1%			0402	1x0.5	0.5
RESISTOR 470k 1%			0402	1x0.5	0.5
RESISTOR 130k 1%			0402	1x0.5	0.5
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 10uF 6.3v X5R	Murata	GRM21BR60J106KE19	0805	2x1.25	2.5
Capacitor 1uF 6.3v X5R	Taiyo Yuden	BJ105MA-T	0603	2x1.25	2.5
Capacitor 1uF 6.3v X5R	Taiyo Yuden	BJ105MA-T	0603	2x1.25	2.5
Capacitor 1uF 6.3v X5R	Taiyo Yuden	BJ105MA-T	0603	2x1.25	2.5
Inductor 3.3uH 0.5Ohm 340mA	Taiyo Yuden	LE LEMC2520T 3R3M	1008	2.7x2	3.4
Inductor 3.3uH 0.5Ohm 340mA	Taiyo Yuden	LE LEMC2520T 3R3M	1008	2.7x2	3.4
Total area for the power IC solution					62.3

Table 41: Power solutions Size comparison

Conclusion : the discrete solution seams to be less room consuming for the DM290 power supply but, looking the complete system power we see that we have an external 2.8V LDO used for the peripherals (not the DM290). When we use the TPS65020 we can remove this external 2.8V LDO and use the TPS65020 IC instead.
So the TPS65020 IC being able to replace the 4 external LDOs we can conclude that the two solutions : TPS65020 IC or the 4 external LDOs is equivalent in term of room and cost. Up to customer to make the most appropriate choice for their system.

11.9 VIDEO PATH

11.9.1 Bloc diagram

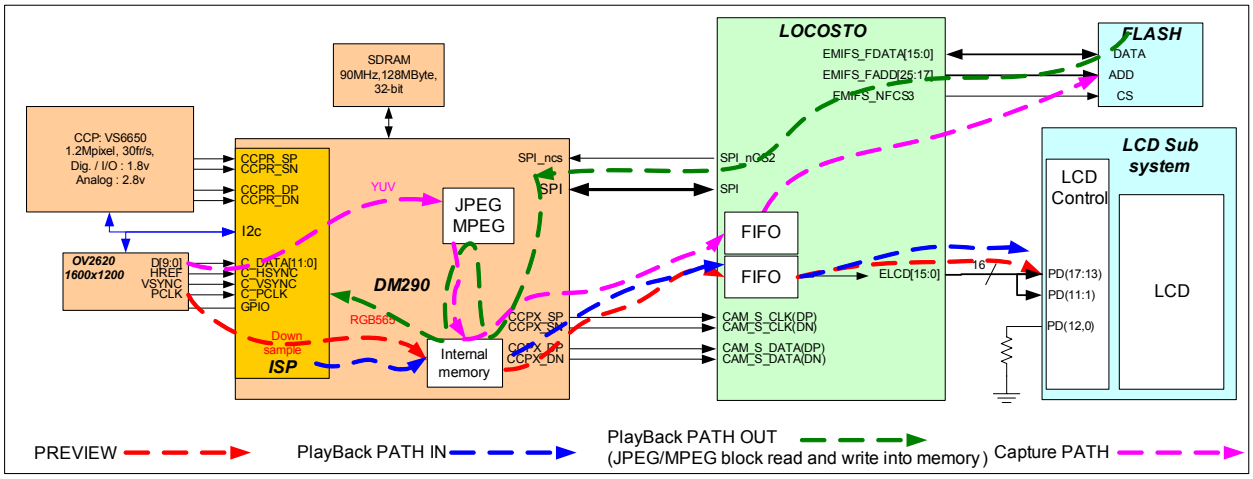


Figure 34: DM290 data flows

The interface between DM290 and Locosto should transfer compressed video, uncompressed preview data, and control data. In addition, the interface handles the overhead of framing codes for the transmission messaging protocol.
Above diagram gives a description of all paths needed to achieve the four video modes.

- Video capture with Encoding plus preview
- Video Decoding with playback
- JPEG Image Capture and Display

11.9.1.1 Video capture with Encoding plus Preview

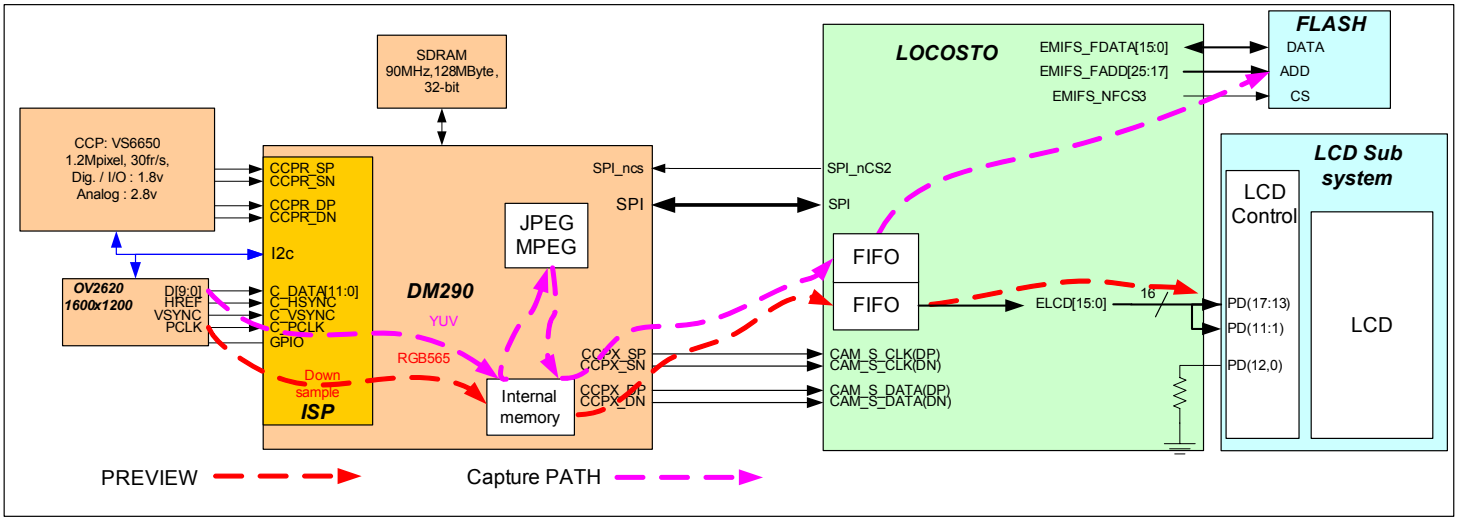


Figure 35: DM290 Video capture with Encoding plus Preview

The image Signal processor (ISP) converts Bayer RGB data from the camera to YUV format. It then sends them to the buffer memory (256Kbyte). Once sufficient amount of data is written in the memory:

- JPEG compression is performed for images.
- MPEG compression block for videos.

The compressed bit-stream is then translated in RGB565 format, written back to the buffer and pulled out to the CCP interface.
In addition to JPEG/MPEG compression the ISP block provides another down sampled image (with a lower resolution as QCIF) shown on the display without compression. The compact camera port (CCP) directly sends this display data out to Locosto.
We must support preview data transfer (uncompressed, QCIF, 15fps) and image capture (JPEG compressed) at the same time both on the CCP interface. For video capture, preview data is still transferred over CCP, but compressed video data is transferred to Locosto over SPI.

Data Type	Quantity	SPI Rate (Mbps)	CCP Rate (Mbps)
Compressed Video	CIF @ 30f/s (10:1 worst case)	4.87	
preview	QCIF @ 15f/s		6.08
Control data	-	0.4	
Framing codes	10% of total traffic	0.586	0.676
Total Data		5.86	6.76

Data from DM290 to Locosto

Data Type	Quantity	SPI Rate
Control data	-	160Kb/s
Framing codes	10% of total traffic	18Kb/s
Total Data		178Kb/s

Data from Locosto to DM290

Locosto receives this data in its camera port FIFO. JPEG/MPEG files are sent to the selected memory (FLASH or MMC or SD) through a DMA transfer. Preview images are directly sent to the display that accepts RGB565 image format.
In our case, the LCD controller only accepts RGB666 (18bit) format. The 16-bit LCD pixel signal is converted to an 18-bit LCD pixel signal by duplicating the LSB red signal to the LSB red signal and duplicating the LSB Blue signal to the LSB blue signal.

11.9.1.2 Video Decoding with playback or streaming

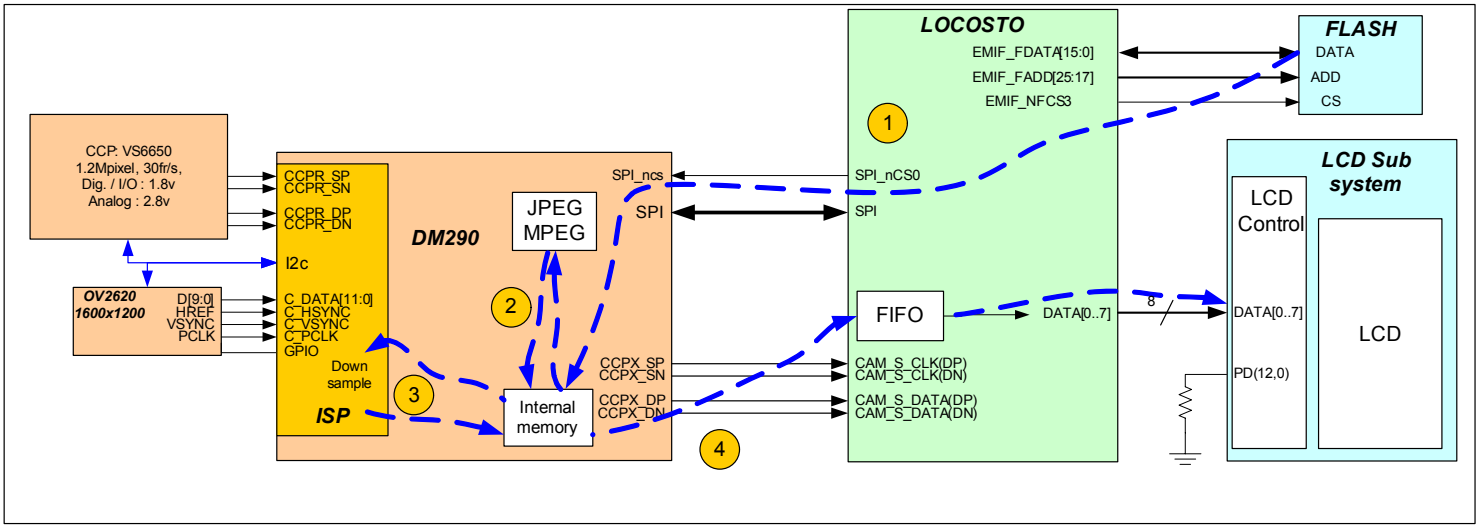


Figure 36: DM290 Video Decoding with playback or streaming

Video can be stored in any non-volatile memory attached to Locosto (FLASH, MMC, SD). It can also come from the network through the RF module and Locosto data pump. This video data has been compressed in the DM290 to limit the amount of needed memory.

1. Thus, it first need to be uncompressed before been sent to the display. Compressed data are sent to the DM290 through the SPI bus.
2. Once uncompressed, they retrieve their previous size. They are partially stored in the 2Mbit internal memory. The present display can show up to a QCIF image.
3. So the uncompressed mage is sent to ISP, where it is down sampled to the adequate size to meet the display characteristics.
4. Then it comes back to the internal memory and is sent to Locosto through the CCP bus.

In case of Visio-phony

We must support

- Video data transfer (compressed CIF, 30fps) on the SPI bus from Locosto to DM290.
- Video playback (uncompressed, QCIF, 15fps) on the CCP BUS from DM290 to Locosto.

Data Type	Quantity	SPI Rate (Mbps)	CCP Rate (Mbps)
Playback Video	QCIF @ 15f/s	0	6.08
Control data	-	0.400	
Framing codes	10% of total traffic	0.044	0.676
Total Data		0.444	6.76

Data from DM290 to Locosto

Data Type	Quantity	SPI Rate
Compressed Video	CIF @ 30f/s (10:1 worst case)	4.87
Control data	-	0.400
Framing codes	10% of total traffic	0.586
Total Data		5.86

Data from Locosto to DM290

11.9.1.3 Jpeg image capture

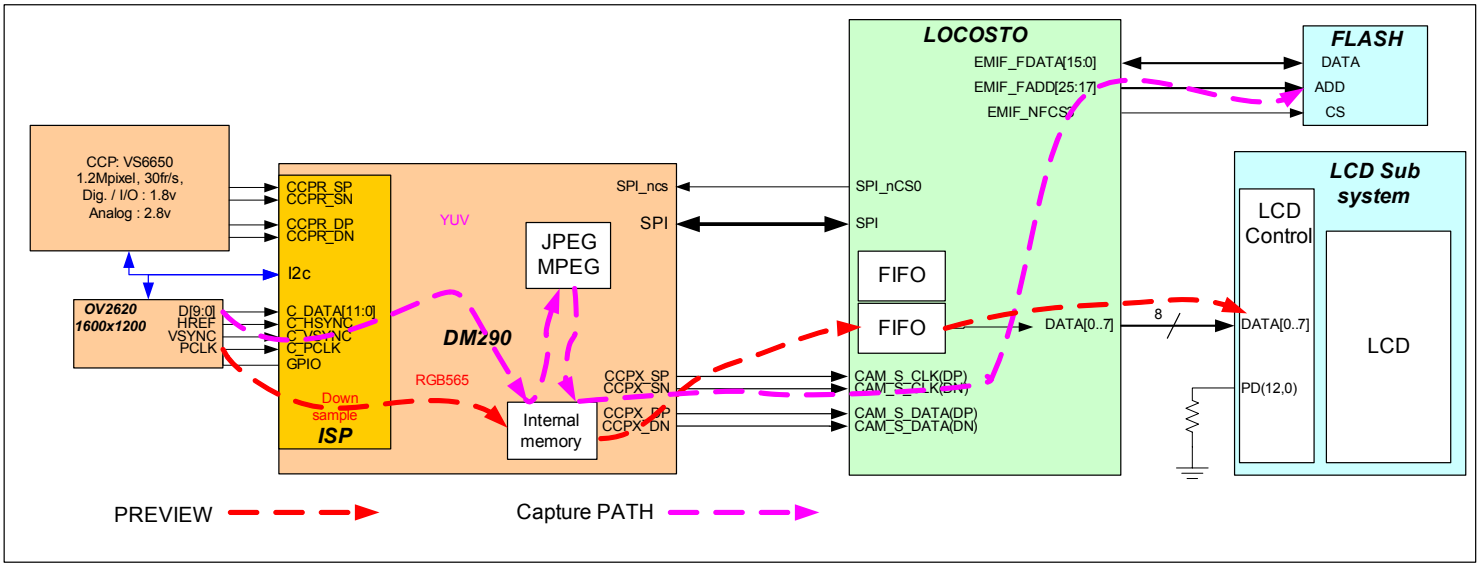


Figure 37: DM290 Jpeg image capture

The paths for JPEG (snapshot) is quite the same than for Movies except for the data flow, which is lower and capture path is through SPI. Report to Video capture with Encoding plus Preview for more detail on the data path.

We must support:

- Preview image data transfer (uncompressed, QCIF, 15fps)
- Image capture (3Mpixel,JPEG compressed 1:10, 15fps)

Data Type	Quantity	SPI Rate (Mbps)	CCP Rate (Mbps)
Compressed image	3Mp @1:10 15fps		75.5 or
Preview image	QCIF @ 15f/s		6.08
Control data	-	0.400	
Framing codes	10% of total traffic	0.444	8.39
Total Data		0.444	83.89

Data from DM290 to Locosto

Data Type	Quantity	SPI Rate (Mbps)
Control data	-	0.160
Framing codes	10% of total traffic	0.0178
Total Data		0.178

Data from Locosto to DM290

11.9.1.4 JPEG Image Display

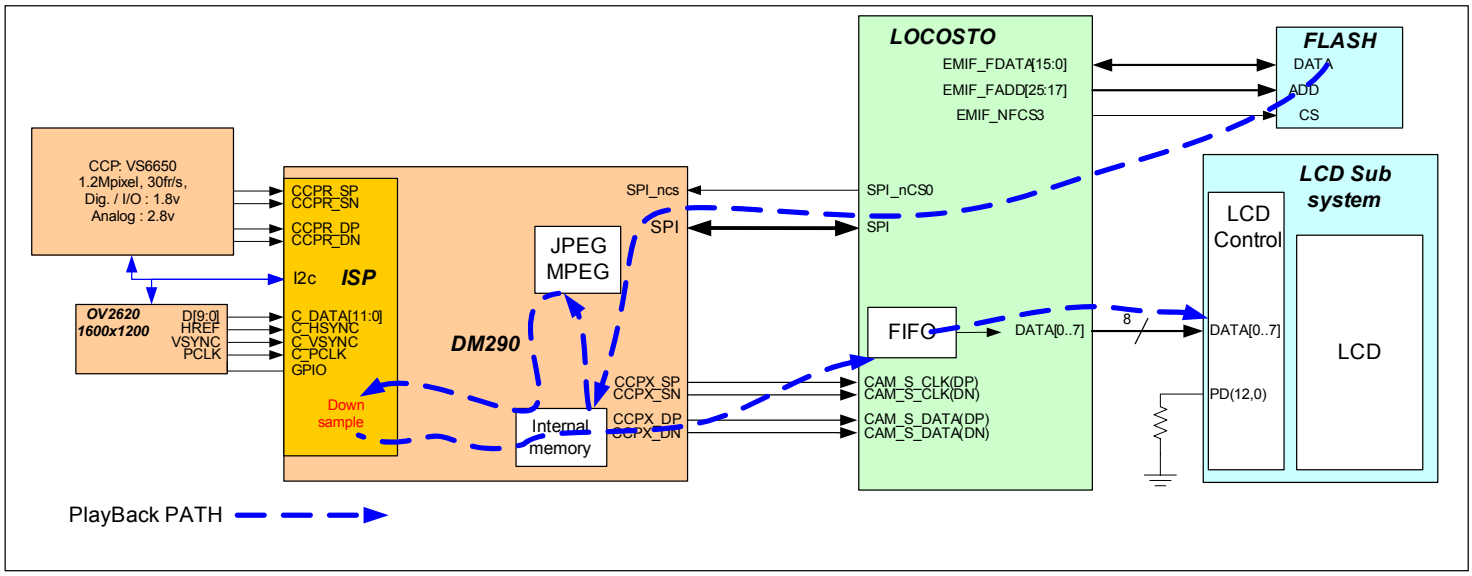


Figure 38: DM290 JPEG Image Display

The paths for JPEG (snapshot) is quite the same than for Movies except for the data flow, which is lower. Report to Video Decoding with playback paragraph for more detail on the data path.

We must support:

- Image data transfer (3Mpixel, compressed, 15fps) on the SPI bus from Locosto to DM290.
- Image playback (uncompressed, QCIF, 4fps) on the CCP BUS from DM290 to Locosto.

Data Type	Quantity	SPI (Kbps)	CCP (Mbps)
Playback Image	QCIF @ 4f/s (RGB565)		1.62
Control data	-	0.400	
Framing codes	10% of total traffic	0.044	0.180
Total Data		0.444	1.80

Data from DM290 to Locosto

Data Type	Quantity	SPI (Mbps)
Compressed Image	3Mp @ (5:1 worst case) 1f/s	10.1
Control data	-	0.400
Framing codes	10% of total traffic	1.17
Total Data		11.67

Data from Locosto to DM290

12 Locosto-Lite

12.1 System definition

The new Locosto-Lite system is a solution for customers to realize a very low cost system using the Locosto Lite processor.

12.1.1 Diff between Locosto and Locosto-Lite

Changes between the previously defined Locosto system and the Locosto-Lite system :

1. Triton Lite IC is changing for a new IC named Triton-Lite (see chap 12.1.3 for Triton-Lite def)
2. Memory : The PSRAM is 16Mb, the NOR flash is 32Mb, the NAND is removed.
3. LCD : In candy bar we can use a 96*96 main LCD connected to the LCD interface. No secondary LCD.
   In Clam shell : we use a 120*160 main LCD on the LCD interface and a secondary LCD (just time and date in black and white) on the SPI.
4. The RF is dual band muxed, it means that the 4 bands are accessible but only both of them in the same time.
5. No camera will be supported : no // camera, no CCP camera, no DM290.
6. BlueTooth and AGPS are not supported any more.
7. Locosto Lite has the same package than Locosto/Locosto + but the internal routing is different (test balls not accessibles at the same place/balls) to allow an easier board routing (less expensive).

12.1.2 Triton-Lite def

Triton-Lite is a new IC done by removing some signals from the Triton 1 described previously in this document.

Signals removed :

1. Pins VRVBUS, SWVBUS are removed. GND_VBUS and the power input VCC6 are keeping one ball each. So the USB master functionality is removed but the USB slave is maintained. Battery charge via USB is also maintained as VRUSB maintained.
2. The Triton DC/DC (not used with Locosto) is removed. So the pin VFBDD and SWDBB are removed but one Vcc1 input ball and one GND_DBB ball are maintained.
3. The dynamic voltage scaling Triton functionality (not used with Locosto) is removed, so the VMODE and PWROK pins are removed.
4. The not used with Locosto following pins are removed : WAKEUP2, P2_INT2, MCLK2.
5. 2 ADCIN signals are removed : ADCIN1 AND ADCIN2 (not used with Locosto).
6. The not used power-bus is also removed : PM_C, PM_D, PM_F.
7. The AUXO audio pin is removed.

12.2 Locosto-Lite System schematic

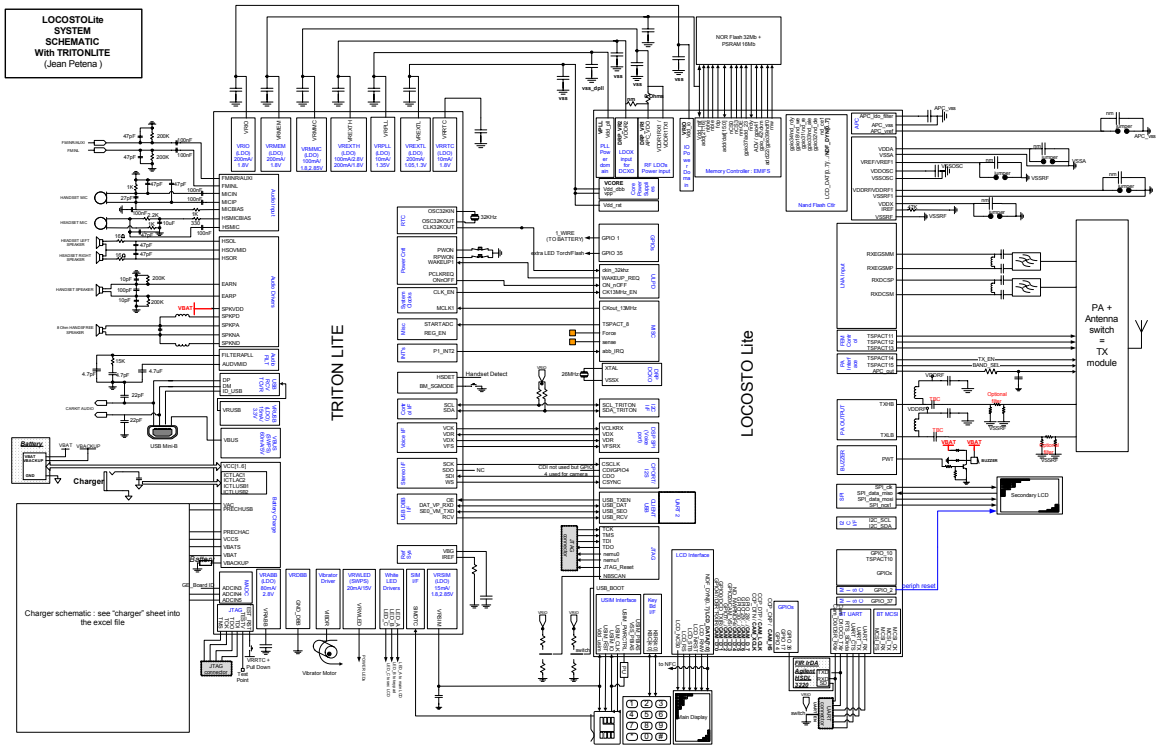


Figure 39 Locosto-Lite system schematic

12.3 Locosto-Lite main LCD

Main LCD short description

The LCD proposed for the Locosto_Lite syatem is the TFS (Three-Five Systems) 128RGB*160 TFT-LCD Module : TFS 6040-0082-01.

This LCD module is 8b I/F, 1.8v I/Os, compatible 68-series and 80-series. The Hitachi HD66773R driver/controller is embedded in the module.

12.3.1 Block diagram

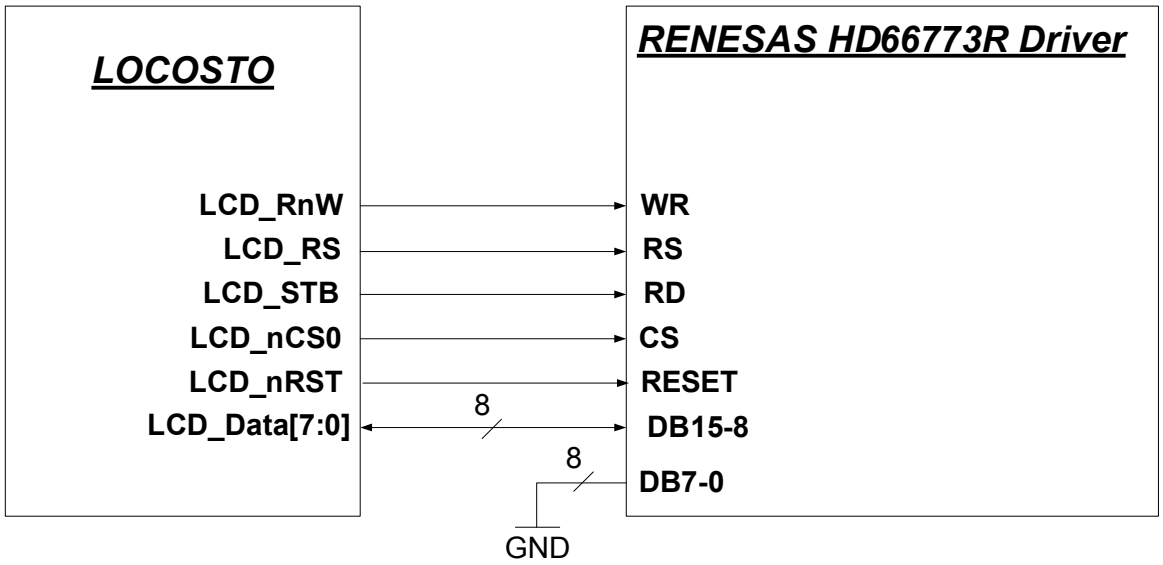


Figure 40 : LOCOSTO-LITE MAIN LCD connection

12.3.2 Interconnect Description

12.3.2.1 Connections between LOCOSTO-Lite and HD66773R

The HD66773R module can be directly connected to LOCOSTO-Lite processor through its LCD interface. The data for display DB (17..10) are written according to the values of the Chip Select and Reset signals in synchronization with WR, RD and RS signals.

LOCOSTO-Lite						HD66773R				
Signal	Ball	Mode	I/O	Power	Dir.	Signal	Pin on connector	I/O	Power	Comments
LCD_D0	E9	0	O	VDD_IO	→	DB8	13	I	VRIO	
LCD_D1	B8	0	O		→	DB9	12	I		
LCD_D2	C8	0	O		→	DB10	11	I		
LCD_D3	E8	0	O		→	DB11	10	I		
LCD_D4	B7	0	O		→	DB12	9	I		
LCD_D5	D8	0	O		→	DB13	8	I		
LCD_D6	C7	0	O		→	DB14	7	I		
LCD_D7	B6	0	O		→	DB15	6	I		
LCD_RnW	F9	0	O		→	WR	23	I		
LCD_RS	D9	0	O		→	RS	24	I		
LCD_STB	B10	0	O		→	RD	22	I		

LCD_nCS0	E10	1	O		→	CS	25	I		
LCD_nRST	C10	0	O		→	RESET	5	I		

Table 42 : LOCOSTO-LITE Main LCD interface

12.3.3 Power management

TFS gives the following numbers as power consumption :

_ Vcc Logic : 2.8v to 1.8v . Current TBD.
_ Vci analog : 2.8v. Current TBD.
_ LED : 3.6V / 45mA

12.3.4 Layout consideration

No available information from TFS but the usual following rules are applicables :

- Match all data and clock wire length.
- Avoid multiple impedance break as VIA or connectors.
- The lines being W wide, the space between 2 lines (data, clocks) must be 2W (to avoid crosstalk).
- The LCD bus must be referenced (layer above or below) by the GND plane (or Power plane if GND is not possible). This GND plane being NOT cut, to allow return current to close the loop.

ANNEX A : Stereo Headset specification (Jesper Pedersen 2005-05-27)

Table of Contents

1. Introduction

This document is an application note that describes the stereo headset implementation that is used on the TI reference “I-Sample”.

Physical interface

For cost and reliability reasons the general rule of thumb are that we want as few contacts as possible. This means that for a stereo headset with microphone we need four connections:

1. Left output channel
2. Right output channel
3. Microphone
4. Common ground

The most popular interface is a 2.5mm jack connector. However, these are only standardized up to 3 connections. The fourth connection can be implemented in different ways. The connector that TI has chosen for reference designs is similar to a standard 3-pin jack except that it has an outer collar ring that represents the fourth connection.
The reasons for choosing this type of connector are the following:

- A “standard” mono headset will fit into the same connector without creating short-circuits
- The connector is able to support the standard mono TTY jack.

The below images illustrates the physical male and female connectors chosen for I-Sample:

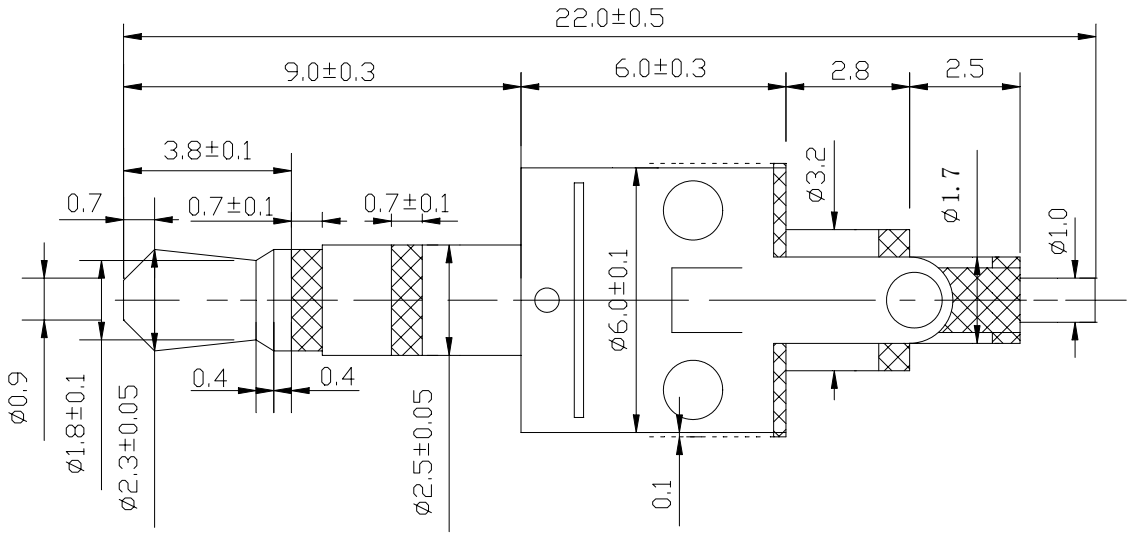


Figure 41: 4-pin jack connector. Male.

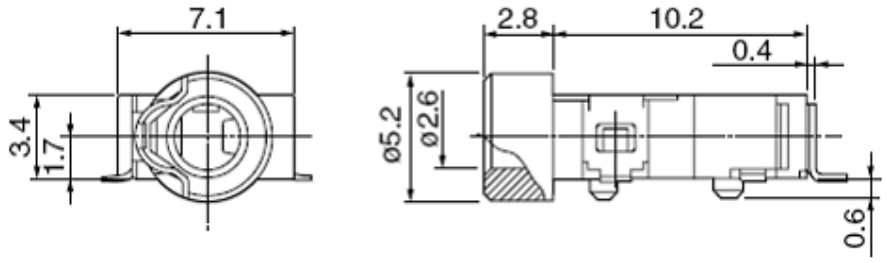


Figure 42: 4-pin jack connector. Female.

Headset circuit

The below circuit is used

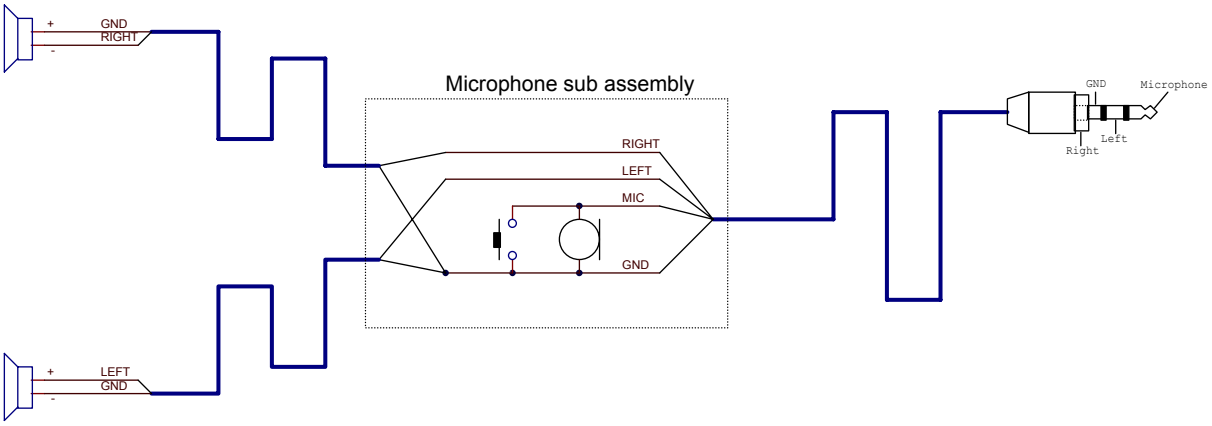


Figure 43: Headset schematic (simplified)

The speakers are specified at 150 ohm nominal impedance.
The microphone is a condenser type with integrated FET which requires a bias voltage present on the microphone signal. The bias current is 0.5mA max.
The microphone sub-assembly includes components for RF suppression (not shown on schematic) which minimize TDMA noise when the headset is used close to the GSM antenna.

Using the headset as a “Personal handsfree” device

As it can be seen on the simplified schematic, the connectors and the first piece of wire between the connector and the headphones are using a common ground wire. This is for cost, simplicity and reliability reasons.
However, when using common ground you will find that a signal sent to the headphones will be superimposed onto the microphone signal due to the impedance of the common ground.
In our case the speakers are 150 ohm and the common ground wire including connectors and contacts are approximately 0.15 ohm. This means that any signal sent to one of the speakers will be present on the microphone input attenuated by 60 dB. However, the microphone signal has about 40 dB more gain than the earphones. So in fact, the common ground wire causes a cross-talk from speaker to microphone of about -20 dB. This is way too much and will cause lot of echo in the far-end of a voice call.
To counteract this problem we take advantage of the fact that we have two speakers available to produce one signal as the voice is mono. So instead of sending the same signal out on both individual speakers we will send out a differential signal on the left and right speaker wires. The two speakers can now be considered to be in series with each other. The voltage at the mid-point of the speakers will always be 0V (even if it was not connected to GND) so no current will flow to the ground wire.

This is illustrated below:

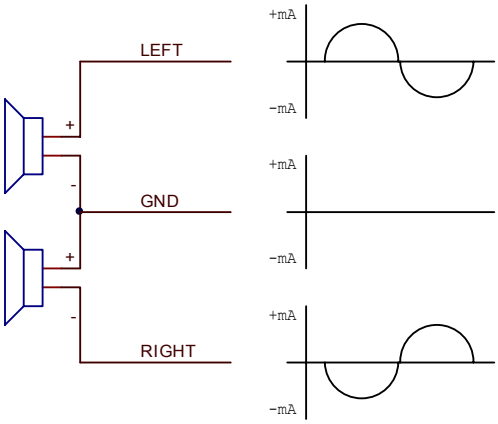


Figure 44: Current flow when left and right signals are generated as a differential signal.

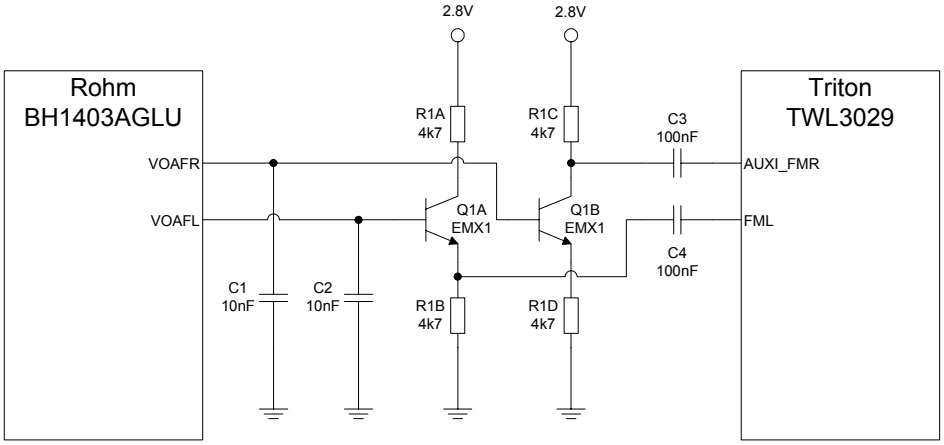
The signal presented to the used must be in-phase. So one of the speakers are connected in reverse (i.e. "+" goes to GND).
The Triton analog baseband chip includes a feature to drive a headset in differential mode. This feature must be enabled (register OUTEN1 bits HSOR must be in "Inverted Voice Speech" mode).

Using the headset as stereo-earphones for e.g. MP3

As the connections for one of the speakers are inverted the same is required when producing stereo sound.
This means that the software for e.g. MP3 playback must include a feature to invert left or right channel.

Using the headset as stereo-earphones for e.g. FM radio

When injecting an external analog stereo signal (e.g. FM radio) into the analog baseband (Triton / TWL3029) we face the problem that left and right channels are out of phase.
In this case an additional circuitry is required to ensure the phase of left and right channel are correct.
The following circuit suggestion is a low-cost, low-component-count yet high-performance solution that uses only two additional components (R1+Q1):



Circuit description

To maintain equal gain and frequency response on both channels it has been decided to implement a discrete bipolar x1 amplifier on each channel. One of the amplifiers is connected in non-inverting mode and the other in inverting mode.

When enabled, the outputs of the FM radio are biased at about 1.4V. This bias voltage is used for DC operating point of Q1A and Q1B as they are DC coupled to the FM outputs.
An advantage of using the bias of the FM radio is obviously component reduction. But an even greater advantage is power management; When the FM radio is put in standby mode the outputs will be pulled to ground effectively shutting down Q1A and Q1B.

"Hook" detection

The headset includes a "hook" key. The purpose of this key is to provide the user a method for answering or terminating calls without reaching out for the handset itself.
In the typical use-case you would have the phone in a pocket so it is more convenient to press a key that is physically placed on the microphone subassembly.
In order not to take up any more wires and connections this button is connected directly in parallel with the microphone.
The status of the button is detected either by observing the microphone bias current or voltage.