CeSARUS Modem

LOCOSTO Processor Silicon Errata

Document ref	locosto_silicon_errata	
Document version	1.0	
Release date	0ct, 5th 2007	
Source file		
Department	Wireless Terminals Business Unit	
Owners	K. Adjriou / C. Lancelot	
Approval	C. Labaume	Date: Sept, 26th 2007
Reviewers	A. Dalwani D. Rouchouse N. Ganesh C. Pitelet R.Quinzio	Date: Sept, 24th 2007
Status	**APPROVED**	

Important Notice

Texas Instruments Incorporated and/or its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products, software and services at any time and to discontinue any product, software or service without notice. Customers should obtain the latest relevant information during product design and before placing orders and should verify that such information is current and complete.

All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment. TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI products, software and/or services. To minimize the risks associated with customer products and applications, customers should provide adequate design, testing and operating safeguards.

Any access to and/or use of TI software described in this document is subject to Customers entering into formal license agreements and payment of associated license fees. TI software may solely be used and/or copied subject to and strictly in accordance with all the terms of such license agreements.

Customer acknowledges and agrees that TI products and/or software may be based on or implement industry recognized standards and that certain third parties may claim intellectual property rights therein. The supply of products and/or the licensing of software does not convey a license from TI to any third party intellectual property rights and TI expressly disclaims liability for infringement of third party intellectual property rights.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products, software or services are used.

Information published by TI regarding third–party products, software or services does not constitute a license from TI to use such products, software or services or a warranty, endorsement thereof or statement regarding their availability. Use of such information, products, software or services may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Recipient agrees that it will not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S, EU and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S or other applicable laws, without obtaining prior authorisation from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws. This provision shall survive termination or expiration of this Agreement.

According to our best knowledge of the state and end-use of this product or technology, and in compliance with the export control regulations of dual-use goods in force in the origin and exporting countries, this technology is classified as follows:

- US ECCN: 5E002
- EU ECCN: 5E002
- other country ECCN: *to be eventually completed.*

and may require export or re-export license for shipping it in compliance with certain countries regulations.

History

Version	Date	Author	Notes
0.1	April, 21st, 2006	C. Lancelot	1
0.2	June, 5th, 2006	C. Lancelot	2
0.3	July, 4th, 2006	C. Lancelot	3
0.4	Sept, 13th 2006	C. Lancelot	4
0.5	Dec, 13th 2006	C. Lancelot	5
0.6	Dec, 21st 2006	K.Adjriou	6
1.0	Sept, 24th 2007	K.Adjriou	7

NOTES:

1. Creation from omapv1030_processor_silicon_errata.doc.
2. Add ES2.0 related information.
3. Updated with reviewer feedback. Released.
4. Added limitations **2.7**, **2.8**, **2.9**, **2.10**, **2.11**, **2.12**
   Added bugs **1.5**
   Updated limitation **2.2**
5. Added limitations, **2.13**, **2.14**
   Added bugs **1.6**, **1.7**, **1.8**, **1.9**, **1.10**
   Updated workaround for bug **1.5**
6. Approved release
7. Added bugs **1.11**, **1.12**, **1.13**
   Updated workaround for bug **1.5**
   Added limitation **2.15**, **2.16**, **2.17**
   Updated workaround for limitation **2.3**

LOCOSTO Silicon Errata

Note: This document describes the LOCOSTO and LOCOSTO LITE bugs, limitations and enhancements with suggested workarounds. As this information is dated, updates will be provided.

The bugs, limitations and enhancements are applicable for both LOCOSTO and LOCOSTO LITE unless specified otherwise.

Topics

List of tables

List of figures

References

[1] Locosto VRSIM GPIO Customization Notes
[2] APN227 Locosto PG2.0 RMS PE Issue

Note:
Please contact you local TI representative to get the reference documents listed above.

1. LOCOSTO Processor Bugs Description

1.1 VREXTL rejection on VRIO

IMPACT
Negligible over power consumption in reset phase.

DESCRIPTION
During about 3.8ms, when VREXTL (Locosto core power supply) is switched from OFF to ACTIVE mode and VRIO maintained to OFF mode, the level on VRIO changed from 0 to 800 mV.

WORKAROUND
No.

STATUS
Deferred.

1.2 Parity error on last character avoid switching from Tx to Rx in T = 0 protocol

IMPACT
Unable to switch the direction in T = 0.

DESCRIPTION
Whenever there is a sequence of bytes sent from the USIM controller to the SIM card, and the last byte has a parity error detected by the SIM card, the USIM controller fails to switch from TX to RX mode until the parity error is cleared.

USIM_RESENT interrupt should fire if CONFRESENT (bits [10:8]) of USIMCONF2 register is configured with a resent number and the character is actually resent the expected number of times. However the last TX character with parity error is never resent and the interrupt never fires.

WORKAROUND

Here is the description of the SW workaround in case of parity error occurring on the last byte of a command:

- If the parity error is indicated, check FIFOTX_EMPTY (bit 7) of USIM_FIFOS register:
  - If FIFO_TX is not empty then do nothing.
  - If FIFO_TX is empty, write a dummy byte in the FIFO_TX (USIM_DTX register).
- If the parity error indication has disappeared, the FIFO_TX must be reset by setting FIFOTX_RESET (bit 6) of USIM_FIFOS register to '1', in order to prevent the transmission of the dummy byte after the repetition of the last byte of command.

STATUS
Open.
SW workaround for ES2.0 is under validation.
Issue is planned to be fixed in future ES.

1.3 DCXO start-up

IMPACT
DCXO unable to start-up.

DESCRIPTION
DCXO doesn't start-up.

WORKAROUND
Add a 1.5Mohms pull-down resistor to ground on Locosto XTAL pad D15.
Refer to **Error! Reference source not found.** showing the schematic changes around XTAL pad (see resistor R4).

STATUS
Open.

1.4 Keyboard / XTAL interaction

IMPACT

RF performance degradation (phase error).

DESCRIPTION
When a keyboard key is pressed the DRP PLL has an out of specification phase error.

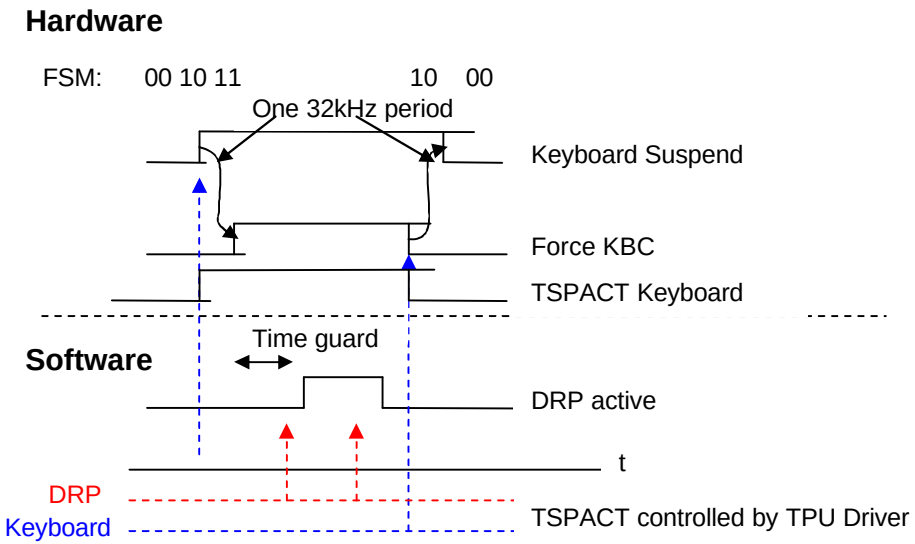
The root cause is a coupling between XTAL and keyboard signals.
This coupling occurs at chip substrate level and may be increased by routing on board if XTAL track is close to keyboard tracks.

WORKAROUND
It is a combination of both HW & SW workarounds.

The principle is to prevent keyboard scan activities while RF activity (DRP active).
In ES2.0, the internal TSPACT4 controlled by TPU is used to hold the keyboard activity while the DRP is active (both RF TX and RX activities).

The Figure 1 illustrates the principle of the workaround.

Figure 1: Keyboard / XTAL interaction workaround principle



STATUS
Open.

1.5 USIM Finite State Machine stuck in NC_PWR_OFF state

IMPACT
Calls not possible anymore unless restart of the UICC driver together with SIM card.

DESCRIPTION
When using the Clock Stop mode whose purpose is to stop the USIM card clock (*sim_clk*) to save power while in transmit mode, it sometimes happens that the USIM FSM gets stuck in NC_PWR_OFF state.

When the command bit 5 (CLOCK_STOP_CMD) of USIMCMD register is set to 1, the clock stop mode is activated and the USIM FSM is in the CLOCK_STOP state. The CLOCK_STOP_CMD bit must be reset to 0 to exit this CLOCK_STOP state and enter the CLOCK_RESTART state. However it sometimes happen that after resetting the CLOCK_STOP_CMD bit, the FSM goes to WARM_RESET state which finally drives the FSM to the NC_PWR_OFF state (Not Connected state).

WORKAROUND
The purpose of this workaround is to control by SW the clock stop sequence; therefore the workaround is split in 2 parts, one related to the Clock Stop sequence and another one related to the Clock Restart sequence.

- Clock Stop sequence:
  - Set bit 5 (CLOCK_STOP_CMD) of USIMCMD register to '1'
  - Wait till the FSM is in CLOCK_STOP state

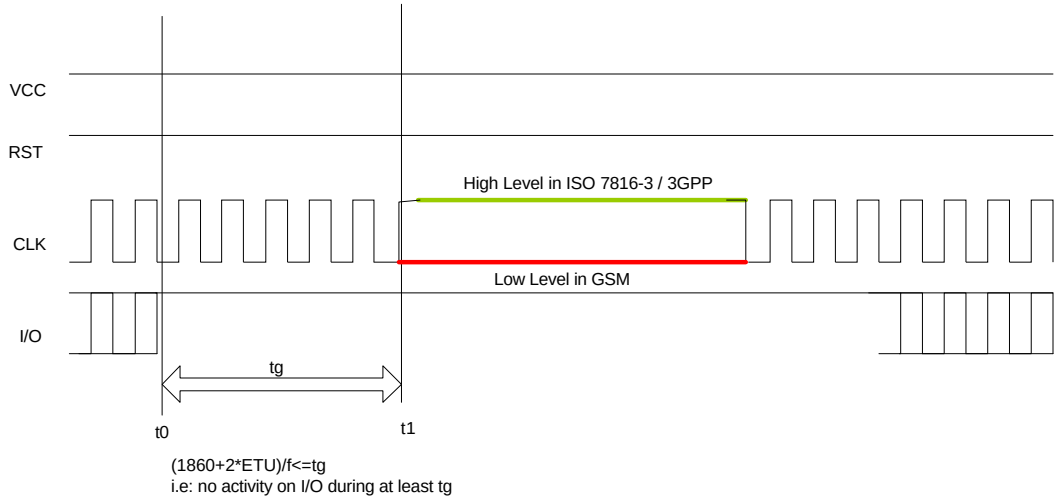
- Clock Restart sequence:
  - Set bit 8 (SOFT_NHARD_FIDI_PROG) of CONF5_REG register to '1'
    => Switch to SW configuration
  - Set bit field 11:0 (SAM1_DIV) of CONF_SAM1_DIV register to '0x000'
  - Wait during (1024 * 20.CPU CLOCK cycle) which is the worst case of HW configuration
  - Set bit 3 (MODULE_CLK_EN) of USIMCMD register to '0' to deactivate the module clock

  The card clock is stopped and the FSM is in the CLOCK_STOP state.

- Set bit 5 (CLOCK_STOP_CMD) of USIMCMD register to ‘0’
- Set bit 8 (SOFT_NHARD_FIDI_PROG) of CONF5_REG register to ‘0’
  => Switch back to HW configuration
- Set bit 3 (MODULE_CLK_EN) of USIMCMD register to ‘1’ to reactivate the module clock.

Start the clock-stop sequence within 1860 Sim clock cycles (Tg) from the end of the last character (typically a received character) to ensure that the FSM entry to CLOCK_STOP state is triggered by the internal Tg timer expiry, and not the programming of CLOCK_STOP_CMD.

Figure 2 Clock stop sequence



STATUS
Open.

1.6 I2C ARDY interrupt reasserted after being cleared

IMPACT
I2C ARDY interrupt re-asserted.

DESCRIPTION
When an I2C ARDY interrupt occurs, after having processed the request, the interrupt is cleared by writing the ARDY bit of I2C_STAT register.

However, the ARDY status bit is not cleared by the write access to I2C_STAT[ARDY] and the IRQ line is de-asserted and then re-asserted.

WORKAROUND
There are two possible software workarounds:

- When clearing the ARDY interrupt, check if the IRQ line is re-asserted and then serve ARDY interrupt again. The second write access to I2C_STAT[ARDY] will be correctly performed.
- When serving the ARDY interrupt, always write twice in the I2C_STAT[ARDY] register.

STATUS
Open.

1.7 DRP wrapper memory not accessible after a watchdog reset

IMPACT
After a watchdog reset, DRP wrapper SCRM memory bus hangs.

DESCRIPTION
A watchdog reset is generated while a transaction on DRP wrapper memory is on-going by SCRM.
After reset when the ARM starts accessing the DRP wrapper memory again, a time-out occurs because the DRP wrapper SCRM memory bus is hung. This is due to the fact that watchdog reset resets DRP wrapper, but does not reset the DRP.

WORKAROUND
After watchdog reset, a soft reset of the DRP shall be done before the ARM performs its first access to the DRP wrapper memory.

STATUS
Open.

1.8 Hang-up on wake-up event from deep sleep when DCXO ON

IMPACT
Phone deadlock without possible recovery other than battery removal.
Identified impacted scenarios (not exhaustive list):

- battery charging
- Locosto idle while Bluetooth activity.

DESCRIPTION
When Locosto ULPD wakes-up from deep sleep while DCXO 13MHz clock is already on and propagated outside DRP (but not to DBB core yet), there is a risk of Locosto hang, causing a phone deadlock without possible recovery other than battery removal.

The configuration when deadlock can occur is deep sleep during battery charging (Triton-Lite externally requests DCXO ON for charging operation) or during Bluetooth activity (Bluetooth device externally requests DCXO clock through Triton-Lite). In both cases, the DCXO 13MHz is kept running while the Locosto ULPD state machine can go in and out of a deep sleep state.

WORKAROUND
The generic workaround consists in preventing the condition that can generate the hang up, i.e. wake-up event from deep sleep when DCXO ON.

STATUS
Open.
Issue is planned to be fixed in ES2.1.

1.9 ARM access into API corrupted during API mode transition by DSP

IMPACT
Data read in 32-bit accesses by ARM from API can be corrupted. ARM 16-bit API read accesses are safe.
This issue was identified to be cause of some call drops.

DESCRIPTION
If the DSP performs a transition of the API mode (HOM to SAM or SAM to HOM) during an ARM 32-bit read access, the data read by the ARM processor from API is corrupted.
For instance, instead of reading 0xABCD**EFGH** the ARM will read 0xABCD**ABCD** (in 32-Bit hex value).

WORKAROUND
Prevent any 32-bit read access by ARM to API by performing only 16-bit ARM read when DSP is changing mode in parallel from HOM to SAM or SAM to HOM.
.

STATUS
Open.

1.10 Camera core DMA request 1 asserted with FIFO empty if auto-idle enabled

IMPACT
Camera core DMA request 1 can not be used.

DESCRIPTION
The camera core DMA request 1 is normally generated at the end of a camera frame if data remains in the FIFO.

However if auto-idle is enabled, camera core DMA request 1 remains asserted even if FIFO is empty. Consequently trash data is read from camera core.

WORKAROUND
The SW workaround is to make sure that the image is multiple of FIFO threshold (by deriving the FIFO threshold based on the image size), instead of using the DMA request 1.

STATUS
Open.

1.11 CPORT control register being written without intention

IMPACT
CPORT control register can be updated without intention.

DESCRIPTION
When a register is being written into a rhea peripheral, other than CPORT, on TIPB strobe 0, CPORT control register can also be written.

WORKAROUND
The SW workaround consists in not allocating CPORT module peripheral to ARM and cDSP when CPORT registers are not being written.
Set MPU_PERIPH_LOCK bit of CPORT_TSW_MPU_CONF register and DSP_PERIPH_LOCK bit of CPORT_TSW_DSP_CONF register to “0”

STATUS
Open.

1.12 Data could be missed while receiving data through MSSPI in DMA mode

IMPACT
MSSPI in DMA read mode is not working.

DESCRIPTION
MSSPI FSM can start a new transaction even though the first one is not read by DMA.
Data could be missed while receiving data through MSSPI in DMA mode.

WORKAROUND
The WA consists to use CPU in pooling mode instead DMA. There is no performance loss with the CPU, but the CPU load is very high (~90%) meaning that if you want to run something else it will impact the performance.

STATUS
Open.

1.13 USIM: Parity Error when switching to high-speed

IMPACT

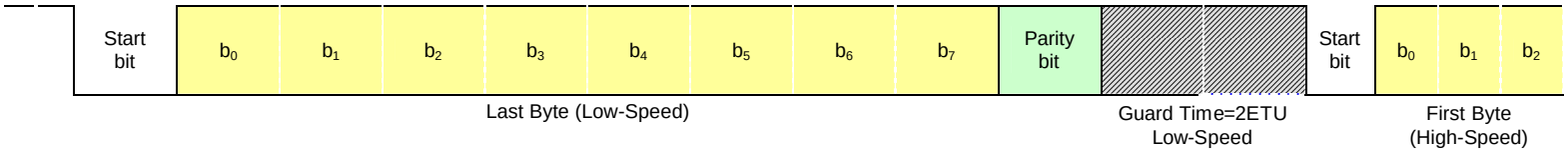
USIM Parity Error when switching from Low-Speed to High-Speed.

DESCRIPTION

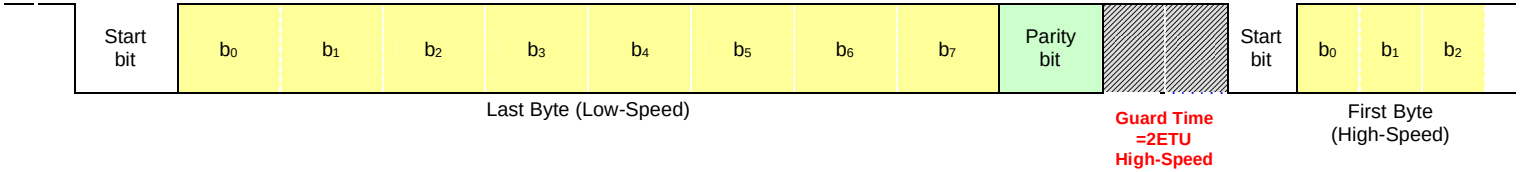
When switching from Low-Speed to High-Speed, the guard time of the last character frame should last 2 ETU whose length is the one from the Low-Speed bit-rate. But in fact the length of this guard time is from the High-Speed bit-rate.
As a consequence, since the duration of this guard time is shorter than expected, if a new character frame is immediately sent at High-Speed, the start bit of this character frame will be processed as a parity error of the last character frame of the Low-Speed and therefore this last character will be repeated.

Figure 3: Guard time when switching from Low-Speed to High-Speed.

Expected behavior



Wrong behavior



WORKAROUND

The SW workaround consists in adding a delay of 5ms before sending the first High-Speed character frame.

STATUS

Open.

2. LOCOSTO Processor Limitations Description

2.1 Electrical SIM FTA test failure

IMPACT
The issue is only FTA related and has no impact on normal SIM usage.

The 2 following electrical SIM FTA test cases fail:
- 27.17.2.1.1
- 27.17.2.1.2

This issue will appear on SIM FTA only after the 16th June 2006 (refer to following description for details).

DESCRIPTION
There is a leakage path through pad internal ESD diodes between USIM IOs (USIM_RST, USIM_IO and USIM_CLK) and VRSIM power supply.

During SIM FTA electrical tests, the SIM IT3 test equipment injects current on USIM IOs before VRSIM is activated. Moreover a resistive load is activated by the test equipment on VRSIM.

Due to that injection of current from SIM IT3 test equipment on USIM IOs before VRSIM is activated (Triton Lite VRSIM LDO is OFF), current flows from USIM IOs to VRSIM through the ESD diode leakage path.
A DC offset is then present on VRSIM.
When activating VRSIM (Triton Lite VRSIM LDO switched from OFF to ON), the DC offset on VRSIM causes overshoots on VRSIM in both 1.8V and 3.0V cases.

From June 16th 2006, the SIM IT3 test equipment will be officially updated for SIM FTA usage involving a change on source currents (used to inject current by test equipment on USIM IOs) and resistive loads on the test equipment.
These changes will increase the DC offset on VRSIM before its activation. They will cause the overshoots to be over ETSI authorized limits causing failures on SIM FTA electrical test cases 27.17.2.1.1 and 27.17.2.1.2.

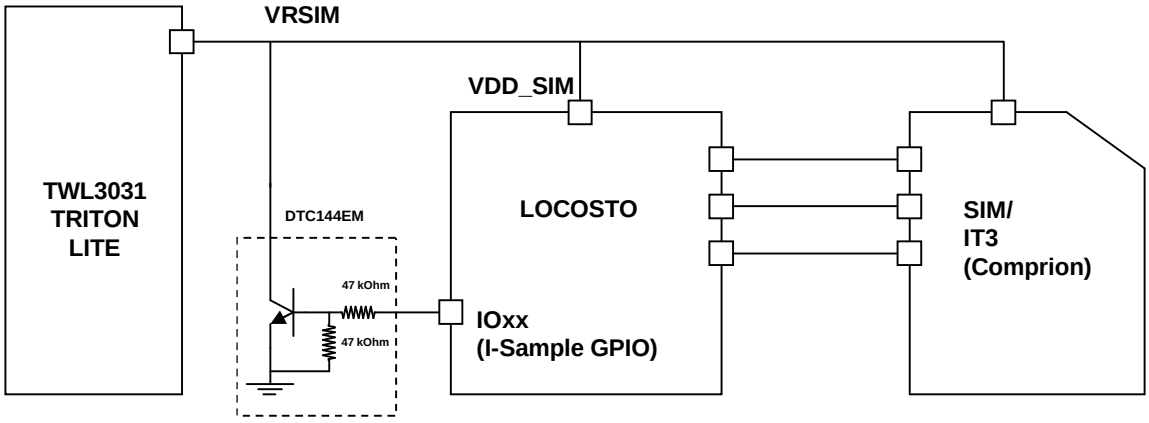
WORKAROUND
The workaround consists in adding an external transistor controlled by software through a Locosto GPIO and capable of sinking to ground the current flowing from USIM IOs to VRSIM.
This will considerably decrease the DC offset and overshoots on VRSIM.

In TI software reference releases, the Locosto GPIO_11 has been selected to control the external transistor. The customer may select any other Locosto GPIO to control the transistor at his convenience. Refer to [1] Locosto VRSIM GPIO Customization Notes for details on the necessary changes to be done for customizing the SW for a different GPIO than that supported by the reference SW.

The circuitry with the external transistor is shown on Figure 4.

The recommended external transistor part number to use is the “DTC144EM”.

Figure 4: Electrical SIM FTA test failure – External transistor schematics



STATUS
Open.
Issue planned to be fixed in future ES.

2.2 13MHz output clock Phase Noise not compliant with TI Bluetooth requirements

IMPACT
Bluetooth carrier frequency drifts.

DESCRIPTION
The 13MHz output clock from Locosto device to TI Bluetooth device has increased jitter when GSM active causing Bluetooth carrier frequency to drift and marginally fails the specification.

WORKAROUND
New TI Bluetooth device firmware available.

STATUS
Open.

2.3 RMS Phase error

IMPACT
RMS phase error failure at DCS1800 and PCS1900 integer channels.

DESCRIPTION
RMS phase error above maximum thresholds at DCS1800 and PCS1900 integer channels.

WORKAROUND
The workaround consists in injecting a non-synchronous signal referred to as *dithering signal* into XTAL input (D15) pin through a filtering network. The dithering signal is of relatively small amplitude with respect to reference FREF signal.
The dithering signal is generated by routing an internal DRP clock signal to either Locosto GPIO_17 (B9), ND_nWP (E5) or LCD_nRST (C10) pin at frequency called *dithering frequency* controlled by

DRP software generated only when transmitting on integer and half-integer channels in the DCS1800 and PCS1900 band.

In TI software reference releases, the Locosto GPIO_17 pin has been selected to output the internal DRP clock signal. Refer to [2] APN227 Locosto PG2.0 RMS PE Issue for details on the necessary changes to be done for customizing the SW for a different pin than that supported by the reference SW.

STATUS
Open.

2.4 Secure ROM code services failed while DMA accesses IMIF in parallel

IMPACT
Secure ROM code services such as binding/unbinding services can not be used by MCU when MCU DMA accesses to IMIF (internal memory) occur in a non 32-bit mode.

In the TI software foundation, only the IMEI and MEPD features driven by the modem protocol stack use the secure ROM code services.

However, the customer software could use any secure ROM code services for any other purposes.

DESCRIPTION
Secure ROM code services failed while MCU DMA accesses to IMIF in parallel occur in a non 32-bit mode.

The Locosto c027 device shall be allowed to perform any MCU DMA transfers during the execution of any secure ROM code services.

However, the concurrent MCU DMA transfers to/from internal memory and the execution of any secure ROM code services are not possible.

WORKAROUND
The software workaround consists in preventing simultaneous accesses to secure ROM code services and non 32-bit MCU DMA accesses to internal memory.

Before accessing secure ROM code services, one shall upgrade any code calling the secure ROM code services based on the following sequence:

- Save interrupt context and Mask all ARM interrupts (ARM CPSR register)
- Identify the DMA channel reserved to the MCU system using the allocation register (DMA.DMA_CAR).
- Check the bit 7 (EN) is ‘0’ for all MCU DMA channels using channel control registers (DMA.DMA_CCR).

The check shall be restricted to the enabled MCU DMA channel performing transfer to/from the IMIF port with non 32 bit mode.

- If the MCU DMA channels are all disabled, then the secure ROM code service can be called. If not, an error shall be returned (the error means the secure ROM code is not available due to concurrent DMA transfers).
- Restore ARM interrupt context.

STATUS

Open.
Issue is planned to be fixed in future ES.

2.5 ADV & ND_RDY IO cells too weak

IMPACT
Limit the number of components to connect to ADV and ND_RDY pads.

DESCRIPTION
ADV & ND_RDY cells are too weak to support more than 3 external components.

WORKAROUND
No.

STATUS
Open.
Issue planned to be fixed in future ES.

2.6 Deep sleep not possible when UART or MSSPI input clock different from 52MHz

IMPACT
Locosto can't enter into deep sleep.

DESCRIPTION
If the UART or MSSPI module input clock is the free running clock different from 52MHz clock domain Locosto does not enter in deep sleep mode.

WORKAROUND
If the UART and MSSPI clocks need to be cut when bridge enters sleep, then the bits [1:0] (CNTL_CLK_PROG_FREE_RUNNING) of CNTL_CLK_PROG_FREE_RUNNING register must be set to "10" to select the 52MHz clock domain.

STATUS
Open.

2.7 No internal pull-up on UART_RX & UART_CTS

IMPACT
UART_RX and UART_CTS are floating inputs at reset because internal pull-down are not enabled by default.
As only internal pull-down are available, external pull-up resistors are required increasing the BOM.

DESCRIPTION
UART_RX and UART_CTS are inputs only.
Both UART_RX and UART_CTS require a pull-up resistor to maintain their default level to high level.
Only internal pull-down are available in Locosto ES2.0.
Moreover, at reset the pull-down are not enabled causing UART_RX and UART_CTS to be floating at reset.

WORKAROUND

External 10kΩ pull-up resistors to VRIO power domain must be added on both UART_RX and UART_CTS.

STATUS
Open.
Issue is planned to be fixed in future ES.

2.8 Undershoots & Overshoots

IMPACT
RF spurs increase.

DESCRIPTION
Some Locosto interfaces like for example camera, LCD and memory interfaces present some under/overshoots.

These under/overshoots are due to low Locosto IO buffer impedance (about 15 Ohms) compared with the trace impedance (from 40 to 60 Ohms).

Locosto IO buffers having a fast rising time (strong slew rate, about 4 to 4.5V/ns) and depending on trace length at board level, this causes signal reflections producing under/overshoots.

WORKAROUND
The workaround to reduce the under/overshoots is to realize a board routing following below rules:
- Reduce the impedance of the lines as much as possible
- Match the length of the traces connected to the same device
- Make the traces as short as possible
- For trace longer than 25mm, add a serial resistor to match the line

In next ES, Locosto pads listed in Table 1 will have their IO cell changed.
Two types of changes will apply:
- Change current buffers (8mA, 15 Ohms impedance) to smallest buffers (4mA, 50 Ohms impedance) on interfaces that do not need strong rise time: **LCD**, **camera**, **UART**, **TSPACT**, **SPI**, **KBD**.
- Modify current buffers (8mA, 15 Ohms impedance) to new buffer with higher impedance (8mA, 37 Ohms) for **memory** interfaces due to the rise time requirements: **EMIF NOR/PSRAM**, **NAND**.

Table 2 lists the changed IO cells with the new IO cells for next ES.

Table 1: List of Locosto pad concerned by IO cell changes

Pin Number	BGA Address	BGA Name	DIR	IO Cell	IO Cells change proposal ALR
3	U2	**spare_2**	IO	BC1825DS	BC1850CS
5	T3	**gpio_2**	IO	BQ0054S	NewCell_BX
12	M7	**usb_txen**	O	OC1825DS	OC1850CS
24	N8	**ckout_13mhz**	O	OC1825DS	OC1825DS_MET
31	R9	**gpio_4**	IO	BQ0055S	NewCell_BX
32	N9	**gpio_5**	IO	BQ0055S	NewCell_BX
33	T10	**usb_boot**	IO	BC1825DS	BC1850CS
112	F12	**tspact_11**	IO	BQ0021S	NewCell_BX
114	H10	**tspact_12**	IO	BQ0021S	NewCell_BX
117	C14	**tspact_13**	IO	BQ0021S	NewCell_BX
118	E12	**tspact_14**	IO	BQ0021S	NewCell_BX
120	G10	**tspact_15**	IO	BQ0021S	NewCell_BX

Pin Number	BGA Address	BGA Name	DIR	IO Cell	IO Cells change proposal ALR
122	F11	**kbr_0**	IO	BQ0055S	NewCell_BX
123	E11	**kbr_1**	IO	BQ0055S	NewCell_BX
124	C12	**kbr_2**	IO	BQ0055S	NewCell_BX
125	H9	**kbr_3**	IO	BQ0055S	NewCell_BX
127	F10	**kbr_4**	IO	BQ0055S	NewCell_BX
128	B12	**kbc_4**	IO	BQ0054S	NewCell_BX
134	E10	**gpio_13**	IO	BQ0055S	NewCell_BX
139	D9	**lcd_rs**	IO	BQ0054S	NewCell_BX
140	B9	**gpio_17**	IO	BQ0054S	NewCell_BX
153	F8	**gpio_19**	IO	BQ0031S.1	BQ442S
154	E7	**gpio_20**	IO	BQ0031S.2	BQ442S
155	A5	**gpio_21**	IO	BQ0031S.1	BQ442S
156	C6	**gpio_22**	IO	BQ0031S.2	BQ442S
157	G9	**gpio_23**	IO	BC1825DSHYPD_wrap	BC1850CSHYPD
158	F7	**gpio_24**	IO	BC1825DSHYPD_wrap	BC1850CSHYPD
159	C5	**gpio_25**	IO	BC1825DSHYPD_wrap	BC1850CSHYPD
160	E6	**gpio_26**	IO	BQ0054S	NewCell_BX
161	G8	**gpio_27**	IO	BQ0054S	NewCell_BX
163	C4	**gpio_28**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
165	G7	**gpio_29**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
166	B3	**gpio_30**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
168	E5	**nd_nwp**	IO	BC1825DSHY	BC1825DS_MET
169	C3	**gpio_31**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
171	B2	**tdo**	O	OQ0028S	NewCell_BX
172	F6	**gpio_32**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
174	H8	**gpio_33**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
175	C2	**gpio_34**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
177	D3	**nd_ce1**	O	OC1825DS	OC1825DS_MET
178	F5	**gpio_35**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
179	D2	**gpio_36**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
180	H7	**gpio_37**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
181	E3	**ncs0**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
182	G6	**gpio_7**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
183	G5	**gpio_39**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
184	F3	**add_21**	IO	BC1825DSHYPD_wrap	BC1825DSHYPD_MET
185	J8	**add_20**	O	OC1825DS	OC1825DS_MET
187	H6	**add_19**	O	OC1825DS	OC1825DS_MET
188	F2	**add_18**	O	OC1825DS	OC1825DS_MET
189	F1	**add_17**	O	OC1825DS	OC1825DS_MET
190	G3	**add_16**	O	OC1825DS	OC1825DS_MET
191	H4	**add_data_15**	IO	BC1825DS	BC1825DS_MET
192	G1	**add_data_14**	IO	BC1825DS	BC1825DS_MET
193	G2	**add_data_13**	IO	BC1825DS	BC1825DS_MET
194	H5	**add_data_12**	IO	BC1825DS	BC1825DS_MET
196	H3	**add_data_11**	IO	BC1825DS	BC1825DS_MET
197	H2	**add_data_10**	IO	BC1825DS	BC1825DS_MET
198	J6	**add_data_9**	IO	BC1825DS	BC1825DS_MET
199	J4	**add_data_8**	IO	BC1825DS	BC1825DS_MET
200	J2	**add_data_7**	IO	BC1825DS	BC1825DS_MET
201	J3	**add_data_6**	IO	BC1825DS	BC1825DS_MET
202	J5	**add_data_5**	IO	BC1825DS	BC1825DS_MET
203	K2	**add_data_4**	IO	BC1825DS	BC1825DS_MET
204	K3	**add_data_3**	IO	BC1825DS	BC1825DS_MET
205	K5	**add_data_2**	IO	BC1825DS	BC1825DS_MET
207	L2	**add_data_1**	IO	BC1825DS	BC1825DS_MET
208	K4	**add_data_0**	IO	BC1825DS	BC1825DS_MET
209	L1	**rnw**	O	OC1825DS	OC1825DS_MET
210	L3	**nbhe**	O	OC1825DS	OC1825DS_MET
211	M2	**nble**	O	OC1825DS	OC1825DS_MET
212	M1	**nmoe**	O	OC1825DS	OC1825DS_MET

Pin Number	BGA Address	BGA Name	DIR	IO Cell	IO Cells change proposal ALR
213	K6	**fdp**	O	OC1825DS	OC1825DS_MET
214	L5	**ncs3**	O	OC1825DS	OC1825DS_MET
216	M3	**nrdy**	IO	BC1850CSHYPU_wrap	BC1825DSHYPU_MET
217	J7	**adv**	IO	BC1850CSHYPU_wrap	BC1825DSHYPU_MET
218	L6	**gpio_42**	IO	BC1825DSHYPU_wrap	BC1825DSHYPU_MET
219	N3	**gpio_43**	IO	BC1825DSHYPU_wrap	BC1850CSHYPU
220	M5	**gpio_44**	IO	BC1825DSHYPU_wrap	BC1850CSHYPU
221	K7	**gpio_45**	IO	BC1825DSHYPU_wrap	BC1850CSHYPU
222	P2	**gpio_46**	IO	BC1825DSHYPU_wrap	BC1850CSHYPU
223	P3	**uart_tx**	O	OC1825DS	OC1850CS
225	L7	**uart_rx**	IO	BC1825DSHYPD_wrap	BC1850CSHYPD
226	R2	**uart_cts**	IO	BC1825DSHYPD_wrap	BC1850CSHYPD
229	R3	**rts_sdirda**	O	OC1825DS	OC1850CS
230	U1	**spare_3**	IO	BC1825DSHYPU_wrap	BC1850CSHYPU

Table 2: List of changed IO cells

ES2.0 IO Cell	IO Cells change
BQ0021S	NewCell_BX
BQ0054S	NewCell_BX
BQ0055S	NewCell_BX
OQ0028S	NewCell_BX
BQ0031S	BQ442S
OC1825DS	OC1850CS
OC1825DS	OC1825DS_MET
BC1825DS/HY/PU/PD	BC1825DS_MET/HY/PU/PD
BC1825DS/HY/PU/PD	BC1850CS/HY/PU/PD

STATUS
Open.
Issue is planned to be fixed in future ES.

2.9 Emulation crash during boot ROM code execution

IMPACT
The issue is only emulation related and has no impact on normal functional mode.
It limits the debug capabilities.

In emulation mode, with Locosto ES2.0 it is not possible to execute ARM code from address 0x00000000.

DESCRIPTION
Emulation tool (Texas Instruments Code Composer Studio or Lauterbach Trace32 for instance) crashes while executing ARM code from reset address 0x00000000.

When executing ARM code from reset address 0x00000000 in emulation mode, a prefetch abort occurs at boot ROM code subroutine execution.

Therefore the only way to run ARM code under emulation tool is to start execution from C-entry point in flash memory (CS3 – Starting address 0x06000000).
That means the boot ROM code is not executed.
In this case, the basic initialization usually performed by boot ROM code is missing.

Therefore it is not possible to insure the same behavior for the embedded software application running under emulation than without emulation as Locosto device basic software initialization will be different from one case to the other one.

WORKAROUND
No.

STATUS
Open.
Issue is planned to be fixed in future ES.

2.10 Camera gated clock mode not supported

IMPACT
Camera "gated clock mode", i.e. pixel clock (*cam_lclk* signal) cut off when the horizontal synchronization line (*cam_hs* signal) is inactive is not supported by Locosto device. This is not part of the camera module specification.
This section is added to errata to highlight this limitation to customers.

DESCRIPTION
During inactive Horizontal synchronization line some camera may gate the pixel clock or not.
The two modes are described as follow:

- "Not gated clock mode": the pixel clock is present even when the horizontal synchronization line (*cam_hs* signal) is inactive
- "Gated clock mode": the pixel clock is cut off (gated) when the horizontal synchronization line (*cam_hs* signal) is inactive

In "gated clock mode", the first 2 pixels of a frame may be lost.

The bit 16 (CC_EN) in CAM_CC_CTRL register of Camera module is internally resynchronized on the "*cam_lclk*" pixel clock before being used to receive data.
Since it takes 2 pixel clock cycles to resynchronize the value from the OCP domain to the pixel clock domain, then the 2 first pixels are lost when the clock is gated and vertical synchronization line (*cam_vs* signal) is not used.

WORKAROUND
No.

STATUS
Open.

2.11 Glitches on EMIF bus

IMPACT
- BTWST bit field of EMIF_CSi register of EMIF shall neither be programmed to '0000b' nor '0001b'.
- RF spurs increased by 5dB.

DESCRIPTION
The BTWST bit field of EMIF_CSi register of EMIF is used to program the Bus Turn-around Wait States inserted during a read-to-write transition.
If the BTWST bit field is '0000b' or '0001b', some glitches may appear on multiplexed DATA_ADD[15:0] bus of the EMIF interface.

The glitches appear after a read transaction whenever there is a change in the direction of the multiplexed DATA_ADD[15:0] bus from input to output.

Due to these glitches RF spurs are increased by up to 5dB.

For BTWST bit field programmed to '0000b' or '0001b', after a read operation, one clock cycle after nCSi going high, the EMIF drives the multiplexed DATA_ADD[15:0] bus with the data read during the read operation.
This is done to prevent bus contention.

For BTWST bit field to '0000b' or '0001b' the change of bus direction as well as the change of data driven by EMIF (with read data) happen in the same clock cycle.
However due to difference in delays between change of bus direction and change of data reaching the multiplexed DATA_ADD[15:0] bus pads, the output buffers of the bus may get enabled before the read data is actually driven on bus.
Due to this there can be some time when instead of the read data being driven on the bus it is the old data driven. And when the real transition from old data to new data occurs it is visible as glitches on multiplexed DATA_ADD[15:0] bus.

For BTWST bit field to '0010b' (decimal value 2), the change of bus direction is driven two clock cycles after nCSi going high while the change of data driven by EMIF (with read data) occurs one clock cycle after nCSi going high.
So the read data being driven on multiplexed DATA_ADD[15:0] bus becomes stable before the bus is actually driven by Locosto EMIF and there are no transitions externally observed on bus.

WORKAROUND
The software workaround consists in programming the BTWST field to value greater than 1.
This provides extra clock cycles to the data driven by Locosto EMIF to settle down before the bus direction is changed.

STATUS
Open.
Issue is planned to be fixed in future ES.

2.12 Key release event miss when using a software long key press detection

IMPACT
The long key press detection can not be implemented by software and the hardware long key press mode of Locosto keypad controller must be used.

DESCRIPTION
If the hardware long key press mode of keypad controller is disabled and the long key press detection is implemented by software, by quickly pressing a key several times, the interrupt matching with the key release event gets missed.

The probability that the issue occurs is increased when increasing the debouncing time.

WORKAROUND
The hardware long key press mode of Locosto keypad controller must be used to manage the long key press detection.

A compromise needs to be done on the debouncing time to apply. More the debouncing time is increased, greater the probability to have an interrupt miss (if there is a press key change during debouncing time)

STATUS
Open.

2.13 RC same configuration not supported for pSRAM

IMPACT
Full-handshaking mode with nRDY asserted at the same time of data phase is not supported for pSRAM write accesses by Locosto device.
This is not part of the EMIF module specification.
This section is added to errata to highlight this limitation to customers.

DESCRIPTION
The pSRAM memory device and Locosto EMIF are both configured in full-handshaking mode with nRDY asserted at the same time. This is done by setting bit 11 (RC) of EMIF_ADV_CSi register to '1' for Locosto EMIF.
Then a synchronous write access to pSRAM should follow the full-handshaking mode with nRDY asserted at the same time.
However irrespective of RC bit programming the Locosto EMIF will follow full-handshaking mode with nRDY asserted one cycle before the data phase, causing a data read misalignment.

WORKAROUND
Set RC bit to '0' (nRDY signal is asserted one cylcle before the data phase) for memory supported both mode (nRDY asserted at the same time or one cycle before the data phase).

STATUS
Open.

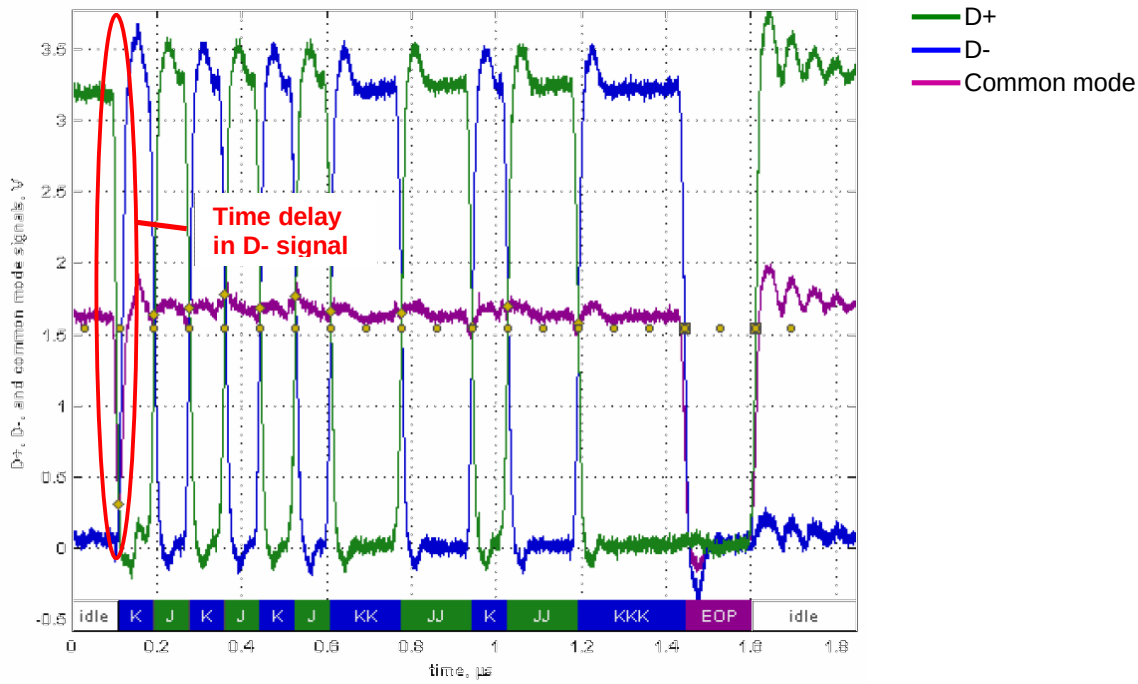
2.14 USB synchronization bit violation

IMPACT
USB synchronization bit violation during USB certification.
Test house waives the bit violation as it is only due to the first synchronization bit, repeated 5 times at the beginning of each packet.
This section is added to errata to highlight this system limitation to customers.
This is not a Locosto device limitation but a Triton Lite limitation.

DESCRIPTION
During the first synchronization bit of packet, there is a time delay in USB D- signal. D+ signal goes down before D- goes high causing a bit violation.

Figure 5 shows the USB first synchronization bit violation.

Figure 5: USB synchronization bit violation



WORKAROUND
No.
Test house waiver granted – “first bit exception invoked”.

STATUS
Open.

2.15 DMA transfer does not work if destination and source addresses are not burst aligned.

IMPACT
DMA transfer does not work if burst mode is enabled on both source and destination ports.

DESCRIPTION
DMA does not complete the transfer if burst mode is enabled on both source and destination ports. It will cause a deadlock. The root causes is the handling of the read and write of the FIFO in the DMA.

WORKAROUND
The WA consists to set both the destination and source addresses burst aligned (4 * 32 bits).

STATUS
Open.

2.16 CDO pin of CPORT module cannot be set in high-Z impedance

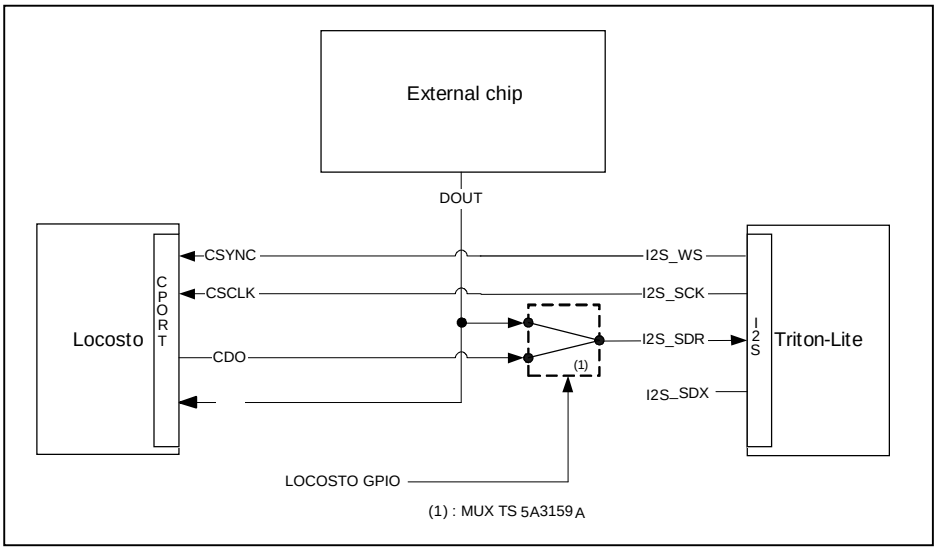
IMPACT
Contention could occur on I2S_SDR pad of Triton-Lite if an external device is connected to this pin while CDO pin of Locosto is already connected to I2S_SDR pin.

DESCRIPTION
Setting bit 6 of CPORT_CPCFR3 register to “1” cannot configure CDO pin in high-Z impedance.

WORKAROUND

The WA consists to add an external multiplexer (e.g. TS5A3159A) on I2S_SDR line.

Figure 6 Multiplexer between CDO and I2S_SDR line



STATUS
Open.

2.17 Bridge sleep requests remains asserted after wakeup from UART.

IMPACT
Bridge clock cannot switch on from UART wakeup while the system is in deep sleep mode

DESCRIPTION

Bridge clock FSM does not come out of sleep state when wakeup request comes. Bridge sleep request signal is not de-asserted so the idle request to UART remains asserted.

WORKAROUND

The software workaround consists to enable UART_SWAKEUP Interrupt (IRQ 17).
By enabling this interrupt, ARM comes out of sleep and bridge clock state machine moves from the sleep state to wakeup state.

STATUS

Open

3. LOCOSTO Processor Enhancements Description

This enhancement section summarized changes or new features which have been added to a LOCOSTO revision to enhance its capabilities compare to previous revisions.

3.1 SIM_PWRDN bit: CONF_LCD_CAM_ND register mapping

ADVANTAGE
Prevent current leakage between VREXTL (Locosto core power supply) and VRSIM when VRSIM is OFF.

DESCRIPTION
Bit 2 (SIM_PWRDN) of CONF_LCD_CAM_ND register of Configuration module has been added to prevent current leakage between VREXTL (Locosto core power supply) and VRSIM when VRSIM is OFF.
The bit 2 (SIM_PWRDN) must be set to 1 when VRSIM is OFF.
Refer to register CONF_LCD_CAM_ND register in Locosto TRM.

ENHANCED REVISION
ES2.0.

3.2 FORCE_KBC bit: FORCE_KBC register mapping

ADVANTAGE
Allow to configure keypad KBC[4:0] input pads either in Tristate or at high level.

DESCRIPTION
Bit 0 (FORCE_KBC) of CONF_FORCE_KBC register of Configuration module has been added to allow configuring keypad KBC[4:0] output pads either in Tristate or at high level when keyboard is in suspend mode.

This bit is used by the workaround of issue 1.4 Keyboard / XTAL interaction.

Refer to register CONF_FORCE_KBC register in Locosto TRM.

ENHANCED REVISION
ES2.0.

3.3 Internal pull-down on VCLKRX

ADVANTAGE
Power management. Deep sleep current consumption reduction.

DESCRIPTION
A programmable internal pull-down was added on VCLKRX input pad to avoid it floating when not driven by Triton Lite in case of voice path not activated.
Refer to register CONF_VCLKRX register in Locosto TRM for details on pull-down control.

ENHANCED REVISION
ES2.0.