TEXAS INSTRUMENTS

I-Sample

TCS2300

Hardware User's Guide

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Read This First

About This Manual

The purpose of this user's guide is to give the reader an overview of the I-Sample reference design hardware. This includes descriptions of functional circuits and how they are interfaced with each other. Furthermore, a description of how to configure the onboard dipswitches can also be found in this user's guide.

Prerequisites: Basic knowledge about digital circuits.

How to Use This Manual

The intention with this manual is to provide information about the I-Sample board and its subcomponents. It is therefore not a requirement that the manual is read from start to end. This manual can be used as a dictionary where the individual components can be looked up.

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This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

WARNING

Related Documentation from Texas Instruments

- LoCosto Basic User Manual (BUM)
- Triton/Triton Lite TWL3029/TWL3031 Datasheet
- RF7115 Datasheet
- BRF6150 Island 2 Datasheet
- I-Sample Schematics
- 13_01_03_02387_bls_0003_audio.doc
- 13_01_03_02378_bls_0010_usb.doc
- TCS2300 GSM/GPRS Chipset Reference Design Quick Start Guide

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Contents

Figures

Tables

Chapter 1

Introduction

The purpose of the I-Sample reference design is to provide customers with a complete hardware solution intended for wireless applications.

1.1 I-Sample

I-Sample is a cellular reference design including TI's LoCosto highly integrated System-On-Chip (SOC) for wireless pocket information devices that combine both voice and data. In Figure 1-1 is shown a top view of the I-Sample board.

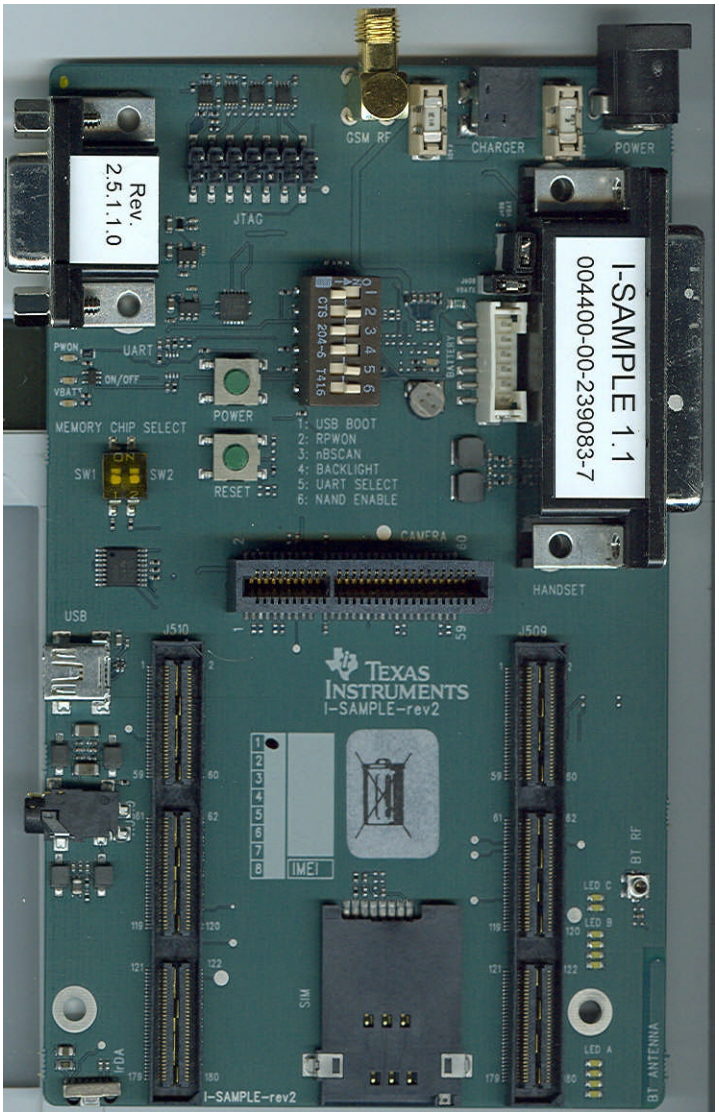


Figure 1-1. I-Sample board.

1.2 I-Sample Board Features

The I-Sample Board is supplied with the following features:

- Processor Circuitry
  - LoCosto™ Digital Baseband Processor with DRP 2 Technology
- Onboard Memory

- MCP: 16 MB (128 Mbit) NOR Flash + 8 MB (64 Mbit) CRAM
- 16 MB (128 Mbit) 16 bit CRAM (I-Sample 1.1 and 2.0+ only)
- 64 MB (512 Mbit) 8-bit NAND Flash

- IrDA
  - SIR support (115 kb/s)
  - MIR support (1.152 Mbit/s)
  - FIR support (4.0 Mbit/s)
- USB
  - On board transceiver
  - Mini AB USB connector on I-Sample 1.0 and 1.1. Mini B USB connector on I-Sample 2.0
- Bluetooth
  - Island 2 Bluetooth Transceiver (BRF6150)
  - Onboard antenna
- Analog BaseBand/Power Management
  - Triton (TWL3029) analog baseband on I-Sample 1.0 and 1.1. Triton Lite (TWL3031) analog baseband on I-Sample 2.0
  - Battery connector
  - Onboard crystal for 32.768 KHz RTC
  - Backup battery for RTC
  - Power-On/Reset Circuitry
- Quad band GSM/GPRS modem
  - Digital Radio Processor 2 technology build into LoCosto
  - Quad-band transmit module (RF7115)
  - Supported GSM bands: 850, 900, 1800, and 1900 MHz
- SIM slot (1.8/3 V)
- Handset
  - 2.2” Colour TFT LCD 16-bit (65.536 colours)
  - 25 + 1 key keypad
  - 8 Ohm speaker and microphone
- Audio
  - 2.5 mm 4 pin audio jack for stereo headset
- Debug
  - On-board JTAG connector

- Most signals routed to expansion connecters which allows probing with the use of a VISU board

Chapter 2

I-Sample Reference Design

2.1 Architecture

The architecture of the I-Sample reference board is shown in the block diagram of Figure 2-2. Each of the blocks shown in this diagram will be described in the following sections of this document. On I-Sample 1.0 and 1.1 the analog baseband device that is used is the Triton. On I-Sample 2.0 and later the Triton is substituted with the Triton Lite. Due to the similarities between the Triton and the Triton Lite, the I-Sample ABB will through out this hardware User's guide be referred to as Triton/Triton Lite.

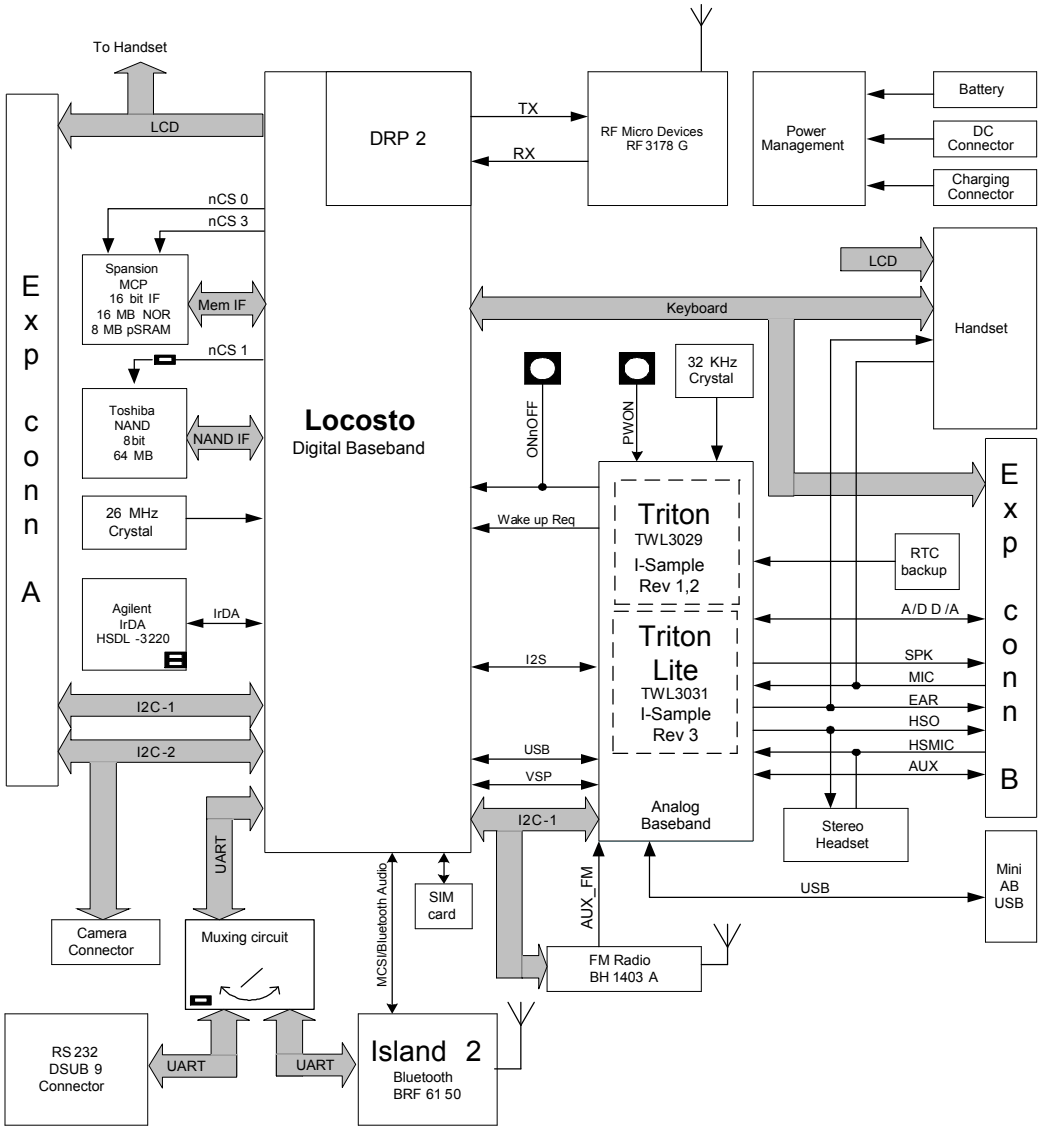


Figure 2-2. I-Sample board architecture.

2.2 Power Supply and Voltage Regulation

The I-Sample board consists of many modules that operate at different voltages. The different power domains are derived from the main supply voltage by the use of LDOs and fed to the individual modules. The main supply voltage can be applied from either the DC power jack (see Section 2.2.3) or the battery (see Section 2.2.4). A description of the different modules and corresponding power domains that are connected to which modules can be found in Section 2.2.2. In the next section a block diagram of the I-Sample power grid is shown.

2.2.1 Power Grid

Figure 2-3 provides an overview of the I-Sample power grid.

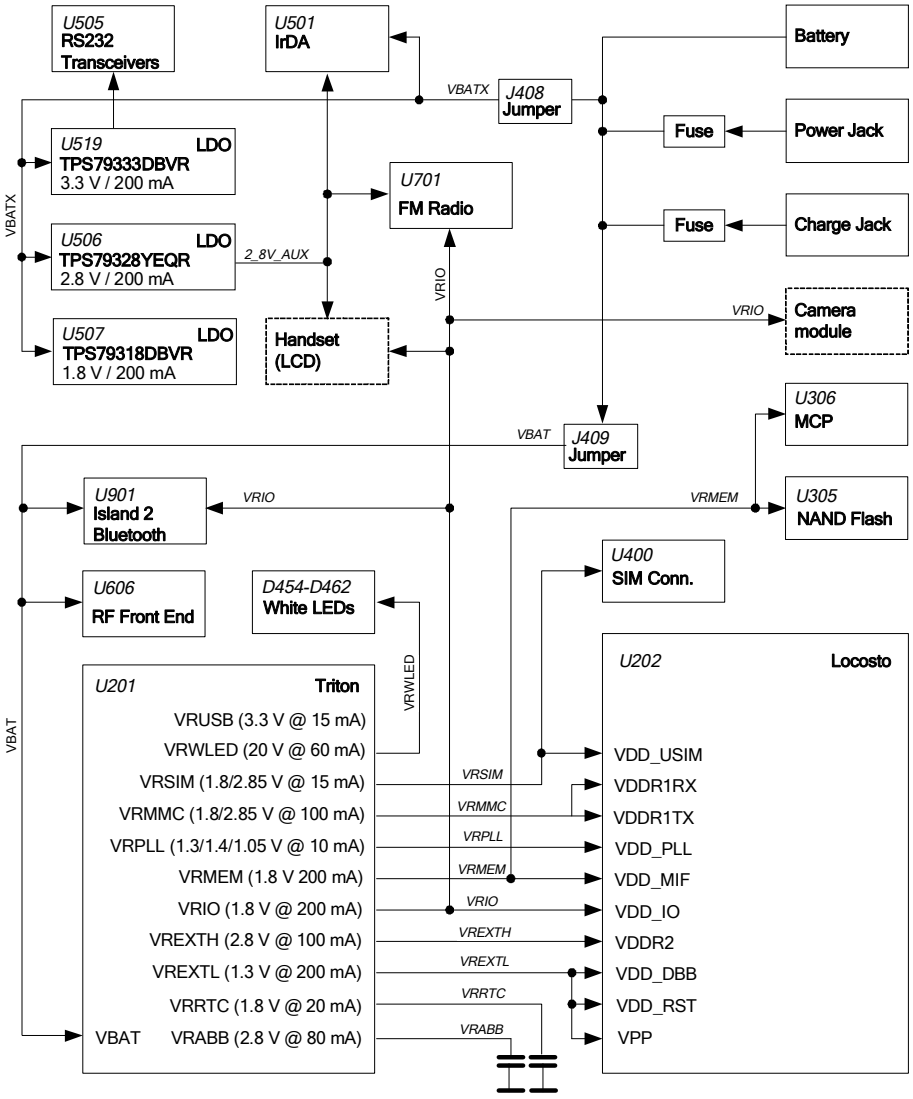


Figure 2-3. I-Sample power grid.

2.2.2 Power Domains

In this section a description of the individual power domains can be found. The names of the power domains are visually represented in Figure 2-3 as nets.

2.2.2.1 VBAT

VBAT is the main power rail supplied directly from the battery or the external power connector. This power domain supplies all the peripheral units that are considered a part of the main reference design. It is possible to disconnect this power domain by removing jumper J409.

By connecting an ampere meter across the J409 jumper terminals the current consumption for the VBAT power domain can be measured.

2.2.2.2 VBATX

VBATX is a power domain that supplies peripheral units that are not part of the reference design. This power domain is supplied directly from the battery or the

external power connector. It is possible to bypass this power domain by removing the jumper J408.

2.2.2.3 VRABB

The VRABB supply domain is provided by a 2.8 V LDO build into the Triton/Triton Lite analog baseband. This LDO is able to source 80 mA where 50 mA is consumed internally by the Triton/Triton Lite itself. The VRABB is not connected to any other peripheral units.

2.2.2.4 VREXTL

The VREXTL supply domain is sourced by a highly configurable LDO located in the Triton/Triton Lite. The LDO is able to source 200 mA at 1.3/1.05 V and 100 mA at 1.8/2.8 V. This power domain supplies the core circuitry on the LoCosto processor which is expected to consume around 140 mA.

2.2.2.5 VREXTH

On the Triton/Triton Lite another highly configurable LDO can be found which is denoted VREXTH. This supply is able to source 200 mA at 1.8 V and 100 mA at 2.8 V. This power domain is used to drive the DRP circuitry located onboard the LoCosto.

2.2.2.6 VRMMC

The VRMMC is another power domain derived from an LDO onboard the Triton/Triton Lite. The supply is able to deliver 100 mA at either 1.8 or 2.85 V and is part of powering the DRP/APC circuitry onboard the LoCosto. The DRP is expected to consume 60 mA and the APC 6 mA.

2.2.2.7 VRSIM

The onboard Triton/Triton Lite VRSIM power domain is used to drive both the USIM interface located onboard the LoCosto processor and power a SIM card inserted into the SIM connector. The power domain supports both 1.8 and 2.8 V SIM cards and is able to source a total of 15 mA. Both SIM card and SIM interface is not expected to consume more than 3 mA.

2.2.2.8 VRRTC

The VRRTC is sourced from another LDO located on the Triton/Triton Lite. This LDO is able to deliver 20 mA at 1.8 V where approximately 10 mA is consumed by the RTC circuitry inside the Triton/Triton Lite. This power domain is not connected to any other peripherals.

2.2.2.9 VRIO

The LDO that drives the VRIO power domain can be found on the Triton/Triton Lite. This LDO delivers 200 mA at 1.8 V and powers the digital circuitry on the FM Radio, the Bluetooth, the LCD, and the camera module.

2.2.2.10 VRMEM

The VRMEM power domain has been provided as means of powering all memory related peripherals. The LDO that powers this domain is located on the Triton/Triton Lite and is able to source 200 mA at 1.8 V. The VRMEM domain is powering the MCP and NAND flash memory modules.

2.2.2.11 VRPLL

The Phase Locked Loop (PLL) circuitry on the LoCosto processor is powered by the VRPLL which is a power domain sourced by an LDO onboard the Triton/Triton Lite. This particular LDO is able to operate at 1.05, 1.3, and 1.4 V delivering 10 mA. The PLL on the LoCosto is not expected to consume more than 1.5 mA.

2.2.2.12 1_8V_AUX

The 1_8V_AUX domain is powered by a 1.8 V external LDO which is able to source 200 mA. The LDO is the Texas Instruments TPS79318DBVR and is used to power different kinds of glue logic such as level converters and the likes. This LDO is not considered a part of the reference design.

2.2.2.13 2_8V_AUX

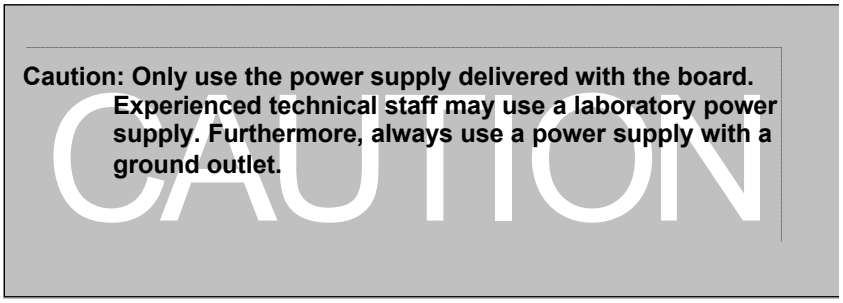
The 2_8V_AUX domain supplies the analog parts of the FM Radio and the camera module and the digital circuitry of the IrDA module. This domain is powered by an external 2.8 V LDO which is a Texas Instruments TPS79328YEQR capable of delivering 200 mA. This LDO is not considered a part of the reference design.

2.2.2.14 3_3V_AUX

The RS232 and JTAG level shifting circuitry is powered by the 3_3V_AUX supply domain. This supply domain is sourced by the Texas Instruments TPS79333DBVR which is an external 3.3 V LDO capable of supplying 200 mA.

2.2.3 DC Main Power Connector

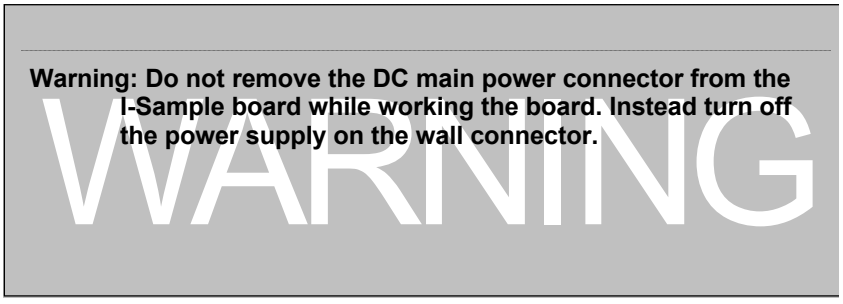
The I-Sample board is powered through the main DC jack connector J481 which is protected by fuse F402.



Using a laboratory power supply the recommended specifications are:

- Output voltage between 3.8 V and 4.2 V
- Must be able to deliver peak currents in excess of 2 A

When the power supply is connected, the pass-through connection on connector J481 (pin 3) disconnects the ground-path to the battery in case the battery is also connected (J483). See schematic for details.



Refer to Section 2.2.5 for information regarding spare fuses.

2.2.4 Battery Connector

Once the I-Sample reference board has been built into a handset the main power supply will be provided by a battery. A battery will not be supplied with the I-Sample as default. However, a battery pack can be ordered. A description of the battery pack can be found in section 4.3**.**

The battery is connected to the I-Sample through the battery connector J483. The individual pins are described In Table 2-1.

Table 2-1. Pin description of the J421 battery connector.

Pin #	Pin Name	Description
1	+BAT	Positive battery terminal
2	+BAT	Positive battery terminal
3	ADCIN5	TBD
4	ADCIN4	TBD
5	GND	Negative battery terminal
6	GND	Negative battery terminal

2.2.5 Fuses

To protect the I-Sample from hazardous power levels fuses have been attached in series with both the DC barrel connector (F481) and the charge barrel connector (F482). In Table 2-2 is provided information about the fuses and how to acquire new ones.

Table 2-2. Information about the fuses F400 and F401.

Fuse	Type	Manufacturer / Order code	European Distributor
F481	1.5 A slowblow nanofuse	Littlefuse / R452 01.5	Farnell (Catalog no. 664-730)
F482	1 A Quickblow nanofuse	Littlefuse / R451 001	Farnell (Catalog no. 508-690)

2.2.6 Jumpers

In order to be able to measure the power consumption in conditions that are related to what is expected from the end product, jumpers have been provided to separate non essential functionality from essential on the I-Sample board. These jumpers together with their descriptions can be found in Table 2-3.

Table 2-3. Jumper description.

Jumper	Description
J408	By removing the jumper placed over J408 and then attach an Ampere meter across the pin header it is possible to measure the total current consumption from the VBATX supply domain.
J409	By removing the jumper placed over J409 and then attaching an Ampere meter across the pin header it is possible to measure the total current consumption from the VBAT supply domain.

2.3 Clock Overview

On the I-Sample board two crystals are used for generating the needed reference frequencies. These are:

- A 26 MHz crystal
- A 32.768 Hz crystal

These together with the peripherals that make use of them are shown in Figure 2-4.

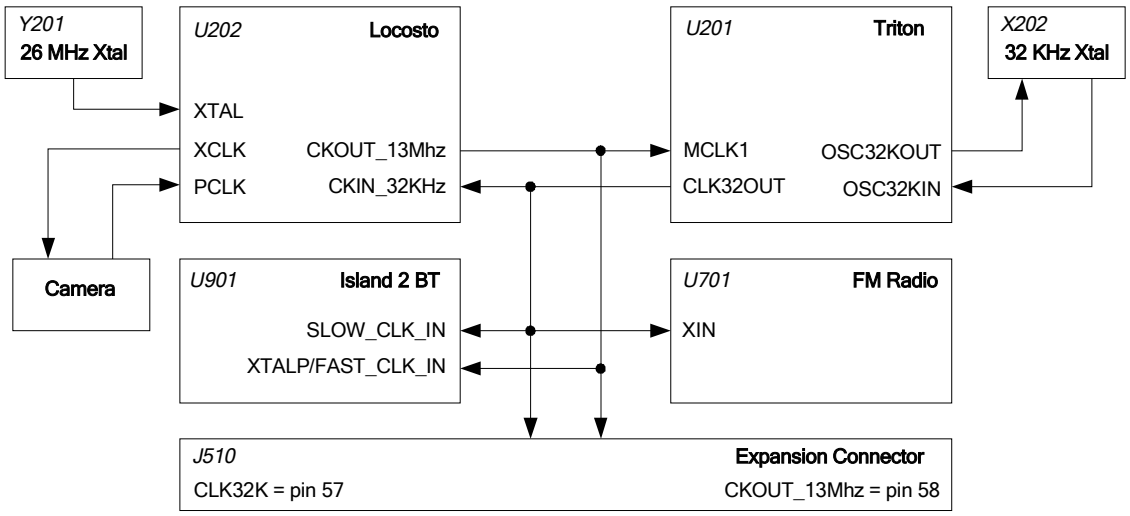


Figure 2-4. Connection of the 26 MHz and the 32.768 kHz clocks.

2.3.1 26 MHz Circuitry

The 13 Mhz reference clock is derived from a 26 MHz crystal connected to the LoCosto. The 26 MHz oscillating signal is divided by two inside the LoCosto in order to produce a 13 MHz square signal. The external 26 MHz crystal has a frequency tolerance of +/- 10 ppm.

The 13 MHz clock signal is used to drive the fast clock inputs on the Island 2 Bluetooth device and the Triton/Triton Lite. Furthermore, the 13 MHz clock is driving the XCLK output on the LoCosto processor which is used to supply the camera with a permanent clock. This clock is returned from the camera in the form of a pixel clock (PCLK).

2.3.2 32 KHz RealTime Clock (RTC)

I-Sample has a 32.768 KHz crystal oscillator that is connected to Triton/Triton Lite. This clock signal is used by Triton/Triton Lite and LoCosto during power on, low power and sleep modes, instead of the main 26 Mhz to reduce current consumption.

The 32.768 KHz crystal oscillator is also used as the RTC block clock input to Triton. The external crystal has a frequency tolerance of +/- 20 ppm (max) and calibration and compensation for the RTC is handled internally by Triton.

The RTC block within Triton/Triton Lite has the following basic functions:-

- Time information (seconds/minutes/hours) directly in BCD code
- Calendar Information (Day/Month/Year/ Day of the week) directly in BCD code up to year 2099
- Interrupts generation, periodically (1s / 1m / 1h / 1d period) or at a precise time of the day (alarm function)
- 30 s time correction
- oscillator frequency calibration

The clock is operational immediately after the battery has been connected to the system and the Triton/Triton Lite's internal 1.8 V LDO (VRRTC) has stabilized.

2.4 LoCosto Digital Baseband Processor

The LoCosto is the digital baseband processor implemented on the I-Sample board. The LoCosto is designed to run with the Nucleus operating system. A block diagram of the internal functionality can be found in Figure 2-5.

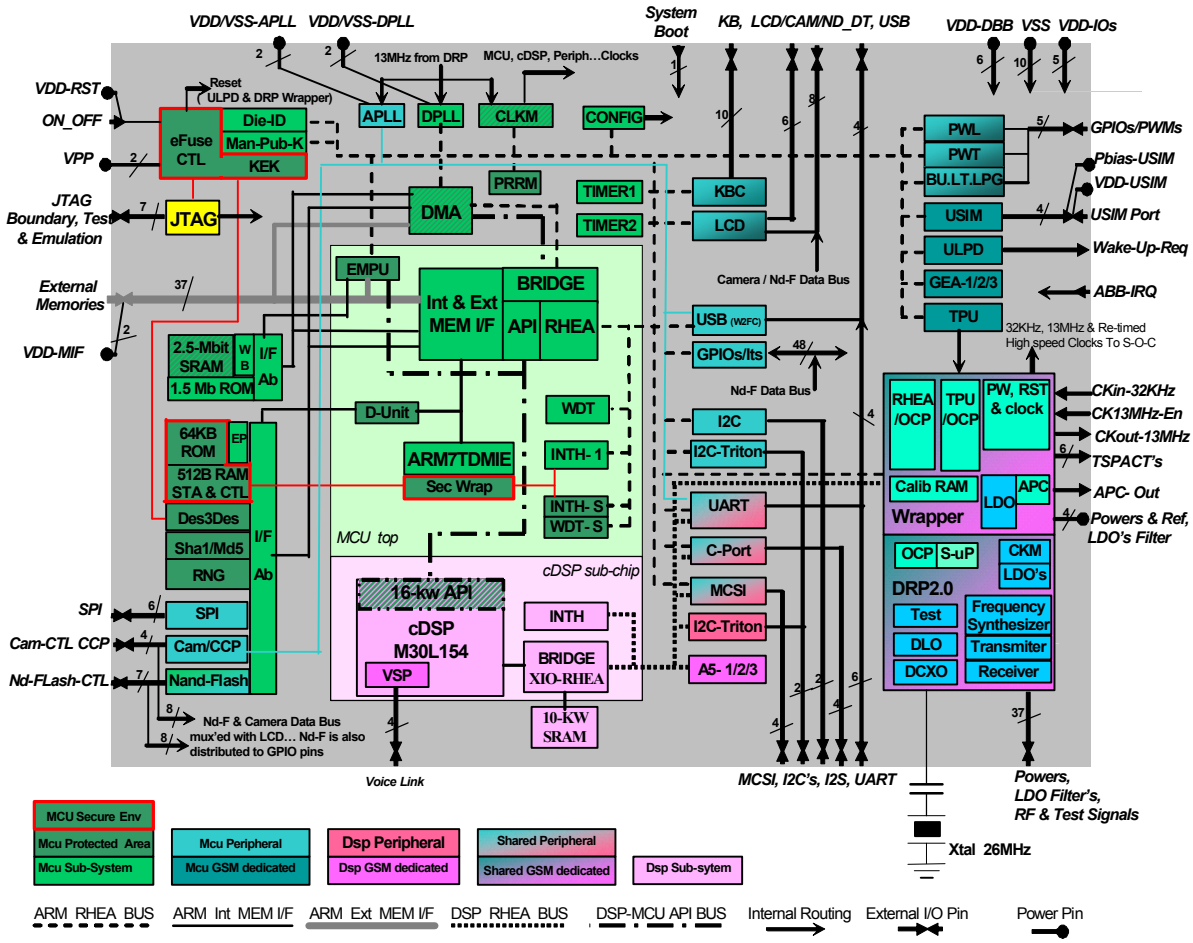


Figure 2-5. Architecture of the LoCosto digital baseband processor.

The LoCosto Integrated Circuit (IC) is a Digital Baseband (DBB) processor, cDSP/ARM7 @ 104 MHz, merged with the Digital Radio Processor 2 (DRP2). The core runs at 1.3 V nominal while the interface is specified at 1.8 V nominal (except USIM, DRP, and APC I/O's).

The DBB supports the processing of GSM radio signals in switching circuit mode and packet data mode (GPRS) for up to class 12, including evolution such as SAIC and Assisted Global Positioning System (A-GPS) in compliance with the ETSI specification. In addition the DBB can process, in a secure environment, messaging and multimedia services such as EMS/MMS, WAP.browsing, Audio-player decoding (MP3, WMP, etc.), camera functions, JAVA based downloaded applications.

The TCR 3.2 software layer that controls the radio function as well as applications is based on and includes all features of TCR 3.1 plus additional specific components.

The LoCosto core functionality is based on the Calypso-Plus device which means that the computing performances as well as the security levels have been maintained. However, system connectivity has been downgraded in order to reflect the LoCosto's primary mission: Low cost component (yet high processing capability) for the mass marked.

Comparing the LoCosto Processor with the Calypso Plus a reduced and repartioned memory system has been embedded.

2.5 Triton/Triton Lite Analog Baseband

The analog baseband that is used on the I-Sample reference design 1.0 and 1.1 is the TWL3029 which is also known as the Triton. On I-Sample 2.0 and later the analog baseband is substituted with Triton Lite (TWL3031).

The Triton/Triton Lite are integrated power management ICs specifically designed for integration with Neptune or LoCosto, providing all the required power supplies and management functions. Power supplies are delivered through 11 LDOs and 3 biases to the digital baseband and the interfaces (memories, PLL, IO, RTC, SIM, MMC, VBUS, USB, LED, and RF). Power management functions include dynamic voltage scaling, state machine control, modem power-up and power management sharing (power management port). System management is done through an I²C serial interface, allowing host (LoCosto) to access the IC configuration registers, and the ability to interrupt the host. Voice and audio capabilities are controlled through both an I²S and a VSP serial interface, and include microphone, headset microphone, FM radio inputs, earplug, analog/digital speakers, and headset amplifier outputs. Additional hook detection input and auxiliary audio output are possible. Transceiver/driver functions include SIM detection, USB/UART interface, 3 White LED drivers and vibrator driver. Housekeeping functions are done through an A/D converter where the analog input is connected to 10 multiplexed ports (5 external and 5 internal). The Triton/Triton Lite provide also RTC functions, JTAG test, and a complete battery charger and control interface.

An overview of the Triton/Triton Lite analog baseband is shown in Figure 2-6.

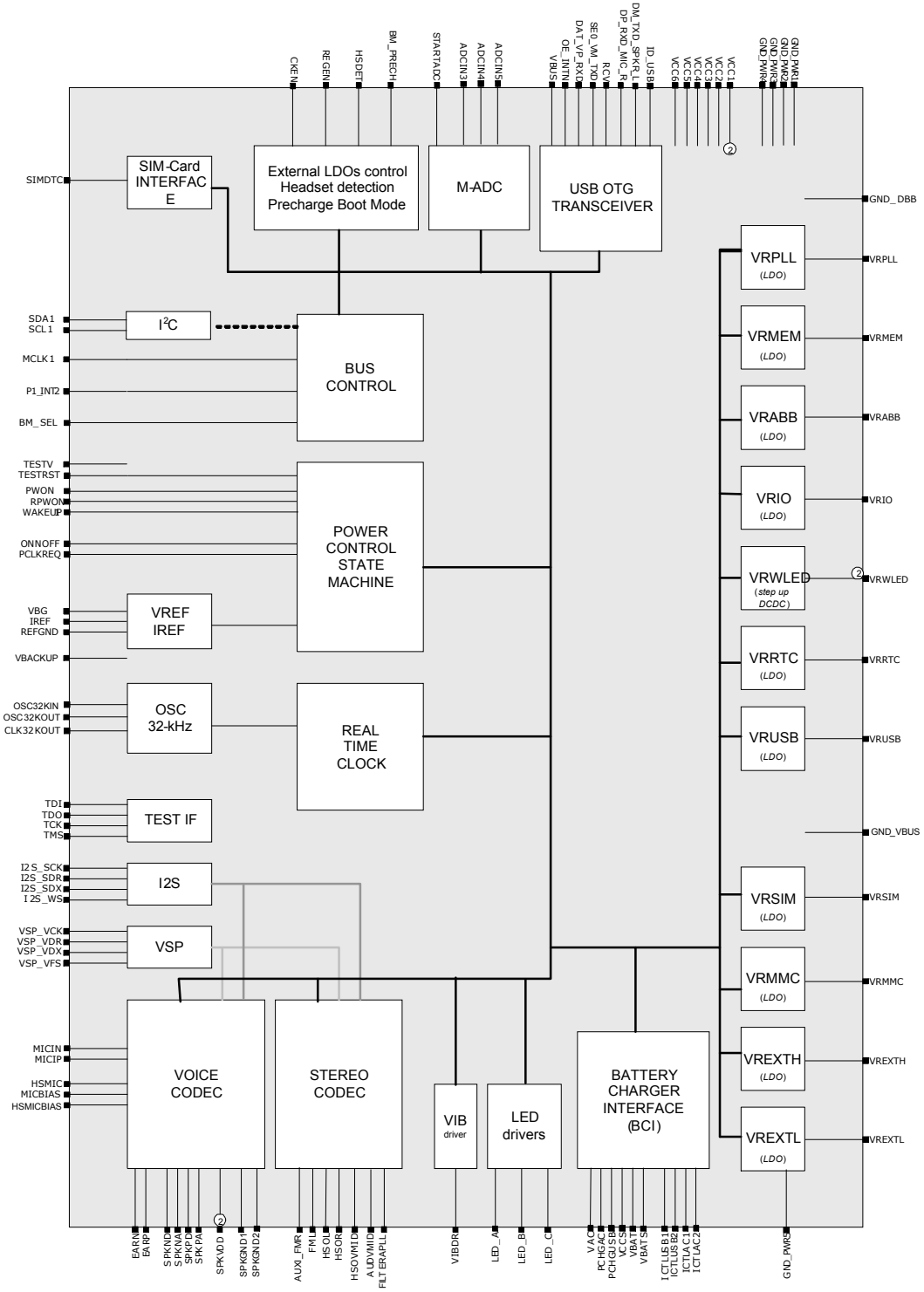


Figure 2-6. Overview of the Triton/Triton Lite ABB.

2.5.1 Power Management

It is the Triton/Triton Lite that handles most of the power management tasks on the I-Sample. Eleven LDOs have been built into the Triton/Triton Lite in order to power most of the peripheral units on the I-Sample board. In the table below is listed info on each of the Triton/Triton Lite LDOs.

Table 4 Overview of the Triton/Triton Lite power supplies

Supply Name	Description	Input	Voltage	Current Capability	Type	Connected to…
VRDBB	Programmable step-down DC-DC converter supplying (0.95 V to 1.4 V, 30 mV steps) the core of the digital baseband counterpart. The main battery directly supplies the VRDBB converter. The VRDBB converter is only available on Triton, not Triton Lite.	VCC1	0.95 to 1.4 V (30 mV steps)	850 mA	DCDC	Exp. Conn.
VRPLL	Low Dropout linear voltage regulator supplying (1.05 V, 1.3 V) the ADPLL, the APLL and the slicer of the digital baseband counterpart. The main battery directly supplies the VRPLL regulator.	VCC1	1.05 V / 1.3 V	10 mA	LDO	VDD_PLL
VRMEM	Low Dropout linear voltage regulator supplying (1.8 V) external SRAM memories (Static RAM), the digital baseband memory interface I/Os and the external memories (Flash RAM, core and interface I/Os) used in the system. The main battery directly supplies the VRMEM regulator.	VCC2	1.8 V	200 mA	LDO	VDD_MIF memory VCC/VDD
VRIO	Low Dropout linear voltage regulator supplying (1.8 V) to the I/Os of the system (Triton/Triton Lite and digital baseband counterpart) and the Triton/Triton Lite digital core. The main battery directly supplies the VRIO regulator.	VCC2	1.8 V	200 mA	LDO	Digital domains on peripherals
VRSIM	Programmable Low Dropout linear voltage regulator supplying (1.8 V, 2.8 V) the SIM card and the SIM card driver. The main battery directly supplies the VRUSIM regulator.	VCC3	1.8 V / 2.85 V	15 mA	LDO	VDD_USIM SIM Conn.
VRABB	Low Dropout linear voltage regulator supplying (2.8 V) the Triton/Triton Lite's analog core. The main battery directly supplies the VRABB regulator.	VCC3	2.8 V	80 mA	LDO	Exp. Conn.
VRVBUS	Step-up DC-DC converter (DCDC) supplying (5.0 V) the VBUS. The main battery directly supplies the VRVBUS converter.	VCC3	5 V	60 mA	DCDC	Exp. Conn.
VRUSB	Low Dropout linear voltage regulator supplying (3.3 V) the Triton/Triton Lite's USB transceiver. The VRVBUS voltage regulator directly supplies the VRUSB regulator (through VRVBUS terminal). An auto-detect circuitry allows an auto-start of the regulator and update a status register bit, when an USB insertion occurs.	VRVBUS	3.3 V	15 mA	LDO	USB interface
VRRTC	Programmable Low Dropout linear voltage regulator supplying (1.8 V) the embedded real time clock (32 KHz oscillator) and dedicated I/O's of the digital baseband counterpart. VRRTC is also the supply voltage of the power management digital state machine. The VRRTC regulator is supplied from the UPR line, switched on the main or backup battery, depending of the system state. VRRTC is always ON, as long as a valid energy source is present.	UPR	1.8 V	20 mA	LDO	No external connection
VREXTH	Programmable Low Dropout linear voltage regulator supplying (2.8 V, 1.8 V) an external peripheral. The main battery directly supplies the VREXTH regulator.	VCC4	2.8 V / 1.8 V	100 mA @ 2.8 V 200 mA @ 1.8 V	LDO	VDDR2 APC_VDD

Supply Name	Description	Input	Voltage	Current Capability	Type	Connected to…
VREXTL	Programmable Low Dropout linear voltage regulator supplying digital baseband The main battery directly supplies the VREXTL regulator.	VCC5	1.8 V / 2.8 V 1.05 V / 1.3 V	100 mA @ >1.3 V 200 mA @ 1.3 V	LDO	VDD_DBB VDD_RST VPP
VRMMC	Programmable Low Dropout linear voltage regulator supplying (1.8 V, 2.85 V) LoCosto DRP The main battery directly supplies the VRMMC regulator.	VCC5	1.8V / 2.85 V	100 mA	LDO	VDDR1RX VDDR1TX1

2.5.2 Battery Charging

Only use the charger delivered with the board. Experienced technical staff may use a laboratory power supply.

CAUTION

When the battery is connected to the I-Sample board (connector J483) it is charged through the charge jack connector J482 (The center-pin is positive). This connector is protected by a 1 A quickblow fuse. Recommended specifications for laboratory power supplies for charging are:

- Output voltage between 4.5 V and 6.5 V
- Must be current limited at 0.7 A

2.5.2.1 DC Charger

The Triton/Triton Lite includes a Battery Charging Interface (BCI). The main function of the BCI is to control the charging procedure of 1-cell Li-Ion, Li-Ion Polymer, or 3-series Ni-MH cell batteries. It supports both regulated and non-regulated chargers of up to 20 V and is able to charge from a USB host (USB charging components not currently added) or a car kit. The BCI is able to charge in linear or pulsed mode.

The battery is monitored using the 10–bit ADC converter from the MADC to measure the battery voltage, battery temperature, battery type, battery charge current, and battery charger input.

The magnitude of the charging current is set by 8 bits of a programming register converted by an 8 bit DAC, whose output sets the reference input of the charging current control loop. The magnitude of the charging voltage is set by 10 bits of a programming register converted by a 10 bit DAC, whose output sets the reference input of the charging voltage control loop.

The BCI also performs some auxiliary functions. These functions are accessory device supply, battery pre-charge with chargers, battery pre-charge with car kits, battery over temperature detection (positive or negative thermistor supported), battery over voltage detection, battery end of charge current detection, and backup battery charge.

2.5.2.2 Battery Temperature

Battery monitoring is performed by the multiplexed 10 channel 10 bit ADC MADC used to measure the battery voltage, battery temperature, battery type, battery charge current, battery charger input voltage and the backup battery voltage. The signals are converted into digital 10 bit words, stored in auxiliary ADC output registers and transmitted to an external µC via the USP interface.

Battery charging current is sensed using a 220 mOhm external resistor connected across terminals VCCS and VBATS of the Triton/Triton Lite device. The battery voltage value is measure using the VBAT terminal of the TWL3031 device.

Pin 3 of the battery connector (J483) allows the connection of an NTC in the battery pack.

2.5.2.3 Battery Identification

In order to identify which battery that has been connected to the battery connector (J483) a battery identification resistor must be placed inside the battery package and then connected to pin 4 of J483. This pin is then connected to the Triton/Triton Lite ADCIN4 input which measures the voltage level of the signal. This value can then be compared with a known value in software. There is currently no convention for which resistor that belongs to which battery technology.

2.5.3 Audio Codec

Comprehensive audio conversion/processing functionality is built into the Triton/Triton Lite in the form of an audio codec.

The Audio Codec (AUC) consists of a voice codec dedicated to GSM application and an audio stereo line. The Voice Codec circuit processes analog audio components in the uplink path and transmits the converted data to the DSP speech coder through the voice serial port (VSP). In the downlink path, the Voice Codec converts the digital samples of speech data received from the DSP via the VSP port into analog audio signals. The Voice Codec supports an 8 kHz (default narrowband mode) or a 16 kHz (wideband mode) sampling frequency. A block diagram of the entire Triton/Triton Lite audio system is shown in Figure 2-7.

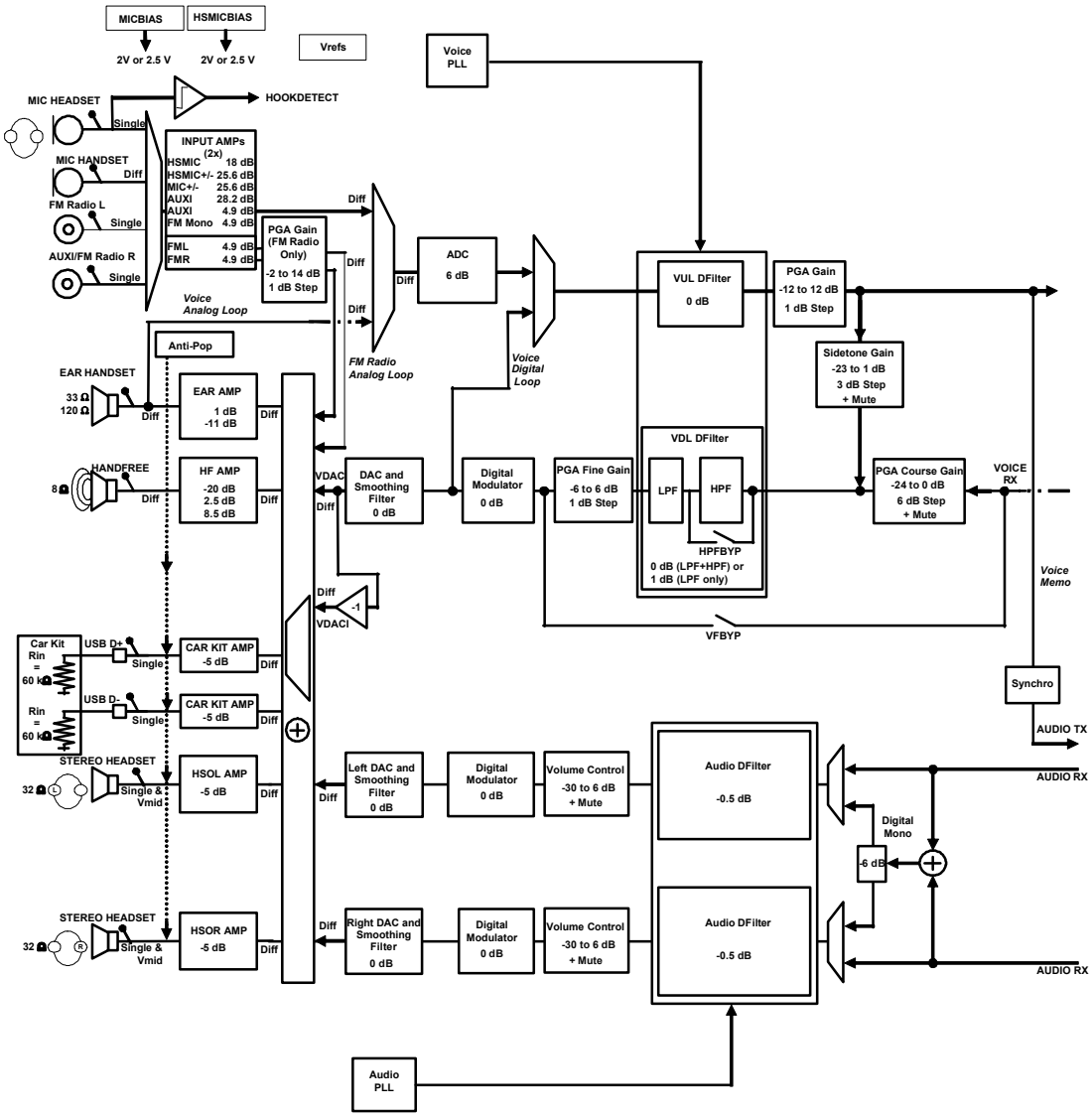


Figure 2-7. Block diagram of the Triton/Triton Lite audio functionality.

The AUC includes the necessary filters, input amplifiers for microphone (headset, phone, auxiliary) and output amplifiers (stereo/mono head set, phone speaker, 8 Ohm speaker, auxiliary).

The AUC also performs the programmable gain, volume control, and side-tone functions for the uplink and downlink path of the voice codec. A common programmable gain and two independent volume controls are available for the right and left channels of the stereo path.

For details concerning the handset pin connections please refer to either section 4.1.3 or the schematic. A more detailed description of the Triton/Triton Lite audio codec/functionality can be found in: "13_01_03_02387_bls_0003_audio.doc".

2.6 Reset and Power-On Circuitry

The Triton/Triton Lite is one of the main components in the power-on and reset circuitry. At battery plug-in the Triton/Triton Lite power-on and reset circuitry generates a reset signal to the internal power control state machine and enables the 32 KHz oscillator.

After Power-On and Reset sequence, the power control state machine maintains a reset condition for the other blocks within Triton/Triton Lite and for external use.

During this state, the control state machine is able to detect and process a switch-on condition from an external event. This external event is generated by pressing the PWON button (S431). The PWON signal is maintained low and will be released to high once switch-on sequence has been completed. As the final step of the Triton/Triton Lite switch-on sequence the output signal ONnOFF is asserted (active high) and this signal is used to switch on the LoCosto DBB.

The connection of the above mentioned Power-On and Reset signals are shown in Figure 2-8 on page 2-16. Also, in this figure it is shown which GPIO's that are used to power-on and reset peripherals such as the Island 2 Bluetooth, the camera module, the FM radio, and the IrDA device.

For testing purposes, the Triton/Triton Lite accepts an unconditional reset input via the TESTRESET input pin (active high). On the I-Sample this pin is not currently connected however by removing resistor R474 and mounting R469 pushbutton S433 can be used for this purpose.

On the Triton/Triton Lite a remote Power-On input has been provided (RPWON). On the I-Sample board this is, as illustrated in Figure 2-8, connected directly to switch 2 of dipswitch S502. By setting this switch in the "ON" position the power-on sequence will be executed automatically when power is connected to the I-Sample board.

For additional information on the reset and power on sequence of the I-Sample, refer to the VRPC State Machine Flowchart and description in the TWL3031 datasheet.

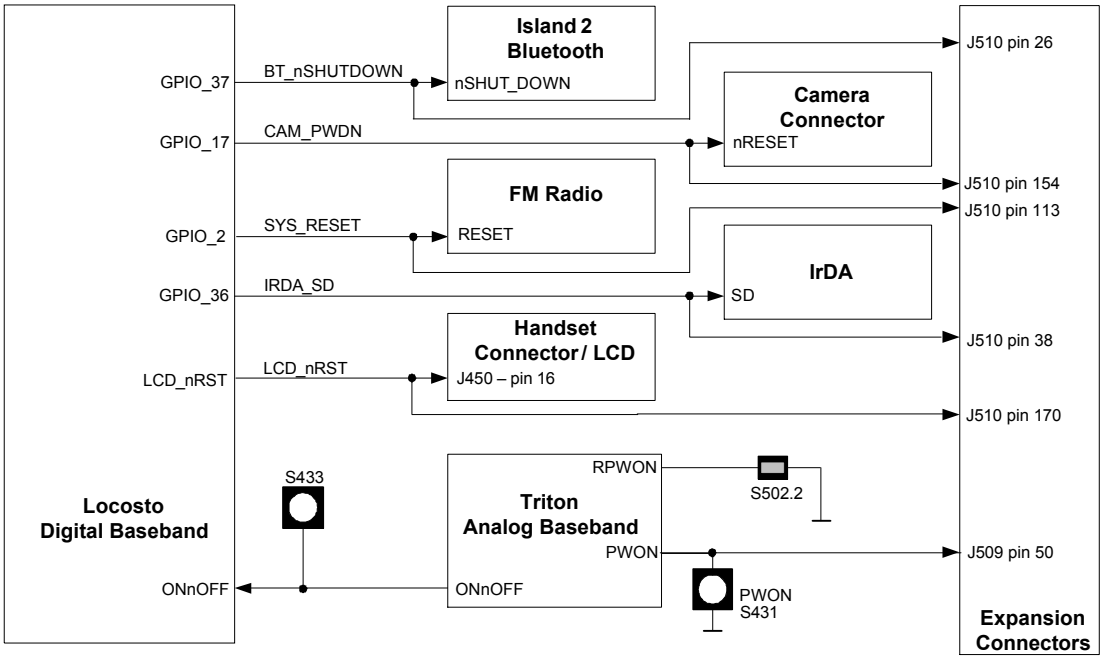


Figure 2-8. The Power-On and Reset circuitry.

2.7 GSM/GPRS Modem

The GSM/GPRS modem block is responsible for handling the RF communication according to specifications defined by 3GPP. The GSM/GPRS modem block contains three major functional units:

- LoCosto RF transceiver
- RF7115 Transmit Module
- Antenna and SMA connector

Figure 2-9 on page 2-17 shows a block diagram of the GSM/GPRS modem block. The LoCosto and the 26 MHz oscillator circuitry have been included in the diagram

in order to illustrate their connections to the GSM/GPRS modem block. The names of the connections are taken from the I-Sample schematics.

Note: The smaller components have been omitted from the diagram. Please refer to the I-sample schematics for further details.

The TX module is controlled by the LoCosto. The 26 MHz oscillator is used as reference clock.

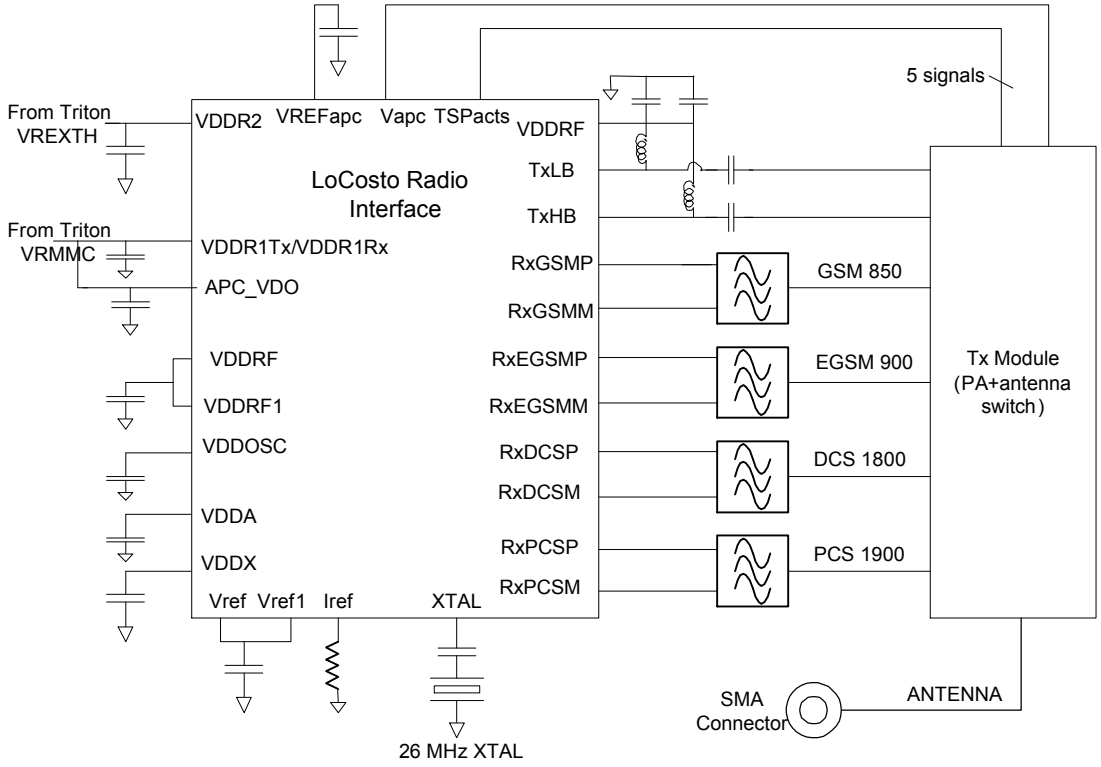


Figure 2-9. The GSM/GPRS modem block.

2.7.1 LoCosto RF Transceiver

The LoCosto Digital Base Band processor is merged with the Digital Radio Processor 2 (DRP 2).

The DRP2 is a GSM/GPRS Class 12 Digital transceiver GSM radio supporting GSM 850, EGSM 900, DCS 1800, and PCS 1900.

2.7.2 Transmit Module with internal switch (RF7115)

The Transmit Module is a device with an integrated antenna switch. It amplifies the up converted signals to a desired level. The transmit module operates in four different bands:

- GSM 850
- EGSM 900
- DCS 1800
- PCS 1900

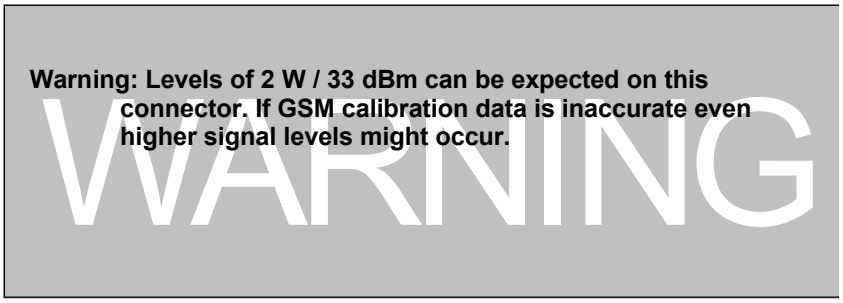
The power envelope is controlled by LoCosto through the APC during transmission. The power envelope is shaped to minimize transitions at the antenna. At the beginning and at the end of a burst, the desired power envelopes are obtained by applying predefined patterns of data (ramps) on the APC. With proper calibration this allows the PA to set the output power with high precision.

The PA is enabled by the TSPACT14 signal which is controlled by the LoCosto. In order to select which band to amplify the signals TSPACT11, TSPACT13, and TSPACT15 are used.

The integrated antenna switch connects the transmitter and receiver to the antenna jack. The transmit signals are low pass filtered, while the receive bands are separated by band pass SAW filters.

2.7.3 Antenna and SMA Connector

The GSM/GPRS-RF signal is available on an SMA connector that can be connected to an antenna or a radio communication tester. The I-sample is delivered with a quad band GSM antenna from Amphenol. The antenna should be mounted on J460 for communication with commercial networks. The characteristic impedance of the antenna is 50 Ohm.



2.8 Memory

The following sections describe the memory devices and the interfacing for the parts connected to the LoCosto EMIF (Enhanced Memory Interface Fast) on the I-Sample.

2.8.1 EMIF Memory Summary

The I-Sample board includes a single MCP IC that contains both NOR flash for code storage and pSRAM (CellularRAM) for code execution.

The I-Sample is designed to support a wide range of MCPs from Spansion with a varying range of densities and combinations on a single footprint. As default the I-Sample will be mounted with a 128 Mbit (NOR) + 64Mbit (CRAM) MCP. The Spansion MCP included on the I-Sample is given part number S71NS128JC0BFWVN.

For this particular device the 128 Mbit of NOR Flash is made up of 8 M x 16 bit memory cells. The NOR flash is divided into 4 banks of 32 Mbits. Bank A contains sectors of 4 x 8 KWords and 63 x 32 KWords. The other banks contain 64 x 32 KWords.

The 64 Mbit of CRAM is capable of high speed burst read and write, including a continuous burst write feature.

The MCP has a multiplexed Add and Data bus and is supplied by 1.8 V with 1.8 V I/Os.

On I-Sample 1.1 and above a single pSRAM is also included for debug and emulation (See Section 2.8.1.5).

2.8.1.1 MCP NOR Performance Specifications

- 65 ns Asynchronous Initial Access Time @ 66 MHz Burst speed
- 11 ns Burst Access Time @ 66 MHz
- 71 ns Synchronous Random Access Time @ 66 MHz
- Continuous Linear Burst as well as 8/16/32 Linear Burst
- Synchronous Burst Read
- Burst Mode Read: 25 mA
- Simultaneous Operation: 40 mA
- Program/Erase: 15 mA
- Standby Mode: 9 uA

2.8.1.2 MCP CRAM Performance Specifications

- 16 Word Page Size
- Interpage Read Access: 70 ns
- Intrapage Read Access: 20 ns
- Asynchronous/Synchronous Continuous Burst Read and Write
- Asynchronous Read < 25 mA
- Intrapage Read < 15 mA
- Initial access, Burst Read < 35 mA
- Continuous Burst Read < 15 mA
- Standby 120 uA

2.8.1.3 Spansion MCP Ball Out

The Ball Out of the S71NS128JC0BFWVN is shown below.

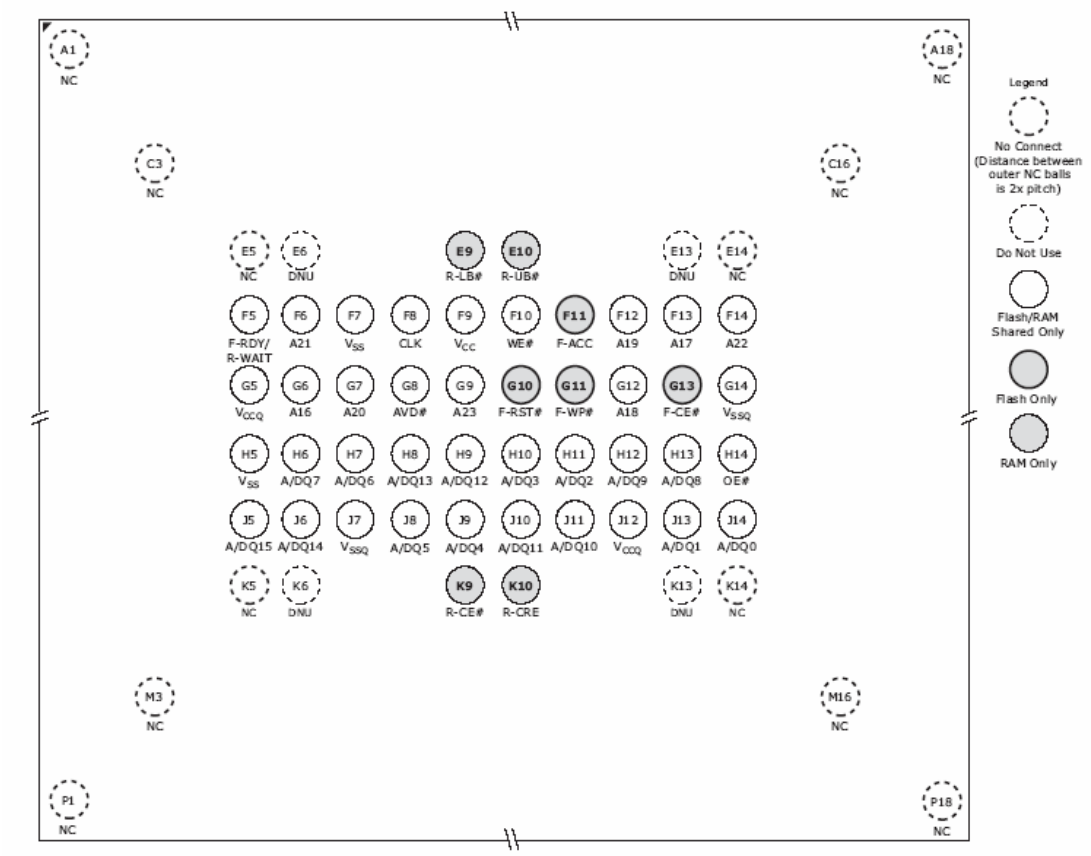


Figure 2-10. Top view of I-Sample MCP device pinout.

2.8.1.4 EMIF Memory Map

In Table 2-5 is listed the LoCosto memory map for the EMIF interface.

Table 2-5. I-Sample LoCosto EMIF memory maps.

Boot Area (0000:0000 - 003F:FFFF)					
Device name	**Start address**	**Stop address**	**Size**	**Data access**	**Device access**
Boot ROM	0000:0000	0000:FFFF	64 KB	8/16/32 R	32
Reserved	0001:0000	003F:FFFF	4032 KB	---	---
External Memory (0040:0000 - 17FF:FFFF)					
Device Name	**Start address**	**Stop address**	**Size**	**Data access**	**Device access**
External memory (CS0)	0040:0000	0x01FFFFFF	29.3 MB	8/16/32 RW	32
External memory (CS1)	0x02000000	0x03FFFFFF	32 MB	8/16/32 RW	32
External memory (CS2)	0x04000000	0x05FFFFFF	32 MB	8/16/32 RW	32
External memory (CS3)	0x06000000	0x07FFFFFF	32 MB	8/16/32 RW	32
Internal Memory (0800:0000 - 08FF:FFFF)					
Device name	**Start address**	**Stop address**	**Size**	**Data access**	**Device access**
Internal RAM (2.5Mbit)	0800:0000	0804:FFFF	320 KB	8/16/32 RW	32
Internal ROM (1.5Mbit)	0805:0000	0807:FFFF	192 KB	8/16/32 R	32
Reserved	0808:0000	08FF:FFFF	15.5 MB	---	---

2.8.1.5 Emulation RAM Memory

I-Sample 1.1 and later versions will contain an extra 128 Mbit of CRAM device that can be selected to provide emulation RAM and so that code can be run from CRAM. The device selected is the Micron MT45W8MW16BGX and is based on the same technology of that in the CRAM within the MCP.

The MT45W8MW16BGX device does not have a multiplexed ADD/DATA bus so the busses are short circuited on the PCB and control is made via the nFADV signal.

The performance is the same as that given for the CRAM part of the MCP above except the power consumption is slightly different.

- Asynchronous Read < 25 mA
- Intrapage Read < 15 mA
- Initial access, Burst Read < 35 mA
- Continuous Burst Read < 15 mA
- Standby 120 uA

2.8.1.6 Ball out for MT45W8MW16BGX Emulation RAM Memory

The Ball Out of the Micron MT45W8MW16BGX is shown below.

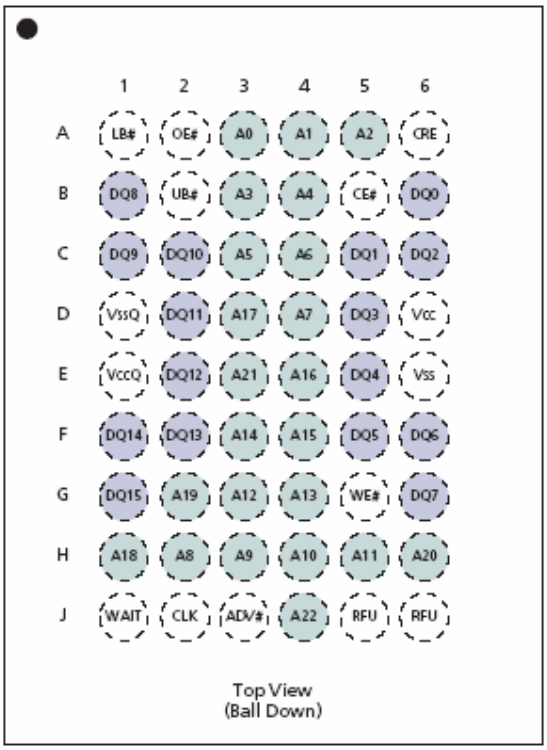


Figure 2-11. Top view of I-Sample Emulation RAM device pinout.

2.8.2 NAND FLASH

The I-Sample board contains a footprint for a NAND Flash device. The device that is mounted as default on the I-Sample is the TC58DYM92A2XGJ5. This is a 512 Mbit device manufactured by Toshiba.

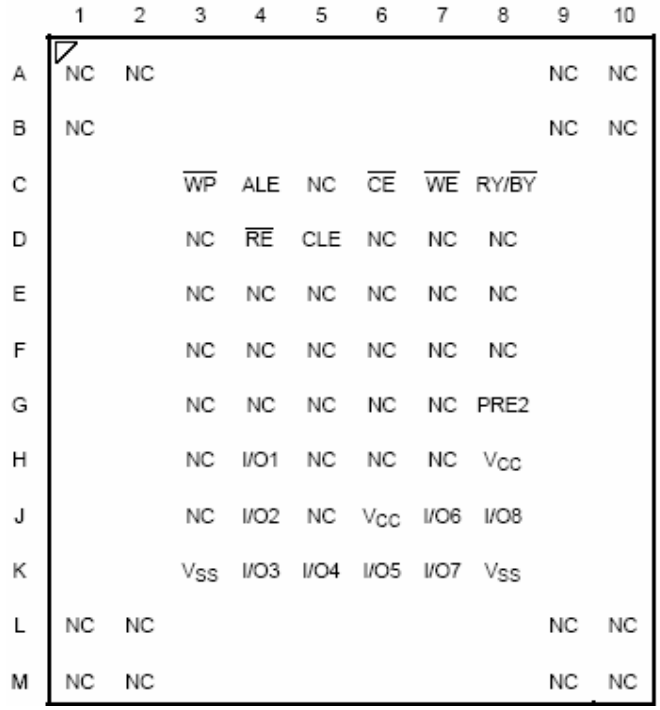


Figure 2-12. Top view of Toshiba TC58DYM92A2XGJ5.

The TC58DYM92A2XGJ5 connects directly to the dedicated NAND interface with LoCosto. The interface is a by 8 multiplexed ADD/DATA and has two Chip enables, but the I-Sample dedicates ND_CE1 to the NAND flash interface.

There is a hardware switch to disconnect the NAND CE which will disable the NAND device to isolate any multiplexed nets on that bus. This can be accomplished by setting dipswitch S502 subswitch 6 in the “ON” position.

The footprint of the NAND device above is compatible with various densities of NAND from Toshiba, from 128 Mbit to 2 Gb. The footprint is also compatible with the latest NAND devices available from Samsung and Micron.

2.8.2.1 Chip Select Switching Scheme

The I-Sample 1.0 has no options for changing the chip select selection. CS0 is connected to the MCP CRAM and CS3 is connected to the MCP NOR Flash. CS3 is the boot chip select.

The NAND Chip select can be disconnected from the NAND device using switch S502.6. On = Connected, Off = Not connected.

The I-Sample 1.1 and later contains the extra emulation RAM and has some capability to select which Chip selects are connected to which devices.

Table 2-6 shows the relevant switch settings for S301 for selecting EMIFS memory devices. The default setting will be to have both switches “OFF” so that the set up from I-Sample 1.0 is replicated.

Table 2-6. Selecting EMIFS devices using dipswitch S301.

S301.1	S301.2	nCS0	nCS3
ON	ON	Disconnected	Disconnected
OFF	ON	MCP (CRAM)	Emulation (CRAM)
ON	OFF	MCP (NOR Flash)	MCP (CRAM)

OFF	OFF	MCP (CRAM)	MCP (NOR Flash)

2.9 USIM Interface

The Locosto chip supports a USIM interface. USIM expands the functionality of a standard interface and enables multimedia context via Smart Card technology for future developments. The LoCosto supports 1.8 V and 3 V SIMs.

All the SIM interface signals are connected to the LoCosto except the signal SIMDTC which is the SIM detection signal connected to Triton/Triton Lite. SIM_CD is a card detect switch that is high when a SIM card is present.

In Table 2-7 is listed the signals available on the SIM interface connector.

Table 2-7. Signals on the SIM interface connector.

Pin #	Signal	Comment
1	VRSIM	SIM Supply from Triton/Triton Lite
	USIM-PBIAS	SIM power supply bias
2	USIM-RST	SIM reset signal
3	USIM-CLK	SIM Clock signal
4	SIMDTC	SIM Detect (Triton/Triton Lite connection)
5	GND	Ground
6	VRSIM	SIM Supply from Triton/Triton Lite
7	USIM-IO	SIM Data In/Out
	USIM-PW-CTL	SIM power supply feedback through 10 KOhm resistor
8	GND	Ground

2.10 White LED Drivers

The Triton/Triton Lite device that is used on I-Sample contains a DC/DC converter capable of providing a 20 mA constant current source up to 21V to each of three separate LED chains. Three separate control signals are available to control three strings of LEDs.

LED_A and LED_B can each have a maximum of 4 White LEDs and LED_C can have a maximum of 2.

The I-Sample has 10 Panasonic LNJ026X8BRAW White LEDs mounted to the board to test and demonstrate this functionality. The connection of the 10 LEDs is shown in Figure 2-13.

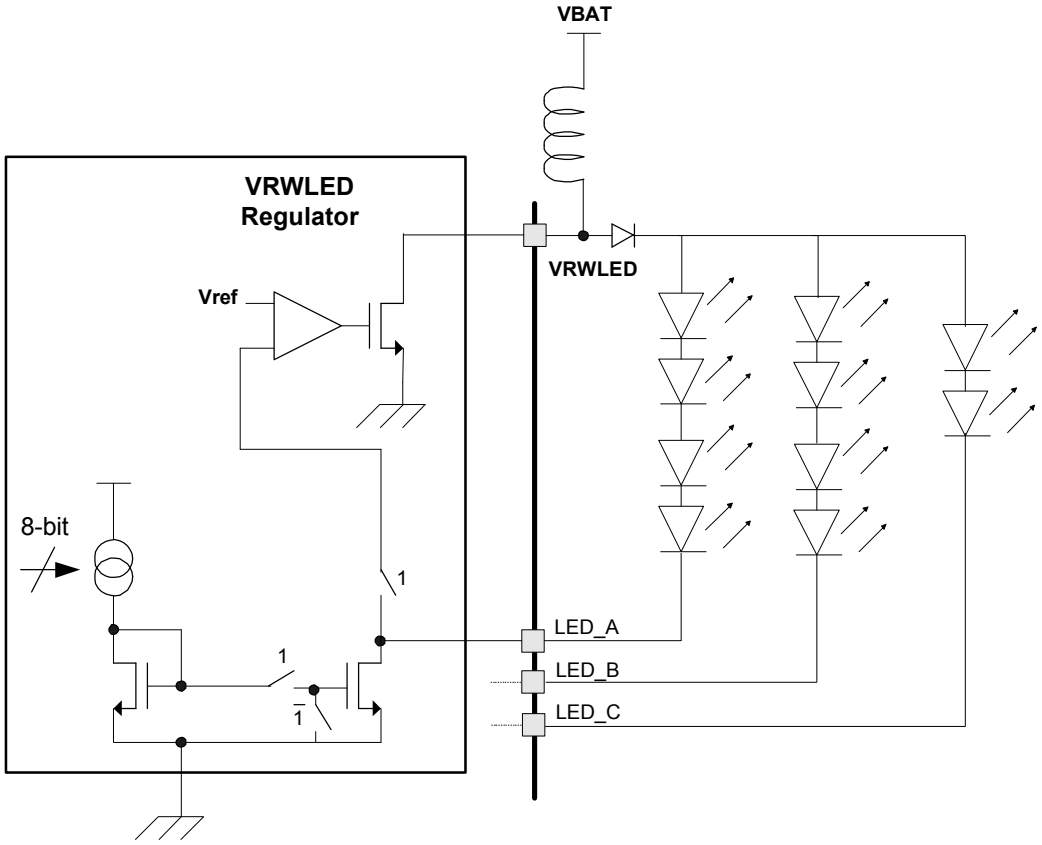


Figure 2-13. White LEDs and white LED driver scenario.

2.11 Dipswitch Functionality

The I-Sample board contains a 6 way dipswitch (S502) to control various functions on the board. The layout of the dipswitch is shown in Figure 2-14 where the individual switches are labeled S1 through S6.

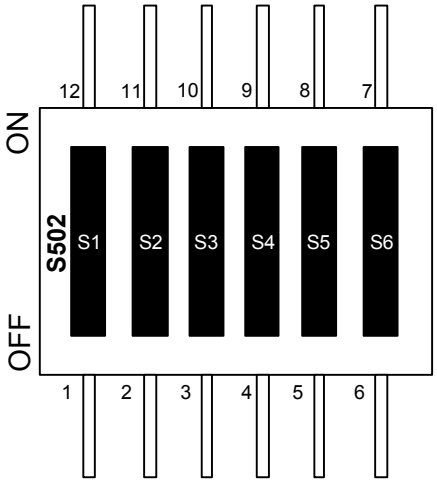


Figure 2-14. Layout of the 6 way dipswitch S502.

In Table 2-8 is listed the functions that are associated with each of the switches.

Table 2-8. Functionality of the S502 6 way dipswitch.

Switch	Switch Name	Description

Switch	Switch Name	Description
S1	USB Boot Select	When OFF, LoCosto pin T10 = Low and ROM booting from UART is enabled. When ON, LoCosto pin T10 = High and USB Boot selection is enabled
S2	RPWON	When OFF, Triton/Triton Lite input RPWON is pulled up internally and not active. When ON, Triton/Triton Lite input is pulled low and RPWON signal activates Triton/Triton Lite state machine to power on
S3	nBSCAN	Boundary scan enable pin for Locosto. When ON, Locosto pin T1 is low and Boundary scan is enabled. When OFF, Locosto pin T1 is high (Boundary scan disabled)
S4	Handset Backlight	When OFF, Handset backlight control is pulled Low and backlight is ON. When ON, Handset backlight control is High and handset backlight is OFF
S5	UART Selection	When OFF, UART selection is pulled low and Locosto UART is connected to the Bluetooth device. When ON, UART selection is held high and Locosto UART is connected to the RS232 device (DSUB9 connector)
S6	NAND Enable	When OFF, the NAND Flash device Chip Enable (CE1) is disconnected, when ON it is connected

2.12 Bluetooth

The Bluetooth part of the I-Sample includes the use of Texas Instruments single chip BRF6150 (Island 2) device. The Island 2 chip is a highly integrated single-chip CMOS Bluetooth device that forms a complete standalone Bluetooth wireless communications system. Some of the features for this device are listed below:

- Single-Chip 0.13 µm CMOS Bluetooth™ Solution
- Bluetooth 1.1 Specification compliant
- Bluetooth 1.2 Specification conformance
- Automatic Clock Recognition Mechanism
- On-Chip Digital Radio Processor (DRP)
- Integrated 2.4 GHz RF Transceiver
- Optimized for Cellular Phone Environment
- On-Chip T/R RF Switch
- Internal Regulators
- Support for 1.9 V to 3.6 V Power Supply
- Embedded ARM7TDMIE Microprocessor
- High-Rate H4 UART Host Controller Interface (HCI)
- Embedded Point-to-Multipoint Bluetooth Core
- Support for all Bluetooth Packet Types (Voice and Data)
- Support for Park, Sniff, Hold and M/S Switch
- A-Law, µ-Law, Linear and Transparent Codec Interface
- Support for Full Bluetooth Data Rate (723.2 KBPS)
- 4.5 x 4.5 mm uBGA

2.12.1 Physical Connections

The connections established between the BRF6150 and its interfacing components are shown in Figure 2-15. The BRF6150 is connected to the LoCosto via an audio codec interface and an UART Host Serial Interface (HCI).

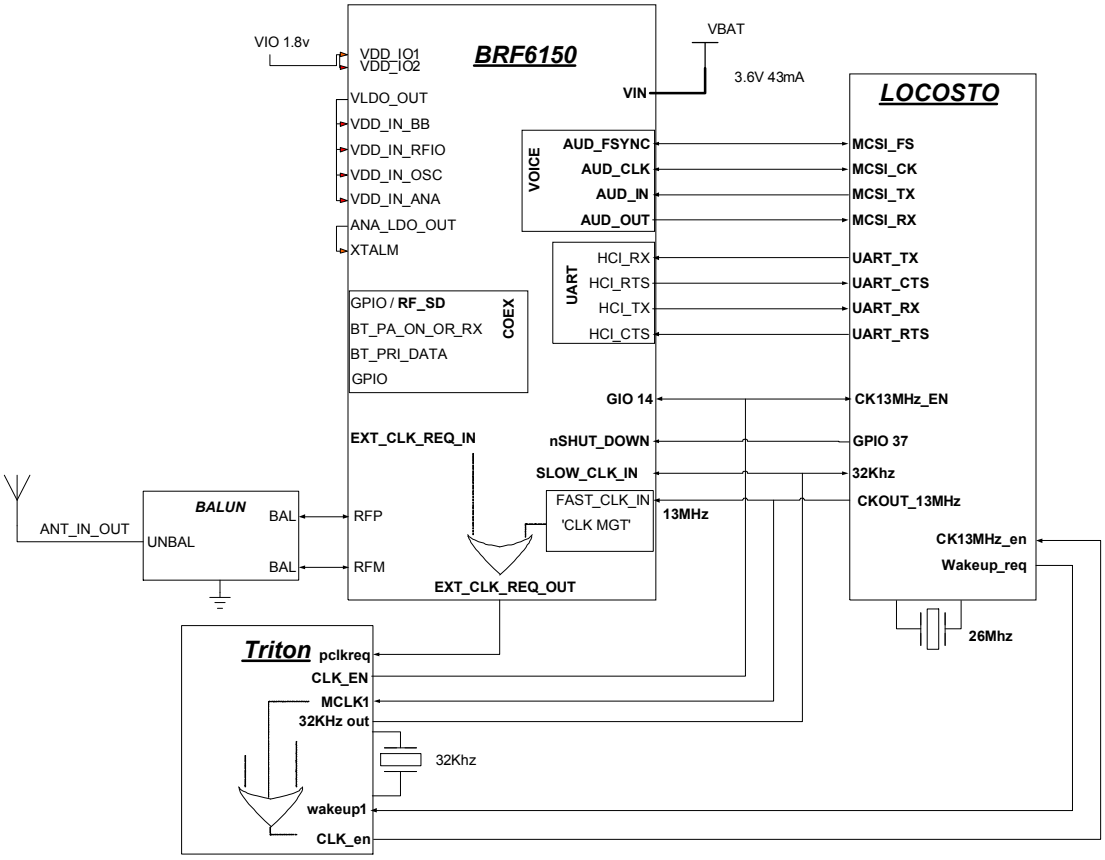


Figure 2-15. The Bluetooth physical connections.

Furthermore, the I-Sample 2.0 and beyond has been prepared for implementation of the Island 3 Bluetooth IC.

2.12.2 UART Host Serial Interface

The BRF6150 incorporates one UART module dedicated to the host controller interface (HCI) transport layer. The UART HCI hardware is compatible with the NS16C750 device, which includes the following features:

- Supports standard PC baud-rates, or any other baud-rate generation using an internal divider
- Transmit and receive FIFO buffers
- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTR/RTS hardware flow control

The HCI UART is compatible with part H4, HCI UART Transport Layer specification in the Bluetooth version 1.1 specifications and also compatible with the new addition – H5, HCI Three Wires UART transport layer.

Since there is only one UART on the LoCosto it is shared between the Island 2 device and the RS232 device. Selection between the two is accomplished by setting dipswitch S502 subswitch 5. For details about this see Section 2.11.

2.12.3 Audio Codec Interface

The BRF6150 comes with an audio codec interface which is a dedicated serial port that provides the necessary logic to interface with several kinds of PCM codecs. The four relevant signals on the BRF6150 are shown in Table 2-9 together with the corresponding pin connections on the I-sample.

Table 2-9. Bluetooth audio interface signals.

BRF6150 Connections		LoCosto Connections			
Name	**Pin #**	**Name**	**Pin #**	**Direction**	**Description**
AUD_CLK	B6	GPIO_43/MCSI_CK	U3	I	Codec Transmit/Receive Clock
AUD_FSYNC	A7	GPIO_44/MCSI_FS	V3	I	Codec Frame Sync Control
AUD_OUT	C7	GPIO_46/MCSI_RX	T4	I	Codec Audio Data Out
AUD_IN	C5	GPIO_45/MCSI_TX	V2	O	Codec Audio Data In

- This interface offers extended flexibility by providing parameters configurable by a vendor-specific HCI command.

2.12.4 Antenna

On the I-Sample the antenna has been provided through the connector J902.

For measurement purposes of the Bluetooth RF signal two different options are offered:

- Measure via the RF switch/antenna (J902)
- Measure with the use of the internal antenna in the PCB

2.13 Serial Busses

On the I-Sample board different serial busses have been included to handle communication between the individual components on the board. These busses are referred to as internal serial busses and a complete list of those available on the I-Sample board is listed below.

- 2 Inter Integrated Circuit Busses (I²C)
- Universal Asynchronous Receiver/Transmitter (UART)
- Serial Port Interface (SPI)

Also, serial busses have been provided to handle external communication e.g. between the I-Sample and a PC. The external serial busses implemented are:

- Universal Serial Bus (USB)
- RS-232 Bus
- Infrared Data Association Bus(IrDA)

2.13.1 I²C

The I²C serial bus is a 2 wire serial bus developed by Phillips Semiconductors. According to Phillips the I²C has become a de facto world standard that is now implemented in more than 1000 different IC's and licensed to more than 50 companies.

Data are packed into 8 bit data packages where the data is transferred between the master and the slave at rates of either 100 kb/sec. or 400 kb/sec.

On the LoCosto two I²C controllers have been implemented that can act both as masters and slaves. However, it is mainly the master functionality that is being used in order to control different peripherals on the I-Sample board. In Table 2-10 is listed which devices the two I²C busses are connected to. Furthermore, for monitoring of the signals, the signals have been routed to the J510 expansion connector.

Table 2-10. I²C pin out on expansion connector J510.

Bus	Connected To	Signal	J510 pin #
I²C-1	• Triton/Triton Lite	I2C_1_SDA	89
	• FM Radio	I2C_1_SCK	93
I²C-2	• Camera Conn.	I2C_2_SDA	90
		I2C_2_SCK	94

2.13.2 UART

The UART is used to transfer data between peripheral units located on the I-Sample reference board. Only one UART is available which is why external switching circuitry is necessary in order to allow access to more than one peripheral unit. The UART interface pins are listed in Table 2-11.

Table 2-11. UART pins.

LoCosto		Description
Pin Name	Pin #	
UART_RX	L7	Data input
UART_TX	P3	Data output
UART_RTS	R3	Ready-To-Send (Hardware flow control)
UART_CTS	R2	Clear-To-Send (Hardware flow control)

On the I-Sample, two UART routing scenarios are available which are listed below:

- ☐ LoCosto UART to RS-232 (DSUB-9 Connector J508)
- ☐ LoCosto UART to Island 2 Bluetooth

The switching circuitry is controlled by dipswich S502 subswitch 5. See Section 2.11 for details concerning the dipswitch. The two routing scenarios are described in details in the next sections.

2.13.2.1 LoCosto UART to RS-232 (DSUB-9 Connector J508)

In this scenario the 4 UART signals are routed from the LoCosto to the DSUB-9 connector J508 through switch U515. The switch is controlled by the dipswitch S502 subswitch 5 where it must be set to “ON”. This scenario is used for interfacing a PC with the LoCosto onboard ARM 7. In Figure 2-16 the routing path for this scenario is illustrated by the boldface line.

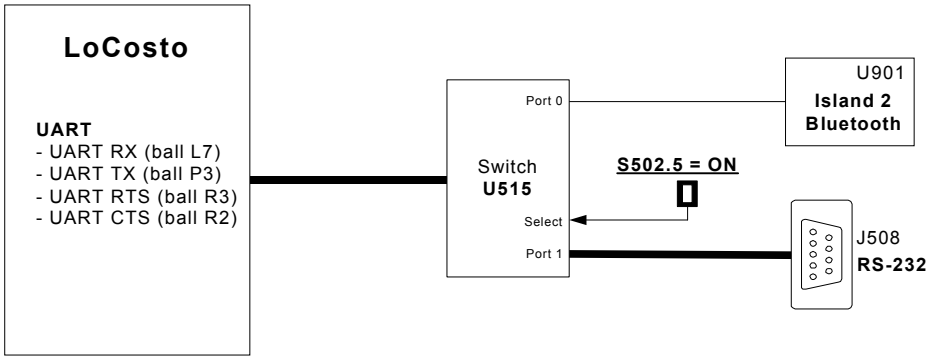


Figure 2-16. Routing between LoCosto UART and DSUB 9 connector.

2.13.2.2 LoCosto UART to Island 2 Bluetooth

In order to be able to use the Island 2 Bluetooth device together with the LoCosto a UART routing scenario must be established between the two. To enable this scenario dipswitch S502 subswitch 5 must be set in the “OFF” position. In Figure 2-17 the routing path is indicated by the boldface line.

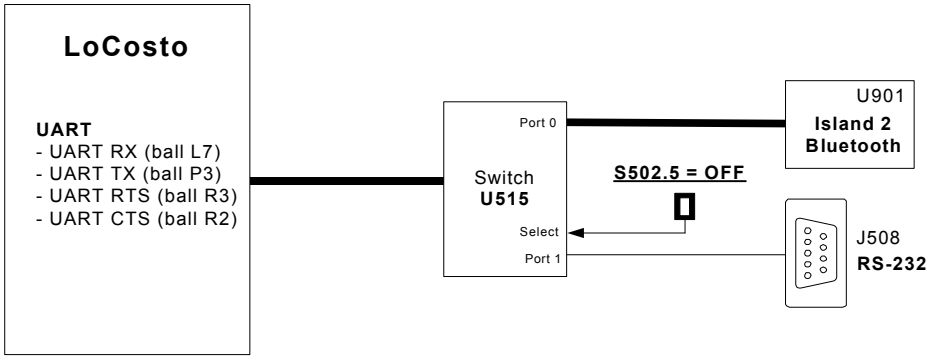


Figure 2-17. Routing between LoCosto UART and Island 2 Bluetooth.

2.13.3 Serial Port Interface (SPI)

The serial interface is a bi-directional four lines interface dedicated to transfer data to and from peripheral devices e.g. a secondary display. The four signals used in the interface are listed in Table 2-12.

Table 2-12. Serial Port Interface pins.

LoCosto		Description
Pin Name	**Pin #**	
SPI_MOSI	C5	The data input
SPI_MISO	F7	The data output
SPI_CLK	G9	The clock used to shift-in and shift-out data
SPI_nCS0	E6	The device enable

This serial port is based on a looped shift-register thus allowing both transmit (PISO) and receive (SIPO) modes. It can operate either in master mode or slave mode, using MCU-DSP or DMA protocol. It supports up to three serial devices by multiplexing 2 other chip selects out (SPI_nCS0 and SPI_nCS0).

During transfer using the SPI bus the MSB is always sent first.

2.13.4 Universal Serial Bus (USB)

On the I-Sample USB functionality is provided by the Triton/Triton Lite ABB. The Triton/Triton Lite includes a Universal Serial Bus (USB) [1.0] transceiver with a car kit interface, able to support USB 12 Mbit/s Full-Speed (FS) and USB 1.5 Mbit/s Low-Speed (LS).

On the Triton/Triton Lite there are a total of 8 pins used for USB transfer operations. Four signals (1.8 V) are interfaced directly with the Locosto DBB and four signals (3.3 V) are connected to the USB mini B receptacle (J411). Both differential and single-ended signaling modes are available for the interface between the Locosto and Triton/Triton Lite. This is controlled by the USB_SE0 signal.

The Triton/Triton Lite USB controller is highly configurable with respect to power management and functionality. This is all controlled by setting the USB registers on the Triton/Triton Lite using the I²C interface.

A diagram of the USB implementation is shown in Figure 2-18.

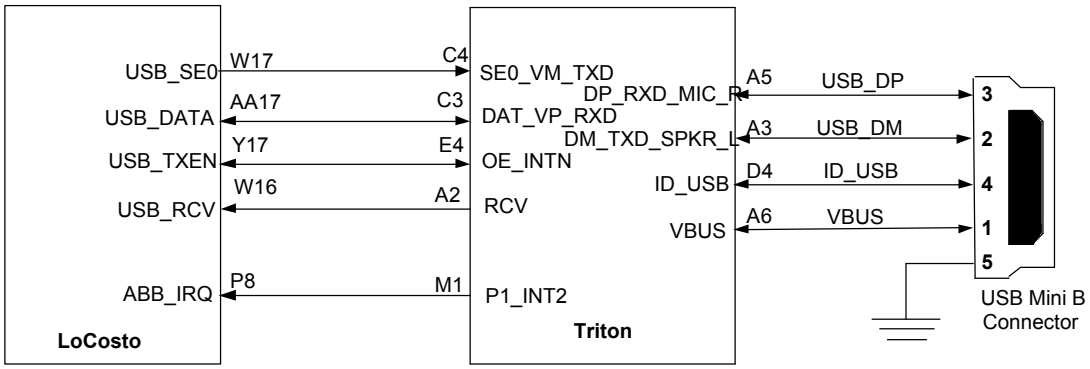


Figure 2-18. USB interface connections.

For more detailed information on the Universal Serial Bus refer to the Triton document: “13_01_03_02378_bls_0010_usb.doc”.

2.13.5 RS-232

For RS-232 serial communication between the I-Sample board and e.g. a PC a Texas Instruments SN65C3232 has been implemented. The SN65C3232 is a complete serial port (2 drivers/2 receivers) designed for PC and notebook computers.

2.13.6 Infrared Data Association (IrDA) Transceiver

To handle infrared communication to and from the I-Sample board an Agilent HSDL-3220 IrDA transceiver has been implemented. The IrDA supports speed options that range from 9.6 Kb/sec. (Slow Infrared SIR) to 4.0 Mbit/sec. (Fast Infrared FIR).

To allow communication from the IrDA transceiver to the LoCosto, a full duplex serial interface is established (RX/TX). Furthermore, it is possible to shutdown the IrDA transceiver using the LoCosto GPIO_36.

2.14 Stereo Headset Connector

A 4 pole stereo audio connector (J484) has been provided on the I-Sample board for headset functional purposes. The headset audio signals are routed from the Triton/Triton Lite to this connector. In Table 2-13 is listed the headset signals and the pins they are connected to.

Table 2-13. Pin description of 2.5 mm stereo output jack connector.

Pin #	Signal Name	Description
1	HSOR	Right audio channel
2	GND	Ground
3	HSOL	Left audio channel
3	HSMIC	Microphone input signal

The corresponding male stereo audio jack is shown in Figure 2-19.

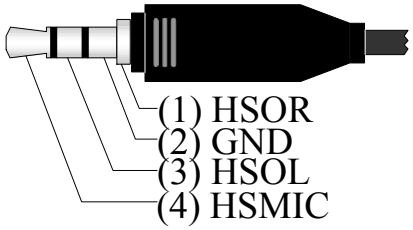


Figure 2-19. Male 4 pin stereo jack.

2.15 Debug Facilities

The I-Sample contains connectors and test points to ease the testing of the board and to enable the addition of extra circuitry for debugging.

Two expansion connectors are available through which all the necessary and important system signals are accessible. A JTAG connector is available for attaching a JTAG module/emulator.

A plug-in “VISU” board is available that gives easy access to all the signals. Furthermore, additional LEDs have been provided which is controlled by selected GPIOs. This is described in detail in the VISU board design documentation.

2.15.1 JTAG

The I-Sample board contains a standard 14 pin JTAG connector (J511). The JTAG signals are also available on the expansion connectors. In Table 2-14 is listed the pins on JTAG connector J511.

Table 2-14. JTAG signals on the connectors J511

Name	Pin #	Description
TMS	1	Test Mode Select: Directs the next state of the IEEE 1149.1 test access port state machine
nTRST	2	Test Logic Reset
TDI	3	Test Data Input: Scan data input to the device
GND	4	GND
3_3V_Aux	5	3.3V Supply
N/C	6	Not Connected
TDO	7	Test Data Output: Scan data output of the device
GND	8	GND

Name	Pin #	Description
RTCK	9	Return Test Clock
GND	10	GND
TCK	11	JTAG Test Clock
GND	12	GND
nEMU1	13	Emulation and Test 1 Not: Helps create trigger channel one
nEMU0	14	Emulation and Test 0 Not: Helps create trigger channel zero

2.15.2 Test Points

Test points on the I-Sample board have been provided in order to verify the operation of some of the critical components. The test points available are listed in Table 2-15.

Table 2-15. Test points available on the I-Sample.

Test Point	Description
TP201	XANATST3
TP202	XANATST4
TP203	XANATST5
TP204	ANATST1
TP205	ANATST2
TP206	XANATST6
TP207	Wake Up Request signal from Triton
TP208	VSP_VFS (Voice Serial Port)
TP209	VSP_VCK (Voice Serial Port Clock)
TP210	VSP_VDX (Voice Serial Port Transmit port)
TP211	Unused Sense signal for PMC (Power management control)
TP212	Unused Force signal for PMC (Power management control)
TP213	VSP_VDR (Voice Serial Port Receive port)
TP214	I2S_SCK (I²S bus Clock)
TP215	I2S_WS (I²S bus)
TP216	I2S_SDX (I²S bus Transmit port)
TP217	I2S_SDR (I²S bus Receive port)
TP313	Test point for accelerated programming voltage to MCP.
TP314	Test point on GPIO_11/nEMU_1 also used as Sleep signal for Golden Eye
TP315	Unused NAND Write protect signal from LoCosto.
TP316	Unused Write protect signal input to NAND flash.

Test Point	Description
TP317	Unused Flash Write protect signal from LoCosto (muxed with CAM_D2 signal)
TP411	System reset signal
TP412	Unused Boot mode select input to Triton/Triton Lite
TP454	Unused GPIO dedicated for control of LED torch
TP455	1.5V supply input from THEO board
TP503	Cathode of IRDA diode
TP562	JTAG TRSTN signal
TP563	CKM Signal
TP601	Spare TSPACT signal (TSPACT12)
TP701	Unused debug port from FM radio module
TP702	Unused debug port from FM radio module
TP703	Detect output port from FM radio module
TP901	TX_DBG input to Island Bluetooth IC
TP902	ANATEST1 signal from Island Bluetooth IC
TP903	ANATEST2 signal from Island Bluetooth IC
TP904	BGAP_I pin on Island Bluetooth IC
TP910	Spare IO7 on Island Bluetooth IC
TP911	CKEN input to Island Bluetooth IC
TP912	Spare IO15 on Island Bluetooth IC
TP913	Spare input on Island Bluetooth IC
TP914	Spare IO4 on Island Bluetooth IC
TP915	Spare IO5 on Island Bluetooth IC
TP916	Spare input on Island Bluetooth IC
TP917	Bluetooth shutdown signal
TP918	BT <–> LoCosto UART connection BT_RX signal
TP919	BT <–> LoCosto UART connection BT_TX signal
TP920	BT <–> LoCosto UART connection BT_RTS signal
TP921	BT <–> LoCosto UART connection BT_CTS signal
TP922	Test Point on BT extension connector (I-Sample 2.0+ Only)

2.15.3 The Camera Board / THEO Connector

A connector is available on the I-Sample to give the option of attaching a PCB containing a camera or the THEO board, The THEO board is an expansion board

containing the GOLDENEYE co-processor which has the capability of enabling Megapixel cameras on the I-Sample platform. The connector chosen for this is the Samtec MEC1-130-02-S-D-LC connector. The connector includes 60 pins and features a connection key. In Figure 2-20 is shown the Samtec MEC1 connector.

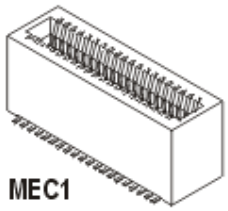


Figure 2-20. The Samtec MEC1 connector.

The Samtec MEC1 connector mates with a 1.6 mm thick PCB board where gold plated copper pads are used as interface connectors. In order for the PCB to be able to fit into the MEC1-130-02-S-D-LC connector it must be no wider than 31.75 mm. An illustration of the PCB connection part is shown in Figure 2-21.

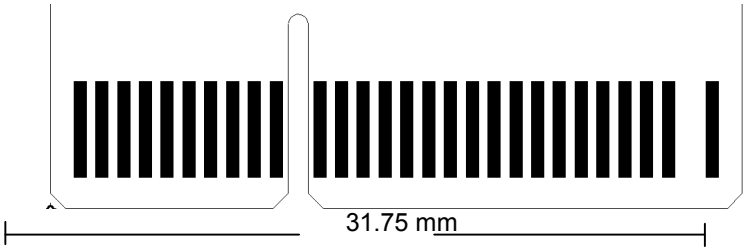


Figure 2-21. The PCB footprint that mates with the Samtec MEC1 connector.

The pinout for the connector is shown in Table 2-16.

Table 2-16. THEO / Camera connector pinout.

Pin #	Signal	Dir	Pin #	Signal	Dir
1	GND		2	GND	
3	CCPX_CP	O	4	NC/HPI_D15	
5	CCPX_CN	O	6	NC/HPI_D14	
7	GND		8	GND	
9	CCPX_DP	O	10	VBATT	
11	CCPX_DN	O	12	VBATT	
13	GND		14	GND	
15	D1_5V		16	D1_8V	
17	NC/HPI_D13		18	CAM_I2CSCL	I/O
19	NC/HPI_D12		20	CAM_I2CSDA	I/O
21	*mechanical key*		22	*mechanical key*	
23	D2_8V		24	BOARD_ID	O
25	NC/HPI_D11		26	RSV0	
27	NC/HPI_D10		28	RSV1	

29	GND		30	RSV2/HPI_A	
31	HTODMINT	I	32	RSV3/HPI_WAITn	
33	RESETn/CAM_RESETn	I	34	GND	
35	POWEREN	I	36	CAM_D0/HPI_D0	I
37	SLEEP/CAM_PWRDN	I	38	CAM_D1/HPI_D1	I
39	DMTOHINT	O	40	CAM_D2/HPI_D2	I
41	NC/HPI_D9		42	CAM_D3/HPI_D3	I
43	SDEN	I	44	CAM_D4/HPI_D4	I
45	SDO	O	46	CAM_D5/HPI_D5	I
47	SDI	I	48	CAM_D6/HPI_D6	I
49	SCLK	I	50	CAM_D7/HPI_D7	I
51	GND		52	GND	
53	NC/HPI_D8		54	CAM_HSYNC/HPI_OEn	I
55	GND		56	CAM_VSYNC/HPI_WEn	I
57	SYSCLK/CAM_EXTCLK	I	58	CAM_PCLK/HPI_CEn	I
59	GND		60	GND	

2.16 Expansion/Debug Connectors

The pin configurations for the two expansion connectors are shown in the tables below. A table of the pins for expansion connector A (J510) and expansion connector B (J509) is shown below.

2.16.1 Expansion Connector A

Table 2-17. Pin configuration of expansion connector A (J510).

Pin #	Name	Function	Pin #	Name	Function
1	GND	Ground	2	GND	Ground
3	DATA/ADD0	Muxed LoCosto EMIFS	4	DATA/ADD1	Muxed LoCosto EMIFS
5	DATA/ADD2	Muxed LoCosto EMIFS	6	DATA/ADD3	Muxed LoCosto EMIFS
7	DATA/ADD4	Muxed LoCosto EMIFS	8	DATA/ADD5	Muxed LoCosto EMIFS
9	DATA/ADD6	Muxed LoCosto EMIFS	10	DATA/ADD7	Muxed LoCosto EMIFS
11	DATA/ADD8	Muxed LoCosto EMIFS	12	DATA/ADD9	Muxed LoCosto EMIFS
13	DATA/ADD10	Muxed LoCosto EMIFS	14	DATA/ADD11	Muxed LoCosto EMIFS
15	DATA/ADD12	Muxed LoCosto EMIFS	16	DATA/ADD13	Muxed LoCosto EMIFS
17	DATA/ADD14	Muxed LoCosto EMIFS	18	DATA/ADD15	Muxed LoCosto EMIFS

19	ADD16	Muxed LoCosto EMIFS	20	ADD17	Muxed LoCosto EMIFS
21	ADD18	Muxed LoCosto EMIFS	22	ADD19	Muxed LoCosto EMIFS
23	ADD20	Muxed LoCosto EMIFS	24	ADD21	Muxed LoCosto EMIFS
25	ADD22	Muxed LoCosto EMIFS	26	BTnSHUTDOWN	Bluetooth Power CTRL
27	GND	Ground	28	GND	Ground
29	RnW		30	nBHE	Muxed LoCosto EMIFS
31	nBLE		32	nMOE	Muxed LoCosto EMIFS
33	nFWP / CAM_D2	Muxed LoCosto EMIFS	34	FDP	Muxed LoCosto EMIFS
35	nRDYMEM	Muxed LoCosto EMIFS	36	nFADV	Muxed LoCosto EMIFS
37	nCS0	Muxed LoCosto EMIFS	38	IRDA_SD	IrDA Shutdown CTRL
39	LED_TRCH	GPIO to control LED TRCH	40	nCS3	Muxed LoCosto EMIFS
41	GND	Ground	42	GND	Ground
43	GND	Ground	44	GND	Ground
45	KBC4	Keypad interface	46	KBR4	Keypad interface
47	KBC3	Keypad interface	48	KBR3	Keypad interface
49	KBC2	Keypad interface	50	KBR2	Keypad interface
51	KBC1	Keypad interface	52	KBR1	Keypad interface
53	KBC0	Keypad interface	54	KBR0	Keypad interface
55	GND	Ground	56	GND	Ground
57	CLK32K	RTC oscillator output - Triton/Triton Lite	58	CKOUT_13Mhz	System Clock output
59	GND	Ground	60	GND	Ground
61	USB_SE0	USB signal - LoCosto	62	BT_AUD_CLK	Bluetooth audio clock
63	GND	Ground	64	GND	Ground
65	USB_DATA	USB data - LoCosto	66	BT_AUD_OUT	Bluetooth audio out - LoCosto
67	GND	Ground	68	GND	Ground
69	USB_TXEN	USB signal - LoCosto	70	BT_AUD_IN	Bluetooth audio in - LoCosto
71	GND	Ground	72	GND	Ground
73	USB_RCV	USB signal - LoCosto	74	BT_AUD_FSYNC	Bluetooth audio sync
75	GND	Ground	76	GND	Ground
77	CAM_D1/DCD_TXIR	Multiplexed, multi use	78	BT_RTS/UART2_RTS	UART RTS
79	GND	Ground	80	GND	Ground

81	CAM_D0/DSR_RXIR	Muxed, Multi Use	82	BT_RX/UART2_RX	UART RX
83	GND	Ground	84	GND	Ground
85	BT_CTS/UART2_CTS	UART CTS	86	BT_TX/UART2_TX	UART TX
87	GND	Ground	88	GND	Ground
89	I2C_1_SDA	I²C-1 data	90	I2C_2_SDA	I²C-2 data
91	GND	Ground	92	GND	Ground
93	I2C_1_SCL	I²C-1 clock	94	I2C_2_SCL	I²C-2 clock
95	GND	Ground	96	GND	Ground
97	SPI_MOSI	SPI data - LoCosto	98	SPI_CLK	SPI bus clock
99	SPI_MISO	SPI data - LoCosto	100	SPI_NCS0	SPI bus Chip select 0
101	SPI_NCS1	SPI Chip Select 1	102	GND	Ground
103	GND	Ground	104	TSPACT8	RF control signal
105	TSPACT8	RF control signal	106	TSPACT10	RF control signal
107	GND	Ground	108	TSPACT11	RF control signal
109	APC_OUT	RF control signal	110	TSPACT12	RF control signal
111	GND	Ground	112	TSPACT13	RF control signal
113	SYS_RESET	Globally used reset	114	TSPACT14	RF control signal
115	GND	Ground	116	TSPACT15	RF control signal
117	GPIO_1	Reserved for battery HDQ	118	GND	Ground
119	GND	Ground	120	GND	Ground
121	PERIP_INTERFACE0	LCD/NAND data	122	ND_WE	NAND control signal
123	GND	Ground	124	GND	Ground
125	PERIP_INTERFACE 1	LCD/NAND data	126	ND_nWP/CAM_D4	NAND control signal
127	GND	Ground	128	GND	Ground
129	PERIP_INTERFACE 2	LCD/NAND data	130	ND_CE1	NAND control signal
131	GND	Ground	132	GND	Ground
133	PERIP_INTERFACE 3	LCD/NAND data	134	ND_RnB	NAND control signal
135	GND	Ground	136	GND	Ground
137	PERIP_INTERFACE 4	LCD/NAND data	138	ND_ALE	NAND control signal

139	GND	Ground	140	GND	Ground
141	PERIP_INTERFACE 5	LCD/NAND data	142	ND_CLE	NAND control signal
143	GND	Ground	144	GND	Ground
145	PERIP_INTERFACE 6	LCD/NAND data	146	ND_RE	NAND control signal
147	GND	Ground	148	GND	Ground
149	PERIP_INTERFACE 7	LCD/NAND data	150	LCD_nCS0	LCD IF chip select
151	GND	Ground	152	GND	Ground
153	CAM_XCLK	Camera input clock	154	CAM_PWDN	Camera Power CTRL
155	GND	Ground	156	GND	Ground
157	CAM_LCLK	Camera output clock	158	LCD_RS	LCD IF register select
159	GND	Ground	160	GND	Ground
161	CAM_VS/CAM_D3	Camera Data/VSync	162	LCD_RnW	LCD IF read not write
163	GND	Ground	164	GND	Ground
165	CAM_HS	Camera horizontal sync o/p	166	LCD_ESTRB	LCD IF strobe signal
167	GND	Ground	168	GND	Ground
169	USIM_RST	SIM reset signal	170	LCDnRST	LCD IF register select
171	GND	Ground	172	GND	Ground
173	USIM_CLK	SIM Clock signal	174	USIM_PW_CTL	SIM Power control signal
175	GND	Ground	176	GND	Ground
177	USIM_IO	SIM data signal	178	USIM_PBIAS	SIM Bias signal
179	GND	Ground	180	GND	Ground

2.16.2 Expansion Connector B

Table 2-18. Pin configuration of expansion connector B (J509).

Pin #	Name	Function	Pin #	Name	Function
1	VBAT	Battery Supply	2	VBAT	Battery Supply
3	VBAT	Battery Supply	4	VBAT	Battery Supply
5	VBAT	Battery Supply	6	VBAT	Battery Supply
7	VBAT	Battery Supply	8	VBAT	Battery Supply
9	VBAT	Battery Supply	10	VBAT	Battery Supply
11	VBATX	Battery supply for peripherals	12	VBATX	Battery supply for peripherals

13	VBATX	Battery supply for peripherals	14	VBATX	Battery supply for peripherals
15	VRABB	Triton/Triton Lite LDO	16	VREXTL	Triton/Triton Lite LDO
17	VRABB	Triton/Triton Lite LDO	18	VREXTL	Triton/Triton Lite LDO
19	VRMEM	Triton/Triton Lite LDO	20	VREXTH	Triton/Triton Lite LDO
21	VRMEM	Triton/Triton Lite LDO	22	VREXTH	Triton/Triton Lite LDO
23	VRSIM	Triton/Triton Lite LDO	24	VRMMC	Triton/Triton Lite LDO
25	VRSIM	Triton/Triton Lite LDO	26	VRMMC	Triton/Triton Lite LDO
27	VRVBUS	Triton/Triton Lite LDO	28	VRPLL	Triton/Triton Lite LDO
29	VRVBUS	Triton/Triton Lite LDO	30	VRPLL	Triton/Triton Lite LDO
31	VRWLED	Triton/Triton Lite LDO	32	VRUSB	Triton/Triton Lite LDO
33	VRWLED	Triton/Triton Lite LDO	34	VRUSB	Triton/Triton Lite LDO
35	VRDBB	Triton/Triton Lite LDO	36	VRIO	Triton/Triton Lite LDO
37	VRDBB	Triton/Triton Lite LDO	38	VRIO	Triton/Triton Lite LDO
39	VBACKUP	Back up Battery Voltage	40	VRRTC	Triton/Triton Lite LDO
41	VBACKUP	Back up Battery Voltage	42	VRRTC	Triton/Triton Lite LDO
43	GND	Ground	44	GND	Ground
45	SIMDTC	SIM detection - Triton/Triton Lite	46	RPWON	Remote power on signal
47	GND	Ground	48	GND	Ground
49	LED_A	LED sink input - Triton/Triton Lite	50	PWON	Key power on signal (Triton/Triton Lite)
51	GND	Ground	52	GND	Ground
53	LED_B	LED sink input - Triton/Triton Lite	54	VIBDR	Vibrator motor driver (Triton/Triton Lite)
55	GND	Ground	56	GND	Ground
57	LED_C	LED sink input - Triton/Triton Lite	58	EXT_CLK_REQ_OU	Clock request input (Triton/Triton Lite)
59	GND	Ground	60	GND	Ground
61	Spare	Spare	62	PM_C	External power control
63	GND	Ground	64	BT_TX	BT UART TX (Ver. 2)
65	Spare	Spare	66	PM_C	External power control
67	Spare	Spare	68	BT_RTS	BT UART RTS (Ver. 2)
69	TESTRESET	Test reset signal (Triton/Triton Lite)	70	PM_F	External power control

71	Spare	Spare	72	BT_CTS	BT UART CTS (Ver. 2)
73	ADCIN1	Analog/Digital converter input	74	P2_INT2	Spare interrupt request
75	Spare	Spare	76	BT_RX	BT UART RX (Ver. 2)
77	ADCIN2	Analog/Digital converter input	78	P1_INT2	Interrupt request to LoCosto
79	Spare	Spare	80	Spare	Spare
81	ADCIN3	Analog/Digital converter input	82	REGEN	External regulator enable
83	Spare	Spare	84	GND	Ground
85	ADCIN4	Analog/Digital converter input	86	VAC	Charger input voltage (Triton/Triton Lite)
87	Spare	Spare	88	GND	Ground
89	ADCIN5	Analog/Digital converter input	90	PCHGAC	Pre charge input voltage
91	GND	Ground	92	GND	Ground
93	N/C	Not Connected	94	PCHGUSB	USB pre charge input voltage
95	GND	Ground	96	GND	Ground
97	PWROK	External power control	98	VCCS	Charge current sense
99	VMODE	External power control	100	GND	Ground
101	GND	Ground	102	ICTLUSB1	USB charge control
103	BM_SGMODE	Pre Charge Boot mode	104	ICTLUSB2	USB charge control
105	N/C	Not Connected	106	ICTLAC1	Normal charge control
107	N/C	Not Connected	108	ICTLAC2	Normal charge control
109	N/C	Not Connected	110	GND	Ground
111	USB_DP	USB data bus (positive)	112	G_EYE_SLEEP	GPIO 11 sleep control
113	USB_DM	USB data bus (negative)	114	GPIO_10	Spare GPIO and nEMU0
115	ID_USB	USB connector identity	116	N/C	Not Connected
117	VBUS	USB VBUS power supply	118	N/C	Not Connected
119	GND	Ground	120	GND	Ground
121	EARN	Earphone out negative	122	SPKPA	8 Ohm speaker amplifier
123	GND	Ground	124	GND	Ground
125	EARP	Earphone out positive	126	SPKNA	8 Ohm speaker amplifier
127	GND	Ground	128	GND	Ground

129	AUXO	Auxiliary Audio output	130	SPKPD	8 Ohm speaker amplifier
131	GND	Ground	132	GND	Ground
133	HSOL	Headset amplifier output	134	SPKND	8 Ohm speaker amplifier
135	GND	Ground	136	GND	Ground
137	HSOR	Headset amplifier output	138	MICIN	Mic. Amp. negative input
139	GND	Ground	140	GND	Ground
141	HSOVMID	Headset amplifier	142	MICIP	Mic. Amp. positive input
143	GND	Ground	144	GND	Ground
145	HSDET	Headset detection input	146	HSMIC	Headset mic. input
147	N/C	Not Connected	148	GND	Ground
149	TRITON_TMS	JTAG TMS (Triton)	150	MICBIAS	Microphone bias input
151	TRITON_TDI	JTAG TDI (Triton)	152	GND	Ground
153	TRITON_TDO	JTAG TDO (Triton)	154	HSMICBIAS	Headset microphone bias
155	TRITON_TCK	JTAG TCK (Triton)	156	GND	Ground
157	TMS	JTAG TMS (LoCosto)	158	AUXI_FMR	FM radio audio input right
159	GND	Ground	160	GND	Ground
161	TDI	JTAG TDI (LoCosto)	162	AUXI_FML	FM radio audio input left
163	GND	Ground	164	GND	Ground
165	TDO	JTAG TDO (LoCosto)	166	nEMU1	Emulation access pin 1
167	GND	Ground	168	GND	Ground
169	RTCK	JTAG RTCK (LoCosto)	170	nEMU0	Emulation access pin 2
171	GND	Ground	172	GND	Ground
173	TCK	JTAG TCK (LoCosto)	174	3_3V_AUX	External 3.3V regulator
175	GND	Ground	176	3_3V_AUX	External 3.3V regulator
177	2_8V_AUX	External 2.8V regulator	178	1_8V_AUX	External 1.8V regulator
179	2_8V_AUX	External 2.8V regulator	180	1_8V_AUX	External 1.8V regulator

2.17 VISU Board

The VISU plug-in board is designed to provide easy access to all the signals on the I Sample expansion connector. The VISU board provides complete access to the

JTAG and emulation signals and has a separate connector for access to debug signals. A Mictor connector has been added for connection to a logic analyzer pod that is compatible with previous Sample boards. 3 LEDs are available and connected to spare or unused GPIOs for use by software engineers for debugging.

Note:

Currently two revisions of the VISU board have been made. The VISU board revision 1 pin header pitch is 1.27 whereas the pin header pitch on VISU board revision 2 is 2.54 mm. Furthermore, VISU board revision 2 includes 3 LEDs for debug purposes. The three LEDs have been connected individually to GPIO_1, GPIO_10, and GPIO_35.

The pin outs of all the VISU board signals are listed in Table 2-19 through Table 2-26.

Table 2-19. Pin configuration of J103.

Pin #	Name	Pin #	Name
1	KBC4	2	KBR4
3	KBC3	4	KBR3
5	KBC2	6	KBR2
7	KBC1	8	KBR1
9	KBC0	10	KBR0
11	GND	12	GND
13	I2C_1_SDA	14	I2C_2_SDA
15	I2C_1_SDA	16	I2C_2_SCL
17	GND	18	GND
19	SPI_MOSI	20	TSPACT8
21	SPI_MISO	22	TSPACT10
23	SPI_CLK	24	TSPACT11
25	SPI_nCS0	26	TSPACT12
27	SPI_nCS1	28	TSPACT13
29	GND	30	TSPACT14
31	SYS_RESET	32	TSPACT15
33	GND	34	GND
35	BT_AUD_CLK	36	APC_OUT
37	BT_AUD_OUT	38	GND
39	BT_AUD_IN	40	USIM_RST
41	BT_AUD_FSYNC	42	USIM_CLK
43	BT_RTS/UART2_RTS/SD_IRDA	44	USIM_IO
45	BT_CTS / UART2_CTS	46	USIM_PW_CTRL

47	BT_RX / UART2_RX	48	USIM_PBIAS
49	BT_TX / UART2_TX	50	Key Pin

Table 2-20. Pin configuration of J104.

Pin #	Name	Pin #	Name
1	GND	2	GND
3	CAM_XCLK	4	LCD_nCS0
5	CAM_LCLK	6	LCD_RS
7	CAM_VS / CAM_D2	8	LCD_RnW
9	CAM_HS	10	LCD_ESTRB
11	CAM_PWDN/G_EYE_INT_LTOG	12	LCDnRST
13	GND	14	GND
15	PERIPHERAL_INTERFACE0	16	ND_WE
17	PERIPHERAL_INTERFACE1	18	ND_nWP / CAM_D4
19	PERIPHERAL_INTERFACE2	20	ND_CE1
21	PERIPHERAL_INTERFACE3	22	ND_RnB
23	PERIPHERAL_INTERFACE4	24	ND_ALE
25	PERIPHERAL_INTERFACE5	26	ND_CLE
27	PERIPHERAL_INTERFACE6	28	ND_RE
29	PERIPHERAL_INTERFACE7	30	N/C
31	GND	32	N/C
33	DLATCH0	34	DLATCH1
35	DLATCH2	36	DLATCH3
37	DLATCH4	38	DLATCH5
39	DLATCH6	40	DLATCH7
41	DLATCH8	42	DLATCH9
43	DLATCH10	44	DLATCH11
45	DLATCH12	46	DLATCH13
47	DLATCH14	48	DLATCH15
49	GND	50	Key Pin

Table 2-21. Pin configuration of J105.

Pin #	Name	Pin #	Name
1	GND	2	GND

3	EARN	4	SPKPA
5	EARP	6	SPKNA
7	GND	8	SPKPD
9	AUXO	10	SPKND
11	GND	12	GND
13	HSOL	14	MICIN
15	HSOR	16	MICIP
17	GND	18	GND
19	HSOVMID	20	HSMIC
21	HSDET	22	MICBIAS
23	GND	24	HSMICBIAS
25	VAC	26	GND
27	GND	28	AUXI_FMR
29	PCHGAC	30	AUXI_FML
31	GND	32	GND
33	PCHGUSB	34	USB_DP
35	GND	36	USB_DM
37	VCCS	38	ID_USB
39	GND	40	VBUS
41	ICTLUSB1	42	USB_SE0
43	ICTLUSB2	44	USB_DATA
45	ICTLAC1	46	USB_TXEN
47	ICTLAC2	48	USB_RCV
49	GND	50	Key Pin

Table 2-22. Pin configuration of J106.

Pin #	Name	Pin #	Name
1	GND	2	GND
3	DATA / ADD0	4	DATA / ADD1
5	DATA / ADD2	6	DATA / ADD3
7	DATA / ADD4	8	DATA / ADD5
9	DATA / ADD6	10	DATA / ADD7
11	DATA / ADD8	12	DATA / ADD9
13	DATA / ADD10	14	DATA / ADD11
15	DATA / ADD12	16	DATA / ADD13

17	DATA / ADD14	18	DATA / ADD15
19	ADD16	20	ADD17
21	ADD18	22	ADD19
23	ADD20	24	ADD21
25	ADD22	26	BT_nSHUTDOWN
27	GND	28	GND
29	RnW	30	nBHE
31	nBLE	32	nMOE
33	nFWP / CAM_D2	34	FDP
35	nRDYMEM	36	nFADV
37	nCS0	38	IRDA_SD / nCS1
39	LED_TRCH / nCS2	40	nCS3
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	GND	50	Key Pin

Table 2-23. Pin configuration of J107.

Pin #	Name	Pin #	Name
1	GND	2	GND
3	VBAT	4	VBAT
5	VBAT	6	VBAT
7	VBATX	8	VBATX
9	VBATX	10	VBATX
11	N/C	12	N/C
13	VRABB	14	VREXTL
15	VRMEM	16	VREXTH
17	VRSIM	18	VRMMC
19	VRVBUS	20	VRPLL
21	VLED	22	VRUSB
23	VRDBB	24	VRIO
25	VBACKUP	26	VRRTC
27	N/C	28	N/C

29	1.8V_AUX	30	Spare
31	2.8V_AUX	32	Spare
33	3.3V_AUX	34	Spare
35	N/C	36	Spare
37	Spare	38	Spare
39	Spare	40	Spare
41	Spare	42	Spare
43	Spare	44	Spare
45	Spare	46	GND
47	GND	48	GND
49	GND	50	Key Pin

Table 2-24. Pin configuration of J108.

Pin #	Name	Pin	Name
1	GND	2	GND
3	GND	4	GND
5	SIMDTC	6	RPWON
7	LED_A	8	PWON
9	LED_B	10	GND
11	LED_C	12	VIBDR
13	GND	14	GND
15	ADCIN1	16	EXT_CLK_REQ_OUT
17	ADCIN2	18	GND
19	ADCIN3	20	PM_D
21	ADCIN4	22	PM_C
23	ADCIN5	24	PM_F
25	GND	26	GND
27	PWROK	28	P2_INT2
29	VMODE	30	P1_INT2
31	GND	32	GND
33	BM_SIGMODE	34	REGEN
35	GND	36	GND
37	GND	38	GND
39	CLK32K	40	CKOUT_13Mhz
41	GND	42	GND

43	CAM_D1 / DCD_TXIR / GPIO_0	44	G_EYE_SLEEP
45	CAM_D0 / DSR_RXIR / GPIO_47	46	GPIO_10
47	GND	48	GPIO_1
49	GND	50	Key Pin

Table 2-25. Pin configuration of J109.

Pin #	Name	Pin #	Name
1	GND	2	GND
3	DTS0	4	GND
5	DTS1	6	DTS17
7	DTS2	8	DTS18
9	DTS3	10	DTS19
11	DTS4	12	DTS20
13	DTS5	14	DTS21
15	DTS6	16	DTS22
17	DTS7	18	DTS23
19	DTS8	20	DTS24
21	DTS9	22	DTS25
23	DTS10	24	DTS26
25	DTS11	26	DTS27
27	DTS12	28	DTS28
29	DTS13	30	DTS29
31	DTS14	32	DTS30
33	DTS15	34	DTS31
35	DTS16	36	RX_START
37	GND	38	drp_dbb_scmdaccpt1
39	TRITON_TMS	40	CLK1
41	TRITON_TDI	42	drp_dbb_rx_req
43	TRITON_TDO	44	TPU_FRAME_INT
45	TRITON_TCK	46	GND
47	GND	48	GND
49	GND	50	Key Pin

Table 2-26. Pin configuration of J110.

Pin #	Name	Pin #	Name
1	TMS	2	TRSTN
3	TDI	4	GND
5	VRIO	6	N/C
7	TDO	8	GND
9	RTCK	10	GND
11	TCK	12	GND
13	nEMU0	14	nEMU1

Chapter 3

Mechanical

In this chapter the physical placements of the I-Sample components are shown.

3.1 Functional View of I-Sample 1.1 – Front View

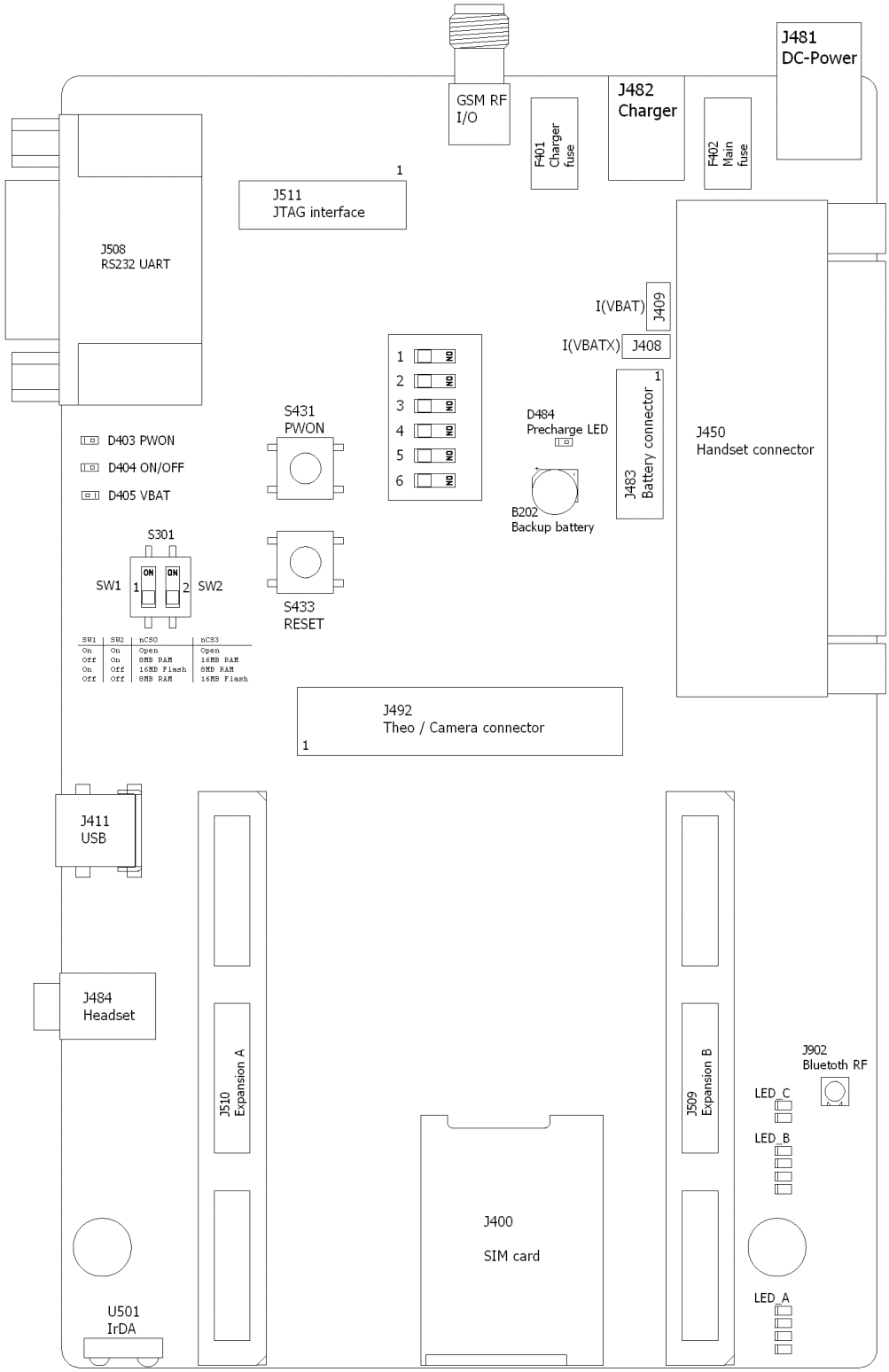


Figure 3-22. Functional View of I-Sample 1.1 - front view.

3.2 Functional View of I-Sample 1.1 – Back View

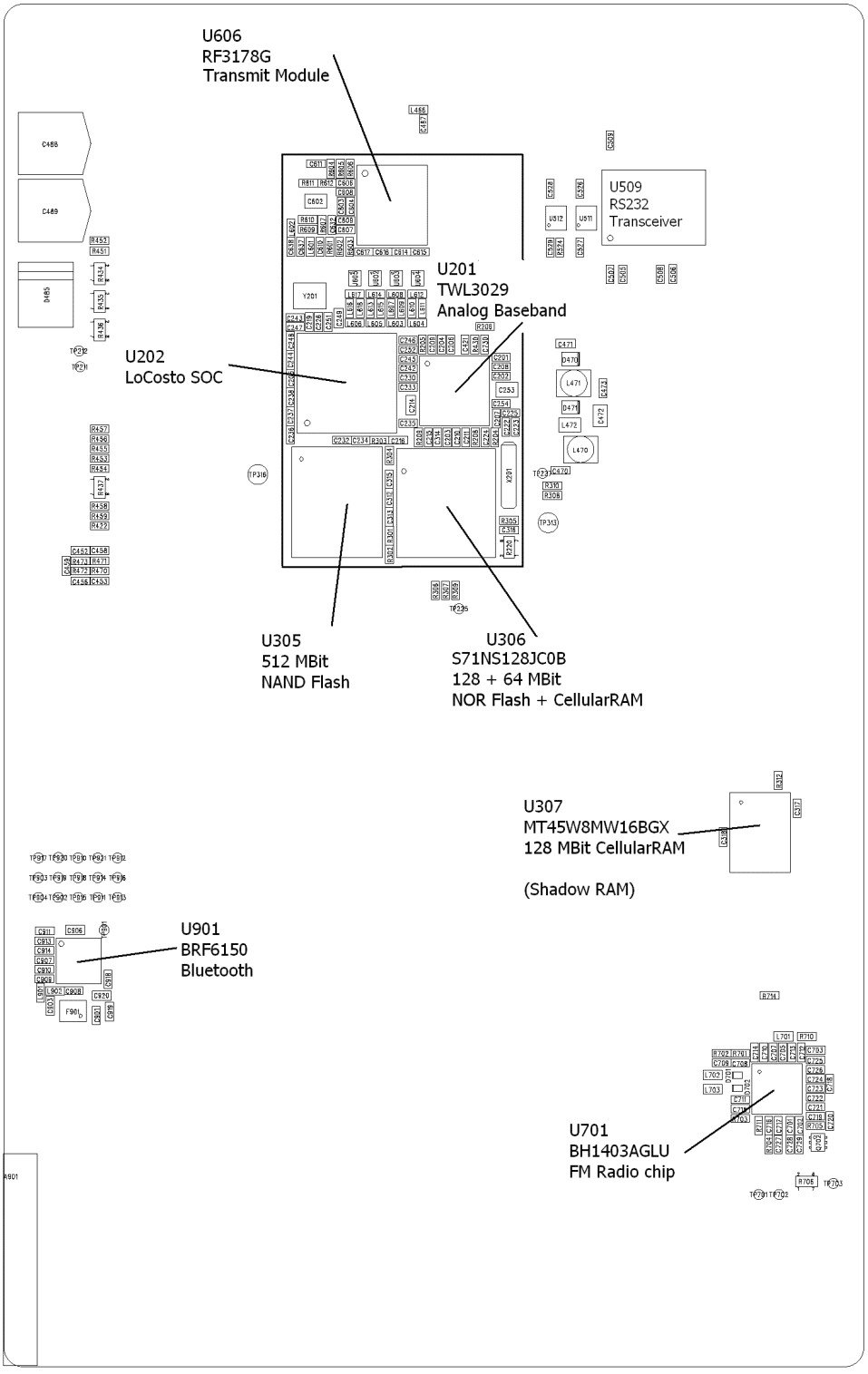


Figure 3-23. Functional view of I-Sample 1.1 back view.

Chapter 4

Accessories

A number of accessories are available for the I-Sample board. The accessories are to be attached to the I-Sample using the wide range of onboard connectors.

4.1 Handset

The I-Sample board user interface is implemented as a handset that connects to the I-Sample board via a cable.

4.1.1 Features

The handset provides basic functionality that corresponds to what can be found in a standard cellular telephone. The features of the handset are listed in Table 4-1:

Table 4-1. Features of the handset.

Handset part	Functionality	Description
Display	Technology	Philips Active Matrix LCD
	Pixels	Width: 176 × Height: 220 = 38720 pixels
	Colours	RGB 5.6.5 (16 bits)
	Dimension	2.2” Active area
Keypad	Keys	26 keys (3 sidekeys, 4 softkeys, 1 hook-on key, 1 hook-off key, 5 navikeys, and 12 standard numeric telephony keys)
Microphone	Type	Electret microphone
Speaker	Operation	Transducer implemented to operate both as melody speaker (optional) and earpiece. Baffled by integration into the mechanics
	Impedance	8 Ohm ± 1.2 Ohm
	Bandwidth	5 kHz
Directional control	Yes	4-way digital joystick with integrated z-direction button (5 switch states)

The handset that is available for the I-Sample board is shown in Figure 4-24.

Figure 4-24. Handset for the I-Sample board.

4.1.2 Keypad Matrix

The keypad in the handset is based on a 5×5 keypad matrix. This allows 25 buttons to be routed to the I-Sample board by asserting a row signal and a column signal. The last button is assigned to PWON. In Table 4-2 is shown the keypad matrix and which button that depends on which of the rows/columns.

The row and column signals of the keypad matrix are routed through the handset connector. For a pin description see Section 4.1.3. Furthermore, these signals are also available on the expansion connectors.

Table 4-2. Keypad matrix with associated key mapping.

	KBC 0	KBC 1	KBC 2	KBC 3	KBC 4
KBR 0	Home	Back	Soft 1	Soft 2	Up
KBR 1	1	2	3	Send	Right
KBR 2	4	5	6	End	Left
KBR 3	7	8	9	Vol –	Down
KBR 4	*	0	#	Vol +	Center

4.1.3 Handset Connector

The external handset is to be plugged into a 44-pin D-SUB connector (J450) present in the upper right corner of the I-Sample board. This connector provides all signals needed for the keypad, audio, and the LCD display (8 bit parallel interface). The connector, J450, is shown in Figure

4-25 and a description of each of the 44 available pins can be found in Table 4-3.

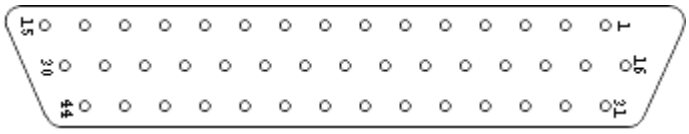


Figure 4-25. The 44 pin handset connector.

Table 4-3. Description of the pins on the handset connector.

Pin	Name	Function
1	VIBDR	Vibrator enable
16	LCDnRST	Reset of LCD
31	GND	GND
2	LCD_RS	Address #1 (Register select)
17	LCD_ESTRB	Read strobe
32	VRIO	1.8V I/O supply
3	LCD_RnW	Write strobe
18	LCD_nCS0	Chip select
33	LCD_D0	Data bit #0
4	LCD_D1	Data bit #1
19	LCD_D2	Data bit #2
34	LCD_D3	Data bit #3
5	LCD_D4	Data bit #4
20	LCD_D5	Data bit #5
35	LCD_D6	Data bit #6
6	LCD_D7	Data bit #7
21	GND	GND
36	GND	GND
7	GND	GND
22	GND	GND
37	GND	GND
8	GND	GND

Pin	Name	Function
23	GND	GND
38	GND	GND
9	VBATX	Battery voltage (for backlight power)
24	2_8V_AUX	2.8V auxiliary voltage (for LCD power)
39	GND	GND
10	KBR0	Keyboard row input #0
25	KBR1	Keyboard row input #1
40	KBR2	Keyboard row input #2
11	KBR3	Keyboard row input #3
26	KBR4	Keyboard row input #4
41	KBC0	Keyboard column output #0
12	KBC1	Keyboard column output #1
27	KBC2	Keyboard column output #2
42	KBC3	Keyboard column output #3
13	KBC4	Keyboard column output #4
28	PWON	Power ON key (active low)
43	HS_PWL	Backlight control
14	EARN	Negative speaker terminal (32 Ohm differential drive)
29	EARP	Positive speaker terminal (32 Ohm differential drive)
44	GND	Ground (audio shielding)
15	MICIP	Microphone positive signal (differential input)
30	MICIN	Microphone negative signal (differential input)

The speaker is driven by the EARP/EARN-outputs on the analog baseband. A 12 ohm resistor is connected in series with both EARP and EARN to match the output impedance of Triton/Triton Lite.

The microphone is connected to the MICIP/MICIN inputs on the analog baseband.

4.2 Stereo Headset

I-Sample is delivered with a stereo headset with microphone and pushbutton.

4.2.1 Features

The headset is suitable for hands-free telephony and stereo-audio listening (FM Radio or MP3).

Table 4-4. Headset features.

Part	Description
Left and right earpiece	Impedance 150 ohm each
Microphone	Electret type
Button	Hook-on / hook-off. Connected in parallel with microphone.
Connector	2.5mm 3-pin jack with additional 4th contact implemented as a collar ring.

4.2.2 Electrical implementation

Figure 4-26 shows the electrical connections of the headset.

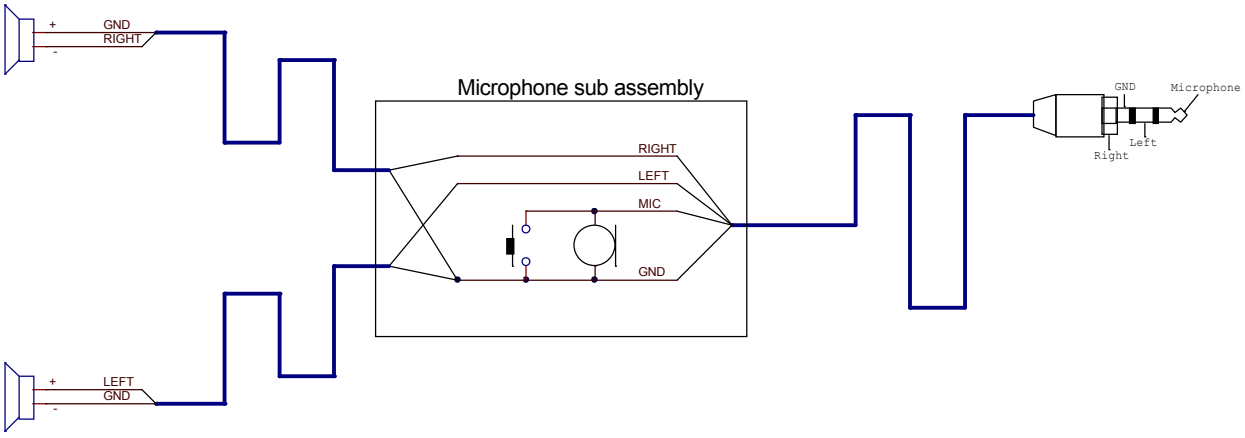


Figure 4-26. Stereo headset principal schematic.

As shown in Figure 4-26 the left and right earphones are connected out-of-phase. The reason for this is to avoid earphone-to-microphone cross-talk caused by ground current. When the current into each earpiece is of opposite polarity the resulting ground current will be virtually zero. This dramatically reduces echo problems when the headset is used for hands-free.

Any stereo audio applications (e.g. MP3) must invert one channel to make sure the perceived stereo perspective is correct.

4.3 Battery

A battery is available for the I-Sample for e.g. development and test of charging algorithms.

Table 4-5. Battery features

Parameter	Description
Type	Li-Ion battery
Capacity	600mAh nominal
Voltage	3.20 – 4.20 V
Safety	Integrated over-current and over-voltage protection circuitry.

The battery can be ordered separately.

Li-Ion batteries contain lithium which is a highly reactive metal. It may explode or burst into fire if not treated correctly.

Never disassemble, over-charge or over-discharge a Li-Ion battery.

WARNING

4.4 Charger

I-Sample is fitted with a standard DC jack socket for interfacing to a charger device (see Table 4-6).

The connector is compatible with a number of commercially available charger devices.

Table 4-6. Charge DC jack socket dimensions.

Parameter	Description
Centre pin	Positive terminal. Dimension = Ø 1mm
Outer ring	Ground terminal. Dimension = Ø 3.8mm

I-Sample can be used with both low-cost non-regulated chargers (transformer + rectifier only) and regulated travel chargers (DC-DC converter).

I-Sample supports several methods of charging:

- For low-cost charger devices a pulsed-charging algorithm can be used. This minimizes the power dissipation on the board.

- For regulated charger devices a linear charging algorithm can be used. The charger device must be 5 V to limit the power dissipation on board if linear charging is used.

The recommended charger device is Nokia ACP-7 or similar low-cost non-regulated chargers.

The charge FET on the board is capable of dissipating up to 1.5 W at room temperature.

Absolute maximum voltage allowed on the charge connector is 20 V.

Never exceed the power dissipating capabilities of the charge circuitry or the board could be damaged.

WARNING

4.5 DC Power supply

I-Sample is delivered with a 5V/4.5 A power supply supporting 110-240 V input range. The supply is connected using a DC jack. Centre pin is positive.

Two different power supplies are available:

- Power supply with ground connection (main power cable is fitted with three pins – phase, null, and earth).
- Power supply without ground connection (main power cable is fitted with two pins – phase and null).

The ground connection ensures that the ground potential of the board is at same level as any instruments or computers used in conjunction with the board. This minimizes the risk of electrically overstressing the board or attached equipment.

Take the following precautions in case you received a power supply without ground connection:
Plug-in all other cables and connectors to the board before the power-supply is connected.

The board or equipment can be damaged if this precaution is not followed.

CAUTION

Chapter 5

Compliance Testing

In order to validate the I-Sample Reference Design Platform (RDP) and prepare for FTA (Full Type Approval) conformance testing has been carried out on the I-Sample platform. The test results will be valid for custom designs provided that no changes have been made to the modem part of the RDP, which means customers can limit the amount of necessary testing needed to pass FTA and significantly expedite the FTA process.

Since I-Sample is a Quadband platform FTA testing has been carried out in accordance with the 3GPP 51.010-1 standard under both the GCF-CC (Global Certification Forum - Conformance Criteria) regime and the PTCRB NAPRD03 regime. Current revisions of all standards have been used.

The tests are listed in this chapter but not discussed in detail. Full test reports are available from Texas Instruments upon request.

Topic **Page**

5.1 GSM RF

The GSM RF module on the I-Sample has been verified to be fully operational and that it complies with the conducted part of 3GPP 51.010. Calibration and test procedures are listed in the next sections but not explained in detail. For more information about these the reader is referred to the latest version of the document "i_sample_rf_test_and_calibration_13_03_04_01991".

5.1.1 Calibration

The GSM RF hardware must be calibrated before performing the actual compliance tests. The following calibration procedures were performed:

- DCXO Calibration
- TX Power Calibration
- TX Power Versus Channel Compensation
- AGC Calibration
- RX RSSI Channel Compensation
- Temperature Sensor Calibration
- Battery Sensor Calibration

5.1.2 Compliance Tests

Part of the compliance testing is verification of the combination of RF hardware and software. The tests performed on the I-Sample are listed below.

- TX test and adjustment for bands GSM850, EGSM900, DCS1800, and PCS1900
- RX test and adjustment for bands GSM850, EGSM900, DCS1800, and PCS1900
- Loop back tests for bands GSM850, EGSM900, DCS1800, and PCS1900
- Co-existence test between Bluetooth and the GSM bands GSM850, EGSM900, DCS1800, and PCS1900

5.2 Bluetooth RF

The Bluetooth RF module of the I-Sample has been verified to be fully operational and is conforming to the standard Bluetooth specification 1.1 defined by the Bluetooth Special Interest Group (SIG). The test specifications can be found in the document TS_A_RF_XXX_,pdf where XXX is substituted with the newest revision number.

5.2.1 Calibration

Before performing the compliance tests the step size of the power control must be calibrated. The step size can be considered calibrated if it is between 2 dB and 8 dB.

5.2.2 Compliance Tests

Due to the complexity of the Bluetooth RF transceiver many different parameters must be performing within a given margin. A list of the parameters that are included in the compliance tests is shown below:

- Output Power
- Power Density
- Power Control
- TX Output Spectrum – Frequency range
- TX Output Spectrum – 20 dB Bandwidth
- TX Output Spectrum – Adjacent channel power
- Modulation Characteristics
- Initial Carrier Frequency Tolerance
- Carrier Frequency Drift
- Out-of-Band Spurious Emissions
- Sensitivity – Single Slot Packets
- Sensitivity – Multi Slot Packets
- C/I Performance
- Blocking performance
- Intermodulation Performance
- Maximum Input Level

For a description of the individual tests the reader is refered to the document mentioned in Section 5.2.

5.3 Quality Assurance and Quality Control

Quality Assurance (QA) and Quality Control (QC) tests have not been performed on the I-Sample board. These tests are expected to be performed on the end product and should as a minimum include:

- GSM850/EGSM900/DCS1800/PCS1900 GPRS (Class 12) performance tests – normal and extreme conditions
- Antenna test – check that performance on internal antenna conforms to specifications

- Acoustic test – check that transducers are mounted properly in the mechanics
- Visual quality tests – check for scratches, gaps in plastic parts, display, etc.

Chapter 6

Power Consumption Measurements

One of the most critical parameters in cellular phone designs is the overall power consumption. In order to increase the time a battery can supply the cellular phone this parameter must be optimized to draw as little current as possible. In this chapter, methods for measuring the power consumption of the I-Sample board are presented.

Techniques are based on PRD TW.09 measurements to GSM Association/ECTEL Battery Life Measurement Technique Document.

Topic	Page

6.1 Electrical considerations

I-Sample includes a number of components that are not considered part of the reference design. These components include parts such as RS232 UART transceiver, JTAG level shifter etc.

When measuring power consumption it is important to disregard the consumption of these peripheral devices and only focus on the actual reference design core. To support this power distribution on the board is split into two parts; one for the reference design core and another for the debug peripherals.

All blocks in the reference design core are powered by the “VBAT” rail and all other blocks are powered by the “VBATX” rail. VBAT and VBATX can be accessed by means of two jumpers, J409 and J408. This means that when optimizing the consumption of the reference design only the portion of power that flows through J409 is of interest.

6.2 Procedure

In modern cellular phone designs, the power levels are varying over time. This means that it is not enough to measure the current consumption by use of a simple Ampere meter. Therefore, a device that can record the current at discrete time intervals and then calculate the average is necessary. An example of a power measurement setup could involve the following components:

- A standard PC with dedicated software
- An Analog to Digital Converter (ADC)
- A shunt resistor

A setup using these components is shown in Figure 6-27.

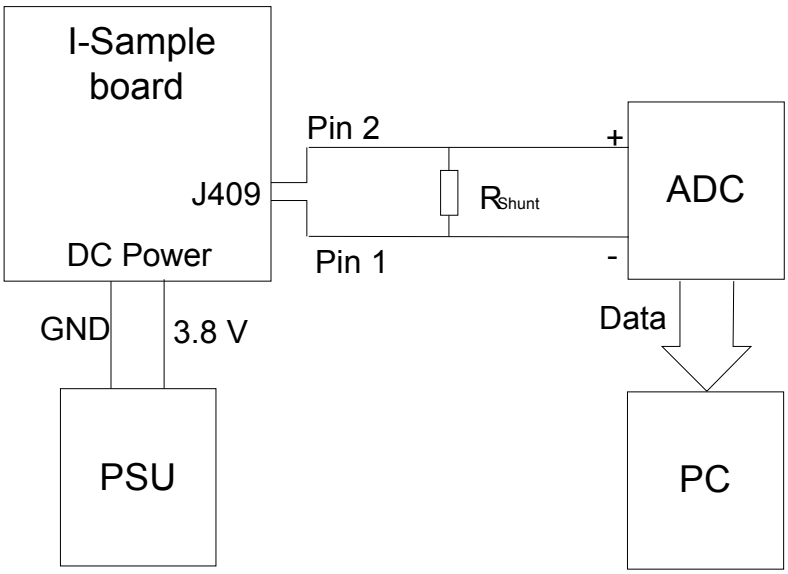


Figure 6-27. Power measurement example.

In this setup a 3.8 V power supply is connected to the main power input jack on the I-Sample board in order to establish a fixed voltage. The jumper J409 has been removed from the I-Sample board and the two exposed pins are connected directly in shunt with resistor $R_{Shunt.}$ R_{Shunt} must be a 1 %, 0.5 W, high precision metal film resistor and its value should be selected to conform to one of the two current modes suggested by ECTEL:

- Idle mode setting: R_{Shunt} = 0.5 Ohm
- Dedicated mode setting: R_{Shunt} = 0.1 Ohm

The positive and negative terminals of the ADC are then connected to each side of R_{Shunt}. This configuration allows the voltage drop of R_{Shunt} to be sampled at discrete intervals. According to ECTEL the samplerate of the ADC must be set to 50.000 samples per second.

The sampled data is transferred to a PC where the sampled voltage drops are converted into discrete current values and then averaged over time.

For the idle mode test it is recommended that the test period is 30 min (90 M samples) and for the dedicated power mode the test period should be 10 min (30 M samples).

Chapter 7

Daughterboards

In this chapter a list of the currently available daughter boards can be found.

7.1 I-Camera 1 Board

The I-Camera 1 camera board fits into the I-Sample camera connector (J492) described in Section 2.15.3. The camera sensor used with the I-Camera 1 board is the Agilent ADCM 2700 which provides the following features:

- 640 x 480 Landscape VGA Resolution
- Command Interface Via I²C Bus
- 24 Bit Colour Depth (16.7 Million Colours)
- 15 Frames per Second
- 70 mW Active Power Consumption Using 13 MHz Input Frequency
- 1.5 µA Standby Current Consumption

Since the ADCM 2700 sensor is designed to interface with a 2.8 V camera interface level shifting components must be attached in between the LoCosto and the camera sensor.

The level converters provide one more important function besides translating voltage levels. The pins for the LoCosto data bus are not only used by the camera but also other functional units. Therefore, during initialization of the LoCosto chip the camera bus signals must be set into high impedance mode. Unfortunately the ADCM camera module does not provide such functionality which is why the level shifters must provide this option.

Disregarding the level shifting components Table 7-7 lists the pin connections from the ADCM camera module through the camera connector to the LoCosto digital baseband.

Table 7-7. I-Camera 1 add-on board connections.

LoCosto		**Camera Connector**	**ADCM 2700**	
Pin #	**Pin Name**	**Pin #**	**Pin #**	**Pin Name**
----	Common Ground	1,2,7,8,13,14,34, 51,52,55,59,60	1	AGND
C6	CAM_XCLK	57	2	CLKIN
E7	CAM_VS/CAM_D3	56	3	VSYNC
M6	CAM_D0/DSR_RXIR/GPIO_47	36	4	D0
N5	CAM_D1/DCD_TXIR/GPIO_0	38	5	D1
G6	nFWP/CAM_D2	40	6	D2
E7	CAM_VS/CAM_D3	42	7	D3
E5	ND_nWP/CAM_D4	44	8	D4

LoCosto		Camera Connector	ADCM 2700	
Pin #	**Pin Name**	**Pin #**	**Pin #**	**Pin Name**
B3	CAM_D5	46	9	D5
G7	CAM_D6	48	10	D6
C4	CAM_D7	50	11	D7
A5	CAM_LCLK	58	12	VCLK
F8	CAM_HS	54	13	HSYNC
----	Not Connected	---	14	TEST
R4	I2C_2_SCL	18	15	SCLK
N6	I2C_2_SDA	20	16	SDATA
----	2_8V_AUX (LDO)	23	17	VDD
----	Common Ground	1,2,7,8,13,14,34, 51,52,55,59,60	18	GND

The physical placement of the components onto the I-Camera 1 board is shown in Figure 7-28.

A 4 layer PCB is used for the base of the camera board design and all components are placed on the same side as where pin 1 of the I-Sample camera board connector is located. The two regulators, U4 and U10, are left as not mounted but the chosen package type makes it easy to hand solder them if needed at a later time. The surface mounted terminal strips J4 and J5 have also been left as not mounted. However, their footprints provide large accessible pads which can be used as test points.

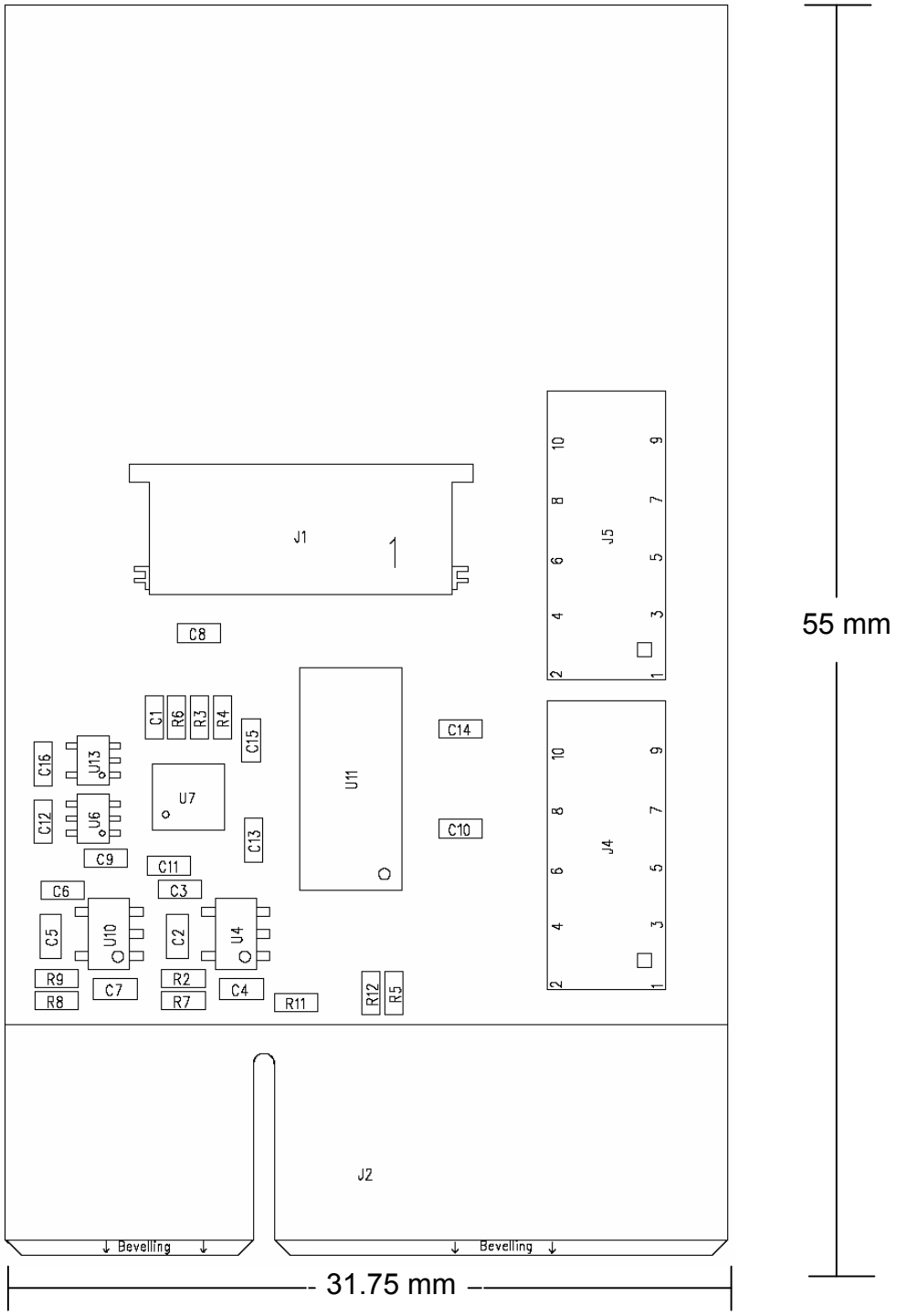


Figure 7-28. The I-Camera 1 add-on board for the I-Sample.

7.2 I-Camera 2 Board

TBD

Appendix A

Glosary

In this appendix an abbreviation table has been provided.

Table 7-8. Abbreviation table.

Abbreviation	Meaning
ADC	Analog to Digital Converter
APC	Automatic Power Control
BGA	Ball Grid Array
BOM	Bill Of Materials
BT	BlueTooth
DRP	Digital Radio Processor
DSP	Digital Signal Processor
DAC	Digital to Analog Converter
EAC	Enhanced Audio Controller
EMIFF	Enhanced Memory Interface Fast
FTY	Final Test Yield
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
I²C	Inter IC
I²S	Inter IC Sound
IC	Integrated Circuit
IF	InterFace
IrDA	Infrared Data Association
JTAG	Joint Test Action Group

Abbreviation	Meaning
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MMC	MultiMedia Card
MPU	MicroProcessor Unit
NTC	Negative Temperature Coefficient
OTG	On-The-Go
PA	Power Amplifier
PDA	Personal Digital Assistant
PGA	Programmable Gain Amplifier
PISO	Parallel In Serial Out
PLL	Phase Locked Loop
PM	Power Management
PRD	Product Requirements Document
PWON	Power On
RGB	Red Green Blue
RS-232	Recommended Standard 232
RTC	Real Time Clock
SIM	Subscriber Identification Module
SIPO	Serial In Parallel Out
SPI	Serial Port Interface
TDM	Time Division Multiplex
TFD	Thin Film Diode
TFT	Thin Film Transistor
TTY	Tele Typewriter
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver Transmitter
VSP	Voice Serial Port