Making Wireless — Making 3G

# Locosto DRP

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# Locosto DRP

- DRP2.0 Overview
- Receiver
- LO, Synthesis and Transmitter
- DCXO
- DRP LDOs and Power Management
- APC
- AGC
- Clock management
- Script Processor and SRM
- DRP Wrapper
- DRP Timings

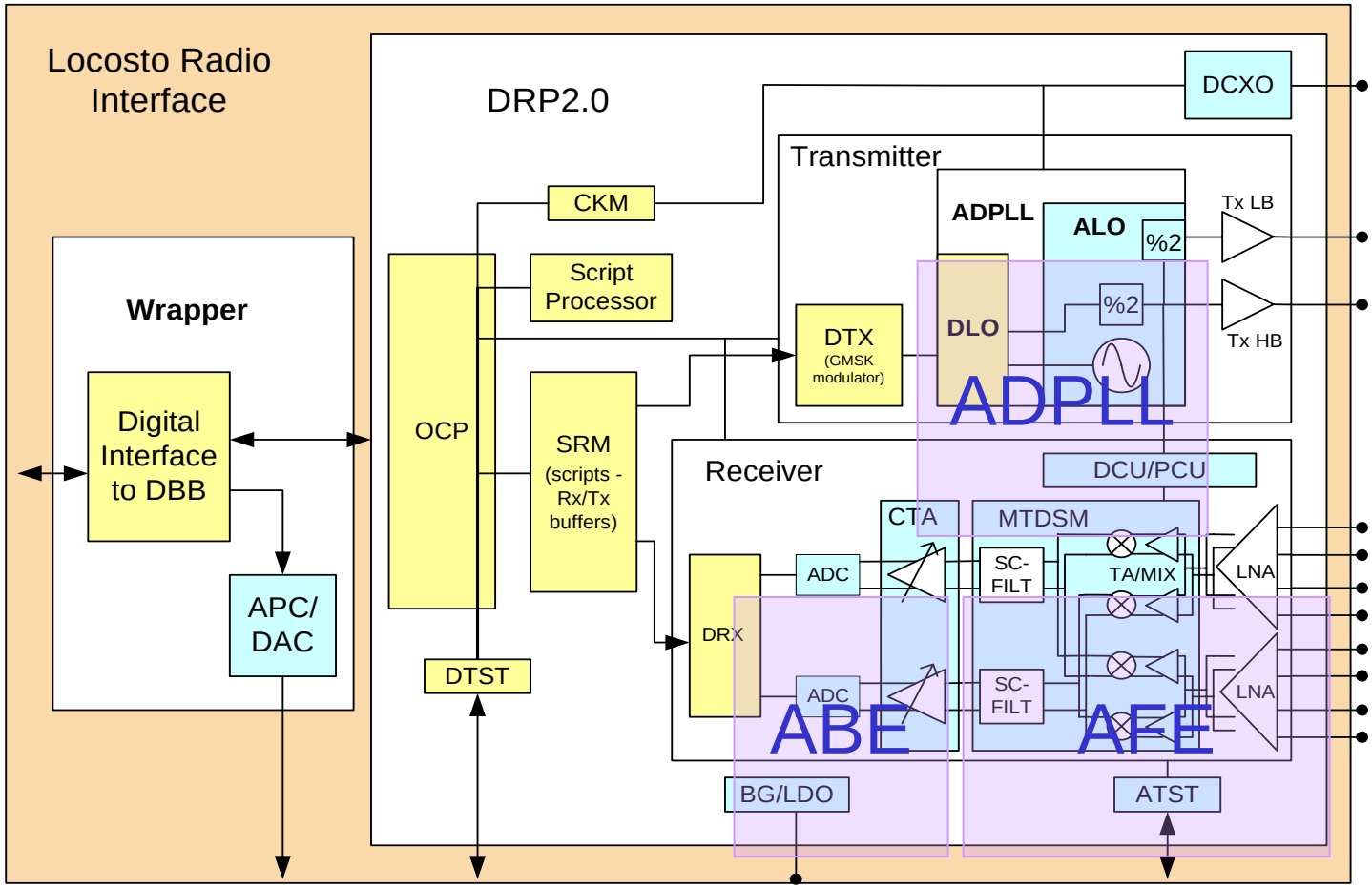
# Digital RF Processor

# Overview

# DRP summary

- Locosto DRP is a fully integrated 4 band GPS/GPRS transmitter
- The DRP technology enables software definable radio (SDR)
- This technology allows cost effective integration of the radio function
- **TI Digital Radio Processor (DRP)** is a complete Radio subsystem including:
  - Frequency synthesizer: ADPLL
    - Digitally Controlled Oscillator (DCO)
    - Digital loop filter and phase detector
    - Reduced Lock Time (Loop BW adaptation)
  - Transmitter:
    - Based on ADPLL
    - Digitally self-calibrated two-point modulation
  - Receiver:
    - Configurable to zero IF or near zero IF
    - MTDSM (multi-tap-direct-sampling-mixer)
    - LO generated by ADPLL
  - Digital Interface with Baseband
  - Power management and start up engine (On-chip Bandgap + LDOs)
  - Clock management (DCXO) with clock noise reduction by retiming
  - Software script processor for transceiver sequencing and calibration

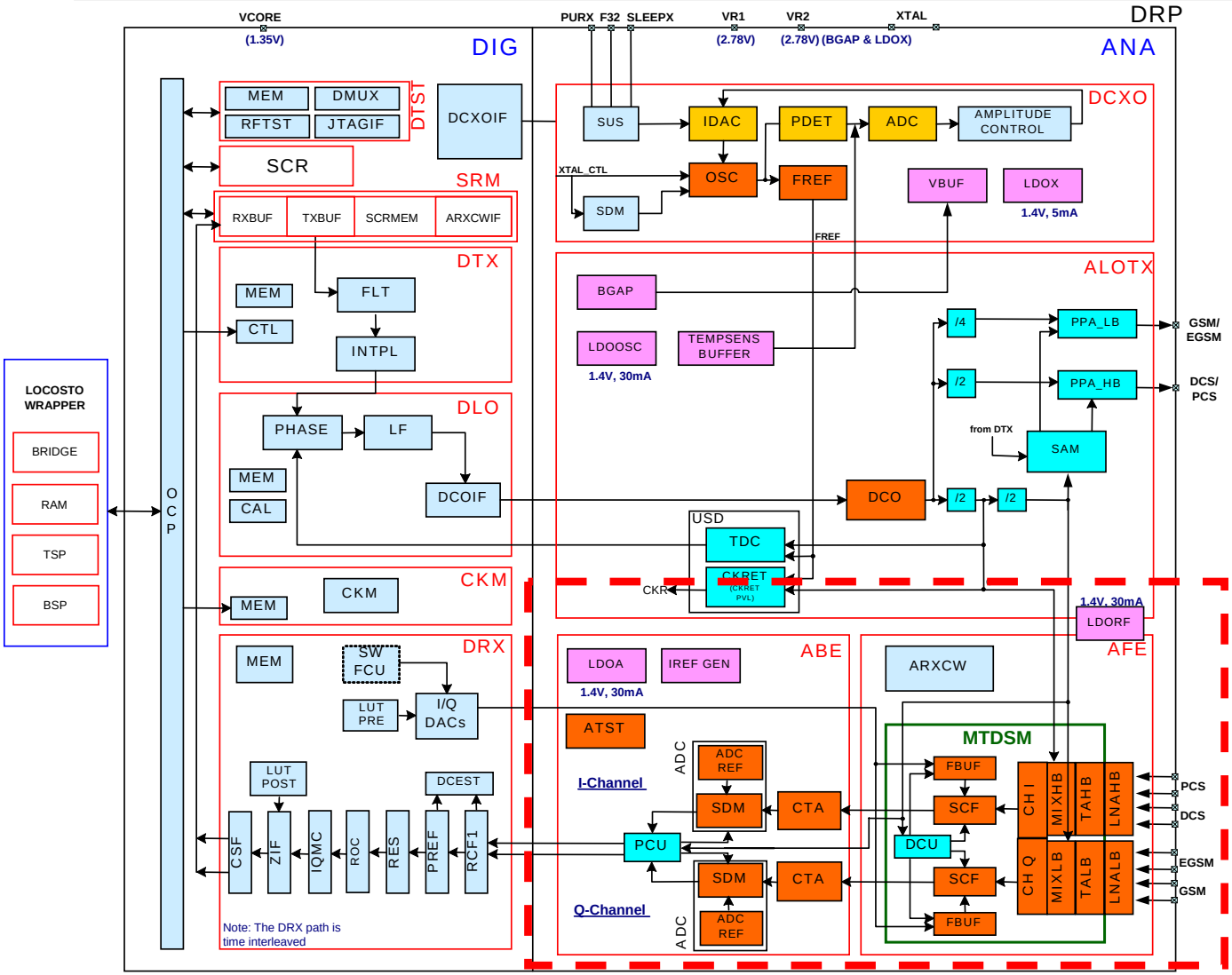
# Radio Interface Block Diagram



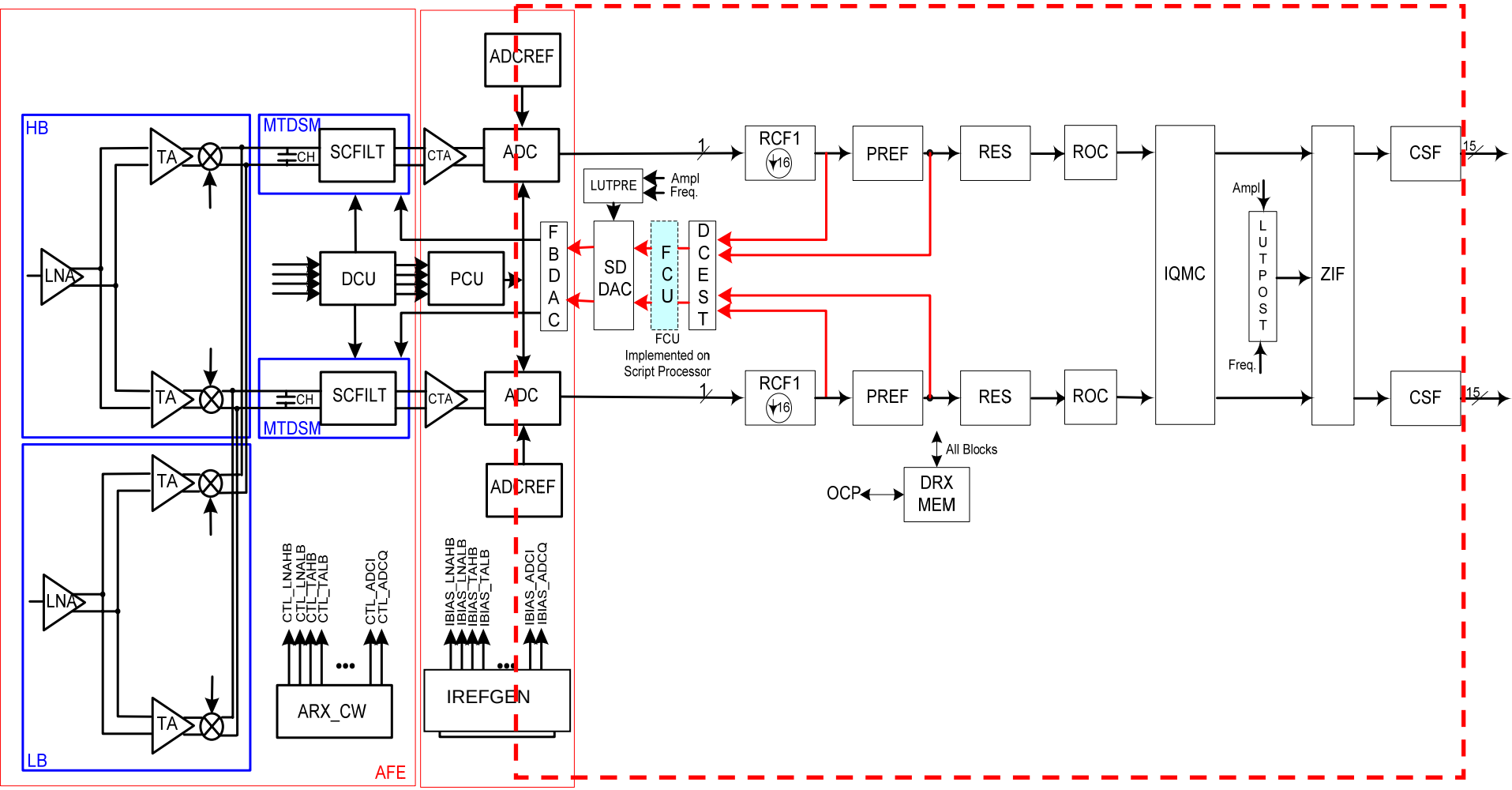
# Digital RF Processor

# Receiver

# RX Location in DRP2 system



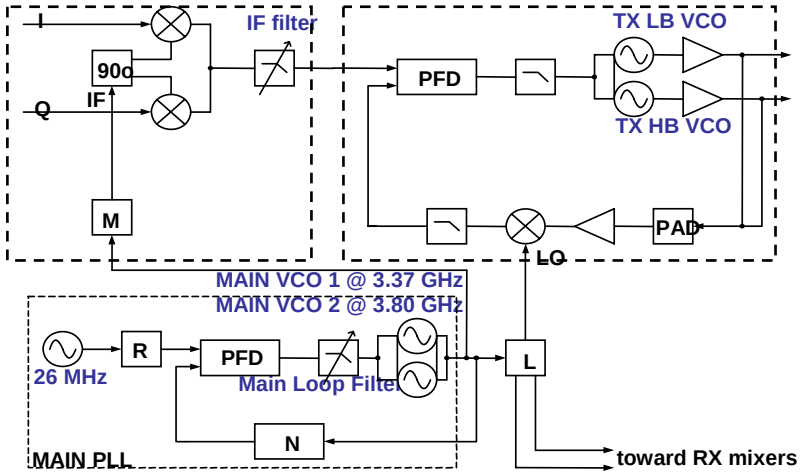
# RX blocks

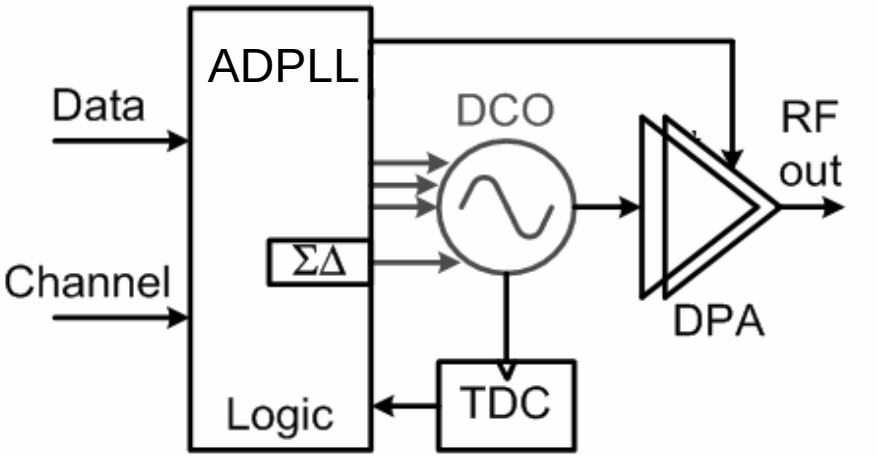

HB
LB
LNA
LNA
TA
TA
TA
TA
MTDSM
MTDSM
CH
CH
SCFILT
SCFILT
CTA
CTA
ADC
ADC
ADCREF
ADCREF
DCU
PCU
FBDAC
SD DAC
FCU
DCEST
FCU
Implemented on
Script Processor
LUTPRE
Ampl
Freq.
1/
RCF1
16
PREF
RES
ROC
IQMC
Ampl
LUTPOST
Freq.
ZIF
CSF
15
1/
RCF1
16
PREF
RES
ROC
CSF
15
All Blocks
OCP
DRX
MEM
CTL_LNAHB
CTL_LNALB
CTL_TAHB
CTL_TALB
CTL_ADCI
CTL_ADCQ
ARX_CW
IBIAS_LNAHB
IBIAS_LNALB
IBIAS_TAHB
IBIAS_TALB
IBIAS_ADCI
IBIAS_ADCQ
IREFGEN
AFE

# Digital RF Processor

## LO & Synthesis
## & Transmitter

# DRP2.0 SYNTHESIZER/TX BLOCK DIAGRAM



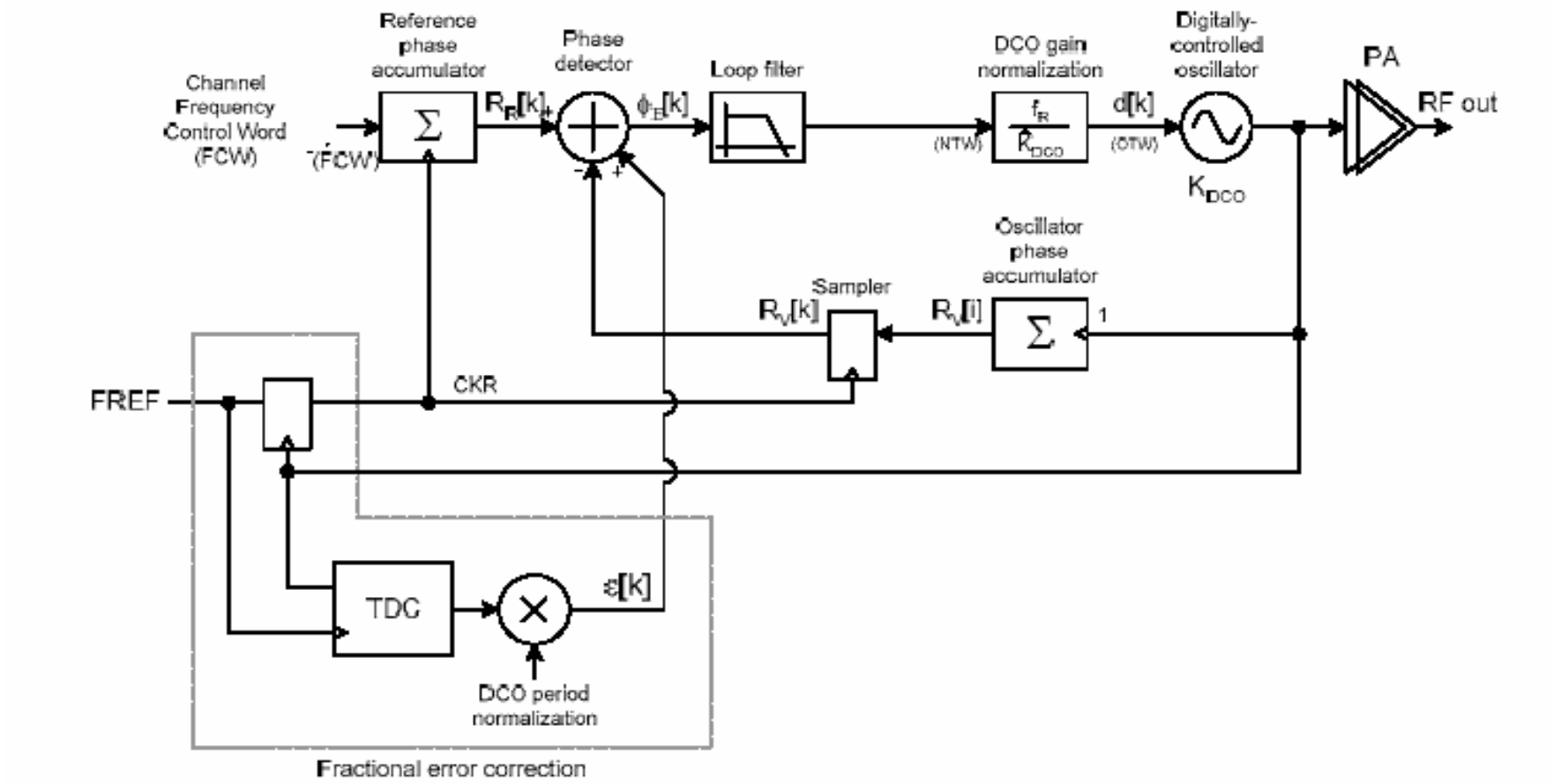




| TRF6151 building blocks | DRP "equivalent" |
|---|---|
| VCO (voltage controlled oscillated | DCO (Digitally-Controlled Oscillator ) |
| PFD (Phase frequency detector) and CP (charge pumps) | Digital comparator + Time-to-Digital Converter (TDC) |
| Loop filter | Digital Loop Filter (LF) |
| Analog TX buffers | programmable pre-power amplifier (DPA) |

# Frequency synthesizer

- Based on an All-Digital PLL (ADPLL)
  - Digitally Controlled Oscillator (DCO) at 1.8 GHz as the RF frequency source
  - The frequency setting uses FCW (fixed-point Frequency Command Word)
  - The phase correction mechanism in 2 steps:
    - The integer part of the phase detector computes the phase difference between the DCO output clock and the retimed reference clock (reference clock resynchronized with the DCO clock)
    - The fractional phase error between the reference and DCO output clocks is estimated by the TDC (Time to Digital Converter) and added to the integer phase error..

# All-Digital PLL (ADPLL) block diagram




Synchronous digital phase domains (key idea of the ADPLL to avoid metastability problems in TDC and reduce noise)

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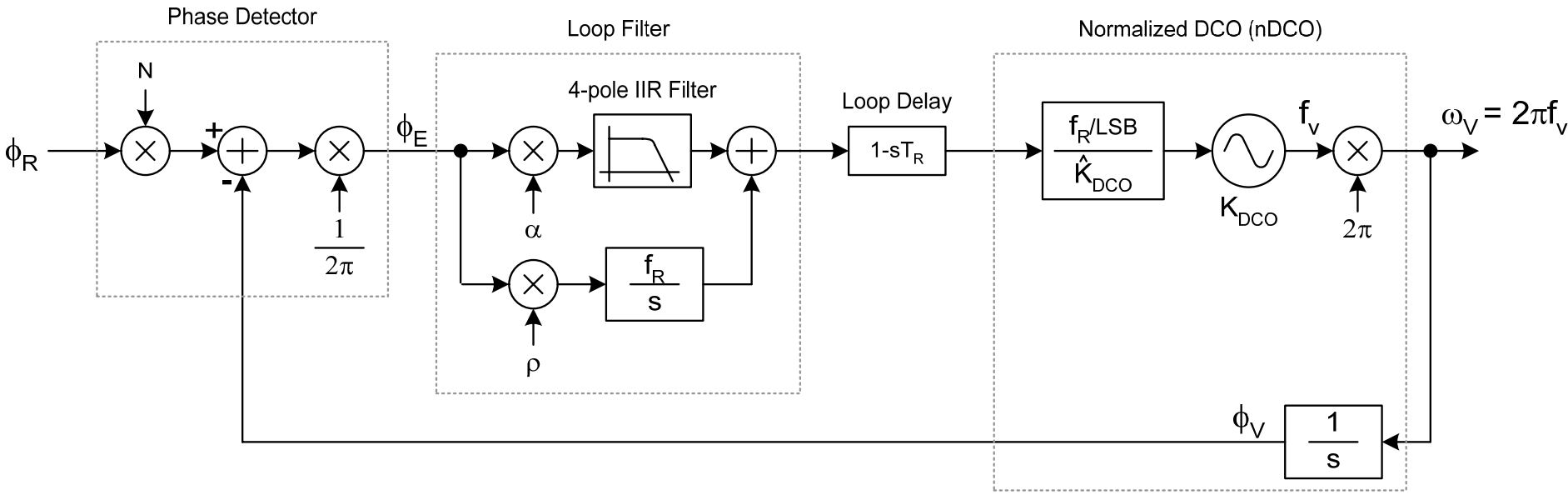
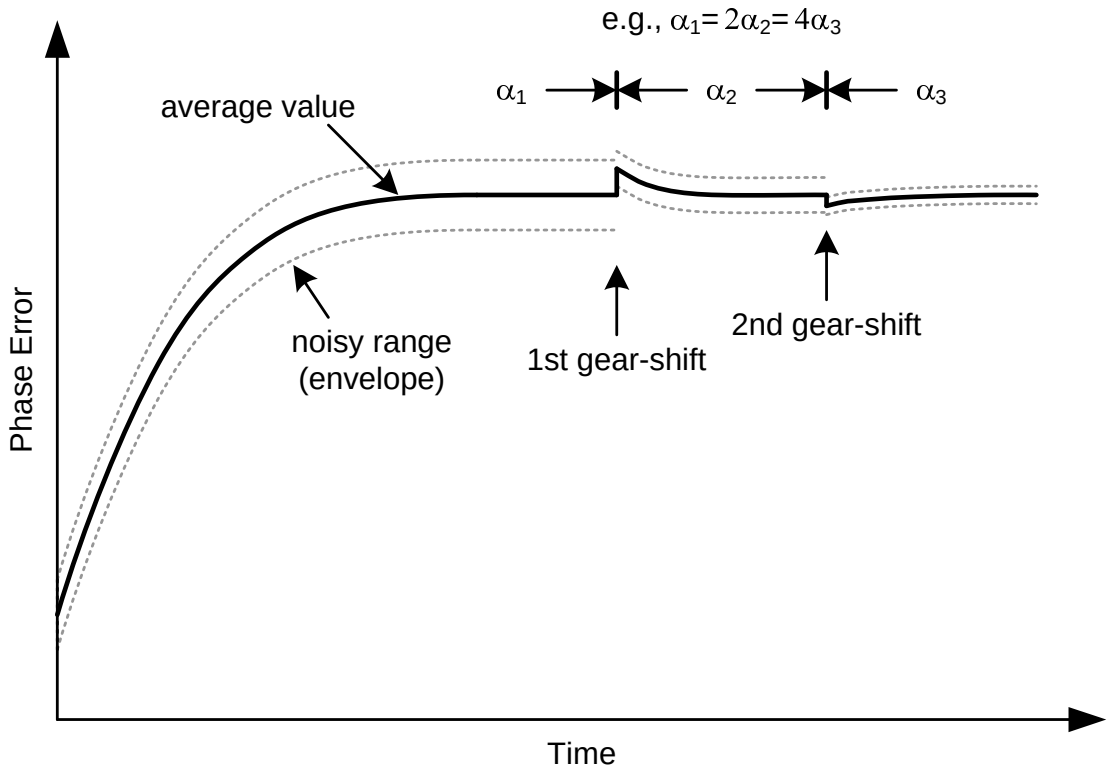
# All-Digital PLL (ADPLL) block diagram



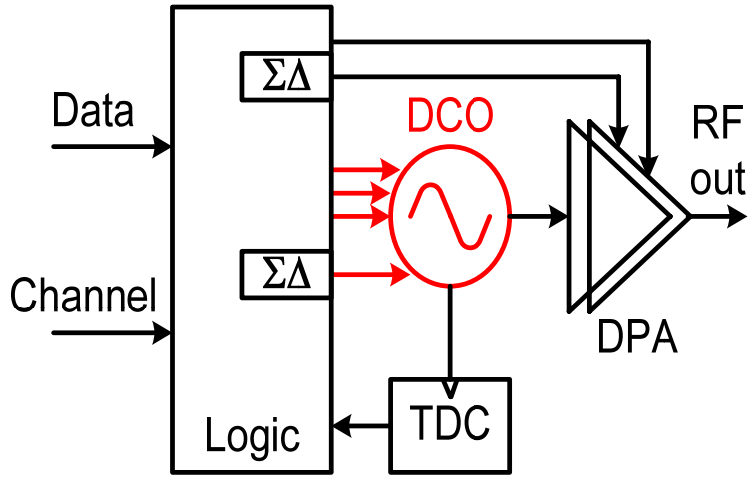
# Gear-Shifting of PLL Bandwidth

- Progressive reduction of ADPLL loop bandwidth while the loop is settling
- Lock time max = 170 usec (RX) and 240usec (TX)

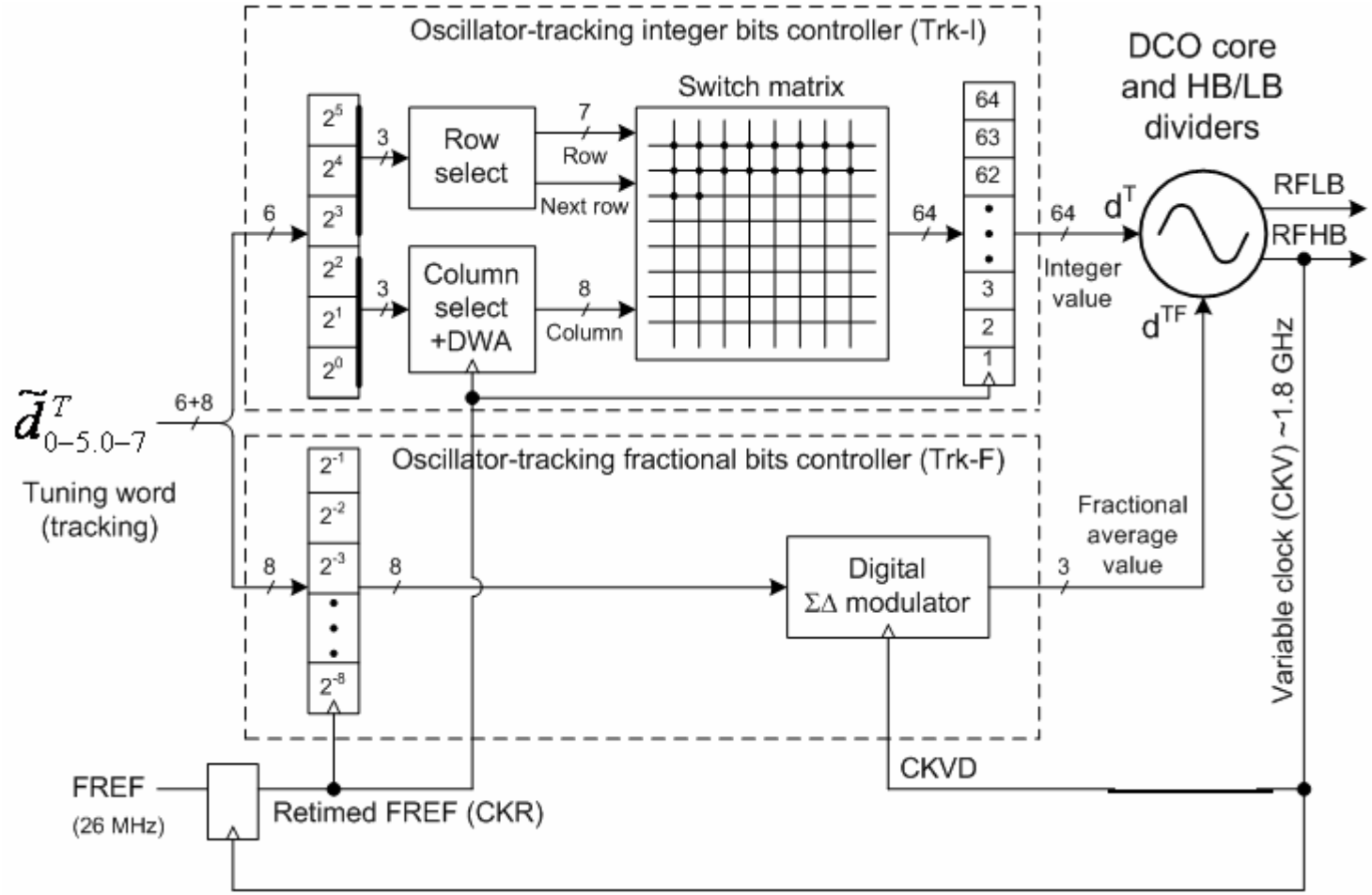


# ADPLL BUILDING BLOCKS (1/5)

- **Digitally-Controlled Oscillator (DCO)**
  Time-to-Digital Converter (TDC)
  Digital Loop Filter (LF)
  All-Digital PLL (ADPLL)
  ADPLL Wideband Frequency Modulation



# DCO: varactor banks overview



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# ADPLL BUILDING BLOCKS (2/5)

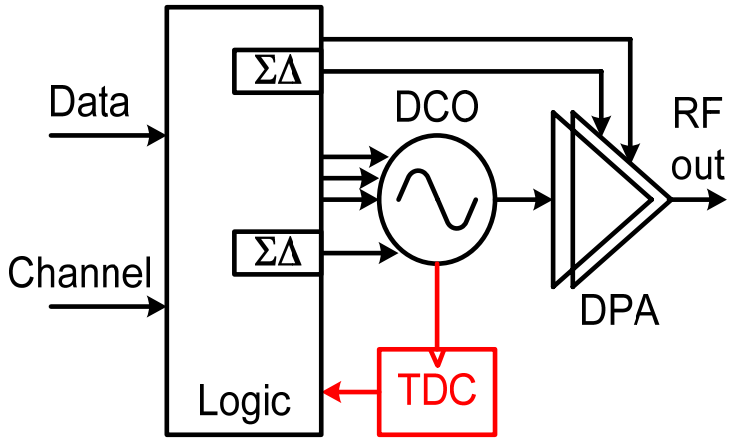
Digitally-Controlled Oscillator (DCO)

- **Time-to-Digital Converter (TDC)**

Digital Loop Filter (LF)

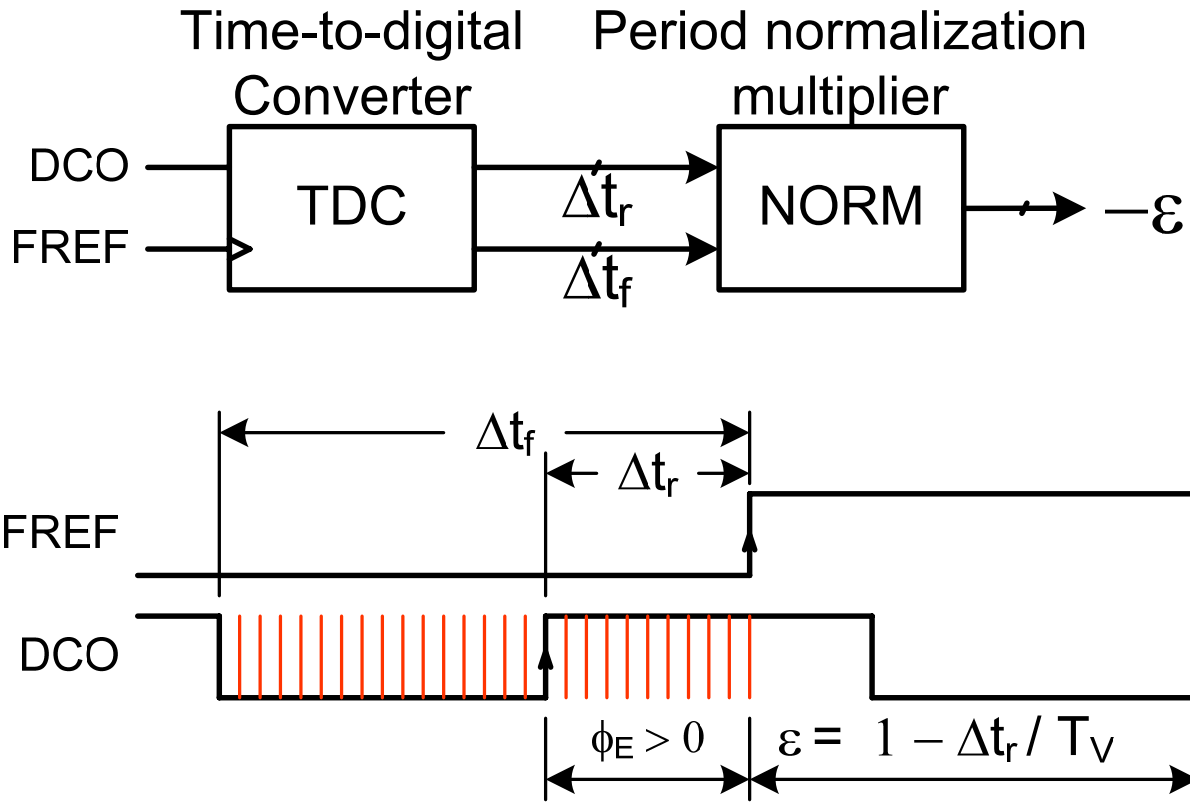
All-Digital PLL (ADPLL)

ADPLL Wideband Frequency Modulation



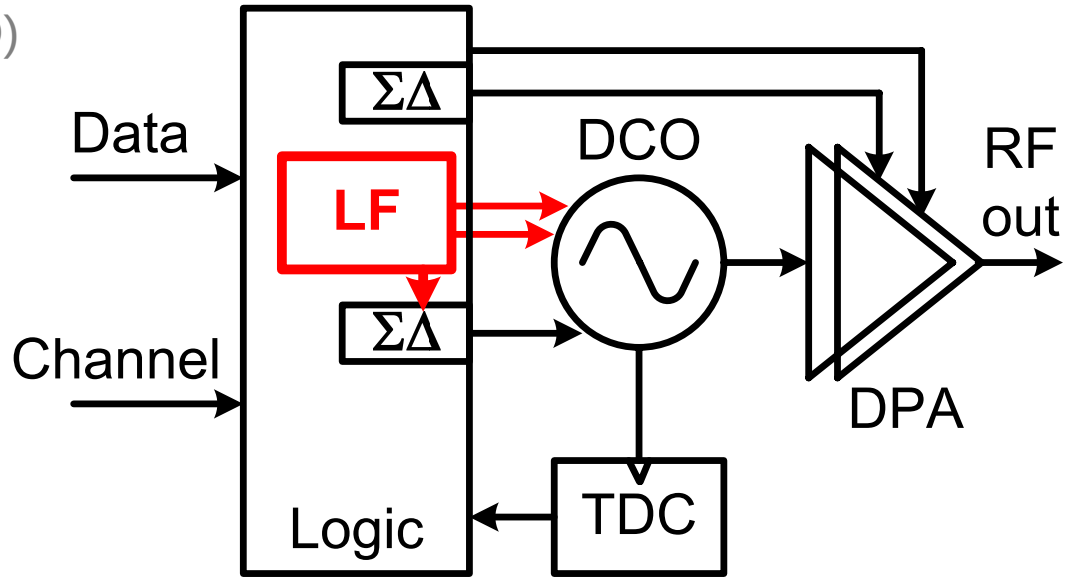
# Time-to-digital Converter (TDC)

- Estimates the fractional Phase Error
- Quantized phase detector with resolution of <20 ps



# ADPLL BUILDING BLOCKS (3/5)

- Digitally-Controlled Oscillator (DCO)
- Time-to-Digital Converter (TDC)
- **Digital Loop Filter (LF)**
- All-Digital PLL (ADPLL)
- ADPLL Wideband Frequency Modulation

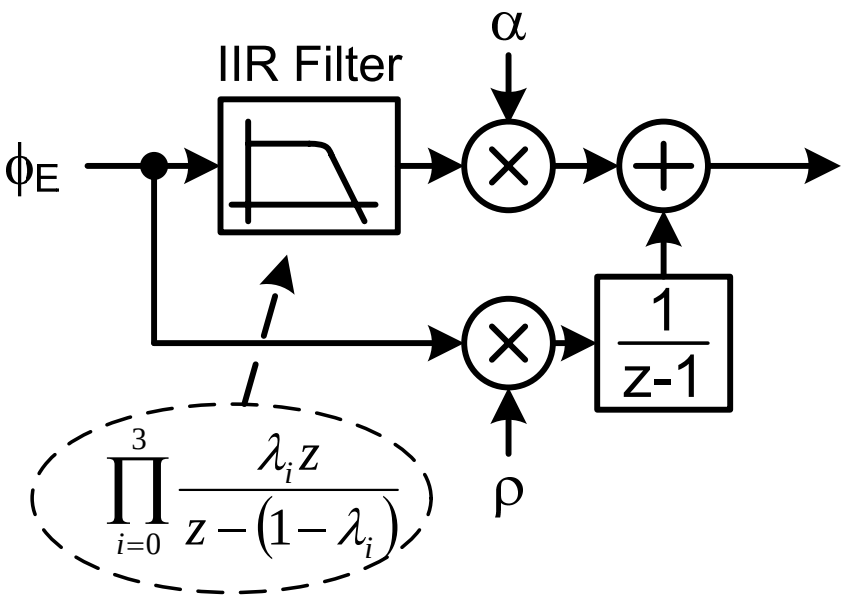


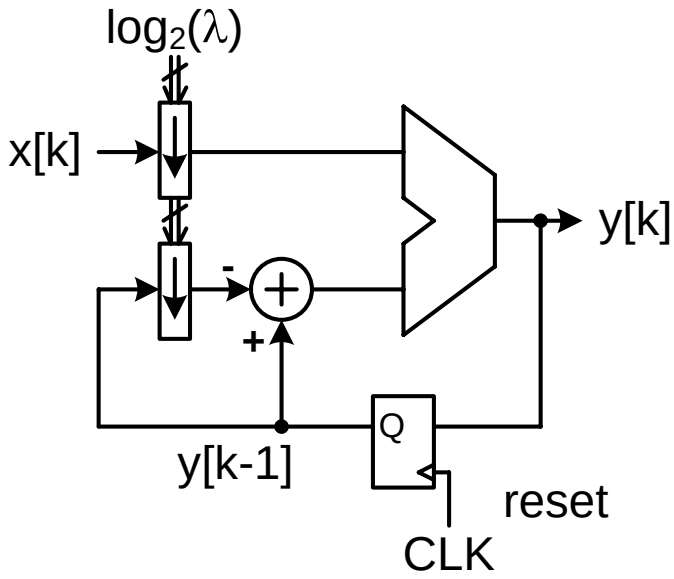
# Digital loop filters

- 4th order digital IIR loop filter to suppress the frequency reference and TDC quantization noise
- Unconditionally stable IIR filters

$$y[k] = (1-\lambda)\cdot y[k-1] + \lambda \cdot x[k]$$

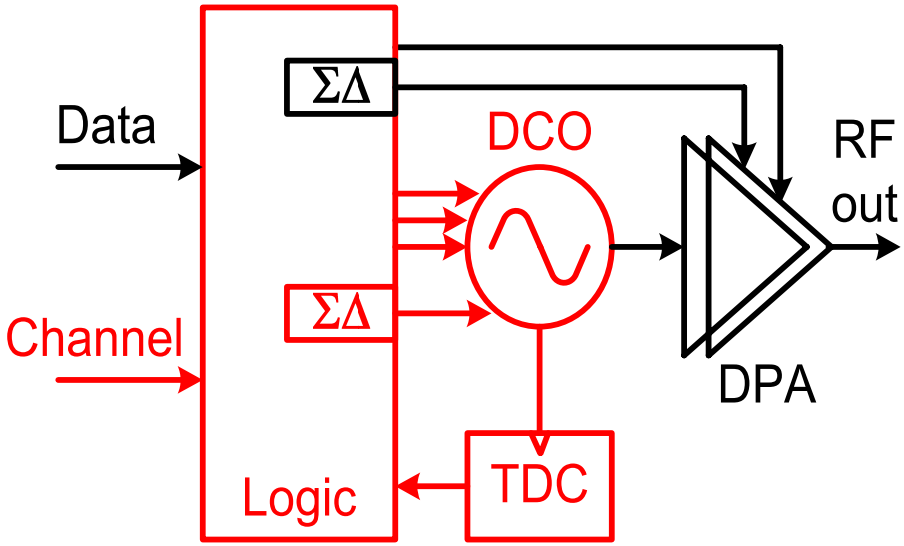
Single-pole IIR stage:



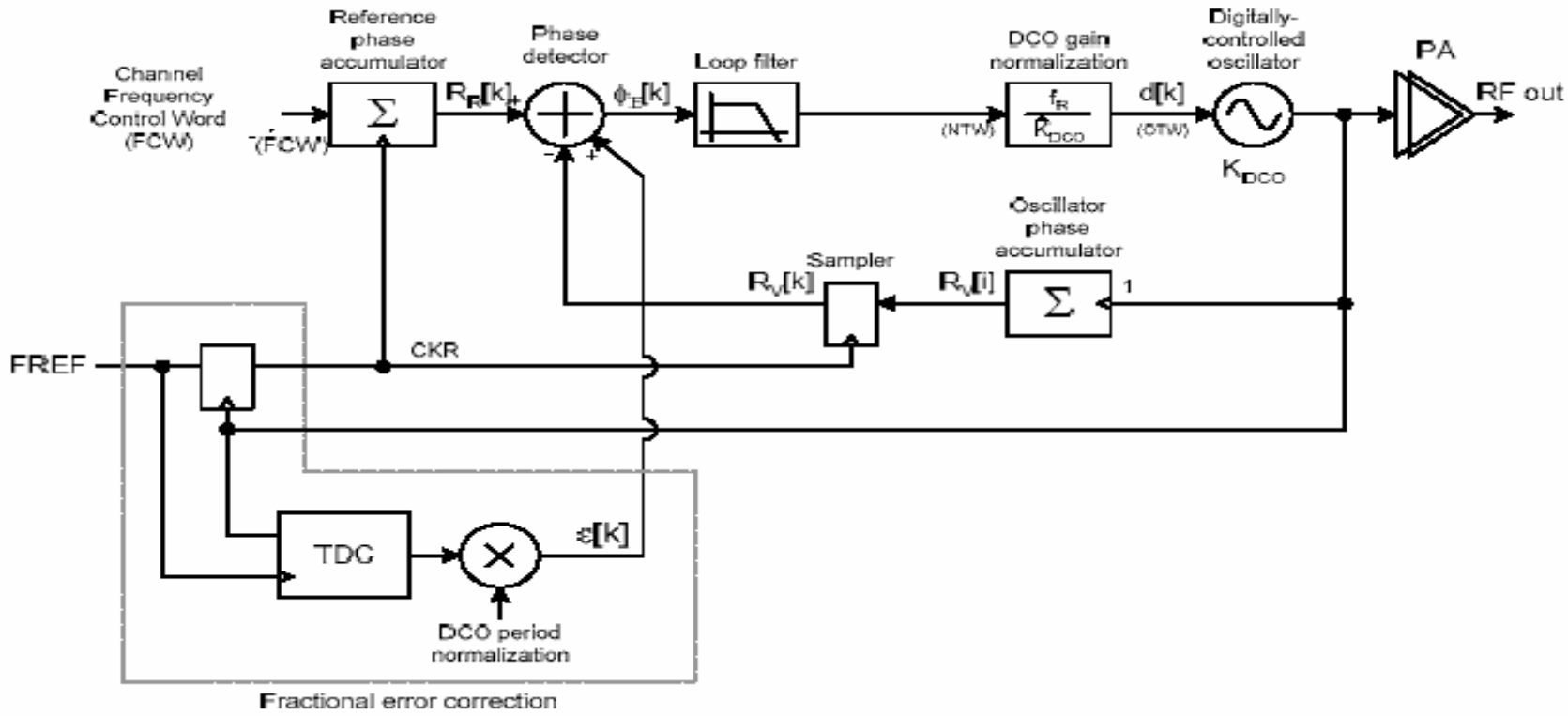
# ADPLL BUILDING BLOCKS (4/5)

- Digitally-Controlled Oscillator (DCO)
- Time-to-Digital Converter (TDC)
- Digital Loop Filter (LF)
- **All-Digital PLL (ADPLL)**
- ADPLL Wideband Frequency Modulation



# All-Digital PLL (ADPLL)

- Type-II 6th-order PLL loop
- Reduced Lock Time (Loop BW adaptation)
- Synchronous digital phase domains (key idea of the ADPLL to avoid metastability problems in TDC and reduce noise)



# ADPLL BUILDING BLOCKS (5/5)

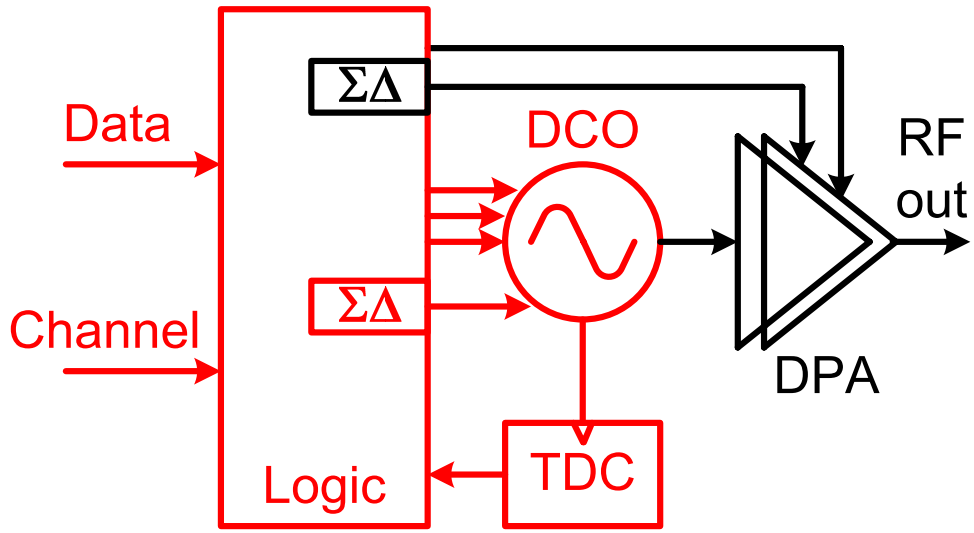
Digitally-Controlled Oscillator (DCO)

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

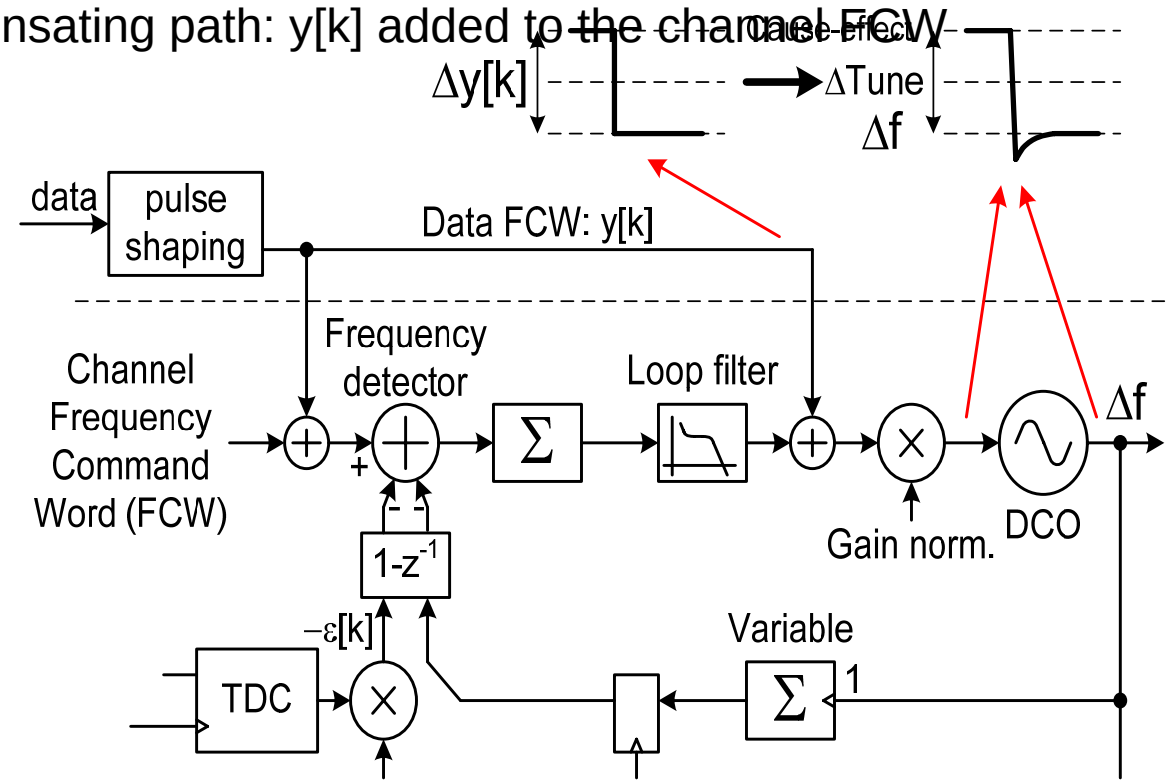
**All-Digital PLL (ADPLL)**

- ADPLL Wideband Frequency Modulation



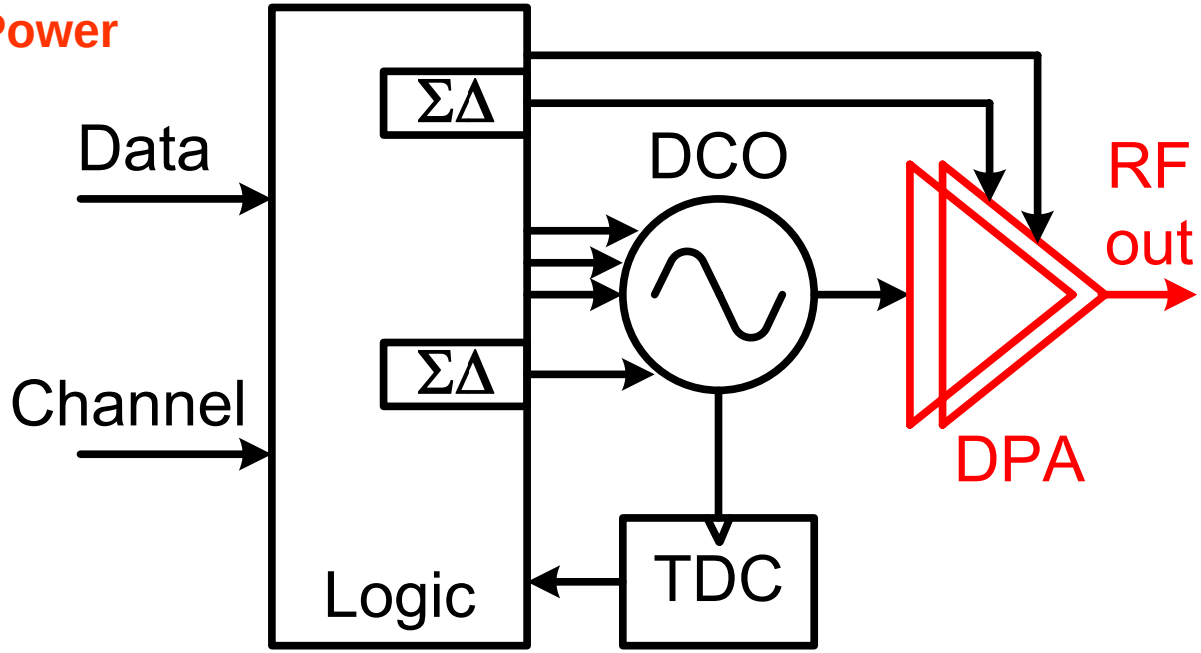
# ADPLL with GMSK Modulation

- Two-point modulation
  - Direct feedforward path : y[k] directly drives the DCO
  - Compensating path: y[k] added to the channel FCW



# OTHER RF TX BUILDING BLOCK

- **Digitally-Controlled Power Amplifier**

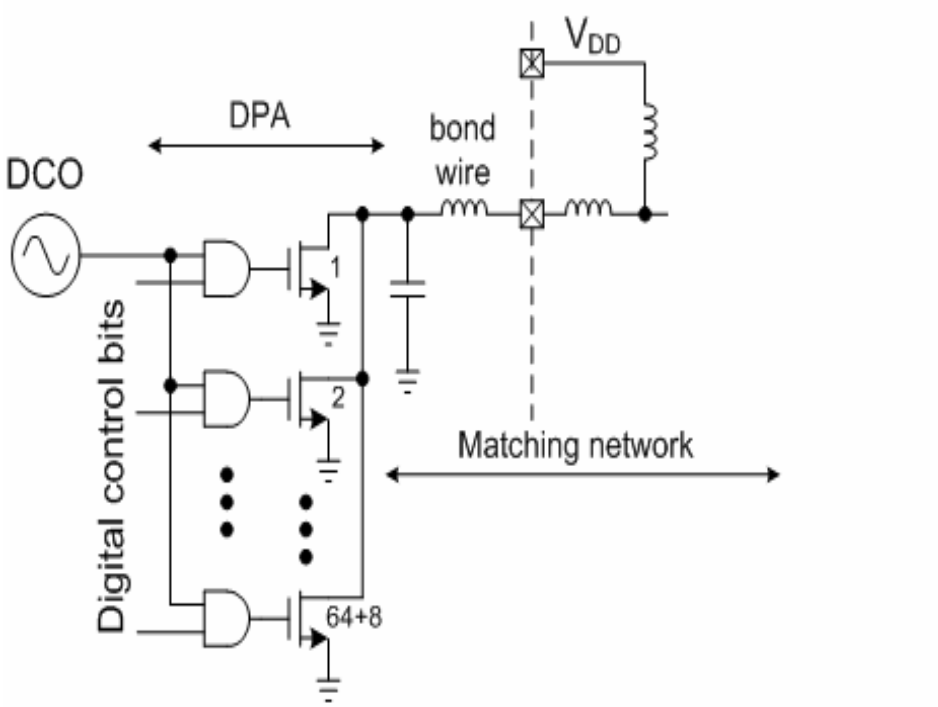


# Digitally-Controlled Power Amplifier

- Class-E PA with MOS transistor switches

The DPA can be thought of as an RF DAC, where “A” is RF “amplitude”

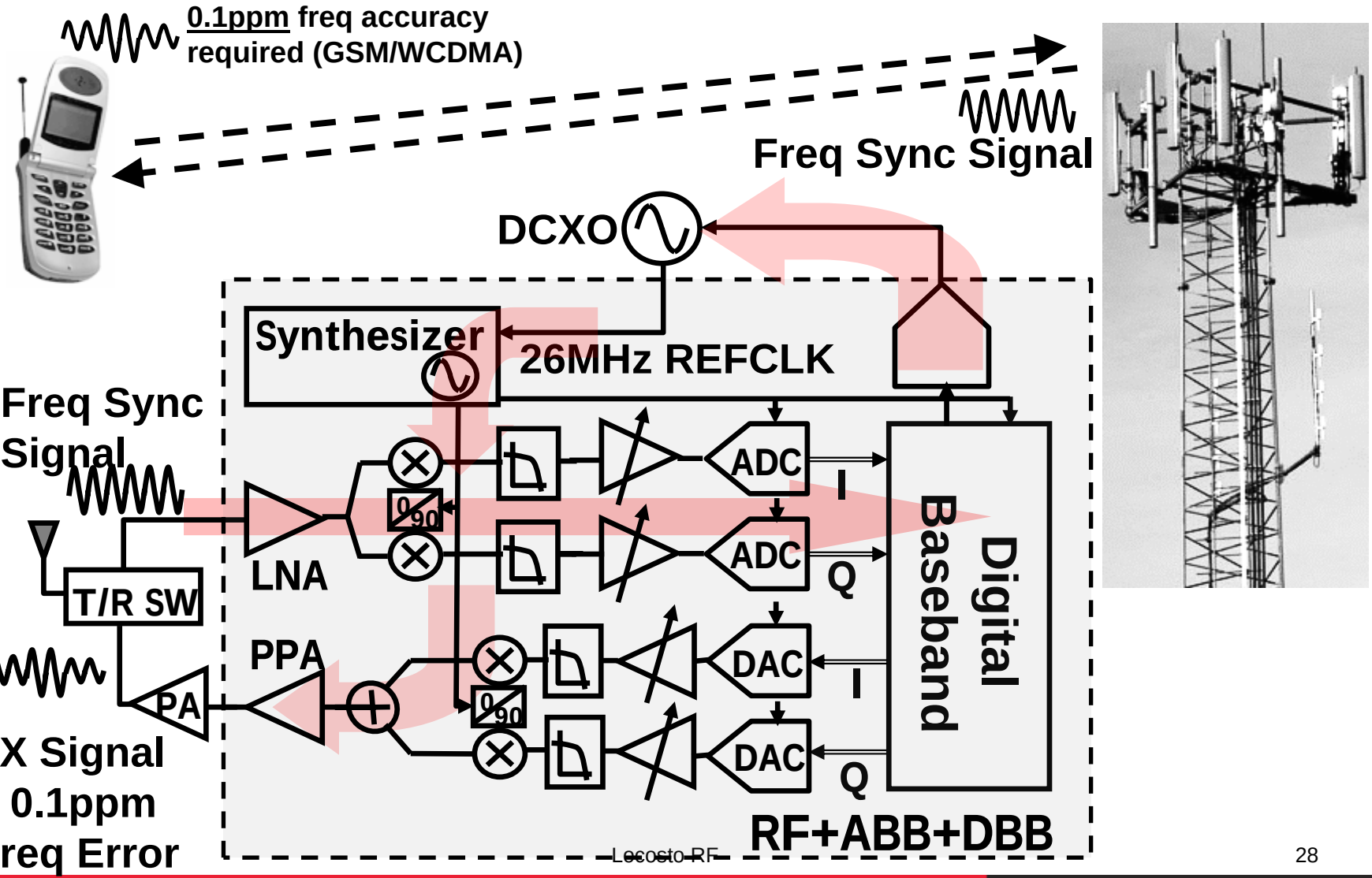
- Array of unit-weighted MOS switches, that can be programmed through API to achieve the TX desired output level (up to +8dBm)



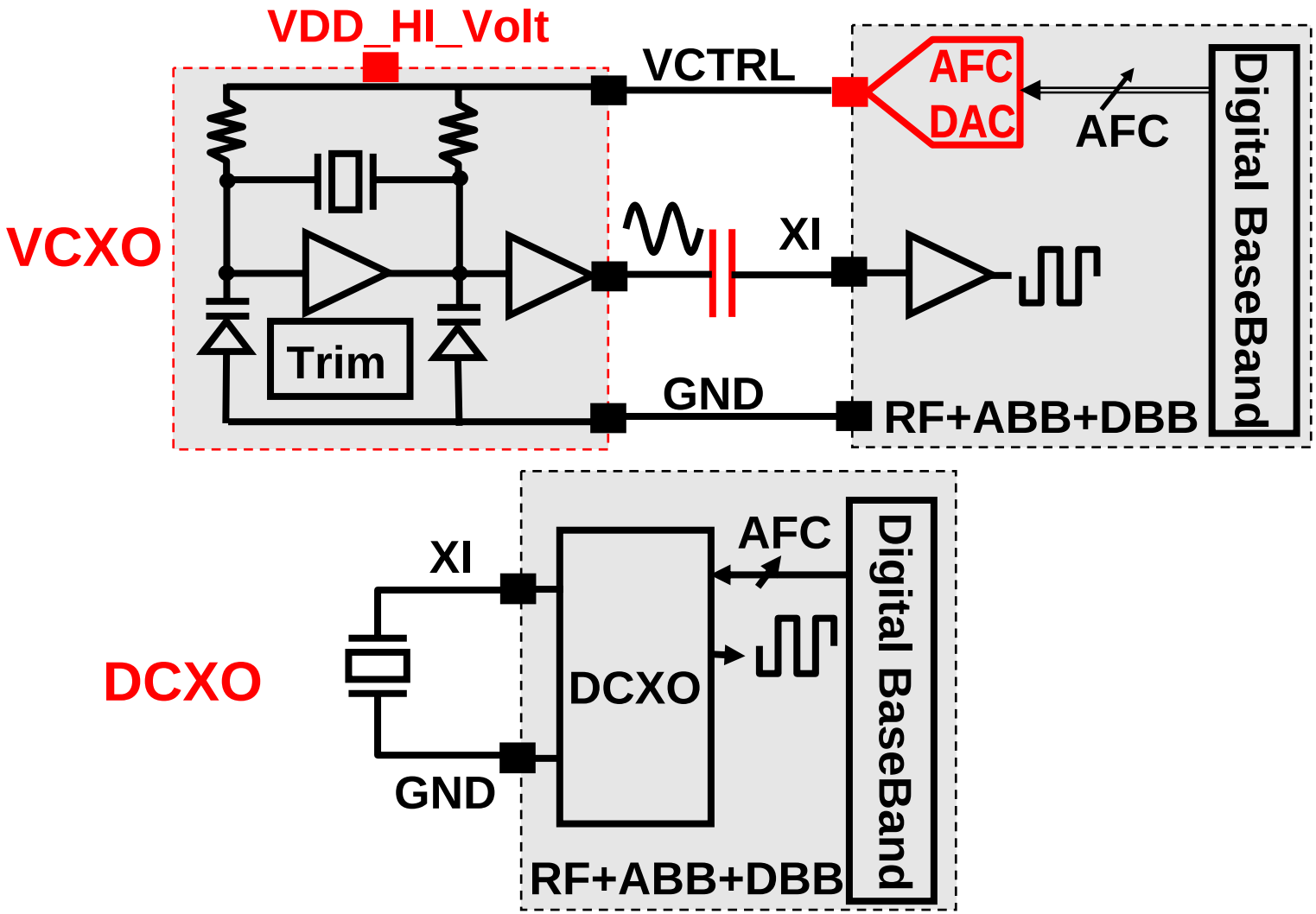
# Digital RF Processor

# DCXO

# AFC Loop in GSM/EDGE Network



# VCXO vs. DCXO


VDD_HI_Volt
VCTRL
AFC
DAC
AFC
Digital BaseBand
VCXO
XI
Trim
GND
RF+ABB+DBB
DCXO
XI
AFC
Digital BaseBand
DCXO
GND
RF+ABB+DBB

# DRP - DCXO overview

- Low phase noise clock reference for RF clock synthesis
- Large tuning range : 10 bits digital codeword for coarse tuning
- Accurate frequency : 14 bits digital codeword for fine tuning
- Oscillation amplitude control to limit crystal power drive
- Oscillation amplitude detection to tune startup time
- State machine for startup tuning procedure

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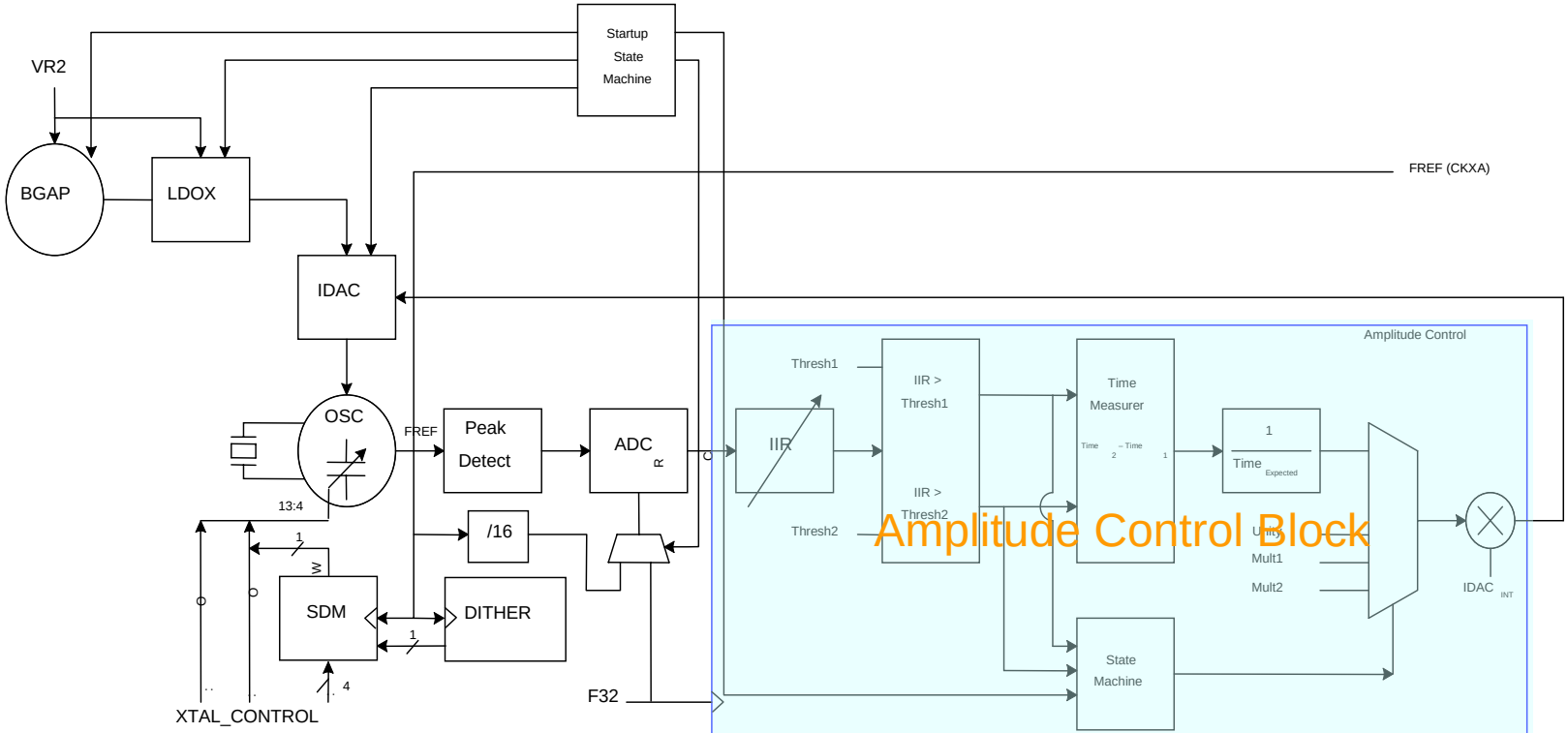
# DCXO System



# Coarse Frequency Control

Coarse Frequency Adjustment (CFA) capacitor consists of:

- Fixed capacitor of size 168 units
- Modified-binary array with 10-bit control, with individual weights of 1, 2, 3, 6, 12, 24, 48, 96, 192 and special capacitor of ~200 units respectively
- CFA calibration is needed to obtain initial CFA value that gives optimal tuning range using Fine Frequency Adjustment only

# Fine Frequency Adjustment

- Fine Frequency Adjustment (FFA) is controlled via 14-bit codeword
- The physical capacitor array consist of 1024 capacitors.
- Capacitor array is tapered, with sizes ranging from ~30fF to 100fF.
- Tapering creates linear transfer function between codeword and the frequency
- Additional 4 bits of frequency resolution are obtained via digital Sigma-Delta modulation of an array element

# Fine Frequency Adjustment (cont.)

Example:

14-bit codeword, codeword 0000000010_0111, or 2 and 7/16$^{th}$ correspond to turning on 2 capacitor array elements, and turning on another capacitor element, 7 out of every 16 FREF clocks (on average)

- Typical frequency resolution of the FFA is 0.002 to 0.003ppm/LSB
- This may vary substantially with the crystal and CFA value chosen during calibration

# Amplitude Control in DCXO

- High amplitude of oscillation in a DCXO produces superior phase noise
- High amplitude of oscillation may cause power drive of crystal to be exceeded causing damage to the unit
- The Amplitude is directly affected by the current
- The Amplitude is also heavily influenced by the changes in tuning capacitance (FFA)

# DCXO Startup

- DCXO startup and wakeup require special hardware, since FREF clock is not available until DCXO becomes fully operational and therefore the DSP, the Script Processor and the FLASH memory are inaccessible
- DCXO startup is clocked by the clock from the 32kHz crystal
- All three IDAC codewords go to their default values of
  - Numerator = 128
  - Denominator + Fraction + Fixed = 0 + .0 +128

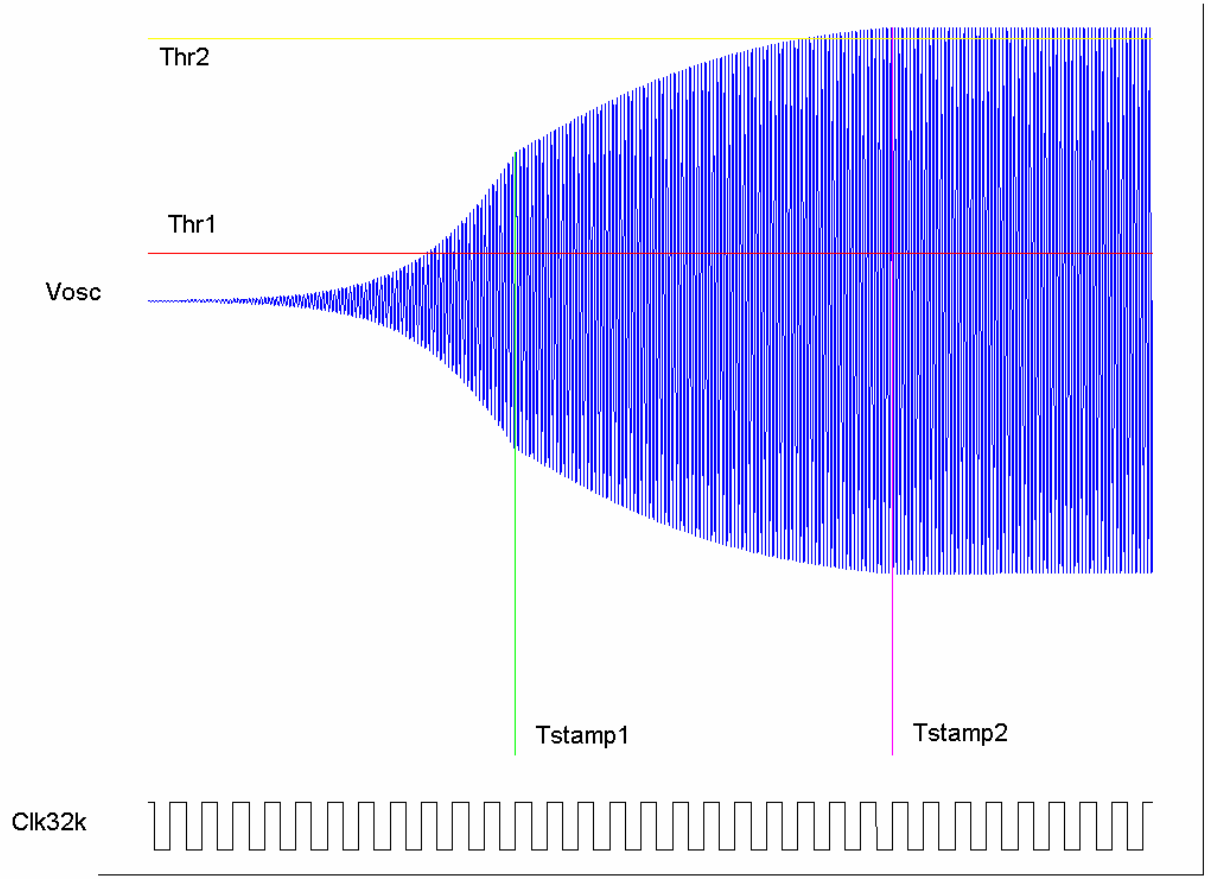
# DCXO Startup

- Startup sequence consists of three phases

1. Quick Charge: IDAC current is set to 3X nominal value of IDAC current. This is done in order to guarantee that the oscillations will begin. The output of the 5-bit ADC is monitored for the crossing of first programmable threshold (thr1). On the second 32 kHz clock cycle after the crossing of the thr1 is detected, Phase 1 ends.
2. Linear Ramp: IDAC current is set to X nominal value of IDAC. The output of the ADC is monitored for crossing of the second programmable threshold (thr2).
3. Final Settling : New value for $IDAC_N$ is set using formula

$$IDAC_{N,new} = IDAC_{N,nom} \frac{\Delta t_{new}}{\Delta t_{nom}}$$

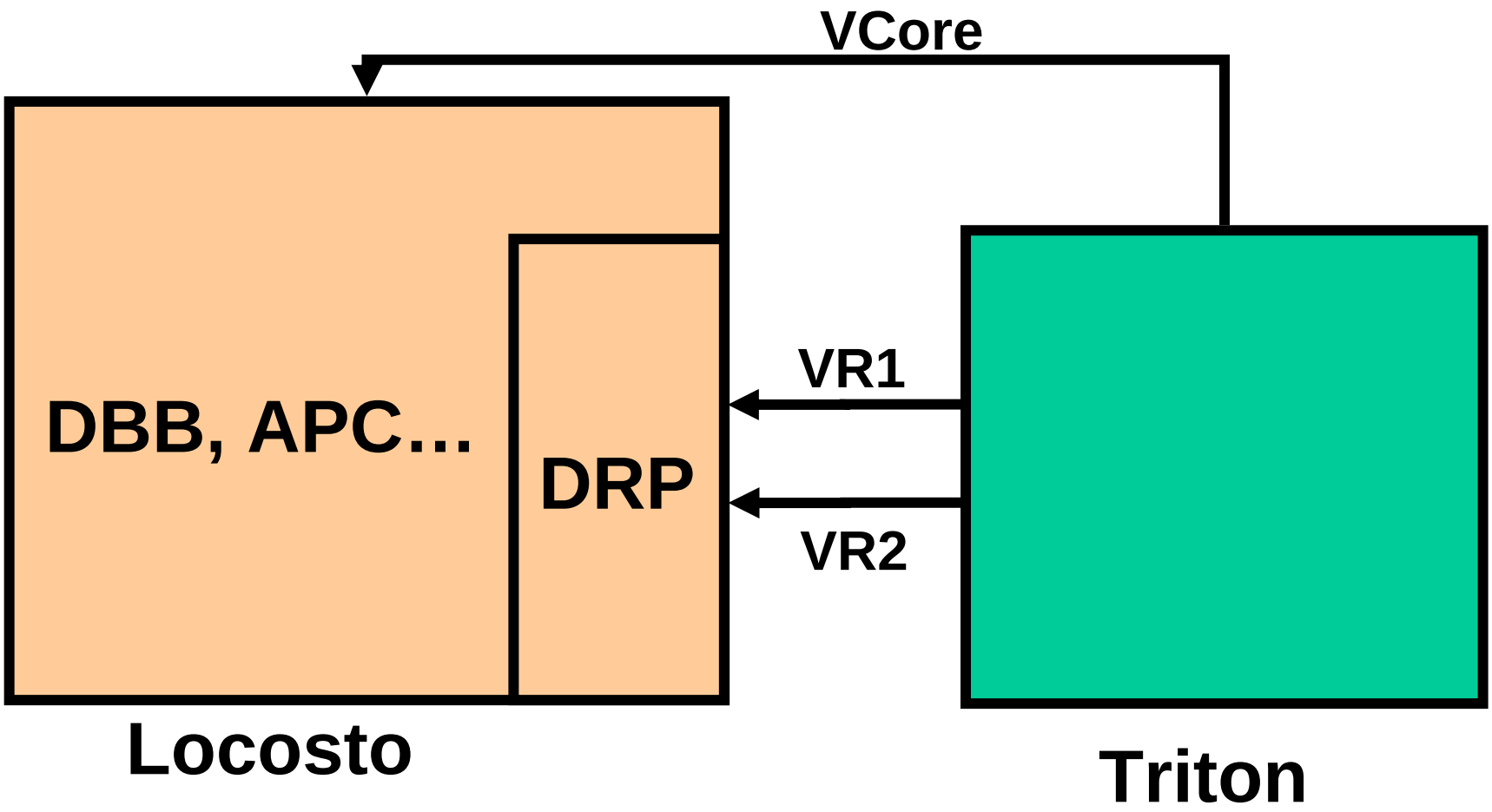
# DCXO Startup (cont.)



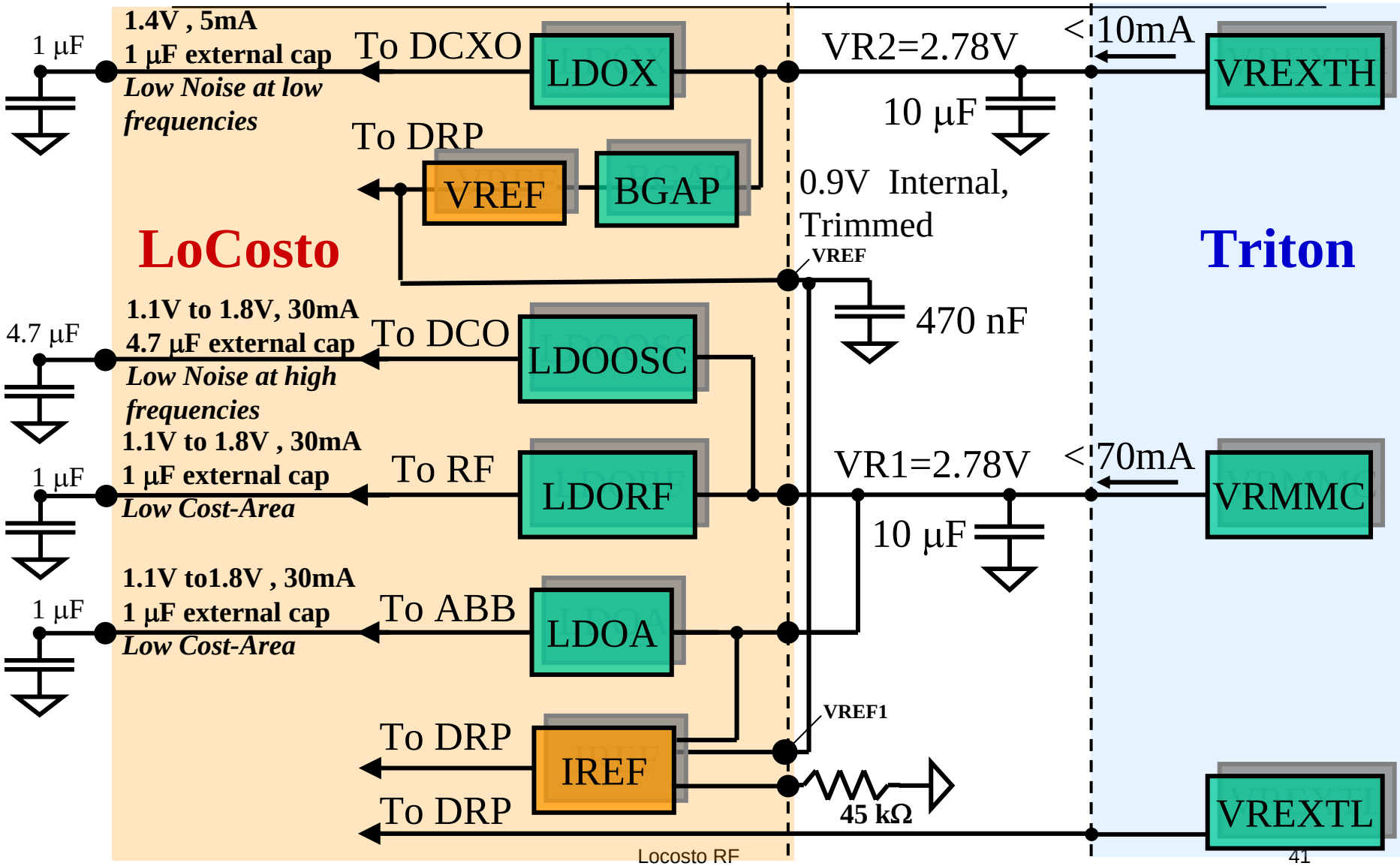
# Digital RF Processor

# Power Management

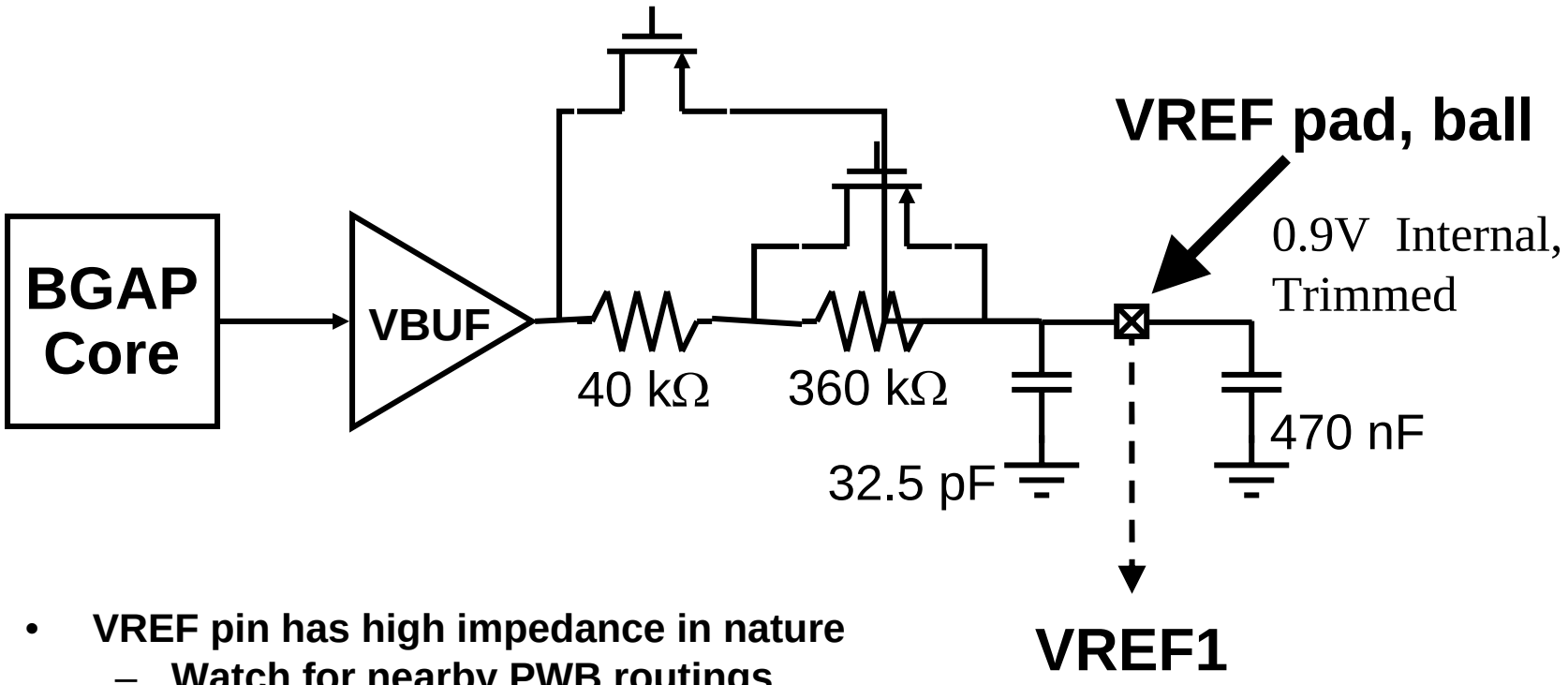
# PCB-Level Overview



# DRP-Triton Interface

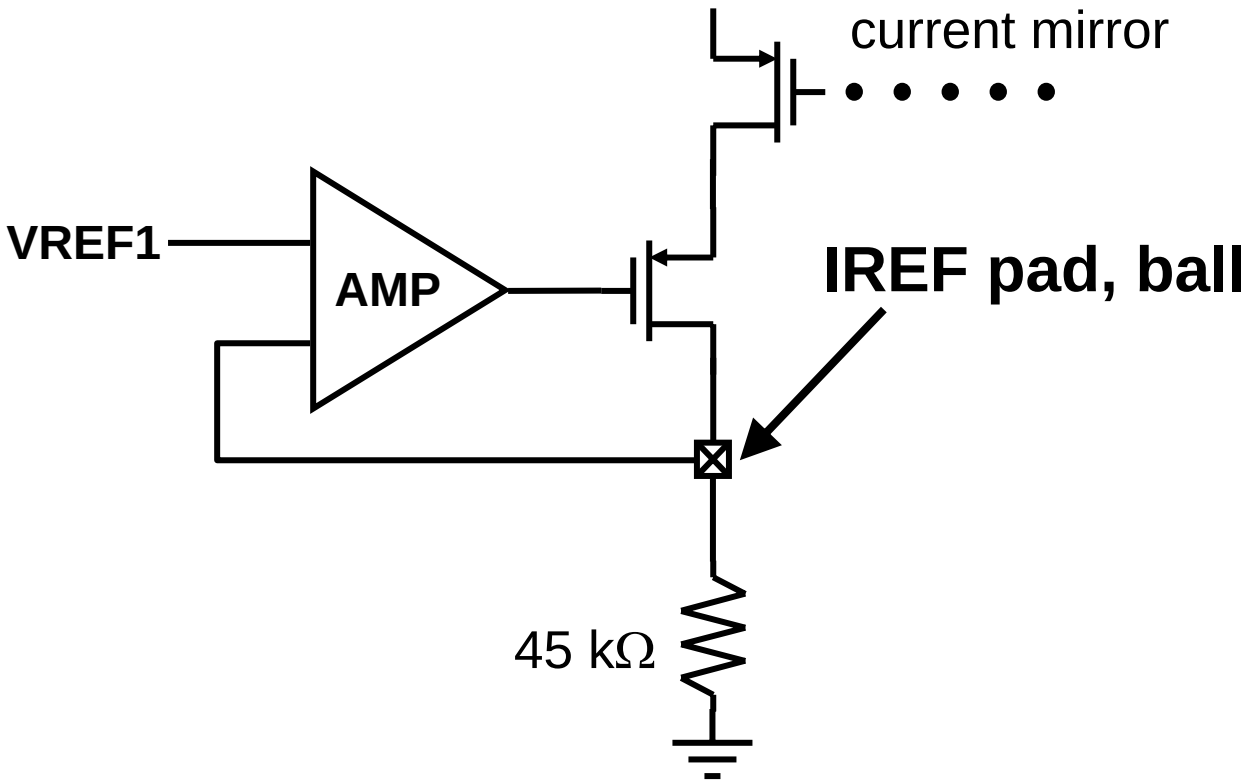


# VREF




- VREF pin has high impedance in nature
  - Watch for nearby PWB routings
- Star connection from VREF
- VREF has priority on PWB
  - VREF1 is secondary

# IREF




- **IREF pin has high impedance in nature**
  - **Watch for nearby PWB routings**

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# LDOs / VREF / IREF specifications

| | *Unit* | LDOX | LDOOSC | LDORF | LDOA | VREF |
|---|---|---|---|---|---|---|
| Vout typ (after trim) | *V* | 1.4 | 1.4 | 1.4 | 1.4 | 0.9 |
| Max average current (during 625us) | mA | 5 | 30 | 30 | 30 | - |
| External Cap | *uF* | 1 | 4.7 | 1 | 1 | 0.47 |
| Main "function" | | Low noise @low freq | Low noise @high freq | Low cost-area | Low cost-area | |
| Vout range | *V* | 1.393/1.407 | 1.2/1.8 | 1.1/1.8 | 1.1/1.8 | 0.882/0.918 |
| Tied to | | DCXO Temp sensor buffer | DCO Freq divider Buffers | PPA SAM LNTA | ABB | |
| Noise typ (1kHz) | *nV/Hz^0.5* | 0.25 | 6.3 | 6.3 | 6.3 | |
| Noise typ (400kHz) | *nV/Hz^0.5* | 27 | 9.1 | 23 | 23 | 16 |

# LDO Key Specifications/Care-about

- **Cost**
  -External capacitor size
  -Silicon area
- **Nominal voltage**
  - 1.4 V after trim
- $\mathbf{I_{load,max,avg}}$
  - 30 mA except LDOX of 5 mA
- **Active and passive disable**
- **PSRR relaxed** (Since VR1 and VR2 are regulated)
  - Reduced LDO bandwidth
  - Better noise performance
- **Turn-on time**
  - (1% settling) < 150 μs
  - Measured: < 80 μs for all LDOs in MS4 data

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# LDO Noise Measurements

- Currently LDOs provide satisfactory noise performance according to transceiver parametric data
  - All LDOs have similar noise performance
  - LDOOSC, LDORF and LDOA have better low-frequency noise than spec.
  - Plan to unify LDO design for future generations
  - Plan to further reduce power/ground domains for future generations, which also further reduces cost

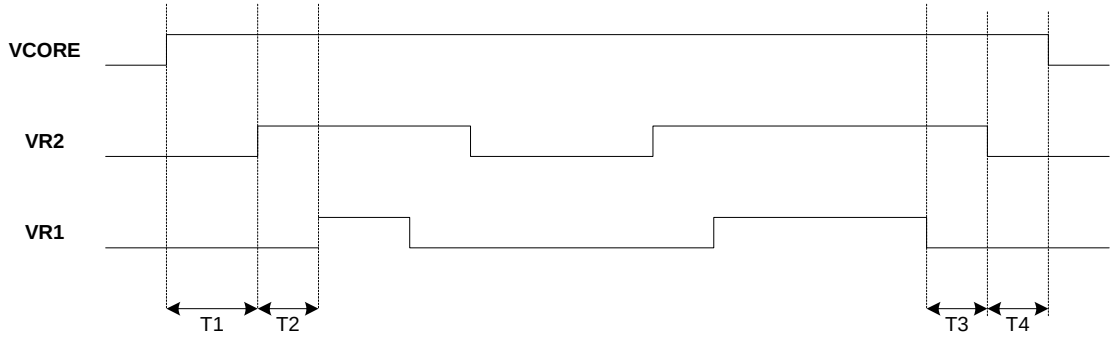
# Power Management

DRP2 needs 3 external power supplies:

- VCORE: DRP Core digital supply: 1.3 V
  - VCORE is connected to DBB core voltage VDD_CORE.
  - Total consumption on this power domain (DRP + DBB) is 140 mA (DRP ~35mA).
  - This power domain must be present before all other DRP mega module supplies.
  - Low voltage mode: to reduce leakage during sleep mode (voltage reduced to 1.05V)
- VR1: Pre-regulated input to LDO_OSC,LDO_A and LDO_RF DRP embedded LDOs. The required supply is 60 mA at 2.8V.
  - This power domain is isolated from the VCORE allowing VR1 switch off while keeping VCORE active or in low consumption mode.
- VR2: Pre-regulated input to LDO_X DRP embedded LDO.
  - The required supply is 10 mA at 2.8V. This power domain is isolated from the VCORE allowing VR2 switch off while keeping VCORE active or in low consumption mode

# Power Management sequencing

- VCORE is provided first at start-up
- Then VR2 (DCXO) is provided by Triton, then VR1 for other RF blocks.
- VCORE and VR2 sequencing is controlled by Triton FSM.
- VR1 is switch ON/OFF is controlled by SW.




| Power Domain | Enabling Order | Disabling Order |
|---|---|---|
| VCORE | 1st | last |
| VR2 | 2nd (T1= TBD*T32k) | 2nd (T4=TBD*T32k) |
| VR1 | last (T2= TBD*T32k) | 1st (T3= TBD*T32k) |

# Digital RF Processor

# APC

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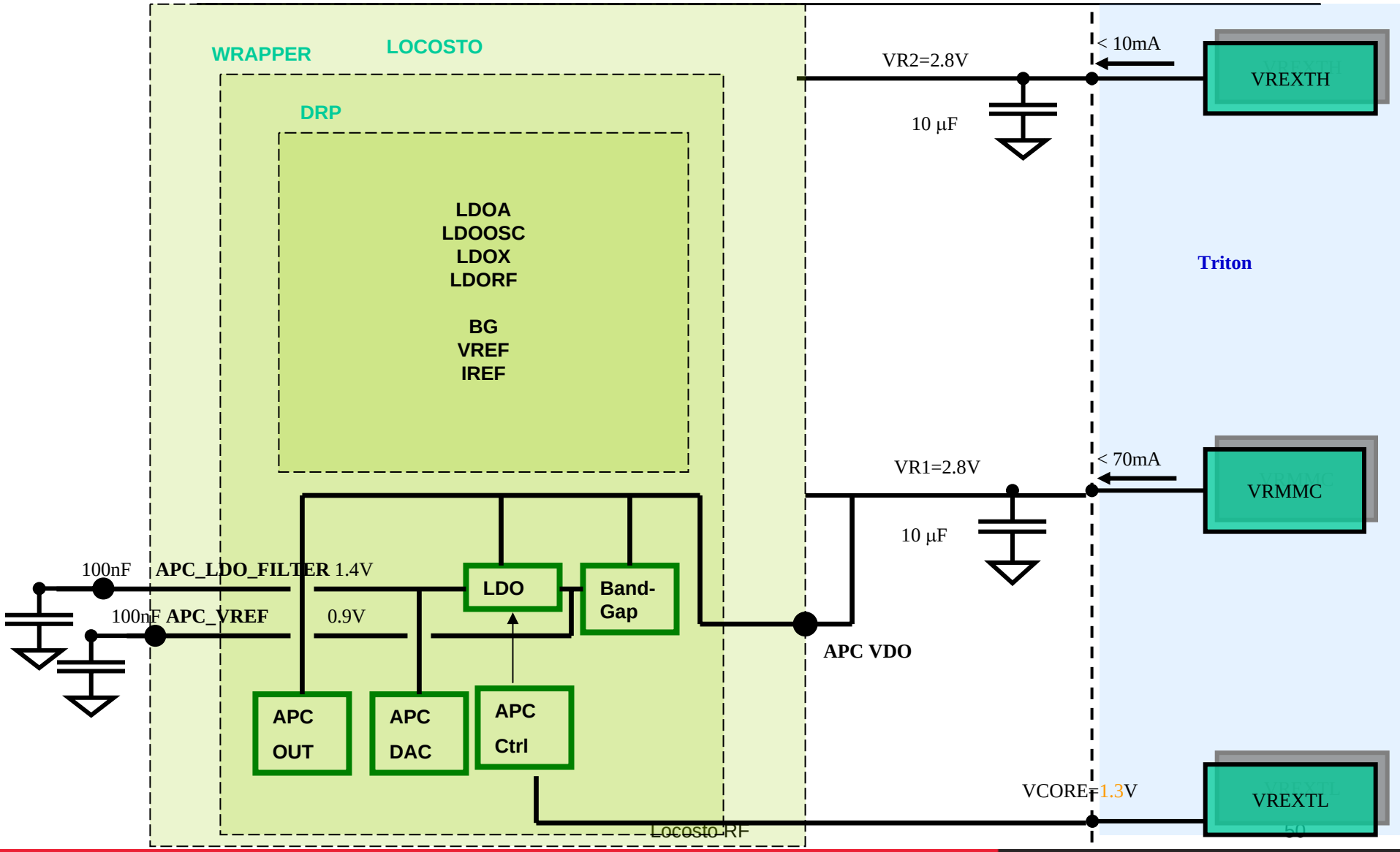
# APC in Wrapper - Triton Interface



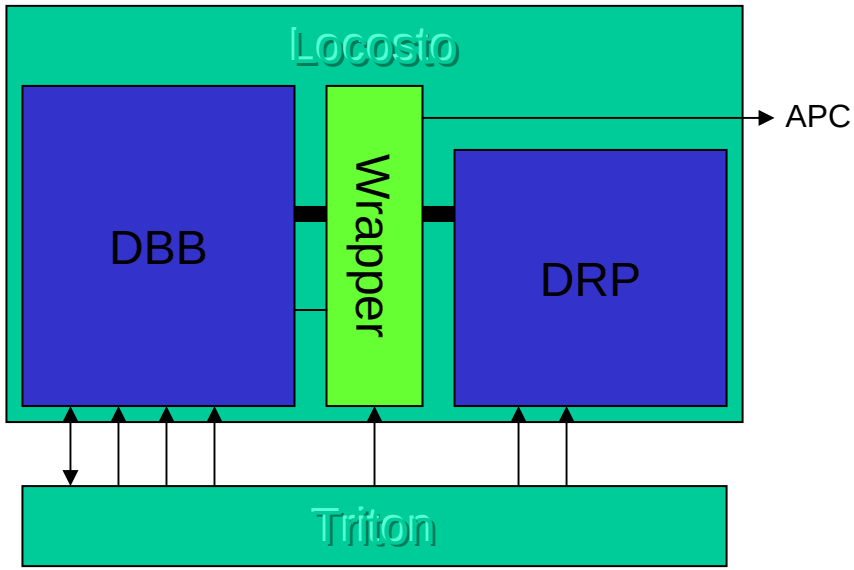
# APC Power Management

APC power supply requirements –

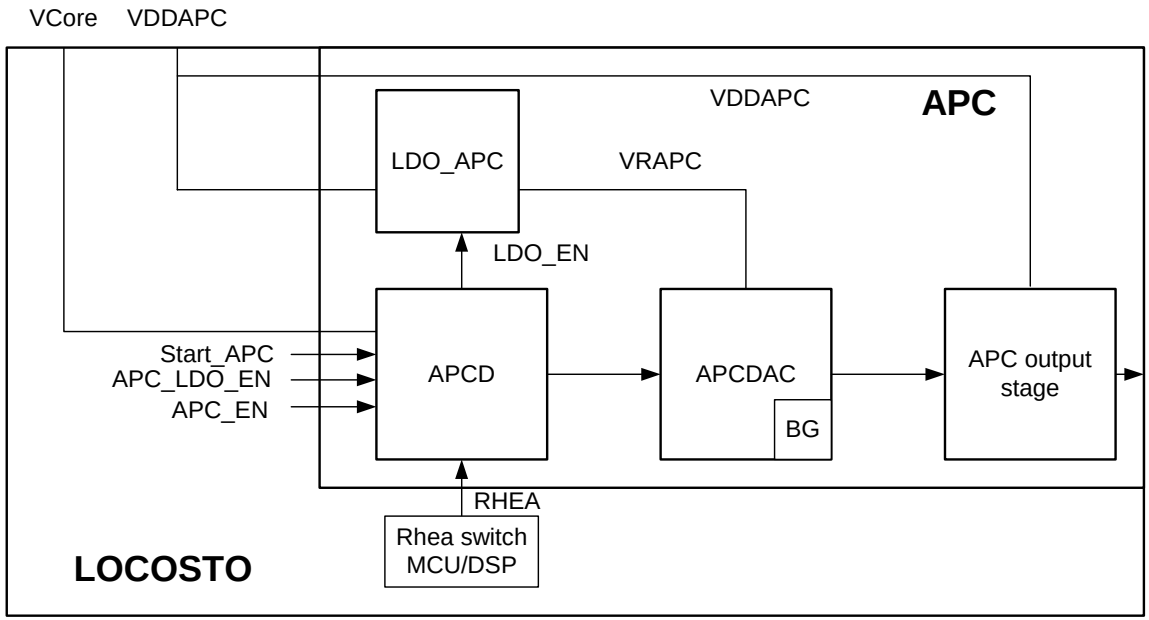
- VCORE: Core digital supply (1.3 V). This supply is dedicated to the APCD (APC Digital) block.
- VRAPC: Pre regulated supply to APC DAC analog output stage. The required supply is 20 mA at 1.4V.
  - This power domain is provided through an integrated LDO, SW controlled through the DBB.
- VDD_APC: APC Output Amplifier power supply. The required supply is 6 mA at 2.8V, this to allow an adequate APCOUT signal swing capable of driving PA circuits.
  - This domain is mapped on the Triton VRMMC supply with star connection respect to the DRP VR1 input to reduce noise. This power domain is enabled under SW control.

# DRP - APC

- APC is integrated in the DRP Wrapper



# DRP - APC




- APCD : Digital block generating the correct ramping profiles
- APCDAC : Digital to Analog Converter and output stage of the APC.

# DRP - APC :Ramp Generation

**In previous TI modem applications,**

-TX ramping up and ramping down were achieved during **8 GSM bit.**
-One ramp shape was described using 1 coefficient every ½ bit ⇨ **16 coefficients**
-Output data rate **was every 1/8 GSM bit** by **interpolating linearly** by a factor 4.

**Now in Locosto application,**

-TX ramping up and ramping down are achieved during **5 GSM bit.**
-One ramp shape is described using 1 coefficient every 1/4 bit ⇨ **20 coefficients**
-Output data rate **is every 1/4 GSM bit (4*270.833kHz). No more interpolation.**

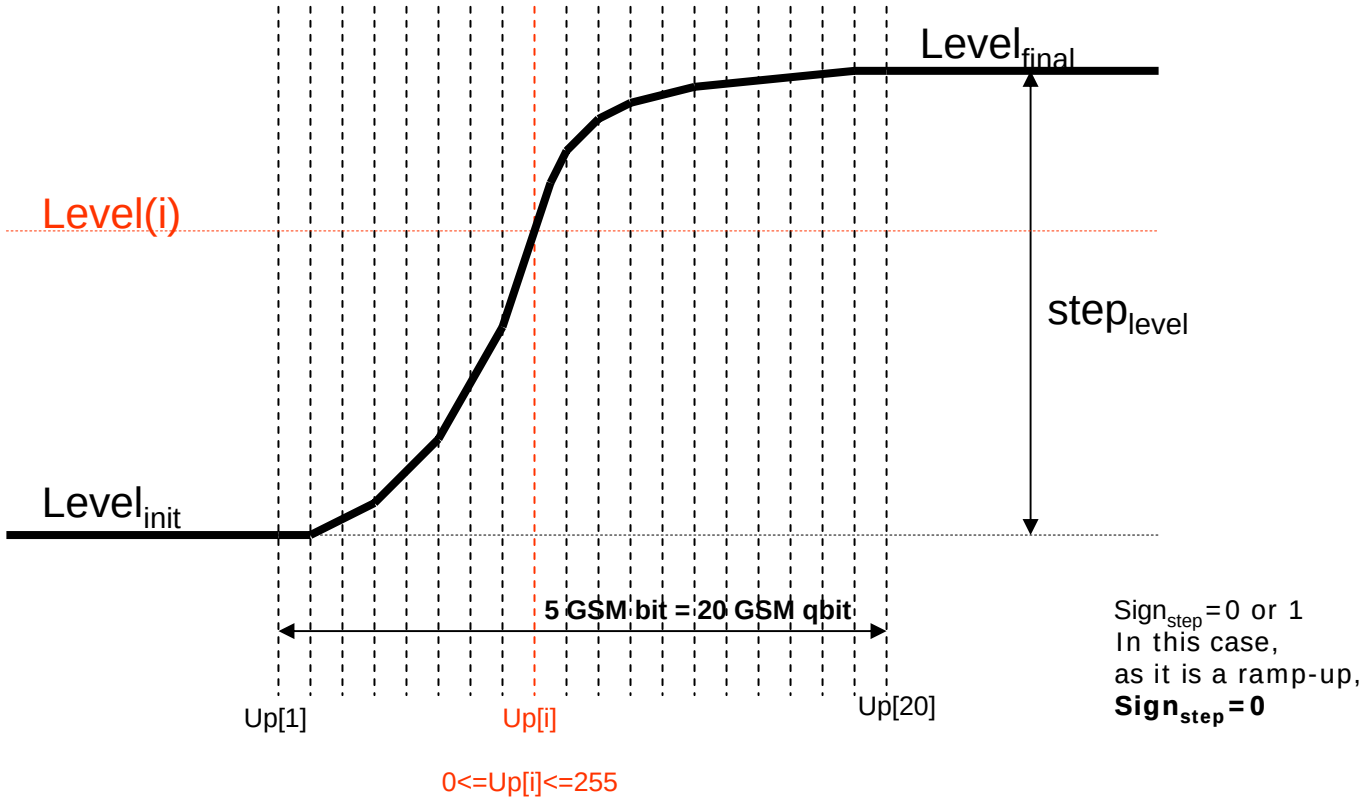
**Remains unchanged:**

-Coefficients are still **8-bit coded**.
-Coefficients are stored in a dedicated RAM
-Last power level is stored for smooth transition in multi-burst mode
-Ramping profile is given by the following equation :

$$Level(i) = Level_{init} + (step_{level} / 256) \cdot \left( up[i] * (1 - sign_{step}) + dw[i] * sign_{step} \right)$$

# DXP-APC: Ramp Generation

$$Level(i) = Level_{init} + (step_{level} / 256) \cdot \left( up[i] * (1 - sign_{step}) + dw[i] * sign_{step} \right)$$

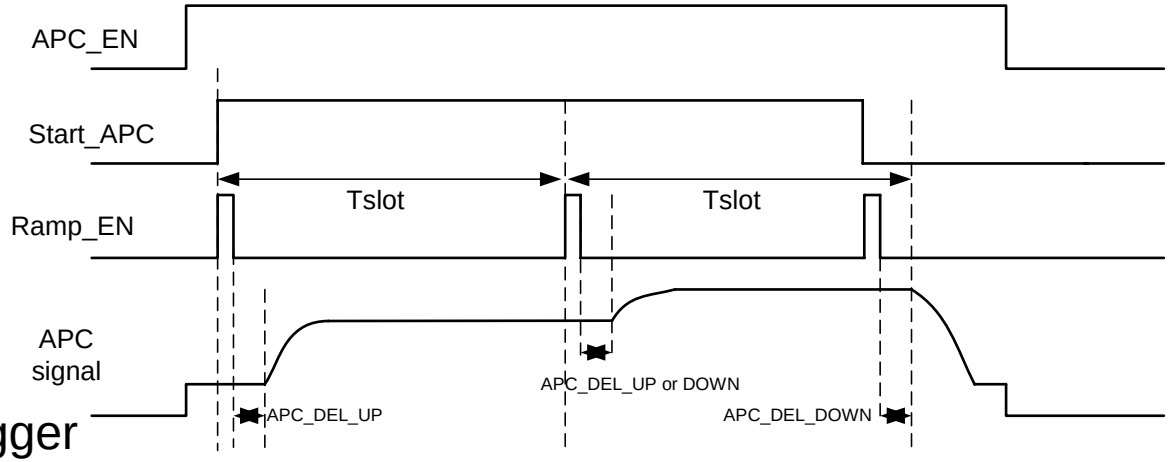


# DRP - APC

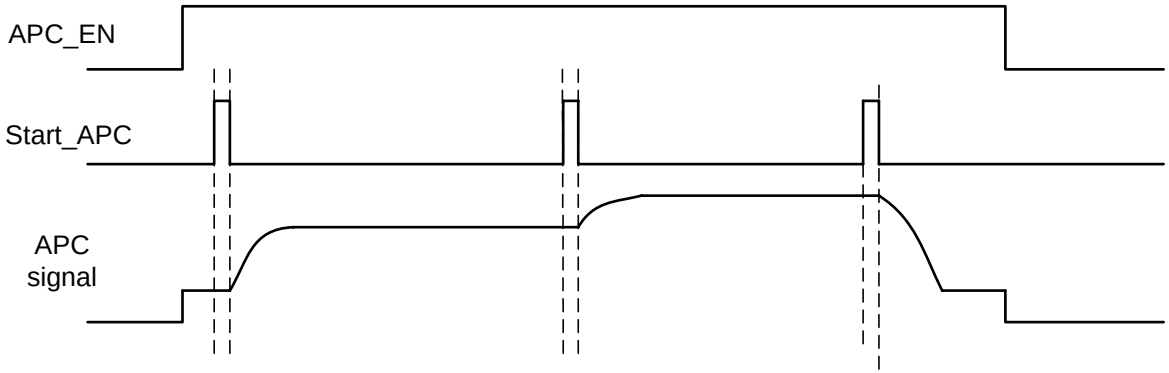
- Ramp timings and triggering
  - Simple interface for enabling/triggering APC ramp up/down
    - APC_LDO_EN : controls APC LDO ON/OFF
    - APC_EN : enables APC core
    - APC_START : Begins ramp sequencing
  - 2 modes
    - Internal sequencing : ramps are automatically generated each timeslot (default used in Locosto)
    - External trigger : TSP is responsible for triggering ramp up/down each burst
  - Programmable delays between trigger and start of ramp up/down
    - APC_DEL_DWN : delay between trigger and start of ramp up
    - APC_DEL_UP : delay between trigger and ramp down

# DRP - APC

- Internal sequencing (default mode)




- External trigger

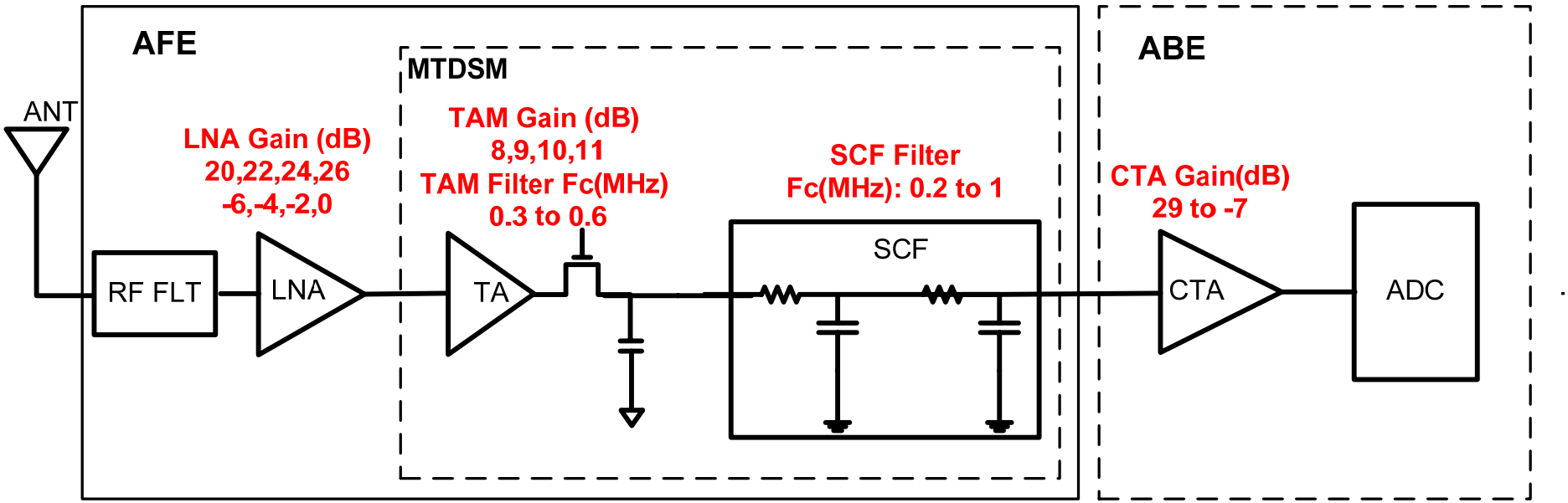


# Digital RF Processor

## Receiver
## Gain strategy

# Receiver Gain-Settings

- Sub-block gains : LNA, TA/Mixer, CTA
- Filter corners : TA/Mixer, SCF



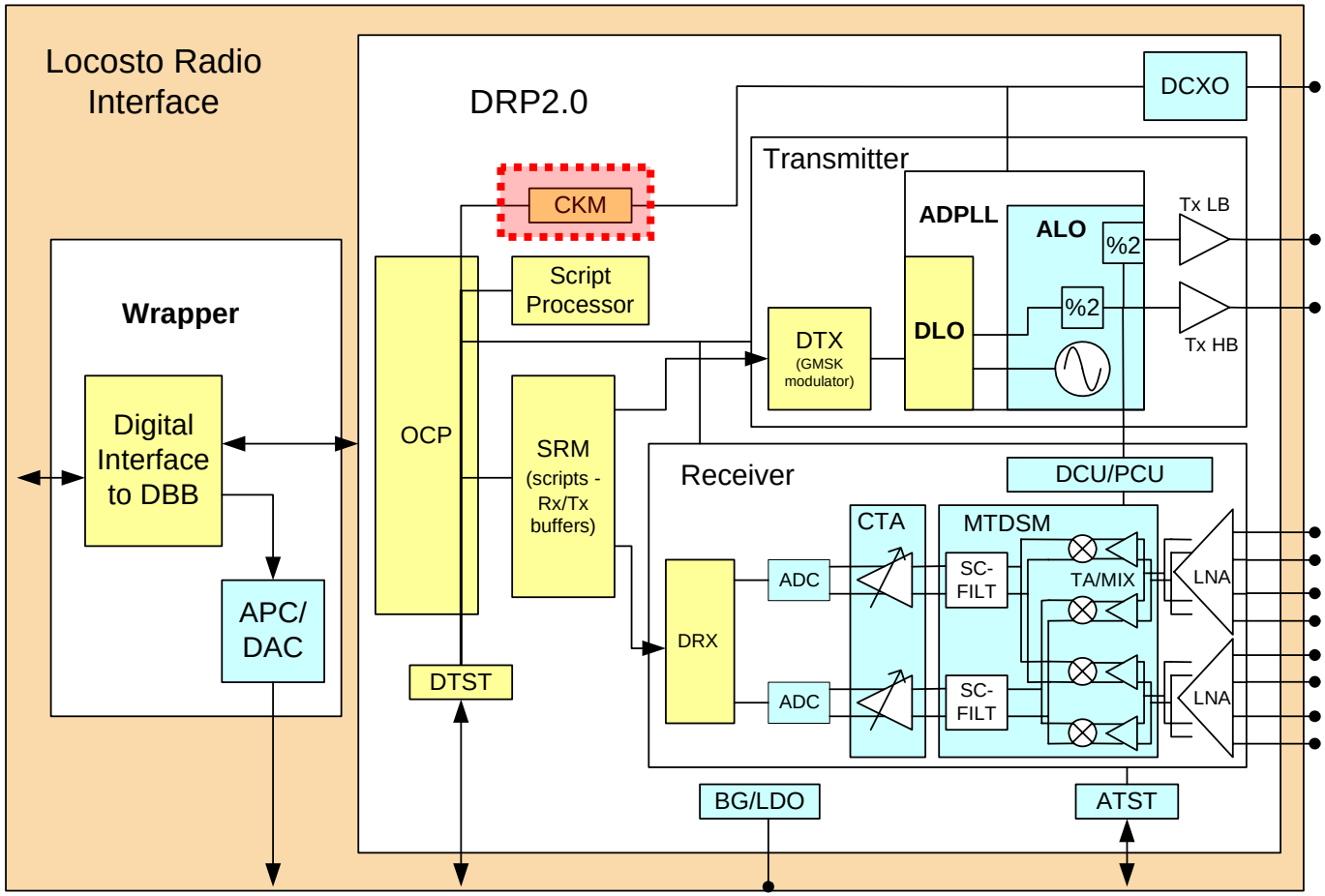
# Receiver Gain-Settings (cont.)

- The DRP will split the global gain across the receive chain according to internal strategy (calibration/compensation).
- 2 levels should be pre-defined for AFE gain (only 1 bit kept in case more steps needed)
  - Low Gain (11 dB)
  - High Gain (38 dB) : 24 dB LNA / 10 dB TA / 4.4 SCF
- (9) levels should be defined for ABE gain: 0, 2, 5, 8, 11, 14, 17, 20, 23 dB
- 2 bandwidths settings should be available for switched cap filter SCF (270 kHz, 170 kHz)

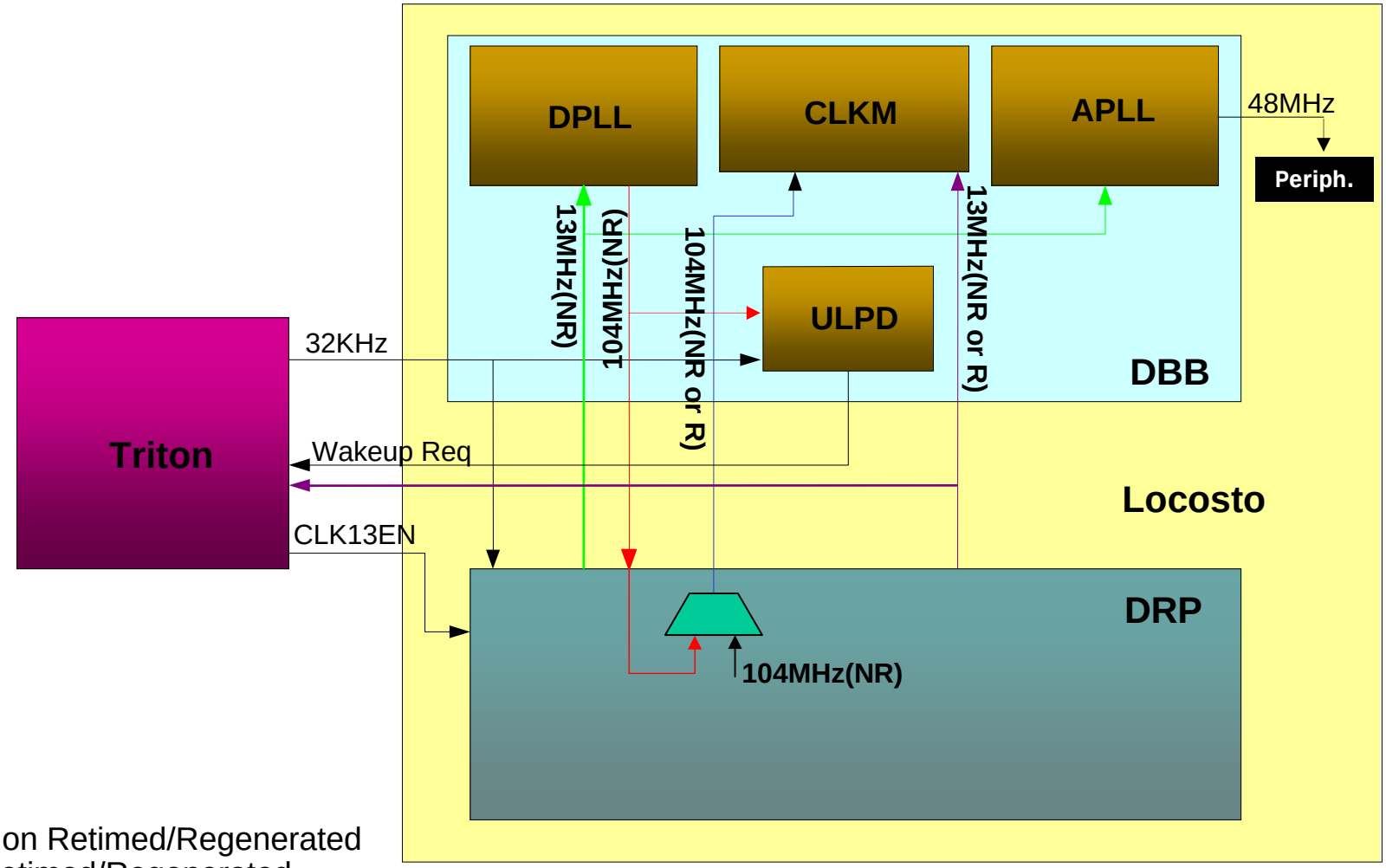
# Digital RF Processor

# Clock management

# Clock manegement



# Clock Management Overview



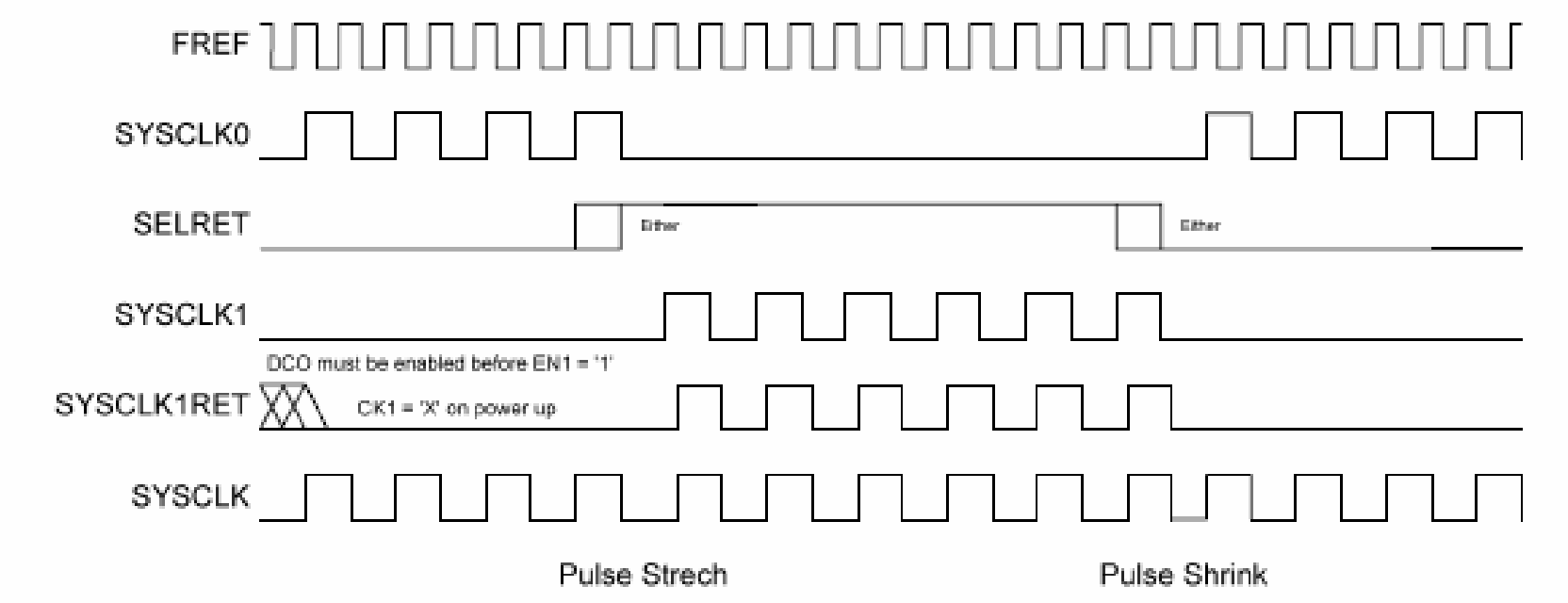

NR - Non Retimed/Regenerated
R - Retimed/Regenerated

# System Clock

- In order to reduce the digital switching noise, it is desirable to have all DBB clocking signals synchronous to the DRP's local oscillator (LO) clock.
- The DRP's CKM function includes a re-synchronization mechanism offering the capability for locking reference clock on the LO clock edges.
- The DRP outputs to versions of the 13MHz clock:
  - ***DRP_DBB_DPLL_CLK*** which is a divided by two version of FREF (26MHz). This clock is a non retimed 13MHz clock and is only used by the DPLL (DPLL needs a non retimed version of the system clock due to the cycle accuracy required by the gauging algorithm).
  - ***DRP_DBB_SYS_CLK*** is the 13MHz system clock sent by the DRP to the DBB clock manager. This clock can be retimed or non-retimed.
    - Default mode: clock is retimed when ADPLL is in tracking mode (switch from non-retimed to retimed clock is managed automatically by the DRP)
    - Disable mode: by SW, retiming can be completely disabled.

# System Clock Retiming

- Retiming consists in passing the non retimed clock into flops operating at CKV (RF clock), CKV/2 or CKV/8 frequency. Clocks are not re-generated (stable clock frequency) but just re-synchronized with a CKV derived clock. The muxing between retimed and non-retimed modes of operation does not lose any pulses.



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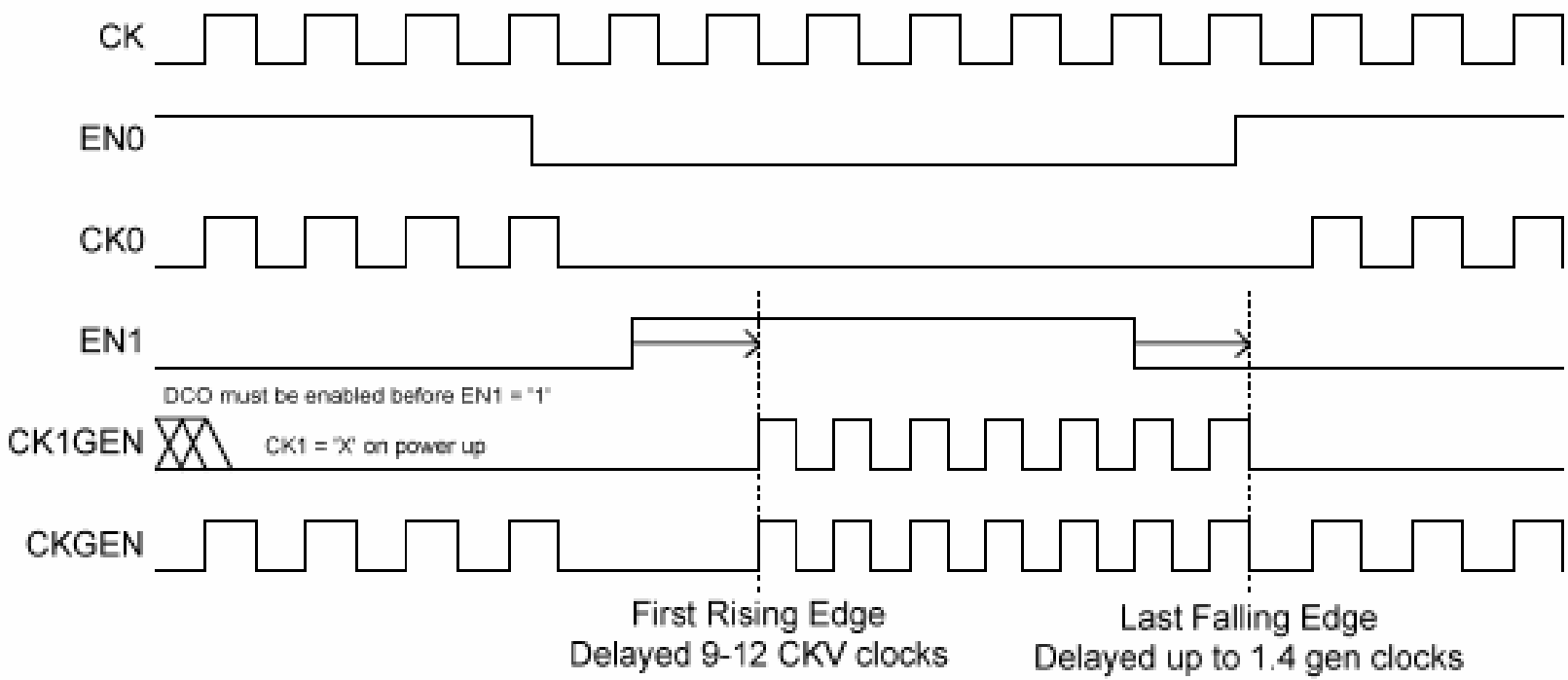
# DSP/MCU Clock Regeneration

- To reduce the digital switching noise, MCU/DSP 104MHz clock also needs to be synchronous to the RF clock (ADPLL clock).
- DPLL block uses the DRP non-retimed 13MHz clock to generate the 104MHz. This 104MHz from DPLL is only used by ULPD (for gauging).
- MCU/DSP don't directly use this clock but use a regenerated version of this clock.
- DPLL clock is sent to DRP for regeneration. DRP muxes this clock with a generated version of this clock to provide the DSP/MCU clock.
- When RF is in idle state, the clock output by DRP is the DPLL clock.
- When in Tx or Rx and once the ADPLL has settled (when in tracking mode), DRP creates the DSP clock by dividing the ADPLL clock by integer value.
- As a consequence, while in Tx or Rx, the MCU & DSP clock can vary from 104.1 MHz to 110.4 MHz depending on the Rx/Tx RF channel.

# DSP/MCU Clock Regeneration



# DSP/MCU Clock Regeneration

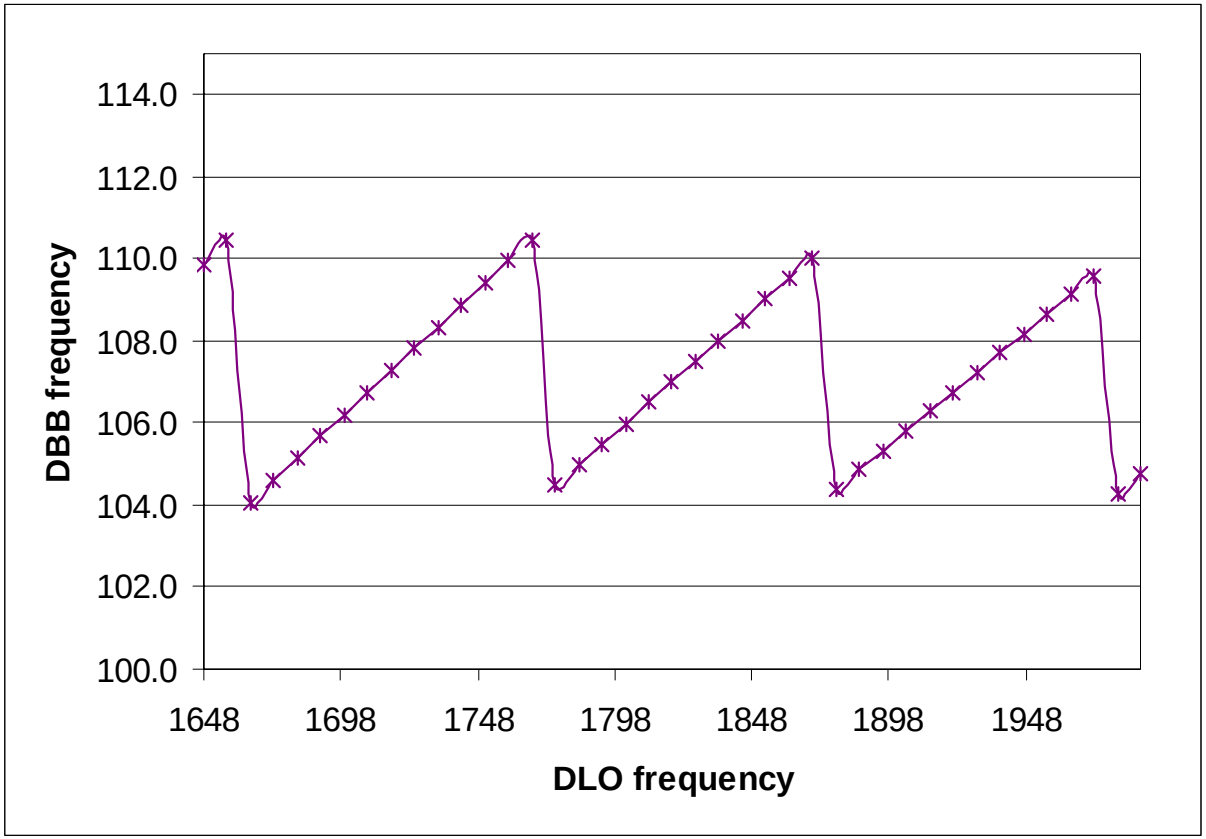
- Switch between DPLL clock and regenerated clock is completely handled by DRP, no action is required from DBB (DBB can only choose by SW programming to completely disable the retiming).

- Division factors inside DRP are chosen so that minimum MCU/DSP frequency is 104MHz. So when regeneration is activated (when ADPLL is in tracking mode), DSP and MCU will see their respective clocks increased.

- ADPLL frequency varying from 1648MHz to 1990MHz depending on the RF channel, a division factor going from 15 to 19 is applied to the RF clock in order to guaranty a minimum DSP/MCU clock frequency of 104MHz.

- Hence DBB frequency can then vary from 104.1 MHz to 110.4 MHz depending on the RX/TX RF channel.

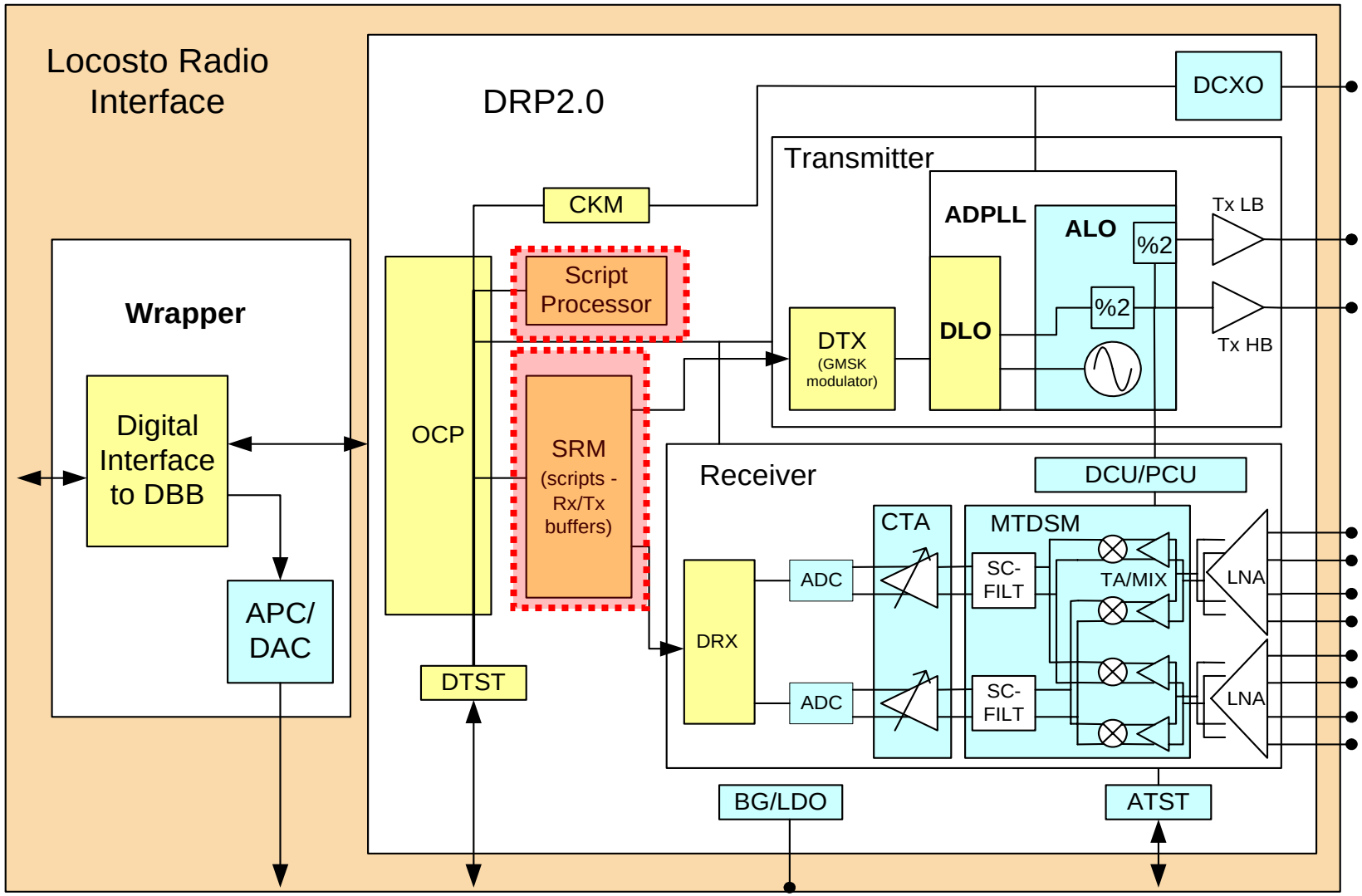
# DSP/MCU Clock Regeneration



# Digital RF Processor

# Script Processor and SRM

# Script Processor & SRM



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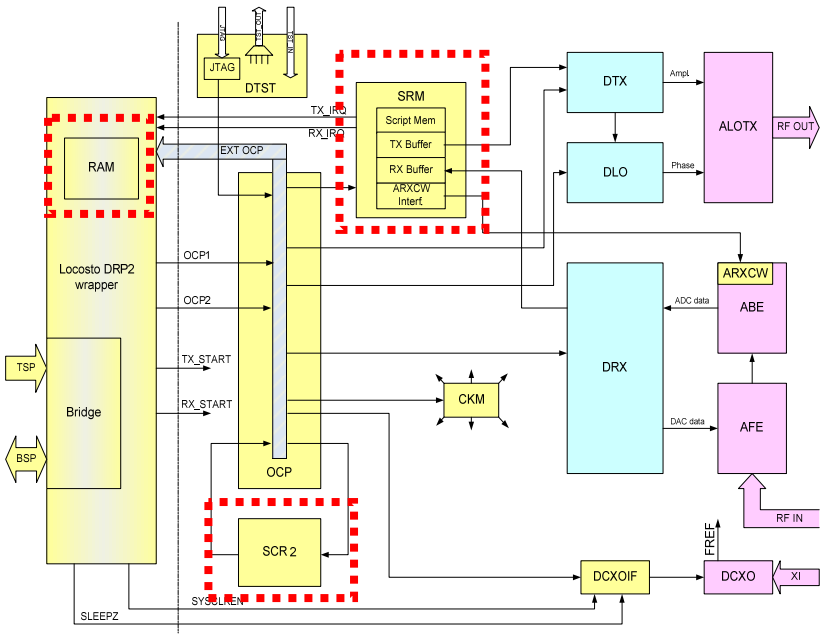
# Control-Centric Diagram of DRP2




| Module | Functions |
|---|---|
| SCR2 – Second Generation Script Processor | Processor used for DRP control and compensation |
| SRM – Shared RAM Module | RX and TX data buffers; script buffer; analog control word regs. |
| OCP – OCP Module | OCP address decode and master/slave connections |
| DTST – Digital Test Module | JTAG access and digital test mux |
| DCXOIF – DCXO Interface Module | DCXO interface; power-up state machine |
| CKM – Clock Module | Clock gating and muxing; clock division and control |
| ARXCW – ABE control | Registers that control ABE configuration |
| Locosto DRP2 Wrapper | Interface to Calypso DBB; Extra RAM for script storage |

# Script Processor

- The Script Processor is a DRP2 module whose main purposes are:
  - Provide simple API to the digital baseband
  - Perform calibration and compensation of the analog and RF front-end

- SCR2 can perform operations based on a preloaded “scripts”

- SCR2 has the following hardware resources:
  - Registers (scalar, vector)
  - 32 bit ALU, Multiplier, a sequential divider
  - Boolean logic
  - OCP master and slave interfaces
  - Wall-clock timer
  - Wait on hardware event

- The SCR2 has no internal RAM, so it uses a section of the SRM memory to store program instructions (scripts) and data. It can also use external RAM (in Locosto wrapper) for storage. There is no performance difference between using SRM RAM or external RAM as Locosto wrapper supports zero wait state response.

# SCR2 Script Control

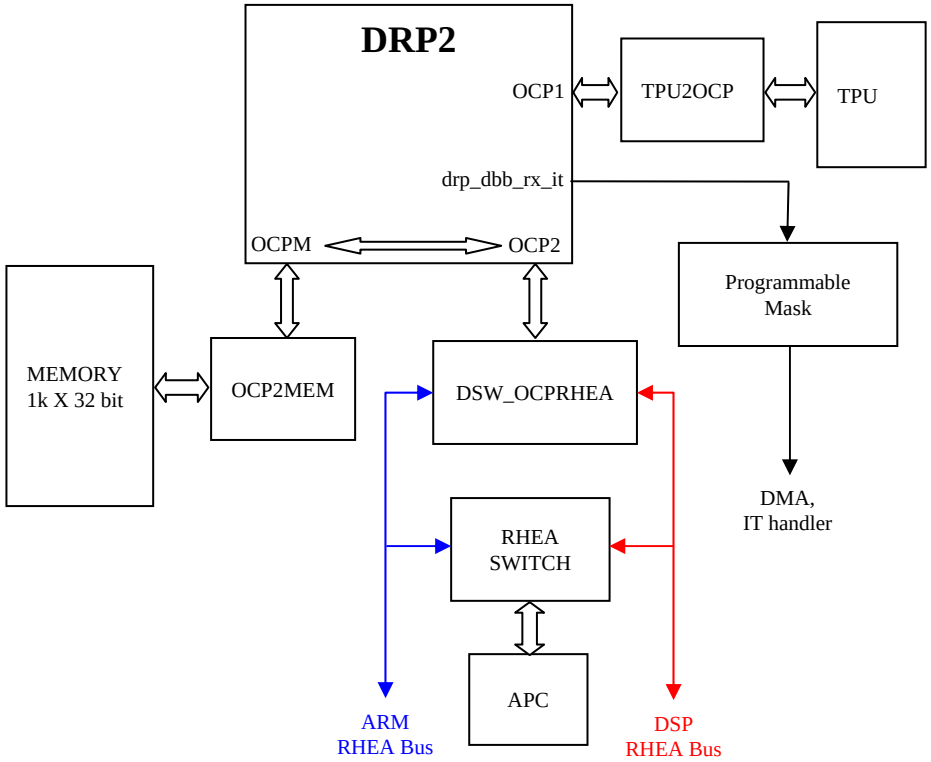
- The SCRIPT_PTR_0 to SCRIPT_PTR_15 registers are used for storing the start addresses of the scripts.
- The SCRIPT_START register has to be programmed with script numbers that need to be executed on a particular triggering condition.
- There are two ways of starting a script:
  - Event-triggered. Currently edges of TX-START and RX-START signals are considered for script triggering.
  - Set the script_start bit in the SCRIPT_START register. Writing ‘0’ to this bit stops any running script.

# Shared RAM Module

- The Shared RAM Module (SRM) provides the following functions:
  - Single time-shared data storage RAM used for TX data, RX data and scripts
  - Memory-mapped access to the control words for analog modules
  - RX data buffer and interface to the DRX module
  - TX data buffer and interface to the DTX module
  - Script processor instruction buffer
  - CALC data buffer for SCR
  - Read access to DRP2 EFUSE data (where bandgap trimming values are stored)
- RAM size is 1024 * 32 bits words (4kbytes) and mapped into the OCP memory space

# SCR2 Wrapper Memory

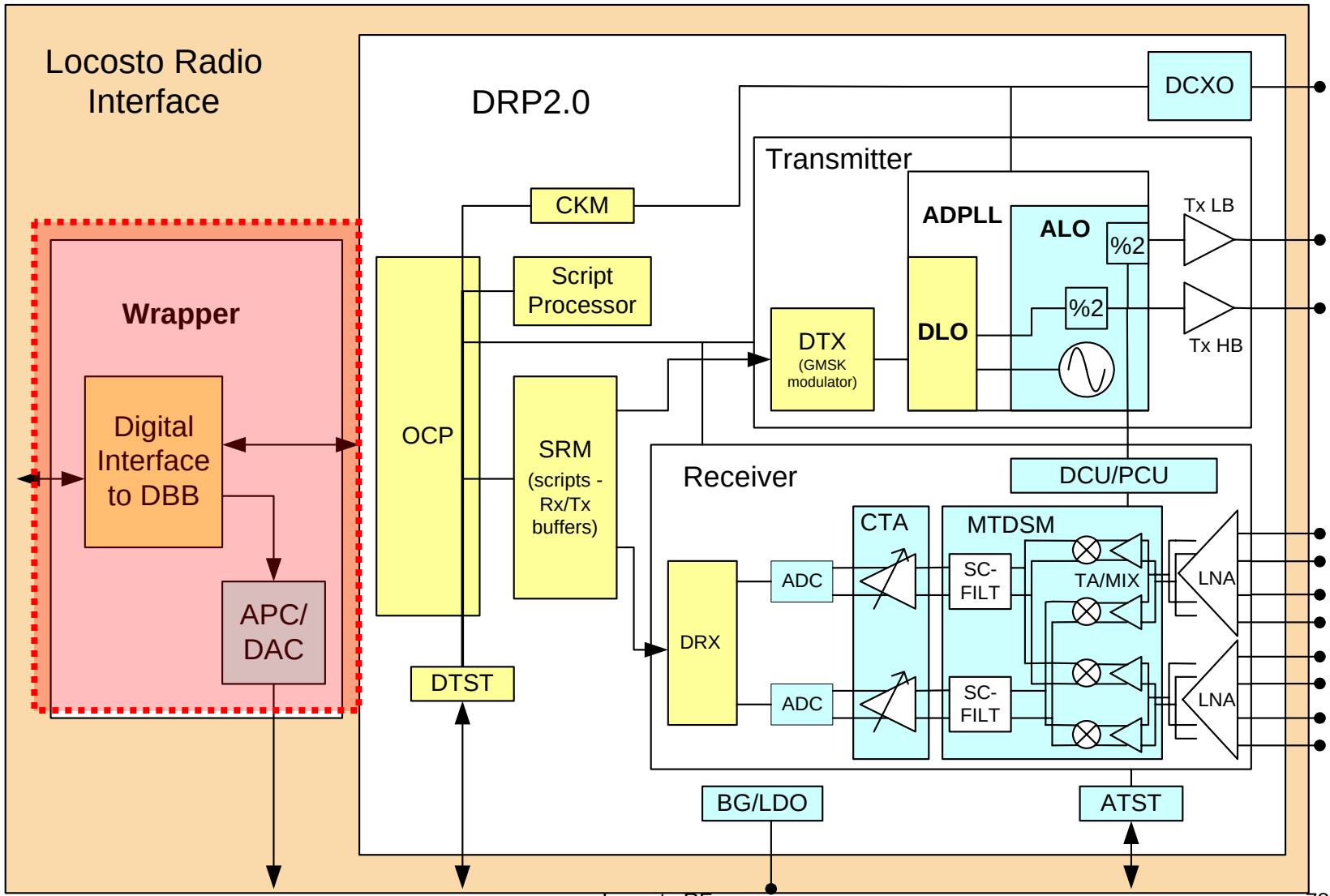
- 4 kBytes RAM added into the wrapper to extend SCR memory:
  - Needed to store the scripts, compensation algorithms and calibration tables
  - This memory can be accessed via OCP bus (OCM port) => it is accessible by the 3 processors (SCR / MCU / DSP)



# Digital RF Processor

# DRP Wrapper

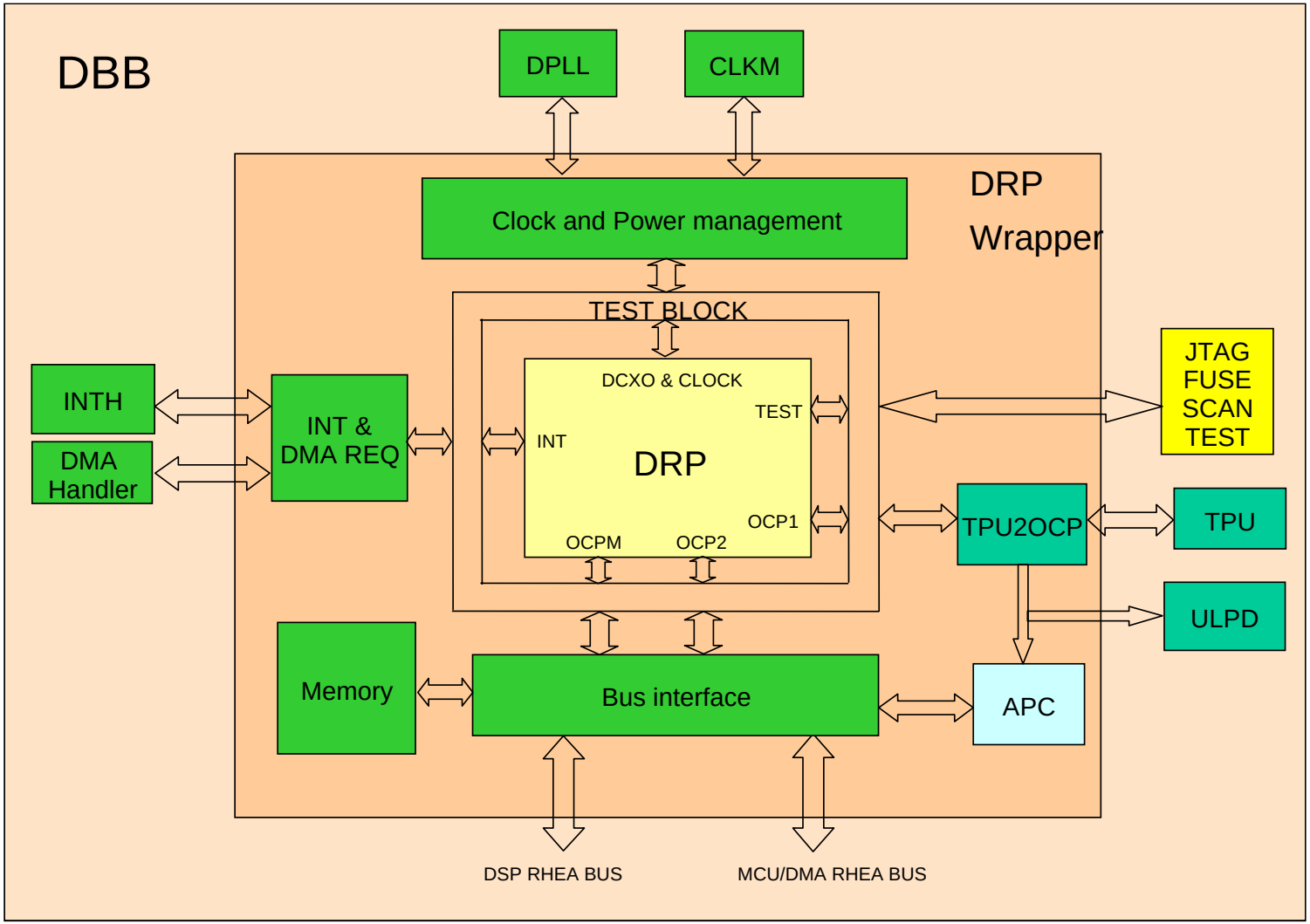
# DRP Wrapper



# DRP Wrapper

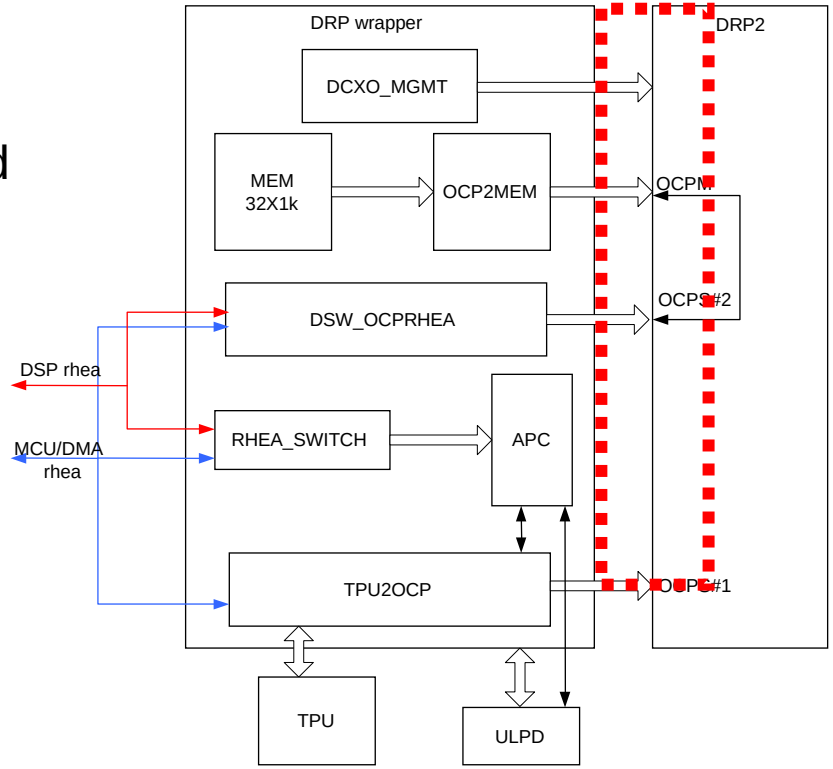
- Bus I/F (RHEA/OCP bridges)
  - DSP-DRP Control & data path
  - MCU/DMA-DRP Control & data path
- TPU2OCP I/F
  - Q-bit timed event control from DBB to DRP
  - Q-bit timed event from DBB to Front End Module & Power Amplifier (TSPACT's)
- Power, reset & Clock system management
  - Power-up sequencing
  - Programmable startup timer (RHEA bus)
  - DCXO & Retimed Clock control
- Interrupt & DMA Request
  - Rx events Programmable mask counter (RHEA bus)
- Calibration/Compensation RAM
  - 4-KByte RAM Shared DBB/DRP
  - XIP for DRP's Script-Processor
  - DSP & MCU/DMA access for calibration scenario load/pre-set
- APC function
- TEST & debug DBB/DRP alignment (TAP/JTAG, eFuse…)

# DRP Wrapper Overview



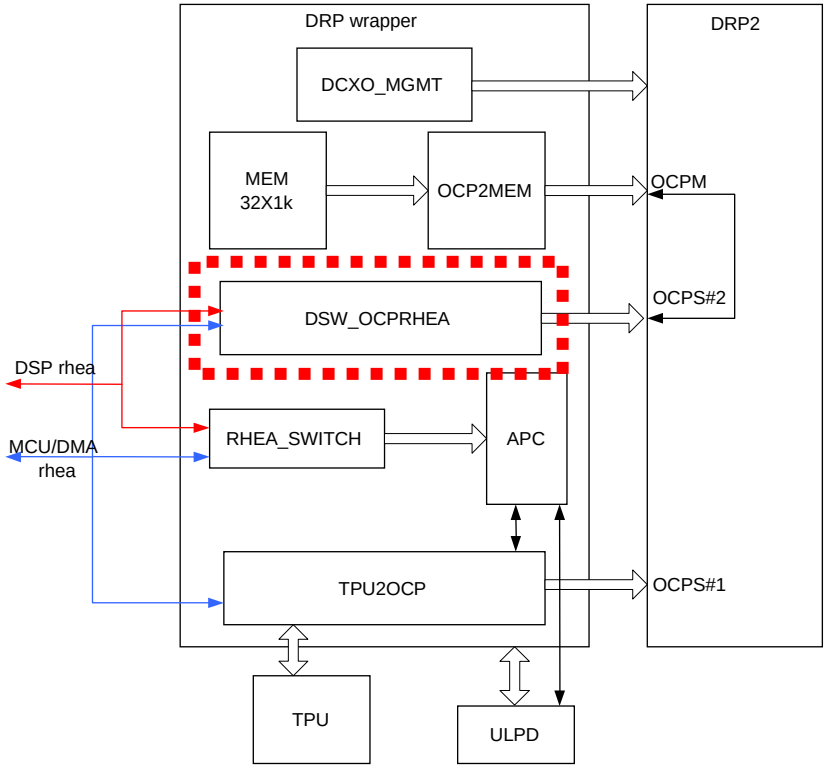
# Bus Interface

- DRP2 has three OCP busses: two slaves and one master managed by the internal script processor.
- OCP1 and OCP2 slave busses are two identical 16 bits data interfaces dedicated to access internal registers.
- OCP1 bus has the priority on OCP2 bus.
- OCP master bus is used by the script processor to access scripts located in wrapper memory.
- All the memory space (8 Kbytes) allocated to the DRP2 is accessed through OCP1 & 2.



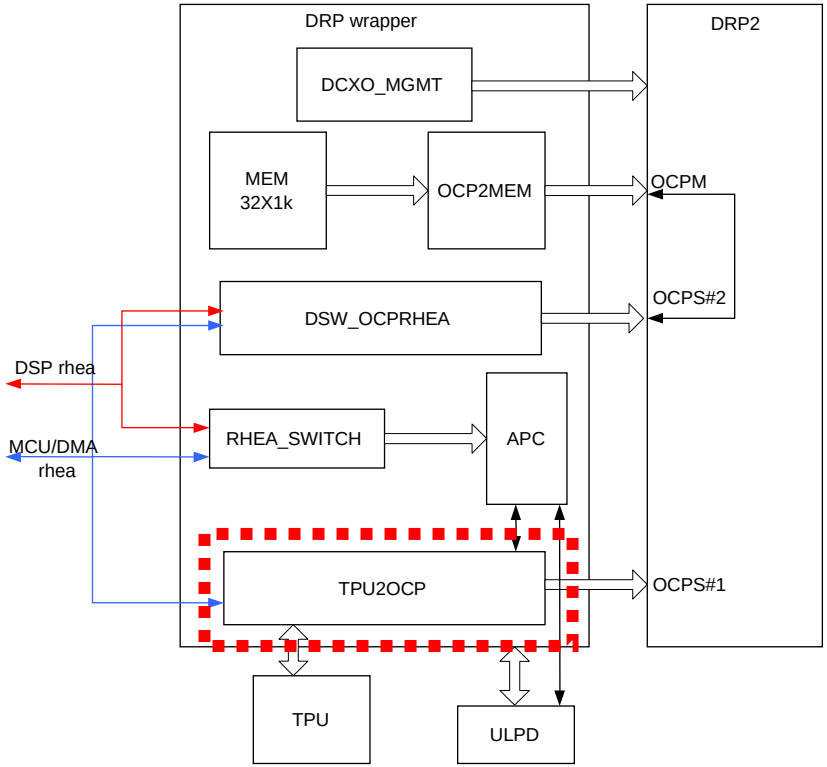
# DSW_OCPRHEA

- MCU (DMA) and DSP are both connected on OCP2 bus and they have their own Rhea bus.
- The arbitration and conversion from Rhea to OCP is done by the DSW_OCPRHEA module.



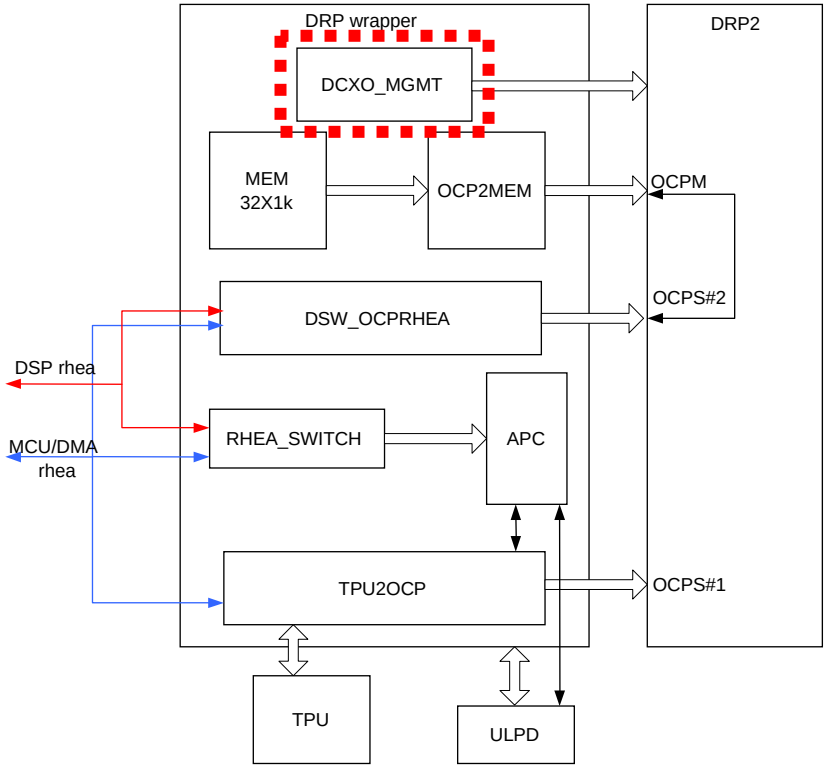
# TPU2OCP

- As TPU access are more constrained, it is connected on OCP1 (OCP1 higher priority than OCP2) bus through the TPU2OCP module.
- TPU used a parallel 8 bits data bus to access the TPU2OCP, which executes the OCP access when requested by TPU.
- TPU2OCP module is based on the previous TSP interface with an OCP master interface replacing the serial interface.

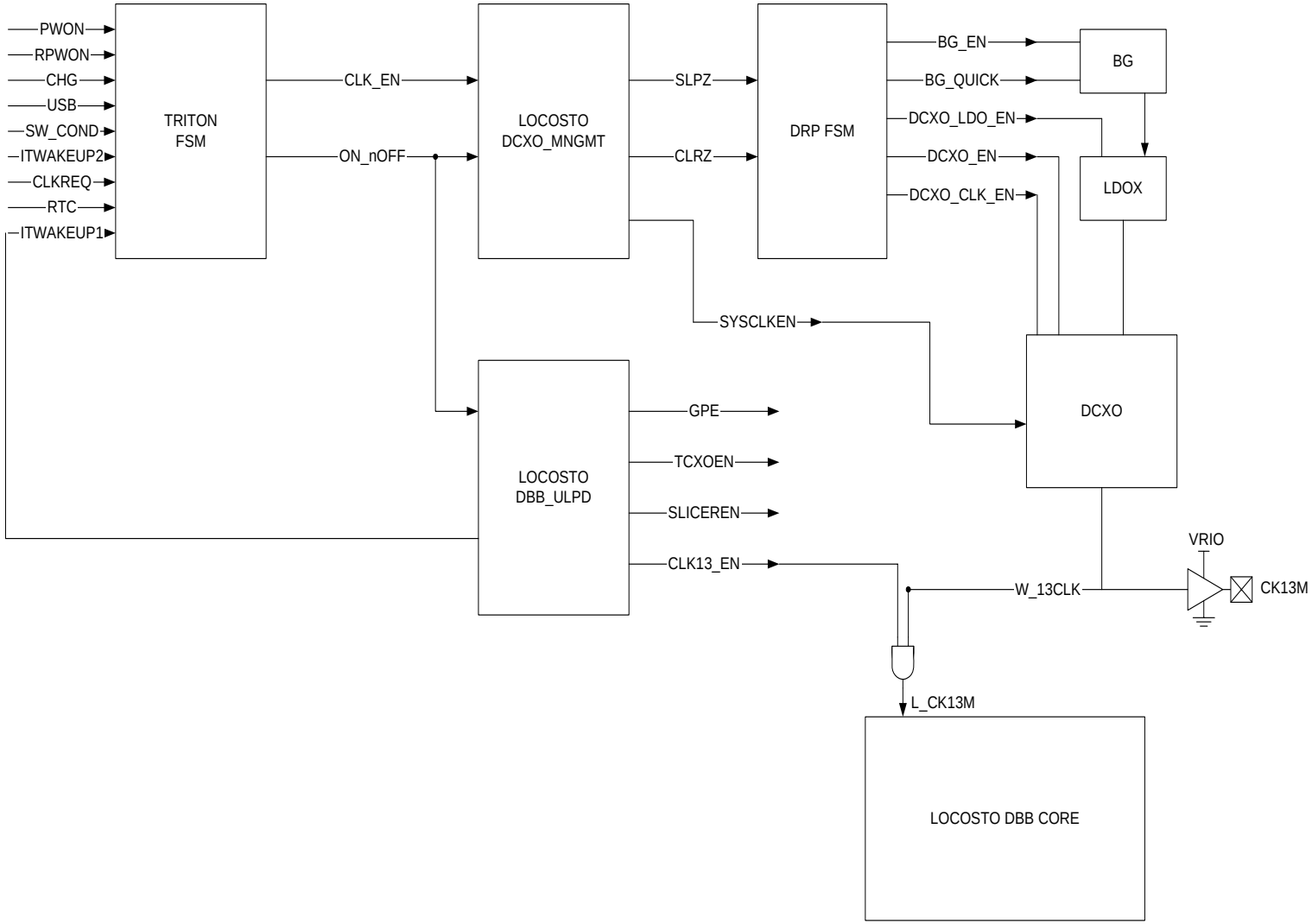


# DCXO MANAGEMENT

- **DCXO_MGMT module manages the DCXO clock in the DBB chip.**
- **It manages DRP2 DCXO interface during the following events**
  - Power-up
  - Sleep on
  - Wake-up
- **It requests and cuts the DCXO clock according to the external Triton clock request.**



# DCXO Management in System View

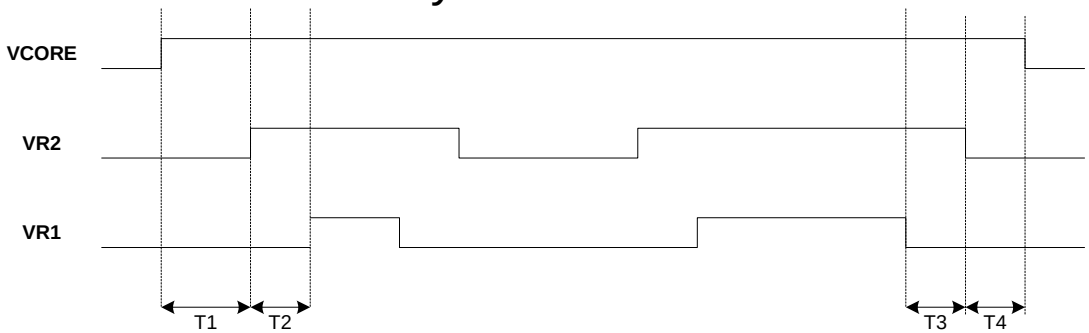


# Digital RF Processor

# DRP Timing

# Power On Sequence

- 26MHz is switched on and Triton LDOs are on
- Scripts are loaded by the MCU to the script processor memory (SRM)
- Then MCU switches on the RF LDOs  by calling the **REG_ON** script
- REG_ON script is triggered by RF_INIT
  - VCORE is provided first at start-up
  - Then VR2 (DCXO) is provided by Triton, then VR1 for other RF blocks
  - VCORE and VR2 sequencing is controlled by Triton FSM
  - VR1 is switched ON/OFF by SW




| Power Domain | Enabling Order | Disabling Order |
|---|---|---|
| VCORE | 1st | last |
| VR2 | 2nd (T1= TBD*T32k) | 2nd (T4=TBD*T32k) |
| VR1 | last (T2= TBD*T32k) | 1st (T3= TBD*T32k) |

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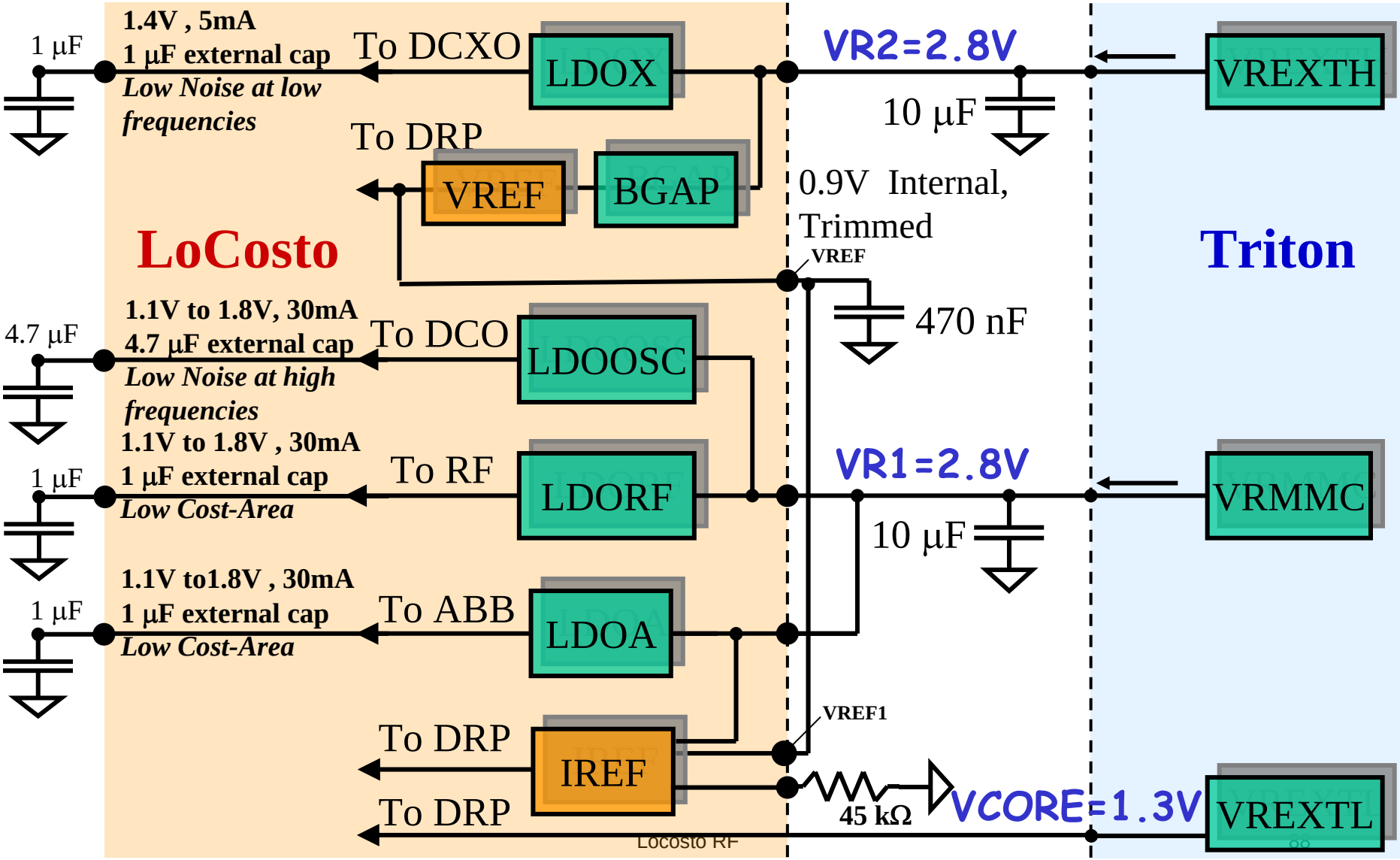
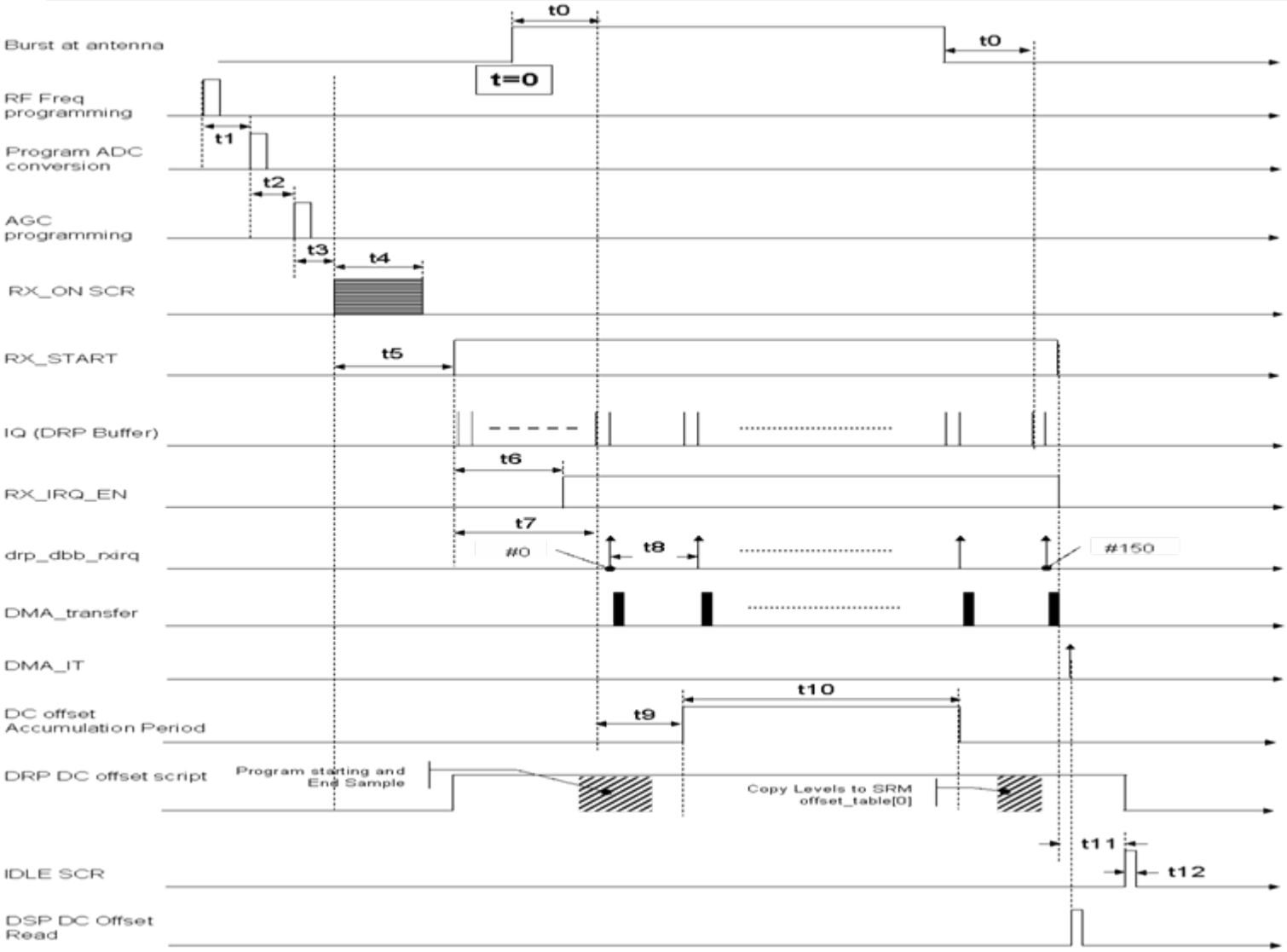
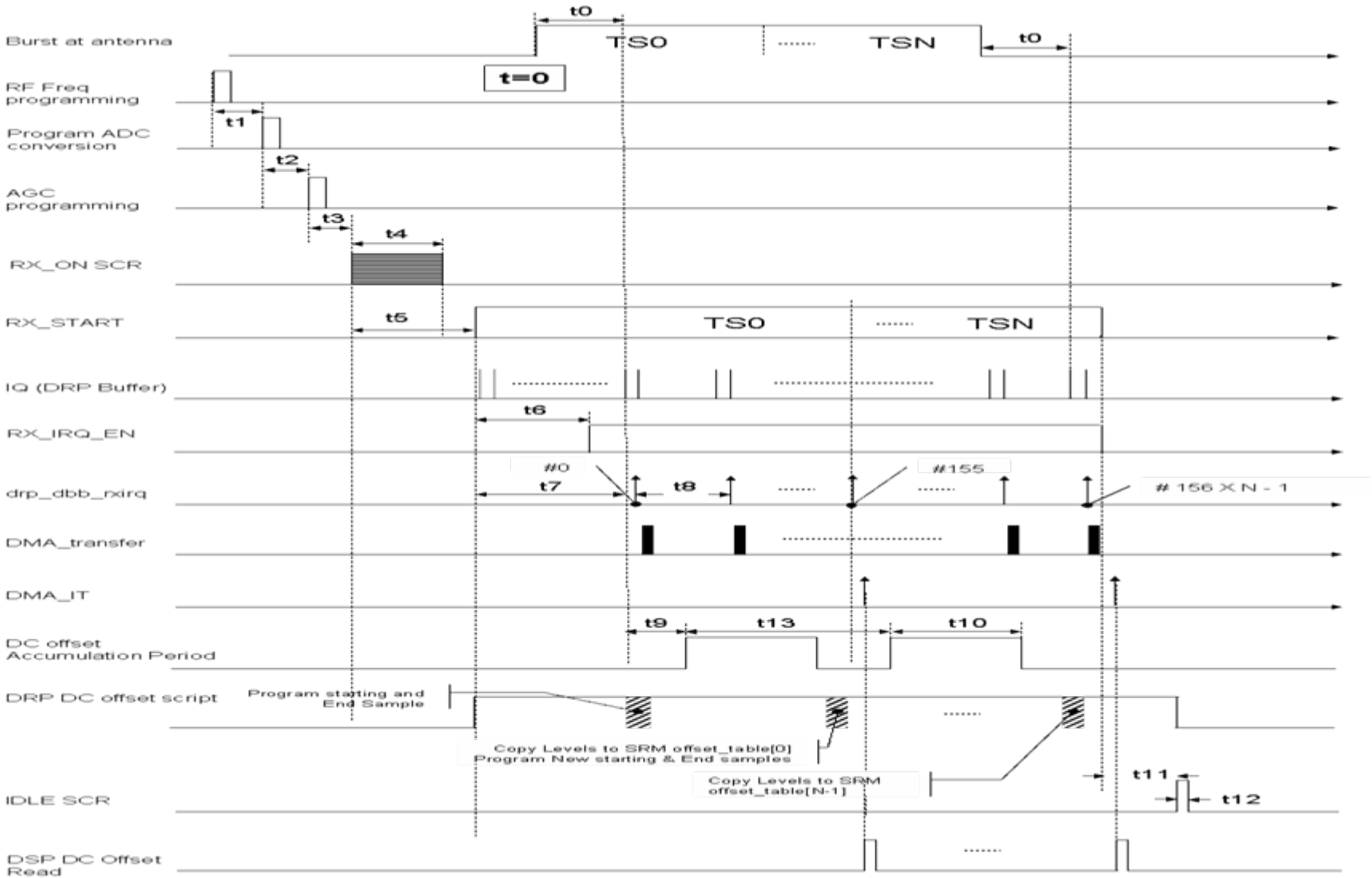
# DRP External Supply Voltage



# RX Operation – Single Slot

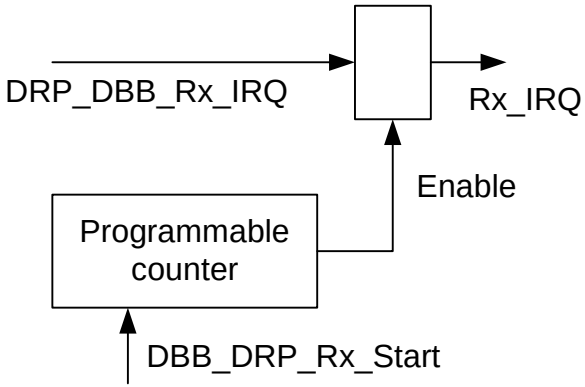


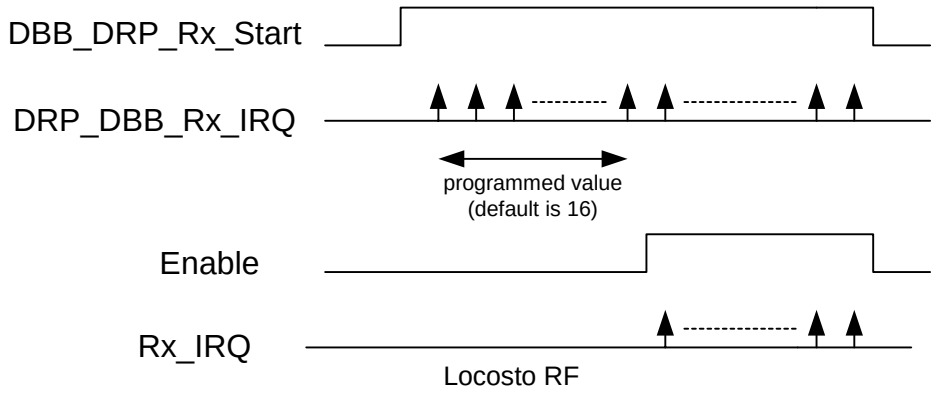
# RX Operation – Multi-Slot



# Masking of The First Rx Interrupts

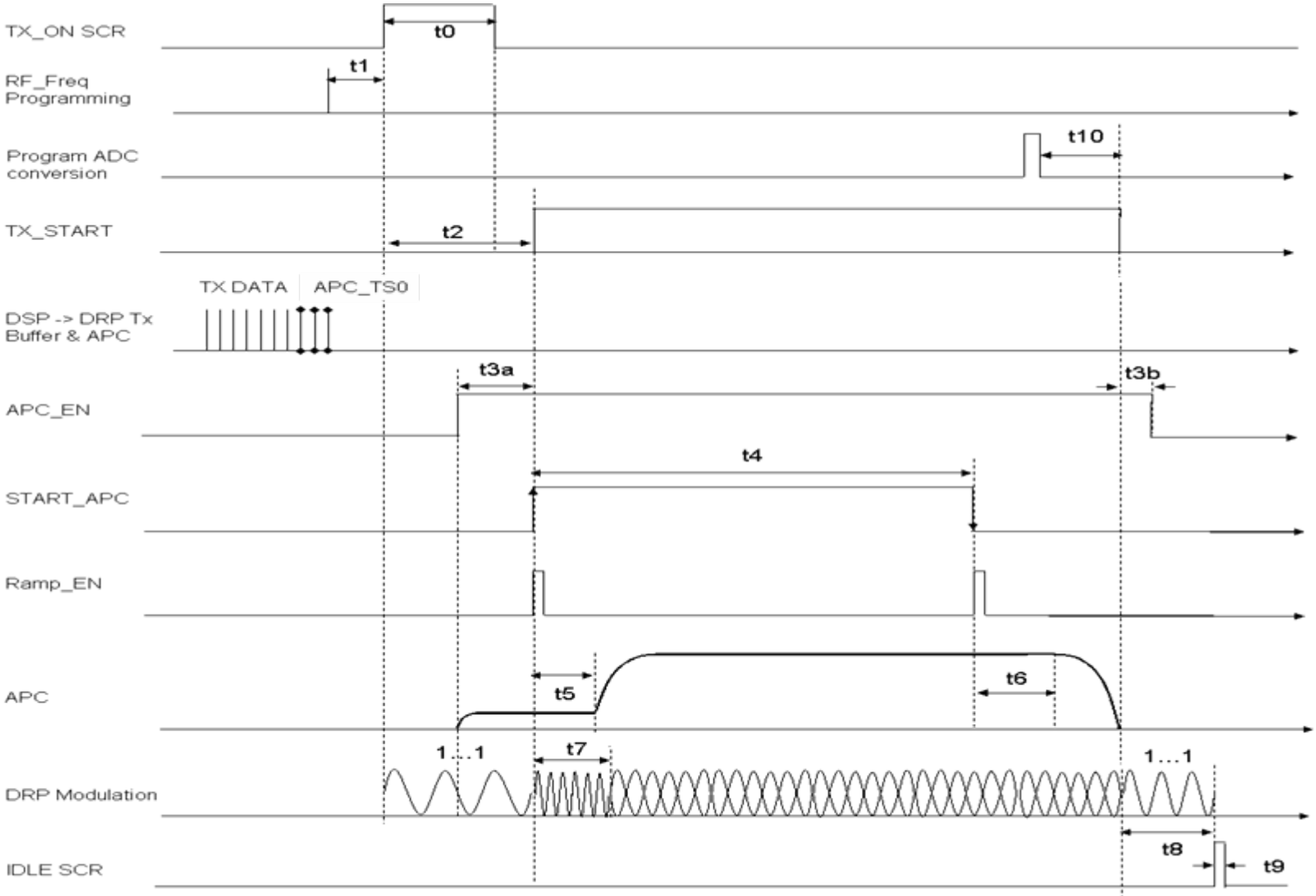
- When RX_Start raises, digital Rx clocks are resynchronized so that 100kHz sine wave has a known initial phase.
- Due to the CSF group delay, first Rx I/Q samples are distorted by this re-synchronization and therefore have to be dropped.



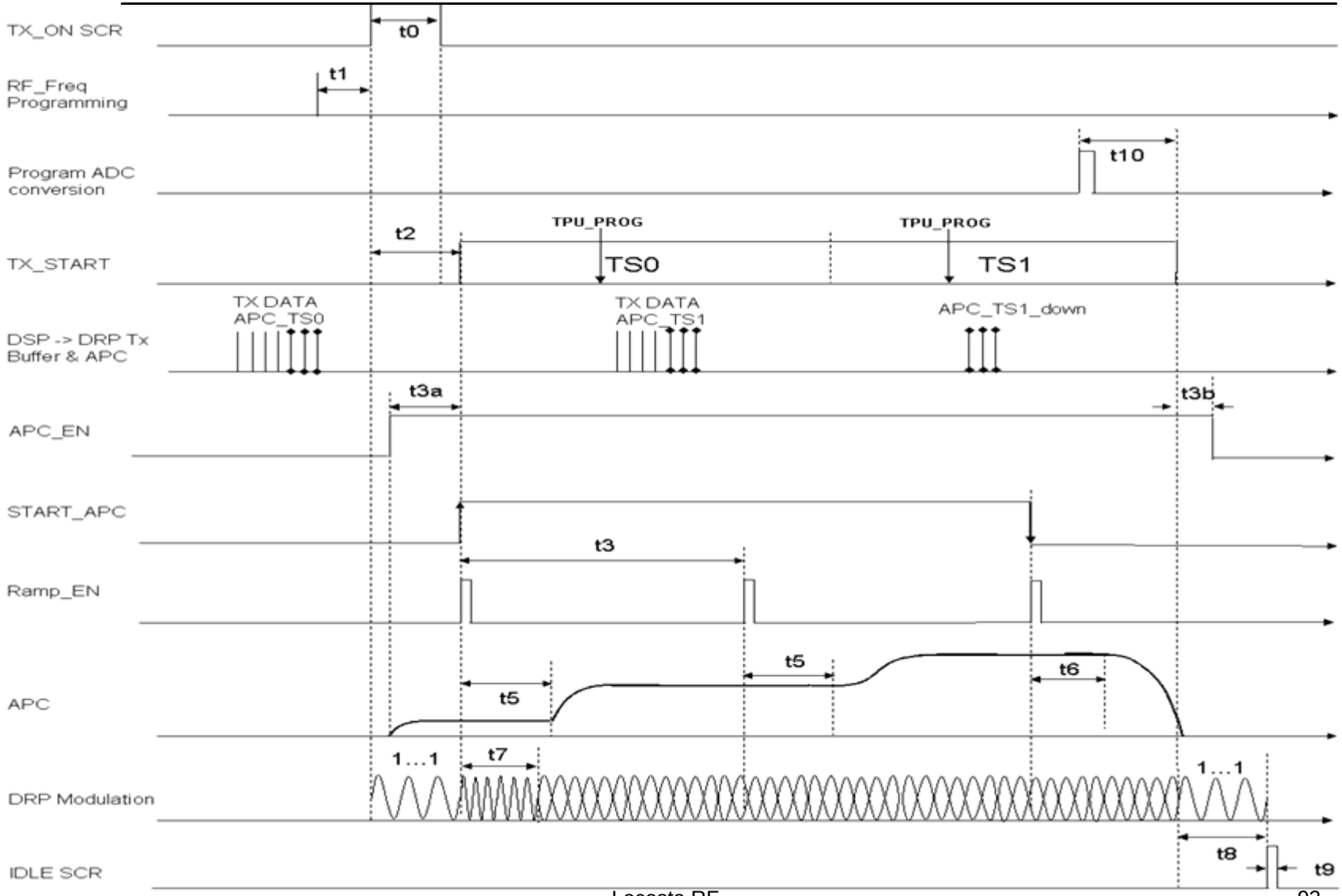




Locosto RF

# Tx Operation - Single Slot



# TX Operation - Multi-slot



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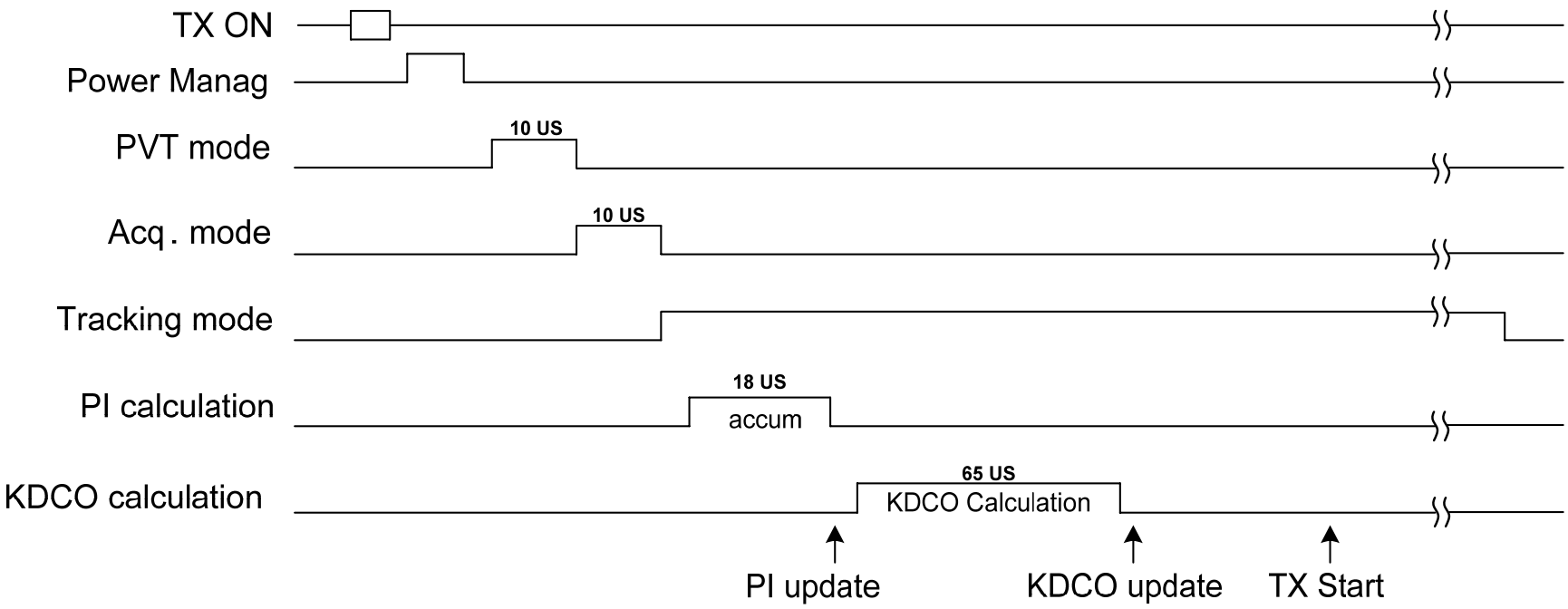
# TX Operation Timeline



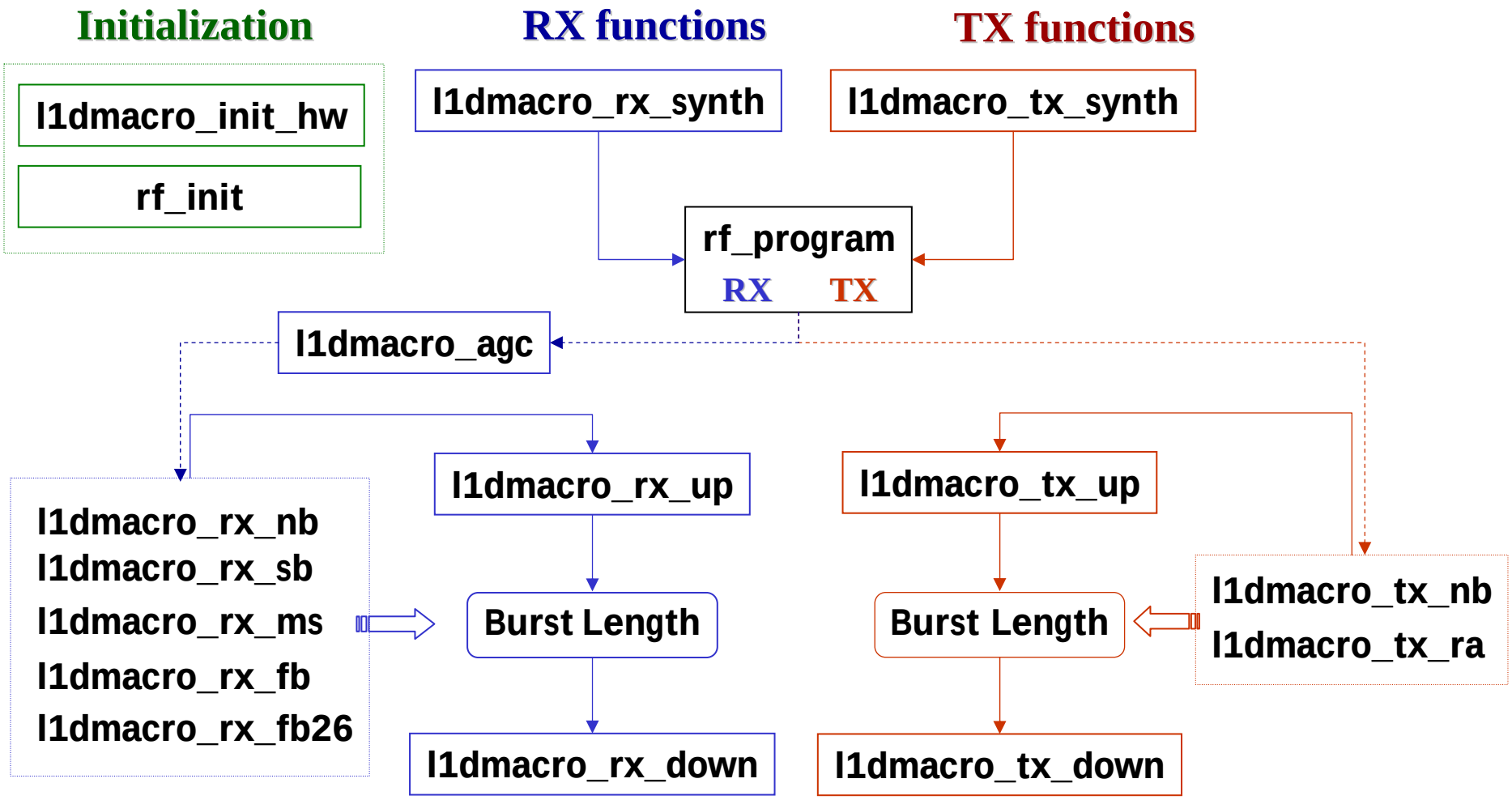
# TPU Drivers

- TPU is responsible for the real-time control and programming of DRP

- Receive operation
  - Normal Burst
  - Synchronization Burst
  - Power Measurement
  - Frequency Burst

- Transmit operation
  - Normal Burst
  - Access Burst

# TPU Drivers


Initialization
RX functions
TX functions
l1dmacro_init_hw
rf_init
l1dmacro_rx_synth
l1dmacro_tx_synth
rf_program
RX
TX
l1dmacro_agc
l1dmacro_rx_nb
l1dmacro_rx_sb
l1dmacro_rx_ms
l1dmacro_rx_fb
l1dmacro_rx_fb26
l1dmacro_rx_up
l1dmacro_tx_up
Burst Length
Burst Length
l1dmacro_tx_nb
l1dmacro_tx_ra
l1dmacro_rx_down
l1dmacro_tx_down

# TPU Programming

- DRP registers are constituted by:
- 16 address bits; 16 data bits
- 1 TPU write to DRP register is done by a 32 bits transfer
  - 5 TPUMOVE instructions (2 for address, 2 for data, 1 for transfer control)
  - OCP transfer

$$T_{16bits} = \underbrace{5 \times \left(\frac{13}{12}\right)^{-1}}_{\text{TPU}} + \underbrace{2 \times (52)^{-1}}_{\text{OCP}} + \underbrace{5 \times (52)^{-1}}_{\text{Latency}} = 4.75\mu s$$

- 5.15 qbits => Minimum time during two consecutive DRP register programming is 5qbits

- OCP registers format

| Setting | Value |
|---|---|
| **Address bus** | **16 bits** |
| **Data Bus** | **16 bits** |
| **Clock** | **DSP_CLK / 2 = 52 MHz** |