Technical Note

Locosto PCB Layout Guideline

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0.2 Document History

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Reference to "4 layer How to do document" added.				
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Add to 32 kHz and TritonLite sections.				
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Approved				

0.3 Abbreviations, Terms

0.4 References:

1. APN206_Locosto_schematic_sanity_check
2. APN220_Locosto_LNA_S-parameters
3. APN221_26MHz_crystal_specification
4. APN222_RF_Band_Arrangement
5. APN227_Locosto_PG20_RMS_PE_ISSUE
6. Locosto_Electrical_Specifications
7. TI I-sample2.x Reference Design Platform (RDP) Schematic and Layout
8. Technical Note 4 layer layout (How to do 4 layer with Locosto-Lite)
9. Locosto_TX_Noise_In_RX_Band_Optimization.

Table of Contents

1 Introduction

Please note that the information contained in this document is subject to change without any further notice.

This document is intended to give guidelines and recommendations of how a PCB layout with the TI Locosto transceiver chip combined with the TI Triton-Lite analog baseband chip can be done. The guidelines are with main focus on RF performance and are given for 8-layer (2-4-2) and 6-layer (1-4-1) PCB stack up. The guidelines are based on the TI reference design I-sample 2.5 and later version of I-sample (8-layer). Also examples for 6 layer PCB build up are discussed.

The document is not intended to give a step by step introduction to best practice for a GSM mobile phone layout. It is expected that the actual project team are familiar with good practice for RF and audio layout in a mobile phone.

To list the order of good practice when working with Locosto

- Secure ground connections for all devices by adding vias in pad and connect to reference ground. Keep the impedance to reference very low also at 1-2 GHz. Top priority.
- Take special care of DRP supplies and decoupling of those when doing the artwork.
- Route the RF and audio traces.
- Take special care of reference signals (reference clock and reference supply).
- Do not route clock or data-bus on top layer outside the shield can.

When doing a design with Locosto it is important to remember that the digital baseband and the RF (DRP2) are designed on the same die and packed in one chip. It means that special care must be taken in the layout to avoid digital noise and unwanted reference clock signals to enter the DRP2. This is optimized by taking care of supply, decoupling and grounding strategy.

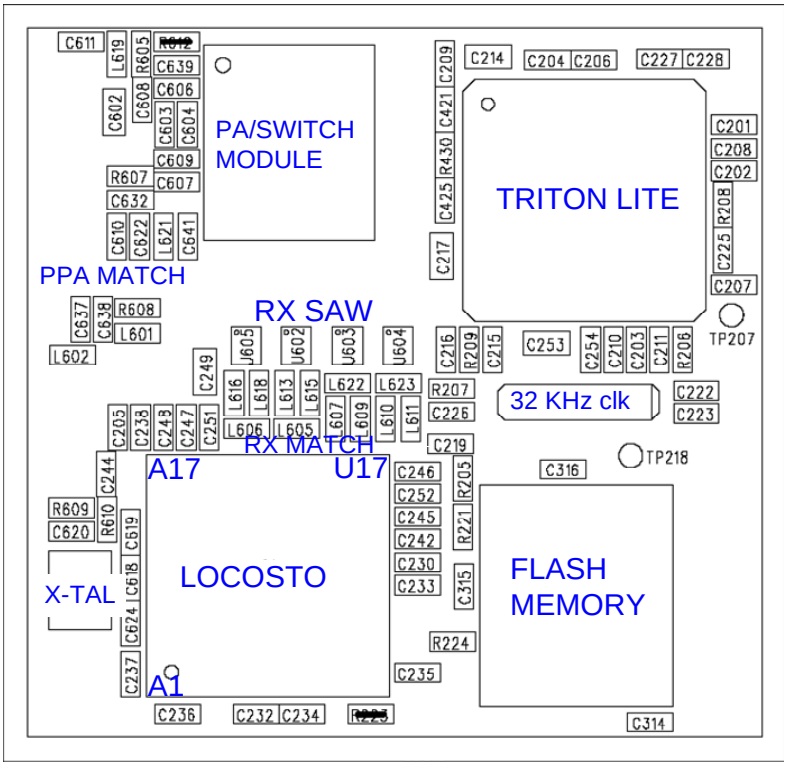
The guidelines and recommendations in this document are based on experience from the PCB build up for the TI I-Sample 2.5 Reference Design Platform.

For a dualband Locosto-Lite in a 4 layer PCB design a supplementary document for “how to do layout with Locosto Lite in a 4 layer design” exists [reference 8].

2 Layout Floor Plan

Placements among major components (i.e. Locosto, PA/switch module, Triton-Lite, Flash Memory, and the crystal) should allow for easy connections of signals between the different blocks (Locosto, PA, Triton and Memory). Figure 1 below outlines the floor plan used on I-sample 2.x.

Figure 1. Example of Floor Plan for a quad band design



Notice: The RX matching is for a quadband design. For a dualband or a triband design the area used for RX matching will be less. The free area is recommended used for improving supply decoupling placement.

Special considerations:

DCXO components including the X-tal and is placed with respect to having distance to TX signals including PPA match.

RX matching components are placed close to LNA input to make the impedance transformation with as low loss as possible.

Decoupling capacitors are places as close to ball on the chip as possible.

Flash Memory is having short distance to Locosto.

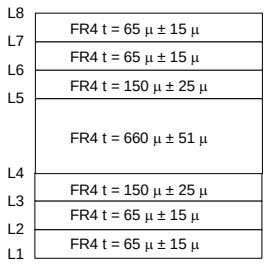
3 PCB Build Up

The guidelines and recommendations are based on the PCB build up for the TI I-Sample Reference Design Platform. It is build by an 8 layer design.

The guidelines are then transferred to a 6 layer build up for the Locosto Lite layout.

3.1 8 Layer PCB (I-sample)

Figure 2. 8 layer PCB build up for I-sample



L8: Main component side, routing RF.

L7: Routing digital, GND under Locosto for VSSA, VSSOSC, VSSRF and VSSRF1.

L6: Routing digital and RF, GND under Locosto for VSSA, VSSOSC, VSSRF and VSSRF1.

L5: Reference GND.

L4: Routing, GND.

L3: Routing, reference GND under reference modem part.

L2: Routing, GND.

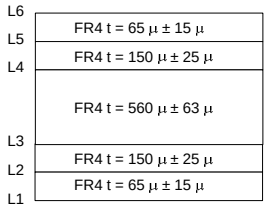
L1: Interface components, GND.

On I-sample routing inside the modem block is done in a manner where it is possible to remove all traces in Layer 4 and Layer 5 in a real form factor design. Traces in Layer 4 and Layer 5 are used to connect external debug signals via the expansion connectors. This means that the main reference GND will be Layer 3 instead of layer 5.

3.2 6 Layer PCB (TI Locosto Lite Demo Layout)

Below an example of how a 6 layer build up (1-4-1) can be planned.

Figure 3. 6 layer PCB build up for Locosto Lite demo layout



L6: Main component side.

L5: Routing, GND under Locosto for VSSA, VSSOSC, VSSRF and VSSRF1.

L4: Routing, GND under Locosto for VSSA, VSSOSC, VSSRF and VSSRF1.

L3: Reference GND

L2: GND and keyboard routing.

L1: Keyboard side

Note: It is important to have low impedance to reference ground. When doing 6 layer and having the reference ground in layer 3 with components on layer 6, the PCB core increases the distance to reference ground. It makes it even more important to add extra ground via's in parallel to reduce the impedance from components to reference ground.

A good approach would be to consider having reference ground in layer 4 if it is possible to route in layer 3 and still have ground in between the traces in layer 3 and the used area on layer 1.

4 Locosto Ground and Supply Strategy

Inside the Locosto chip there is no common ground plane. This means that it is dependent on the PCB layout to connect ground between different circuits inside the chip.

To avoid disturbance and coupling through GND it is important to separate RF GND from Digital GND. The strategy used on I-sample is shown in Table 1. Components are on layer 8 and reference ground in layer 5. Digital GND pins is recommended to have separate connection to reference ground by using vias. Analog and DRP LDO may also be connected on semi ground planes that again must be connected to reference ground.

Examples of how it can be implemented is shown in section 4.1.

Table 1. Locosto GND Strategy (8 Layer PCB build)

Pin name	Pin number	Description	1st. GND layer (Semi GND).	2nd. GND layer (Semi GND).	3rd. GND layer (Reference GND)
VSSPBIAS	U11				L5
VSSPLL	**B14**				L5
VSSA	M13	Analog ground	L7	L6	L5
VSSA	N15	Analog ground	L7	L6	L5
VSSX	E15	DCXO ground			L5
VSS	R1	Digital ground			L5
VSS	H1	Digital ground			L5
VSS	C1	Digital ground			L5
VSS	A7	Digital ground			L5
VSS	**A10**	Digital ground			L5
VSS	**A12**	Digital ground			L5
VSS	**T14**	Digital ground			L5
VSS	**U12**	Digital ground			L5
VSS	U5	Digital ground			L5
VSS	**U8**	Digital ground			L5
VSS	**C17**	Digital ground			L5
VSSRF1	G15	RF_LDO ground	L7	L6	L5
VSSRF1	H14	RF_LDO ground	L7	L6	L5
VSSRF	M15	RF_LDO ground	L7	L6	L5
VSSRF	L15	RF_LDO ground	L7	L6	L5
VSSRF	K15	RF_LDO ground	L7	L6	L5
VSSRF	K14	RF_LDO ground	L7	L6	L5
VSSRF	L13	RF_LDO ground	L7	L6	L5
VSSOSC	J14	DCO ground	L7	L6	L5
VSSOSC	J15	DCO ground	L7	L6	L5
VSSOSC	H15	DCO ground	L7	L6	L5
VSSAPC	N13	APC ground			L5

NOTE: It is recommended to do the connections for the Locosto GND balls by using µvia in pad and add vias further to reference ground on the PCB. Where possible it is recommended to add vias in parallel to decrease the impedance and inductance to reference ground.

VSSA, VSSOSC, VSSRF and VSSRF1 balls are connected to “semi-ground layer” L7 using µvia and then connected to next “semi-ground layer” L6 via µvia and finally connected to reference ground layer.

All other GND connections are only connected to reference ground layer and not connected to “semi-ground”.

Pin numbers written in **red bold** needs special attention to secure shortest possible distance to reference ground.

It is OK to share via for U11 and U12. Also U5 and U8 can share via to reference ground if the vias are closest to U8.

Converted to similar build up for a 6 layer PCB is shown in Table 2. Components on layer 6 and reference ground in layer 3 (if possible reference ground can be layer 4. See comments in section 3.2)

Table 2. Locosto GND Strategy (6 Layer PCB build)

Pin name	Pin number	Description	1st. GND layer (Semi GND).	2nd. GND layer (Semi GND).	3rd. GND layer (Reference GND)
VSSPBIAS	U11				L3
VSSPLL	**B14**				L3
VSSA	M13	Analog ground	L5	L4	L3
VSSA	N15	Analog ground	L5	L4	L3
VSSX	E15	DCXO ground			L3
VSS	R1	Digital ground			L3
VSS	H1	Digital ground			L3
VSS	C1	Digital ground			L3
VSS	A7	Digital ground			L3
VSS	**A10**	Digital ground			L3
VSS	**A12**	Digital ground			L3
VSS	**T14**	Digital ground			L3
VSS	**U12**	Digital ground			L3
VSS	U5	Digital ground			L3
VSS	**U8**	Digital ground			L3
VSS	**C17**	Digital ground			L3
VSSRF1	G15	RF_LDO ground	L5	L4	L3
VSSRF1	H14	RF_LDO ground	L5	L4	L3
VSSRF	M15	RF_LDO ground	L5	L4	L3
VSSRF	L15	RF_LDO ground	L5	L4	L3
VSSRF	K15	RF_LDO ground	L5	L4	L3
VSSRF	K14	RF_LDO ground	L5	L4	L3
VSSRF	L13	RF_LDO ground	L5	L4	L3
VSSOSC	J14	DCO ground	L5	L4	L3
VSSOSC	J15	DCO ground	L5	L4	L3
VSSOSC	H15	DCO ground	L5	L4	L3
VSSAPC	N13	APC ground			L3

NOTE: Same restrictions as for the 8 layer build up. Pins numbers written in **red bold** needs special attention to secure shortest possible distance to reference ground.

4.1 Examples of GND and Vias

Figure 4 and Figure 5 shows how the DRP ground strategy from Table 1 and Table 2 can be implemented on a layout.

Figure 4 combine related circuits on top layer and add a µvia in each ball to the layer below. In the second layer all DRP ground is connected in a plane. From 2nd layer a lot of vias connect to reference ground to secure low impedance to reference GND at GHz frequency. It is important to have as low impedance as possible for each analog GND ball on Locosto.

VSSX is supposed to have a separate connection to reference ground and not to be connected to other ground before reference ground. The same goes for all digital ground pins.

Figure 5 is the I-sample RDP. Here it is implemented a bit different but it still obtains the same strategy. Here each ball has a via to semi ground layer where all DRP ground is connected in a plane that again is well connected to reference ground. Again VSSX is separated.

Figure 4. Example of DRP GND strategy on I-sample

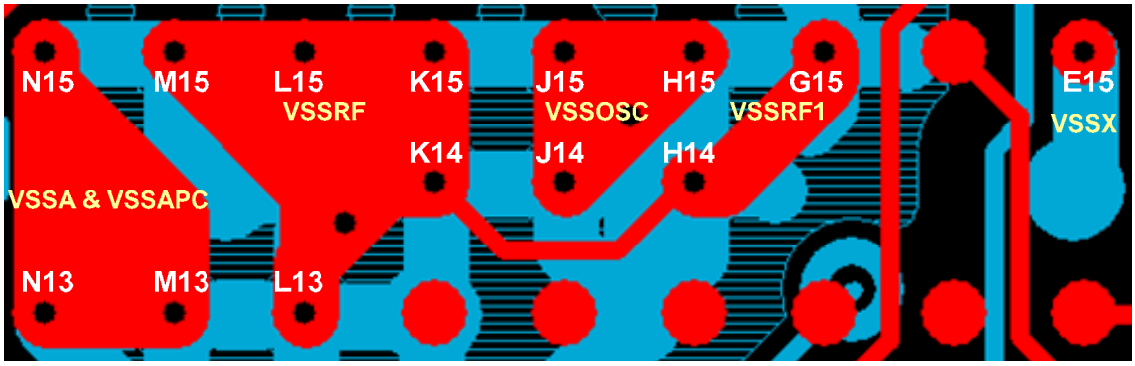
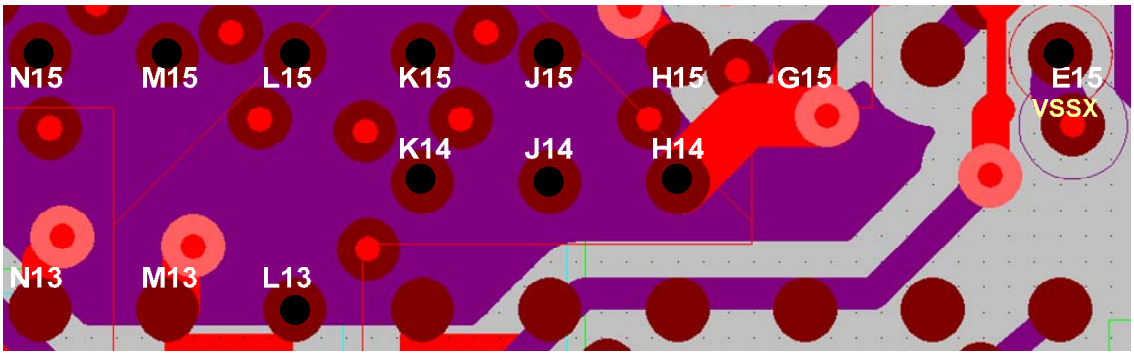
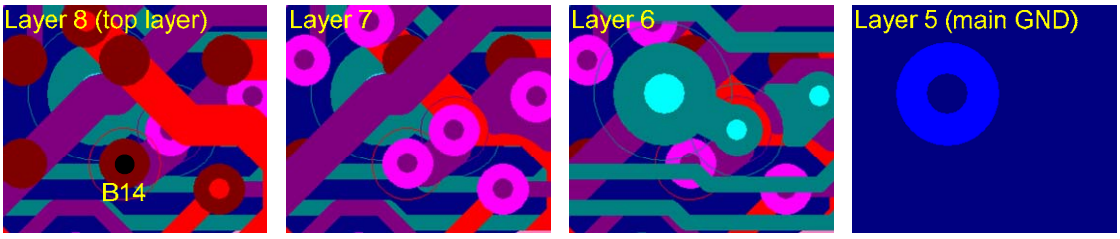


Figure 5. Example of DRP GND strategy on Reference Design Platform (I-sample 2.x)



Digital ground is recommended to be connected to reference ground only. An example is shown in Figure 6. Here ball B14 is connected from top layer to layer 7 with a µvia in the ball. From layer 7 to layer 6 there is also a µvia. From layer 6 to reference ground in layer 5 a normal via (3-6) makes the connection. Notice that ground is also separated from other ground connections on layer 7 and layer 6.

Figure 6. Example of via for Locosto digital ground VSSPLL ball B14



4.2 Important Supply Connections

The Locosto RF (DRP2) needs 3 external power supplies.

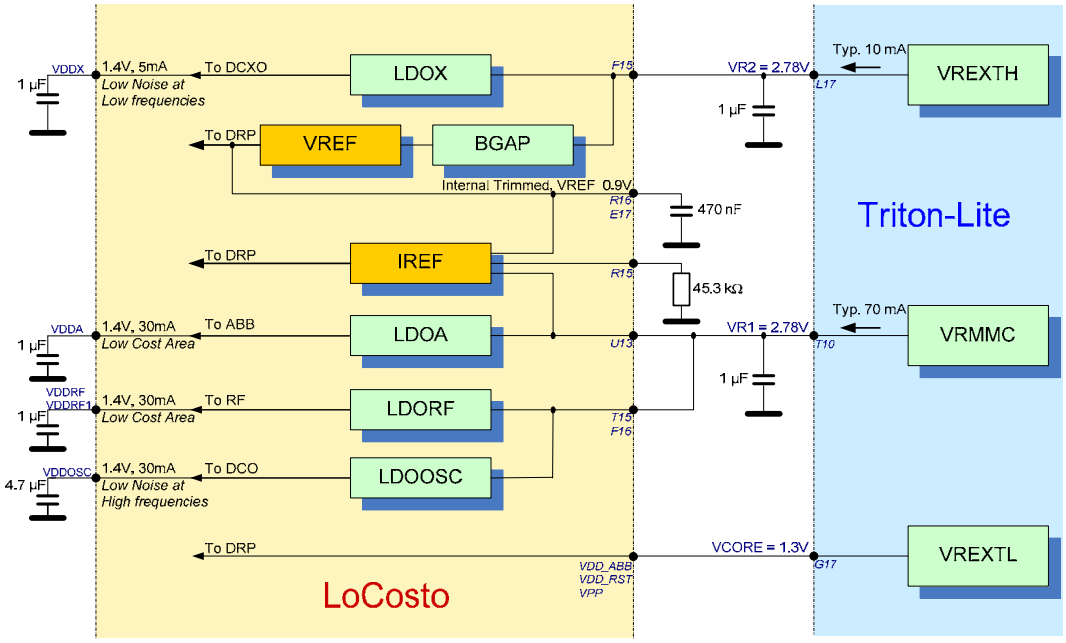
VCORE: 1.3 V DRP2 core digital supply

VR1: Pre regulated input to the DRP embedded LDO's (LDO_OSC, LDO_A and LDO_RF).

VR2: Pre regulated input to the DRP embedded LDO_X.

It is strongly recommended that those DRP2 supplies are routed so that strong coupling to any digital supplies is avoided (do not route in parallel with other supplies where this can be avoided).

Figure 7. Locosto DRP2 - TritonLite Interface



VDDRF1 (source) is shorted to VDDRF on the PCB (Locosto pin G16-H17). Place the decoupling capacitor (1 µF) as close as possible to the Locosto H17.

VREF (Source) is shorted to VREF1 on the PCB (Locosto pin E17 – R16). Place the decoupling capacitor (470 nF) as close as possible to the Locosto pin E17.

VDDOSC (Locosto pin H16) is connected to a decoupling capacitor (4.7 µF). Keep the capacitor close to Locosto pin H16 and be careful not to do routing with this supply directly under the TX output signals (Locosto pin F17 and G17).

VREF should have high priority on the PCB routing. Do not route in parallel with noisy digital signals or signals containing RF. The reason is that VREF is a high impedance signal, and by that sensitive to noise.

IREF is high impedance and must also be protected from very noisy signals. It is recommended to separate ground on the IREF resistor to reference ground from other ground signals in the IREF area.

NOTE: Pay extra attention to the grounding of all decoupling capacitors. Special high attention must be given to ground on LDO decoupling for the DRP2 supplies. It is highly recommended to secure short and solid connection to reference GND by multiple ground vias close to each decoupling capacitor.

As a reference for schematic and routing, the TI I-sample can be used as reference.

5 RX Requirements

5.1 Receiver Trace Pairs

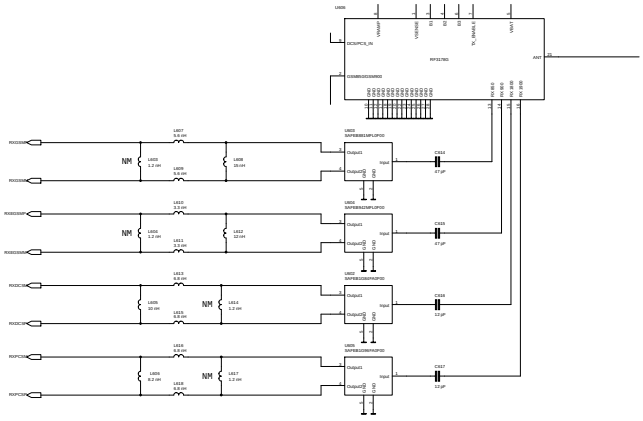
Try to keep the length of the balanced receive trace pairs close equal to avoid phase imbalance.

The traces are:

- Length of RXGSMM ≈ length of RXGSMP
- Length of RXEGSMM ≈ length of RXEGSMP
- Length of RXDCSM ≈ length of RXDCSP
- Length of RXDCSM ≈ length of RXDCSP

Where RXGSMM etc. are the net names in the I-sample schematic.

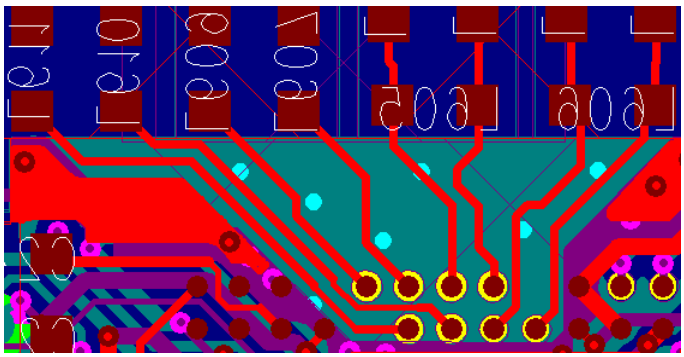
Figure 8. I-sample RX schematic



To minimize the loss it is important to keep the RX traces in the high impedance area (LNA input to RX matching and RX SAW filter) as short as possible.

On I-sample the traces are routed in layer 8 with GND reference in layer 6. This require GND cutout in layer 7 below the traces. The LNA input is high impedance (see APN220 for further information). It is beneficial to have the trace impedance high also between LNA input and matching component. The trace width used on I-sample is 100 µm. This gives a trace impedance of approximately 78 ohm. It is also fine to achieve even higher line impedance.

Figure 9. I-sample RX trace layout at Locosto input.



Note: For dual- and triband configurations some of the LNA inputs are swapped. For further information see instructions in APN222.

It is recommended on tri- and dualband designs to connect unused LNA inputs to GND.

5.2 RX SAW

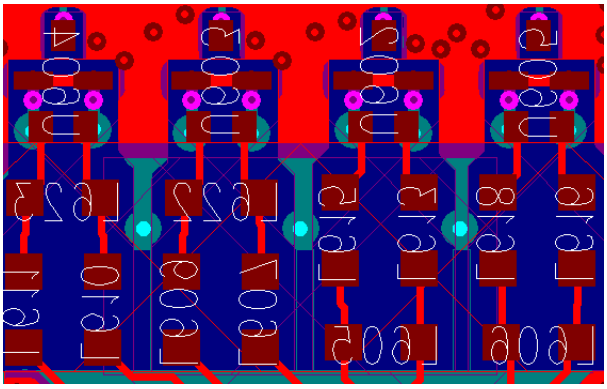
To minimize stray capacitance coupling to GND from the SAW filter pads, there must be a cutout in GND layers below the SAW filter RF pads and all the RX matching components.

For an 8 layer PCB it is recommended to have cutout in the layers 7 and 6. Ref. GND is in Layer 5.

For a 6 layer PCB it is recommended to have cutout in the layer 5 and 4. Ref. GND is in Layer 3.

Please notice that each SAW filter needs good connections to GND to secure the expected filter performance. This must be accomplished by several vias close the the GND pins, preferable in the pads if possible.

Figure 10. Cut-out in GND in layers below RX SAW and RX match



5.3 Locosto RX Input

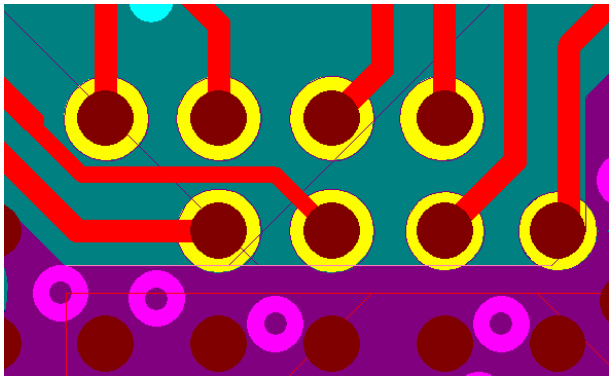
All the RX balls on Locosto are recommended to have cutout in GND layers below to minimize stray capacitance.

For an 8 layer PCB it is recommended to have cutout in the layers 7 and 6. Ref. GND is in Layer 5.

For a 6 layer PCB it is recommended to have cutout in the layer 5 and 4. Ref. GND is in Layer 3.

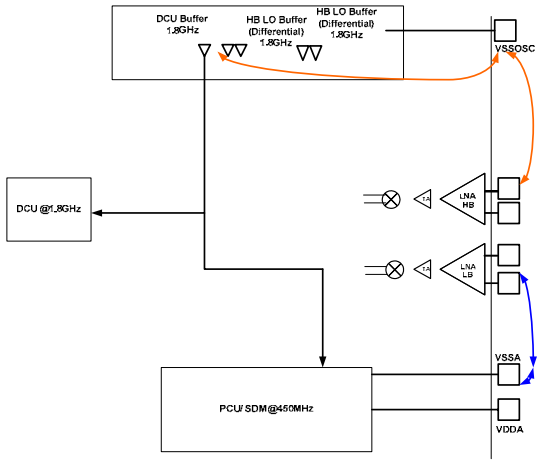
The RX balls are:

RXDCSM (U202.K17)
RXDCSP (U202.L17)
RXPCSM (U202.J16)
RXPCSP (U202.K16)
RXGSMM (U202.N17)
RXGSMP (U202.M17)
RXEGSMM (U202.M16)
RXEGSMP (U202.L16)



5.4 Coupling

When doing the layout it is important to think about unintended coupling that can cause reduction in performance.



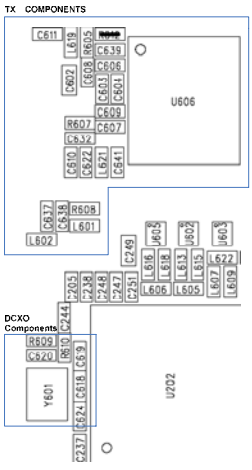
At LNA input:

- Peripherals on the board may couple to LNA input and result in degradation of sensitivity on specific RX channels.
- TX power can couple to LNA input and disturb the DCO and RF Oscillator degrading phase error performance in TX burst.
- IIP2 can be degraded by coupling of LO frequency clocks on VDDOSC domain and VDDA domain into LNA input.

At DCXO:

- PPA output coupling back to XTAL input may cause degradation on phase/frequency
  - Optimize placement of XTAL with respect to TX output path (see Figure 11).
  - Suppress second harmonic of PPA output (may apply appropriate shunt cap).
- Avoid TX output (PPA, PA) disturbing DCO domain (VDDOSC/VSSOSC).

Figure 11. TX and DCXO component placement of I-sample 2.7



6 TX

All the TX balls on Locosto are recommended to have cutout in GND layers below.

For an 8 layer PCB it is recommended to have cutout in the layers 7 and 6.

For a 6 layer PCB it is recommended to have cutout in the layer 5 and 4.

The TX balls are:

TXLB (U202.F17)

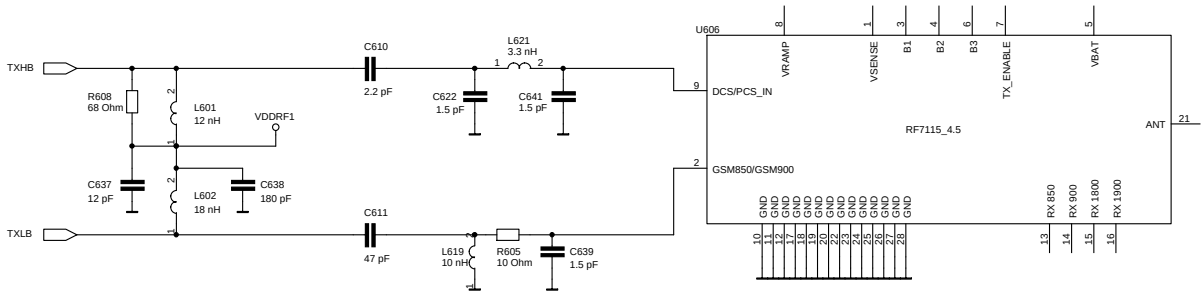
TXHB (U202.G17)

The transmit traces between Locosto and PA is recommended to be routed in inner layer. They are routed as 50 ohm traces. On I-sample this give a width W=100 µm in layer 6 with GND reference on layer 7 / layer 5.

VDDRF1 going from Locosto to the PPA supply inductors (L601, L602) must be isolated as much as possible from the TXLB and TXHB signals to avoid unwanted RF feedback.

On I-sample the width of this trace is W= 200 µm.

Figure 12. TX matching components, example from I-sample 2.6



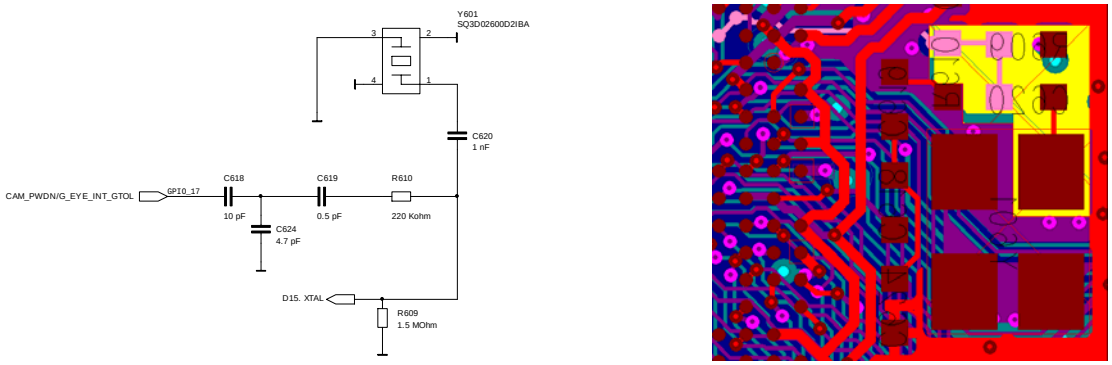
7 26 MHz DCXO

To minimize stray capacitance coupling in the active part of the DCXO it is important to ensure maximum distance to GND for the active pin of the X-tal. On TI I-sample this is obtained with a GND cut out in Layer 7 to Layer 4 below the X-tal pin 1.

Minimize the distance from the 26 MHz X-tal to the Locosto ball D15 and take care of signals crossing the active 26 MHz signal in layer below. To have optimum performance on the DCXO using the X-tal (Cl=12.5 pF) specified in APN221 the parasitic capacitance in the PCB should be kept below 1 pF, see Figure 14.

Also secure cutout below R610 in the dithering circuit to the 26 MHz reference. Example of how it is done on I-sample 2.7 is shown in Figure 13. For further information refer to APN227.

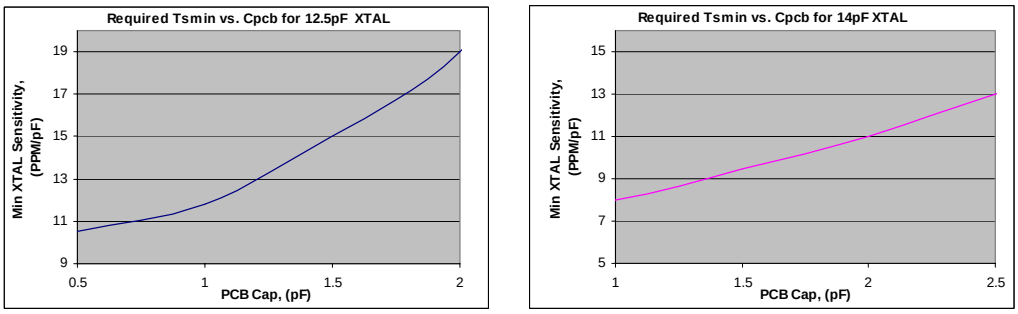
Figure 13. DCXO Schematic I-sample **DCXO layout I-sample**



Below in Figure 14 the importance of minimising stray capacitance is illustrated.

If the stray capacitance in the PCB layout exceed the specified 1 pF the specification for the X-tal tuning sensitivity is not valid any more. This results in yield- and design problems for the DCXO circuit.

Figure 14. Requirement to X-tal tuning sensitivity vs. stray capacitance in PCB



If the physical design prevents the stray capacitance in the PCB to be below 1 pF it is necessary to find an alternative X-tal with higher C_{load} value and an appropriate Tuning Sensitivity (TS).

See APN221 for further information about X-tal specification.

8 Clocks (13 MHz)

To obtain optimum RF performance it is important to take special care of how the 13 MHz clk is routed on the PCB. The 13 MHz clk is often root cause to many clock related spurious problems for RF performance.

To limit the current flow at the buffer output for ckout_13MHz (Locosto N8) TI recommend to add a series resistor between the Locosto and Triton or any other external device connected to this output. The value of the resistor must be adjusted according to the load from external devices. The resistor should be placed as close to ball N8 on Locosto as possible.

Figure 15. 13 MHz clock connection

The resistor may also be replaced by an inductor to RF terminate the 13 MHz buffer. For further information about this issue please refer to reference [9] about TX noise in RX band optimization.

9 32 kHz

The 32 kHz oscillator is placed in the Triton Lite TWL3031. This oscillator is sensitive to digital noise, so it is important to avoid digital noise on the traces to the 32 KHz X-tal. Good GND plane below the X-tal is recommended. It is recommended that the two traces are routed as short as possible, and as of equal length as possible. The capacitors must be placed on the paths of the routed traces, ie not on a separate branch.

Figure 16. 32kHz X-tal connection

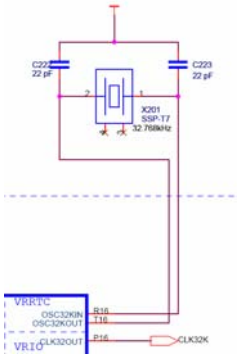
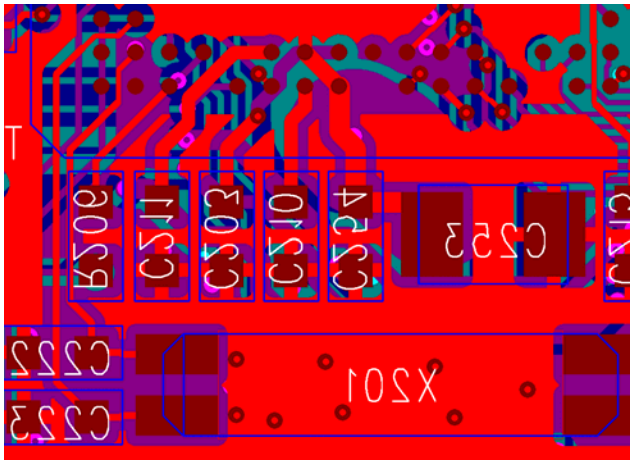


Figure 17. 32 KHz layout I-sample

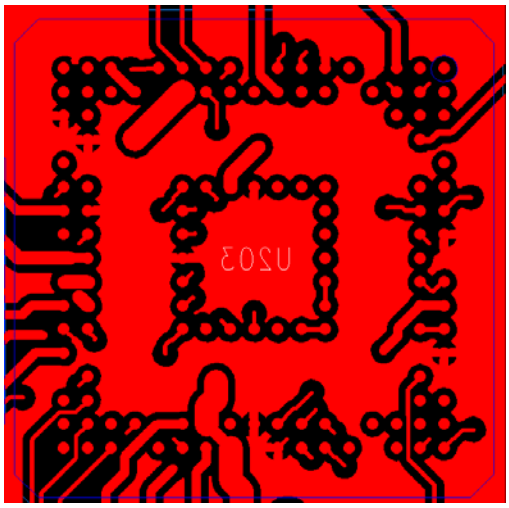


10 TritonLite

Triton-Lite (TWL3031) is the Analog baseband used together with Locosto on the TI I-sample reference design.

TI recommends making a GND plane under Triton-Lite to minimize TDMA noise in audio.

Figure 18. Triton Lite, layout of GND plane



Special attention should be given to the reference pins and components. These are:

- L12: resistor for current reference generator;
- M16: capacitor for bandgap reference input voltage;
- M17: system reference ground.

10.1 Audio Signals

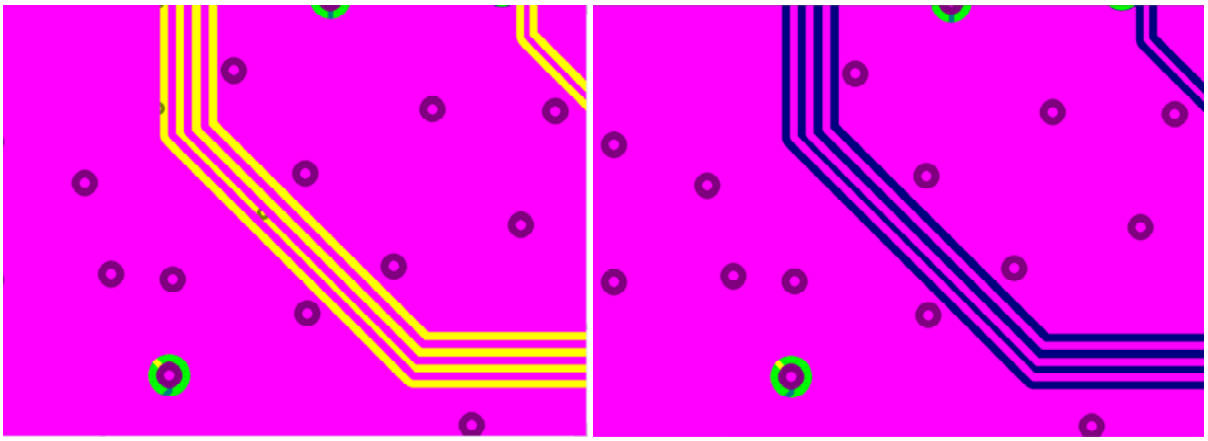
All audio traces should be protected as much as possible, from all sides, by "ground tunelling." This concept means that audio traces should be routed as much as possible in inner layers, and that they should only have ground areas (which are in turn well connected to main reference ground) directly next to them, above and below as well as to either side.

Differential signals (earpiece, speaker, and in some cases differentially-designed microphone signals) should be routed side by side as much as possible the entire routing. They should also be routed as much as possible to the same lengths from start to finish.

Ensuring these implementations will protect the audio signals from noise generated by other parts of the PCB, as well as from radiated TDMA noise from RF traces and the antenna.

An example of optimal routed audio traces is shown with the microphone differential and bias signals on I-sample; notice the uninterrupted ground above, below and to either side of the routing.

Figure 19. Microphone signal traces of I-sample



11 Misc

11.1 Memory

It is highly recommended to secure proper grounding of the memory. Both directly grounding of MEM_VSS and grounding of decoupling capacitors used for VRMEM. It is recommended to have a GND via in each GND ball for the Memory. Make sure each via do have solid connection to reference GND. Please also secure that memory GND is not sharing any GND connections for Locosto and Locosto decoupling before it reaches reference GND. Memory accesses have a tendency to generate noise that degrade RF performance in both RX and TX slots.

11.2 Locosto Ball Arrangement

Figure 20. Locosto ball arrangement overview

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
U	anatst2	xanatst4	xanatst3	NoBall	apc_vdo	vss	vsspbias	vdd_rst	NoBall	vss	vdd_io	vdd_dbb	vss	NoBall	vdd_io	spare_2	spare_3
T	anatst1	xanatst5	vddr1rx1	vss	NoBall	vdd_usim	sim_pbias	usb_boot	cdo	ckin_32khz	ck13mhz_en	vdx	NoBall	usb_rcv	gpio_2	trstn	nbscan
R	xanatst6	vref1	iref	Reserved	apcvref	apcldofilter	sim_io	vdd_dbb	gpio_4	wakeup_req	vclkrx	sda_trit	usb_dat	i2c_scl	rts_sdirda	uart_cts	vss
P	NoBall	vdda	vdda	NoBall	NoBall	NoBall	NoBall	sim_clk	csclk	abb_irq	NoBall	NoBall	NoBall	NoBall	uart_tx	gpio_46	NoBall
N	rxgsmm	NoBall	vssa	NoBall	apc_vss	NC	sim_rst	on_noff	gpio_5	ckout_13mhz	scl_trit	i2c_sda	gpio_47	NoBall	gpio_43	NoBall	vdd_dbb
M	rxgsmp	rxegsmm	vssrf	NoBall	vssa	NC	apcout	sim_pwrctrl	csync	vdr	usb_txen	gpio_0	gpio_44	NoBall	nrdy	nble	nmoe
L	rxdcsp	rxegsmp	vssrf	NoBall	vssrf	NC	NC	NC	apcspare1	usb_se0	uart_rx	gpio_42	ncs3	NoBall	nbhe	add_data_1	rnw
K	rxdcsm	rxpcsp	vssrf	rssrf	NC	NC	NC	NC	vfsrx	gpio_1	gpio_45	tdp	add_data_2	add_data_0	add_data_3	add_data_4	vdd_mif
J	NoBall	rxpcsm	vssosc	rssosc	NC	NC	NC	NC	NoBall	add_20	adv	add_data_9	add_data_5	add_data_8	add_data_6	add_data_7	NoBall
H	vddrf	vddosc	vssosc	vssrf1	NC	NC	NC	tspact_12	kbr_3	gpio_33	gpio_37	add_19	add_data_12	add_data_15	add_data_11	add_data_10	vss
G	txhb	vddrf1	vssrf1	NoBall	NC	NC	kbc_0	tspact_15	gpio_23	gpio_27	gpio_29	gpio_7	gpio_39	NoBall	add_16	add_data_13	add_data_14
F	txlb	vddr1tx1	vddr2	NoBall	NC	tspact_11	kbr_0	kbr_4	lcd_rnw	gpio_19	gpio_24	gpio_32	gpio_35	NoBall	add_21	add_18	add_17
E	vref	NoBall	vssx	NoBall	kbc_2	tspact_14	kbr_1	gpio_13	lcd_data_0	lcd_data_3	gpio_20	gpio_26	nd_nwp	NoBall	ncs0	NoBall	vdd_mif
D	NoBall	vddx	xtal	NoBall	NoBall	NoBall	NoBall	nemu1	lcd_rs	lcd_data_5	NoBall	NoBall	NoBall	Reserved	nd_ce1	gpio_36	NoBall
C	vss	kbc_1	kbc_3	tspact_13	vdd_pll	kbr_2	nemu0	lcd_nrst	vdd_io	lcd_data_2	lcd_data_6	gpio_22	gpio_25	gpio_28	gpio_31	gpio_34	vss
B	vpp	f_force	vdd_dbb	vss_pll	NoBall	kbc_4	gpio_12	lcd_stb	gpio_17	lcd_data_1	lcd_data_4	lcd_data_7	NoBall	vdd_dbb	gpio_30	tdo	tdi
A	vpp	sense	vdd_io	NoBall	vdd_dbb	vss	vdd_dbb	vss	NoBall	vdd_dbb	vss	gpio_18	gpio_21	NoBall	vdd_io	tms	tck

11.3 General Recommendations

Normal good PCB design practice should be observed for the layout with Locosto and TritonLite. Secure that GND planes in different layers are properly connected with vias as described in section 4.

Secure that all GND planes on the PCB are well connected to reference ground.

Protect analog audio lines from digital and RF signals.

Make sure that RF traces are 50 ohm except for RX input. Keep RX input signals traces with a high impedance to minimize loss.

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