Application note

APN221_26_MHz_Crystal_specification

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0.2 Document History

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2006-09-04	1.2		F.C	
Added section 4 and 5. Tuning sensitivity updated according to H.G.J. [6]				
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2007-04-11	002	Submitted	a0389010	
Updated content with info about stray capacitance. X-tal specification for Cl=14 pF added				
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Important Notice added				
2007-07-30	007	Approved	a0389010	a0794494
X-tal mouting figure added				

0.3 References, Abbreviations, Terms

[1] 3GPP TS 45.005 version 5.9.0 (Release 5)

"Digital cellular telecommunications system (phase 2+); Radio transmission and reception "

[2] 3GPP TS 51.010-1 version 5.5.0 (Release 5)

"Digital cellular telecommunications system (phase 2+); MS conformance specification "

[3] Locosto Radio Interface (lcost_radio_interface, Rev 1.0)

[4] System hardware implementation LOCOSTO and LOCOSTO-LITE (locosto_shi_13_01_00_01796.doc Rev 1.4)

[5] RD329: Leonardo VCXO specification. (RD329.DOC)

[6] H. G. J..: "Locosto_26MHz_Crystal_Specification"

[7] Locosto Electrical Specification v1.8

[8] Locosto Layout Guidelines.

Table of Contents

1 Introduction

Purpose of this document is to provide to the Locosto user the 26 MHz requirements for the reference quartz crystal oscillator (XTAL).

This document describes the Locosto 26 MHz crystal specification [3] with following modifications coming from TIDK [6]

- Tuning sensitivity requirement replaces C0 and C1 requirements. This change is intended to make it easier to widen selection of acceptable crystals from different suppliers
- It must be possible to approve the crystals according to the IEC 60444 specification. This is not a requirement but is specified to ensure that the crystal manufactures deliver what is specified.
- Better description of frequency dip, since the original description has been misunderstood several times.
- Requirements for spurious response, shock and vibration tolerance, leak and solderability are added. The requirements come from RD329 [5].
- Requirements for storage temperature and humidity added.

The Locosto DCXO consists of 3 basic blocks. 2 active blocks (Locosto and crystal) and one passive (the PCB).

To achieve desired DCXO performance, it is important to optimize the PCB layout and to select a crystal that matches the requirements. To assist customers, crystal specifications for two different load capacitances are listed in this document, one corresponding to a PCB layout with low capacitance and one with high capacitance.

The Document also gives a DCXO architecture overview and main parameters which may help in the crystal selection and verification.

2 26 MHz crystal specification:

2.1 Specification for C_{load} = 12.5 pF

Table 1. Specification for crystal with Cl = 12.5 pF

Parameters	Test conditions	Min.	Typ.	Max.	Unit
Nominal Frequency			26		MHz
Frequency tolerance @ CL	at 25ºC ±3ºC			±10.0	ppm
Temperature Characteristics	in reference to +25ºC over –20ºC ~+75ºC			±10.0	ppm
Aging 1st year after 5 years				 ±1.0 ±2.5	 ppm ppm
Dips vs. temperature (Slope)	–20ºC ~ +75ºC			0.3	ppm/°C
Frequency versus temperature slope at 25°C	at 25° C ± 7°C	-0.5		0	ppm/°C
Equivalent Series Resistance				50	Ω
Standard load capacitance (CL)			**12.5**		**pF**
Tuning sensitivity @ CL = 12.5 pF	Tuning sensitivity specification is only valid for a PCB layout where the parasitic stray capacitance is **below 1.0 pF.**	11.1		18	ppm/pF
Shunt capacitance (C0)	Tuning sensitivity is primary requirement but Min., Typ. and Max. C0 must be specified to TI.				pF
Series capacitance (C1)	Tuning sensitivity is primary requirement but Min., Typ. and Max. C1 must be specified to TI.				fF
Drive level			50	100	µW
Spurious Ratio (20log(R_{sp}/R_1))		10			dB
Humidity		20		75	%
Storage temperature		-40		+90	°C
Shock test	Test Ea according to IEC 60068-2-27 or similar Test Eb according to IEC 60068-2-29 or similar				
Vibration test	Test Fc according to IEC 60068-2-6 or similar				
Leak test	Test according to IEC 60068-2-17, method 1 and 2 or similar				
Solderability	Test according to IEC 60068-2-54 and IEC 60068-2-69 or similar				

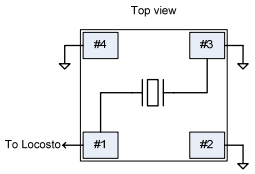


Figure 1. Crystal mounting for specification validation

Crystal testing procedure is left to the discretion of the suppliers, however, it must meet the requirements in Table 1 or Table 2 when tested according to the IEC 60444 test specifications and mounted as shown in Figure 1.

2.2 Specification for C_{load} = 14 pF

Table 2. Specification for crystal with Cl = 14.0 pF.

Parameters	Test conditions	Min.	Typ.	Max.	Unit
Nominal Frequency			26		MHz
Frequency tolerance @ CL	at 25ºC ±3ºC			±10.0	ppm
Temperature Characteristics	in reference to +25ºC over –20ºC ~+75ºC			±10.0	ppm
Aging 1st year after 5 years				 ±1.0 ±2.5	 ppm ppm
Dips vs. temperature (Slope)	–20ºC ~ +75ºC			0.3	ppm/°C
Frequency versus temperature slope at 25°C	at 25° C ± 7°C	-0.5		0	ppm/°C
Equivalent Series Resistance				50	Ω
Standard load capacitance (CL)			**14**		**pF**
Tuning sensitivity @ CL = 14 pF	Tuning sensitivity specification is only valid for a PCB layout where the parasitic stray capacitance is **between 1.0 pF and 2.0 pF.**	10.8		15	ppm/pF
Shunt capacitance (C0)	Tuning sensitivity is primary requirement but Min., Typ. and Max. C0 must be specified to TI.				pF
Series capacitance (C1)	Tuning sensitivity is primary requirement but Min., Typ. and Max. C1 must be specified to TI.				fF
Drive level			50	100	µW
Spurious Ratio ($20\log(R_{sp}/R_1)$)		10			dB
Humidity		20		75	%
Storage temperature		-40		+90	°C
Shock test	Test Ea according to IEC 60068-2-27 or similar Test Eb according to IEC 60068-2-29 or similar				
Vibration test	Test Fc according to IEC 60068-2-6 or similar				
Leak test	Test according to IEC 60068-2-17, method 1 and 2 or similar				
Solderability	Test according to IEC 60068-2-54 and IEC 60068-2-69 or similar				

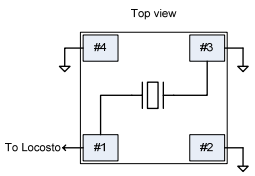


Figure 2. Crystal mounting for specification validation

Crystal testing procedure is left to the discretion of the suppliers, however, it must meet the requirements in Table 1 or Table 2 when tested according to the IEC 60444 test specifications and mounted as shown in Figure 2

2.3 Tuning sensitivity vs. stray capacitance in PCB.

The curves in Figure 3 and Figure 4 below show the dependence of the crystal tuning sensitivity on the stray capacitance of the PCB. If the stray capacitance is above 1 pF the crystal specification for the tuning sensitivity has to be modified to fulfil the tuning requirements. Also change of both C_{load} and the tuning sensitivity is a possibility.

Figure 3. Tuning sensitivity requirements vs. stray capacitance. Cl = 12.5 pF

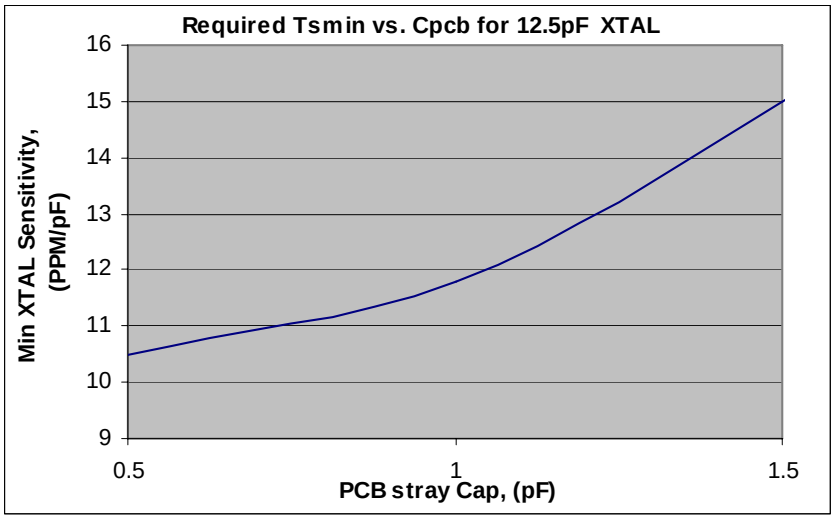
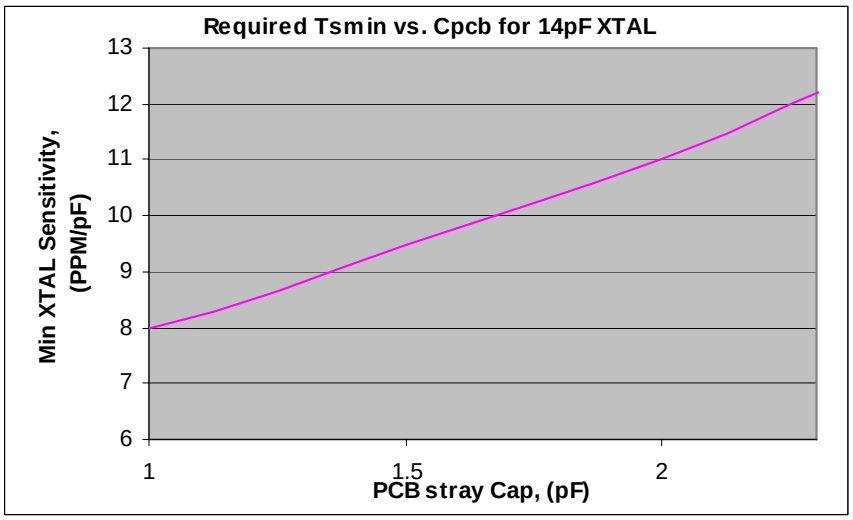


Figure 4.Tuning sensitivity requirements vs. stray capacitance. Cl = 14.0 pF



From Figure 3 it can be seen, that the stray capacitance in the actual used PCB must be below 1 pF to be able to use the crystal specification from section 2.1 regarding tuning sensitivity.

If it is not possible to keep the stray capacitance in the layout below 1 pF the alternative specification from section 2.2 is to be used to secure the expected performance and secure CFA calibration.

3 Is the crystal “centred” versus DCXO coarse tuning (CFA)?

In order to evaluate if the crystal is centred versus DCXO coarse tuning (CFA word), the frequency deviation versus CFA code (coarse tuning) has to be characterized. This can be done using ETM commands.

The following test equipment is needed for performing this characterization:

• A laptop or stationary PC with a RS-232 or USB interface for running the ETM SW on target.

• A Base Station Simulator (BSS), (e.g. R&S CMU200).

• A calibrated power supply.

• Misc. cables and level converters for interfacing to Mobile Station (MS).

The characterization includes the following steps

1. The MS is set up to transmit at channel 40 at power level 15

2. The frequency error of the carrier is measured with a BSS

3. The needed parameters are calculated and changed

ETM Procedure:

tms 1 (enter in test mode)

rfpw 7 6 0 (select GSM-900 band)

rfpw 2 40 (select TCH 40)

rfpw 8 0 (disable AFC)

rfpw 9 0 (set AFC at middle range)

txpw 1 15 (select TX power to power level 15)

rfe 3 (do both RX and TX on TCH without network sync)

mw -2 0xFFFF1E4C 0x0001 (write the CFA value into the target)

<measure the frequency deviation on the BSS

mw -2 0xFFFF1E4C 0x0081 (add 0x80 to CFA value, see section 5.3)

<measure the frequency deviation on the BSS

mw -2 0xFFFF1E4C 0x0101 (add 0x80 to CFA value)

<measure the frequency deviation on the BSS

…

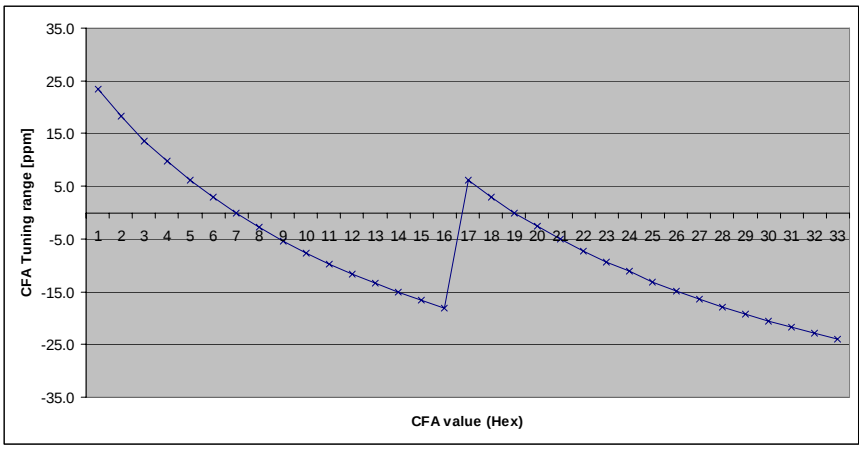
<measure the frequency deviation on the BSS

mw -2 0xFFFF1E4C 0x0FFD (add 0x80 to CFA value)

<measure the frequency deviation on the BSS

The typical result should be similar to the one illustrated in Figure 5.

Figure 5. CFA tuning range validation



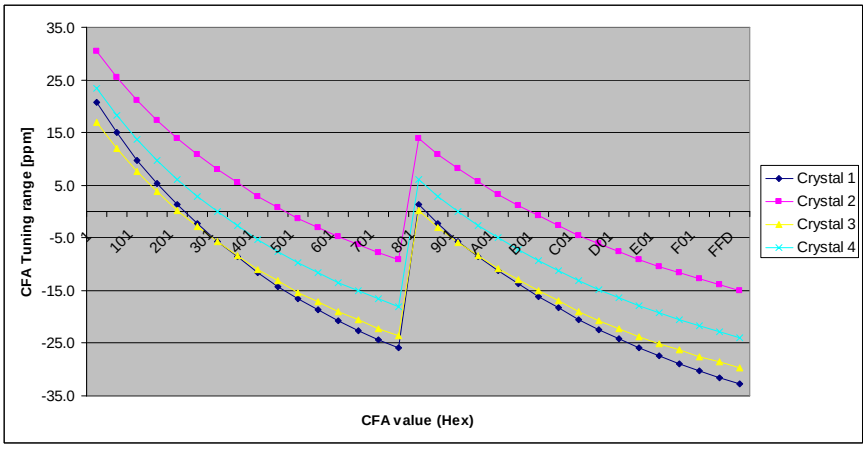
The discontinuity in the middle of the graph occurs because of CFA tuning range extension capacitor. The two subranges, on the left and on the right side of Figure 5 show partial overlap, and for some values of coarse frequency adjustment CFA values from either left sub-range or from the right sub-range may be chosen.

In order to see if the selected crystal is centred over the CFA range, max and min deviation have to be similar. Of course it is expected that in production crystals will exhibit some deviation from being perfectly centred. This is perfectly normal, providing crystal frequency tolerance specified in Table 1 or Table 2 is met. CFA calibration will be used to compensate this frequency tolerance during in-phone calibration.

When CFA tuning range is measured with a perfectly centred (0 ppm tolerance) crystal, at least +/-20 ppm of CFA tuning range is required, in order to compensate for the allowed frequency tolerance of the crystal plus DCXO tolerances in Locosto as well as variations of the stray capacitance tolerances in the PCB.

Nevertheless the range has to be limited from 0x0001 to 0x0F80 for in-phone production calibration. When the DCXO coarse tuning calibration is not working properly (example is no signal provide at Locosto input during CFA calibration) then 0x0F81 CFA code is reported which is a potential code that could also be valid after a correct calibration. Failing calibration codes greater than 0x0F80 removes this potential issue.

Figure 6. Example of crystal selection:



In this example, crystal 4 would give the best fit, with symmetrical CFA tuning range of +/-22ppm and it could be selected as a reference example against which all other crystals should be compared.

4 Is the crystal having enough AFC tuning range (FFA)?

In order to evaluate if the selected crystal is having enough AFC tuning range after CFA calibration, the frequency deviation versus FFA code (Fine Frequency Adjustment) has to be characterized. This can be done using ETM commands.

The following test equipment is needed for performing this characterization:

• A laptop or stationary PC with a RS-232 or USB interface for running the ETM SW on target.

• A Base Station Simulator (BSS),(e.g. R&S CMU200).

• A calibrated power supply.

• Misc. cables and level converters for interfacing to Mobile Station (MS).

The characterization includes the following steps

1. The MS is set up to transmit at channel 40 at power level 15

2. The frequency error of the carrier is measured with a BSS

3. The needed parameters are calculated and changed

ETM Procedure:

tms 1 (enter in test mode)

rfpw 7 6 0 (select gsm900 band)

rfpw 2 40 (select TCH 40)

rfpw 8 0 (disable AFC)

rfpw 9 -8000 (set AFC at lower range value)

txpw 1 15 (select TX power to power level 15)

rfe 3 (do both RX and TX on TCH without network sync)

<measure the frequency deviation on the BSS

rfpw 9 -7500 (AFC value is increased in step of 500)

<measure the frequency deviation on the BSS

rfpw 9 -7000 (AFC value is increased in step of 500)

<measure the frequency deviation on the BSS

…

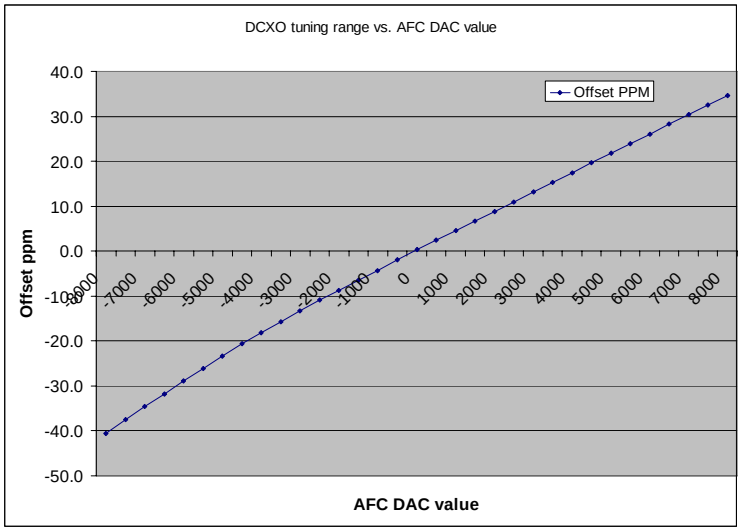
<measure the frequency deviation on the BSS

rfpw 9 8000 (AFC value is set to higher range value)

<measure the frequency deviation on the BSS

Calculate the measured values into ppm deviation.

Figure 7. AFC tuning range vs. AFC DAC value



The requirement for any design will be to have an AFC tuning range > ±21 ppm to secure proper tuning range for temperature, aging ….

The selected crystal in Figure 7 does full fill this requirement with a tuning range of more than ± 35 ppm.

5 DCXO details

5.1 DCXO system description

The DCXO system consists of an external crystal, DCXO core based on Colpitts oscillator, a switchable capacitor array, amplitude control loop and a current DAC. It also includes an autonomous digital startup system to control the startup sequence of the band-gap reference and the LDO voltage regulator for the DCXO that is based on a 32 KHz clock. It is also used to ensure reliable start-up of the DCXO itself. An ADC inside the block is used as part of the amplitude control loop.

5.2 DCXO core description

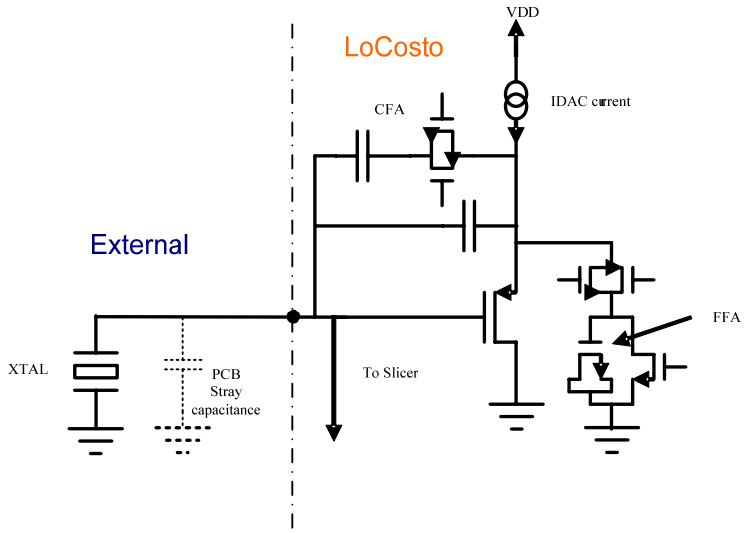
DCXO (Digitally Controlled Crystal Oscillator) is a digitally tuneable crystal oscillator centred at 26MHz for GSM applications. Both the amplitude and the frequency of oscillation are digitally controllable. Figure 8 here below shows a simplified top level schematic of DCXO core schematic.

Colpitts style oscillator is chosen for pin savings, with only one crystal connection pin required besides VDDX and VSSX.

Coarse frequency adjustment (CFA) is controlled through 10 bit digital control word. Frequency change is accomplished by altering the feedback capacitor.

AFC fine frequency control (also called FFA “Fine Frequency adjustment”) is controlled through a 14-bit capacitor array. Frequency change is accomplished by altering the source-to-ground capacitance.

Figure 8. DCXO equivalent diagram



5.3 CFA

Coarse Frequency Adjustment (CFA) capacitor consists of modified-binary array with 10-bit control, with individual weights of 1, 2, 3, 6, 12, 24, 48, 96, 192 corresponding to bits 0 through 8 respectively and a special sub-ranging capacitor of ~144 units controlled by the MSB bit (bit 9) of the CFA word.

CFA word can be read at register CTL_LDO_DCXO at address: 0xFFFF1E4C.

Bits <15:12> => not used

Bits <11:2> => Capacitor non-binary weighted: 144,192,96,48,24,12,6,3,2,1

Bit <1:0> => reserved (internal use)

Example: 0FD1=[~~0000~~ 1111 1101 00~~01~~] = 144+192+96+48+24+12+0+3+0+0 = 519 unit caps

The range of CFA capacitor array is the following:

CFA = CFAmin + CFAstep * CFAcode

Where: CFAmin=7pF, CFAstep=31fF and 0<=CFAcode<=583

Note: These numbers are simulated values given by design team.

5.4 FFA

The Fine Frequency Adjustment is controlled through a 14-bit capacitor array with a segmented tapered capacitor array which effectively linearize the transfer function. The top 10bits are thermometer coded and the lower 4 LSBs are Sigma Delta (1st order) modulated. A memory array like architecture is used to facilitate the layout.

The range of FFA capacitor array is the following:

FFA = FFAmin + FFAstep * FFAcode

Where: FFAmin=10pF, FFAstep=3.7fF and 0<=FFA code<=2^14-1

Note: These numbers are simulated values given by design team

As FFA is typical covering +/-25ppm, the average slope is typically 0.003ppm/LSB

(Tuning range/ number of bits=50ppm/2^14~0.003ppm/LSB)

This is not aligned with frequency resolution as extracted from “Locosto Electrical specification” v1p6

Parameters	Test conditions	Symbol	Min. 2	Min. 1	Typ.	Max. 1	Max. 2	Unit
Center Frequency			-	-	26	-	-	MHz
Frequency error before calibration			-50	-	-	-	+50	ppm
Dynamic range	After calibration		-20/+20					ppm
Frequency resolution	Step to step		0	-	0.03	-	+0.05	ppm/LSB
Number of control bits					14			bits

As mentioned in test condition column, this item is not related to the average slope of the FFA but to the maximum FFA step to step frequency deviation.

(Step to step resolution = Delta F / 1 LSB [ppm/LSB] where Delta F is frequency deviation in ppm between FFA value and FFA value + 1 LSB)

The FFA has a monotonic response but all steps do not provide equivalent frequency deviation. Several steps will have minor frequency deviation and then next step will have like 0.03ppm frequency deviation. Average

slope will still show 0.003ppm/LSB slope and overall system frequency accuracy does not suffer from this FFA response.

5.5 Locosto input capacitance

Locosto input capacitance can be estimated as follow:

C_input = 1 / (1/CFA + 1/FFA) + Cpara

Where: Cpara is the Locosto internal parasitic capacitor to ground and can be estimated as 2pF (It does not include any PCB parasitic capacitor)

5.6 Typical voltage swing at crystal

Locosto typical voltage swing at crystal is 0.45 Volt peak.

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