**PROGRAM**

**Technical Note**

# APC application note

| | | | |
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## 0.2 Document History

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## 0.3 References, Abbreviations, Terms

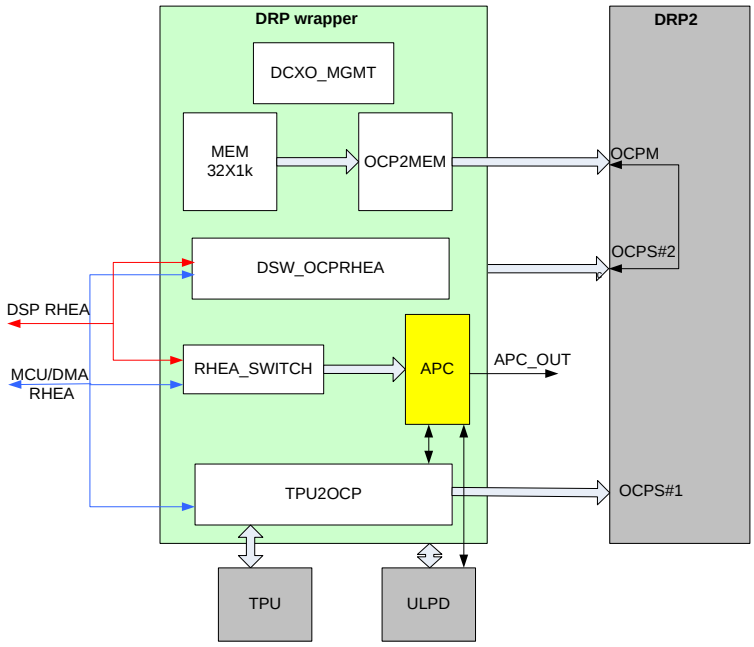
## Table of Contents

# 1 APC module overview

The Automatic Power Control (APC) module is included in the DRP wrapper. The module is used to control the PA RAMP and the PA output power level. The APC module is split into a digital part and an analog part.

The automatic power control (APC) generates an envelope signal to control the power ramp-up, power ramp down and the power level of the TX radio burst. The APC structure is intended to support single-slot and multi-slot transmission with smooth power transition when consecutive bursts are transmitted at different power levels.

**Figure 1. APC and DRP wrapper highlight**




## 1.1 Main Features

A Interface logic between digital Base band and APC analog part.
B Output voltage for the UP- and DOWN ramp.

## 1.2 Signals and I/O description

**Figure 2: Module overview**

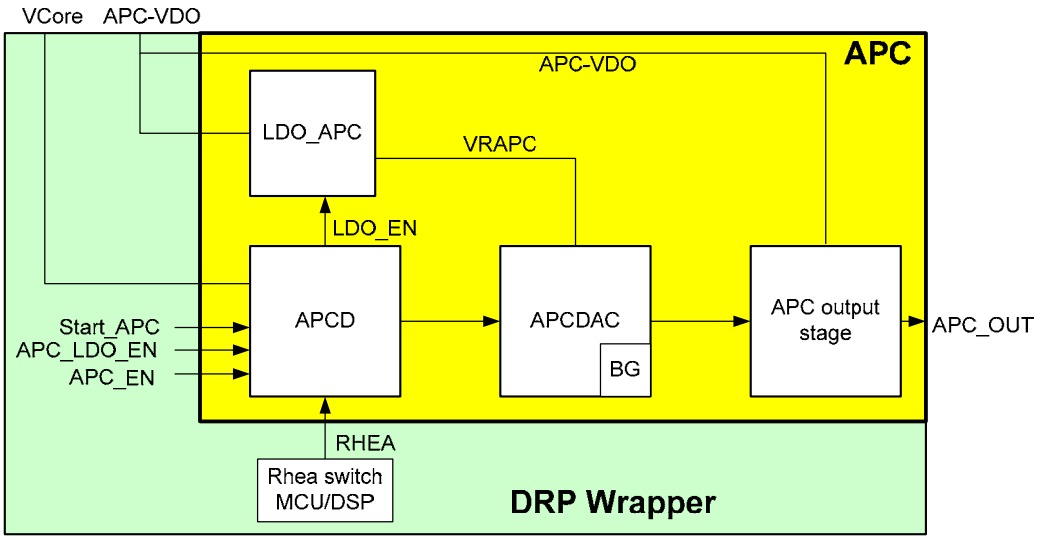



**Table 1: I/O description**

| Signal Name | I/O | Description |
|---|---|---|
| VCore | I | Core digital supply for Locosto. (VDD-DBB).<br>Only used to APC digital part in this module. (1.8 Volt) |
| APC-VDO | I | APC output amplifier supply. (2.8 Volt) |
| Start_APC | I | Internal TSPACT signal from DRP Wrapper (controlled by TPU in DBB). |
| APC_LDO_EN | I | Internal TSPACT signal from DRP Wrapper (controlled by TPU in DBB). |
| APC_EN | I | Internal TSPACT signal from DRP Wrapper (controlled by TPU in DBB). |
| RHEA | IO | 16 bit address and data bus from DBB |
| APC_OUT | O | Analog APC output ramp signal to PA. |

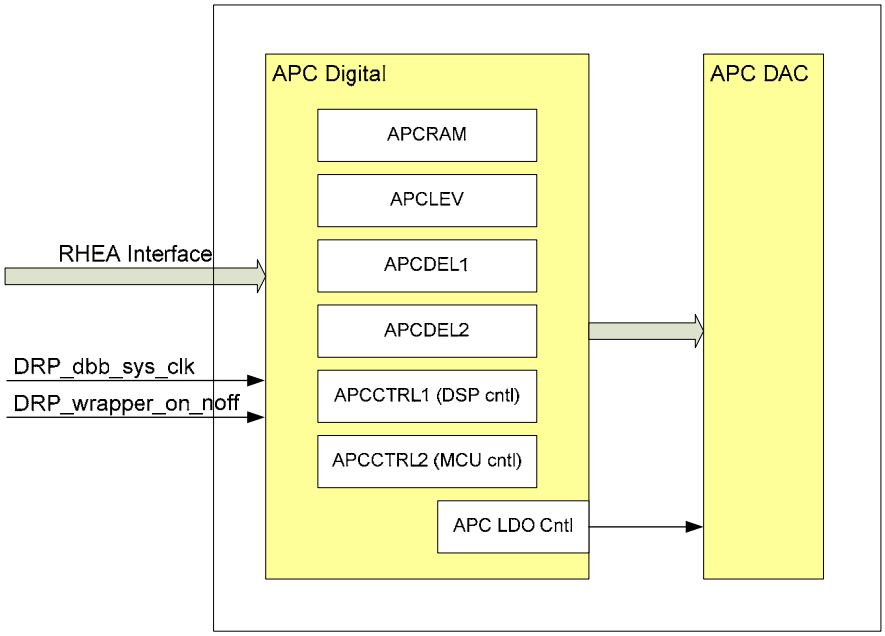
I=Input, O=Output

Note: On TI I-sample VCore and APC-VDO is supplied from Triton. VCore is supplied from VREXTL and APC-VDO is supplied from VRMMC.

# 2 Functional description

## 2.1 Block diagram

**Figure 3: APC digital block diagram**

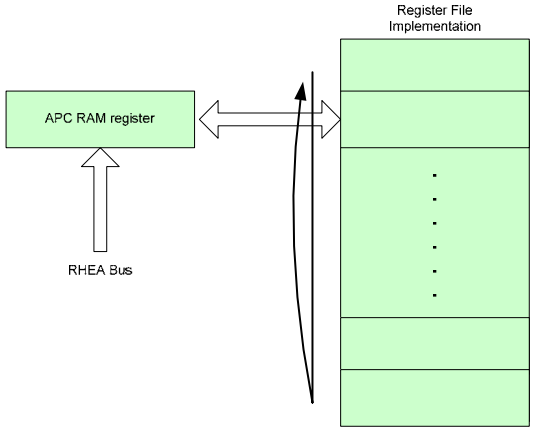



The RHEA interface is used to write/read into/from all registers. All registers are locked for writing once RAMP build up starts.

The RAMP build up is an essential part of this module. To control the precise timing a small microcontroller is built in to help determining precise step to build up the RAMP signal. Ramp is built up by 20 up-/down coefficients stored in APC RAM and fetched through the register (see Table 3: APCRAM)

The APCRAM register includes 20 16-bits words. The 8 LSBs of each word represent the coefficients of the ramp-up shape, the 8 MSBs represent the coefficients of the ramp-down shape. The write pointer will load the register based on an enable signal, which will be generated based on whether RHEA wants a read, or write.

**Figure 4. APCRAM register implementation**




There are three pointers, which run independently of each other namely the RHEA write pointer, RHEA read pointer and the APC internal read pointer, which fetches coefficients. The pointer movements are calculated automatically. Hence repeated Reads/and Write is possible. Write to APCCTRL1 register bit 0 will initialize all the pointers.

Each cell in the APC register contains 8 bits up ramp coefficient and 8 bits down ramp coefficient see Table 3: APCRAM in section 4.2.

## 2.2 RAMP generation.

The shape of ramp-up/down is computed from the value of the *power level step* and from the *coefficients* of the desired shaping filter:

- The *power step* is obtained by subtracting the previous power level (initialized to zero when APC_EN rises) from the new power level programmed by the DBB (APCLEV: 10 bits word).
- The ramp shape is sampled at Fs= 4* 270.833kHz. Its duration (ramp-up or ramp-down) is 5 bits duration (5/270.833e3= 18.4us). So the ramp shape (up or down) is constituted by 20 *coefficients* which are stored in RAM (APCRAM).
- At the end of the ramp, APCLEV is stored (will be previous power level for next burst) and APCLEV register is reset to zero. If a burst is to be transmitted in the next slot, the DBB programs the new power level by programming APCLEV register otherwise APCLEV remains 0.

According to the sign of the power step to be performed, ramp-up or ramp-down coefficients are selected.

The sequence of 10-bits words fed to the 10bit APC DAC is:

Fs= 4* 270.833 kHz:

$$Level(i) = Level_{init} + (step_{level} / 256) \cdot \left( up[i] * (1 - sign_{step}) + dw[i] * sign_{step} \right)$$

where:

$level_{init}$ is the current power level

$step_{lev}$ is the power level step to be done

up[i] are the coefficients of the ramp-up

dw[i] are the coefficients of the ramp-down

$sign_{step}$ is the sign of $step_{lev}$ (0 for plus, 1 for minus)

This ramp is therefore constituted by 20 steps for ramp-up and 20 steps for ramp-down (Fs=4*270.833kHz). No further interpolation is needed.

**Notice:**

Each of the 20 coefficients is an absolute value between 0 and 255. This is different from previous TI solutions.

Before being fed to the 10-bit DAC, the content of the offset register (APCOFF) is added to the 10-bit words computed before.

## 2.3 Sequencing.

APC_LDO_EN TSPact signal enables/disables APC LDO. This LDO can also be enabled by register programming (see Table 8: APCCTRL2).

The APC block is enabled/disabled by APC_EN TSPact signal. When APC_EN goes high, APC is enabled and the content of the offset register APCOFF is fed to the DAC.

There are two modes to control APC ramps. Internal sequencing or External trigger, See Table 8: APCCTRL2

### 2.3.1 Internal sequencing (default mode)

In this mode, APC ramps are controlled by the TSPact signal Start_APC coming from DBB, APC delay registers and an internally generated Ramp_EN signal.

Two delay registers (APC ramp delay 1 and APC ramp delay 2) contain two 10-bit words to control the effective start of the ramp-up (APC_DEL_UP) or ramp-down (APC_DEL_DOWN) relative to Ramp_EN signal. APC ramp delay 1 register contains the 5 LSBs of the two 10–bit words while APC ramp delay 2 register contains the 5 MSBs of the two 10-bit words. These delays can be adjusted independently for ramp-up and ramp-down from 0 to 1023 by quarter-bit units.

| PARAMETER | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| APC_DEL_UP | 0 | | 1023 | ¼ bit |
| APC_DEL_DWN | 0 | | 1023 | ¼ bit |
| Tslot | | 156.25 | | bit |

Bit is relative to GSM bit = 1/270.833kHz

When the rising edge of Start_APC occurs, the APC block generates a Ramp_EN pulse (1/4 bit duration) and APC internal sequencer launches a counter which regenerates a Ramp_EN pulse every Tslot until Start_APC goes low. When Start_APC goes low, a Ramp_EN pulse is also generated.

The ramp starts APC_DEL_UP (or APC_DEL_DOWN according to the power step to be performed) quarter-bits after each Ramp_EN falling edge (leaving the ¼ bit duration of the pulse to compute the APC step).

Before each ramp, DBB programs the new APCLEV for the burst to be transmitted. At the end of the ramp, APCLEV is stored (to be used as the old power level) and APCLEV register is reset to zero. If a new burst is to be transmitted in the following slot, the DBB programs the new APCLEV (otherwise APCLEV stays at 0).

Figure 5. Single slot operation shows APC behavior in single slot operation.

**Figure 5. Single slot operation**

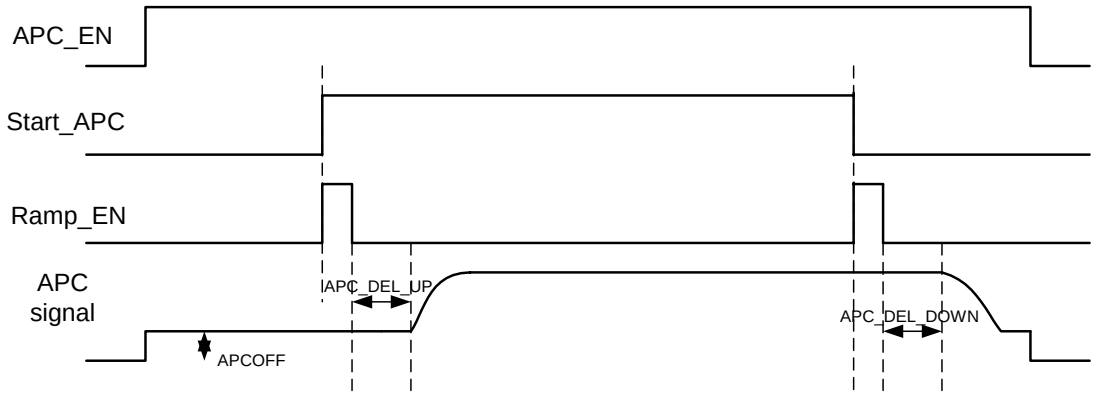
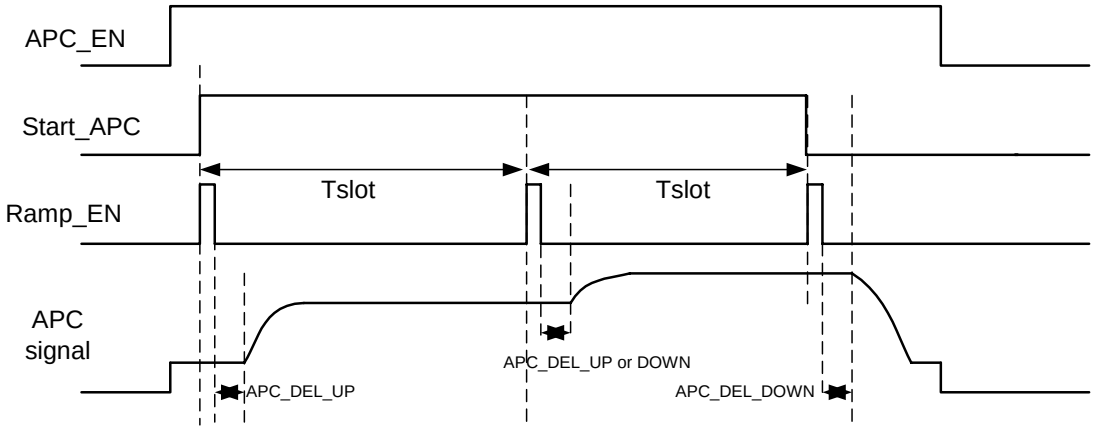


Figure 6. Multi slot operation shows APC behavior in multi-slot operation.

**Figure 6. Multi slot operation**




#### 2.3.1.1 Protection

An internal LOCK signal is generated which will prevent any software writes to any register during RAM build up/down.

Additional hardware protection is provided in terms of that once the ramp achieves the maximum value and if all 20 coefficients are not used then the ramp will stop, this is done to readily reach the full ramp value and not oscillate at the final ramp value. No more fetches will be done from the APCRAM register.

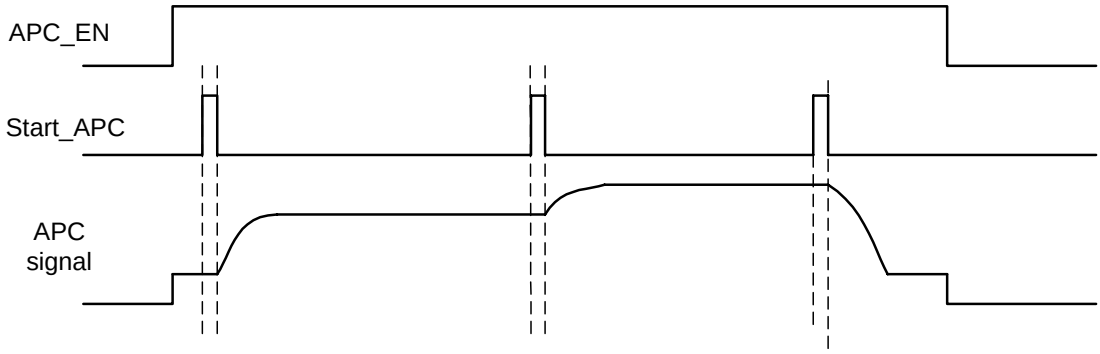
### 2.3.2 External trigger

In this mode, APC delay registers are not used to control the ramp-up/down. Ramp up/down are only controlled by the dedicated TSPact Start_APC, which is a pulse with 1 quarter bit duration signal.

Each time a Start_APC pulse occurs, a ramp-up or down (according to the power level step to be performed) is generated (on falling edge of the pulse to leave one ¼ bit to compute APC step).

Before the ramp, DBB programs the new APCLEV for the burst to be transmitted. When Start_APC occurs, the ramp starts. At the end of the ramp, APCLEV is stored as the old power level and APCLEV register is reset to zero. If a new burst is to be transmitted in the following slot, DBB programs the new APCLEV (otherwise APCLEV stays at 0). When Start_APC occurs, a ramp-up or down (according to the power step to be performed) is generated and so on according to the number of consecutive bursts to be transmitted.

**Figure 7. External trigger mode (multi-slot).**




# 3 APC output.

As described before the APC module consists of 2 parts, a digital part and an analog part. At the output of the digital part is a 10 bit DAC that is buffered to the APC-out signal (ball # U13). The APC-out is connected to the RAMP input of the selected PA.

The maximum APC-out level is minimum 2.1 Volt. With a 10 bit resolution this gives roughly a resolution of 2.1 mV/LSB

The APC offset voltage (pre-ramp voltage) is programmed by 6 bit in the APCCTRL2 register. The maximum offset is 250 mV with a resolution of 4 mV/LSB.

The APC-out has a maximum source current of 200 µA.

# 4 Register manual

## 4.1 Module register mapping summary

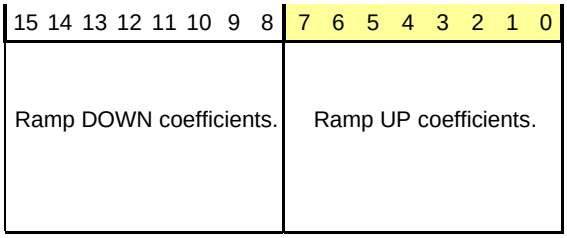
**Table 2: APC Module Register offset address**

| Register Name | Type | Register Width (Bits) | Address offset | Physical Address |
|---|---|---|---|---|
| APCRAM | R/W | 16 | 0x04 | FFFF:5004 / CS10 |
| APCLEV | R/W | 16 | 0x02 | FFFF:5002 / CS10 |
| APCDEL1 | R/W | 16 | 0x06 | FFFF:5006 / CS10 |
| APCDEL2 | R/W | 16 | 0x08 | FFFF:5008 / CS10 |
| APCCTRL1 | R/W | 16 | 0x0A | FFFF:500A / CS10 |
| APCCTRL2 | R/W | 16 | 0x0C | FFFF:500C / CS10 |

## 4.2 APC Register description

**Table 3: APCRAM**

| | | | |
|---|---|---|---|
| **Address Offset** | 0x04 | | |
| **Physical address** | FFFF:5004 | **Instance** | APCRAM |
| **Description** | This register contains the DOWN and UP ramp coefficients. | | |
| **Type** | R/W | | |
| **Write Latency** | Not relevant | | |

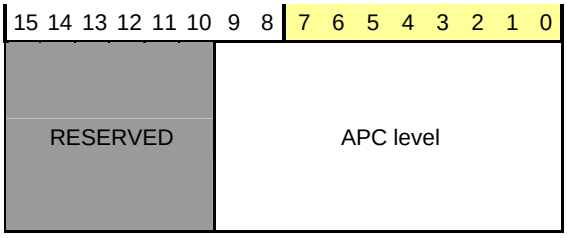



| Bits | Field Name | Description | Type | Reset |
|---|---|---|---|---|
| 15:8 | DWN | Ramp DOWN coefficient, the APC will access 20 * 8 bits RAM through this register | R/W | 0x00 |
| 7:0 | UP | Ramp DOWN coefficient, the APC will access 20 * 8 bits RAM through this register | R/W | 0x00 |

Hence APCRAM is a 20*16 bit circular buffer whose write pointer is automatically reset after the write of the last coefficient.

**Table 4: APCLEV**

| | | | |
|---|---|---|---|
| **Address Offset** | 0x02 | | |
| **Physical address** | FFFF:5002 | **Instance** | APCLEV |
| **Description** | This register contains the APC power level | | |
| **Type** | R/W | | |
| **Write Latency** | Not relevant | | |

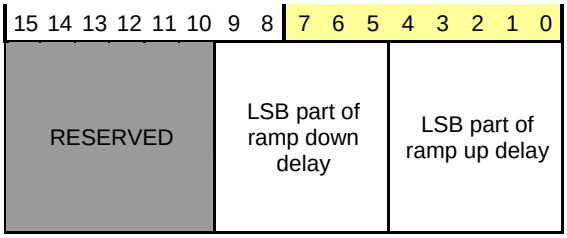



| Bits | Field Name | Description | Type | Reset |
|---|---|---|---|---|
| 15:10 | RESERVED | | | 0x00 |
| 9:0 | APCLEV | 10 bits APC level | R/W | 0x00 |

At the end of each ramp, APCLEV is reset to 0.

**Table 5: APCDEL1**

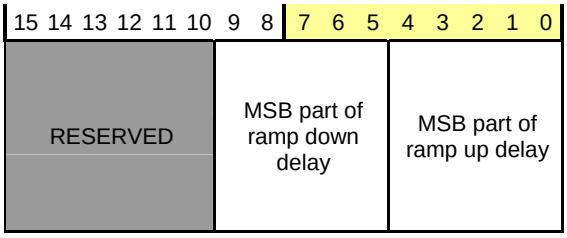
| | | | |
|---|---|---|---|
| **Address Offset** | 0x06 | | |
| **Physical address** | FFFF:5006 | **Instance** | APCDEL1 |
| **Description** | This register contains the LSB part of the Ramp down and Ramp up delays. | | |
| **Type** | R/W | | |
| **Write Latency** | Not relevant | | |




| Bits | Field Name | Description | Type | Reset |
|---|---|---|---|---|
| 15:10 | RESERVED | | | 0x00 |
| 9:5 | APC_DEL_DWN1 | 5 bit LSB part of down ramp delay relative to the rising edge of Start_APC in internal sequencing mode only | | |
| 4:0 | APC_DEL_UP1 | 5 bit LSB part of down up delay relative to the rising edge of Start_APC in internal sequencing mode only | | |

**Table 6: APCDEL2**

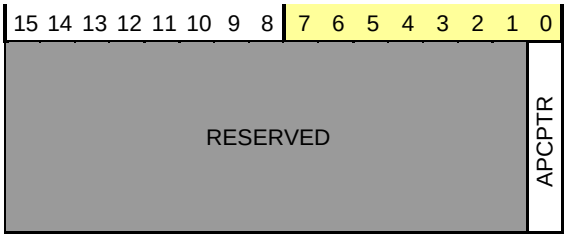
| | | | |
|---|---|---|---|
| **Address Offset** | 0x08 | | |
| **Physical address** | FFFF:5008 | **Instance** | APCDEL2 |
| **Description** | This register contains the MSB part of the Ramp down and Ramp up delays. | | |
| **Type** | R/W | | |
| **Write Latency** | Not relevant | | |




| Bits | Field Name | Description | Type | Reset |
|---|---|---|---|---|
| 15:10 | RESERVED | | | 0x00 |
| 9:5 | APC_DEL_DWN2 | 5 bit MSB part of down ramp delay relative to the rising edge of Start_APC in internal sequencing mode only | | |
| 4:0 | APC_DEL_UP2 | 5 bit MSB part of down up delay relative to the rising edge of Start_APC in internal sequencing mode only | | |

**Table 7: APCCTRL1**

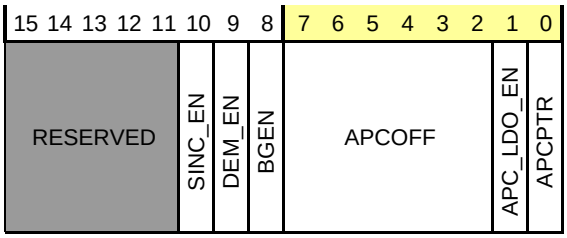
| | | | |
|---|---|---|---|
| **Address Offset** | 0x0A | | |
| **Physical address** | FFFF:500A | **Instance** | APCCTRL1 |
| **Description** | Initialize the APCRAM pointer by writing 1. | | |
| **Type** | R/W | | |
| **Write Latency** | Not relevant | | |




| Bits | Field Name | Description | Type | Reset |
|---|---|---|---|---|
| 15:1 | RESERVED | | | 0x00 |
| 0 | APCPTR | Writing 1 initializes the APC RAM pointer to 0. | | 0x00 |

**Table 8: APCCTRL2**

| | | | |
|---|---|---|---|
| **Address Offset** | 0x0C | | |
| **Physical address** | FFFF:500C | **Instance** | APCCTRL2 |
| **Description** | Initialize the APCRAM pointer by writing 1. | | |
| **Type** | R/W | | |
| **Write Latency** | Not relevant | | |




| Bits | Field Name | Description | Type | Reset |
|---|---|---|---|---|
| 15:11 | RESERVED | | | 0x00 |
| 10 | SINC EN | Sinc Enable | | 0x00 |
| 9 | DEM_EN | DEM Enable | | 0x00 |
| 8 | BGEN | Band Gap Enable | | 0x00 |
| 7:2 | APCOFF | 6 bit APC offset register | | 0x00 |
| 1 | APC_LDO_EN | Enable APC LDO (VRAPC) | | 0x00 |
| 0 | MODE | 0: internal sequencer; 1: external trigger for ramp start | W | 0x00 |

APCOFF is fed to the DAC while APC_EN is high. The APCOFFSET is left shifted by 1 bit and appended with zero, thus internally making it 7 bits, to be added with the APCOUT value calculated.

The APC LDO can be enabled in two different ways:

- Using APC_LDO_EN bit in APCCTRL2 register
- Or using APC_LDO_EN TSPact signal from the TPU2OCP module in the DRP Wrapper.

# 5 Appendix A – Defalut Ramp values example.

## 5.1 Default Power Ramp Table

This section contains an example on how the coefficients of the ramp-up and ramp-down shaping filters and level value registers of the Locosto are to be controlled.

For each power level the following numbers must be defined:

**Table 9. The values used to define the power ramps.**

| Ref | Register | Function |
|---|---|---|
| Level | APCLEV | 10 bit APC power level |
| Up[0..19] | APCRAM | 20 ramp up steps |
| Dw [0..19] | APCRAM | 20 ramp down steps |
| DELU | APCDEL1,2 | APC up ramp delay, 10 bit |
| DELD | APCDEL1,2 | APC down ramp delay, 10 bit |

Each power level is associated with a nominal output power, a power template, a default level value, and a set of ramp timing values, DELU and DELD.

### 5.1.1 Power ramp tables for RF3178G

Below table show the Ramp shape coefficient that is used on I-sample as initial values. All power levels has got the same ramp shape, but this will be changed during verification and optimized to best performance. See Table 12 for information about improved RAMP shape on I-sample 2.8.

**Table 10. Initial ramp shaping coefficient for I-sample version 1.0**

| RAMP shape coefficient | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GSM 850 | Ramp up | 0 | 0 | 0 | 0 | 0 | 10 | 10 | 21 | 44 | 69 | 96 | 119 | 143 | 166 | 188 | 210 | 228 | 243 | 255 | 255 |
| | Ramp down | 255 | 247 | 236 | 220 | 199 | 167 | 120 | 82 | 45 | 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EGSM 900 | Ramp up | 0 | 0 | 0 | 0 | 0 | 10 | 10 | 21 | 44 | 69 | 96 | 119 | 143 | 166 | 188 | 210 | 228 | 243 | 255 | 255 |
| | Ramp down | 255 | 247 | 236 | 220 | 199 | 167 | 120 | 82 | 45 | 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DCS1800 | Ramp up | 0 | 0 | 0 | 0 | 0 | 10 | 10 | 21 | 44 | 69 | 96 | 119 | 143 | 166 | 188 | 210 | 228 | 243 | 255 | 255 |
| | Ramp down | 255 | 247 | 236 | 220 | 199 | 167 | 120 | 82 | 45 | 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCS1900 | Ramp up | 0 | 0 | 0 | 0 | 0 | 10 | 10 | 21 | 44 | 69 | 96 | 119 | 143 | 166 | 188 | 210 | 228 | 243 | 255 | 255 |
| | Ramp down | 255 | 247 | 236 | 220 | 199 | 167 | 120 | 82 | 45 | 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 11. Initial ramp shaping coefficient for I-sample 1.1 and I-sample 2.0**

| RAMP shape coefficient | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GSM-850 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 14 | 37 | 64 | 95 | 127 | 160 | 191 | 218 | 238 | 251 | 255 |
| | RAMP-DOWN | 255 | 251 | 238 | 218 | 191 | 160 | 127 | 95 | 64 | 37 | 14 | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EGSM-900 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 14 | 37 | 64 | 95 | 127 | 160 | 191 | 218 | 238 | 251 | 255 |
| | RAMP-DOWN | 255 | 251 | 238 | 218 | 191 | 160 | 127 | 95 | 64 | 37 | 14 | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DCS-1800 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 14 | 37 | 64 | 95 | 127 | 160 | 191 | 218 | 238 | 251 | 255 |
| | RAMP-DOWN | 255 | 251 | 238 | 218 | 191 | 160 | 127 | 95 | 64 | 37 | 14 | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCS-1900 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 14 | 37 | 64 | 95 | 127 | 160 | 191 | 218 | 238 | 251 | 255 |
| | RAMP-DOWN | 255 | 251 | 238 | 218 | 191 | 160 | 127 | 95 | 64 | 37 | 14 | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 5.1.2 Final APC filter and RAMP coefficients for I-sample 2.8.

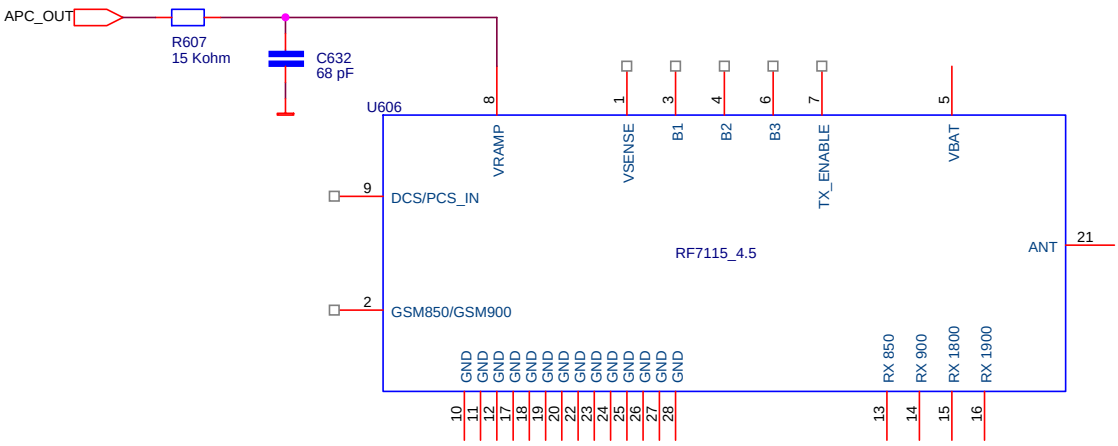
To improve TX switching spectrum a full characterisation of the PA module RF7115 used on I-sample has been done. This leads to updates in the ramping coefficients and APC filter for I-sample 2.8.

The RAMP coefficients are different for each band to compensate for the small differences in the PA transfer function (APC in to PA out)

**Table 12. Updated ramp shaping coefficient for I-sample 2.8. APC filter changed to 15 kΩ series resistor and 68 pF shunt capacitor**

| RAMP shape coefficient | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GSM-850 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 16 | 32 | 58 | 93 | 127 | 158 | 186 | 210 | 229 | 244 | 252 | 255 |
| | RAMP-DOWN | 252 | 244 | 229 | 210 | 186 | 158 | 127 | 93 | 58 | 29 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EGSM-900 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 15 | 30 | 54 | 90 | 125 | 157 | 185 | 210 | 229 | 243 | 252 | 255 |
| | RAMP-DOWN | 252 | 243 | 229 | 210 | 185 | 157 | 125 | 90 | 54 | 27 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DCS-1800 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 16 | 31 | 55 | 92 | 126 | 158 | 186 | 210 | 229 | 244 | 252 | 255 |
| | RAMP-DOWN | 252 | 244 | 229 | 210 | 186 | 158 | 126 | 92 | 55 | 28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCS-1900 | RAMP-UP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 15 | 30 | 53 | 90 | 124 | 156 | 185 | 209 | 229 | 243 | 252 | 255 |
| | RAMP-DOWN | 252 | 243 | 229 | 209 | 185 | 156 | 124 | 90 | 53 | 37 | 10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 8. Updated APC filter for I-sample**



### 5.1.3 Initial APC values for I-sample 1.0

Initial APC-level values for TX module RF3178G

**Table 13. Initial APC-level used on I-sample version 1.0**

| Power level | Output power | | GSM850 APC level | | | GSM900 APC level | | | Output power | | DCS APC level | | | PCS APC level | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | V | | DAC level | V | | DAC level | | | V | | DAC level | V | | DAC level |
| **0** | | | | | | | | | 29,5 | dBm | 1,152 | V | **561** | 1,191 | V | **580** |
| **1** | | | | | | | | | 28 | dBm | 1,033 | V | **503** | 1,033 | V | **503** |
| **2** | | | | | | | | | 26 | dBm | 0,894 | V | **436** | 0,894 | V | **436** |
| **3** | | | | | | | | | 24 | dBm | 0,775 | V | **378** | 0,775 | V | **378** |
| **4** | | | | | | | | | 22 | dBm | 0,697 | V | **340** | 0,697 | V | **340** |
| **5** | 32,5 | dBm | 1,230 | V | **599** | 1,23 | V | **599** | 20 | dBm | 0,617 | V | **301** | 0,617 | V | **301** |
| **6** | 31 | dBm | 1,092 | V | **532** | 1,092 | V | **532** | 18 | dBm | 0,557 | V | **271** | 0,557 | V | **271** |
| **7** | 29 | dBm | 0,934 | V | **455** | 0,934 | V | **455** | 16 | dBm | 0,497 | V | **242** | 0,497 | V | **242** |
| **8** | 27 | dBm | 0,795 | V | **387** | 0,795 | V | **387** | 14 | dBm | 0,458 | V | **223** | 0,458 | V | **223** |
| **9** | 25 | dBm | 0,716 | V | **349** | 0,716 | V | **349** | 12 | dBm | 0,439 | V | **214** | 0,439 | V | **214** |
| **10** | 23 | dBm | 0,617 | V | **301** | 0,617 | V | **301** | 10 | dBm | 0,418 | V | **204** | 0,418 | V | **204** |
| **11** | 21 | dBm | 0,557 | V | **271** | 0,557 | V | **271** | 8 | dBm | 0,398 | V | **194** | 0,398 | V | **194** |
| **12** | 19 | dBm | 0,498 | V | **243** | 0,498 | V | **243** | 6 | dBm | 0,378 | V | **184** | 0,378 | V | **184** |
| **13** | 17 | dBm | 0,458 | V | **223** | 0,458 | V | **223** | 4 | dBm | 0,358 | V | **174** | 0,358 | V | **174** |
| **14** | 15 | dBm | 0,438 | V | **213** | 0,438 | V | **213** | 2 | dBm | 0,338 | V | **165** | 0,338 | V | **165** |
| **15** | 13 | dBm | 0,398 | V | **194** | 0,398 | V | **194** | 0 | dBm | 0,318 | V | **155** | 0,318 | V | **155** |
| **16** | 11 | dBm | 0,378 | V | **184** | 0,378 | V | **184** | | | | | | | | |
| **17** | 9 | dBm | 0,358 | V | **174** | 0,358 | V | **174** | | | | | | | | |
| **18** | 7 | dBm | 0,338 | V | **165** | 0,338 | V | **165** | | | | | | | | |
| **19** | 5 | dBm | 0,318 | V | **155** | 0,318 | V | **155** | | | | | | | | |

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