

TCS2300 Program
LoCosto – Integrated Circuit
Top Level Specification
F761553

Rev: 0.1

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	Originator	Approval
Name	TI	
Date	June 24, 2005	



HISTORY

Version	Date	Originator	Notes
0.1	June 24, 2005	Eric, Saket, Asif	1

Notes:

1. Creation of the document; Integrated DBB (Calypso-Plus Device based) and Digital RF Processor

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Reference Documents

Last document revision should be used unless specified

- | | |
|--|-------------------|
| 1. LoCosto Product Requirements Document | Texas Instruments |
| 2. TriTon Analog & Power Management Device top level Specification | Texas Instruments |
| 3. LoCosto Software Architecture Specification Document | Texas Instruments |
| 4. CalypsoPlus F761710 Device Specification | Texas Instruments |
| 5. DRP 2.0 Module Integration Document | Texas Instruments |
| 6. GS50 Specification and Design Information | Texas Instruments |
| 7. LoCosto Chip-Set Power Management System Specification | Texas Instruments |
| 8. Locosto debug observation module specification | Texas Instruments |
| 9. Locosto Register Map Document | Texas Instruments |

1. LoCosto-IC Introduction

The **LoCosto** Integrated Circuit (IC), associated to **TriTon** Analog Base Band (ABB) chip (cf document [2]), and **TCR3.2** software layer (cf document [3]), make up the low-cost TI chip-set solution (**TCS2300 Program**) for addressing the full 2.5G GSM/GPRS^[TU1] as initiated by the LoCosto Product Requirements Document (cf document [1]).

2. LoCosto System-On-Chip (SOC) Overview

The LoCosto-IC, designed from the TI **GS50 90-Nanometer** ASIC back-plane technologies, merges Digital Base Band (DBB) and Radio Frequency (RF) functions. Based on the GS50 Standard Cells macro library and the **1218C027** manufacturing process, Analog-RF and Digital modules are integrated on a single-chip, thereby maximizing the system integration.

The LoCosto-IC basically consist of:

- ?? The Digital Base Band structure
- ?? The Radio Frequency Sub-System
- ?? The RF Sub-System Wrapper

2.1 Digital Base Band Structure

The DBB supports the processing of GSM radio signals in switching circuit mode and packet data mode (GPRS) for up to class 12^[TU2], including evolution such as SAIC & localization system (A-GPS...) in compliance with the ETSI specification.

In addition the DBB can process, in a secure environment, messaging & multimedia services, such as EMS/MMS, WAP-browsing, Audio-players, Camera-functions^[TU3], JAVA-based downloaded application...

The TCR3.2 software layer that controls the radio function as well as applications is based on and includes all features of TCR 3.1 plus additional specific components (See document [3]).

The DBB H/W function is based on the Calypso-Plus device (cf document [4]) and as such maintains the computing performance as well as the security levels, whereas system connectivity is down graded however still enabled for supporting system such as TI-Bluetooth, TI-AGPS &/ Camera systems^[TU4].

Performances:

The computing and busses performances are illustrated *Figure 1*

To achieve the low-cost target, still providing the High processing capability, LoCosto-IC compared to CalypsoPlus embeds a reduced & re-partitioned memory system; the computing performances of the DBB System rely on:

?? cDSP (M30L154) Sub-System @104Mhz

~~EE~~ 30-K 16-bit word RAM (including 16-Kw API)

~~EE~~ 154-K 16-bit word ROM

~~EE~~ 10-K 16-bit word RAM (external to cDSP macro, intended for Application; MP3[TU5]...)

~~EE~~ Memory-mapped control & status register (XIO/RHEA @52MHz).

?? **ARM7 @104Mhz**, (Host processor)

~~EE~~ **2.5-Mbit Internal SRAM, single cycle access @104MHz**

~~EE~~ **1.5-Mbit Internal ROM** (Midi, JPEG... engines support) **single cycle access @104MHz**

~~EE~~ 16-Kw ARM/cDSP RAM I/F (API), 2-cycle @104Mhz

Important notice:

In Shared Access Mode wait state must be inserted to comply with DSP clock synchronization; access time must be greater than 4 DSP cycle

~~EE~~ Memory-mapped control & status register (RHEA & Memory-Like Peripherals) 2-cycle @104Mhz,.

~~EE~~ Up to **124M-Byte External memory accessed @52MHz** Max (~15ns access time)

- **Mux'ed Address-Data Burst-Memories (Flash &/ PSRAM)**
- 16-bit bus width; Support Byte, Half-word (16-bit), Word (32-bit) access
- **1/2(default)/3/4 CS's x 4/8(Default)/16/32-Mbyte**
- Asynchronous/Burst single-access Read/Write (Default),
- **Continuous or 4 x 32-bit (8 x 16-bit) word burst Read/Write**
- **2-line 4 x 32-bit word (8 x 16-bit) Pre-Fetch Buffer**
- Access-Mode and I/F timing configurable for each CS's
- Flexible timing control (Wait/Dummy Cycles insertion) for supporting most common memories

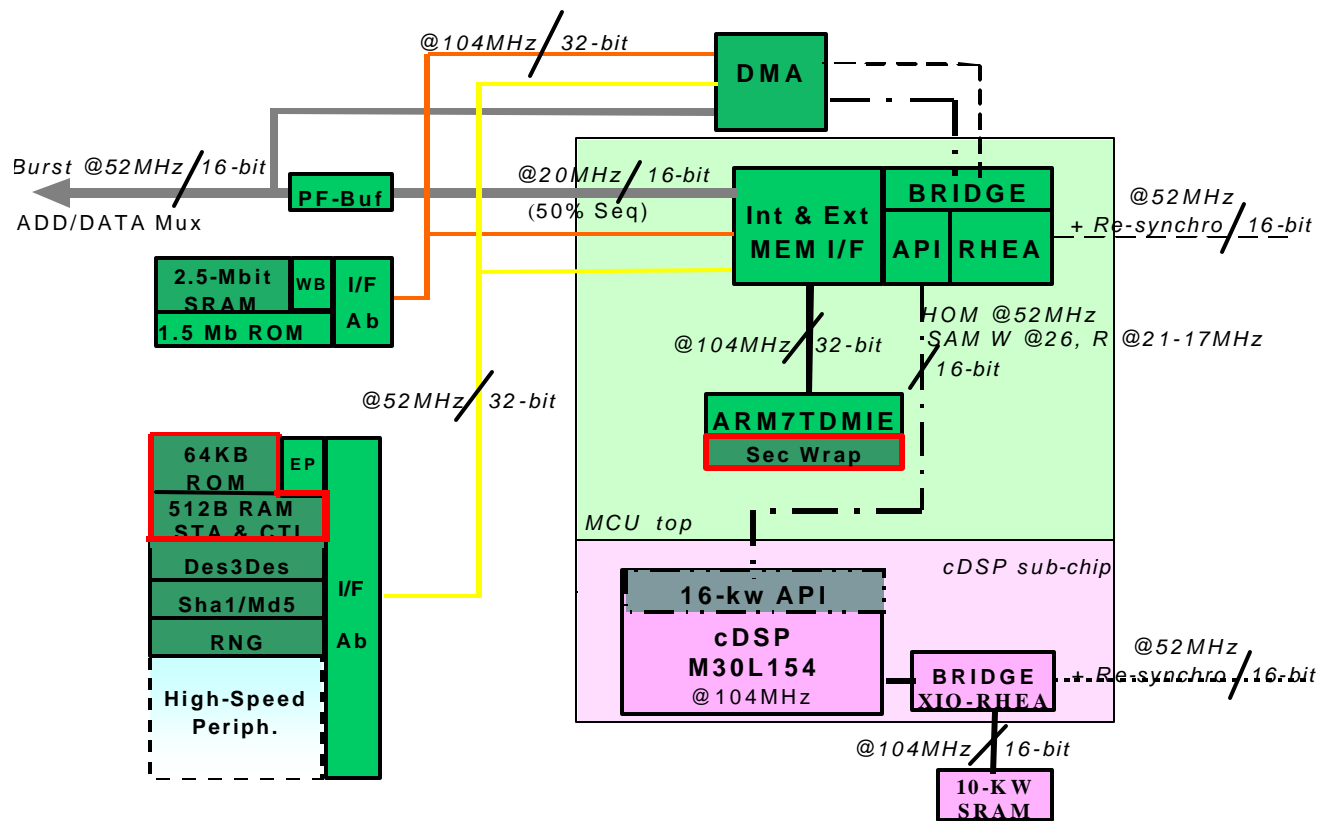
?? Direct Memory Access supporting

~~EE~~ **5-Port,**

- **Internal SRAM/ROM @104MHz,**
- **"Memory-like" peripherals @52MHz,**
- RHEA Peripherals @52Mhz,

- ARM/cDSP Com-RAM @52MHz,
- External-memory up to 52MHz
- ✂ Addressing mode
 - Constant
 - Incremented
 - Frame-Increment
- ✂ 6-Channel,
- ✂ 31 Request-sources

Figure 1: Busses performances



Security:

In addition to the CalypsoPlus's Secure services, the LoCosto-IC support the "Boot-manufacturing" from an USB or UART link for firmware setup; **"Boot-manufacturing" from IRDA is no more supported**

The MCU secure & protect-able functions are distributed to The RHEA bus (16-bit width) and to the "Memory-Like" peripheral bus (32-bit width) both running @52MHz; The MCU Secure environment consist of:

Memory-Like Peripheral Bus (MCU)

- ?? **64-KByte Boot ROM,**
- ?? 512-Byte Secure RAM
- ?? Protected Mode control & status register
- ?? Random Number Generator
- ?? Hashing SHA-1/MD5 Crypto-processor
- ?? Symmetrical encryption DES/3-DES Crypto-processor

RHEA Bus (MCU)

- ?? Secure Interrupt Handler
- ?? Secure Watch-Dog/Timer
- ?? Protected Resources Reset Manager
- ?? Enhanced Memory Protection Unit
- ?? DMA's secure-Channel
- ?? CLKM; system-Clock's Lock
- ?? Manufacturer Public Key (128-bit eFuses programmed @package)

Connectivity:

LoCosto-IC Connectivity peripherals are listed below. Peripherals are mainly distributed to the 16-bit width RHEA bus (either cDSP or MCU) and to the 32-bit width "Memory-Like" bus for peripheral requiring high throughput and accessed from the MCU only.

RHEA Bus (MCU &/ cDSP)

- ?? 1 Enhanced Keyboard controller
 - ?? Up to 5-Row x 5-Column matrix /25 keys (interrupt driven)
- ?? 1 LCD-controller 8-bit parallel interface @13MHz (6800 & 8080 protocol) with DMA capability
- ?? 1 USIM (Universal Subscriber Identity Module) Interface @100Kbps
- ?? 1 Multi-Channel Serial Interface @13Mbps; **Exclusive Static sharing DSP(default @reset) / MCU with DMA capability**
 - ?? Voice Interface for external BlueTooth PCM-Codec connection
 - ?? cDSP sub-system debug...

- ?? 1 UART Modem/IRDA with Auto-Baud capability @115.2Kbps (Exclusive Static sharing DSP / MCU (default @reset). DMA capability for MCU setting
- ✂✂ Data Interface for external BlueTooth Modem connection
 - ✂✂ Or Host serial cable 115.2Kbps (support Manufacturing Flash Loader @3.25Mbps)
 - ✂✂ Or IRDA FIR @4Mbps
- ?? 2 I2C H/W-controller @400Kbps (1 MCU + 1 DSP /same external bus I/F) for controlling
- ✂✂ TriTOn ABB (Power, USB-Xcvr, Voice & Stereo Codec's)
 - ✂✂ Slave-Only components may be added on this bus (see section 7.4.4.14)
- ?? 1 I2C H/W-controller @400Kbps (MCU only) for controlling options such as:
- ✂✂ A-GPS module
 - ✂✂ Frequency Modulation Radio chip(FM Stereo Radio)
 - ✂✂ Camera Sensor/Module[TU6]
 - ✂✂ B/W LCD...

Important Note:

FM, Camera [TU7]& LCD chips are slave-only components and may be connected on the I2C bus with Triton ABB...

- ?? 1 C-port/I2S Audio-Stereo Codec serial interface, Slave up to 3.072Mbps; **Exclusive Static sharing DSP(default @reset) / MCU. DMA capability for both setting**
- ?? 1 USB 1.1 client full speed (12Mbps)
- ✂✂ Host serial cable (PC connection...)
- And Support for
- ✂✂ Car-kit
- ?? Up to 48 General Purpose I/O's with Interrupt capability, all available as primary or secondary function combined with:
- ✂✂ Ext-Memory control signal's (Address, Chip-Select...)
 - ✂✂ LCD, Camera-Core[TU8], Nand-Flash, UART control signal's
 - ✂✂ Audio CODEC input
 - ✂✂ Modulated pulse-width generation,
 - ✂✂ MCSI, SPI's data & control
 - ✂✂ KeyBoard, Co-Emulation control...

Memory-Like Peripheral Bus (MCU)

- ?? 1 **Parallel Camera-port** (8-bit, H/V synchs, Ctl/Pxl Clks @48/52MHz) or **serial Compact Camera Port** (Slave 2 x 2-wires @208 Mbps)
- ✂✂ Camera module (RGB, YUV and optional JPEG output format)
 - ✂✂ Video companion chip with compression engine (TI Golden-Eye chip...)
- ?? [TU9]1 Nand-Flash 8-bit I/F up to 26MHz intended for Data storage

?? 1 **SPI Master/Slave up to 26Mbps** to optionally support external component such as:

~~??~~ LCD-controller with serial I/F (secondary screen B/W or basic-color)

~~??~~ Video companion chip (TI Golden-Eye chip...)

cDSP embedded TI Bus

?? 1 Voice Serial Port Slave @500kbps (DSP sub-system)

Note:

All connectivity interfaces support a 1.8V maximum voltage with the exception of the USIM pin's that are 3V compliant

Compared to CalypsoPlus

The LoCosto IC **does not integrate**:

?? RTC; this function is included into TriTon ABB chip.

?? Slicer & 13MHz//26MHz input-clock detector

?? TSP (see DRP Wrapper)

?? Patch-Unit

?? SIM Card I/F (USIM only is implemented in LoCosto)

?? 3 UART's ; (1 UART - Modem & IRDA - is implemented; IRDA boot no more supported)

?? μ Wire

?? MMC/MS

?? cDSP 32Kw Shared RAM (extended RAM is reduced to 10Kw & not accessible by MCU)

?? 3V I/O's (exception for USIM)

?? Package & Pin compatibility

The following **functions are upgraded**:

?? Internal Memory, Int/Ext Memory I/F, DMA (see above -DBB Computing performance-)

?? 104Mhz/52MHz MCU sub-system partitioning (Memory / Rhea & Memory-Like Periph)

?? cDSP Sub-System & extension RAM

?? 2 x I2C DSP & MCU (ABB no more controlled by SPI)

?? ULPD & CLKM (Power & Clock sequencing)

?? Interrupt-Handler and DMA (Channels allocation)

?? EMPU (Memory alignment, granularity...)



- ?? C-port & MCSI (DSP/MCU RHEA-Switch)
- ?? TPU alignment /DRP (see DRP Wrapper)
- ?? APLL(96Mhz + div/2)
- ?? A5-1/2/3 & GEA 1/2/3 Cipherring module
- ?? LoCosto S-O-C Configuration
- ?? USIM I/O's Voltage (DEMOS & Pbias implementation)
- ?? TI reserved Security-Emulation Mode (adjusted w/ new memory footprint);
- ?? eFuse & JTAG Controller
- ?? Manufacturing-Boot via USB, no more IRDA (Secure Boot ROM)

Whereas some **blocks remain un-changed:**

- ?? Bridge API & RHEA
- ?? Timer 1,2 & WDT
- ?? PWL, PWT, LPG
- ?? DPLL
- ?? GPIO's, BU, LT
- ?? Keyboard (5x5)
- ?? NandFlash (slave port not supported)
- ?? LCD

Important Notes

The DBB part maintains the same capability as Calypso-family in terms of H/W debug, S/W development as well as test engineering support (Die-Id, BIST Memory...)

2.2 LoCosto S-O-C Block Diagram

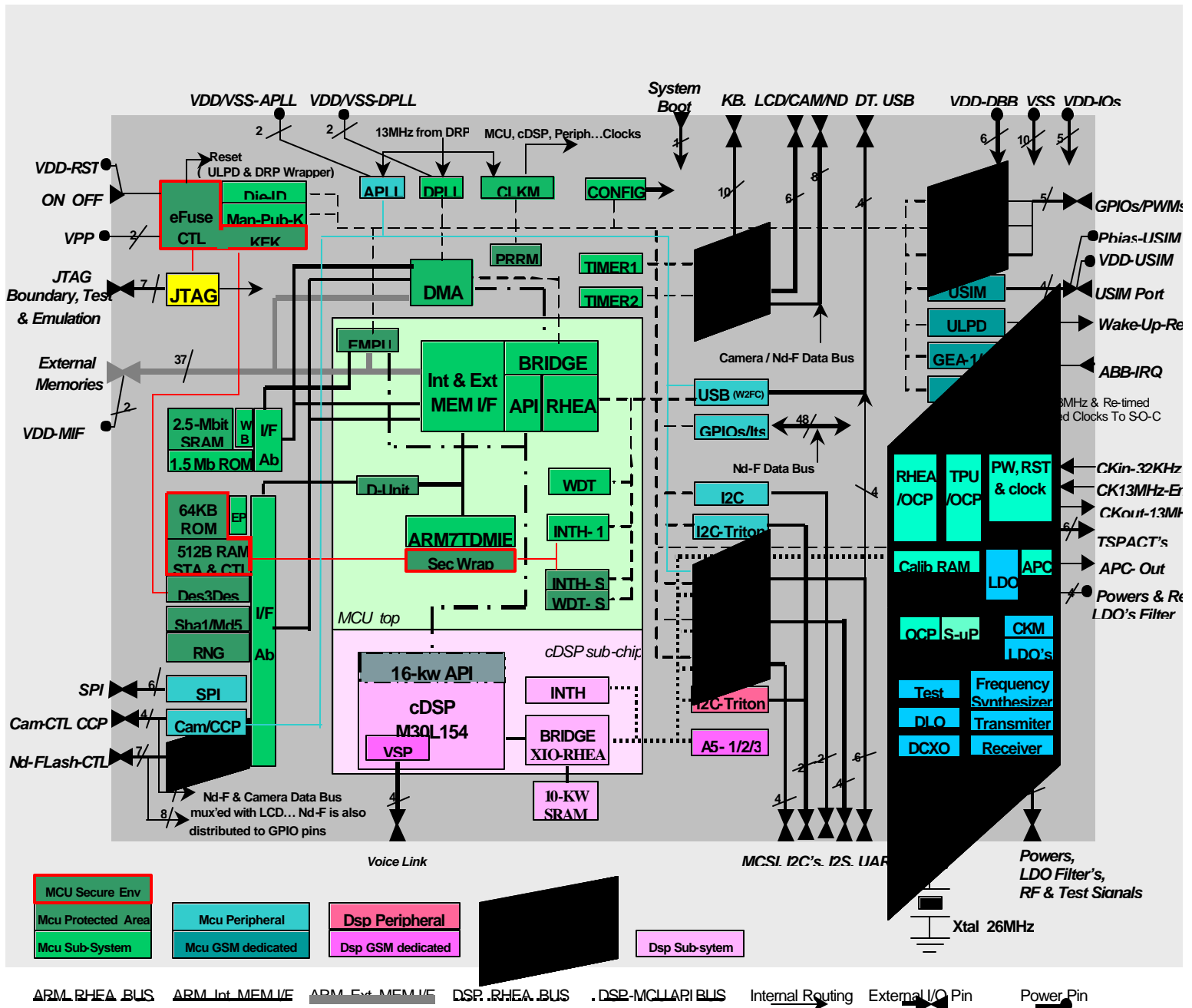


Figure 2: LoCosto-IC Block Diagram[TU10]

2.3 Radio Frequency Sub-System

The Radio Frequency part is an RF transceiver based on the Digital Radio Processor (DRP) architecture. The DRP2.0 Sub-Chip supports GPRS up to class 12[TU11]; it is designed for Quad band operation supporting both the Europe and the US bands (E-GSM 900 and DCS 1800 bands, GSM 850 and PCS 1900 bands respectively)..

The **Figure 3** below highlight the DRP2.0 Sub-Chip architecture which is based on:

- ?? A frequency synthesizer implemented as an All Digital PLL (ADPLL) loop. Both transmitter and receiver part are controlled from this single ADPLL
- ?? A Direct frequency/phase modulation transmitter.
 - ?? Pulse forming DTX block
 - ?? Low and high band pre-power amplifiers
- ?? A near-zero I/F receiver scheme.
 - ?? RF front-end (LNA, TA, Mixer & SCF)
 - ?? RF back-end (CTA, ?? modulator & DRX)

In addition the DRP2.0 includes:

- ?? The CKM module that generates clocking signals for the RF part and permits the DBB system clock re-synchronization.
- ?? The Script Processor, used for configuring the transmitter, receiver and ADPLL.
- ?? The CTL module that manages the analog control bits and launches the script processor.
- ?? The DCXO supplying the reference frequency for the APDLL.
- ?? The DTST and ATST for digital and analog test.
- ?? The OCP module as communication path to a DBB domain.
- ?? LDO's for powering separately DCXO, DLO, Analog components and RF I/O's. The DRP digital-block's are supplied with the DBB-Core power source (TriTon-VRCore)

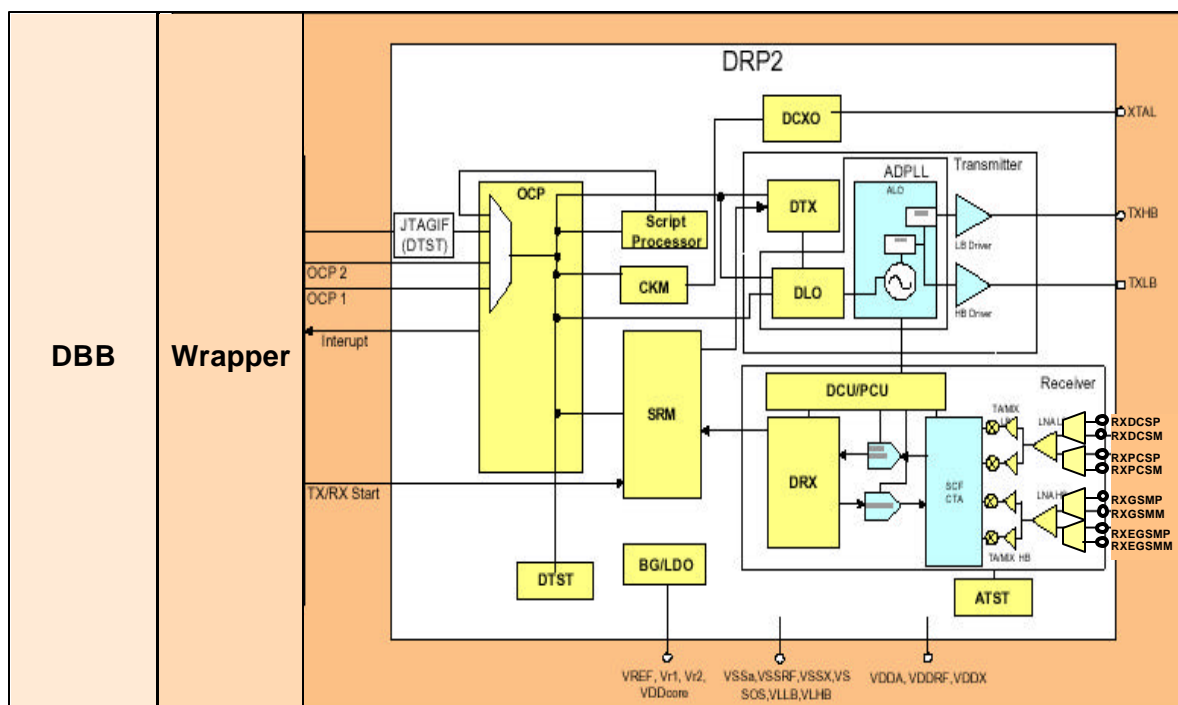


Figure 3: DRP2.0 Block Diagram

Note:

The DRP2.0 Sub-chip has dedicated H/W debug, S/W development as well as test engineering support that remains available within LoCosto-IC, either combined with DBB test & emulation facility, or directly available @package level; here again Validation as well as Product engineering requirement are provided in separate documents

The DRP2.0 is delivered as a Sub-chip with “complex I/O’s” including RF Front-End I/F, Power-pins & test-pins. See **DRP 2.0 Module Integration Document** (cf document [5]). The DRP2.0 package ball requirement is listed section: **5. LoCosto-IC I/O signals**

2.4 RF Sub-System Integration (DRP Wrapper)

The DRP Wrapper completes the LoCosto System-On-Chip. This additional circuitry is designed to adjust the DRP2.0 Sub-Chip to the LoCosto-IC environment. The DBB processing units (DSP, MCU, TPU) interface the DRP through this wrapper.

The DRP Wrapper includes:

- ?? RHEA/OCP bridges;
 - ?? DSP-DRP Control & data path
 - ?? MCU/DMA-DRP Control & data path
- ?? Interrupt & DMA Request
 - ?? Rx events Programmable mask counter (RHEA bus)
- ?? TPU/OCP I/F
 - ?? Q-bit timed event control from DBB to DRP
 - ?? Q-bit timed event control from DBB to Front-End Module & Power-Amplifier (TSPACT's)
- ?? Power, reset & Clock system management;
 - ?? Power-up sequencing
 - ?? Programmable startup timer (RHEA bus)
 - ?? DCXO & Retimed Clock control
- ?? Calibration/Compensation RAM
 - ?? 4-KByte RAM Shared DBB/DRP
 - ?? XIP for DRP's Script-Processor
 - ?? DSP & MCU/DMA access for calibration scenario load/pre-set
- ?? APC function
 - ?? Dedicated LDO
 - ?? APC digital control
 - RHEA I/F to DSP & MCU/DMA
 - APC sequencer
 - Ramp-Table/Memory
 - APC & LDO Configuration registers
 - ?? Digital/Analog Converter
 - ?? Output Amplifier
- ?? TEST & debug capability DBB/DRP alignment regarding
 - ?? TAP/JTAG interface
 - ?? eFuse-programmable logic
 - ?? Scan-chain

The **Figure 4** here after, shows the DRP wrapper sub-functions.

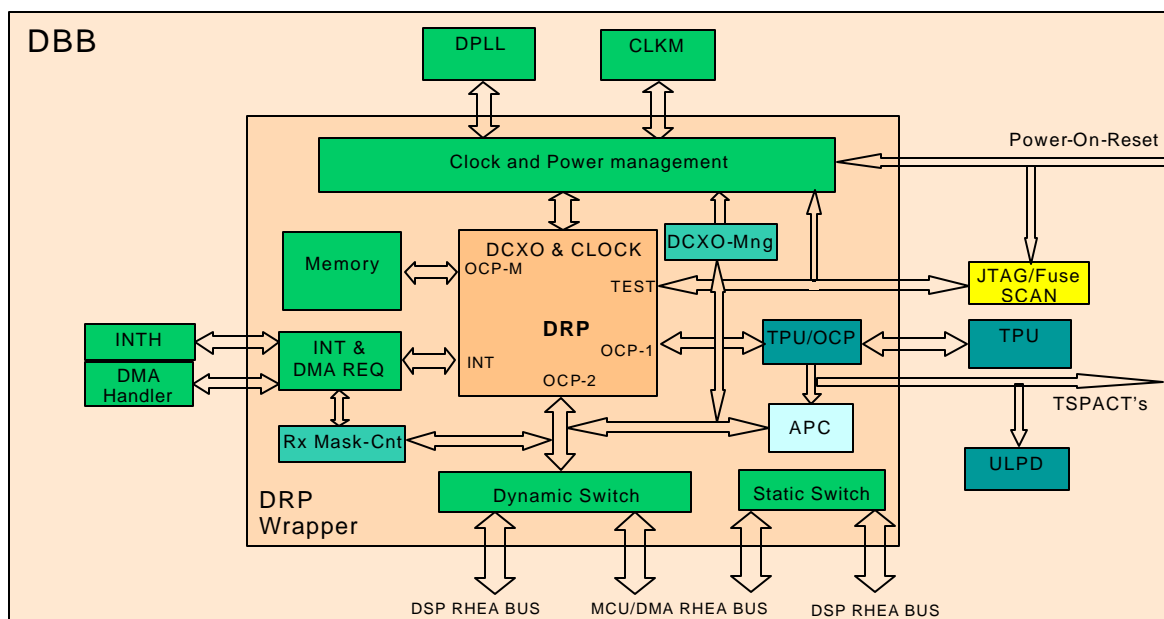


Figure 4: DRP Wrapper Block Diagram

3. Operating Conditions

LoCosto-IC operating conditions are mainly fixed from the **1218C027 manufacturing process** and the external system inter-connection requirement.

The 1218C027 process (optimized for 1.8v LVCMOS I/O's operation), using 5 layers of second-generation dual-damascene process (copper with low-K dielectric), combined with a 1.05v, 1.2v and 1.3v core power supply and low-peak power dissipation, provides the performances, High-Density integration, and power management capabilities required for power-budgeted mobile equipment.

System inter-connect requirement:

- ?? All Chip I/O's (except USIM, Reset, DRP & APC I/Os) are standard 1.8V LVCMOS Level-Shifter cell to accommodate the dual-supply-voltage requirements (VDD-DBB / VDD-IO or VDD-MIF).
- ?? All Input cells (Receiver & driver/Receiver) have input hysteresis; these cells are less sensitive to noise and accept slow input transition times.
- ?? I/O Frequency-class is selected accordingly with interface speed's and based on an external load of 50pf (e.g. High-Frequency class -C/D- is used for supporting external memory access targeted @52Mhz /50pf...)
- ?? USIM I/O's are TI tactical-cell's supporting 3V voltage thanks to DeMOS structure and PBIAS reference voltage implementation
- ?? Reset input (On_nOFF) is also a TI tactical-cell; fail-safe input tolerant up to 3V (DeMOS switch input). This cell has a specific power domain (VDD-RST) which is connected to the VDD-DBB voltage
- ?? LoCosto SOC owns 10 power domains
 - ?? DBB Core
 - ?? Memory I/O Bus
 - ?? Reset Input Cell
 - ?? USIM I/O Bus
 - ?? I/O's (all other)
 - ?? 2 x DRP Domains (VR1 & VR2 with specifics VSS lines)
 - ?? DPLL Sub-chip (isolated VSS, shared with APLL)
 - ?? APLL Sub-chip (isolated VSS, shared with DPLL)
 - ?? APC module (isolated VSS)

Important notice:

- ?? Tactical I/O Cells are necessary for compliance with function such as I2C (fail-save Open-Drain), USIM (3V support), Reset-Input (fail-safe)
 - ?? DRP2.0 Sub-Chip includes RF Analog-I/O's;
 - ?? The high-voltage protection (DeMOS) for supplying the DRP2.0 (VR1 & VR2 ~2.8V) is implemented within the Sub-Chip, which is ready to receive pre-regulated voltage.
-

- ?? APC (DRP Wrapper) is also high-voltage protected and ready for supporting a 2.8V voltage (VDD-APC; same source as DRP's VR1)
- ?? APC-OUTput is an analog output supplied from VDD-APC
- ?? P-BIAS implementation (See Neptune Chip) may require an additional pad as a backup solution

DBB Parameter values listed here after are extracted from the “**GS50 Specification and Design Information**” (cf document [6]), which should be consulted for detailed parameters description and further recommendations. The Electrical Characteristics are targeted values and should be consolidated design & engineering characterization.

3.1 Absolute Maximum Conditions

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Parameter		Maximum Range	Unit
V _{DD} Core-cell's steady-state value		-0.5 to 1.7	V
Storage-temperature range, T _{stg}		-65 to 150	°C
Clamp current for a receiver or driver		±20	mA
V _{DD} I/O-cell's steady-state supply voltage (1.8V I/O cells)		-0.5 to 2.5	V
V _{I/O} steady-state input or output voltage (@Die's Pad)		-0.5 to V _{DD} I/O + 0.5	V
Electrostatic discharge (ESD)	Human Body Model	2000	V
	Charged Device Model	500	V

Table 1: Absolute maximum ratings over operating junction temperature range

Stresses beyond those listed under “**Absolute maximum ratings**” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “**Recommended operating conditions**” is not implied.

3.2 Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
T _A (Industrial)	Operating Free-air temperature	-40	-	85	°C
T _J (Industrial)	Operating Junction temperature	-40	-	125	°C
VDD-I/Os	I/O cells Supply Voltage	1.71	1.8	1.89	V
VDD-MIF	Memory I/F I/O cells Supply Voltage	1.71	1.8	1.89	V
VDD-RST	Input reset-cell Supply Voltage	1.0	1.3	1.89	V
VDD-USIM	SIM-Card I/O-cell's Supply Voltage	2.7	2.85	2.95	V
VDD-RFV1	DRP-VR1 Supply Voltage	2.7	2.85	2.95	V
VDD-RFV2	DRP-VR2 Supply Voltage	2.7	2.85	2.95	V
VDD-APC	APC Supply Voltage	2.7	2.85	2.95	V
VPP	eFuse Power (Reserved for TI engineering, connected to VDD-DBB in functional mode)	-	-	2.00	V
VDD-DBB	DBB-Core Active Supply Voltage	1.24	1.3	1.365	V
	DBB-Core Retention Supply Voltage	1.0	1.05	1.1	V
VDD-DPLL	DPLL Supply Voltage	1.24	1.3	1.365	V
VDD-APLL	APLL Supply Voltage	1.24	1.3	1.365	V
Vih-I/O	High-level input voltage	0.65 * VDD-I/O	-	VDD-I/O	V
Vil-I/O	Low-level input voltage	0	-	0.35 * VDD-I/O	V
Vih-USIM	High-level input voltage	0.65 * VDD-USIM	-	VDD-USIM	V
Vil-USIM	Low-level input voltage	0	-	0.35 * VDD-USIM	V
Vih-RST	High-level input voltage	0.65 * VDD-RST	-	3.00	V
Vil-RST	Low-level input voltage	0	-	0.35 * VDD-RST	V
Vih-I2C (SDA & SCL)	High-level input voltage	<i>tbd</i>	-	3.00	V
Vil-I2C (SDA & SCL)	Low-level input voltage	0	-	<i>tbd</i>	V
MCU-Frq	ARM Sub-System Frequency	-	-	104	MHz
cDSP-Frq	cDSP Sub-System Frequency	-	-	104	MHz
DCXO-Xtal	External Reference Crystal	-	26	-	MHz

Table 2: Recommended Operating Condition

Parameter	Description	Min	Typ	Max	Unit
Voh-I/O	High-level output voltage /rated current	VDD-I/O – 0.45	-		V
Voh-USIM	High-level output voltage /rated current	VDD-USIM – 0.45	-		V
Voh-RST	High-level output voltage /rated current	VDD-RST – 0.45	-		V
Vol	Low-level output voltage /rated current	-	-	0.45	V
Iol/Ioh	Rated output current	-	-	4	mA
Vol-I2C (SDA & SCL)	Low-level output voltage /3mA	-	-	0.4	V
Vhys-I2C	I2C Input hysteresis	-	-	<i>tbd</i>	mV
CpB-I2C (SDA & SCL)	I2C-Bus load supported	-	-	90	pF
Cpi-I2C (SDA & SCL)	I2C-I/O's capacitance	-	-	10	pF
Vhys	Input hysteresis	-	-	100	mV
I _L	Input leakage current (Input Only)	-	-	+/- 1	uA
I _{oz}	High-Z leakage current (I/O's)	-	-	+/- 20	uA
I _{pu}	Pull-Up current (V _{I/O} = 0V)	-	-100	-	uA
I _{pd}	Pull-Down current (V _{I/O} =VDD-I/O)	-	100	-	uA
ICC	Supply current; Operating Mode	-	<i>tbd</i>	-	mA
	Deep Sleep	-	-	<i>tbd</i>	uA
Vo-APC	Output voltage (maximum code)	-	2.1	-	V
Voff-APC	Offset voltage AUXAPC=0 APCOFF=0	-	100	-	mV
Voff_adj-APC	Offset voltage Adjustment	-	<i>tbd</i>	-	V
Voff_stp-APC	Offset voltage Adjustment Step	-	<i>tbd</i>	-	V
Zo_pwd-APC	Offset voltage Adjustment	-	-	150	?
Vo_pwd-APC	Offset voltage Adjustment Step	-	-	50	mV
CpL-13Mhz	13MHz line supported load	-	-	100	pF

Table 3: Electrical characteristics over recommended ranges of operating conditions

4. System Performances

4.1 I/F's Bandwidth summary

The following table summarizes the bandwidth achieved for each peripheral

I/F's	Internal Source Clock (MHz)	External Bus I/F				Internal Bus I/F	
		Data Width (bit)	Peak Bandwidth (Mbits/s)	Max Frequency (MHz)	Load @Max Fq (pF)	Data Width (Bit)	Max Frequency (MHz)
/SP (cDSP)	Slave	1	0.5	0.5	50	16	104
↳-Port/I2S	Slave(I2S) 13(DCXO)	1	3.072 13	3.072 13	50	16	52
MCSI	13(DCXO)	1	6	6	50	16	52
UART Mod UART Manuf UART IRDA	"Free-Clock" 13(DCXO) 52(ARM/2) 48(APLL)	1	0.1152 3.25 4	0.1152 3.25 4	50	16	52
USB	48(APLL)	1	12	12	50	16	52
I2C's	13(DCXO)	1	0.4	0.4	90	16	52
USIM	13(DCXO)	1	0.1	0.1	50	16	52
LCD	13(DCXO)	8	104	13	80	16	52
NAND-Flash	52(ARM/2)	8	208	26	80	32	52
SPI	"Free-Clock" 13(DCXO) 52(ARM/2) 48(APLL)	1	13 26 24	26	50	32	52
Camera //	48 (APLL) 52 (ARM/2)	8	384 416	48 52	80	32	52
Serial CCP	Slave	1	208	208	50	32	52
EMIFS	104(ARM)	16	832	52	80	32	52

Table 4: I/F's Bandwidth Summary

Important notices



Due to the Clock re-generation scheme, system clock may vary while in Rx/Tx mode; for instance ARM/2 can switch from 52/55Mhz. See section 7.3.1, Clock Management (DPLL & CLKM)

5. LoCosto-IC I/O signals

5.1 RF package-ball's

DRP2.0 External Interface & Powers		38 Balls
RXDCSP	RX DCS band differential input	2
RXDCSM		
RXPCSP	RX PCS band differential input	2
RXPCSM		
RXGSMP	RX GSM band differential input	2
RXGSMM		
RXEGSMP	RX E-GSM band differential input	2
RXEGSMM		
TXHB	TX high band output	1
TXLB	TX low band output	1
XTAL	DCXO crystal input	1
XANATST1	Bi-directional analog test pin	6 (corner reliability- ball that cannot be used for functional signals)
XANATST2		
XANATST3		
XANATST4		
XANATST5		
XANATST6		
VREF	bandgap voltage reference bypass cap connection (VREF dn VREF1 are shorted on PCB)	2
VREF1		
IREF	current reference resistor connection	1
VDDR1TX	Input supply for DRP2 analog circuits except DCXO and bandgap	2
VDDR1RX		
VDDR2	Input voltage for DCXO and bandgap	1
VDDA0	Output of LDO_A regulator; connect to filter capacitor	2
VDDA1		
VDDRF	Output of LDO_RF regulator; connect to filter capacitor	2
VDDRF1		
VDDX	Output of LDO_DCXO regulator; connect to filter capacitor	1
VSSA0		
VSSA1	LNA and PPA grounds	4
VSSRF1		
VSSRF2		
VSSRF3		
VSSRF4		
VSSX	DCXO ground	1
VDDOSC	Output of LDO_OSC regulator; connect to filter capacitor	1
VSSOSC0		
VSSOSC1		

Table 5: DRP2.0 package ball

APC External Interface & Powers		5 Balls
VDD-APC	APC 2.8V Input Source voltage	1
VSS-APC	APC dedicated ground	1
APC-LDO	LDO Filter	1
APC-REF	Reference voltage filter	1
APC-OUT	APC output	1

Table 6: APC package ball

5.2 DBB package ball's

The pin's functions that are multiplexed at the chip's pad level (I/O mux's plus configuration control registers implementation) are **highlighted** whereas multi-mode pin controlled from the inside of a module function is not (i.e. ND_CE1 /NAND-FLASH CONTROL /F...). Alls pulls have an enable/disable control within the Chip-Configuration control registers.

The tables here below are the pin's functional requirement only.

ARM Memory Interface: 37 pins (10 multi-mode), VDD-MIF Power Domain			Pull	Reset
ADD/DATA(15:0)	IN/OUT	ARM/DMA mux'ed Address/Data bus		0x0000
ADD(20:16)	OUT	ARM/DMA address bus		0x00
ADD21/GPIO(6)	IN/OUT	ADD21 (default) configurable as GPIO	Down	0 (pull disabled)
GPIO(39)/ADD22 / ND_DT0	IN/OUT	GPIO (default) configurable as ADD22 or Nand-Flash data-Bus 0	Down	Input Low
GPIO(37)/ADD23 / ND_DT1	IN/OUT	GPIO (default) configurable as ADD23 or Nand-Flash data-Bus 1	Down	Input Low
nCS0/GPIO(38)/ LT1 / TSPACT7 / ND_DT0	IN/OUT	chip-select 0 (default); active low. Configurable as GPIO or LT1 (PWM) or TSPACT7 or Nand-Flash data-Bus 0	Up	1 (pull disabled)
GPIO(32)/ nCS1 ND_DT2	IN/OUT	GPIO (default) configurable as nCS1 or Nand-Flash data-Bus 2	Up	Input High
GPIO(35)/ nCS2 ND_DT3	IN/OUT	GPIO (default) configurable as nCS2 or Nand-Flash data-Bus 3	Up	Input High
nCS3	OUT	chip-select 3 active low.		1
RnW	OUT	Memory read (high) / write (low) control		1
nBHE	OUT	High Byte Enable; active low.		0
nBLE	OUT	Low Byte Enable; active low.		0
nMOE	OUT	Memory output enable; active low		1
GPIO(7) / nFWP / LT1/ TSPACT7/ ND_DT2 / CAM_DT2[TU12]	IN/OUT	GPIO (default) configurable as Flash Write Protect command; active low. or LT1 (PWM) or TSPACT7 or Nand-Flash data-Bus 2 or Parallel-Cam data-Bus 2	Down	Input Low
FDP	OUT	Flash deep low-power; active high		0
nRDYM/GPIO(40)	IN	External devices wait assertion (default); active low or configurable as GPIO	Up	Input Float (pull disabled)
ADV/GPIO(41)	IN/OUT	Address valid signal for Synchronous Burt memory control (default); active low or configurable as GPIO	Up	1 (pull disabled)
GPIO(42)/CKM	IN/OUT	GPIO (default) or Clock signal for Synchronous burst memory control	Up	Input High

Table 7: External Memory Interface package ball

Note:

In addition to GPIO capability, ADD22/nCS0, ADD23, nFWP/nCS1, nCS2 can be configured as Nand-Flash Data Bus (ND_DT0 to ND_DT3 respectively) in complement of ND_nWP/ND_DT4, LT/ND_DT5, BU/ND_DT6 SPIEN_2/ND_DT7.

NAND-Flash Control I/F: 7 pins (6 multi-mode), VDD-IOs Power Domain			Pull	Reset
ND_CE1	OUT	NandFlash Chip enable or General purpose output		1
ND_nWP/ ND_DT4/ CAM_DT4[TU13]	IN/OUT	Write protect or General purpose output or Nand-Flash data-Bus 4 or Parallel Cam data bus 4		0
GPIO(18)/ND_W E	IN/OUT	GPIO (default) configurable as N-F Write Enable	Up	Input High
GPIO(31)/ND_R E	IN/OUT	GPIO (default) configurable as N-F Read Enable	Up	Input High
GPIO(32)/ND_C LE	IN/OUT	GPIO (default) configurable as N-F Command Latch Enable	Down	Input Low
GPIO(33)/ND_A LE	IN/OUT	GPIO (default) configurable as N-F Address Latch Enable	Down	Input Low
GPIO(34)/ND_R nB	IN/OUT	GPIO (default) configurable as N-F Ready/Busy	Up	Input High

Table 8: NandFlash I/F, Control signals package ball

Note:

The Nand-Flash Data Bus (in/out) is multiplexed with the 8-Bit LCD or Parallel-Camera[TU14] Data bus. In addition, ND_nWP can be re-assigned to Parallel-Camera data bus 4 [TU15] or to Nand-Flash data bus (ND_DT4) in complement of ADD22/nCS0(ND_DT0), ADD23(ND_DT1), nFWP/nCS1(ND_DT2), nCS2(ND_DT3) & LT(ND_DT5), BU(ND_DT6) SPIEN_2(ND_DT7).

The ND_DT3 functionality is also available via the Parallel-Cam control signals (CAM_HS or CAM_VS or CAM_XCK)[TU16]

The Bus allocation switch as well as pin/ball selections are performed via the Chip-Configuration control register.

The Nand-Flash data bus, from the on chip controller, is output and drives all 0 at reset

Bolded pin can be dynamically controlled

Nd Flash Dispatched 8-bit Bus	Nd Flash 8-bit Bus	Nd-Flash Shared 8-bit Bus
GPIO(39) / ADD22	ND_DT0	LCD / CAM DT0
nCS0 / GPIO(38) / LT1 / TSPACT7		
GPIO(37) / ADD23	ND_DT1	LCD / CAM DT1
GPIO(36) / nCS1		

GPIO(7) / nFWP / LT1 / TSPACT7 / CAM_D2	ND_DT2	LCD / CAM DT2
GPIO(20) / CAM_VS / CKN / CAM_DT3	ND_DT3	LCD / CAM DT3
GPIO(19) / CAM_HS / CKP / CAM_DT3		
GPIO(22) / CAM_XCK / DTN / CAM_DT3		
ND_nWP / CAM_D4	ND_DT4	LCD / CAM DT4
GPIO(30) / LT3 / CAM_D5	ND_DT5	LCD / CAM DT5
GPIO(29) / BU / CAM_D6	ND_DT6	LCD / CAM DT6
GPIO(28) / SPIEN_2 / CAM_D7	ND_DT7	LCD / CAM DT7

Table 9: Nand Flash I/F, Mux'ing Summary[TU17]

LCD Interface: 14 pins (5 multi-mode) VDD-IOs Power Domain			Pull	Reset
LCD/CAM[TU18]/ ND_DT (7:0)	IN/OUT	LCD Data-bus (default) configurable as 8-bit Camera-Data bus or		Drive 0
GPIO(17)/LCD_ nCS1	IN/OUT	GPIO (default) configurable as LCD Controller chip-select's.	Up	Input High
GPIO(13)/LCD_ nCS0	IN/OUT	GPIO (default) configurable as LCD Controller chip-select's.	Up	Input High
LCD_RS/GPIO(16)	IN/OUT	LCD data/control selection (default) configurable as GPIO	Up	0 (pull disabled)
LCD_RnW/GPIO (15)	IN/OUT	LCD Read/Write (default) configurable as GPIO	Up	0 (pull disabled)
LCD_STB/GPIO (14)	IN/OUT	LCD Strobe Enable (default) configurable as GPIO	Up	0 (pull disabled)
LCD_nRst	OUT	LCD Controller dedicated reset or General-purpose output.		0

Table 10: LCD I/F package ball

Note:

The 8-Bit data bus is shared with the LCD, the Nand-Flash and the Parallel-Camera function[TU19]. The Bus selection switch can be performed dynamically via the Chip-Configuration control register.

At reset the LCD data bus is selected and output a low level on the package pin LCD/ND/CAM[TU20] bus.

Camera-Core Control I/F: 4 multi-mode pins, VDD-IOs Power Domain			Pull	Reset
GPIO(19)/CAM_HS/ CKP / ND_DT3 / CAM_DT3	IN/OUT	GPIO (default), configurable as Camera Horizontal Synchronization or serial CCP_CKP (LVDS pad) or Nand-Flash data bus 3 or Parallel Cam data bus 3		Input Float
GPIO(20)/CAM_VS/ CKN ND_DT3 / CAM_DT3	IN/OUT	GPIO (default), configurable as Camera Vertical Synchronization or serial CCP_CKN (LVDS pad) or Nand-Flash data bus 3 or Parallel Cam data bus 3		Input Float
GPIO(21)/CAM_LCK/DTP	IN/OUT	GPIO (default), configurable as Camera Image data latch clock or serial CCP_DTP (LVDS pad)		Input Float
GPIO(22)/CAM_XCK/ DTN / ND_DT3 /CAM_DT3	IN/OUT	GPIO (default), configurable as Camera Output Clock or serial CCP_DTN (LVDS pad) or Nand-Flash data bus 3 or Parallel Cam data bus 3		Input Float

Table 11: Camera I/F, Control/Serial-CCP package ball[TU21]

Note:

The parallel-camera 8-Bit Input data bus is multiplexed with LCD and Nand-Flash data-busses; LCD, Camera or Nand-Flash bus can be dynamically selected by S/W. the clock and synchronization control signals are multiplexed with the Serial Camera Port. In addition, 8-Bit parallel data can be statically re-assigned as shown in the following table [TU22]

Bolded pin can be dynamically controlled

Cam Dispatched 8-bit Bus	Cam 8-bit Bus	Cam Shared 8-bit Bus
GPIO(47) / DSR_RXIR	CAM_DT0	LCD / ND DT0
GPIO(0) / DCD_TXIR	CAM_DT1	LCD / ND DT1
GPIO(7) / nFWP / LT1 / TSPACT7 / ND_D2	CAM_DT2	LCD / ND DT2
GPIO(20) / CAM_VS / CKN / ND_DT3	CAM_DT3	LCD / ND DT3
GPIO(19) / CAM_HS / CKP / ND_DT3		
GPIO(22) / CAM_XCK / DTN / ND_DT3		
ND_nWP / ND_D4	CAM_DT4	LCD / ND DT4
GPIO(30) / LT3 / ND_D5	CAM_DT5	LCD / ND DT5
GPIO(29) / BU / ND_D6	CAM_DT6	LCD / ND DT6
GPIO(28) / SPIEN_2 / ND_D7	CAM_DT7	LCD / ND DT7

Table 12: Parallel Camera I/F, Mux'ing Summary[TU23]

The pin/ball configuration is selected within the Chip-Configuration control register. The parallel-camera data bus from on-chip camera controller is Input floating at reset.[TU24]

Reset Control (TriTOn I/F): 1 single-mode pin, VDD-RST Power Domain			Pull	Reset
ON-nOFF	IN	Power-On Reset signal; Start the power, clock & reset sequencing. Low: reset state, High: active state		Input Float

Table 13: SOC Reset input package ball

Power & Clocks (TriTOn I/F): 4 single-mode pins, VDD-IOs Power Domain			Pull	Reset
CKin-32KHz	IN	32 KHz input square wave clock signal.		Input Float
CK13MHz-En	IN	Enable 13MHz System Clock generation from 26MHz DCXO for LoCosto Internal &/ External use. Active high		Input Float
CKout-13MHz	OUT	13MHz System Clock; Available after CK13MHz-En has been activated and depending on programmed sequence		0
Wake-Up-Req	OUT	Indicates a Sleep/Wake-up condition requesting to TriTOn for proper power setting and clock activity. Active Mode: High, Deep-Sleep Mode: Low		0

Table 14: Power & Clock management I/F package ball

Note:

The 13MHz System-Clock output buffer is sized to support several external components (100 pF)

MCU Interrupt (TriTOn I/F): 1 single-mode pin, VDD-IOs Power Domain			Pull	Reset
ABB_IRQ	IN	External interrupt from ABB	Up	Input High

Table 15: Analog BaseBand Interrupt package ball

TPU Port (TriTOn & RF I/F): 6 pins (1 multi-mode), VDD-IOs Power Domain			Pull	Reset
TSPACT(11-15)	OUT	RF Front-End control /GSM Qbit Synchronous signal		0
GPIO(5)/TSPAC T8	IN/OUT	GPIO (default) configurable as TriTOn's ADC control signal	Down	Input Low

Table 16: GSM-Qbit timed event signals package ball

Note:

Additional TSPACT (7, 9&10) are available mux'ed with nFWP (Mem I/F), CDI (C-Port) & LPG (PWM) respectively. The pin/ball configuration is selected within the Chip-Configuration control register

KeyBoard Interface: 10 pins (2 multi-mode), VDD-IOs Power Domain			Pull	Reset
KBC(3:0)	OUT	Keyboard matrix 4column access.		0x0F
KBR(3:0)	IN	Keyboard matrix 4 row access.	Up	Input High
KBC(4)/GPIO(9)	IN/OUT	Keyboard matrix 5Th column access (default) configurable as GPIO.	Up	1 (pull disabled)
KBR(4)/GPIO(8)	IN/OUT	Keyboard matrix 5Th row access. (default) configurable as GPIO.	Up	Input High

Table 17: Keyboard I/F package ball

PWM's output: 5 multi-mode pins, VDD-IOs Power Domain			Pull	Reset
GPIO(12)/LPG /TSPACT10	IN/OUT	GPIO (Default) configurable as Light pulse Generator LED control signal or TSPACT10	Down	Input Low
GPIO(28)/BU/ ND_DT6/ CAM_DT6	IN/OUT	GPIO (Default) configurable as PWM output signal (Buzzer...) or NandFlash Data Bus bit6 or Parallel Cam data bus 6	Down	Input Low
GPIO(30)/LT3/ ND_DT5/ CAM_DT5	IN/OUT	GPIO (Default) configurable as LT3 (PWM) output signal (Light...) or NandFlash Data Bus bit5. or Parallel Cam data bus 5	Down	Input Low
GPIO(1)/PWT	IN/OUT	GPIO (Default) configurable as Pulse Width modulated signal (vibrator...)	Down	Input Low
GPIO(2)/PWL/ PCM_CK	IN/OUT	GPIO (Default) configurable as Pulse Width modulated (camera optics...) or PCM input Clock	Down	Input Low

Table 18: GPIO/PWM signal's package ball^[TU25]

Notes:

In addition to GPIO & PWM capability, LT3 & BU can be configured

- As Nand-Flash Data Bus (ND_DT5 & ND_DT6 respectively) in complement of ADD22/nCS0, ADD23, nFWP/nCS1, nCS2 (ND_DT0 to ND_DT3 respectively) & ND_nWP (ND_DT4), SPIEN_2(ND_DT7)...

See **Table 9**

- As Camera data bus (CAM_DT5 & CAM_DT6 respectively) in complement of DSR_RXIR (CAM_DT0), DCD_TXIR (CAM_DT1), nFWP (CAM_DT2), CAM_VS/CAM_HS/CAM_XCK (CAM_DT3), ND_nWP (CAM_DT4) & SPIEN_2(CAM_DT7)... See **Table 12**^[TU26]

The PCM_CK input signal is intended to supply the C-PORT Master configuration in replacement of the internal 13Mhz sources

The pin/ball selections are performed via the Chip-Configuration control register

MCU & DSP I ² C: 2 single-mode pins, Fails-safe Input, Open Drain output			Pull	Reset
SCL_TriTon	IN/OUT	I2C interface Master serial clock reserved for TriTon Control		Input Float
SDA_TriTon	IN/OUT	I2C interface Serial bi-directional data reserved for TriTon Control		Input Float

Table 19: I2C I/F package ball

Note:

This I2C interface is reserved for TriTon ABB control.

MCU App I ² C: 2 single-mode pins, Fails-safe Input, Open Drain output			Pull	Reset
SCL	IN/OUT	I2C interface Master serial clock		Input Float
SDA	IN/OUT	I2C interface Serial bi-directional data		Input Float

Table 20: I2C I/F package ball

Serial Port Interface: 7 multi-mode pins, VDD-IOs Power Domain			Pull	Reset
GPIO(25)/SPI_S IMO	IN/OUT	GPIO (Default) configurable as SPI Slave Input Master Output Data	Down	Input Low
GPIO(24)/SPI_S OMI	IN/OUT	GPIO (Default) configurable as SPI Slave Output Master Input Data	Down	Input Low
GPIO(23)/SPI_C LKI	IN/OUT	GPIO (Default) configurable as SPI Clock	Down	Input Low
GPIO(26)/SPIEN_0	IN/OUT	GPIO (Default) configurable as SPI's Chip-Enable	Down	Input Low
GPIO(27)/SPIEN_1	IN/OUT	GPIO (Default) configurable as SPI's Chip-Enable	Up	Input High
GPIO(28)/SPIEN_2/ND_DT7/CA M_DT7[TU27]	IN/OUT	GPIO (Default) configurable as SPI's Chip-Enable or Nand-Flash Data Bus bit7 or Parallel Cam data bus 7	Up	Input High

Table 21: Serial Peripheral I/F package ball

Note:

In addition to GPIO capability, SPIEN_2 can be configured as Nand-Flash Data Bus (ND_DT7) or Parallel Cam data bus (CAM_DT7)[TU28])... See **Table 9** & **Table 12**

The pin/ball selections are performed via the Chip-Configuration control register

USIM CARD: 4 single-mode pins, VDD-USIM Power Domain			Pull	Reset
USIM_RST	OUT	Card Reset		0
USIM_IO	IN/OUT	Card I/O Data		0
USIM_CLK	OUT	Card Reference Clock		0

USIM_PW_CTL	OUT	Pull-Up power control		0
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Table 22: USIM I/F package ball

MCU USB I/F: 4 multi-mode pins, VDD-IOs Power Domain			Pull	Reset
USB_RCV/ UART_CTS	IN	USB Differential Receiver input (default); not used in 3 pins DAT_SE0 mode. Or configurable as UART CTS control		Input Float
USB_SE0/ UART_TX	IN/OUT	USB function (default) - USB SE0 in 3 pins bi-dir DAT_SE0 mode - VM function in 4 pins bi-dir VP_VM mode Or configurable as UART transmit pin function		Input Float
USB_DAT/ UART_RX	IN/OUT	USB function (default) - DAT function in 3 pins bi-dir DAT_SE0 mode - VP function in 4 pins bi-dir VP_VM mode Or configurable as UART receive pin function		Input Float
USB_TXEN/ UART_RTS	OUT	USB Transmit Enable (default) Or configurable as UART RTS control		0

Table 23: USB I/F package ball

Note:

The UART signals are multiplexed to be available at the USB ball's. The pin/ball configuration is selected within the Chip-Configuration control register

CODEC Audio (TriTOn I/F): 4 pins (1 multi-mode), VDD-IOs Power Domain			Pull	Reset
CSYNC	IN/OUT	CODEC frame synchro interface	Down	Input Low
CSCLK	IN/OUT	CODEC serial clock interface	Down	Input Low
GPIO(4)/CDI/LT 2/TSPACT9	IN/OUT	GPIO (Default) configurable as CODEC serial data input interface or LT2 (PWM) or TSPACT9	Up	Input High
CDO	OUT	CODEC serial data output interface with Hz capability		0

Table 24: C-Port/I2S package ball

Note:

CSYNC & CSCLK received from external master can be forwarded to the MCSI Port, CDO output from C-PORT can be routed to the MCSI_TX pin; this allows having an output data flow available on the MCSI Port still controlled from an external master CoDec device (TriTOn).

UART MODEM/IRDA: 6 pins (3 multi-mode), VDD-IOs Power Domain			Pull	Reset
TX	OUT	Transmit Data.		1
RX	IN	Receive Data.		Input Float
CTS	IN	Clear To Send.		Input Float
RTS_SDIRDA	OUT	Request To Send, configurable as IRDA transceiver Shut Down mode.		1
GPIO(47)/DSR_RXIR	IN/OUT	GPIO (Default) configurable as Data Set Ready, or as Infra-Red receive pulse.	Up	Input High
GPIO(0)/DCD_TXIR	IN/OUT	GPIO (Default) configurable as Data Carrier Detect, or as Infra-Red transmit pulse.	Up	Input High

Table 25: UART I/F package ball

DSP MCSI (BlueTooth voice): 4 multi-mode pins, VDD-IOs Power Domain			Pull	Reset
GPIO(43)/MCSI_CK/CSCLK	IN/OUT	GPIO (Default) configurable as MCSI Bit synchronization clock or as C-PORT external forward clock	Up	Input High
GPIO(44)/MCSI_FS/CSYNC	IN/OUT	GPIO (Default) configurable as MCSI Frame synchronization clock or as C-PORT external forward Channel Sync.	Up	Input High
GPIO(45)/MCSI_TX/CDO	IN/OUT	GPIO (Default) configurable as MCSI Transmit serial data or C-PORT data out	Up	Input High
GPIO(46)/MCSI_RX	IN/OUT	GPIO (Default) configurable as Receive serial data	Up	Input High

Table 26: Multi-Channel Serial I/F package ball

Note:

MCSI_CK & MCSI_FS can be mux'ed respectively with CSYNC & CSCLK as well as MCSI_TX that can be replaced by CDO; this configuration makes the component attached to the MCSI receiving the C-PORT data still flow controlled by the external Master-CoDec port (TriTon).

The pin/ball configuration is selected within the Chip-Configuration control register

DSP Voice (TriTon I/F): 4 single-mode pins, VDD-IOs Power Domain			Pull	Reset
VCLKRX	IN	Transmit/Receive clock.		Input Float
VDX	OUT	Transmit Data.		Drive Unknown
VDR	IN	Receive data.		Input Float
VFSRX	IN	Transmit/Receive Synchro.		Input Float

Table 27: Voice Port package ball

Device Test control: 2 single mode pins, VDD-IOs Power Domain			Pull	Reset
USB-Boot/GPIO(3)/LPG	IN/OUT	This pin is sensed during the system reset (ROM code controlled). Must be to a high level during the system-reset to enable the USB-Boot sequence; If sensed to a low level the Boot-code assumes an UART link is used for booting. After system-reset the pin can be re-configured as GPIO or LPG(PWM) function		Input Float

Table 28: System Boot configuration package ball

JTAG/Emulation Interface: 6 pins (2 multi-mode), VDD-IOs Power Domain			Pull	Reset
nBSCAN	IN	Test-Mode & Boundary-scan selection; Active low	Up	Input High
TDI	IN	Test Data Input.	Up	Input High
TDO	OUT	Test Data Output.		Drive Unknown
TMS	IN	Test Mode Select.	Up	Input High
TCK	IN	Test Clock.	Down	Input Low
nEMU0/GPIO(10)	IN/OUT	Emulation pin 0 (Default) configurable as GPIO.	Up	Input High
nEMU1/GPIO(11)	IN/OUT	Emulation pin 1 (Default) configurable as GPIO	Up	Input High

Table 29: JTAG Boudary,Test & Emulation signals package ball

5.3 Ball Count Summary^[TU29]

The (numbers in bracket) indicate **primary**/secondary GPIO functions multiplexed to each I/F's.

Interfaces:	# Balls
ARM Memory I-F Data / Address + Control	21 +6 (+6 +4) = 37
Nand Flash Control I/F	2 (+5) = 7
LCD / Nand / Camera data + LCD control I/F's	8 +1 (+2 +3) = 14
Camera Control / CCP I/F	(+4)
Reset, Power & Clocks System (to Triton)	5
ARM External Interrupt (to Triton)	1
TPU PORT (5 /RF Front-End + 1 /TriTon)	5 (+1) = 6
KEYBOARD	8 (+2) = 10
PWM's (BU, LT, LPG, PWM, PWT)	(+5)
I2C X 2	2 + 2 = 4
SERIAL PORT INTERFACE (SPI)	(+6)
SIM CARD INTERFACE	4
USB	4
AUDIO Stereo C-PORT	3 (+1) = 4
BLUETOOTH DATA INTERFACE / UART_IRDA	4 (+2) = 6
BLUETOOTH VOICE / DAI	(+4)
VOICE PORT	4
USB-Boot	(+1)
NBSCAN + JTAG + Emu's	1 + 5 (+2) = 8
DRP 's RF & power + 6 test corner-pins	35 + 6 = 41
APC (output, 1.8V LDO Filter, Vref, spare)	4
Un-used corner spares	2
Reserved pins[Double bonded nd_nwp]	1
Unconnected Balls	19
Sub-Total =	201
Powers & Grounds (DRP excluded):	
VDD-MIF	2
VDD-IOs	5
VDD-USIM	1
VDD-RST	1
VDD-PLL(APLL+DPLL)	1
VDD-DBB	8
VDD-APC	1
VDDX	1
PBIAS output	1
VSS-PBIAS	1
VSS-APC	1
VSS-PLL(APLL+DPLL)	1
SENSE	1
FORCE	1
VSS	12

VPP	2
Total =	241
Including <i>Primary</i> + Secondary GPIO's	36 + 12 = 48

5.4 GPIO's Distribution

The block diagram below shows the GPIO's distribution.

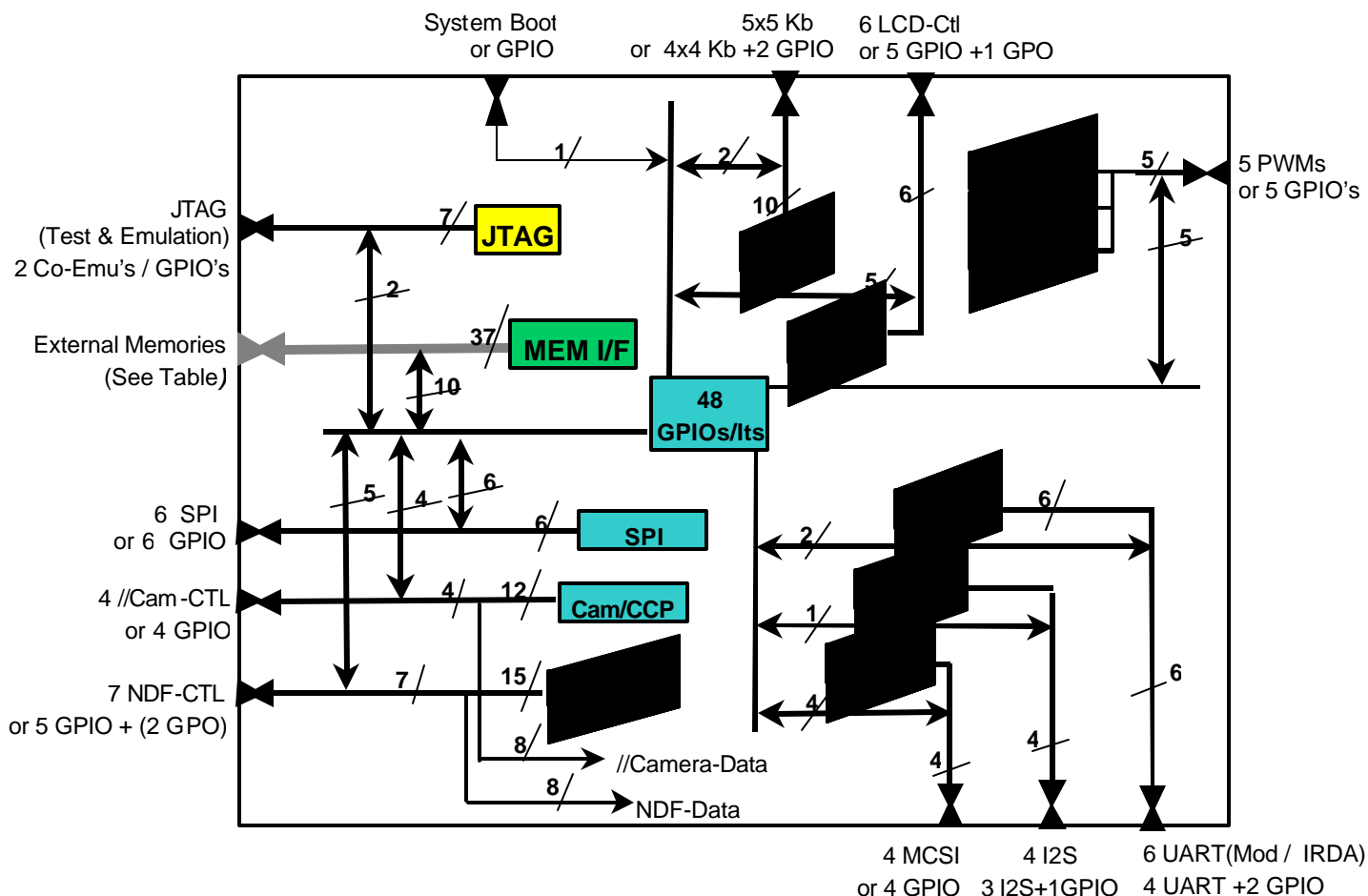


Figure 5: GPIO's Mux'ing diagram[TU30]

6. Chip manufacturability

Chip's test engineering as well as I/O 's Boundary Scan (PCB's test) is set by pulling "nBSCAN" pin to a low level. When the "nBSCAN" pin is high (on-chip pull-up) functional mode with emulation capability is set; emulation effective entry is defined from the "EMU" protected control bit (See section **7.4.5, *Secure Environment***)

The LoCosto-IC Test/Productization strategy is finalized @chip-Design level based on product engineering requirements.

6.1 TAP/JTAG Controller

LoCosto Test Access Port controller interfaces the standard IEEE JTAG serial protocol.

The chip integrates 5 x TAP/JTAG controllers to control respectively the LoCosto chip and the DRP2.0 Sub-Chip test hardware configurations, the Fuse-Farm controller, the ARM7TDMI MCU and the C54x DSP emulation's.

The JTAG Test Access Port (TAP) of the chip depending on "nBSCAN" pin value can be selected:

- ?? To access the 3 processors on-chip emulators with a pseudo IEEE JTAG protocol for emulation purposes. A PC or workstation can be connected to the interface to set the tri-emulation mode with the ARM core linked to DSP core, which in turn is linked to DRP. The IceCrusher module supports the synchronization between the 2 cores.
- ?? To dialog with embedded TAP/JTAG controller's, which instructions set is compliant with the IEEE 1149 standard for controlling Boundary Scan modes, Fuse-Farm activation, DRP's specific test configuration & the programming of the chip I/Os configuration (PMT modes, full-scan modes, memory-BIST modes...).

6.2 BIST Controller's

H/W BIST controller's are implemented for memories test; BIST can be set, activated & monitored either from JTAG or RHEA interfaces.

6.3 Fuse-Farm

The Fuse-Farm contains a Fuse ROM that is burnt at the Chip manufacturing level with all the relevant information (DIE -ID, Device ID, memory repair information, encryption keys etc...)
The Fuse-Farm is accessed via, its own TAP/JTAG controller.

At power-on reset, while the Chip is in a reset state, the Fuse-ROM data is serially shifted out (@32KHz) into the chained configuration related Read/Write-registers/memories. The LoCosto fuse-chain is defined during the Chip Design phase...

7. Digital Base Band System Description

7.1 Power-On-Reset

Power, Reset and clock sequencing is initiated from the ABB (TriTon) and managed via ULPD, eFUSE, DRP's wrapper and DRP2.

When the LoCosto Chip-Set system is turned-On, TRITON power-IC, launch the Power-On-Reset steps... (see Triton [2]);

After powers ramp-up, the 32 KHz clock is supplied to the DBB and the system reset (ON_nOFF) is released, allowing for starting the fuse-controller sequence. Then the clock request signal can be asserted however clock availability will rely on additional internal sequences. As soon as the fuse-controller has completed, internal DBB system reset is released enabling the ULPD, the DCXO-startup (wrapper) and DRP's DCXO modules to start their respective wake-up counter.

After the programmed time has elapsed, a 13 MHz system clock (26 MHz DCXO is divided in DRP CKM module) is enabled to the DBB part and supplies the DPLL that generates the processor clock's.

The Power-On-Reset sequencing and the subsequent clock generation is depicted in the following figure

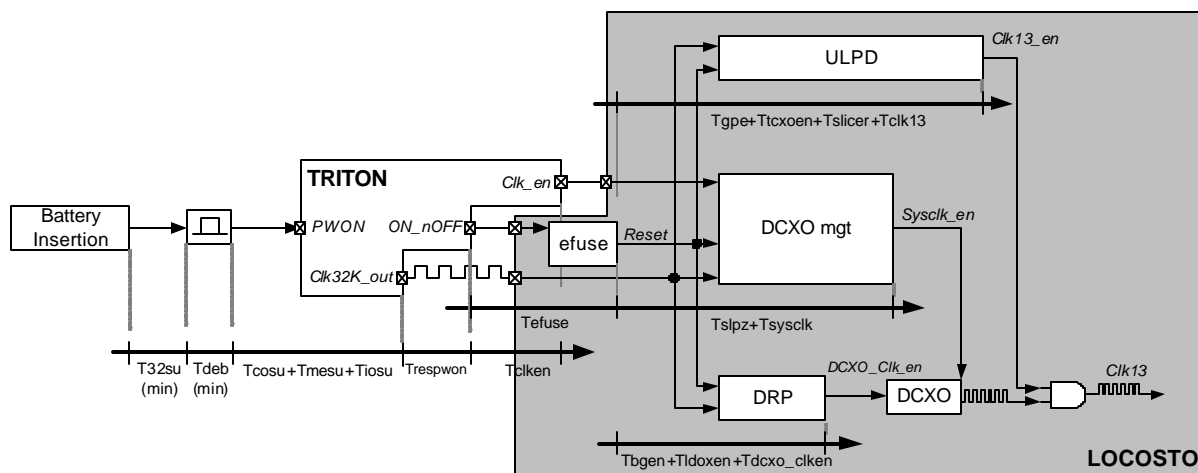


Figure 6 Power-on reset and clock generation

7.2 System-Boot

At reset the System can boot differently depending on programmed (eFuse) Die-ID's MSbit, "Man Pub Key" and "USB-Boot" pin values. The USB-Boot pin can be re-configured after firmware authentication.

- ?? Die-ID eFuse MSbit selects
 - ~~??~~ Protected device
 - ~~??~~ Non-Protected device
- ?? “Man Pub Key” for protected chip selects
 - ~~??~~ Internal secure-ROM boot
 - ~~??~~ External memory boot (still going through Internal ROM)
- ?? USB-Boot pin for protected Chip selects (Secure ROM code handling)
 - ~~??~~ Manufacturing boot for Flash download via USB link
 - ~~??~~ Manufacturing boot for Flash download via UART link

Based on the above definition, the following boot sequences can be entered

- ?? Non-Protected Device (TI-engineering reserved)
 - ~~??~~ Security unlocked; internal secure Boot-ROM disabled
 - ~~??~~ Boot on external nCS0 memory-space
 - ~~??~~ Chip emulation & Secure-environment emulation enabled
- ?? Protected Device (Man Pub Key ? 0)
 - ~~??~~ Boot on internal Secure Boot-ROM
 - ~~??~~ Boot link monitoring & control (USB or UART depending on USB-Boot pin setting)
 - ~~??~~ Certificate & Firmware authentication
 - ~~??~~ Chip-Emulation setting based on certificate parameter
 - ~~??~~ Firmware boots on nCS3 memory-space (Boot-ROM Secure code Handling)
 - ~~??~~ Secure-environment emulation disabled
- ?? Non-Protected Device (Man Pub Key = 0)
 - ~~??~~ Secure Boot disabled still booting on internal ROM
 - ~~??~~ Boot link monitoring & control (USB or UART depending on USB-Boot pin setting)
 - ~~??~~ Chip-Emulation enabled
 - ~~??~~ Firmware boots on nCS3 memory-space (Boot-ROM Secure code Handling)
 - ~~??~~ Secure-environment emulation enabled

7.3 S-O-C Control peripherals

S-O-C peripherals include functions that configure the whole LoCosto-IC. After system-Reset, the S-O-C setting, however, remains under host- processor (MCU) software control.

7.3.1 Clock Management (DPLL & CLKM)

The Clock-Management system consists of a Digital Phase Locked loop (DPLL) and dividers (CLKM) each associated to memory-mapped registers for programming DBB system clocks frequencies (DSP, MCU, Rhea-Bridge & Peripherals clocks).

In addition:

?? The CLKM includes circuitry that manages the reset of all modules controlled either by the MCU or the DSP.

?? The CLKM controls the memory low-power/Retention mode (See section 7.3.3)

The DPLL is programmable in "multiplication-mode" with the following values:

$$F_{out} = F_{in} \cdot \frac{m}{d} \quad m = 1 \text{ up-to } 32 \text{ (step } 1) \quad d = 1, 2, 3 \text{ or } 4$$

and in "division-Mode" with the following values:

$$F_{out} = \frac{F_{in}}{k} \quad k = 1, 2 \text{ or } 4$$

From the DPLL generated clocking signal, the CLKM module supplies clock and controls activity for the DSP, the MCU and the RHEA peripherals. The CLKM module supports the small and big-sleep modes with the disabling of the MCU system clock and the scheduling of the deep power of the external FLASH memory.

In the LoCosto-IC system, a 13 MHz DBB's source-clock is internally generated from the 26Mhz DCXO cell implemented in the DRP2.0 module; note that DCXO cell is a 1-pin oscillator hence connected through a capacitor to one 26Mhz-Crystal's node only.

The 13 MHz frequency is

?? Sourced to the CLKM and the DPLL, which generates the highest DBB system clock.

?? Internally propagated to the DBB Peripherals through the CLKM module

?? Available @package-pin level; Output Buffer is sized to support several external devices

Important notices

In order to reduce the digital switching noise, it is desirable to have all DBB clocking signal's, synchronous to the DRP's local oscillator (LO) clock. The DRP's CKM function includes a re-synchronization mechanism offering the capability for locking all DBB clock's on the LO clock edge. The diagram below shows the DBB/DRP clock path.

In order not compromising the 32KHz clock Gauging mechanism (See 7.4.3.2), The **NON-Retimed** clock generated by the DPLL (DPLL-Clock-out) is supplied to the ULPD as the High frequency calibration clock.

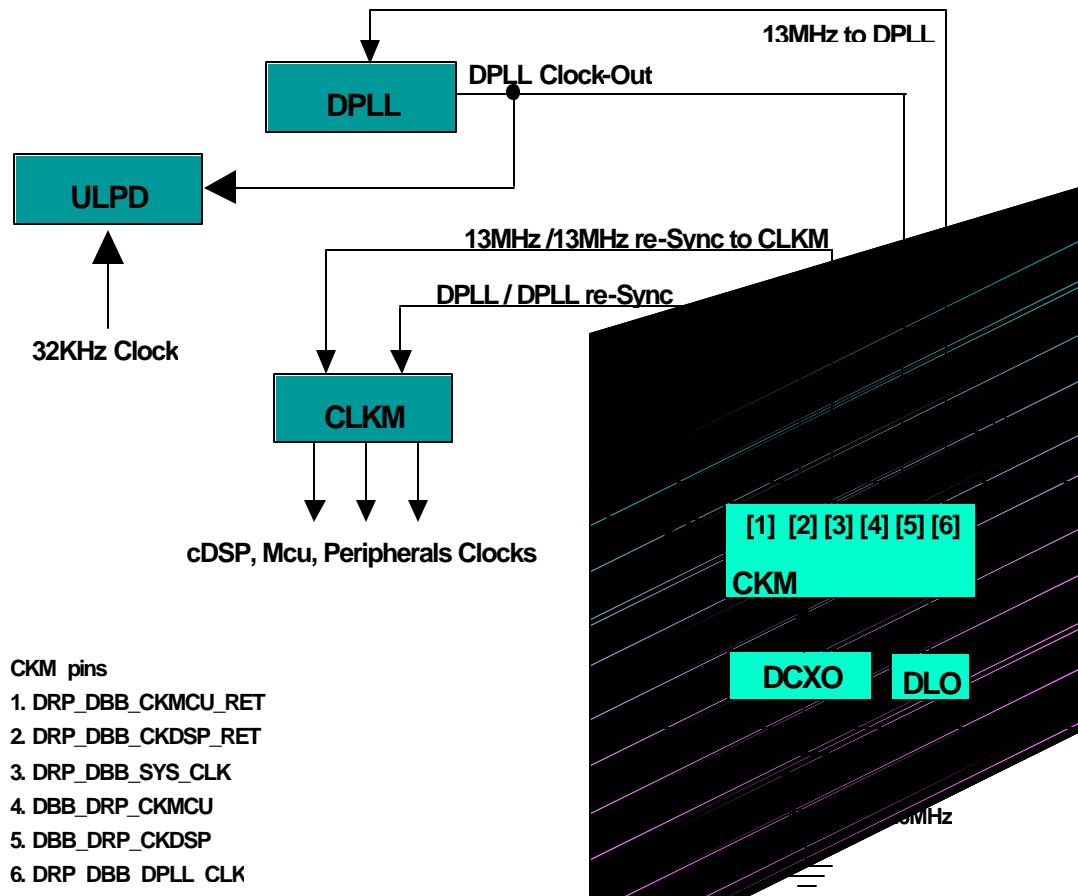


Figure 7: DBB / DRP clock path

The functional clock distribution within the DBB is summed up in the following diagram

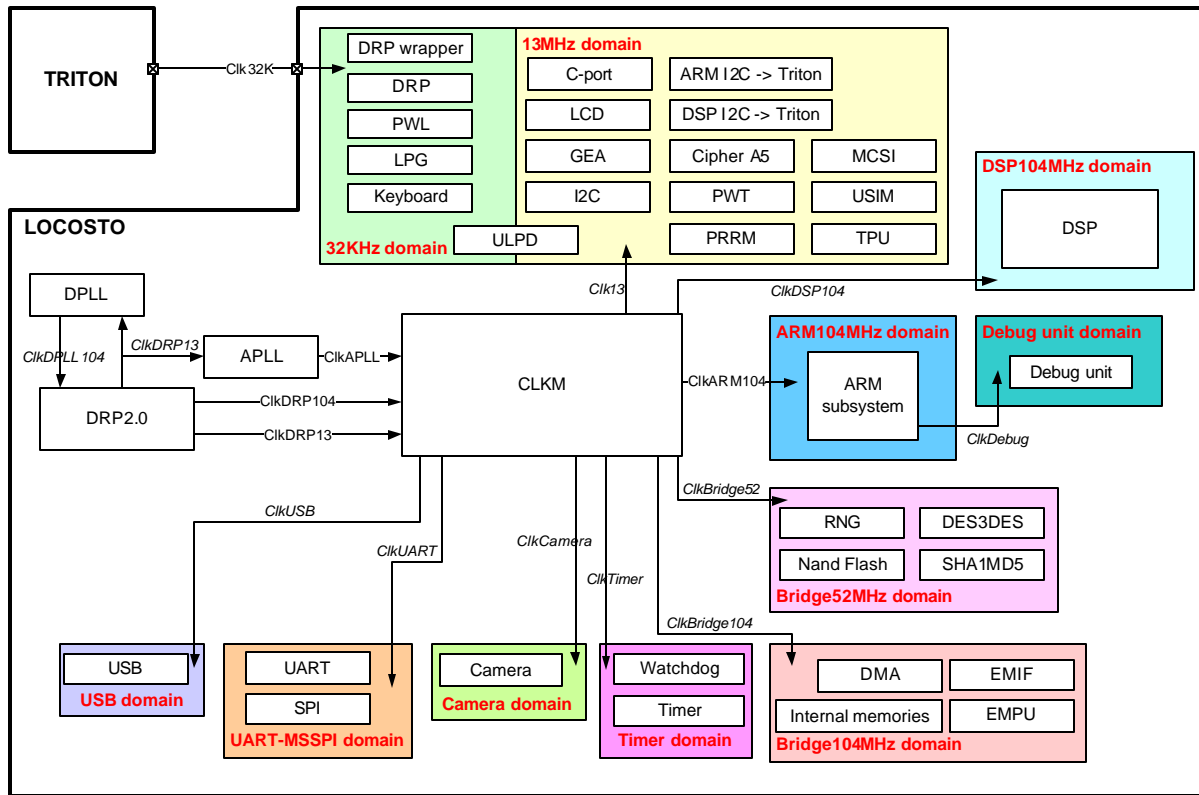


Figure 8 Functional Clock distribution in Locosto DBB

While in Tx or Rx, and as a result of the clock re-generation from the Local oscillator source, the DBB system clock frequency (MCU & DSP) can vary from 104.1 MHz to 110.4 MHz depending on the Rx/Tx channel.

As an example, the Figure below shows the maximum possible number of clock switches (re-generated / non re-generated) that can occur in a single frame (8 successive power measurements).

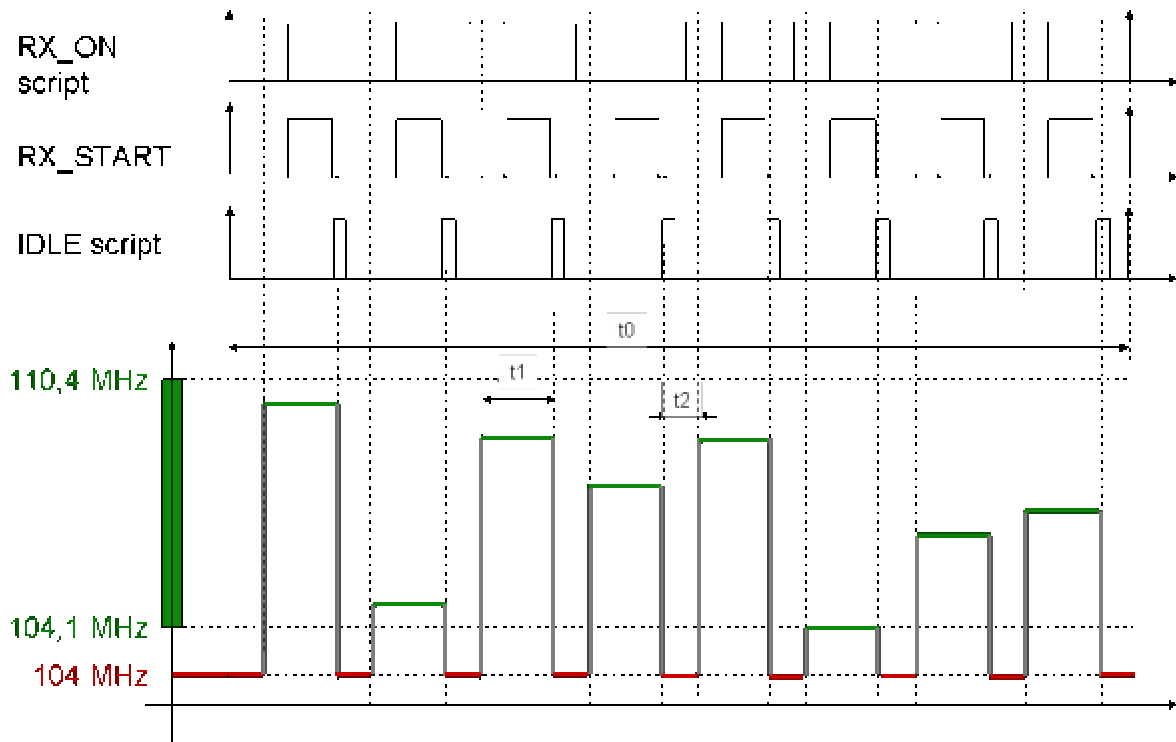


Figure 9: Re-generated/ Non Re-generated Clock switches

7.3.2 Chip Configuration registers (CONFIG)

S/W programmable registers, memory-mapped to the RHEA Bus, are used to (re)-configure the device hardware. The main functions considered are:

?? LoCosto-IC I/O's multi-mode configuration (see **DBB package ball's** section 5.2)

 I/O's mode selection (Multi-function I/O's, Test & debug...)

 Pull Up/Down enable control

?? ARM & cDSP Debug mode

- ?? ARM & cDSP S/W trace control
- ?? Memory Retention Mode control

7.3.3 Memory Retention/Leakage Management

The TI-ASIC GS50 technology offers memories (BRF/S, MVF...) that support a Low-Power/Retention mode by reducing leakage currents. LoCosto S-O-C has a hardware control to manage low-power feature.

In this mode the memory cannot be accessed, the memory-array voltage is dropped, reducing leakage currents and the memory is frozen in a static state still retaining its data content.

While in retention mode, a wakeup time is needed before the memory can be accessed.

This feature is control-able and can be turned off by software in the clock management Function (CLKM) that drives Retention Management logic block. The LoCosto S-O-C memories listed below take advantage of this feature

- ?? MCU 2.5M-bit SRAM
- ?? DSP DARAM, DSP API RAM, cDSP extension RAM, DRP Wrapper RAM

7.4 MCU sub-system

The μ -Controller sub-system is formed by:

- ?? The Computing entity
- ?? MCU' s system & GP peripherals
- ?? GSM dedicated peripherals
- ?? Connectivity peripherals
- ?? The secure resource/environment

7.4.1 μ -Controller computing unit & resources access

The μ -Controller's computing unit is based on an ARM7TDMIE processor combined with internal Static RAM and ROM memories. The internal memory size can be extended with external component interfaced via the external memory I/F, which manages memory adaptations (protocol, timing bus-width ...).

Peripherals control & status registers (RHEA & Memory-like) as well as ARM/cDSP communication RAM (API) are mapped within the ARM memory space; Peripherals and cDSP Sub-system accesses are achieved via the RHEA/Memory-like busses & API BRIDGE respectively.

7.4.1.1 MCU memory map

The ARM memory interface handles the program/data as well as control & status accesses with the out-of-chip and on-chip memories as well as memory-mapped resources. The memory space is divided to 5 busses. The figures below give an overview of the MCU memory space.

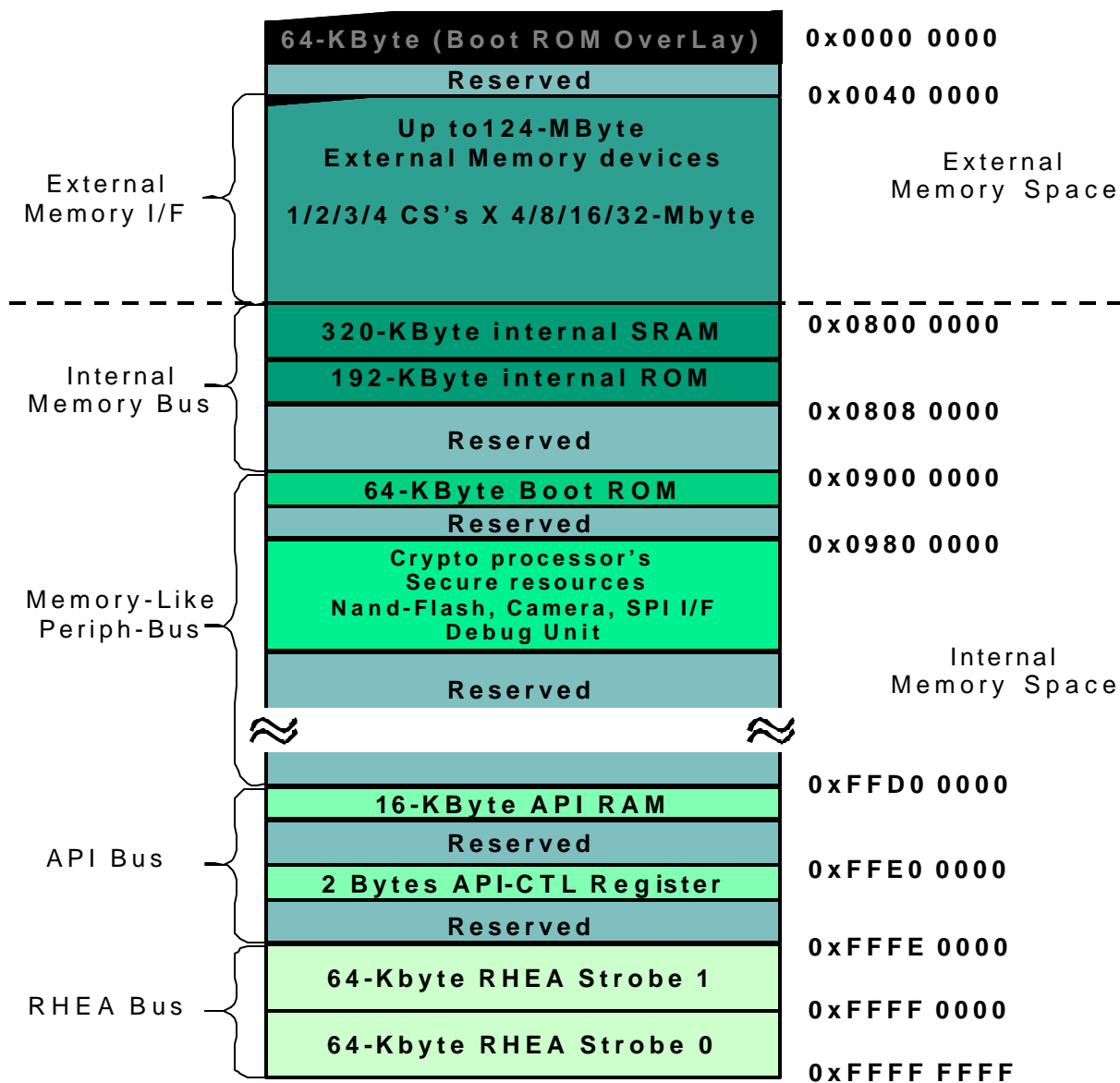


Figure 10: MCU Memory space organization

7.4.1.2 Asynchronous, synchronous-burst External Memory Interface (EMIF).

The asynchronous/synchronous External Memory Inter-Face (EMIF) supports most common memory interface protocols through a flexible programming and timing signals control.

The EMIF can control up to 4 memory devices for a total address range up to 124-Mbyte (1 x 28-Mbyte + 3 x 32M-byte), without any external adding logic. See *Figure 11: External Memory organization*

The number of memory Chip Select signal is configurable from 1 to 4 (default to 2 CS's) and the address bus width is sizable from 21-bit /2Mx16bit-word (32Mbit) to 24-bit /16Mx16bit-word (256 Mbit). Default setting @reset is 22-bit /4Mx16bit-word (64Mbit memory).

Each CS's address-space has dedicated Wait-State and/or Dummy-Cycle insertion configuration registers to fulfill protocol and timing constraints of attached memory devices. Elementary Wait-state and Dummy-cycle are referenced to the programmed clock mode on a chip-select(104 MHz, 52MHz...etc)

The list below summarizes the EMIF features.

- ?? Up to 124-Mbyte external memory
 - ~~??~~ 1/ **2(default)** / 3 / 4 CS's x 4 / **8(default)** / 16 / 32-Mbyte (CS0 limited to 28-Mbyte)
- ?? 16-bit little-endian word data-bus, with 8-bit & 32-bit word size adaptation
- ?? Each CS separately configurable for
 - ~~??~~ Asynchronous/burst single-access Read/Write (Default)
 - ?? Programmable Wait-State & Dummy-Cycle (104MHz granularity)
 - ~~??~~ Synchronous Burst Read/**Write**
 - ?? 1 or 4 x 8/16/32-bit word fixed burst
 - ?? Continuous mode
- ?? Asynchronous memory up to **60** ns access time & synchronous Burst clock up to 52Mhz
- ?? Asynchronous/Synchronous Memory WAIT/nREADY monitoring
- ?? Multiplexed address and data memory-devices without external adding logic. (Applies for synchronous and asynchronous access mode).
- ?? Programmable time-out counter for automatic access completion with interrupt and status logging on time-out events.
- ?? Dynamic local idle mode & IC deep power-down mode request synchronization.
- ?? Write protection mechanism
- ?? Data bus always driven (last data read/write driven back on the bus)
- ?? **External Memory Pre-Fetch Buffer**
 - ~~??~~ 2 lines 4 X 32-bit words (8 x 16-bit);
 - ~~??~~ 2 Cycles (@104MHz) CPU access, 24 cycles per line filling
 - ~~??~~ LRU replacement policy
 - ~~??~~ Code only, Support ARM (32) & Thumb (16) modes or Code & Data
 - ~~??~~ Wrap-Around support

In addition, the EMIFS is a multi-master memory interface that can be controlled from the CPU or the DMA. It supports flexible and programmable arbitration protocol:

- ?? LRU priority ordering or
- ?? MCU/DMA fixed highest priority (no burst interruption).

Example of supported Flash devices

?? SPANSION, S29NS016J

~~??~~ Mux'ed Add/Data

- o 1.8V Core & I/O's
- o 1 Meg x 16-bit

~~??~~ Asynchronous/Burst Single-access (70ns),

- o Synchronous-Burst; Cont or 8/16/32-word, WAIT synchronization, 87.5ns/13.5ns @54MHz
- o Read: 25mA, Program/Erase: 15/15mA, Standby: 9µA
- o Programming: 6µS/byte

?? ST, M58WR016Fx

- o Mux'ed Add/Data
- o 1.8V Core & I/O's
- o 1 Meg x 16-bit

~~??~~ Asynchronous/Burst Single-access (80ns),

- o Synchronous-Burst; Cont or 4/8/16-word, WAIT synchronization, 80ns/14.5ns @54MHz
- o Read: 20mA, Program/Erase: 15/20mA, Standby: 50µA
- o Programming: 4µS/byte

?? INTEL, 28F640L18

~~??~~ Non Mux'ed Add/Data (Add & Data bus connected together on PCB)

- o 1.8V Core & I/O's
- o 4 Meg x 16-bit
- o Synchronous-Burst; Cont or 4/8/16-word, WAIT synchronization, 85ns/14ns @54MHz
- o Read: 22mA, Program/Erase: 50/32mA, Standby: 25µA
- o Programming: 7µS/byte

?? INTEL-DANALI: 28F128W18TD-60-mux (128Mb, Mux'ed Add/Data)

?? AMD: AM29BDS643G-7M (64Mb, Mux'ed ADD/Data)

?? FUJITSU: MBM29PL12LM_10 (128Mb Mux'ed ADD/Data)

Example of supported RAM devices

?? MICRON, MT45W2MW16BFB CellularRAM (1.5) Memory

~~EE~~ **Non Mux'ed Add/Data (Add & Data bus connected together on PCB)**

~~EE~~ 1.8V Core & I/O's

~~EE~~ 2 Meg x 16-bit

~~EE~~ Asynchronous/Burst Single-access (70ns),

~~EE~~ Synchronous Read/Write Burst (Cont or 4/8/16-word, 39ns/6.5ns @104MHz Max

~~EE~~ Active-Max: < 25mA, Standby: 120µA, Deep Power-Down: <10µA

Example of supported Stacked Multi-Chip Product

?? SPANSION, S71NS064JA0

~~EE~~ Mux'ed Add/Data

~~EE~~ 4 Meg x 16-bit Flash & 1 Meg x 16-bit PSRAM

~~EE~~ 1.8V Core & I/O's

~~EE~~ Asynchronous/Burst Single-access (Flash; 70ns PSRAM: 90ns),

~~EE~~ Synchronous-Burst (Flash Only); Cont or 8/16/32-word, 87.5ns/13.5ns @54MHz Max

~~EE~~ Active-Max: Flash/PSRAM 40mA/20mA, Standby: 120µA, Deep Power-Down: <10µA

?? Intel MCP RD38F3050L0YBQ2

~~EE~~ **Non Mux'ed Add/Data (Add & Data bus connected together on PCB)**

○ 1.8V Core & I/Os.

○ 128Mb x 16-bit Flash & 64Mb x 16-bit PSRAM

○ Synchronous-Burst

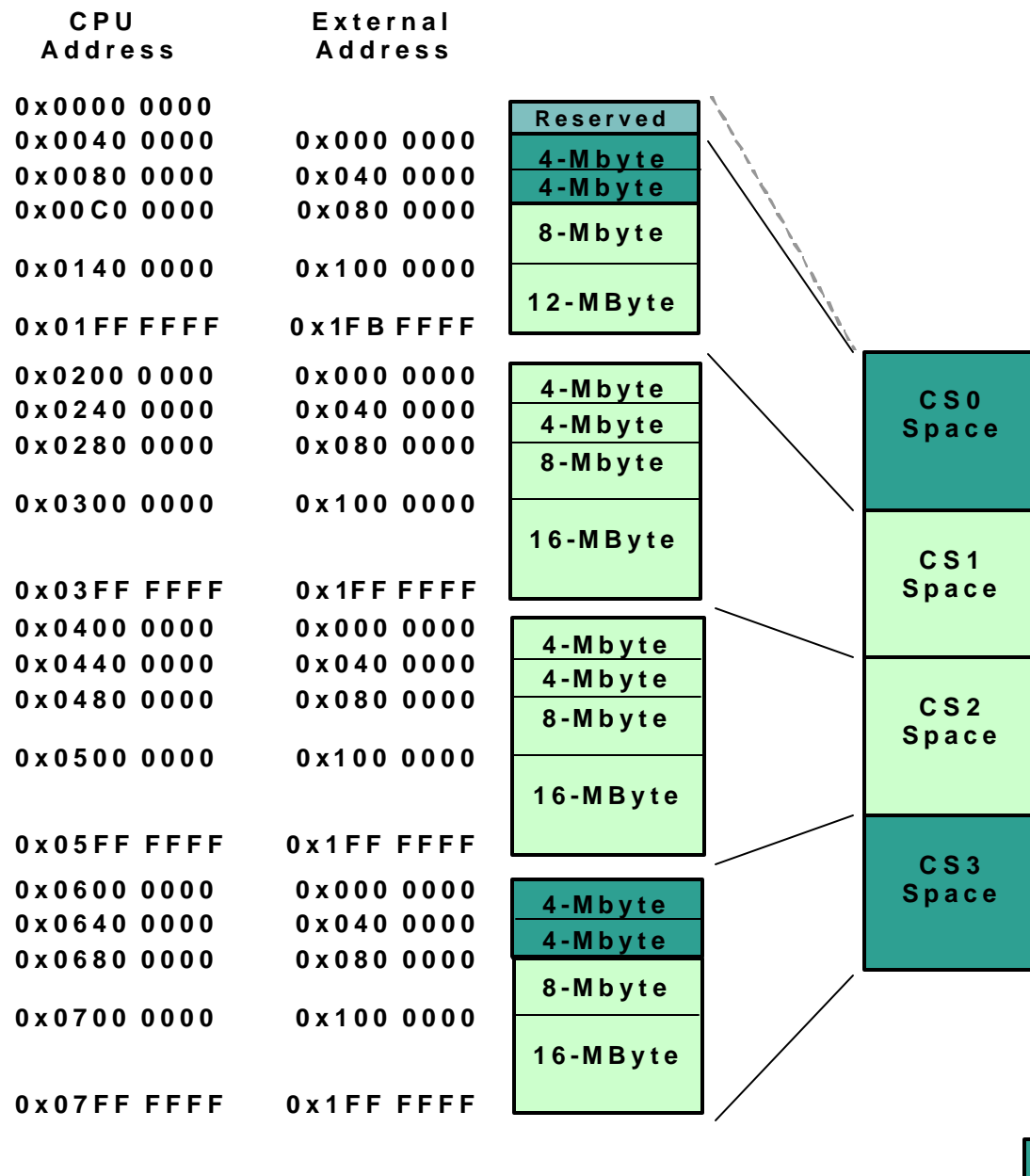


Figure 11: External Memory organization

7.4.1.3 Internal Memory Bus

The MCU' s internal-memory bus is divided in two sections; one is reserved for embedded memories (SRAM & ROM) running @104Mhz (Fast-Bus), whereas the second connects few peripherals built in ARM-memory like I/F (native 32-bit OCP IP's) running @52Mhz (Slow-bus); this peripheral direct mapping is an alternative to the RHEA bridge mapping allowing for connecting high-speed 32-bit data modules with no additional latency.

Timing adaptation (Wait-State and/or Dummy-Cycle insertion) does not apply to the internal-memory busses.

7.4.1.3.1 Internal SRAM

The on-chip 2.5-Mbit Static-RAM is accessed in 1 cycle up to 104 MHz either by the ARM processor or By the DMA. Read and write accesses are serviced either in 8, 16 or 32 bits format.

This embedded memory is used as program space and working data space for improving the execution performance of real-time critical software routines (i.e. protocol stack).

A 2-Mbit portion of the RAM can be partially or entirely protected thanks to the Enhanced Memory Protection Unit. The content of this 2-Mbit block is cleared at power-on reset

7.4.1.3.2 Internal ROM

The on-chip 1.5-Mbit ROM is accessed by ARM processor as well as DMA in 1 cycle up to 104 Mhz in read mode either in 8, 16 or 32 bits format. This embedded memory mainly contains the MIDI-engine including Down-Loadable Sound...

7.4.1.3.3 Boot-ROM (See also section: 7.4.5.1 Secure Hardware)

The device's boot-sequence is executed from the internal 64-KBytes Boot-ROM. The Boot-ROM is double-mapped, accessed from internal memory space (0x0900:0000) and from the first/boot addresses of the ARM memory space (0x0000:0000)... See *Figure 10: MCU Memory space organization*. The Boot-ROM is connected to the internal-memory Slow-bus then accessed for execution in read mode up to 52 MHz either in 8, 16 or 32 bits format. The Boot-ROM content is protected and cannot be read from a "Firmware code".

Basically, the Secure Boot-ROM code authenticates and verifies the integrity of the external Firmware or the downloaded FLASH Programmer before their execution on the device.

7.4.1.3.4 Secure SRAM (See also section: 7.4.5.1 Secure Hardware)

The Secure SRAM, intended for secure data operation/storage, is a 512-byte embedded SRAM and that is only accessed while running the secure mode (Boot-ROM code execution). In secure mode, Read and Write accesses either in 8, 16 or 32 bits format are allowed from MCU only (no DMA accesses) whereas the memory is not accessible neither for MCU nor for DMA in non-secure mode (Firmware code execution). The Secure SRAM, connected to the internal-memory Slow-bus, is accessed up to 52Mhz. The Secure SRAM content's is cleared at system reset.

7.4.1.3.5 Others Internal-memory Slow-bus resources

In addition to the Secure-System-Memory (Secure SRAM & Boot-ROM), following components are connected to the MCU' s internal-memory Slow-bus where they are accessed up to 52Mhz either from ARM processor or from DMA.

?? Crypto processors (See description section: **7.4.5; Secure Environment**)

Read/Write operation to the Crypto-Processor's memory-mapped registers and FIFO-Buffer memory is performed in 32-bit word format only. Access to Cryptographic resources can be protected during secure-mode execution.

?? Protected-Mode control & status register (See description section: 7.4.5.1.3)

Read/Write operation to the PMCTLST's memory-mapped register is performed in 32-bit word format only. Access is only granted while running the secure mode (Boot-ROM code execution)..

?? Debug Unit (See description section: **7.4.2.3**)

The Debug-Unit's 256-Byte (64 X 32-bit word) embedded SRAM can be Read/Write addressed in 8/16/32 bits word size when debug is disabled only.

?? Nand-Flash controller (See description section: **7.4.4.5**)

The Nand-Flash's Memory-mapped registers for control & monitoring operation are Read/Write accessed with a 32-bit word format only. The Double-page (2 x 128-Bytes) memory-buffer for data transfer can be addressed in 8/16/32-bit word format

?? Serial-Port I/f (See description section: **7.4.4.8**)

The Serial Port I/F's Memory-mapped registers for control & monitoring operation are Read/Write accessed with in 8/16/32-bit word (32-bit word address aligned).

?? Camera-Core (See description section: **7.4.4.13**)

The Camera-Core's Memory-mapped registers for control & monitoring operation are Read/Write accessed with a 32-bit word format only.

7.4.1.4 [TU31] MCU/cDSP shared memory (API) Bus

The MCU and cDSP sub-systems exchange data via the API bus. This interface support:

?? 16K 16-bit word shared RAM

?? **Host Only Mode** (DSP idle) or **Shared Access Mode** (concurrent MCU/DSP accesses)

?? 32/16/8 bits word size adaptation

?? Programmable MCU wait-state access (Access Factor); Support '0' wait-state HOM @52MHz

7.4.1.5 MCU RHEA-peripherals bus

The RHEA bus connects the μ -Controller's peripheral functions. The last 128 K-Byte addresses block of the ARM memory map is reserved for addressing RHEA peripherals

The RHEA space is divided in 2 sectors, each having configurable Access-Factor (wait-State)

?? "STROBE-0" sector: 0xFFFF-0000 up to 0xFFFF-FFFF (64 K-Byte)

?? "STROBE-1" sector: 0xFFFE-0000 up to 0xFFFE-FFFF (64 K-Byte)

Note:

Basically each sector is divided in sub-section of 2 K-Byte that defines address-range for one peripheral. However, Sub-sections are sometimes (re)sized to fit peripheral set requirements.

Please see the chapter on MCU interconnect (section: 12.1) for details

The RHEA Bus supports:

- ?? Memory-mapped registers &/ FIFO-Buffer memory
- ?? 32/16/8 bits word size adaptation
- ?? Programmable wait-state access (Access Factor); Support '0 wait-state, @52MHz

Notes:

1. RHEA-bridge supports the word size adaptation, however, peripherals modules documentation should be consulted to effectively define the word-size supported...
2. Modules may include Access synchronization mechanism that affects access latency...

7.4.1.6 Rhea-Switches

APC, DRP OCP Slave 2, MCSI, C-Port & UART functions are shared to the MCU and to the DSP. For each module, allocation to the ARM or DSP processor is managed through either static or dynamic switches.

Static switch is one which is configured based on processor's Mail-box/hand-shaking mechanism. Once set the module is exclusively reserved to the elected processor.

The default configuration is:

- ?? APC allocated to DSP
- ?? MCSI allocated to DSP
- ?? C-port allocated to DSP
- ?? UART allocated to MCU (Reset to none by the boot code)

APC, MCSI & C-Port are shared via **"RHEA-Switch"** Cells (figure below), The UART which is an OCP native bus is shared using a **"Static SWitch OCP-RHEA"** that include the bus switching mechanism and the OCP to RHEA bridge.

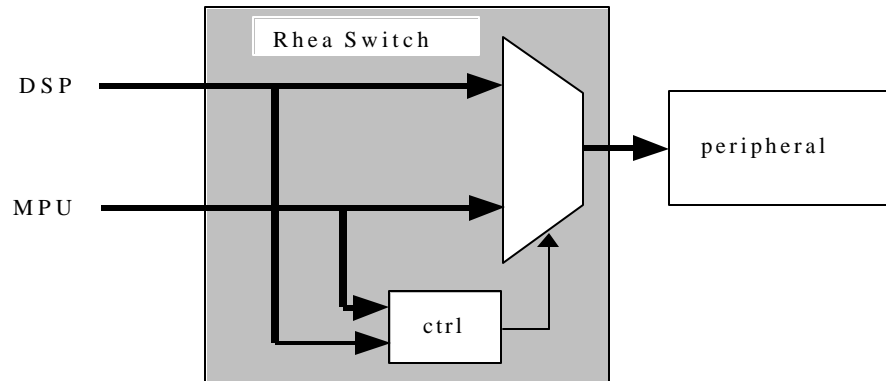


Figure 12: RHEA switch design

The RHEA-Bus module's sharing is done through semi-static multiplexers where the Bus path can be set in three positions:

- ?? DSP path
- ?? Inactive path
- ?? MCU path

The Bus switch is glitches-free thanks to the "inactive-path" state that is inserted when switching from an active bus to the other. When the configuration is programmed for switching from MCU to DSP, the multiplexer's path goes from MCU to inactive, then inactive to DSP. DSP to MCU Switch sequence is DSP to inactive, then inactive to MCU.

Here the C-Port integration requires a special mention since it is a two port device.

C-Port has two RHEA interfaces namely the MCU/DMA interface (accessing the C-Port FIFO and status registers, RHEA CS 27, strobe 0) and a DSP interface (accessing C-Port all the module registers and FIFO).

Since Locosto supports MIDI, which is controlled by MCU, it requires access to the configuration registers of C-Port. This access is provided through the DSP interface of C-Port by sharing it with MCU and DSP through the RHEA-Switch mentioned above. The following diagram illustrates this hook-up

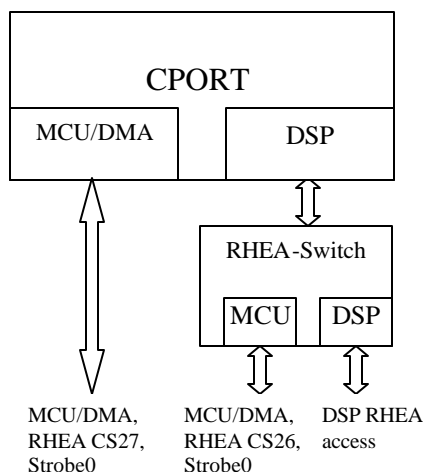


Figure 13 C-port hookup in Locosto

Dynamic switch though is the one where both masters can simultaneously access the peripheral, DRP OCP Slave 2 in this case, and the arbitration and the priority management is done by the dynamic switch. The dynamic switch for DRP OCP Slave 2 converts the RHEA requests from ARM and DSP and post arbitration converts them to the native OCP protocol of DRP.

Note:

DMA channel control's can be shared to the MCU/DSP; this sharing control is part of the DMA function not relying on RHEA-Switch module.

7.4.2 **μ-Controller's system & GP peripherals**

The Direct Memory Access (DMA) controller accessing internal-memory, RHEA and API busses speed up the data manipulation and reduce CPU data-operation load.

Asynchronous events (either chip internal or external) are recorded via an Interrupt-Handler module while a Watch-Dog Timer permanently monitors the good course of processing operations.

In addition, 2 general-Purpose Timers with interrupt capability are available for controlling scheduled operations.

7.4.2.1 **DMA controller**

In order to sustain the increased data throughput required by multimedia peripherals (such as LCD or camera I/F's[TU32]...), the enhanced DMA controller has 6 physical channels, each able transferring data from/to any of the 5 ports supported. DMA can access part of Secure-resources through a secure channel mode setting.

The ports and resources are:

?? API Bus

~~??~~ cDSP API RAM

?? Internal Memory Fast-Bus

~~??~~ 2.5-Mbit SRAM

~~??~~ 1.5Mbit ROM

?? Internal Memory Slow-Bus

~~??~~ SHA-1 (secure channel) (Tx)

~~??~~ DES-3DES (secure channel) (Rx/Tx)

~~??~~ Nand Flash (Rx/Tx)

~~??~~ Camera-Core (Rx)[TU33]

~~??~~ SPI (Rx/Tx)

?? MCU RHEA Bus (cDSP RHEA Bus cannot be accessed by DMA)

~~??~~ DRP's InterFace (Rx/Tx)

~~??~~ USB (3 Rx/Tx pairs)

~~??~~ LCD parallel interface (Tx)

~~??~~ UART (Rx/Tx when set to MCU)

~~??~~ I2C General-Purpose (Tx/Rx)

~~??~~ I2C TriTon MCU instance (Tx/Rx)

~~??~~ USIM (Rx/Tx)

~~??~~ Codec-Port/I2S (Tx)

~~??~~ MCSI (Rx/Tx when set to MCU)

?? External Memory Bus

~~??~~ Asynchronous/single-access memory

~~??~~ Synchronous Burst memory

The DMA controller main features are:

?? 8,16 or 32 bits data transfer

?? Source & destination can share a same port

?? Data pipelining (embedded FIFO)

?? Fixed data transfer length

?? 2 levels of priority



- ?? H/W or S/W request
- ?? End of transfer interrupt on ½ block, block or frame
- ?? Addressing mode
 - ?? Constant
 - ?? Incremented
 - ?? Frame-Increment
- ?? Secure channel capability

7.4.2.1.1 DMA mapping

The DMA transfer for any of the six channels can be launched from 31 H/W request Lines, which are H/W connected to Peripheral function;

Note:

Please see the chapter on MCU interconnect (section: 12.1) for details

7.4.2.2 Interrupt handler's

The Main interrupt handler allows the connection of up to 32 prioritized and mask-able interrupts to the ARM core. It receives interrupts from both internal modules and the chip external environment. Each incoming interrupt is configured as a low-level sensitive or falling-edge sensitive interrupt and can be individually masked using dedicated configuration registers.

An Interrupt Level Register is associated to each incoming interrupt to define a priority to the corresponding interrupt. If several interrupts have the same priority level, they are decoded based on the H/W predefined order.

Each interrupt can be configured either as ARM's FIQ (Fast Interrupt request) or ARM's IRQ (Low priority Interrupt request).

Furthermore a secondary interrupt handler (secure interrupt handler) is routed to the IRQ29 input-line of the main interrupt Handler. The IRQ29 line cannot be masked/disabled.

7.4.2.2.1 External interrupts

LoCosto-IC supports 1 dedicated external-interrupt to monitor ABB event. This interrupt-source is mapped onto a separate interrupt-handler channel, where it can be configured (mask, polarity...)

In addition, all GPI/O's can be configured as external interrupts all together OR-mapped on a single request-line of the MCU interrupt handler.

Edge detection (falling/rising) is programmable for each source. The value of the data inputs to the GPI/O port is latched upon the interrupt event. A 32kHz based filtering logic can be programmed for de-bouncing of the interrupt signal when necessary.

External-interrupt including GPI/O's support the system wake-up from the deep-sleep mode.

7.4.2.2.2 MCU interrupts mapping

The ARM7 owns 2 interrupt lines nIRQ and nFIQ. The fast interrupt (nFIQ) is preferably allocated to the emergency interrupt events related to a system miss-function, which could affect the physical integrity of the electronic devices. All other peripheral interrupts are mapped on the nIRQ.
The MCU interrupt handler supports up to 32 physical interrupt channels IRQ[31:0].

Note:

Please see the chapter on MCU interconnect (section: 12.1) for details

7.4.2.3 Debug Unit

The Debug Unit is a hardware resource intended to provide additional support to a software abort-handler. The DU provides 64 stages deep history table of the last memory accesses prior entering the abort mode, then permitting analysis of previous bus transaction's.

The DU is a stand-alone function that does not need any configuration. The DU is connected directly to the processor busses (address & control signals) from where it collects the data and is mapped in the MCU memory space to allow retrieving the saved history table.

The Debug Unit main features are:

- ?? 64 words FIFO depth memory mapped
- ?? 32-bit data words made of
 - ~~26~~ 26 bit address
 - ~~8~~ 8 control : nM[1:0], MAS[1:0], nEXEC, nOPC, nMREQ, nRW
- ?? continuous data record clocked on every processor fetch (instruction or data)
- ?? Data record automatically frozen upon mode switch to abort
- ?? Disabling capability via signal control (S/W control from a configuration register bit)
- ?? Reuse as General Purpose RAM storage facility when debug function is disabled

7.4.2.4 Enhanced Memory Protection Unit (EMPU)

The Enhanced Memory Protection Unit (EMPU) allows defining internal-memory sub-regions, each having a separate protection attribute; this permit for partitioning the memory space into program instruction, system data, user data, stack ...

The application program configures the EMPU, which interfaces to the processor via the RHEA bus. The address bus directly issued from the processor is monitored providing a real-time position of the memory region accessed. When a protection breach attempt occurs, the memory control signals are affected, not writing/reading the memory and the fault condition is indicated to the processor.

The EMPU allows for controlling 3 different protected memory spaces shared by a Micro-controller and a Direct Memory Access (DMA):

- ?? API memory space.
- ?? External memory space.
- ?? Internal memory space.

For each region, memory mapped control registers define:

Internal memory

- ?? Up to four programmable protected regions within a maximum memory space of 256 k-byte
- ?? A 64 k-byte maximum region size (256 k-byte for 4 regions).
- ?? A minimum granularity of 8 bytes on internal memory
- ?? A minimum granularity of 1 byte on the API
- ?? A minimum granularity of 128 bytes on external memory
- ?? A privileged-code memory region (see Protection Mode definition)
- ?? Protected memory region base-address
- ?? Protection mode (Non-User R/W, User Read-only, ROM, Privileged-region write) applied to the memory sub-region bounded by the starting/ending addresses
- ?? Starting/ending addresses within the protected memory region

API

- ?? The boundary of the API protected region.
- ?? Protection mode (Read protect, Write Protect, Read/Write protect)

External Memory

- ?? The protected region from the External memory base address within the system memory map to the limit of this region.
- ?? Protection Mode enabled/disabled (protection type is internally hard coded to protected write)
- ?? The protection enable bit is "write once" and is activated according to the External memory chip select defined in the control register. This feature allows protecting an external memory in any chip select configuration.

The EMPU generates:

Internal, external memory and API

- ?? An illegal-access signal for each type of protected memory space (internal, external and API) if the application program attempts a non-authorized access to a memory region (i.e. User write access to a region programmed for User Read-only accesses).
- ?? A MPU-fault signal which is a logical function of the 3 protected spaces (internal, external and API) Illegal-access signals.

?? A fault indication (Illegal-access) flagged into the EMPU status register which is available to the processor for fault analyze

Important notes

The “Out-of-protection” monitoring available in the Calypso chip's family is not supported.

The external memory protection part is built with the External Memory I/F and monitors ARM processor as well as DMA accesses.

7.4.2.5 General-Purpose & Watch-Dog Timers (TIMER).

The chip implements three 16 bits timers configurable either in ‘auto-reload’ or in ‘one shot’ modes. These timers generate interrupts to the ARM when equal to zero.

One of the timers is configured by default as a watchdog of the MCU and is clocked by a 13MHz/14 source. This watchdog function can be deactivated through a specific data write sequence into a dedicated register thus re-configuring the timer as a general-purpose one.

The two other general-purpose only timers are clocked from the 13MHz source.

7.4.3 GSM Dedicated Peripherals

7.4.3.1 Time Processing Unit: (TPU)

The TPU is a real-time sequencer dedicated to the monitoring of the GSM base-band processing.

From an event table referring to a GSM TDMA time base, the TPU activates tasks to control DSP peripherals with respect of the time constraints related to the GSM sequencing (quarter of bit time accuracy).

The execution of the GSM scenario is based on real-time micro-instructions to schedule the programming of the real-time parallel port (TSPACT) that control the embedded Digital Radio Processor as well as the external RF Front End.

The scenarios are stored in a 2 ports RAM of 1024 words of 16 bits with a dual page addressing capability to support a TDMA frame based pipe-lining. The TPU RAM can be accessed by the MCU in write mode only when the TPU sequencer is active.

7.4.3.2 Ultra Low-Power Down controller (ULPD)

The ULPD controller manages the deep-sleep mode of the baseband function in coordination with the CLKM manager. It allows switching off the 13MHz clock de (divided by two from DRP's DCXO) during the discontinuous reception phases in GSM idle mode (DRX) for power saving. During this Deep-Sleep mode, the ULPD maintains the GSM time-base activity from the low-power 32KHz clock reference thus keeping the mobile phone synchronization with the network. Moreover, as an extrapolation of the deep-sleep management concept, the ULPD controller is used to monitor the chip wake-up and falling asleep sequences when switching from OFF to ON mode and conversely.

The main functions of the ULPD block are:

?? Gauging of the 32 kHz Clocking signal supplied from ABB Chip.

- ?? Maintenance of GSM time during deep-sleep mode with the minimum time accuracy to allow a burst demodulation at wake-up
- ?? Programmable timer to exit deep-sleep
- ?? Delivery of the 13MHz master clock to the CLKM/DPLL modules
- ?? Switching between 13MHz and 32KHz
- ?? Generation of the chip functional reset

The It-Wakeup signal indicates to the TriTon Power-IC when the DBB is entering/exiting the deep sleep mode in order the power is adjusted to the relevant operating modes. When high, a full power setting is requested, when low (deep-Sleep) the low-power mode can be set.

The figure here after illustrates the ULPD functional Blocks

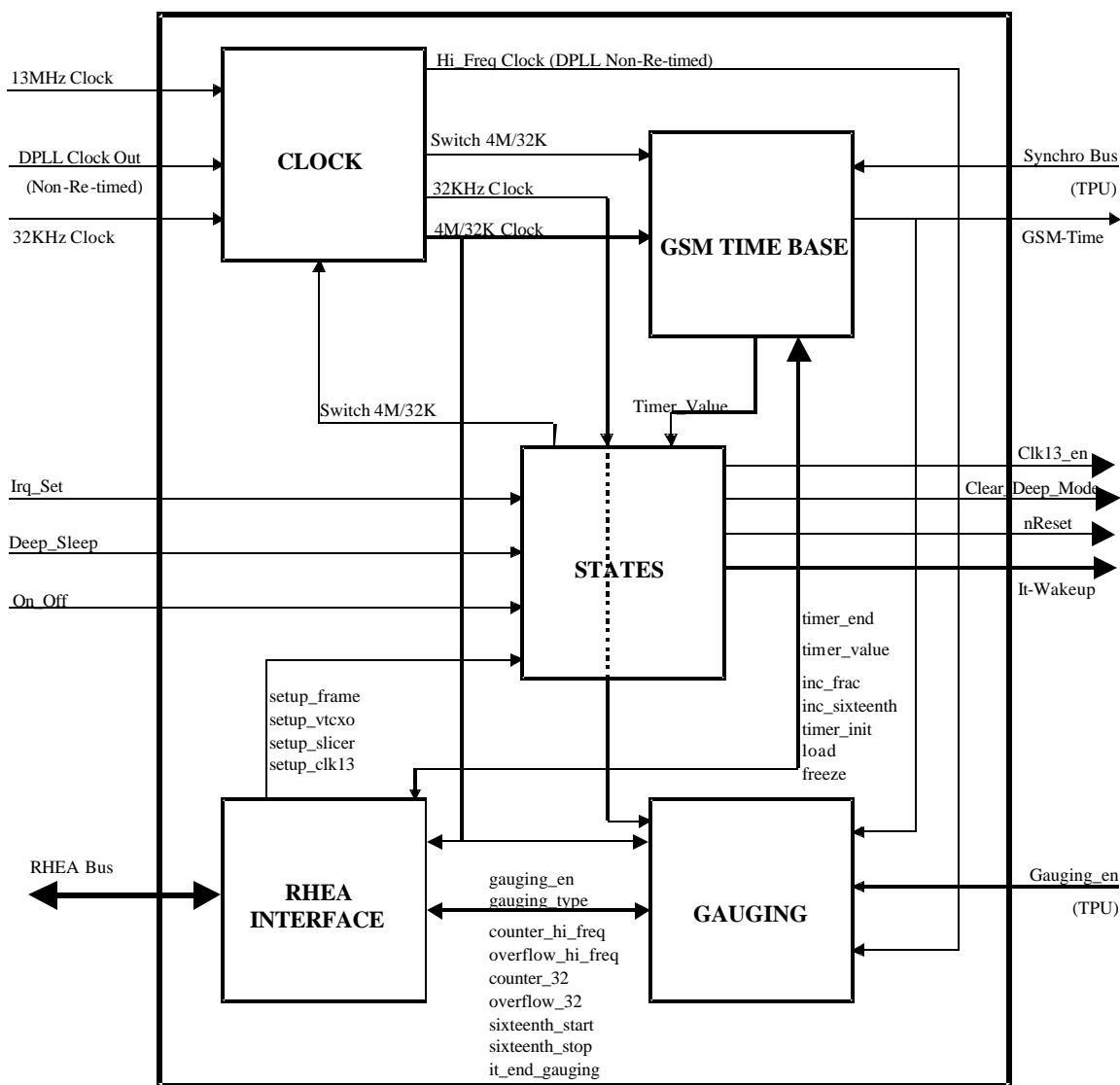


Figure 14: Ultra Low-Power Down Controller Block Diagram

7.4.3.2.1 32KHz Clock Gauging

In GSM idle mode the RF path is not continuously active, then to reduce the terminal power consumption all clocking signals sourced from the 13MHz reference are stopped; only the 32KHz clock remains enabled.

While the RF part and the reference clock are deactivated (Deep-Sleep Mode), the DBB has to maintain an accurate GSM time-base in order to recover and process the next radio data to receive.

In deep sleep mode, the GSM time base counter is clocked on the 32 KHz clock. To insure that time base accuracy is maintained, the counter increment is adjusted based on the 32 KHz-Clock period gauging before entering the Deep-Sleep Mode.

Two methods may apply for 32KHz Gauging

?? Sample 32 KHz clocking signal with the high frequency clock issued from the DPLL (DPLL Clock Out) during GSM active phases.

?? Compare 32 KHz with the GSM network time.

Note :

Gauging start and stop can be executed from CPU or through a TPU Scenario (TSPACT).

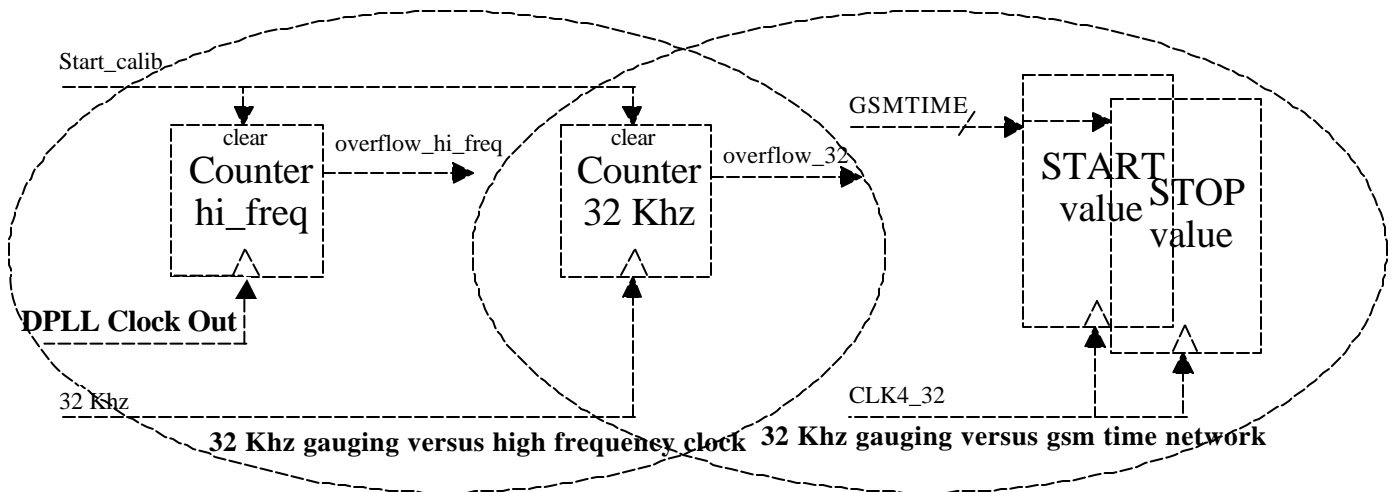


Figure 15: 32KHz Clock gauging schemes

7.4.3.3 USIM Interface

The Universal Subscriber Identity Module Interface is designed to support many simultaneous smart-card applications such as SIM (GSM), USIM (3GPP), banking (EMV) and loyalty application. This module implements the hardware interfaces to the Smart Card and a sequencer that manages the transmission protocols T-0 and T-1, defined in the ISO7816.3 standard, thus freeing the MCU of the real-time constraints.

In a LoCosto Chip-Set environment, the USIM I/F is restricted for controlling the GSM SIM -card

The USIM Interface handles:

- ?? The activation sequence
 - ~~??~~ H/W interpretation of coding convention
 - ~~??~~ Timing management for ATR sequence
- ?? T=0 transmit & receive protocol with parity error and timers management,
- ?? T=1 transmit & receive protocol with error (parity/EDC) and timers management,
- ?? The warm reset sequence,
- ?? The clock stop Sequence,
- ?? The deactivation sequence.

7.4.3.4 GPRS Encryption Algorithm (GEA1/2/3)[TU34]

In GPRS mode, the data confidentiality is performed by a ciphering function called GEA (GPRS Encryption Algorithm). The ciphering is executed within the LLC upper layer. According to the option negotiated with the network the GEA mode 1 mode 2 or mode 3 may be selected.

The purpose of the LLC is to convey information between the mobile station and the Serving GPRS Support Node. The procedures used are modeled upon the HDLC concepts. The LLC shall support both acknowledge and unacknowledged mode and implement a Frame Check Sequence (FCS) according to the selected mode.

The GEA block supports the computation of the FCS according to the LLC and the ciphering/deciphering mode 1,2 and 3. These procedures are described in the GSM 01.61, 04.64 recommendations and detailed in GSM MoU documents.

7.4.3.5 GSM Cipher-processor (A51/2/3)

The cipher-processor implements both A51 and A52 algorithms as defined in GSM Rec03.20 and detailed in GSM MoU documents. This processor is enhanced with the new A5/3 algorithm (Kasumi) as defined in GSM/EDGE Cipher algorithm A5/3 MoU document.

These algorithms realize the protection of both user data and signaling information elements at the physical layer on the dedicated channel. A5/3 algorithm implements additional registers to configure long key (up to 128 bits) and to generate long encipher/decipher data.

Note:

The cipher-processor is mapped to the cDSP-RHEA bus.

7.4.4 Connectivity peripherals

7.4.4.1 Universal Asynchronous Receiver/transmitter 16C750 (UART Modem/IRDA interface)

These UART interface is compatible with the NS 16C750 device. It is devoted to connect an external modem device through a standard wired interface or an IRDA module or the Bluetooth control/data path. The three functions can be supported dynamically with additional GPIO's & Software control as far as external components can be tri-stated. In case of mux'ed system, the standard wired UART should be set by default (@reset) if it is selected as booting path.

All modem operations are controllable either via a software API or using the hardware flow control signals.

Each upgraded UART 16C750 includes the following additional features:

- ?? Hardware flow control (RTS/CTS)
- ?? Software flow control (XON/XOFF)
- ?? baud rate up to 115.2 Kbaud (standard PC) and up to
 - 812.5Kbaud (if selection of 13MHz clock source as reference system clock)
 - 1.625Mbaud (if selection of 26MHz clock source as reference system clock)
 - 3.25Mbaud (if selection of 52MHz clock source as reference system clock)
- ?? Data rate based on a programmable divisor N ($N = 1 \sim 65536$)
- ?? Data clock = $13 \text{ MHz} / N$
- ?? Data rate = Data clock / 16
- ?? Auto-baud with the possibility to match to baud-rate from 1200 to 115.2Kbits/s

Important Notice:

UART module is shared between the MCU and the DSP processors. One processor only at a time can control the module with the allocation defined by processor's handshaking through the REHA-Switch Module. By default, the UART is connected to the MCU RHEA bus.

The reference-clocking signal providing 13/48/52MHz is generated and configured into the CLKM function.

7.4.4.2 General purposes I/O (GPI/O).

3 sets of 16 General Purpose I/O ports (GPI/O) are offered and can be individually configured as input or output ports through registers programming.

Additionally, each I/O can be configured as a generic purpose external interrupt:

- ?? Edge programming (falling/rising)
- ?? Latch of all GPI/O external input port electrical state on the interrupt event
- ?? 32KHz debouncing filter (bypass capability)
- ?? Deep-sleep Wake-up

Each 16-GPIO Set are mapped on a single physical channel of the MCU interrupt handler.

Each 16-GPIO module includes the BU & LT PWM generators; One BU instance only is available at the LoCosto chip, whereas LT1, LT2 and LT3 can be used depending on pin mux'ing selection.

Note:

BU & LT have the same functionalities as PWT & PWL modules respectively...

7.4.4.3 Keyboard interface

The keyboard interface is sized to support keyboards up to 8 columns per 8 rows. Only a 5x5 configuration is considered in the LoCosto chip.

The keyboard controller implements a built-in scanning algorithm for hardware based key press decoding. Several key press detection modes are offered:

- ?? Event detection on both key press and key release
- ?? Programmable press detection on key release only
- ?? Long key detection on prolonged key press
- ?? Time-out on permanent key press or after keyboard release

The controller supports the detection of single and multiple key press. On key press or release, after a programmable debouncing time, the scanning sequencer is activated. The resulting digital snapshot of the keyboard is registered and compared to the previous one. On change detection, an interrupt is sent to the MCU.

The scanning sequencer will keep running if a long key detection is programmed or until the no-activity time-out. Interrupts will be generated accordingly.

Debouncing time, long key duration and time-out value are software programmable.

In order to operate whatever the system activity mode, the controller logic is scheduled on the 32KHz reference clock thus allowing the system to wake-up from any sleep modes.

The keyboard interface also supports the Roller Key functionality based on three bi-directional IOs multiplexed with the keyboard keys.

7.4.4.4 LCD Parallel Interface

In order to improve the data throughput to support the connection of an external color graphical LCD controller, the chip integrates an 8-bit parallel interface module dedicated to the connection of an external LCD-controller chip.

This interface is compliant with the 8bit 6800-Series and 8086-Series Parallel interface standard in order to support a large range of LCD displays available on the market.

The interface implements a DMA channel to allow the transfer of the data from the internal SRAM or any Rhea peripheral to the display RAM of the external graphical LCD concurrently to the MCU activity. The transfer rate between the internal SRAM or a Rhea peripheral and the interface can be operated at MCU maximum speed with words of 16-bits.

This interface targets LCD device with the following features:

- ?? Color LCD screens (passive or active matrix)
- ?? 8-bit 6800/8086-Series Parallel interface
- ?? 16-bit (RGB 656) or 24-bit (RGB 888) Color
- ?? up to QVGA (320x240) format

The transfer of the LCD data from the LCD interface to the external LCD controller is performed at a fractional rate (1,2,4,8) of the 13Mhz reference clock.

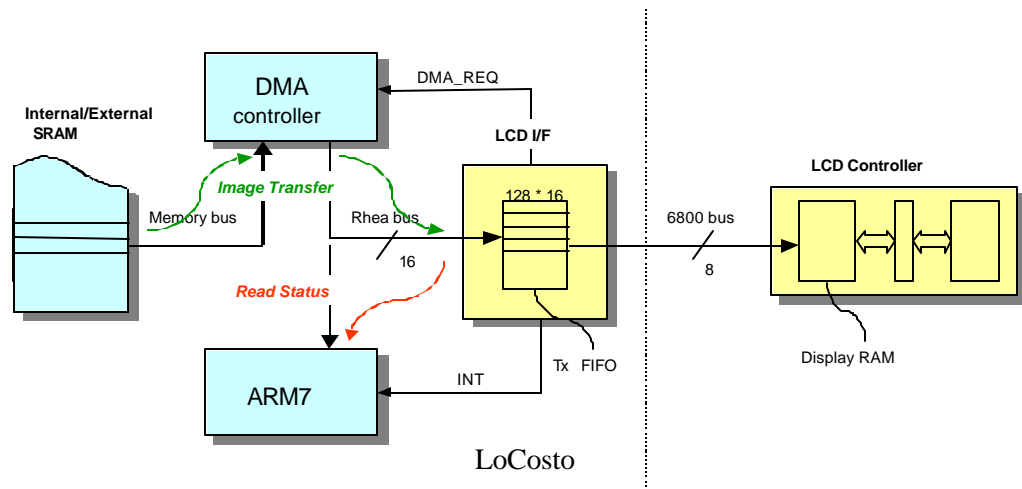


Figure 16: LCD parallel display transfer data-flow

Note:

Other alternatives for external LCD-controller are serial interface (SPI, I²C) for limited PCB traces.

7.4.4.5 NAND Flash interface

The NAND Flash interface allows connecting NAND Flash EEPROM as an external mass storage facility.

The interface implements a 8 bits parallel data bus in addition to the control signals for selecting chip, writing/reading, command and address latching, ready/busy status:

- ?? 8, 16 and 32 bits interface from host processor (mapped on internal memory interface)
- ?? Double page FIFO implementation (2*128 bytes)
- ?? Programmable access time
- ?? Interrupt and flag (polling operations) for end page or end transfer
- ?? Fully automatic transfer process
- ?? Programmable number of bytes for command, address and data
- ?? Programmable page size of Nand Flash Memory
- ?? Support hardware computation of Error Code Correction (ECC) in read and program mode
- ?? Support DMA transfer with DMA request

Example of supported Nand-Flash devices

- ?? SAMSUNG K9F5608UOM - 8-bit I/F, 1.8V, 256Mbit...
- ?? SAMSUNG K9K1G08U0M - 8-bit I/F, 1.8V, 1Gbit...

7.4.4.6 USB Client (W2FC)

The USB_W2FC module supports the implementation of a "Full-Speed" device fully compliant to USB 1.1 standard. It provides an interface between the MCU and the USB device and handles USB transactions with minimal MCU intervention.

The USB_W2FC module supports one control endpoint (EP0), up-to fifteen (15) IN endpoints and up-to fifteen (15) OUT endpoints. The exact endpoint configuration is software programmable. The specific items configurable for each endpoint are the size in bytes, the direction (IN, OUT), the type (Bulk/Interrupt or ISO), and the associated endpoint number.

The USB_W2FC module also supports three DMA channels for IN endpoints and three DMA channels for OUT endpoints for either Bulk/Interrupt or ISO transactions. In operation, the USB requires a 48MHz clock generated by a dedicated embedded DPLL upon request. The USB module interface is PSCI compliant. Therefore this module interfaces with the TI MCU RHEA bus via a RHEA-PSCI bridge.

Locosto chip does not integrate the transceiver (differential drivers) that are available in TriTOn ABB chip; the USB_W2FC interface is supplied at 1.8v.

Important Notice:

3 & 4-wire LoCosto/Triton I/F are supported with an additional specific on-chip USB wrapper. The wrapper implementation can be extracted from the USB-OTG design & integration spec's

7.4.4.7 APLL (USB specific Clock generation)

The APLL is the UC684 cell available within the TI-ASIC GS50 analog cell library. This cell is a clock multiplier for creating a 96MHz from 12, 13, 16.2 and 19.2MHz. In LoCosto S-O-C the APLL is hard-wired for receiving the 13Mhz from the DRP's DCXO. The APLL is a stand-alone function not mapped to the memory space; the only available control "APLL On/Off" is set from register bit located within the CLKM function.

The APLL includes:

- ?? Phase Frequency detector
- ?? Charge Pump
- ?? Passive loop filter
- ?? Voltage Controlled Oscillator
- ?? Prescaler
- ?? Fractional Accumulator
- ?? Bias Reference
- ?? Lock Detector
- ?? Multiple Input shift-register
- ?? Power domain level-shifter

The APLL is powered from dedicated power-lines (VDD-APLL & VSS-APLL) for noise rejection hence reduced jitter

7.4.4.8 Serial Port Interface (SPI)

The serial port interface is a bi-directional, four-line interface dedicated to the transfer of data to and from external devices offering a four-line serial interface. The four-line interfaces are:

- ?? The clock used to shift-in and shift-out data
- ?? The device enable
- ?? The data input
- ?? The data output

This serial port interface is based on a looped shift-register, thus allowing both transmit (PISO) and receive (SIPO) modes. It can operate either in master or slave mode, using MCU or DMA control.

A read process is always simultaneous with a write process, because the internal shift register (REG_SR) is based on a loop (FILO principle). However the concurrent write process can be dummy if no data is transmitted.

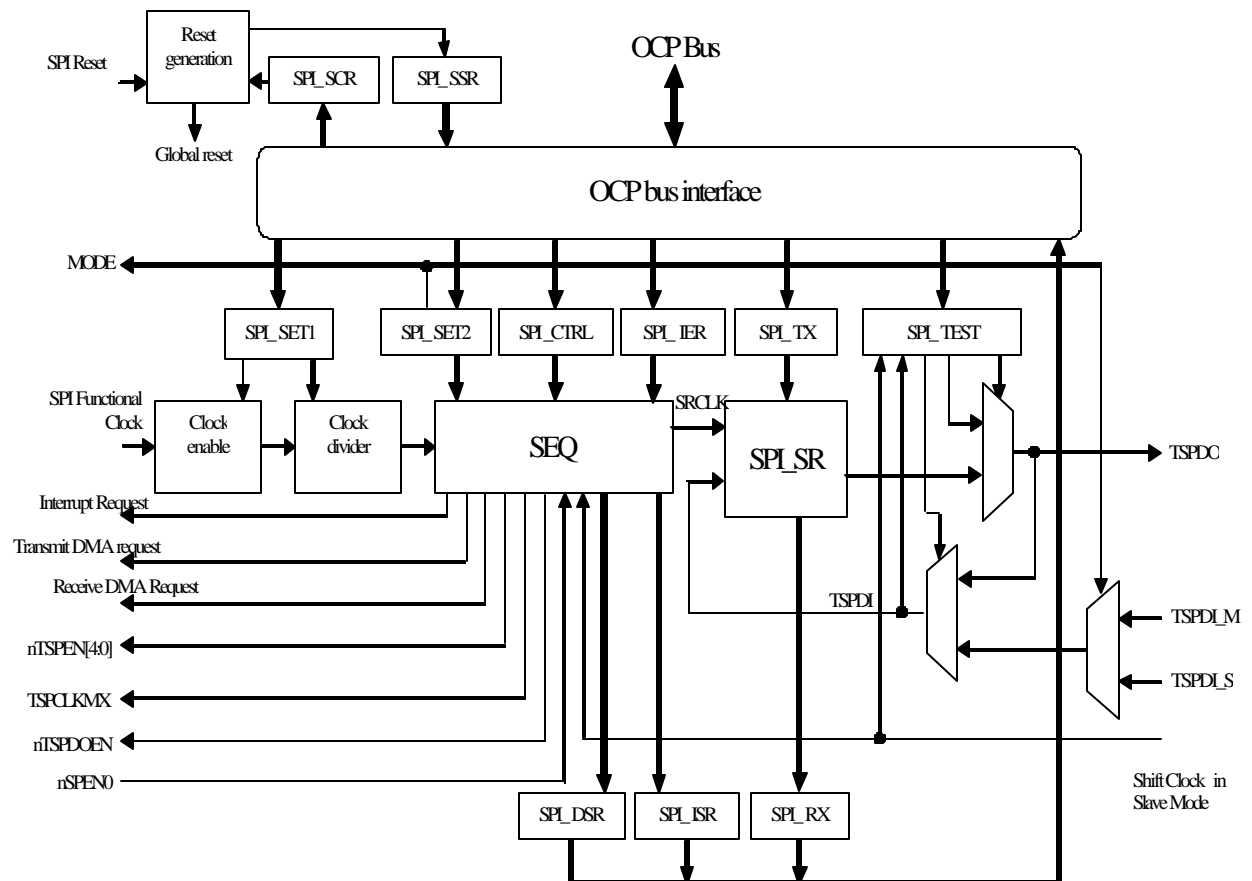


Figure 17: SPI Block Diagram

The serial port interface is configured through its setup registers (REG_SET1, REG_SET2).

After loading the transmit register, the transfer is effectively started by setting one bit of a control register (REG_CTRL) to high level, enabling it to indicate a read or a write operation.

The external transfer of a packet starts as soon as the transmit clock is generated. The transmitted data packet is shifted out on the rising or falling edge of the transmission clock, and the received data packet is shifted in on the complementary edge of the clock.

The loading of the packet in the external device is then validated on the deactivation of the enable signal (rising or falling edge, depending on configurable parameters).

An interrupt can be generated (depending on the setup register) at the end of the write or read/write cycle. The IRQ request is reset when the MCU writes a 1 in the corresponding status register bit (REG_STATUS) or reads the receive register (REG_RX) after a read.

In master mode, the SPI provides up to five chip-selects; three of them are propagated outside LoCosto. In slave mode, the SPI has its own chip-select.

In master or slave mode, the maximum SPI data rate is 26 bits/s. The clock supplied in master mode is issued from the CKLM (13/48/52Mhz reference clock).

Important Notice:

The SPI module is a native 32-bit OCP bus. It is connected to the 32 bits internal-memory slow-bus through a specific Wrapper that permits ARM processor or DMA to access SPI resources.

7.4.4.9 Multi-Channel Serial Interface

The MCSI is a Serial Interface with a Multi-Channels transmission capability. It expands the addressing capability of the parallel interface of a Digital Signal Processor to connect external devices such as CODEC, DSP or any external device integrating audio capability.

All transmission parameters are configurable to cover the maximum number of operating conditions:

- ?? MASTER or SLAVE clock control (transmission clock and frame synchronization pulse)
- ?? Programmable transmission clock frequency from 3.15KHz to 6MHz (Reference clock 13MHz)
- ?? Single or Multi (x16) channels frame structure
- ?? programmable word length : 3 to 16 bits
- ?? Full-duplex transmission
- ?? Programmable frame configuration
 - ?? Continuous or burst transmission
 - ?? Normal or Alternate framing
 - ?? Normal or inverted frame polarity
 - ?? Short or long frame pulse
 - ?? Programmable over-size frame length
 - ?? Programmable frame length
- ?? Programmable interrupts occurrence time (TX and RX)
- ?? Error detection with interrupt generation on wrong frame length

This physical interface is mainly intended to support the audio link with an external Bluetooth baseband IC device based on 8-bit data format with 8KHz sample rate. However it may support any other component implementing compliant serial I/F.

Moreover, the interface supports the GSM DAI operating modes (Radio uplink, Radio downlink and acoustic). In DAI mode, the MCSI interface is configured to being directly connected to the GSM System Simulator interface including the Reset System Simulator signal.

Important Notices

MCSI module is shared between the MCU and the DSP processors. One processor only at a time can control the module with the allocation defined by processor's handshaking through the REHA-Switch Module. By default, the MCSI is connected to the DSP RHEA bus.

MCSI_CK & MCSI_FS can be mux'ed respectively with CSYNC & CSCLK as well as MCSI_TX that can be replaced by CDO; this configuration makes the component attached to the MCSI receiving the C-PORT data still flow controlled by the external Master-CoDec port (TriTon).

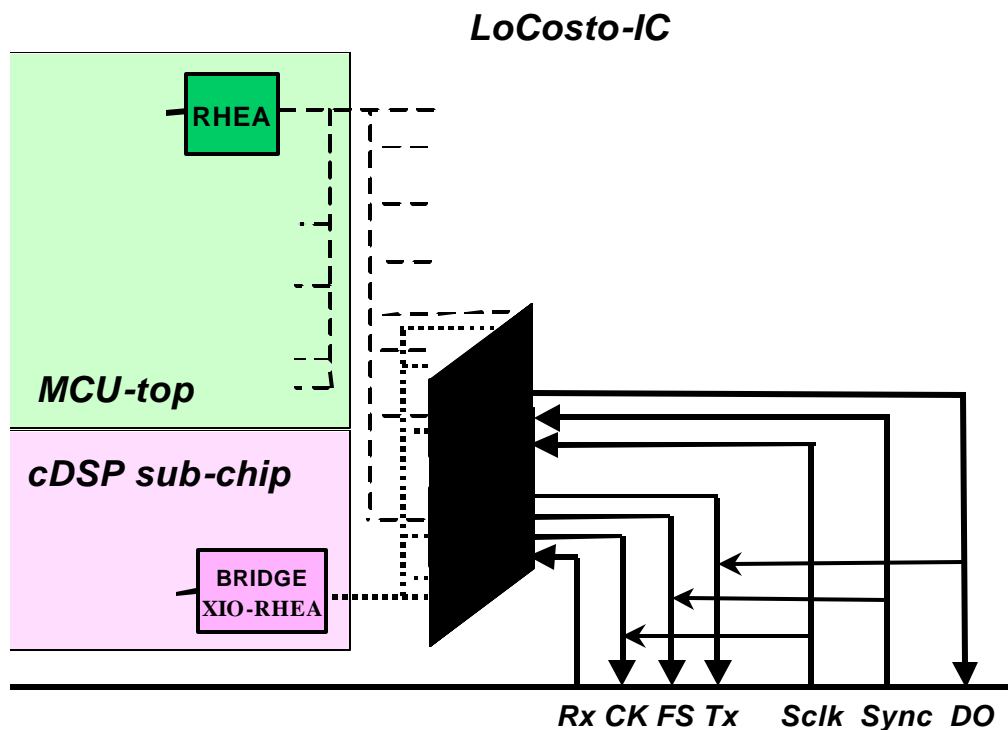


Figure 18: MCSI/C-Port pins mux'ing

7.4.4.10 Pulse Width Tones (PWT)

These modules generate a modulated frequency signal for an external buzzer.

The PWT frequency is programmable between 349Hz and 5276Hz with 12 half tone frequencies per octave. The volume is also programmable.

7.4.4.11 Pulse Width Light (PWL)

These modules allow controlling the backlight of a LCD and/or a keypad

The PWL voltage level control technique, based from a 4096bit random sequence, decreases the spectral power at the modulator harmonic frequencies. The logic operates from the 32KHz reference clock to be independent from the system activity mode.

7.4.4.12 Light Pulse Generator (LPG)

This module produces the electrical signal for a blinking LED.

The blink period and duration are programmable.

The logic operates from the 32KHz reference clock to be independent from the system activity mode.

7.4.4.13 Camera Core Interface^[TU35]

The camera core module supports two image-sensor interfaces (Serial / Parallel). The interface selection is exclusive; one only at a time can be set.

Both Serial and Parallel I/F's have:

- ?? 128 X 32-bit FIFO
 - ~~EE~~ DMA access with Enable/Disable capability
 - ~~EE~~ Configurable FIFO Trigger level
- ?? One interrupt line supporting Programmable Interrupt's;
 - ~~EE~~ start/end of line,
 - ~~EE~~ start/end of image,
 - ~~EE~~ FIFO overflow, and
 - ~~EE~~ data threshold status
- ?? Byte swapping capability /32-bit word packet supply

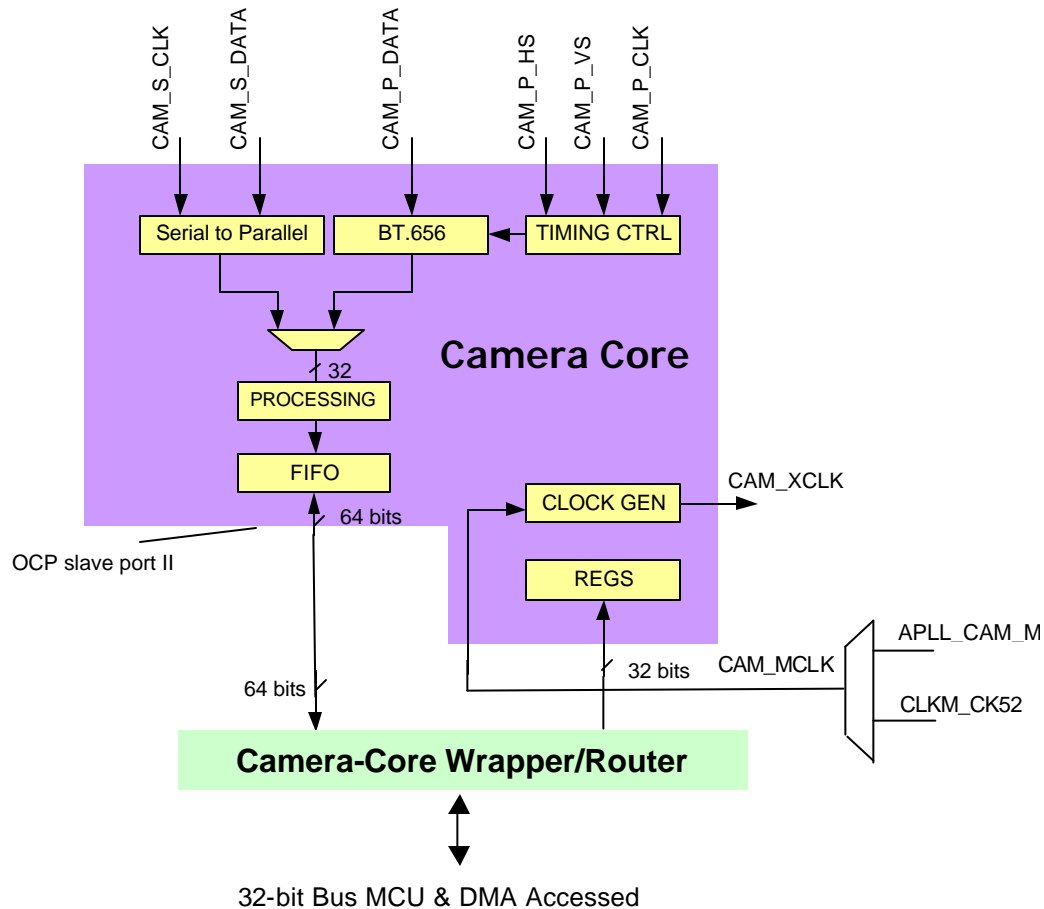


Figure 19: Camera-Core I/F block Diagram

Serial Camera I/F, (Compact Camera Port -CCP-)

The serial camera interface is a unidirectional differential interface that enables the connection to a camera sensor in compliance with MIPI Rev1.0. The physical link is of Sub-LVDS differential (Clock & Data) type for low EMI supporting external clocking signals up to 208 MHz.

The Compact Camera Port bit stream has embedded synchronization signals: frame start, line start, line end and frame end. The table below, lists image-data format supported by the CCP module.

Data Type	Abbreviation
YUV4:2:2 Image Data	YUV422
YUV4:2:0 Image Data	YUV420
RGB888 Image Data	RGB888
RGB565 Image Data	RGB565
RGB444 Image Data	RGB444
Raw Bayer, 8-bit Image Data	RAW8
Raw Bayer, 10-bit Image Data	RAW10
Raw Bayer, 12-bit Image Data	RAW12
JPEG, 8-bit Data FSP	JPEG8FSP
JPEG, 8-bit Data	JPEG8

Table 30: CCP Image-Data format

Parallel Camera I/F

The parallel camera I/F is an 8bit interface with camera horizontal/vertical synchronization signals, Camera Reference clock and Pixel-capture clock operating up to 48MHz.

The Parallel Camera module can provide a Camera Reference clock (CAM_XCLK) to the camera-sensor based on on-chip APLL (48MHz) or MCU (52MHz) clock sources

The parallel camera I/F Supports two operating modes:

?? BT656: ITU-R BT656 compatible parallel interface;

The BT.656 block extracts the start of active video (SAV), end of active video (EAV) and image-data from the 8-bit data-flow.

?? NO-BT: general parallel interface with Camera H/V Synchro to detect valid data, Reference clock and Pixel-capture clock.

7.4.4.14 I2C Multi-Master Serial Interface (I2C)

The I2C is a Multi-Master half-duplex serial port using 2 lines (data and clock) for data transmission with software addressable external devices. The interface is compliant with the Philips standard.

The main features of the interface (TI 's IP version WMU_22_2) are:

?? Multi-Master arbitration

?? Standard (100KHz) and the fast (400KHz) transmission modes



- ?? Support both burst write, single read and combined read modes
- ?? Transmit/receive burst buffer of 16 words
- ?? 3 bits programmable spike filtering logic
- ?? Error handling capability during I2C bus access

I2C-bus is used as communication path with the TriTon ABB chip. Additional external components such as FM Radio, A-GPS system, Camera module[TU36]... are also controlled via an I2C bus

To not impact the real-time constrain of the DSP/TriTon Voice-control path (based on CalypsoPlus S/W implementation) a specific on-chip Dual-I2C port scheme (tri-I2C controller instance) is designed.

Two I2C-port's are available: (**Figure 20** below highlights this implementation w/i LoCosto-IC)

?? "I2C-TriTon"

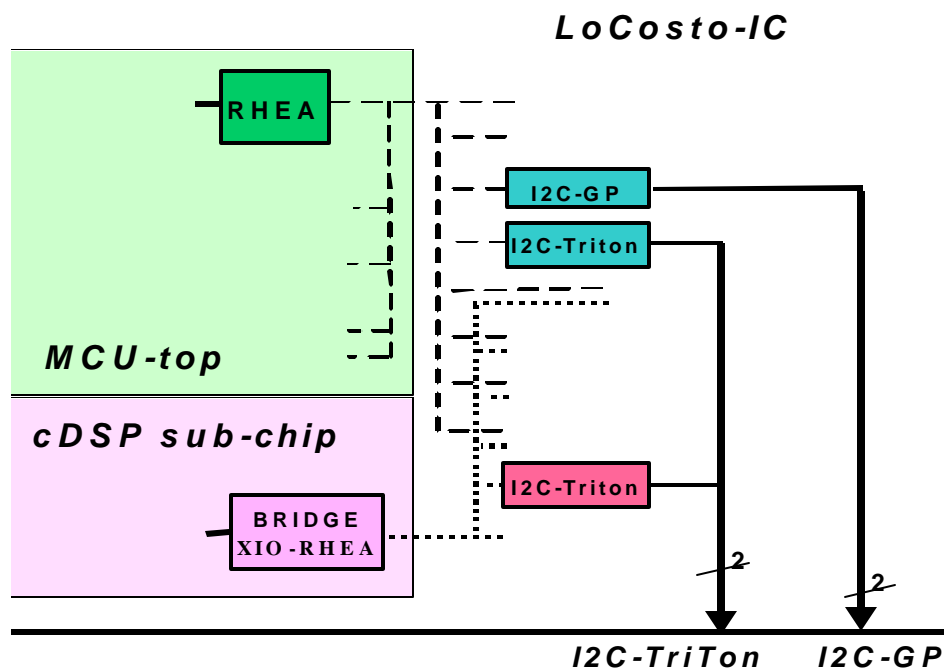
✍✍ Mainly dedicated for supporting TriTon ABB. However, additional Slave-only components can be attached to this bus.

✍✍ Controlled from two on-chip I2C-modules; (See module I/O's On-Chip wiring **Figure 21**)

- One being associated to the MCU domain (TriTon-power control... plus additional Slave-only components...),
- The second is mapped to the DSP subsystem (voice, audio controls...).

?? "I2C-GP"

✍✍ Intended for multi-master system such as A-GPS.



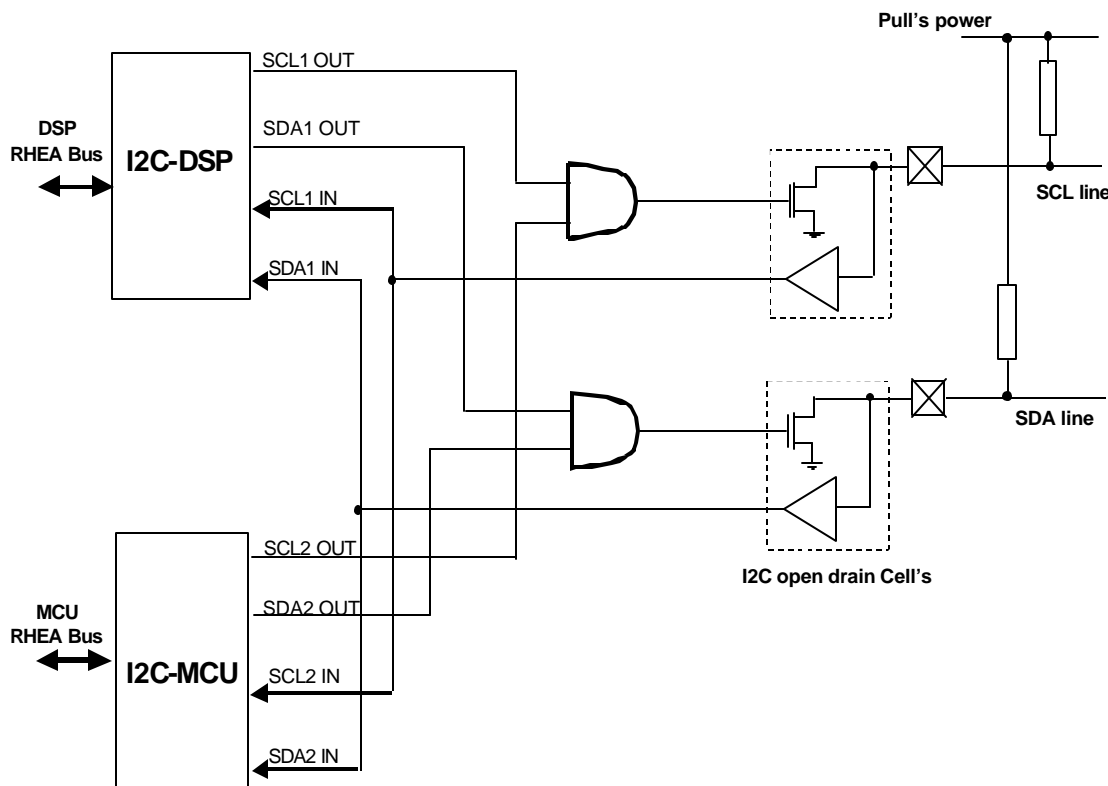


Figure 21: TriTon's I2C Controller's On-Chip AND Wiring

7.4.4.15 Voice Serial Port (VSP)

The voice serial port (VSP) is a bi-directional (transmit/receive) serial port that directly connects the c30L154's Serial Port Interface (DSP SPI) to the voice CODEC of the ABB companion chip (TriTon). Format is 16-bit data packet with frame synchronization. Clock frequency is 500 KHz.

The signal VCK is the output serial clock used to control the transmission or reception of the data. The transmitted serial data (VDX) is the serial data output, the frame synchronization (VFS) is used to initiate the transfer of transmit *and* receive data. The received data (VDR) is the serial data input. One extra cycle is generated before VFS and one extra cycle is generated after the LSB.

The Mute Mode sets the VDX signal at '0'; This mode is programmable via the DXEN bit in VBUR register. The Bit VCLKMODE (reg. VBCR) allows a continuous output of the clock VCK.

7.4.4.16 Codec Port interface (C-PORT)

The CoDec port interface (C-port) can be configured to support the Inter-IC sound (I2S) industry standard serial interface protocol. The serial interface is basically a time division multiplexed (TDM) based scheme.

The format is programmed by setting:

- ?? The number of time slots per CODEC frame, and
- ?? The number of serial clock cycles (or bits) per time slot.

The interface in all modes is bi-directional and full duplex. Both audio data and command/status data can be transferred via the serial interface depending on the mode activated. In certain operation mode, the serial data output and input signal is delayed for one serial clock (SCLK) cycle in the reference to the leading edge of the SYNC signal.

I2S operating mode allows for configuration of:

- ?? Number of time slots per Codec frame: 1 to 32
- ?? Number of serial clock cycles for time slot 0: 8, 16, 32 or others
- ?? Number of data bits per audio time slot: 8, 16, 18, 20, 24 or 32
- ?? Number of serial clock cycles for all slots other than slot 0: 8, 16, 18, 20, 24 or 32
- ?? Data delay in the reference to the leading edge of the SYNC signal: no delay or one cycle delay
- ?? Data serial output state: tri-state or enable
- ?? The Synchro and Data signals can be generated either on the negative or the positive edge of the bit clock signal and the Data signal will be sampled with the opposite edge the same clock signal.
- ?? Programmable polarity, duration, and direction of the CODEC frame sync signal
- ?? Programmable direction of the clock source
- ?? Time slot format: time slot 1 for address and time slot 2 for data or other format

Important notices

The Codec-Port connects the Audio companion chip (TriTon) that supplies the serial clock and the frame synchronization

CSYNC & CSCLK signals received from external master can be forwarded to the MCSI Port, CDO output from C-PORT can be routed to the MCSI_TX pin; this allows having an output data flow available on the MCSI Port still controlled from the external master CoDec device (TriTon).

In order to use the C-PORT in master mode still being compliant with AUDIO formats (i.e: I2S @11.2896MHz) and because the 13Mhz only is internally available, external clock can be supplied to the C-port from the PCM_CK pin (PWL pin mux'ed configuration)

Description of the Inter-IC Sound (I2S) mode

In Inter-IC Sound (I2S) mode, the CODEC port interface can be configured as an I2S link serial interface to the I2S CODEC device. The serial interface is configured in time division multiplexed (TDM) slot based mode used to transfer both audio data and command/status data to the CODEC device.

In this mode, the CODEC port interface is configured as a bi-directional full duplex serial interface with two time slots per frame: Time slot 0 is used for the left channel audio data and time slot 1 for the right channel audio data. Each time slot is 32 serial clock cycles in length. So the frame is $2 \times 32 = 64$ serial clock cycles in length. The left/right channel clock signal has a 50% duty cycle. This signal is low for the left channel time slot and high for the right channel time slot. There is 1 cycle delay from the edge of the channel clock and the most significant bit shifted out data for both the left and right channels.

The Codec Port is directly interfaced to audio processing part with a 16 bits resolution. Valid data bits and Time Slot length setting should not be less than 16 bits. In case of higher values, only the 16 Msbs of each left and right sample is taken into account: Input samples Lsbs are discarded whereas output samples Lsbs are filled with zeros.

Important Notice:

C-Port control register is shared between the MCU and the DSP processors. One processor only at a time can control the module. The allocation to the ARM or DSP processor is configurable based on processor's Mail-box/hand-shaking mechanism. By default, the C-Port control is allocated to the DSP RHEA bus.

7.4.5 Secure Environment

The secure environment, relying on ROM, secure RAM and Control-Register, eFuse array, Crypto-processors, and protected H/W resources complete the μ -Controller sub-system part of the DBB

7.4.5.1 Secure Hardware

The secure hardware module consists in three parts:

- ?? 64Kbyte secure boot ROM (as explained in **7.4.1.3.3**)
- ?? 512byte secure RAM.
- ?? 16-bit protected mode control and status register (PMCTLST register).
- ?? Secure Access Controller

7.4.5.1.1 Boot ROM

The secure boot ROM is split in a vector sector area (mapped from 0x0000 up to 0x007F) dedicated to the software services entry-points as well as the MCU's exception-vectors and test entry-points and a subroutines sector area (remaining memory space from 0x0080) that contains all the secure code including services library pointed to by the entry-points (services, test, and the exception-vectors). The Secure ROM content cannot be read/dumped neither from MCU nor from DMA; any access to the Secure-ROM subroutine area from outside the Secure-ROM is denied, returning a data to "0" and generating a security violation to the EMPU for abort generation (DMA violation is not flagged). Access to the subroutine part is also denied in emulation mode

The secure-ROM code takes the control of the system activity upon System Reset. It cannot be interrupted or bypassed until the completion of its execution. It is not dependant on the OS. It includes software-library (Macro-functions & H-W Drivers) allowing for encryption Algorithm & H-W crypto-processor control. These software libraries are available for User Secure-Application through reserved secure-ROM entry-points.

The Secure ROM code is partitioned with the following features:

- ?? Synchronization on UART (Modem) or USB to download FLASH programmer in Internal SRAM
 ~~??~~ Boot-link Selected from the "USB-Boot" pin value
- ?? FLASH-programmer or Firmware certification and authentication before execution
- ?? Secure services to perform platform binding and unbinding
- ?? Services to perform engineering tests (BIST)

7.4.5.1.2 Secure SRAM

The Secure RAM is a dedicated SRAM used for secure context stack operations and short data/variables storage. DMA accesses are not serviced. The secure-RAM is reserved for secure-ROM code execution. Any access from outside the Secure-ROM code is denied, returning a data to "0" and generating a security violation to the EMPU for abort generation.

Access to the Secure RAM is also denied in emulation mode. The content of the Secure RAM is cleared upon reset event

7.4.5.1.3 PMCTLST Register

The Protection Mode Control & Status (PMCTLST) register is a 16-bit memory-mapped register that manages the secure-mode's states enabling/disabling access to the protected hardware resources. The PMCTLST register is updated from a combination of event hardware detection and software controls executed from the secure-ROM code only. Access to the PMCTLST register from outside the Secure-ROM code is denied, returning a data to "0" and generating a security violation to the EMPU for abort generation. Access to the PMCTLST register is also denied in emulation mode.

7.4.5.1.4 Secure Access Controller

The secure access controller monitors and grants accesses to the secure hardware resources depending on MCU's fetch-type (Instruction/Data) and from where it has been initiated (ROM, SRAM...). In addition, this logic block manages the Re-mapping of exception-vectors and entry-points based on the normal/protected mode state, and the masking of the IRQ, FIQ and ABORT exceptions when secure code is executed.

7.4.5.2 Security peripherals

In order to provide the computing acceleration for cryptographic services as requested for Mobile Commerce applications, symmetrical encryption, and hashing co-processors are memory mapped on the MCU. In addition, a true RNG module is implemented for generating the necessary key-building's seeds.

7.4.5.2.1 DES/3-DES Crypto-Processor (3DES)

This crypto-processor supports the DES & 3-DES cipher algorithms. It implements the encryption and decryption functions with the following features :

- ?? ECB (Electronic Codebook)
- ?? CBC (Cipher Block Chaining)
- ?? 8 bytes input & output buffers
- ?? 56-bit key size (up to 3)
- ?? 16^(DES) round cycles per block
- ?? write and read DMA channels

7.4.5.2.2 MD5/SHA-1 Hashing Accelerator (SHA)

This crypto-processor supports the MD5 and SHA-1 hashing algorithms. It implements the hashing functions with the following features :

- ?? 64 bytes input data block
- ?? 160^(SHA) / 128^(MD5) bits output digest
- ?? 80^(SHA) / 64^(MD5) round cycles per block
- ?? write DMA channel
- ?? read interrupt

7.4.5.2.3 Random Number Generator (RNG)

The Random Number Generator provides a true, non deterministic noise source for the purpose of generating keys for cryptographic algorithms.

This true RNG is based on

- ?? dual-shot noise generators
- ?? non-linear mixer

Its main features are:

- ?? FIPS 140-1 built-in self test compliant.
- ?? 32 bits output register
- ?? 2²⁴ system clock cycles for 1st random output after reset
- ?? 32-bit random number produced each 160 clock cycles

?? interrupt on 32-bit generation completion

7.4.5.3 eFuse Array

7.4.5.3.1 Root Key Identifier (KEK)

The root key identifier is a 64-bit register composed of fuse-cells electrically programmed during the manufacturing process from an external RNG source. This identifier is intended to be used as a root key for the DES crypto-processor to encrypt secret data (keys, certificates,...) before storage in external memory.

The value of this Key Encryption Key (KEK) is not accessible to the MCU and thus cannot be tampered through non-physical means.

7.4.5.3.2 Manufacturer Public Key Identifier

The manufacturer Public Key identifier is a 128-bit register composed of fuse-cells electrically programmed and enclosing the 128 lsb of the hashing value (SHA-1) of the Public Key component of the manufacturer's Public Key pair. This value is used to authenticate any certificate signed with the Private Key from the Manufacturer.

7.4.5.3.3 Die ID cell (DIE ID)

The Die ID cell is a 128-bit register composed of fuse-cells electrically programmed during the manufacturing process. Originally intended for engineering purpose, each Die ID being unique can be used for application requiring the authentication of the device.

The Die-ID's MSBit defines a secure/non-secure Chip

7.4.5.4 Protected Resources

7.4.5.4.1 Memory Protection Unit (EMPU)

See **7.4.2.4 Enhanced Memory Protection Unit (EMPU)**

7.4.5.4.2 Protected Resource Reset Management (PRRM)

The Protected Resource Reset Management is a "reset module" that can perform a reset on:

?? The 2Mbit Internal memory space by providing an address bus for the internal memory space. This address is incremented from the start address register to the end address register.

?? The API memory space by providing an address bus for the API memory space. This address is incremented from the start address register to the end address register.

?? The Protected resources.

It also can generate:

?? A Global chip reset.

?? A protected resource reset.

?? An opcode prefetch abort.

This reset is initiated on different reset sources:

- ?? Global chip reset request.
- ?? Protected resource reset request.
- ?? Secure watchdog timer reset request (see conditions)
- ?? Soft reset.

7.4.5.4.3 Secure Timer

A secure timer is added in the secure solution. It can be programmed as a secure watchdog timer when a protected space is defined in secure mode. It can be used as a second watchdog timer in normal mode.

The secure timer consists in two parts:

- ?? 16 bits watchdog/general purpose timer
- ?? a wrapper that filters the secure/control signals

7.4.5.4.4 Secure Interrupt Handler

The "main interrupt handler" executes in non-secure mode only, hence cannot access protected-area to service secure interrupts when in secure mode. All interruption sources of the protected resources are then connected to a "secure interrupt handler", whose output defines a unique protected interrupt line. This line is routed to the main interrupt handler as an IRQ (Low priority interrupt request).

The secure interrupt handler provides 5 prioritized and maskable interrupts. Each interrupt is configured as a low level sensitive or falling edge sensitive interrupt and can be individually masked using dedicated configuration registers.

An Interrupt Level Register controlled through the RHEA I/F bus is associated to each incoming interrupt to define a priority to the corresponding interrupt. If several interrupts have the same priority level, they are sent in a predefined order.

7.5 DSP sub-system

7.5.1.1 DSP subchip (M30L154)

The DSP sub-chip is a Digital Signal Processor core compliant with the TMS320C54x family. The CPU core LEAD2 is associated with an ARM Port Interface (API), an interrupt handler, a parallel interface XIO, a Timer, 30K words of RAM including 16K words of API shared memory, 154K words of ROM (mainly 8Kw block), a serial port (VSP), and a JTAG interface.

The cDSP memory footprint is extended with an on-chip 10K words PDRAM memory.

The DSP sub-chip as well as the extended memory operates up to 104MHz; input clock is delivered by the S-O-C's DPLL (After DRP's regeneration).

Note:

The GSM Voice Port is the serial port included within the DSP sub-chip; it is described section **7.4.4.15 Voice Serial Port (VSP)**

7.5.1.2 DSP memory mapping

DARAM: dual access data RAM. It is always mapped in data space and can be overlaid in program space using the OVLY bit.

APIRAM: dual access data RAM. It is always mapped in data space and can be overlaid in program space using the OVLY bit. The ARM host processor via the API interface module can also access this memory. It behaves as a communication memory between the Lead CPU and the ARM host processor.

PROM: program ROM, always in program space.

DROM: data ROM, always in data space.

PDROM: program or data ROM. This ROM is always mapped in program space and can also be mapped in data space by setting the DROM control bit.

Extended PDRAM: Program / Data RAM mapped on both the data space and the program space of the DSP XIO interface

Please see the chapter on DSP interconnect (section: 12.2) for details

7.5.1.3 API shared memory

The API interface offers a dual access capability to 16K words of 16 bits of mixed data program memory.

The API bridge can be configured to manage data access of 8,16 or 32 bits through the API control registers and the memory interface configuration registers.

The API dual access capability is either enabled (SAM mode) or disabled (HOM mode) by the DSP. SAM mode is the default configuration when the DSP exits from a reset phase.

In SAM mode (Shared Access Mode), ARM (or DMA controller) and DSP can both access simultaneously to this shared memory space with ARM access resynchronized on DSP cycle-clock (4+ times ratio required between ARM and DSP cycle clocks).

In HOM mode (Host Only Mode), the API RAM is dedicated to the sole external access under the control of either the ARM or the DMA controller and therefore the access time is not constrained.

7.5.1.4 XIO memory mapping

All the data space is mapped on the **page 0** from the address **0x7800** to **0x87FF**.
A non-overlaid 2KW memory is mapped at address 0x7000.

7.5.1.5 XIO-RHEA

Internal and external peripherals are mapped on XIO or data memory spaces

DSP-RHEA bus peripherals

- ?? Memory-mapped registers &/ FIFO-Buffer memory
- ?? 16/8 bits word size adaptation
- ?? Programmable wait-state access (support up to '0 wait-state access)

Notes:

RHEA-bridge supports the word size adaptation, however, peripherals modules documentation should be consulted to effectively define the word-size supported...

Peripherals mapping to the XIO space is compliant to the CalypsoPlus device; see [4]

Exclusive cDSP functions and Shared (/MCU) functions are available to the DSP via its RHEA bus. These function are mapped on the data-space and/or the I/O-space or both as described in the below list:

Fixed & exclusive to DSP

- ?? Interrupt Handler (INTH), I/O-space
- ?? NMI Status, I/O-space

- ?? XIO controller, I/O-space
- ?? API controller, I/O-space
- ?? A5/1/2/3 Cipher, I/O & Data spaces
- ?? I2C (TriTon dedicated), Data-space

Shared MCU/DSP

- ?? UART module, Data-space
- ?? C-Port module, Data-space
- ?? MCSI module, I/O & Data spaces
- ?? DMA channel control. I/O space.
- ?? APC (DRP's Wrapper)
- ?? DRP control & Data, I/O with 1KW double-mapped to data-space (frequently used register, parts of the SP-RAM & Wrapper Cal-RAM)
 - ~~??~~ 128-word /Frequently used registers:TX_DAT (Buffer), ROC_CALCI, ROC_CALCQ, DCXO_XTAL
 - ~~??~~ 384-Word internal DRP RAM
 - ~~??~~ 512-Word Wrapper Calibration-RAM

7.5.1.6 DSP Interrupt Handler (INTH).

The DSP interrupt handler can provide 21 interrupts to the DSP core.

Each incoming interrupt can be configured as a low-level sensitive or falling edge sensitive interrupt. The mask and the interruption level of the interrupts are configured in the DSP core itself.

7.5.1.7 DSP interrupts mapping

The DSP sub-chip owns 17 interrupt lines with 11 of which INT0n to INT10n are dedicated for external peripherals.

Note:

8. Software debug

The purpose of this design is to enable software debug with some internal design nodes being available on a debug scope. Since these internal nodes are not normally not available out of silicon, having them mapped to a chip level IO helps in debugging software routines during development testing and debug of a customer returned sample.

Some internal nodes as defined in the document link are mapped to the Locosto IO-pads. To keep the debug module design robust and flexible certain amount of redundancy is intentionally present. The same signal could be present at multiple locations and could be chosen at different pads by programming debug and IO configuration registers. This well defined redundancy enables debug with different observation scenarios which may have different concurrent signal observation requirement. This is helpful as we have limited number of pins which can be dedicated for software debug purpose. In the design implementation, 37 functional pads listed below have been identified for debug. Please note, the normal functionality is no more be available, owing to the debug usage. It is assumed here all software debug operations are performed on a board with reduced functionality.

Debug module is a stand alone module, no external component needed to complete the functionality.

Please refer to [cf document 8] for details of usage.

9. RF System & DRP2.0's Integration

Locosto integrates an RF transceiver subchip based on the Digital Radio Processor (DRP) architecture. The DRP subchip in its main embodiment of a GSM transceiver is designed for dual band operation in both Europe and the US. In Europe, this corresponds to the E-GSM 900 and DCS 1800 bands, while in the US it is the GSM 850 and PCS 1900 bands. The US or European region of operation is hardware selectable by altering the LNA matching circuit. The transmitter is based on a frequency synthesizer with a direct frequency/phase modulation capability. The frequency synthesizer is implemented as an All Digital PLL (ADPLL) loop. The receiver is based on a near-zero IF architecture. A common ADPLL is used to generate the transmit signal and the receiver LO.

Please refer to [cf document 6] for more information on DRP2 operation and usage.

10. Automatic Power Control

The purpose of this design is to control the external Power Amplifier when the DRP2 is transmitting Tx frames. The automatic power control (APC) generates an envelope signal to control the power ramp up, power ramp down, and power level of the radio burst. The APC structure is intended to support single-slot and multi-slot transmission with smooth power transition when consecutive bursts are transmitted at different power levels.

11. LoCosto-IC Power Management

The TriTon ABB chip is the power-management companion-chip in charge for sequencing LoCosto-IC power on/off sequences. For detailed description Please refer to [cf document 2] & [cf document 7].

The LoCosto IC has separate power domains for:

- ?? DBB Core (VDD_DBB)
- ?? DPLL Sub-chip (VDD_DPLL)
- ?? APLL Sub-chip (VDD_APLL)
- ?? DRP_VR1 Domain (VDD_RFV1)
- ?? DRP_VR2 Domain (VDD_RFV2)
- ?? APC module (VDD_APC)
- ?? Memory I/O Bus (VDD_MIF)
- ?? Reset Input Cell (VDD_RST)
- ?? USIM I/O Bus (VDD_USIM)
- ?? I/O's "all others" (VDD_IOs)

The Table here after summarizes the Power-Supply connection TriTon / LoCosto. TriTon power source's listed are the value applying to the LoCosto-CS configuration.

TriTon Power Sources			LoCosto_IC Power Domains		
LDO Source	Typical Voltage (Volt)	Max. Current Delivered (mA)	Power domain	Typical operating voltage (Volt)	Active mode (1.3v) Estimate Current Consumption (mA)
VREXTL	1.3 & 1.05	200	VDD_DBB VDD_RST	1.3 1.3	140(72,35,18,10,5) (~ µA)
VRPLL	1.3 & 1.05	10	VDD_DPLL VDD_APLL	1.3 1.3	1 0.5
VRMMC	2.8	100	VDD_RFV1 VDD_APC	2.85 2.85	60 6
VREXTH	2.8	100	VDD_RFV2	2.85	10
VRMEM	1.8	200	VDD_MIF	1.8	10
VRSIM	1.8 / 2.8	15	VDD_USIM	2.85	3
VRIO	1.8	200 (30/TriTon)	VDD_IOs	1.8	45
VRABB	2.8	80 (40/TriTon)	N/A		
VRRTC	1.8	20 (10/TriTon)	N/A		
VRUSB	3.3	15	N/A		
VRVBUS	5.0	60	N/A		
VRDBB	0.95 -1.4	850	N/A		

Table 31: TriTon / LoCosto Power Supply

12. Appendix

12.1 Detailed description of MCU Interconnect

12.1.1 ARM memory map

ARM memory space is shared between:

- ?? External Memory space
- ?? Internal Memory space
- ?? Internal memory like peripherals
- ?? DSP Shared Memory space (API memory)
- ?? RHEA Bus space

Boot Area [0000:0000 - 003F:FFFF]

Device name	Start address	Stop address	Size	Unit	Data access	Device access
Boot ROM	0000:0000	0000:FFFF	64	KB	8/16/32 R	32
<i>Reserved</i>	<i>0001:0000</i>	<i>003F:FFFF</i>	<i>4032</i>	<i>KB</i>	<i>---</i>	<i>---</i>

External Memory [000:0000-17FF:FFFF]

Device Name	Start address	Stop address	Size	Unit	Data access	Device access
External memory	0040:0000	07FF:FFFF	124	MB	8/16/32 RW	32

Internal Memory [0800:0000 - 08FF:FFFF]

Device name	Start address	Stop address	Size	Unit	Data access	Device access
Internal RAM (2.5Mb)	0800:0000	0804:FFFF	320	KB	8/16/32 RW	32
Internal ROM (1.5Mb)	0805:0000	0807:FFFF	192	KB	8/16/32 R	32
<i>Reserved</i>	<i>0808:0000</i>	<i>08FF:FFFF</i>	<i>15.5</i>	<i>MB</i>	<i>---</i>	<i>---</i>

Internal memory like Peripherals [0900:0000 - 0FFF:FFFF]

Device name	Start address	Stop address	Size	Unit	Data access	Device access
Boot ROM	0900:0000	0900:FFFF	64	KB	8/16/32 R	32
<i>Reserved</i>	<i>0901:0000</i>	<i>096F:FFFF</i>	<i>7104</i>	<i>KB</i>	<i>---</i>	<i>---</i>
Camera	0970:0000	097F:FFFF	1.0	MB	32 RW	32[TU37]
SHA1/MD5	0980:0000	0980:007F	1.0	MB	32 RW	32
DES/3DES	0990:0000	0990:007F	1.0	MB	32 RW	32
RNG	09A0:0000	09A0:007F	1.0	MB	32 RW	32
TI use only	09B0:0000	09BF:FFFF	1.0	MB	32 RW	32

TI use only	09C0:0000	09C0:007F	1.0	MB	32 RW	32
NAND Flash	09D0:0000	09DF:FFFF	1.0	MB	8/16/32 RW	32
MSSPI	09E0:0000	09EF:FFFF	1.0	MB	32 RW	32
Debug Unit	09F0:0000	09FF:FFFF	1.0	MB	32 RW	32
Reserved	0A00:0000	0FFF:FFFF	104.0	MB	---	---

API & RHEA [1000:0000 - FFFF:FFFF]

Device name	Start address	Stop address	Size	Unit	Data access	Device access
Reserved	1000:0000	FFCF:FFFF	3.7	GB	---	---
API RAM	FFD0:0000	FFD0:3FFF	16.0	KB	16/32 RW	16
Reserved	FFD0:4000	FFDF:FFFF	1.0	MB	---	---
API control register	FFE0:0000	FFE0:0001	2.0	B	16 RW	16
Reserved	FFE0:0002	FFFD:FFFF	1.9	MB	---	---
RHEA strobe 1	FFFE:0000	FFFE:FFFF	64.0	KB	8/16 RW	16
RHEA strobe 0	FFFF:0000	FFFF:FFFF	64.0	KB	8/16 RW	16

Table 32 Memory split for MCU

12.1.1.1 External memory map

The asynchronous/synchronous **External Memory Inter-Face (EMIF)** supports most common memory interface protocols through a flexible programming and timing signals control.

The EMIF can control up to 4 memory devices for a total address range up to 124-Mbyte (1 x 28-Mbyte + 3 x 32M-byte), without any external adding logic. The number of memory Chip Select signal is configurable from 1 to 4 (default to 2 CS's) and the address bus width is sizable from 22-bit /4M-Byte to 25-bit /32MByte (default to 23-bit /8-MByte).

Each CS's address-space has dedicated Wait-State and/or Dummy-Cycle insertion configuration registers to fulfill protocol and timing constraints of attached memory devices. Elementary Wait-state and Dummy-cycle are referenced to the highest S-O-C clock (DPLL clock-out; @104Mhz max).

The following figure explains the organization of external memory.

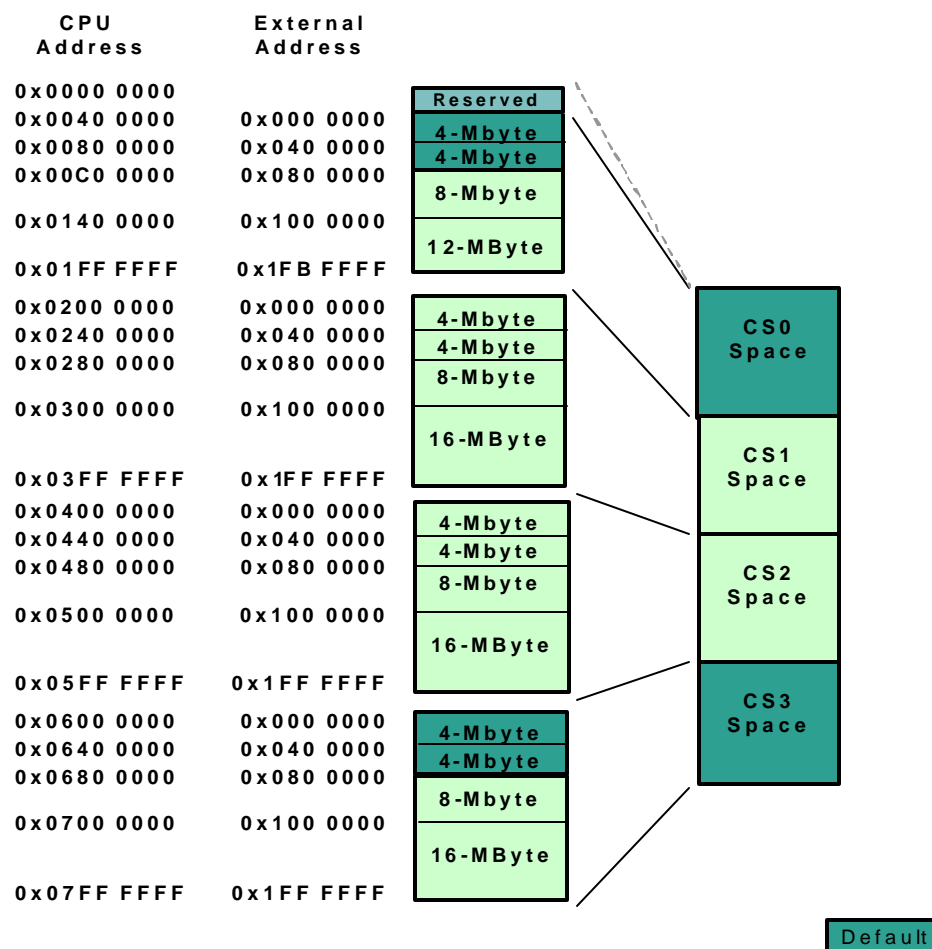


Figure 22 Organization of external memory

12.1.1.2 RHEA strobe 0 peripherals

RHEA strobe 0 peripherals are those which are accessible by both DMA and MCU.

Peripheral Name	Chip select number	Start address	End Address	Size	Access
DRP2 OCP2	CS0	FFFF:0000	FFFF:07FF	2KB	16 bit R/W
	CS1	FFFF:0800	FFFF:0FFF	2KB	16 bit R/W
	CS2	FFFF:1000	FFFF:17FF	2KB	16 bit R/W
	CS3	FFFF:1800	FFFF:1FFF	2KB	16 bit R/W
	CS4	FFFF:2000	FFFF:27FF	2KB	16 bit R/W
	CS5	FFFF:2800	FFFF:2FFF	2KB	16 bit R/W
	CS6	FFFF:3000	FFFF:37FF	2KB	16 bit R/W
	CS7	FFFF:3800	FFFF:3FFF	2KB	16 bit R/W

DRP wrapper internal memory	CS8	FFFF:4000	FFFF:47FF	2KB	16 bit R/W
	CS9	FFFF:4800	FFFF:4FFF	2KB	16 bit R/W
DRP wrapper APC	CS10	FFFF:5000	FFFF:57FF	2KB	16 bit R/W
Reserved	CS11	FFFF:5800	FFFF:5FFF	---	---
Reserved	CS12	FFFF:6000	FFFF:67FF	---	---
Reserved	CS13	FFFF:6800	FFFF:6FFF	---	---
UART/SSW switch	CS14	FFFF:7000	FFFF:77FF	2KB	8 bit R/W
MCSI	CS15	FFFF:7800	FFFF:7FFF	2KB	16 bit R/W
DSW switch	CS16	FFFF:8000	FFFF:87FF	2KB	16 bit R/W
RHEA switch	CS17	FFFF:8800	FFFF:8FFF	2KB	16 bit R/W
TPU RAM	CS18	FFFF:9000	FFFF:97FF	2KB	16 bit R/W
DPLL config	CS19	FFFF:9800	FFFF:9FFF	2KB	16 bit R/W
LCD interface	CS20	FFFF:A000	FFFF:A7FF	2KB	16 bit R/W
USIM interface	CS21	FFFF:A800	FFFF:AFFF	2KB	16 bit R/W
USB	CS22	FFFF:B000	FFFF:B7FF	2KB	16 bit R/W
I2C	CS23	FFFF:B800	FFFF:BFFF	2KB	16 bit R/W
GEA3	CS24	FFFF:C000	FFFF:C7FF	2KB	16 bit R/W
I2C 2	CS25	FFFF:C800	FFFF:CFFF	2KB	16 bit R/W
C-Port Reg	CS26	FFFF:D000	FFFF:D7FF	2KB	16 bit R/W
C-Port FIFO	CS27	FFFF:D800	FFFF:DFFF	2KB	16 bit R/W
BCM	CS28	FFFF:E000	FFFF:E7FF	2KB	16 bit R/W
DMA controller	CS29	FFFF:E800	FFFF:EFFF	2KB	16 bit R/W
TPU registers	CS30	FFFF:F000	FFFF:F7FF	2KB	16 bit R/W
Watch dog timer	CS31	FFFF:F800	FFFF:F87F	128	16 bit R/W
Watch dog timer (Secure)		FFFF:F880	FFFF:F8FF	128	16 bit R/W
Bridge		FFFF:F900	FFFF:F9FF	256	16 bit R/W
INTH		FFFF:FA00	FFFF:FA7F	128	16 bit R/W
INTH (Secure)		FFFF:FA80	FFFF:FAFF	128	16 bit R/W
Memory Interface		FFFF:FB00	FFFF:FBFF	256	16 bit R/W
PRRM		FFFF:FC00	FFFF:FCFF	256	16 bit R/W
CLKM		FFFF:FD00	FFFF:FDFF	256	16 bit R/W
JTAG ID code		FFFF:FE00	FFFF:FE03	4	16 bit R/W
MPU		FFFF:FF00	FFFF:FFFF	256	16 bit R/W

Table 33 RHEA strobe 0 peripherals

Note :

1. There are three RHEA switch modules in the design and they are all available on the CS17. The split up for RHEA switches within CS17 is as follows. The Uart SSW register address is also mentioned below

RHEA Switch for peripheral	CS17	FFFF:8800	FFFF:8FFF	Size	16 bit R/W
Rhea SW APC		FFFF:8800	FFFF:881F	32 Bytes	16 bit R/W
Rhea SW MCSI		FFFF:8820	FFFF:883F	32 Bytes	16 bit R/W
Rhea SW CPORT		FFFF:8840	FFFF:885F	32 Bytes	16 bit R/W
UART SSW	CS14	FFFF:7280	FFFF:7280	16 Bits	16 bit R/W

12.1.1.3 RHEA strobe1 peripherals

RHEA strobe1 peripherals are those which can be accessed only by the MCU and not by DMA.

Peripheral Name	Chip select number	Start address	End Address	Size	Access
Reserved	CS0	FFFE:0000	FFFE:07FF	---	---
TPU 2 OCP	CS1	FFFE:0800	FFFE:0FFF	2KB	16 bit R
Reserved	CS2	FFFE:1000	FFFE:17FF	---	---
Reserved	CS3	FFFE:1800	FFFE:1FFF	---	---
ULPD	CS4	FFFE:2000	FFFE:27FF	2KB	16 bit R/W
Reserved	CS5	FFFE:2800	FFFE:2FFF	---	---
Reserved	CS6	FFFE:3000	FFFE:37FF	---	---
TIMER1	CS7	FFFE:3800	FFFE:3FFF	2KB	16 bit R/W
Reserved	CS8	FFFE:4000	FFFE:47FF	---	---
GPIO	CS9	FFFE:4800	FFFE:4FFF	2KB	16 bit R/W
GPIO1	CS10	FFFE:5000	FFFE:57FF	2KB	16 bit R/W
GPIO2	CS11	FFFE:5800	FFFE:5FFF	2KB	16 bit R/W
Reserved	CS12	FFFE:6000	FFFE:67FF	---	---
TIMER2	CS13	FFFE:6800	FFFE:6FFF	2KB	16 bit R/W
Reserved	CS14	FFFE:7000	FFFE:77FF	---	---
LPG	CS15	FFFE:7800	FFFE:7FFF	2KB	8 bit R/W
PWL	CS16	FFFE:8000	FFFE:87FF	2KB	8 bit R/W
PWT	CS17	FFFE:8800	FFFE:8FFF	2KB	8 bit R/W
Software debug registers	CS18	FFFE:9000	FFFE:97FF	2KB	16 bit R/W
Reserved	CS19	FFFE:9800	FFFE:9FFF	---	---
Reserved	CS20	FFFE:A000	FFFE:A7FF	---	---
Reserved	CS21	FFFE:A800	FFFE:AFFF	---	---
Reserved	CS22	FFFE:B000	FFFE:B7FF	---	---
Keyboard interface	CS23	FFFE:B800	FFFE:BFFF	2KB	16 bit R/W
Reserved	CS24	FFFE:C000	FFFE:C7FF	---	---
Reserved	CS25	FFFE:C800	FFFE:CFFF	---	---
Reserved	CS26	FFFE:D000	FFFE:D7FF	---	---
Reserved	CS27	FFFE:D800	FFFE:DFFF	---	---
Reserved	CS28	FFFE:E000	FFFE:E7FF	---	---
Reserved	CS29	FFFE:E800	FFFE:EFFF	---	---

JTAG ID	CS30	FFFE:F000	FFFE: F001	2B	16 bit R
JTAG_Version		FFFE:F002	FFFE:F003	2B	16 bit R
DieID (63 to 0)		FFFE:F004	FFFE:F00B	8B	16 bit R
Man_pub Key		FFFE:F00C	FFFE:F01B	16B	16 bit R
Calypso Core Config		FFFE:F01C	FFFE:F03F	36B	16 bit R/W
DieID(127 to 64)		FFFE:F040	FFFE:F047	8B	16 bit R
Reserved		FFFE:F048	FFFE:F0FF	---	---
IO conf registers		FFFE:F100	FFFE:F1FF	256B	16 bit R/W
Reserved		FFFE:F200	FFFE:F2FF	---	---
Reserved		FFFE:F300	FFFE:F7FF	---	---
Reserved	CS31	FFFE:F800	FFFF:FFFF	---	---

Table 34 RHEA strobe 1 peripherals

12.1.2 MCU interrupts mapping

The ARM7 owns 2 interrupt lines nIRQ and nFIQ.

The fast interrupt nFIQ is dedicated to the emergency interrupt events related to a system misfunction which could affect the physical integrity of the electronic devices.

All other peripheral interrupts are mapped on the nIRQ.

The MCU interrupt handler supports up to 32 physical interrupt channels IRQ[31:0].

Name	Sense	IRQ	FIQ	Function
IRQ0	Edge	?		Watchdog TIMER interrupt
IRQ1	Edge	?		TIMER1 interrupt
IRQ2	Edge	?		TIMER2 interrupt
IRQ3	Level	?		MCSI RX interrupt MCSI TX Interrupt MCSI frame interrupt MCSI DAI interrupt RHEA switch MCSI interrupt
IRQ4	Edge	?		TPU frame interrupt
IRQ5	Edge	?		TPU page interrupt
IRQ6	Level	?		DRP_DBB_SINTERRUPT
IRQ7	Level	?		UART IRDA/MODEM interrupts UART modem mode - Receiver line status - RX timeout - RHR - THR - Modem status - XOFF special character interrupt - CTS, RTS and DSR UART IRDA mode - RHR - THR - Last byte in RX FIFO - RX overrun - Status FIFO interrupt - TX status - Receiver line status - EOF
IRQ8	Level	?		Keyboard interrupt
IRQ9	Edge	?		DRP_DBB_RX_IRQ
IRQ10	Level	?		Camera Interrupt - FIFO Under flow - FIFO Overflow - FIFO Threshold - FIFO full - FIFO not empty - Shifted synchronization code - False synchronization code - Frame width error - Frame start - Frame End - Line start - Line end[TU38]
IRQ11	Edge	?		ULPD end of gauging interrupt
IRQ12	Level	?		ABB interrupt
IRQ13		?		MSSPI interrupt

IRQ14	Level	?		DMA interrupt
IRQ15	Edge	?		API interrupts (nHINT)
IRQ16		?		GPIO0 interrupt
IRQ17	Level	?		Unused
IRQ18		?		DRP_DBB_TX_IRQ
IRQ19	level	?		ULPD GSM timer
IRQ20	level	?		GEA interrupt
IRQ21	level	?		GPIO1 interrupt
IRQ22	level	?		GPIO2 interrupt
IRQ23				C-PORT (I2S) transmit interrupt C-PORT (I2S) receive interrupt RHEA switch CPORT interrupt
IRQ24	edge	?		USIM interrupt - no answer to reset - character underflow - character overflow - character to transmit - received character
IRQ25	level	?		LCD interrupts - Tx FIFO empty - Status register full
IRQ26	level	?		USB interrupt - DMA transfer completed on Transmit channel #n - completion of DMA transfer from Receive channel #n - End of Transfer (EOT) packet detection on receive channel #n - Start of Frame detected - OUT transaction detected on endpoint #n - IN transaction detected on endpoint #n - Device status change - Setup transaction completed on control endpoint (#0) - OUT transaction detected on control endpoint (#0) - IN transaction detected on control endpoint (#0)
IRQ27	level	?		Unused
IRQ28	level	?		I2C data transfer error / completion (Triton)
IRQ29	level	?		Secure interrupt handler IRQ (see table below)
IRQ30	level	?		I2C data transfer error / completion
IRQ31	level	?		Nand Flash interrupt

Table 35 Interrupt mapping of ARM

12.1.2.1 Secure interrupt handler table

Name	Sense	IRQ	FIQ	Function
SEC_IRQ0	edge	?	N/A	Random Number Generator interrupt
SEC_IRQ1	edge	?	N/A	SHA1MD5 interrupt
SEC_IRQ2	edge	?	N/A	EMPU secure interrupt
SEC_IRQ3	edge	?	N/A	DMA secure interrupt
SEC_IRQ4	edge	?	N/A	Secure TIMER interrupt

Table 36 Interrupt map of secured interrupt handler

12.1.3 DMA map of ARM

The enhanced DMA controller supports 6 logical channels and 4 ports

HW request number	Peripheral name	Request type
1	DRP	TX
2		RX
3	LCD interface	TX
4	UART IRDA/MODEM	TX
5		RX
6	MSSPI	TX
7		RX
8	Unused	TX
9	Unused	RX
10	USB	RX 1
11		TX 1
12		RX 2
13		TX 2
14		RX 3
15		TX 3
16	I2C (Triton)	RX
17		TX
18	Unused	--NA--
19	USIM	RX
20		TX

	Camera DMA request for FIFO threshold Camera DMA request for data remaining in FIFO	
	or	
21	Camera DMA request for data remaining in FIFO[TU39]	----NA----
22	<i>Unused</i>	----NA----
23	<i>Unused</i>	RX/TX
24	NAND flash	RX/TX
25	I2C	RX
26		TX
27	SHA-1	TX
28	DES-3/DES	RX
29		TX
30	C-PORT (I2S)	RX
31		TX

Table 37 DMA channel mapping

Note: TX means data transfer from DMA to Peripheral
RX means data transfer from Peripheral to DMA

12.2 Detailed description of DSP Interconnect

12.2.1 DSP memory mapping

Description of various types of memories in DSP

DARAM: dual access data RAM. It is always mapped in data space and can be overlaid in program space using the OVLY bit.

APIRAM: dual access data RAM. It is always mapped in data space and can be overlaid in program space using the OVLY bit. The ARM host processor via the API interface module can also access this memory. It behaves as a communication memory between the Lead CPU and the ARM host processor.

PROM: program ROM, always in program space.

DROM: data ROM, always in data space.

PDROM: program or data ROM. This ROM is always mapped in program space and can also be mapped in data space by setting the DROM control bit.

PDRAM: program / data RAM mapped on both the data space and the program space of the DSP XIO interface

	Data	Prog0	Prog1	Prog2	Prog3	Prog 4	XI/O						
0000	DARAM 2K												
0800	API 16K												
1000													
1800													
2000													
2800													
3000													
3800													
4000													
4800	DARAM 10K												
5000													
5800													
6000													
6800													
7000													
7800	DARAM 2K	PROM 4K											
	Peripherals on data space												
8000	P	D R O M	PROM 24K	PROM 32K	PROM 32K	PROM 24K		P D R A M 10K					
8800	D												
9000	R												
9800	A												
A000	M 10K												
A800		22K											
B000													
B800													
C000													
C800		PDROM 8K				PROM 8K [TU40]							
D000													
D800													
E000													
E800													
F000													
F800													

Table 38 DSP memory mapping

12.2.1.1 API shared memory

The API interface offers a dual access capability to 16K words of 16 bits of mixed data program memory.

The API bridge can be configured to manage data access of 8,16 or 32 bits through the API control registers and the memory interface configuration registers.

The API dual access capability is either enabled (SAM mode) or disabled (HOM mode) by the DSP. SAM mode is the default configuration when the DSP exits from a reset phase.

In SAM mode (Shared Access Mode), ARM (or DMA controller) and DSP can both access simultaneously to this shared memory space with ARM access resynchronized on DSP cycle-clock (3+? times ratio required between ARM and DSP cycle clocks).

In HOM mode (Host Only Mode), the API RAM is dedicated to the sole external access under the control of either the ARM or the DMA controller and therefore the access time is not constrained.

12.2.1.2 DSP XIO memory mapping

The PDRAM on data space is mapped on the **page 0** from the address 0x8000 to 0xA7FF. The PDRAM is also mapped on page 4 of program space.

12.2.1.3 XIO-RHEA

Internal and external peripherals are mapped on XIO or data memory spaces. These spaces are accessible through nXSTROBE[3:0] with a range of 2KWords for external peripherals allowing to connect up to :

- 6 external devices on program space
- 26 external devices on data space
- 31 external devices on I/O space

Note: 32 bits internal peripherals are directly connected on the internal memory interface.

DSP XIO-RHEA mapping					
Device name		Start address	Stop address	Size in Words	Data
External peripherals mapping - Program space					
Strobe 0					
Not allocated	CS0	0000	07FF	2K	16
...
Not allocated	CS5	3000	37FF	2K	16
External peripherals mapping - Data Space 1					
Strobe 1					
Not allocated	CS6	3800	3FFF	2K	16
...
...
MCSI-1 (DAI)	CS15	7800	787F	128	16
I2C		7880	78FF	128	16

UART/SSW switch ¹		7900	797F	128	16
APC		7980	79FF	128	16
DRP external memory 1		7A00	7A7F	128	16
DRP external memory 2		7A80	7AFF	128	16
DRP internal memory 1		7B00	7B7F	128	16
DRP internal memory 2		7B80	7BFF	128	16
C-PORT (I2S)		7C00	7C7F	128	16
RHEA switch		7C80	7CFF	128	16
Not used		7D00	7DFF	256	16
DRP register1 (TX_DATA)		7E00	7E7F	128	16
DRP register2 (ROC_CALCI)		7E80	7EFF	128	16
DRP register3 (ROC_CALOQ)		7F00	7F7F	128	16
DRP register4 (DCXO_XTAL)		7F80	7FFF	128	16
External peripherals mapping - Data Space 2					
Strobe 2					
Not allocated	CS16	A800	FFFF	2K	16
---	--	---	---	---	---
Not allocated	CS31	F800	FFFF	2K	16
External peripherals mapping -I/O Space					
Strobe 3					
Not allocated	CS0	0000	07FF	2K	16
MCSI-1 (DAI)	CS1	0800	0FFF	2K	16
Not allocated	CS2	1000	17FF	2K	...
Not allocated	CS3	1800	1FFF	2K	...
Not allocated	CS4	2000	27FF	2K	...
A51/2/3	CS5	2800	2FFF	2K	16
Not allocated	CS6	3000	37FF	2K	...
Not allocated	CS7	3800	3FFF	2K	...
Not allocated	CS8	4000	47FF	2K	...
Not allocated	CS9	4800	4FFF	2K	...
Not allocated	CS10	5000	57FF	2K	...
Not allocated	CS11	5800	5FFF	2K	...
Not allocated	CS12	6000	67FF	2K	...
Not allocated	CS13	6800	6FFF	2K	...
Not allocated	CS14	7000	77FF	2K	...
Not allocated	CS15	7800	7FFF	2K	...
DRP OCP2	CS16	8000	87FF	2K	16
	CS17	8800	8FFF	2K	16
	CS18	9000	97FF	2K	16

¹ The Exact SSW address is 0x7940 in the DSP data space

	CS19	9800	9FFF	2K	16
DRP external memory	CS20	A000	A7FF	2K	16
Not allocated	CS21	A800	AFFF	2K	...
...
Not allocated	CS28	E000	E7FF	2K	...
DMA controller	CS29	E800	FFFF	2K	16
<i>Not allocated</i>	CS30	F000	F7FF	2K	16
XIO-RHEA bridge	CS31	F800	F8FF	256	16
API Control		F900	F9FF	256	16
INTH		FA00	FAFF	256	16
NMI St Reg		FB00	FBFF	256	16
<i>Not allocated</i>		FC00	FFFF	1K

Table 39 DSP XIO memory space

Note :

1. There are three RHEA switch modules in the design and they are all available on the DSP data space. The exact address are mentioned below

Rhea Switch	Star Address	End Address	Total space
Rhea SW APC	7C80	7C81	32 Bits
Rhea SW MCSI	7CA0	7CA1	32 Bits
Rhea SW CPORT	7CC0	7CC1	32 Bits

12.2.2 DSP interrupt map

The DSP sub chip owns 17 interrupt lines with 11 of which INT0n to INT10n are dedicated for external peripherals. These interrupts are mapped as follows:

Name	Sense	DSP INT	Function
RSN	Level	RSN	DSP sub-system reset (HW or SW)
nMIN		nMIN	Abort on Rhea bus
	Edge	INT0n	Drp_dbb_rx_int
	Edge	INT1n	Drp_dbb_tx_int
	Level		Drp_dbb_sinterrupt
		INT2n	UART IRDA/MODEM interrupts UART modem mode - Receiver line status - RX timeout - RHR - THR - Modem status - XOFF special character interrupt

			<ul style="list-style-type: none"> - CTS, RTS and DSR - UART IRDA mode - RHR - THR - Last byte in RX FIFO - RX overrun - Status FIFO interrupt - TX status - Receiver line status - EOF
TINT		TINT	Timer interrupt
RINT		RINT	SPI receive interrupt
XINT		XINT	SPI transmit interrupt
	Level	INT3n	MCSI-1 receive interrupt
	Level	INT4n	MCSI-1 transmit interrupt
	Level	INT5n	MCSI-1 frame duration error interrupt RHEA switch MCSI interrupt
	Level	INT6n	MCSI-1 DAI interrupt C-PORT (I2S) transmit interrupt C-PORT (I2S) receive interrupt RHEA switch CPORT interrupt
	Edge	INT7n	CYPHER interrupt <ul style="list-style-type: none"> - end of ciphering process - error of processing
	Edge	INT8n	TPU frame interrupt
AINT		AINT	API interrupts
	Edge	INT9n	TPU programmable interrupt
	Level	INT10n	DMA interrupt
	Level	INT11n	I2C error/completion interrupt

Table 40 DSP Interrupt map

12.3 241ZPH ball mapping

BGA Address	Lead Number	BGA Name	DIR	Mode0	Mode1	Mode2	Mode3	
T2	1	trstn	I	trstn				
M6	2	gpio_0	IO	gpio_0	dcd_txir	cam_d_1		
U2	3	spare_2	IO	spare_2				
K8	4	gpio_1	IO	gpio_1	pwt	pmc_reset		
T3	5	gpio_2	IO	gpio_2	pwl	pmc_clk		
U3	6	vdd_io	P	vdd_io	vdd_io	vdd_io	vdd_io	
R4	7	i2c_scl	IO	i2c_scl				
N6	8	i2c_sda	IO	i2c_sda				
T4	9	usb_rcv	I	usb_rcv	uart_cts			
L8	10	usb_se0	IO	usb_se0	uart_tx			
R5	11	usb_dat	IO	usb_dat	uart_rx			
M7	12	usb_txen	O	usb_txen	uart_rts			
N7	13	scl_trit	IO	scl_trit				
R6	14	sda_trit	IO	sda_trit				
K9	16	vfsrx	I	vfsrx				
U5	15	vss	P	vss	vss	vss	vss	
M8	18	vdr	I	vdr				
T6	19	vdv	O	vdv				
U6	17	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
R7	21	vclkrx	I	vclkrx				
P8	22	abb_irq	IO	abb_irq				
U7	20	vdd_io	P	vdd_io	vdd_io	vdd_io	vdd_io	
T7	24	ck13mhz_en	I	ck13mhz_en				
N8	26	ckout_13mhz	O	ckout_13mhz				
U8	23	vss	P	vss	vss	vss	vss	
R8	27	wakeup_req	O	wakeup_req				
T8	25	ckin_32khz	I	ckin_32khz				
M9	28	csync	IO	csync				
P9	29	csclk	IO	csclk	dpll_led_clkref			
T9	30	cdo	O	cdo				
R9	31	gpio_4	IO	gpio_4	cdi	tspace_9	lt2	

N9	32	gpio_5	IO	gpio_5	tspect_8			
T10	33	usb_boot	IO	usb_boot	gpio_3	lpg		
R10	34	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
N10	36	on_noff	I	on_noff				
U10	35	vdd_rst	P	vdd_rst	vdd_rst	vdd_rst	vdd_rst	
T11	37	sim_pbias	IO	sim_pbias				
P10	42	sim_clk	O	sim_clk				
U11	39	vsspbias	P	vsspbias	vsspbias	vsspbias	vsspbias	
R11	40	sim_io	IO	sim_io				
T12	41	vdd_usim	P	vdd_usim	vdd_usim	vdd_usim	vdd_usim	
U12	44	vss	P	vss	vss	vss	vss	
M10	43	sim_pwrctrl	O	sim_pwrctrl				
N11	38	sim_rst	O	sim_rst				
U13	45	apc_vdo	P	apc_vdo	apc_vdo	apc_vdo	apc_vdo	
R12	46	apcldofilter	IO	apcldofilter				
L9	47	apcspare1	IO	apcspare1				
M11	48	apcout	IO	apcout				
R13	49	apcvref	IO	apcvref				
N13	50	apc_vss	P	apc_vss	apc_vss	apc_vss	apc_vss	
T14-R14	51	vss	P	vss	vss	vss	vss	
T17	52	anatst1	IO	anatst1				
U17	53	anatst2	IO	anatst2				
U15	54	xanatst3	IO	xanatst3				
U16	55	xanatst4	IO	xanatst4				
T16	56	xanatst5	IO	xanatst5				
R17	57	xanatst6	IO	xanatst6				
M13-N15	58	vssa	P	vssa	vssa	vssa	vssa	
P15-P16	59	vdda1	P	vdda1	vdda1	vdda1	vdda1	
P15-P16	60	vdda	P	vdda	vdda	vdda	vdda	
T15	61	vddr1rx1	P	vddr1rx1	vddr1rx1	vddr1rx1	vddr1rx1	
M13-N15	62	vssa	P	vssa	vssa	vssa	vssa	
M13-N15	63	vssa	P	vssa	vssa	vssa	vssa	
R16	64	vref1	I	vref1				
R15	65	iref	O	iref				
P15-P16	66	vdda2	P	vdda2	vdda2	vdda2	vdda2	
M13-N15	67	vssa2	P	vdda2	vdda2	vdda2	vdda2	

M13-N15	68	vssa2	P	vssa2	vssa2	vssa2	vssa2	
M15-L13-K14-K15-L15	69	vssrf	P	vssrf	vssrf	vssrf	vssrf	
N17	70	rxgsmm	I	rxgsmm				
M15-L13-K14-K15-L15	71	vsslbm	P	vsslbm	vsslbm	vsslbm	vsslbm	
M16	72	rxegsmm	I	rxegsmm				
L16	73	rxegsmp	I	rxegsmp				
M15-L13-K14-K15-L15	74	vsslbp	P	vsslbp	vsslbp	vsslbp	vsslbp	
M17	75	rxgsmp	I	rxgsmp				
M15-L13-K14-K15-L15	76	vssrf	P	vssrf	vssrf	vssrf	vssrf	
M15-L13-K14-K15-L15	77	vsshbp	P	rxdcsp				
L17	78	rxdcsp	I	vsshbp	vsshbp	vsshbp	vsshbp	
K16	79	rxpcsp	I	rxpcsp				
J16	80	rxpcsm	I	rxpcsm				
M15-L13-K14-K15-L15	81	vsshbm	P	vsshbm	vsshbm	vsshbm	vsshbm	
K17	82	rxdcsm	I	rxdcsm				
M15-L13-K14-K15-L15	83	vssrf	P	vssrf	vssrf	vssrf	vssrf	
H17	84	vddrf	P	vddrf	vddrf	vddrf	vddrf	
J14-J15-H15	85	vssosc	P	vssosc	vssosc	vssosc	vssosc	
J14-J15-H16	86	vssosc	P	vssosc	vssosc	vssosc	vssosc	
J14-J15-H17	87	vssosc	P	vssosc	vssosc	vssosc	vssosc	
H16	88	vddosc	P	vddosc	vddosc	vddosc	vddosc	
J14-J15-H17	89	vssosc	P	vssosc	vssosc	vssosc	vssosc	
J14-J15-H17	90	vssosc	P	vssosc	vssosc	vssosc	vssosc	
H16	91	vddosc	P	vddosc	vddosc	vddosc	vddosc	
H16	92	vddosc1	P	vddosc1	vddosc1	vddosc1	vddosc1	
F16	93	vddr1tx1	P	vddr1tx1	vddr1tx1	vddr1tx1	vddr1tx1	
G17	94	txhb	O	txhb				
H14-G15	95	vssrf1	P	vssrf1	vssrf1	vssrf1	vssrf1	
F17	96	txlb	O	txlb				
G16	97	vddrf1	P	vddrf1	vddrf1	vddrf1	vddrf1	
F16	98	vddr1tx2	P	vddr1tx2	vddr1tx2	vddr1tx2	vddr1tx2	
E17	99	vref	O	vref				
F15	100	vddr2	P	vddr2	vddr2	vddr2	vddr2	
E15	101	vssx	P	vssx	vssx	vssx	vssx	
D15	102	xtal	I	xtal				

D16	103	vddx	P	vddx	vddx	vddx	vddx	
C17	104	vss	P	vss	vss	vss	vss	
G11	105	kbc_0	O	kbc_0	test_port_17			
C16	106	kbc_1	O	kbc_1	test_port_18			
A17	107	vpp	P	vpp	vpp	vpp	vpp	
E13	108	kbc_2	O	kbc_2	test_port_15			
C15	109	kbc_3	O	kbc_3	test_port_14			
B17	110	vpp	P	vpp	vpp	vpp	vpp	
B16	111	i_force	I	i_force				
F12	112	tspact_11	IO	tspact_11	clkm_clk			
A16	113	sense	O	sense				
H10	114	tspact_12	IO	tspact_12				
B15	115	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
A15	116	vdd_io	P	vdd_io	vdd_io	vdd_io	vdd_io	
C14	117	tspact_13	IO	tspact_13				
E12	118	tspact_14	IO	tspact_14				
B14	119	vss_pll	P	vss_pll	vss_pll	vss_pll	vss_pll	
G10	120	tspact_15	IO	tspact_15				
C13	121	vdd_pll	P	vdd_pll	vdd_pll	vdd_pll	vdd_pll	
F11	122	kbr_0	IO	kbr_0	test_port_22			
E11	123	kbr_1	IO	kbr_1	test_port_21			
C12	124	kbr_2	IO	kbr_2	test_port_20			
H9	125	kbr_3	IO	kbr_3	test_port_19			
A13	126	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
F10	127	kbr_4	IO	kbr_4	gpio_8	test_port_18		
B12	128	kbc_4	IO	kbc_4	gpio_9	test_port_13		
A12	129	vss	P	vss	vss	vss	vss	
C11	130	nemu0	IO	nemu0	gpio_10			
D10	131	nemu1	IO	nemu1	gpio_11			
A11	132	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
B11	133	gpio_12	IO	gpio_12	lpg	tspact_10		
E10	134	gpio_13	IO	gpio_13	lcd_ncs0			
A10	135	vss	P	vss	vss	vss	vss	
C10	136	lcd_nrst	IO	lcd_nrst	test_port_12			
B10	137	lcd_stb	IO	lcd_stb	gpio_14	test_port_11		
F9	138	lcd_rnw	IO	lcd_rnw	gpio_15	test_port_10		
D9	139	lcd_rs	IO	lcd_rs	gpio_16	test_port_9		
B9	140	gpio_17	IO	gpio_17	lcd_ncs1	test_port_8		

C9	141	vdd_io	P	vdd_io	vdd_io	vdd_io	vdd_io	
E9	142	lcd_data_0	IO	lcd_data_0	cam0_d_0	test_port_7	ndf_dyn_0	
B8	143	lcd_data_1	IO	lcd_data_1	cam0_d_1	test_port_6	ndf_dyn_1	
C8	144	lcd_data_2	IO	lcd_data_2	cam0_d_2	test_port_5	ndf_dyn_2	
E8	145	lcd_data_3	IO	lcd_data_3	cam0_d_3	test_port_4	ndf_dyn_3	
A8	146	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
B7	147	lcd_data_4	IO	lcd_data_4	cam0_d_4	test_port_3	ndf_dyn_4	
D8	148	lcd_data_5	IO	lcd_data_5	cam0_d_5	test_port_2	ndf_dyn_5	
A7	149	vss	P	vss	vss	vss	vss	
C7	150	lcd_data_6	IO	lcd_data_6	cam0_d_6	test_port_1	ndf_dyn_6	
B6	151	lcd_data_7	IO	lcd_data_7	cam0_d_7	test_port_0	ndf_dyn_7	
A6	152	gpio_18	IO	gpio_18	nd_we			
F8	153	gpio_19	IO	gpio_19	cam_hs	cam_d_3	test_port_32	
E7	154	gpio_20	IO	gpio_20	cam_vs	cam_d_3	test_port_31	
A5	155	gpio_21	IO	gpio_21	cam_lclk	test_port_30		
C6	156	gpio_22	IO	gpio_22	cam_xclk	cam_d_3	test_port_29	
G9	157	gpio_23	IO	gpio_23	spi_clk			
F7	158	gpio_24	IO	gpio_24	spi_data_miso			
C5	159	gpio_25	IO	gpio_25	spi_data_mosi			
E6	160	gpio_26	IO	gpio_26	spi_ncs0			
G8	161	gpio_27	IO	gpio_27	spi_ncs1			
B4	162	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	
C4	163	gpio_28	IO	gpio_28	spi_ncs2	ndf7	cam_d_7	dpl
A3	164	vdd_io	P	vdd_io	vdd_io	vdd_io	vdd_io	
G7	165	gpio_29	IO	gpio_29	bu	ndf6	cam_d_6	
B3	166	gpio_30	IO	gpio_30	lt3	ndf5	cam_d_5	
A2	167	tms	I	tms				
D4-E5	168	nd_nwp	IO	nd_nwp	ndf4	cam_d_4	test_port_28	
C3	169	gpio_31	IO	gpio_31	nd_re	test_port_27		
A1	170	tck	I	tck				
B2	171	tdo	O	tdo				
F6	172	gpio_32	IO	gpio_32	nd_cle	test_port_26		
B1	173	tdi	I	tdi				
H8	174	gpio_33	IO	gpio_33	nd_ale	test_port_25		
C2	175	gpio_34	IO	gpio_34	nd_rdy	test_port_24		
C1	176	vss	P	vss	vss	vss	vss	
D3	177	nd_ce1	O	nd_ce1	test_port_23			
F5	178	gpio_35	IO	gpio_35	ncs2	ndf3		

D2	179	gpio_36	IO	gpio_36	ncs1	ndf2		
H7	180	gpio_37	IO	gpio_37	add_23	ndf1		
E3	181	ncs0	IO	ncs0	gpio_38	lt1	tspact_7	
G6	182	gpio_7	IO	gpio_7	nfwf	tspact_7	lt1	
G5	183	gpio_39	IO	gpio_39	add_22	ndf0		
F3	184	add_21	IO	add_21	gpio_6			
J8	185	add_20	O	add_20				
E1	186	vdd_mif	P	vdd_mif	vdd_mif	vdd_mif	vdd_mif	
H6	187	add_19	O	add_19				
F2	188	add_18	O	add_18				
F1	189	add_17	O	add_17				
G3	190	add_16	O	add_16				
H4	191	add_data_15	IO	add_data_15				
G1	192	add_data_14	IO	add_data_14				
G2	193	add_data_13	IO	add_data_13				
H5	194	add_data_12	IO	add_data_12				
H1	195	vss	P	vss	vss	vss	vss	
H3	196	add_data_11	IO	add_data_11				
H2	197	add_data_10	IO	add_data_10				
J6	198	add_data_9	IO	add_data_9				
J4	199	add_data_8	IO	add_data_8				
J2	200	add_data_7	IO	add_data_7				
J3	201	add_data_6	IO	add_data_6				
J5	202	add_data_5	IO	add_data_5				
K2	203	add_data_4	IO	add_data_4				
K3	204	add_data_3	IO	add_data_3				
K5	205	add_data_2	IO	add_data_2				
K1	206	vdd_mif	P	vdd_mif	vdd_mif	vdd_mif	vdd_mif	

L2	207	add_data_1	IO	add_data_1				
K4	208	add_data_0	IO	add_data_0				
L1	209	rnw	O	rnw				
L3	210	nbhe	O	nbhe				
M2	211	nble	O	nble				
M1	212	nmoe	O	nmoe				
L5	213	ncs3	O	ncs3				
K6	214	fdp	O	fdp				
N1	215	vdd_dbb	P	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb	vdd_dbb
M3	216	nr dy	IO	nr dy	gpio_40			
J7	217	adv	IO	adv	gpio_41			
L6	218	gpio_42	IO	gpio_42	ckm			
N3	219	gpio_43	IO	gpio_43	mcsi_ck	csc lk_o	test_port_33	
M5	220	gpio_44	IO	gpio_44	mcsi_fs	csync_o	test_port_34	
K7	221	gpio_45	IO	gpio_45	mcsi_tx	cdo	test_port_35	
P2	222	gpio_46	IO	gpio_46	mcsi_rx	test_port_36		
P3	223	uart_tx	O	uart_tx				
R1	224	vss	P	vss	vss	vss	vss	
L7	225	uart_rx	IO	uart_rx				
R2	226	uart_cts	IO	uart_cts				
T1	227	nbscan	I	nbscan				
R3	228	rts_sdirda	O	rts_sdirda				
N5	229	gpio_47	IO	gpio_47	dsr_rxir	cam_d_0		
U1	230	spare_3	IO	spare_3				

12.4 Dual Pin Mapping

BGA Address	BGA Name	DIR	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5
M6	gpio_0	IO	gpio_0	dcd_txir	cam_d_1			
K8	gpio_1	IO	gpio_1	pwt	pmc_reset			
T3	gpio_2	IO	gpio_2	pwl	pmc_clk			
T4	usb_rcv	I	usb_rcv	uart_cts				
L8	usb_se0	IO	usb_se0	uart_tx				
R5	usb_dat	IO	usb_dat	uart_rx				
M7	usb_txen	O	usb_txen	uart_rts				
P9	cscclk	IO	cscclk	dpll_led_clkref				
R9	gpio_4	IO	gpio_4	cdi	tspact_9	lt2		
N9	gpio_5	IO	gpio_5	tspact_8				
T10	usb_boot	IO	usb_boot	gpio_3	lpg			
G11	kbc_0	O	kbc_0	test_port_17				
C16	kbc_1	O	kbc_1	test_port_16				
E13	kbc_2	O	kbc_2	test_port_15				
C15	kbc_3	O	kbc_3	test_port_14				
F12	tspact_11	IO	tspact_11	clkm_clk				
F11	kbr_0	IO	kbr_0	test_port_22				
E11	kbr_1	IO	kbr_1	test_port_21				
C12	kbr_2	IO	kbr_2	test_port_20				
H9	kbr_3	IO	kbr_3	test_port_19				
F10	kbr_4	IO	kbr_4	gpio_8	test_port_18			
B12	kbc_4	IO	kbc_4	gpio_9	test_port_13			
C11	nemu0	IO	nemu0	gpio_10				
D10	nemu1	IO	nemu1	gpio_11				
B11	gpio_12	IO	gpio_12	lpg	tspact_10			
E10	gpio_13	IO	gpio_13	lcd_ncs0				
C10	lcd_nrst	IO	lcd_nrst	test_port_12				
B10	lcd_stb	IO	lcd_stb	gpio_14	test_port_11			
F9	lcd_rnw	IO	lcd_rnw	gpio_15	test_port_10			
D9	lcd_rs	IO	lcd_rs	gpio_16	test_port_9			
B9	gpio_17	IO	gpio_17	lcd_ncs1	test_port_8			
E9	lcd_data_0	IO	lcd_data_0	cam0_d_0	test_port_7	ndf_dyn_0		
B8	lcd_data_1	IO	lcd_data_1	cam0_d_1	test_port_6	ndf_dyn_1		
C8	lcd_data_2	IO	lcd_data_2	cam0_d_2	test_port_5	ndf_dyn_2		

E8	lcd_data_3	IO	lcd_data_3	cam0_d_3	test_port_4	ndf_dyn_3		
B7	lcd_data_4	IO	lcd_data_4	cam0_d_4	test_port_3	ndf_dyn_4		
D8	lcd_data_5	IO	lcd_data_5	cam0_d_5	test_port_2	ndf_dyn_5		
C7	lcd_data_6	IO	lcd_data_6	cam0_d_6	test_port_1	ndf_dyn_6		
B6	lcd_data_7	IO	lcd_data_7	cam0_d_7	test_port_0	ndf_dyn_7		
A6	gpio_18	IO	gpio_18	nd_we				
F8	gpio_19	IO	gpio_19	cam_hs	cam_d_3	test_port_32	ndf3	
E7	gpio_20	IO	gpio_20	cam_vs	cam_d_3	test_port_31	ndf3	
A5	gpio_21	IO	gpio_21	cam_lclk	test_port_30			
C6	gpio_22	IO	gpio_22	cam_xclk	cam_d_3	test_port_29	ndf3	
G9	gpio_23	IO	gpio_23	spi_clk				
F7	gpio_24	IO	gpio_24	spi_data_miso				
C5	gpio_25	IO	gpio_25	spi_data_mosi				
E6	gpio_26	IO	gpio_26	spi_ncs0				
G8	gpio_27	IO	gpio_27	spi_ncs1				
C4	gpio_28	IO	gpio_28	spi_ncs2	ndf7	cam_d_7	dpil_led_clkref	
G7	gpio_29	IO	gpio_29	bu	ndf6	cam_d_6		
B3	gpio_30	IO	gpio_30	lt3	ndf5	cam_d_5		
D4-E5	nd_nwp	IO	nd_nwp	ndf4	cam_d_4	test_port_28		
C3	gpio_31	IO	gpio_31	nd_re	test_port_27			
F6	gpio_32	IO	gpio_32	nd_cle	test_port_26			
H8	gpio_33	IO	gpio_33	nd_ale	test_port_25			
C2	gpio_34	IO	gpio_34	nd_rdy	test_port_24			
C1	vss	P	vss	vss	vss	vss	vss	vss
D3	nd_ce1	O	nd_ce1	test_port_23				
F5	gpio_35	IO	gpio_35	ncs2	ndf3			
D2	gpio_36	IO	gpio_36	ncs1	ndf2			
H7	gpio_37	IO	gpio_37	add_23	ndf1			
E3	ncs0	IO	ncs0	gpio_38	lt1	tspace_7	ndf0	
G6	gpio_7	IO	gpio_7	nfw	tspace_7	lt1	ndf2	cam_d_2
G5	gpio_39	IO	gpio_39	add_22	ndf0			
F3	add_21	IO	add_21	gpio_6				
M3	nrty	IO	nrty	gpio_40				
J7	adv	IO	adv	gpio_41				
L6	gpio_42	IO	gpio_42	ckm				
N3	gpio_43	IO	gpio_43	mcsi_ck	csclk_o	test_port_33		
M5	gpio_44	IO	gpio_44	mcsi_fs	csync_o	test_port_34		
K7	gpio_45	IO	gpio_45	mcsi_tx	cdo	test_port_35		

P2	gpio_46	IO	gpio_46	mcsi_rx	test_port_36			
N5	gpio_47	IO	gpio_47	dsr_rxir	cam_d_0			

12.5 Ballout Mapping

		Locosto																NC ball not connected	
		17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
U G	txnb																		
	vddrf1																		
	vssrf1																		
H G																			
J G																			
K G																			
L G																			
M G																			
N G																			
P G																			
R G																			
T G																			
U G																			

F	txlb	vddr1tx1	vddr2	NoBall	NC	tspace_11	kbr_0	kbr_4	lcd_rnw	gpio_19	gpio_24	gpio_32	gpio_35	NoBall	add_21	add_18	add_17
E	vref	NoBall	vssx	NoBall	kbc_2	tspace_14	kbr_1	gpio_13	lcd_data_0	lcd_data_3	gpio_20	gpio_26	nd_nwp	NoBall	nsc0	NoBall	vdd_mif
D	NoBall	vddx	xtal	NoBall	NoBall	NoBall	NoBall	nemu1	lcd_rs	lcd_data_5	NoBall	NoBall	NoBall	Reserved	nd_ce1	gpio_36	NoBall
C	vss	kbc_1	kbc_3	tspace_13	vdd_pll	kbr_2	nemu0	lcd_nrst	vdd_io	lcd_data_2	lcd_data_6	gpio_22	gpio_25	gpio_28	gpio_31	gpio_34	vss
B	vpp	i_force	vdd_dbb	vss_pll	NoBall	kbc_4	gpio_12	lcd_stb	gpio_17	lcd_data_1	lcd_data_4	lcd_data_7	NoBall	vdd_dbb	gpio_30	tms	tck
A	sense	vdd_io	NoBall	vdd_dbb	vss	vdd_dbb	vss	NoBall	vdd_dbb	vss	gpio_18	gpio_21	NoBall	vdd_io	tms	tck	tck

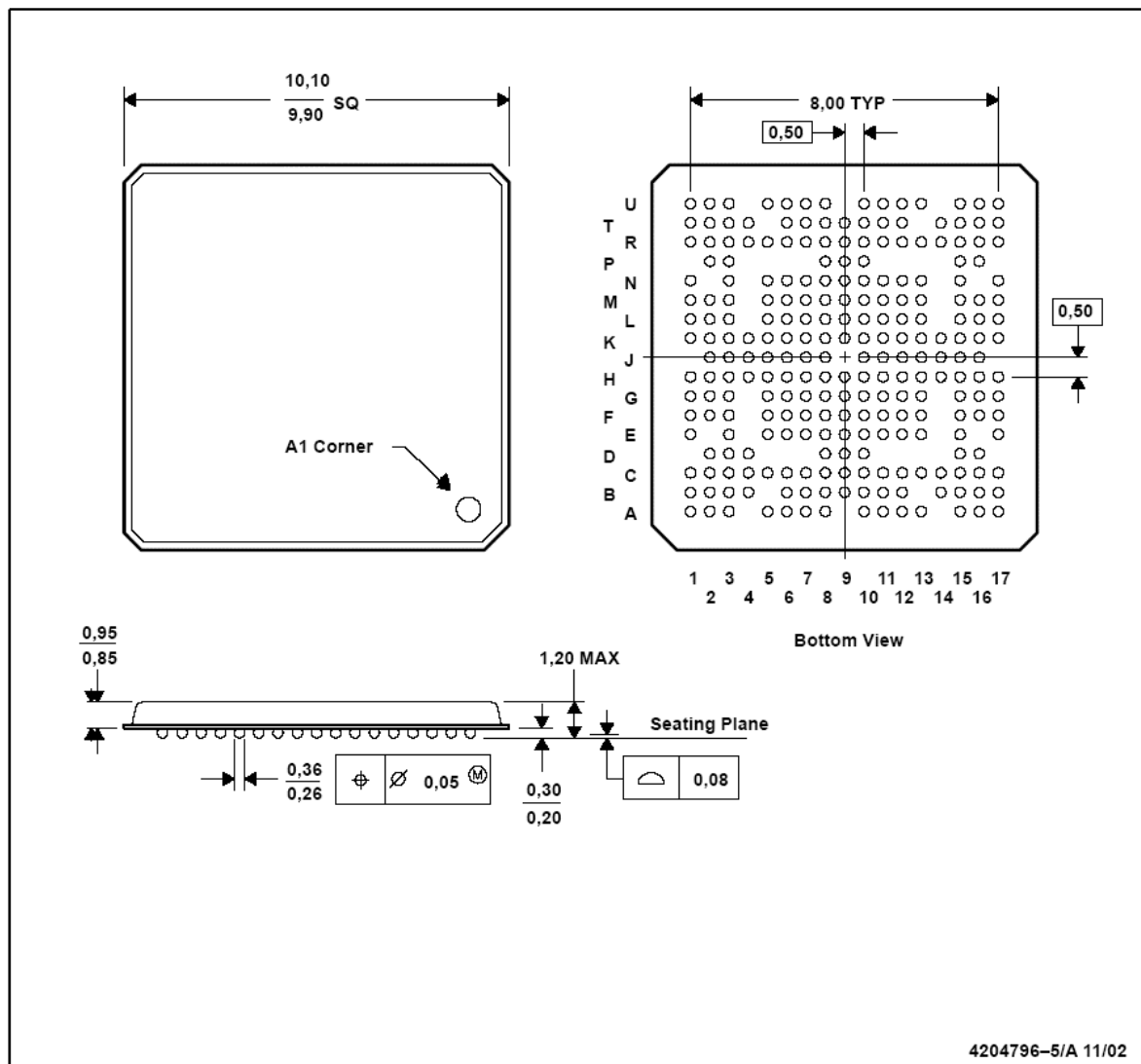
13. LoCosto-IC Package:

The LoCosto_IC package selection is driven by the Digital Radio Processor integration constraints still achieving a low-cost PCB-integration solution.

?? **Series:** ?Star-BGA
 ?? **Balls:** 241
 ?? **Pitch:** 0.50 mm.
 ?? **Height:** 1.20 mm.
 ?? **SQ size:** 10.00x10.00 mm².

ZPH (S-PBGA-N241)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar BGA™ configuration
 - D. This package is lead-free.