

**DATA SHEET**

# SKY77328 iPAC™ PAM for Quad-Band GSM / GPRS

## Applications

- Quad-band cellular handsets encompassing
  - Class 4 GSM850/900
  - Class 1 DCS1800 PCS1900
  - Class 12 GPRS multi-slot operation

## Features

- Low input power range
  - 0 to 6 dBm
- High efficiency
  - GSM850 56%
  - GSM900 56%
  - DCS 54%
  - PCS 53%
- BiCMOS PA controller and interface IC
  - Low power control slope
  - Fast response time
  - Improved control accuracy
- Integrated closed loop power amplifier control
- Internal Icc sense resistor for PAC
- Input/Output matching 50 Ω internal (with DC blocking)
- 20-pin package
- Small outline
  - 6 mm x 6 mm
- Low profile
  - 1.2 mm maximum
- Gold plated, lead-free contacts
- MSL3/250 °C

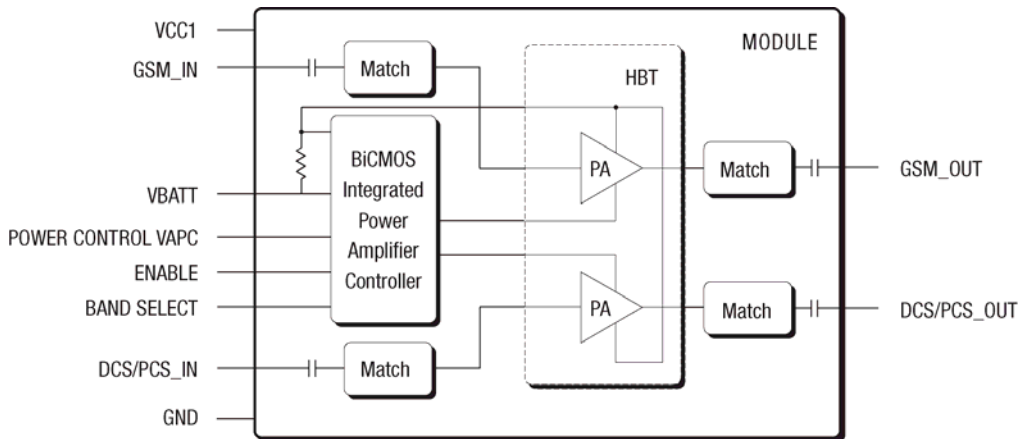
## Description

The SKY77328 Power Amplifier Module (PAM) is designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation.

The module consists of separate GSM850/900 PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50 Ω input and output impedances, and a Power Amplifier Control (PAC) block with an internal current-sense resistor. The custom BiCMOS integrated circuit provides the internal PAC function and interface circuitry. Fabricated onto a single Gallium Arsenide (GaAs) die, one Heterojunction Bipolar Transistor (HBT) PA block supports the GSM850/900 bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current. The GaAs die, the Silicon (Si) die, and the passive components are mounted on a multi-layer laminate substrate. The assembly is encapsulated with plastic overmold.

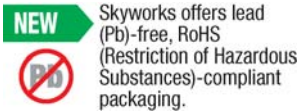
RF input and output ports of the SKY77328 are internally matched to a 50 Ω load to reduce the number of external components for a quad-band design. Extremely low leakage current (2.5 μA, typical) of the dual PA module maximizes handset standby time. The SKY77328 also contains band-select switching circuitry to select GSM (logic 0) or DCS/PCS (logic 1) as determined from the Band Select (BS) signal. In Figure 1 below, the BS pin selects the PA output (DCS/PCS OUT or GSM850/900 OUT) and the Analog Power Control (VAPC) controls the level of output power.

The VBATT pin connects to an internal current-sense resistor and interfaces to an integrated power amplifier control (iPAC™) function, which is insensitive to variations in temperature, power supply, process, and input power. The ENABLE input allows initial turn-on of PAM circuitry to minimize battery drain.



**Figure 1. Functional Block Diagram**

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**Electrical Specifications**

The following tables list the electrical characteristics of the SKY77328 Power Amplifier Module. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Table 3 lists the electrical characteristics of the

SKY77328 for modes GSM850, GSM900, DCS1800, and PCS1900. Figure 2 is a diagram of a typical SKY77328 application.

The SKY77328 is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields. Detailed information on device dimensions, pin descriptions, packaging and handling can be found in later sections of this data sheet.

**Table 1. Absolute Maximum Ratings**

Parameter	Minimum	Maximum	Unit
Input Power (P <sub>IN</sub> )	—	15	dBm
Supply Voltage (V <sub>CC</sub> ), Standby, V <sub>APC</sub> ≤ 0.3 V, ENABLE ≤ 0.2 V	—	7	V
Control Voltage (V <sub>APC</sub> )	-0.5	V <sub>CC_MAX</sub> - 0.2 (See Table 3)	V
Storage Temperature	-55	+150	°C

**Table 2. Recommended Operating Conditions**

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V <sub>CC</sub> )	2.9	3.5	4.8	V
Supply Current (I <sub>CC</sub> )	0	—	2.5	A
Operating Case Temperature (T <sub>case</sub> ) – Package Bottom Surface				°C
1-Slot (12.5% duty cycle)	-20	—	+100	
2-Slot (25.0% duty cycle)	-20	—	+100	
3-Slot (37.5% duty cycle)	-20	—	+85	
4-Slot (50.0% duty cycle)	-20	—	+85	

**Table 3. SKY77328 Electrical Specifications <sup>1</sup> (1 of 9)**

General							
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units	
Supply Voltage	V <sub>CC</sub>	—	2.9	3.5	4.8	V	
Power Control Impedance	Z <sub>APC</sub>	—	—	200	—	kΩ	
ENABLE Control Voltage	V <sub>PE</sub>	Low	—	-0.1	—	0.6	V
		High	—	1.2	—	V <sub>CC</sub>	
ENABLE current	I <sub>PE</sub>	V <sub>PE</sub> ≤ 3.0 V	—	—	30	μA	
Band Select Control Voltage	V <sub>BS</sub>	Low	—	-0.1	—	0.6	V
		High	—	1.2	—	V <sub>CC</sub>	
Band Select Current	I <sub>BS</sub>	V <sub>BS</sub> ≤ 3.0 V	—	—	30	μA	
Standby Mode Leakage Current	I <sub>Q</sub>	V <sub>CC</sub> ≤ 4.5 V V <sub>APC</sub> = 0.1 V ENABLE ≤ 0.2 V T <sub>CASE</sub> = +25 °C P <sub>IN</sub> ≤ -60 dBm	—	2.5	10	μA	
V <sub>APC</sub> Input Filter Bandwidth	V <sub>APC</sub> FBW	—	85	120	150	kHz	
V <sub>APC</sub> Threshold	V <sub>APC</sub> THCL	—	100	150	200	mV	

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (2 of 9)**

GSM850 Mode ( $f = 824 \dots 849$ MHz and $P_{IN} = 0 \dots 6$ dBm)						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Frequency Range	F	—	824	837	849	MHz
Input Power	$P_{IN}$	—	0	3	6	dBm
Analog Power Control Voltage	$V_{APC}$	—	0.2	—	1.7	V
Power Added Efficiency	PAE	$V_{CC} = 3.5$ V $P_{OUT} = 34.5$ dBm ENABLE > 2.0 V pulse width 577 $\mu$ s duty cycle 1:8 $T_{CASE} = +25$ °C	50	56	—	%
2nd...13th Harmonics	$2f_0 \dots 13f_0$	BW = 3 MHz $6.5$ dBm $\leq P_{OUT} \leq 34.5$ dBm	—	-30	-10	dBm
Output Power	$P_{OUT\ MAX}$	$V_{CC} = 3.5$ V $T_{CASE} = +25$ °C	34.5	35.4	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	$V_{CC} = 2.9$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	32.0	33.5	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	$V_{CC} = 4.5$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	32.0	36.4	—	
Input VSWR	$\Gamma_{IN}$	$P_{OUT} = 6.5 \dots 34.5$ dBm, controlled by $V_{APC}$	—	1.5:1	2.3:1	—
Forward Isolation	$P_{OUT\ STANDBY}$	$P_{IN} = 6$ dBm $V_{APC} = 0.1$ V ENABLE $\leq 0.2$ V	—	-45	-35	-dBm
Spurious	Spur	All combinations of the following parameters: $V_{APC} =$ controlled <sup>(2)</sup> $P_{IN} =$ min...max. $V_{CC} = 2.9$ V...4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > -36 dBm			

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (3 of 9)**

GSM850 Mode ( $f = 824...849$ MHz and $P_{IN} = 0...6$ dBm) [continued]						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Load Mismatch	Load	All combinations of the following parameters: $V_{APC} = \text{controlled}^2$ $P_{IN} = \text{min...max.}$ $V_{CC} = 2.9\text{ V...}4.8\text{ V}$ Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise Power	PNOISE	At $f_0 + 20$ MHz RBW = 100 kHz $V_{CC} = 3.5\text{ V}$ $6.5\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$ $T_{CASE} = +25\text{ }^\circ\text{C}$	—	-84	-82	dBm
		At 1805...1880 MHz RBW = 100 kHz $V_{CC} = 3.5\text{ V}$ $6.5\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$ $T_{CASE} = +25\text{ }^\circ\text{C}$	—	-106	-84	
Coupling of Fundamental, 2nd, and 3rd Harmonics from the GSM Band into the DCS/PCS Band	$f_0$	Measured at the DCS/PCS output $-15\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$	—	-3	3	dBm
	$2f_0$		—	-23	-15	
	$3f_0$		—	-22	-17	
Power Control Dynamic Range	Pcdr	—	30	50		dB
Power Control Variation <sup>4</sup> (Control level 5–15) $3.2 \leq V_{CC} \leq 4.5$	Pcv	$P_{OUT} +14.5...+34.5\text{ dBm}, +25\text{ }^\circ\text{C}$	-0.8	—	0.8	dB
Power Control Variation <sup>4</sup> (Control level 16–19)		$P_{OUT} +14.5...+34.5\text{ dBm}$	-1.3	—	1.3	
		$P_{OUT} +6.5...+12.5\text{ dBm}, +25\text{ }^\circ\text{C}$	-1.1	—	1.1	
		$P_{OUT} +6.5...+12.5\text{ dBm}$	-1.7	—	1.7	
Power Control Slope	Pcs	6.5...34.5 dBm	—	—	150	dB/V

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (4 of 9)**

GSM900 Mode ( $f = 880...915$ MHz and $P_{IN} = 0...6$ dBm)						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Frequency Range	$f$	—	880	900	915	MHz
Input Power	$P_{IN}$	—	0	3	6	dBm
Analog Power Control Voltage	$V_{APC}$	—	0.2	—	1.7	V
Power Added Efficiency	PAE	$V_{CC} = 3.5$ V $P_{OUT} = 34.5$ dBm ENABLE > 2.0 V pulse width 577 $\mu$ s duty cycle 1:8 $T_{CASE} = +25$ °C	50	56	—	%
2nd...13th Harmonics	$2f_0...7f_0, 9f_0...13f_0$ $8f_0$	BW = 3 MHz $6.5$ dBm $\leq P_{OUT} \leq 34.5$ dBm	— —	-27 -15	-10 -5	dBm
Output Power	$P_{OUT\ MAX}$	$V_{CC} = 3.5$ V $T_{CASE} = +25$ °C	34.5	35.1	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	$V_{CC} = 2.9$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	32.0	33.3	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	$V_{CC} = 4.5$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	32.0	36.0	—	
Input VSWR	$\Gamma_{IN}$	$P_{OUT} = 6.5...34.5$ dBm, controlled by $V_{APC}$	—	1.5:1	2.3:1	—
Forward Isolation	$P_{OUT\ STANDBY}$	$P_{IN} = 6$ dBm $V_{APC} = 0.1$ V ENABLE $\leq 0.2$ V	—	-45	-35	dBm
Spurious	Spur	All combinations of the following parameters: $V_{APC} =$ controlled <sup>2</sup> $P_{IN} =$ min...max. $V_{CC} = 2.9$ V...4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > -36 dBm			

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (5 of 9)**

GSM900 Mode ( $f = 880\dots915$ MHz and $P_{IN} = 0\dots6$ dBm) [continued]						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Load Mismatch	Load	All combinations of the following parameters: $V_{APC} = \text{controlled}^2$ $P_{IN} = \text{min}\dots\text{max}$ . $V_{CC} = 2.9\text{ V}\dots4.8\text{ V}$ Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise Power	PNOISE	At $f_0 + 20$ MHz RBW = 100 kHz $V_{CC} = 3.5\text{ V}$ $6.5\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$ $T_{CASE} = +25\text{ }^\circ\text{C}$	—	-84	-82	dBm
		At $f_0 + 10$ MHz RBW = 100 kHz $V_{CC} = 3.5\text{ V}$ $6.5\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$ $T_{CASE} = +25\text{ }^\circ\text{C}$	—	-81	-76	
		At 1805...1880 MHz RBW = 100 kHz $V_{CC} = 3.5\text{ V}$ $6.5\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$ $T_{CASE} = +25\text{ }^\circ\text{C}$	—	-106	-84	
Coupling of Fundamental, 2nd, and 3rd Harmonics from the GSM band into the DCS/PCS band	$f_0$	Measured at the DCS/PCS output, $-15\text{ dBm} \leq P_{OUT} \leq 34.5\text{ dBm}$	—	-1	3	dBm
	$2f_0$		—	-25	-17	
	$3f_0$		—	-22	-17	
Power Control dynamic range	P <sub>CDR</sub>	—	30	50	—	dB
Power Control variation <sup>4</sup> (Control level 5–15) $3.2 \leq V_{CC} \leq 4.5$	P <sub>CV</sub>	$P_{OUT} + 14.5\dots+34.5\text{ dBm}$ , $+25\text{ }^\circ\text{C}$	-0.8	—	0.8	dB
		$P_{OUT} + 14.5\dots+34.5\text{ dBm}$	-1.3	—	1.3	
Power Control variation <sup>4</sup> (Control level 16–19)	P <sub>CV</sub>	$P_{OUT} + 6.5\dots+12.5\text{ dBm}$ , $+25\text{ }^\circ\text{C}$	-1.1	—	1.1	dB
		$P_{OUT} + 6.5\dots+12.5\text{ dBm}$	-1.7	—	1.7	
Power Control slope	P <sub>CS</sub>	$6.5\dots34.5\text{ dBm}$	—	—	150	dB/V

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (6 of 9)**

DCS1800 Mode ( $f = 1710...1785$ MHz and $P_{IN} = 0...6$ dBm)						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Frequency range	$f$	—	1710	1750	1785	MHz
Input Power	$P_{IN}$	—	0	3	6	dBm
Analog Power Control voltage	$V_{APC}$	—	0.2	—	1.7	V
Power Added Efficiency	PAE	$V_{CC} = 3.5$ V $P_{OUT} = 32.0$ dBm ENABLE > 2.0 V pulse width 577 $\mu$ s duty cycle 1:8 $T_{CASE} = +25$ °C	48	54	—	%
2nd...7th Harmonics	$2f_0...7f_0$	BW = 3 MHz $1.5$ dBm $\leq P_{OUT} \leq 32.0$ dBm	—	-30	-10	dBm
Output Power	$P_{OUT\ MAX}$	$V_{CC} = 3.5$ V $T_{CASE} = +25$ °C	32.0	33.2	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	$V_{CC} = 2.9$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	29.0	31.4	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	$V_{CC} = 4.5$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	29.0	33.8	—	
Input VSWR	$\Gamma_{IN}$	$P_{OUT} = 1.5...32.0$ dBm, controlled by $V_{APC}$	—	1.5:1	2.0:1	—
Forward isolation	$P_{OUT\ STANDBY}$	$P_{IN} = 6$ dBm $V_{APC} = 0.1$ V ENABLE $\leq 0.2$ V	—	-40	-35	dBm
Spurious	Spur	All combinations of the following parameters: $V_{APC} =$ controlled <sup>3</sup> $P_{IN} =$ min...max. $V_{CC} = 2.9$ V...4.8 V Load VSWR = 8:1, all phase angles	No parasitic oscillation > -36 dBm			

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (7 of 9)**

DCS1800 Mode ( $f = 1710...1785$ MHz and $P_{IN} = 0...6$ dBm) [continued]						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Load Mismatch	Load	All combinations of the following parameters: $V_{APC} = \text{controlled}^3$ $P_{IN} = \text{min...max.}$ $V_{CC} = 2.9 V...4.8 V$ Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise Power	$P_{NOISE}$	At $f_0 + 20$ MHz RBW = 100 kHz $V_{CC} = 3.5 V$ $1.5 \text{ dBm} \leq P_{OUT} \leq 32.0 \text{ dBm}$ $T_{CASE} = +25 \text{ }^\circ\text{C}$	—	-82	-80	dBm
		At 925...960 MHz RBW = 100 kHz $V_{CC} = 3.5 V$ $1.5 \text{ dBm} \leq P_{OUT} \leq 32.0 \text{ dBm}$ $T_{CASE} = +25 \text{ }^\circ\text{C}$	—	-97	-87	
Power Control dynamic range	$P_{CDR}$	—	35	50	—	dB
Power Control variation <sup>4</sup> (Control level 0–8) $3.2 V \leq V_{CC} \leq 4.5 V$	$P_{CV}$	$P_{OUT} +15.5...+32.0 \text{ dBm}, +25 \text{ }^\circ\text{C}$	-1.1	—	1.1	dB
		$P_{OUT} +15.5...+32.0 \text{ dBm}$	-2.0	—	1.2	
		$P_{OUT} +5.5...+13.5 \text{ dBm}, +25 \text{ }^\circ\text{C}$	-1.1	—	1.1	
Power Control variation <sup>4</sup> (Control level 9–13)	$P_{CV}$	$P_{OUT} +5.5...+13.5 \text{ dBm}$	-3.4	—	1.4	
Power Control variation <sup>4</sup> (Control level 14–15)		$P_{OUT} +1.5...+3.5 \text{ dBm}, +25 \text{ }^\circ\text{C}$	-1.4	—	0.8	
Power Control slope	$P_{CS}$	$P_{OUT} +1.5...+3.5 \text{ dBm}$	-4.0	—	2.0	
		$1.5...32.0 \text{ dBm}$	—	—	150	dB/V



**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (8 of 9)**

PCS1900 Mode ( $f = 1850...1910$ MHz and $P_{IN} = 0...6$ dBm)						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Frequency range	F	—	1850	1880	1910	MHz
Input Power	$P_{IN}$	—	0	3	6	dBm
Analog Power Control voltage	$V_{APC}$	—	0.2		1.7	V
Power Added Efficiency	PAE	$V_{CC} = 3.5$ V $P_{OUT} = 32.0$ dBm ENABLE > 2.0 V pulse width 577 $\mu$ s duty cycle 1:8 $T_{CASE} = +25$ °C	48	53	—	%
2nd...7th Harmonics	$2f_0...7f_0$	BW = 3 MHz $1.5$ dBm $\leq P_{OUT} \leq 32.0$ dBm	—	-35	-10	dBm
Output Power	$P_{OUT\ MAX}$	$V_{CC} = 3.5$ V $T_{CASE} = +25$ °C	32.0	32.9	—	dBm
	$P_{OUT\ MAX\ LOW\ VOLTAGE}$	$V_{CC} = 2.9$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	29.0	31.2	—	
	$P_{OUT\ MAX\ HIGH\ VOLTAGE}$	$V_{CC} = 4.5$ V ENABLE > 2.0 V $T_{CASE} = -20$ °C...+100 °C (See Table 2 for multi-slot.) $P_{IN} = 0$ dBm	29.0	33.7	—	
Input VSWR	$\Gamma_{IN}$	$P_{OUT} = 1.5...32.0$ dBm, controlled by $V_{APC}$	—	1.5:1	2.0:1	—
Forward isolation	$P_{OUT\ STANDBY}$	$P_{IN} = 6$ dBm $V_{APC} = 0.1$ V ENABLE $\leq 0.2$ V	—	-40	-35	dBm
Spurious	Spur	All combinations of the following parameters: $V_{APC} =$ controlled <sup>3</sup> $P_{IN} =$ min...max. $V_{CC} = 2.9...4.8$ V Load VSWR = 8:1, phase angles	No parasitic oscillation > -36 dBm			

**Table 3. SKY77328 Electrical Specifications<sup>1</sup> (9 of 9)**

PCS1900 Mode ( $f = 1850...1910$ MHz and $P_{IN} = 0...6$ dBm) [continued]						
Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Load Mismatch	Load	All combinations of the following parameters: $V_{APC} = \text{controlled}^3$ $P_{IN} = \text{min...max.}$ $V_{CC} = 2.9 \text{ V}...4.8 \text{ V}$ Load VSWR = 10:1, all phase angles	No module damage or permanent degradation			
Noise Power	PNOISE	At $f_0 + 20$ MHz RBW = 100 kHz $V_{CC} = 3.5 \text{ V}$ $1.5 \text{ dBm} \leq P_{OUT} \leq 32.0 \text{ dBm}$ $T_{CASE} = +25 \text{ }^\circ\text{C}$	—	-82	-80	dBm
		At 869...894 MHz RBW = 100 kHz $V_{CC} = 3.5 \text{ V}$ $1.5 \text{ dBm} \leq P_{OUT} \leq 32.0 \text{ dBm}$ $T_{CASE} = +25 \text{ }^\circ\text{C}$	—	-97	-87	
Power Control dynamic range	PCDR	—	35	50	—	dB
Power Control variation <sup>4</sup> (Control level 0–8) $3.2 \text{ V} \leq V_{CC} \leq 4.5 \text{ V}$	PCV	$P_{OUT} +15.5...+32.0 \text{ dBm}, +25 \text{ }^\circ\text{C}$	-1.1	—	1.1	dB
		$P_{OUT} +15.5...+32.0 \text{ dBm}$	-2.0	—	1.2	
Power Control variation <sup>4</sup> (Control level 9–13)	PCV	$P_{OUT} +5.5...+13.5 \text{ dBm}, +25 \text{ }^\circ\text{C}$	-1.1	—	1.1	dB
		$P_{OUT} +5.5...+13.5 \text{ dBm}$	-3.4	—	1.4	
Power Control variation <sup>4</sup> (Control level 14–15)	PCV	$P_{OUT} +1.5...+3.5 \text{ dBm}, +25 \text{ }^\circ\text{C}$	-1.4	—	0.8	dB
		$P_{OUT} +1.5...+3.5 \text{ dBm}$	-4.0	—	2.0	
Power Control slope	Pcs	$1.5...32.0 \text{ dBm}$	—	—	150	dB/V

<sup>1</sup> Unless specified otherwise:

$T_{CASE} = -20 \text{ }^\circ\text{C}$  to max. operating temperature (see Table 2)

$R_L = 50 \text{ } \Omega$

pulsed operation with pulse width  $\leq 1154 \text{ } \mu\text{s}$  and duty cycle  $\leq 2:8$

$V_{CC} = 2.9 \text{ V}...4.8 \text{ V}$ .

<sup>2</sup>  $I_{CC} = 0\text{A}$  to  $x\text{A}$ , where  $x$  = current at  $P_{OUT} = 34.5 \text{ dBm}$ ,  $50 \text{ } \Omega$  load, and  $V_{CC} = 3.5 \text{ V}$ .

<sup>3</sup>  $I_{CC} = 0\text{A}$  to  $x\text{A}$ , where  $x$  = current at  $P_{OUT} = 32.0 \text{ dBm}$ ,  $50 \text{ } \Omega$  load, and  $V_{CC} = 3.5 \text{ V}$ .

<sup>4</sup> Power control variation is measured by comparing Power obtained at a specified control voltage over all conditions, against the power obtained with the same control voltage at nominal conditions. For this module, nominal conditions are defined as:

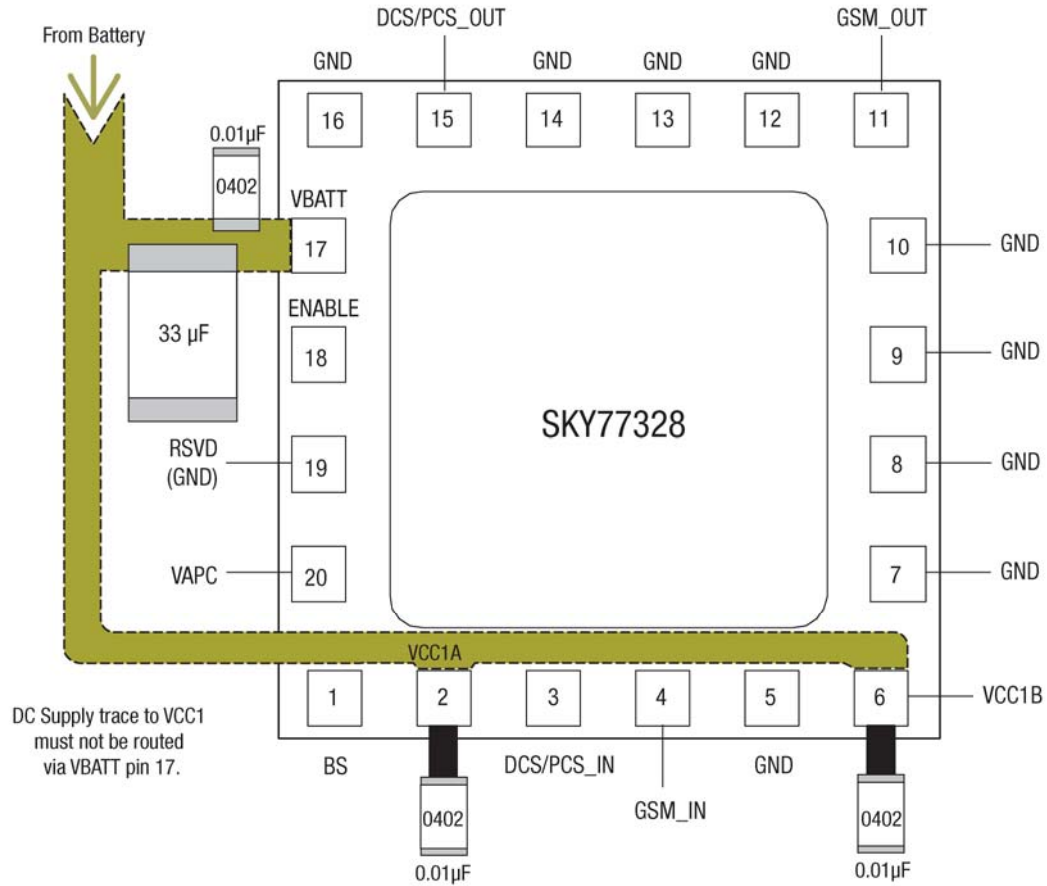
$T = 25 \text{ }^\circ\text{C}$

$V_{CC} = 3.5 \text{ V}$

$P_{IN} = 3 \text{ dBm}$

Frequency = mid-band

Place 0402 and 33  $\mu$ F caps as close as possible to the VBATT pin with the 0402 closer to the pin.



NOTES:

1. The value of 33  $\mu$ F cap depends on the noise level on the phone board.
2. Depending on phone board noise level, not all 0402 and 0.01  $\mu$ F caps may be needed.
3. Ensure sufficient numbers of vias connect VBATT pin to battery trace.
4. VBATT trace should be <sup>3</sup> 1.0 mm.
5. Ensure sufficient numbers of vias connect VCC1A and B to battery trace.
6. VCC1A and VCC1B trace widths should be <sup>3</sup> 0.25 mm.
7. Ground terminals of all bypass caps are connected to ground plane with vias.
8. Dotted traces can be routed in the inner layers.

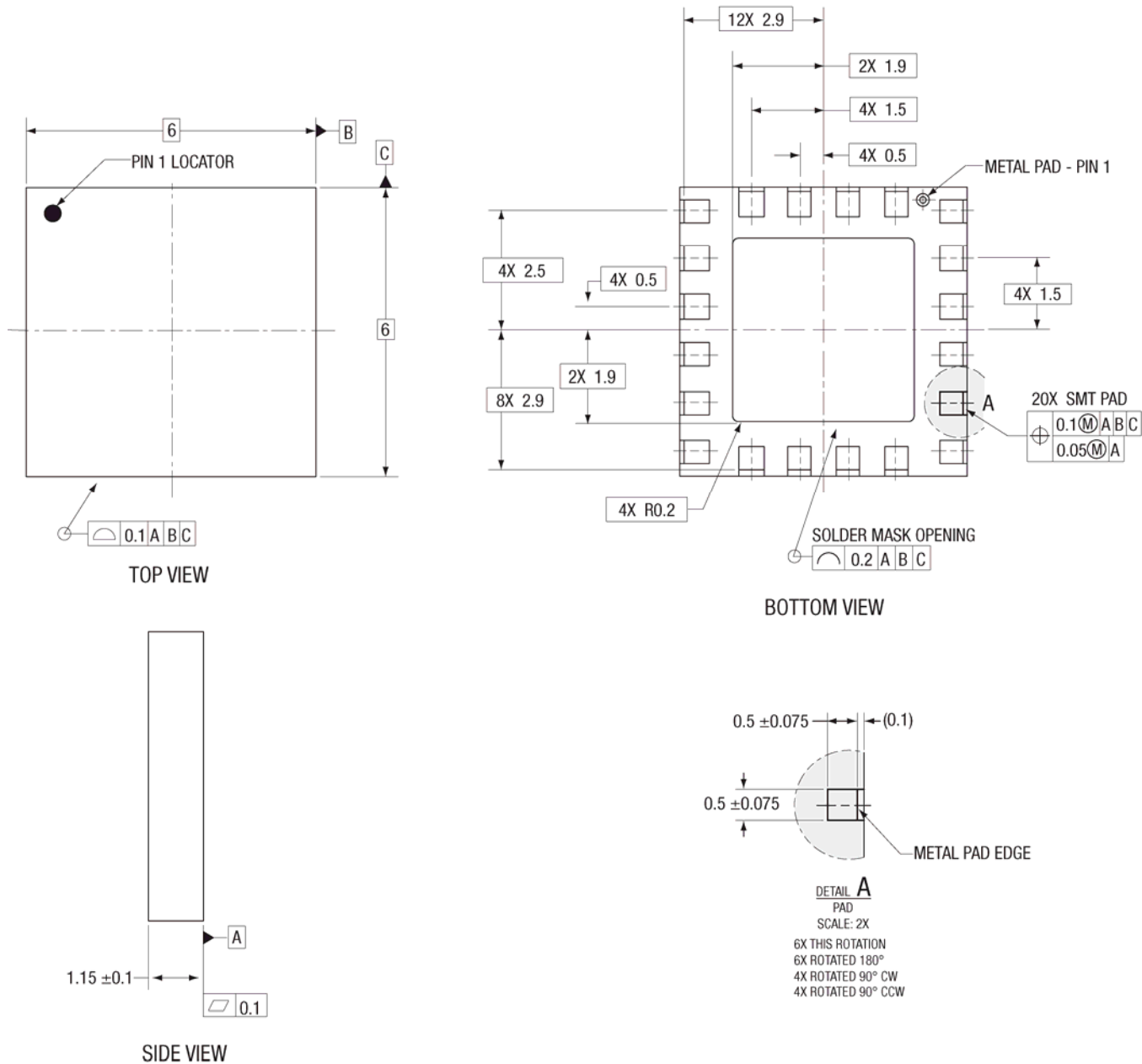
103237\_002

**Figure 2. Typical SKY77328 PAM Application**

**Package Dimensions**

Figure 3 is a mechanical diagram of the pad layout for the SKY77328, a 20-pin leadless quad-band PA module. Figure 4 provides a recommended phone board layout footprint for the

PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50 ohm terminals.

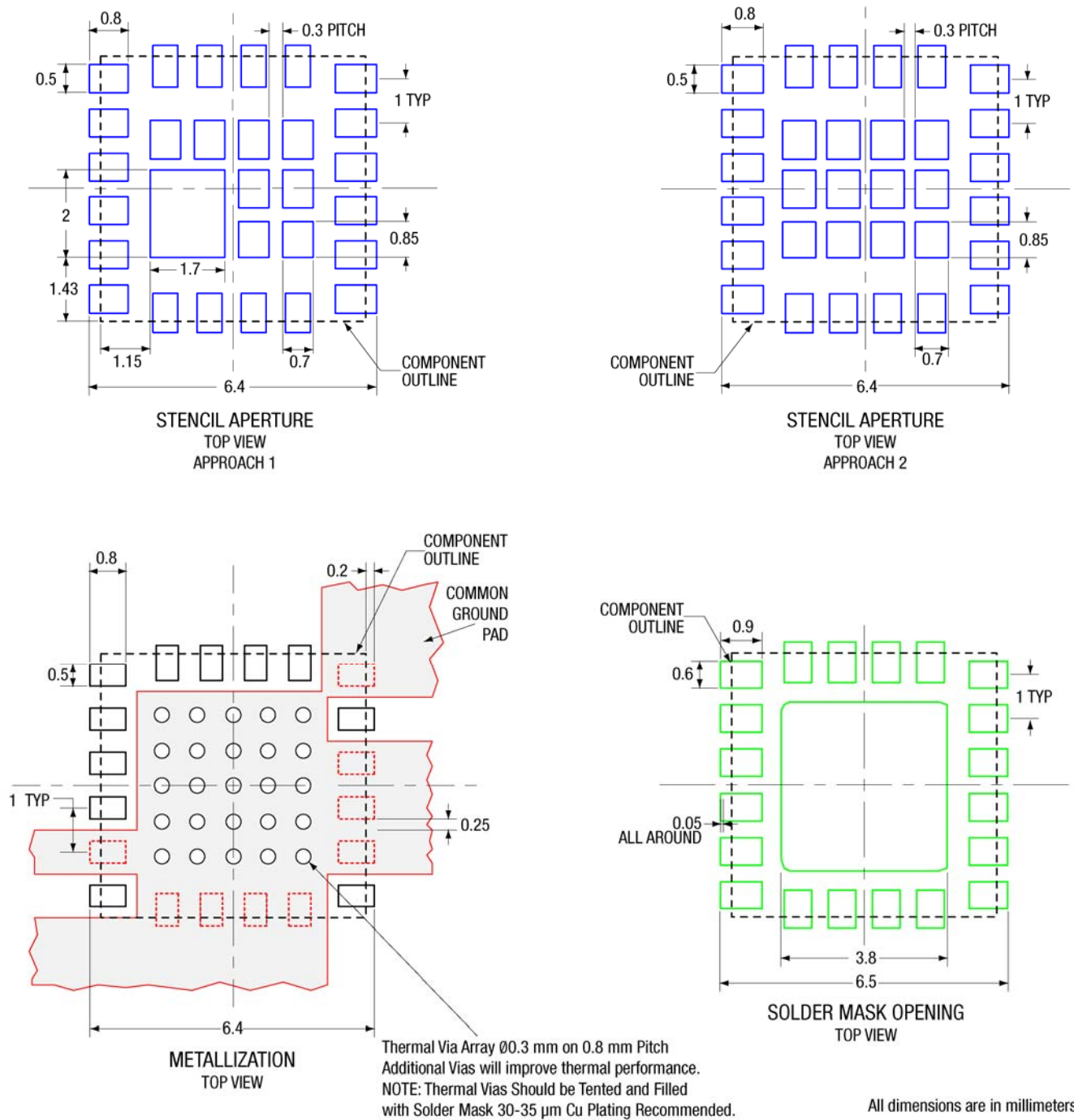


NOTES: UNLESS OTHERWISE SPECIFIED.

1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. PADS ARE SOLDER MASK DEFINED ON ALL INSIDE EDGES.

**Figure 3. SKY77328 PAM Package Dimensions—20-Pin Leadless (All Views)**

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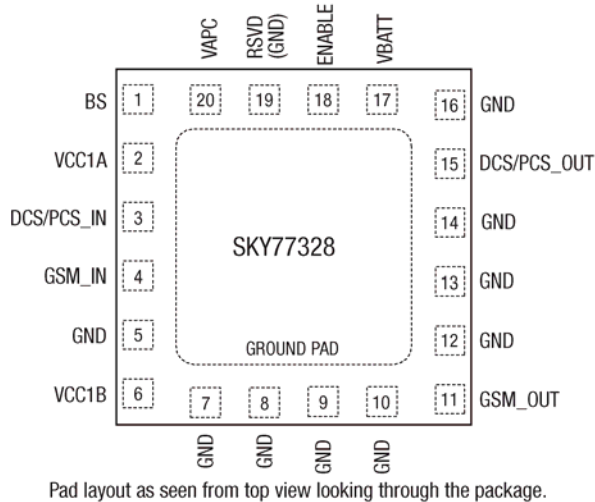
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Figure 4. Phone Board Layout Footprint for 6 x 6 mm, 20-Pad SKY77328 Package

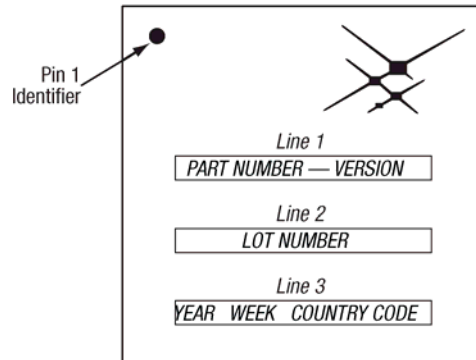
**Package Descriptions**

Figure 5 shows the device pin configuration and Table 4 lists the pin names and signal descriptions. The pin numbering convention

starts with pin 1 at the upper left, as indicated in Figure 5, and increments counter-clockwise around the package. Figure 6 interprets typical case markings.



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NOTE: Lines 1, 2, 3 have a maximum of 12 characters  
 YEAR = Year of Manufacture  
 WEEK = Week Package Was Sealed  
 Country Code = Country of Manufacture (MX)

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**Figure 5. SKY77328 PAM Pin Configuration—20-Pin Leadless (Top View)**

**Figure 6. Typical Case Markings**

**Table 4. SKY77328 Pin Names and Signal Descriptions**

Pin 1	Name	Description
1	BS	Band Select
2	VCC1A	VCC (to GSM 1st stage, DCS/PCS 1st stages, BiCMOS PAC)
3	DCS/PCS_IN	RF input 1710–1910 MHz (DCS1800, PCS1900)
4	GSM_IN	RF input 824–915 MHz (GSM850/900)
6	VCC1B	VCC (to GSM 2nd stage, DCS/PCS 2nd stages)
11	GSM_OUT	RF Output 824–915 MHz (GSM850/900)
15	DCS/PCS_OUT	RF Output 1710–1910 MHz (DCS1800, PCS1900)
16	GND	RF and DC Ground
17	VBATT	Battery input to high side of internal sense resistor
18	ENABLE	BiCMOS Enable
20	VAPC	Power Control Bias Voltage
GND PAD (21)	GND	Ground Pad, bottom

<sup>1</sup> Pads 5, 7–10, 12–14, 16 are Ground pads; pad 19 is a RSVD/GND pad

## Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77328 is capable of withstanding an MSL3/260 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 260 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 260 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Skyworks Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard

- Personnel Grounding
  - Wrist Straps
  - Conductive Smocks, Gloves and Finger Cots
  - Antistatic ID Badges
- Protective Workstation
  - Dissipative Table Top
  - Protective Test Equipment (Properly Grounded)
  - Grounded Tip Soldering Irons
  - Solder Conductive Suckers
  - Static Sensors

SMT reflow profiles can also be found in the *JEDEC Standard J-STD-020B*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Skyworks Application Note: Tape and Reel – RF Modules, Document Number 101568*.

## Electrostatic Discharge Sensitivity

The SKY77328 has been classified as a Human Body Model Class 1C (1000 volts to < 2000 volts) and Machine Model Class M2 (100 volts to < 200 volts) device. ESD testing has been performed in compliance to the latest JEDEC Human Body Model specification, HBM (JESD22-A114-B) and Machine Model specification, (JESD22-A115-A). A report summarizing the ESD testing, including ESD failure level thresholds on each pin-to-ground and pin-to-pin combination may be obtained upon request.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed below.

- Facility
  - Relative Humidity Control and Air Ionizers
  - Dissipative Floors (less than  $10^9 \Omega$  to GND)
- Protective Packaging and Transportation
  - Bags and Pouches (Faraday Shield)
  - Protective Tote Boxes (Conductive Static Shielding)
  - Protective Trays
  - Grounded Carts
  - Protective Work Order Holders

## Technical Information

Closed loop control of the amplifier is enabled when ENABLE is driven to logic high. The PA collector current will then be directly proportional to the  $V_{APC}$  input voltage over the range of 200 mV to 2.1 V.

To meet the GSM power versus time mask and switching transient requirements the PAM must be provided with a DAC ramp profile on the  $V_{APC}$  input as well as proper timing on digital controls for the PAC circuitry.

**Note:** *Please refer to 3GPP TS 51.010-1: Mobile Station (MS) conformance specification. All GSM specifications are now the responsibility of 3GPP. The standards are available at <http://www.3gpp.org>.*

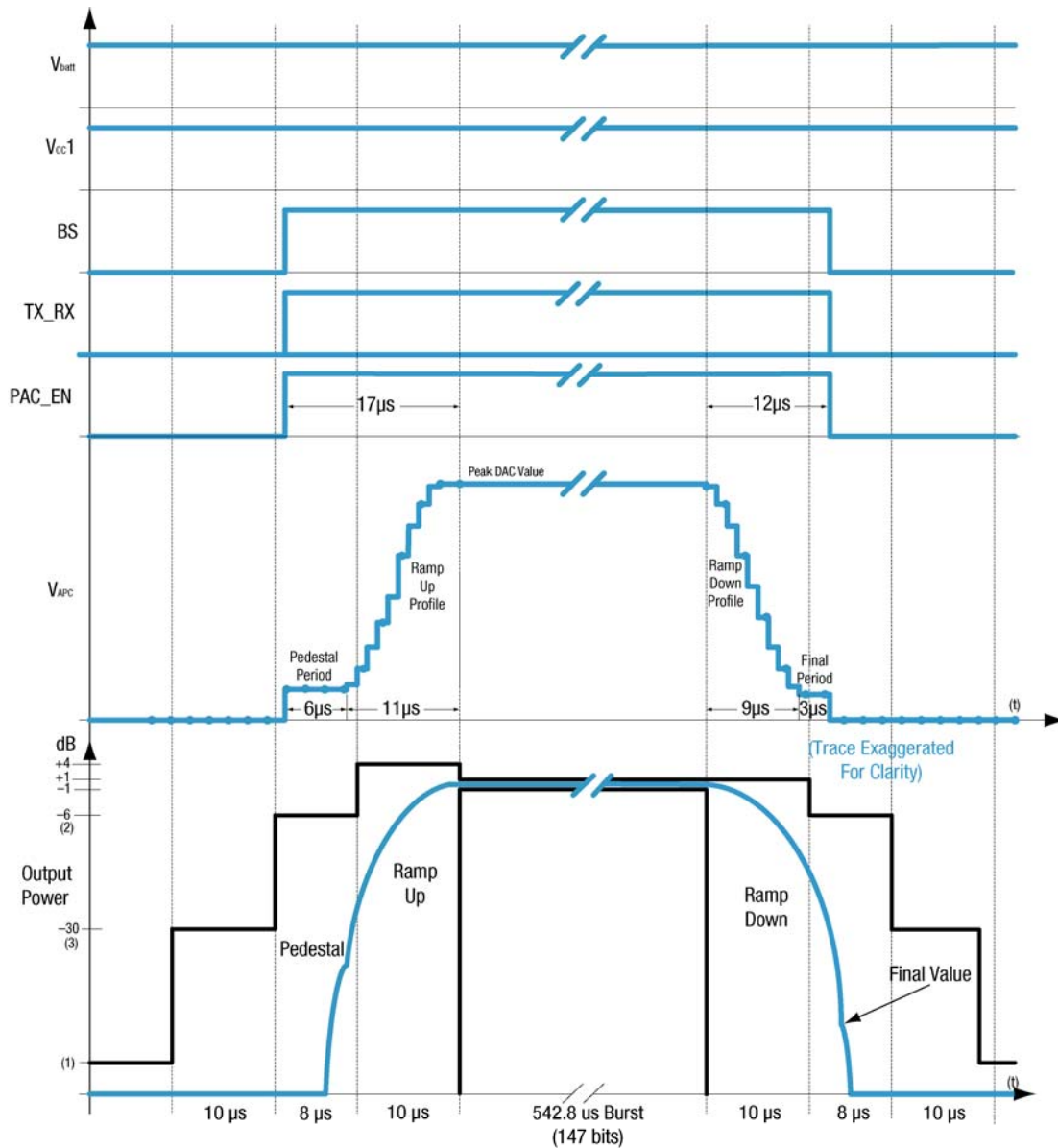
The SKY77328 has been designed to comply with interface requirements and DAC resolution of leading base band devices. The ramp profile typically consists of a pedestal voltage, 10–16 discrete voltage steps on the rising edge of the burst, a constant region, 10–16 steps on the falling edge, and a final voltage. Typically, the user defines the start, stop, and 10–16 percentage values for each rising and falling edge, which are then applied as discrete voltages at the  $V_{APC}$  input. For the SKY77328, generally the same profile, scaled in amplitude, is used for all frequencies and power control levels. The ultimate purpose is to keep the RF

output power ramp within the time mask and to maintain acceptable spectral limits at specified offset frequencies. The  $V_{APC}$  input has an internal reconstruction filter such that external resistors or capacitors are unnecessary on the phone board or the test fixture.

Figure 7 represents the dynamic characteristics of the RF output burst power that results from the ramp profile delivered by the DAC to the  $V_{APC}$  input. The transmit power must not exceed the given limits at the time specified relative to the start and end of the data burst. Additional requirements are placed on spectral components generated by switching transients. Ramping at high rates will result in components that violate these spectral limits. A ramp control signal must be applied to the  $V_{APC}$  pin, which results in the desired power ramp response. The log relationship of  $V_{APC}$  to  $P_{OUT}$ , along with the finite bandwidth and potential slew rate limitations of the feedback loop, results in a complex mapping of the ramp profile to the actual output power. Careful attention is required in generating the input waveform which results in the desired output response.

Figure 8 shows an example of the Skyworks PAM test setup for evaluation of RF performance with various ramp profiles. The user's test setup may also include a TX/RX switch and a diplexer in the output signal path. Alternatively, the SKY77328 PAM may be installed in a phone board.

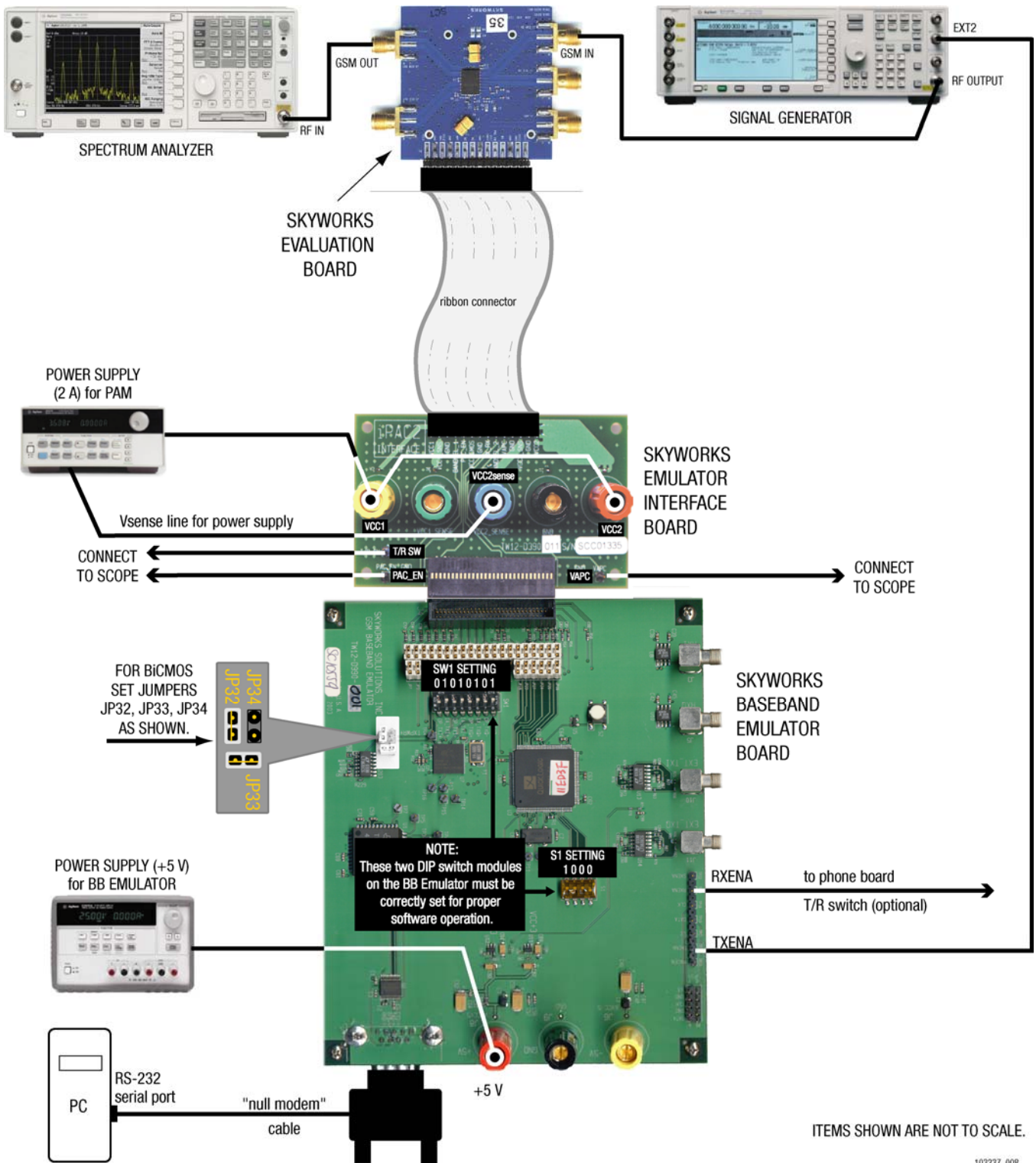




- |     |                       |  |
|-----|-----------------------|--|
| (1) | For GSM850 / EGSM     | -59 dBc or -36 dBm, whichever is higher.   |
|     | For DCS1800 / PCS1900 | -48 dBc or -48 dBm, whichever is higher.   |
| (2) | For GSM850 / EGSM     | -4 dBc for power control level 16,<br>-2 dBc for power control level 17,<br>-1 dBc for power control level 18 and 19.  |
|     | For DCS1800 / PCS1900 | -4 dBc for power control level 11,<br>-2 dBc for power control level 12,<br>-1 dBc for power control level 13, 14, 15. |
| (3) | For GSM850 / EGSM     | -30 dBc or -17 dBm, whichever is higher.   |
|     | For DCS1800 / PCS1900 | -30 dBc or -20 dBm, whichever is higher.   |

103237\_008

Figure 7. Example of PAM Recommended Timing Diagram



ITEMS SHOWN ARE NOT TO SCALE.

103237\_008

Figure 8. PAM Evaluation Test Setup – BiCMOS.

## Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
SKY77328	SKY77328		6 x 6 x 1.2 mm	-20 °C to +100 °C

## Revision History

Revision	Date	Description
A	March 17, 2009	Initial Release

## References

Application Note: Tape and Reel Information – RF Modules, Document Number 101568

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

Application Brief: iPAC™ GSM Transmitter Timing, Calibration and Baseband Control, Document Number 103138

Application Note: iPAC™ Peak Output Power Calibration, Document Number 103180

User Guide: iPAC™ Test and Control – Baseband Emulator Interface, Document Number 103125

JEDEC Standard J–STD–020

3GPP TS 51.010-1; Mobile Station (MS) Conformance Specification (<http://www.3GPP.org>)

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