# S6B33B1X

132 RGB Segment & 132 Common Driver For 65,536 Color STN LCD

APRIL. 10. 2003
Ver. 0.5

| S6B33B1X Specification Revision History | | |
|---|---|---|
| **Version** | **Content** | **Date** |
| 0.0 | Original | May.2002 |
| 0.1 | Page 14 : Remove CDIR, REG_ENB Pins, Add CS,SK,E_DI,E_DO pins for EEPROM Interface<br>Page 20 : Add the description EEPROM interface<br>Page 29.30 : Correct Reg and OSC fiqure<br>Page 31 : Add fuctions for EEPROM Interface<br>Page 33 : Add CDIR of Driver Output Mode Set<br>Page 58,59 : Add Instructions for EEPROM Interface<br>Page 74 : Add EEPROM Interface timing<br>Page 76,77 : Add the schottky barrier diode and EEPROM block | June.2002 |
| 0.2 | Page 3,5-11 : Add Pad Informations<br>Page 24 : Modify Display Data RAM Map<br>Page 33 : Add the fuction of OSC Mode Set<br>Page 65 : Add DC2IN,VIN45,VIN2 Characteristics | July.2002 |
| 0.3 | Page 2,11 : Remove VDDO Pin<br>Page 4 : Change Tom lenghth<br>Page 7 : Change the VEES pad to the VEE pad<br>Page 23 : Add the bit alignment of data in the figure13<br>Page 28 : Change the Figure20<br>Page 50 : Delete the sentence “refer to page51”<br>Page 51 : Delete this page<br>Page 62 : Change the LCD supply voltage range and the supply voltage(2)<br>Page 63 : Add VREG and Change max voltage of VIN2<br>Page 65 : Change VM *6 to VM * bias<br>Page 68 : Delete this page | Aug.2002 |
| 0.4 | Page 13 : Change OSC1,OSC2,OSC5 description<br>Page 14 : Change TEST description<br>Page 20 : Add Data Transfer and Time Wait Information<br>Page 36 : Correct Bias Set Instruction and DIV instruction<br>Page 37 : Change Temperature Compensation Center Value<br>Page 56 : Add RAM Access<br>Page 63 : Change the DIV value of Reset Operation<br>Page 65 : Add values of VEE and VCC<br>Page 72 : Add Serial Interface Timing<br>Page 73 : Add EEPROM Interface Timing | Jan.2003 |
| 0.5 | Page 14 : Change TEST description. | April.2003 |

# CONTENTS

# INTRODUCTION

S6B33B1X is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip CR oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 132 output) corresponding to the display data and the internal bit-map display RAM of 132 ×132 ×16-bit, S6B33B1X is capable of operating max. 132 RGB x 132 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 16-bit data and S6B33B1X can max display 65,536 color.

# FEATURES

### Driver Output

– 132 RGB x 132

### Gray Scale Function

– 65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale
– 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
– 256 color display of R: 8 gray scale, G: 8 gray scale, B: 4 gray scale

### On-chip Display Data RAM

– Capacity: 132 x 16 x 132 = 278.784k bits
– Burst RAM write function

### Display Mode

– Normal display mode: Entire duty displaying
– Partial display mode: Partial duty displaying
– Standby mode: Internal display clocks off
– Area scroll mode: Particular area scrolling

### Microprocessor Interface

– 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
– 3/4 Pin SPI (only write operation)

### On-chip Low Power Analog Circuit

– On-chip CR oscillator (Internal cap. & external resistor), external clock available
– Voltage converter / Voltage regulator / Voltage follower
– On-chip electronic contrast control (256 steps)

### Operating Voltage Range

– VDD : 1.8 to 3.3 [V] (without Internal Regulator), 2.4 to 3.3 [V] (With internal Regulator)
– VIN1: 2.4 to 3.6 [V]
– Display operating voltage(V1): 2.0 to 3.3 V
– LCD Operating Voltage Range : Max. 20 V

### Low Power Consumption

– TBD μA Typ.

### Package Type

– COG (Output Pad Pitch Min. 38 μm)

# BLOCK DIAGRAM

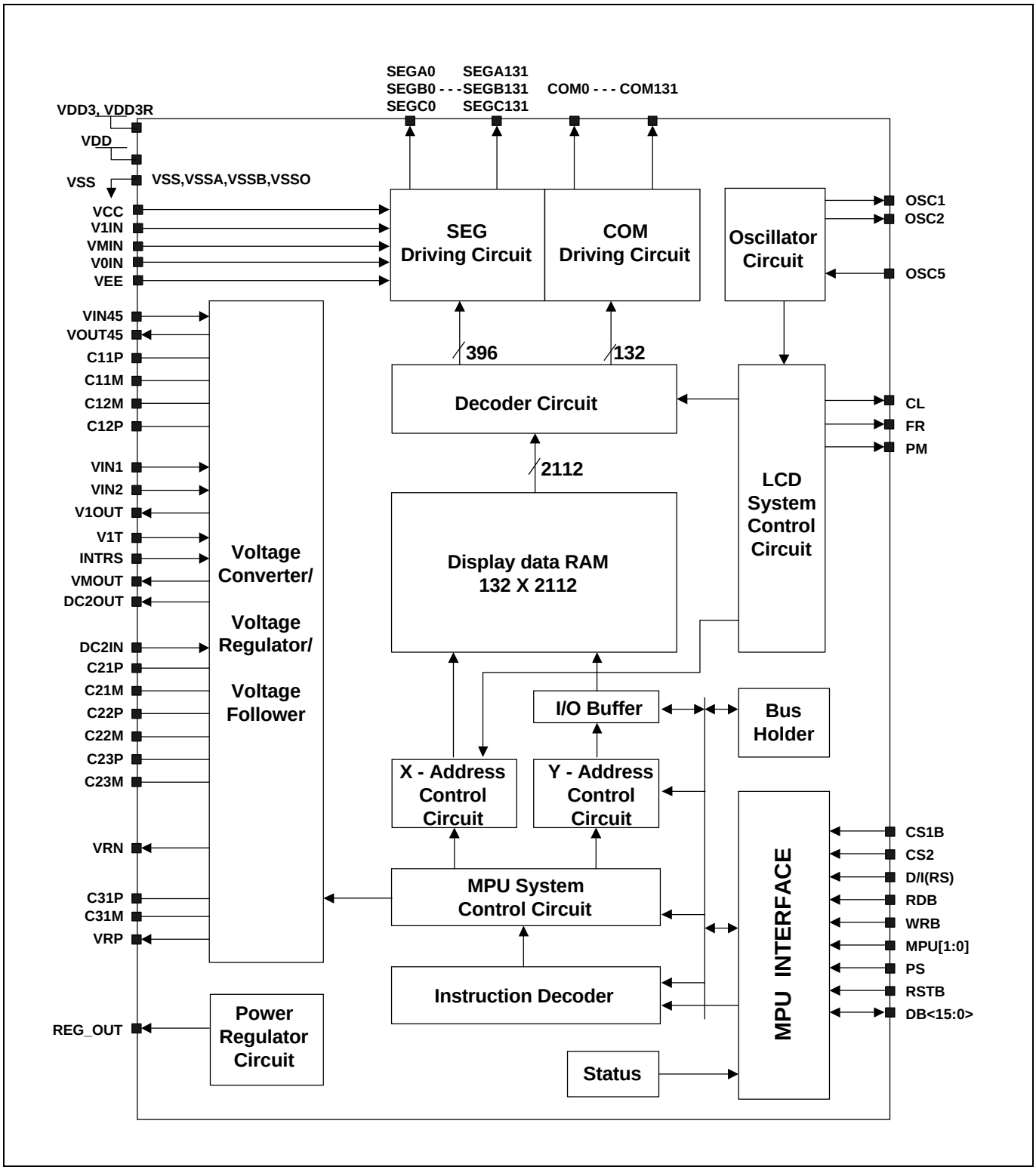



**Figure 1. Block Diagram**

# PAD CONFIGURATION

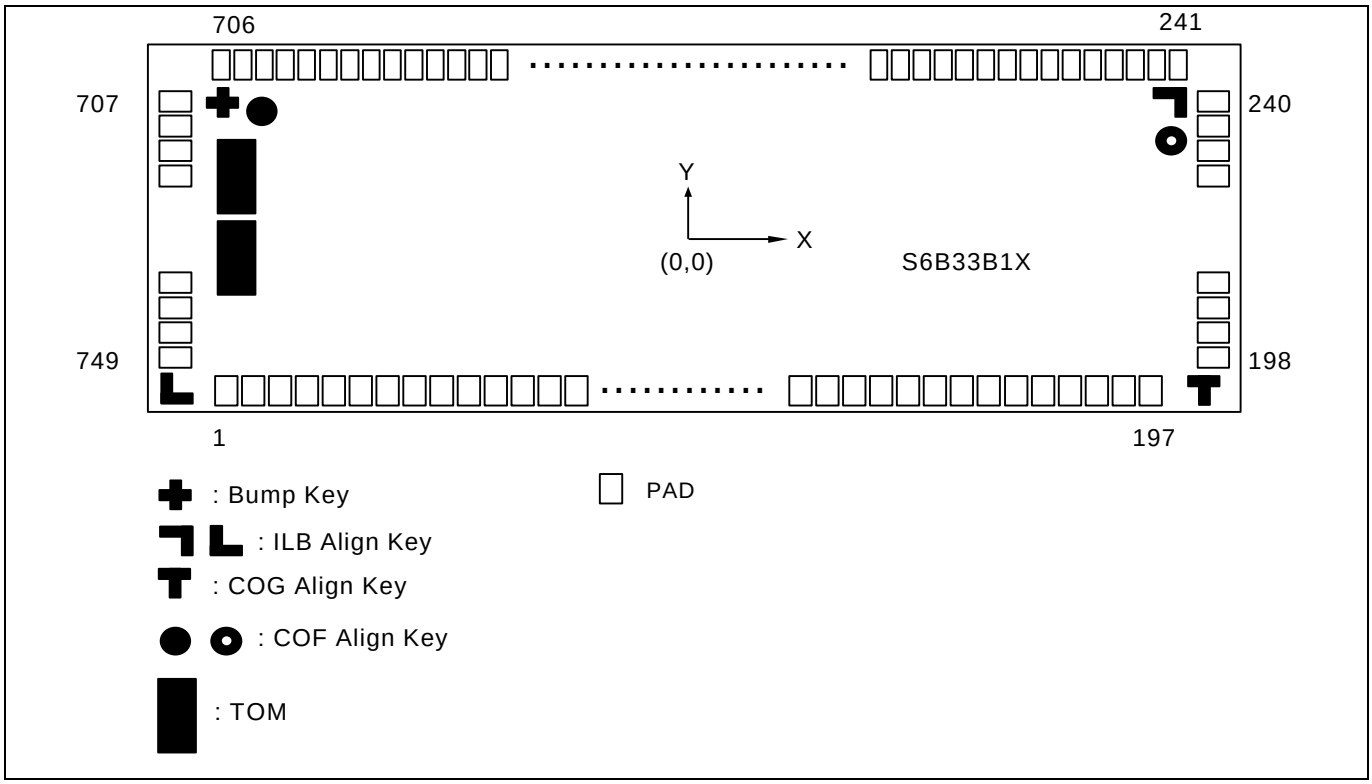


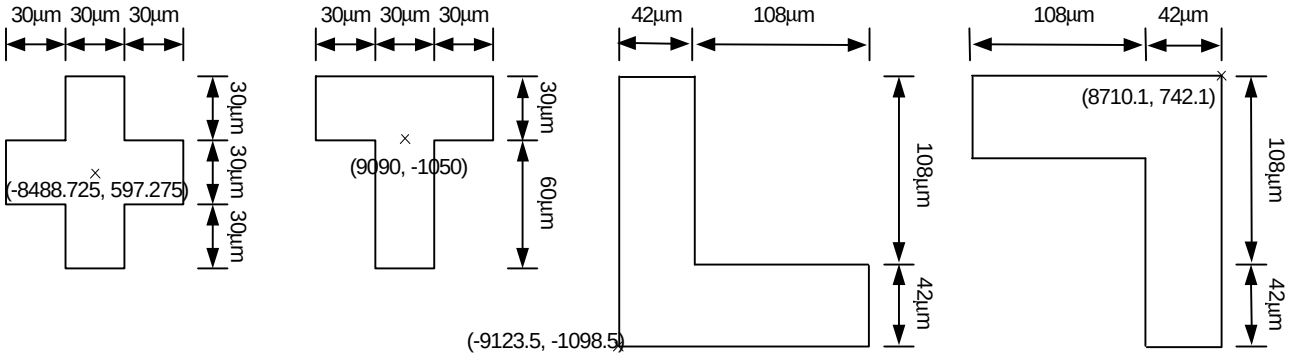

**Figure 2. S6B33B1X Chip Pad Configuration**

**Table 1. S6B33B1X Pad Dimensions**

| Item | Pad No. | Size | | Unit |
|---|---|---|---|---|
| | | X | Y | |
| Chip size (with S/L 120µm) | - | 18610 | 2560 | µm |
| Pad pitch | 1 to 197 | 90 | | |
| | 198 to 240, 241 to 706, 707 to 749 | 38 | | |
| Bumped pad size | 1 to 197 | 70 | 70 | |
| | 198 to 240, 707 to 749 | 170 | 23 | |
| | 241 to 706 | 23 | 170 | |
| Bumped pad height | All Pad | 17 | | |

**Figure 3. Bump, COG Align Key Coordinate**

**Figure 4. ILB Align Key Coordinate**



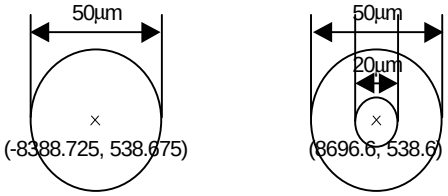




**Figure 5. COF Align Key Coordinate**

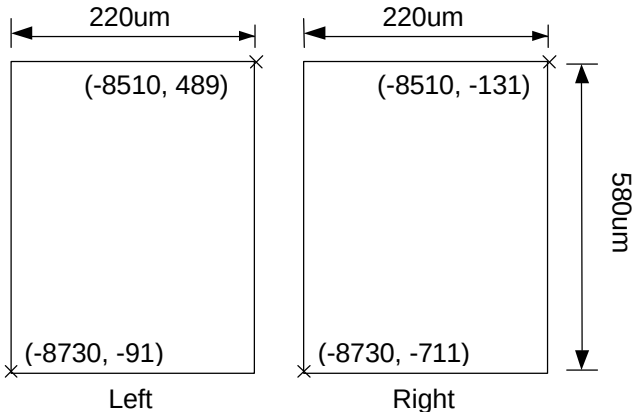



**Figure 6. TOM Coordinate**

# PIN CONFIGURATION

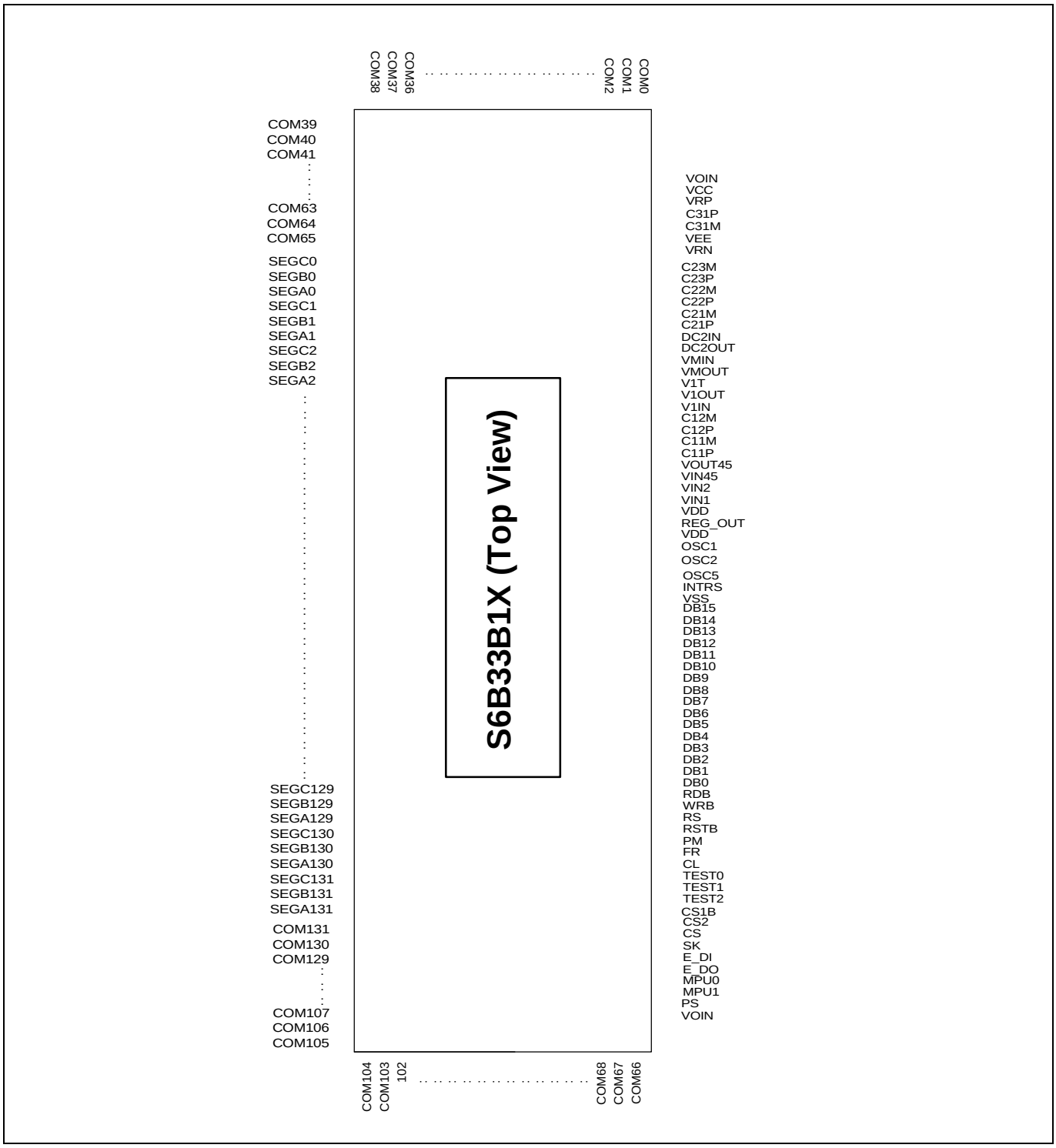



**Figure 7. S6B33B1X Chip Pin Configuration**

# PAD CENTER COORDINATES

**Table 2. Pad Center Coordinates**

[Unit: μm]

| No | X | Y | NAME | No | X | Y | NAME | No | X | Y | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | -8820 | -1165 | DUMMY<0> | 51 | -4320 | -1165 | VSS | 101 | 180 | -1165 | VIN1 |
| 2 | -8730 | -1165 | DUMMY<1> | 52 | -4230 | -1165 | VSS | 102 | 270 | -1165 | VIN1 |
| 3 | -8640 | -1165 | V0IN | 53 | -4140 | -1165 | VSS | 103 | 360 | -1165 | VIN1 |
| 4 | -8550 | -1165 | V0IN | 54 | -4050 | -1165 | VSS | 104 | 450 | -1165 | VIN1 |
| 5 | -8460 | -1165 | VSS | 55 | -3960 | -1165 | VSS | 105 | 540 | -1165 | VIN1 |
| 6 | -8370 | -1165 | PS | 56 | -3870 | -1165 | VSSA | 106 | 630 | -1165 | VIN1 |
| 7 | -8280 | -1165 | VDD3 | 57 | -3780 | -1165 | VSSA | 107 | 720 | -1165 | VIN1 |
| 8 | -8190 | -1165 | MPU1 | 58 | -3690 | -1165 | VSSA | 108 | 810 | -1165 | VIN1 |
| 9 | -8100 | -1165 | VSS | 59 | -3600 | -1165 | VSSO | 109 | 900 | -1165 | VIN1A |
| 10 | -8010 | -1165 | MPU0 | 60 | -3510 | -1165 | VSSO | 110 | 990 | -1165 | VIN1A |
| 11 | -7920 | -1165 | VDD3 | 61 | -3420 | -1165 | VSSO | 111 | 1080 | -1165 | VIN1A |
| 12 | -7830 | -1165 | E_DO | 62 | -3330 | -1165 | VSSO | 112 | 1170 | -1165 | VIN2 |
| 13 | -7740 | -1165 | E_DI | 63 | -3240 | -1165 | VSSB | 113 | 1260 | -1165 | VIN2 |
| 14 | -7650 | -1165 | SK | 64 | -3150 | -1165 | VSSB | 114 | 1350 | -1165 | VIN2 |
| 15 | -7560 | -1165 | CS | 65 | -3060 | -1165 | VSSB | 115 | 1440 | -1165 | VIN2 |
| 16 | -7470 | -1165 | VSS | 66 | -2970 | -1165 | VSSB | 116 | 1530 | -1165 | VIN45 |
| 17 | -7380 | -1165 | CS1B | 67 | -2880 | -1165 | VDD3 | 117 | 1620 | -1165 | VIN45 |
| 18 | -7290 | -1165 | CS2 | 68 | -2790 | -1165 | VSSB | 118 | 1710 | -1165 | VOUT45 |
| 19 | -7200 | -1165 | TEST2 | 69 | -2700 | -1165 | VSSB | 119 | 1800 | -1165 | VOUT45 |
| 20 | -7110 | -1165 | TEST1 | 70 | -2610 | -1165 | VSSB | 120 | 1890 | -1165 | C11P |
| 21 | -7020 | -1165 | TEST0 | 71 | -2520 | -1165 | VSSB | 121 | 1980 | -1165 | C11P |
| 22 | -6930 | -1165 | VDD3 | 72 | -2430 | -1165 | VSSB | 122 | 2070 | -1165 | C11P |
| 23 | -6840 | -1165 | CL | 73 | -2340 | -1165 | VSSB | 123 | 2160 | -1165 | C11M |
| 24 | -6750 | -1165 | FR | 74 | -2250 | -1165 | VSSB | 124 | 2250 | -1165 | C11M |
| 25 | -6660 | -1165 | PM | 75 | -2160 | -1165 | INTRS | 125 | 2340 | -1165 | C11M |
| 26 | -6570 | -1165 | RSTB | 76 | -2070 | -1165 | OSC5 | 126 | 2430 | -1165 | C12P |
| 27 | -6480 | -1165 | RS | 77 | -1980 | -1165 | VSS | 127 | 2520 | -1165 | C12P |
| 28 | -6390 | -1165 | VSS | 78 | -1890 | -1165 | OSC2 | 128 | 2610 | -1165 | C12P |
| 29 | -6300 | -1165 | WRB | 79 | -1800 | -1165 | OSC1 | 129 | 2700 | -1165 | C12M |
| 30 | -6210 | -1165 | RDB | 80 | -1710 | -1165 | VDD | 130 | 2790 | -1165 | C12M |
| 31 | -6120 | -1165 | VDD3 | 81 | -1620 | -1165 | VDD | 131 | 2880 | -1165 | C12M |
| 32 | -6030 | -1165 | DB0 | 82 | -1530 | -1165 | VDD | 132 | 2970 | -1165 | V1IN |
| 33 | -5940 | -1165 | DB1 | 83 | -1440 | -1165 | VDD | 133 | 3060 | -1165 | V1IN |
| 34 | -5850 | -1165 | DB2 | 84 | -1350 | -1165 | VDD | 134 | 3150 | -1165 | V1OUT |
| 35 | -5760 | -1165 | DB3 | 85 | -1260 | -1165 | VDD | 135 | 3240 | -1165 | V1OUT |
| 36 | -5670 | -1165 | DB4 | 86 | -1170 | -1165 | VDD | 136 | 3330 | -1165 | V1T |
| 37 | -5580 | -1165 | DB5 | 87 | -1080 | -1165 | VDD | 137 | 3420 | -1165 | VMOUT |
| 38 | -5490 | -1165 | DB6 | 88 | -990 | -1165 | REG_OUT | 138 | 3510 | -1165 | VMOUT |
| 39 | -5400 | -1165 | DB7 | 89 | -900 | -1165 | REG_OUT | 139 | 3600 | -1165 | VMOUT |
| 40 | -5310 | -1165 | DB8 | 90 | -810 | -1165 | REG_OUT | 140 | 3690 | -1165 | VMIN |
| 41 | -5220 | -1165 | DB9 | 91 | -720 | -1165 | VDD3R | 141 | 3780 | -1165 | VMIN |
| 42 | -5130 | -1165 | DB10 | 92 | -630 | -1165 | VDD3R | 142 | 3870 | -1165 | VMIN |
| 43 | -5040 | -1165 | DB11 | 93 | -540 | -1165 | VDD3R | 143 | 3960 | -1165 | VMIN |
| 44 | -4950 | -1165 | DB12 | 94 | -450 | -1165 | VDD3 | 144 | 4050 | -1165 | VMIN |
| 45 | -4860 | -1165 | DB13 | 95 | -360 | -1165 | VDD3 | 145 | 4140 | -1165 | VMIN |
| 46 | -4770 | -1165 | DB14 | 96 | -270 | -1165 | VDD3 | 146 | 4230 | -1165 | DC2OUT |
| 47 | -4680 | -1165 | DB15 | 97 | -180 | -1165 | VDD3 | 147 | 4320 | -1165 | DC2OUT |
| 48 | -4590 | -1165 | VSS | 98 | -90 | -1165 | VIN1 | 148 | 4410 | -1165 | DC2IN |
| 49 | -4500 | -1165 | VSS | 99 | 0 | -1165 | VIN1 | 149 | 4500 | -1165 | DC2IN |
| 50 | -4410 | -1165 | VSS | 100 | 90 | -1165 | VIN1 | 150 | 4590 | -1165 | DC2IN |

## Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

| No | X | Y | NAME | No | X | Y | NAME | No | X | Y | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 151 | 4680 | -1165 | DC2IN | 201 | 9135 | -652 | COM<1> | 251 | 8455 | 1110 | COM<47> |
| 152 | 4770 | -1165 | C21P | 202 | 9135 | -614 | COM<2> | 252 | 8417 | 1110 | COM<48> |
| 153 | 4860 | -1165 | C21P | 203 | 9135 | -576 | COM<3> | 253 | 8379 | 1110 | COM<49> |
| 154 | 4950 | -1165 | C21P | 204 | 9135 | -538 | COM<4> | 254 | 8341 | 1110 | COM<50> |
| 155 | 5040 | -1165 | C21M | 205 | 9135 | -500 | COM<5> | 255 | 8303 | 1110 | COM<51> |
| 156 | 5130 | -1165 | C21M | 206 | 9135 | -462 | COM<6> | 256 | 8265 | 1110 | COM<52> |
| 157 | 5220 | -1165 | C21M | 207 | 9135 | -424 | COM<7> | 257 | 8227 | 1110 | COM<53> |
| 158 | 5310 | -1165 | C22P | 208 | 9135 | -386 | COM<8> | 258 | 8189 | 1110 | COM<54> |
| 159 | 5400 | -1165 | C22P | 209 | 9135 | -348 | COM<9> | 259 | 8151 | 1110 | COM<55> |
| 160 | 5490 | -1165 | C22P | 210 | 9135 | -310 | COM<10> | 260 | 8113 | 1110 | COM<56> |
| 161 | 5580 | -1165 | C22M | 211 | 9135 | -272 | COM<11> | 261 | 8075 | 1110 | COM<57> |
| 162 | 5670 | -1165 | C22M | 212 | 9135 | -234 | COM<12> | 262 | 8037 | 1110 | COM<58> |
| 163 | 5760 | -1165 | C22M | 213 | 9135 | -196 | COM<13> | 263 | 7999 | 1110 | COM<59> |
| 164 | 5850 | -1165 | C23P | 214 | 9135 | -158 | COM<14> | 264 | 7961 | 1110 | COM<60> |
| 165 | 5940 | -1165 | C23P | 215 | 9135 | -120 | COM<15> | 265 | 7923 | 1110 | COM<61> |
| 166 | 6030 | -1165 | C23P | 216 | 9135 | -82 | COM<16> | 266 | 7885 | 1110 | COM<62> |
| 167 | 6120 | -1165 | C23M | 217 | 9135 | -44 | COM<17> | 267 | 7847 | 1110 | COM<63> |
| 168 | 6210 | -1165 | C23M | 218 | 9135 | -6 | COM<18> | 268 | 7809 | 1110 | COM<64> |
| 169 | 6300 | -1165 | C23M | 219 | 9135 | 32 | COM<19> | 269 | 7771 | 1110 | COM<65> |
| 170 | 6390 | -1165 | VRN | 220 | 9135 | 70 | COM<20> | 270 | 7733 | 1110 | DUMMY<14> |
| 171 | 6480 | -1165 | VRN | 221 | 9135 | 108 | COM<21> | 271 | 7695 | 1110 | DUMMY<15> |
| 172 | 6570 | -1165 | VRN | 222 | 9135 | 146 | COM<22> | 272 | 7657 | 1110 | DUMMY<16> |
| 173 | 6660 | -1165 | VEE | 223 | 9135 | 184 | COM<23> | 273 | 7619 | 1110 | DUMMY<17> |
| 174 | 6750 | -1165 | VEE | 224 | 9135 | 222 | COM<24> | 274 | 7581 | 1110 | DUMMY<18> |
| 175 | 6840 | -1165 | VEE | 225 | 9135 | 260 | COM<25> | 275 | 7543 | 1110 | DUMMY<19> |
| 176 | 6930 | -1165 | VEE | 226 | 9135 | 298 | COM<26> | 276 | 7505 | 1110 | SEGC<0> |
| 177 | 7020 | -1165 | VEE | 227 | 9135 | 336 | COM<27> | 277 | 7467 | 1110 | SEGB<0> |
| 178 | 7110 | -1165 | VEE | 228 | 9135 | 374 | COM<28> | 278 | 7429 | 1110 | SEGA<0> |
| 179 | 7200 | -1165 | DUMMY<2> | 229 | 9135 | 412 | COM<29> | 279 | 7391 | 1110 | SEGC<1> |
| 180 | 7290 | -1165 | C31M | 230 | 9135 | 450 | COM<30> | 280 | 7353 | 1110 | SEGB<1> |
| 181 | 7380 | -1165 | C31M | 231 | 9135 | 488 | COM<31> | 281 | 7315 | 1110 | SEGA<1> |
| 182 | 7470 | -1165 | C31M | 232 | 9135 | 526 | COM<32> | 282 | 7277 | 1110 | SEGC<2> |
| 183 | 7560 | -1165 | DUMMY<3> | 233 | 9135 | 564 | COM<33> | 283 | 7239 | 1110 | SEGB<2> |
| 184 | 7650 | -1165 | C31P | 234 | 9135 | 602 | COM<34> | 284 | 7201 | 1110 | SEGA<2> |
| 185 | 7740 | -1165 | C31P | 235 | 9135 | 640 | COM<35> | 285 | 7163 | 1110 | SEGC<3> |
| 186 | 7830 | -1165 | C31P | 236 | 9135 | 678 | COM<36> | 286 | 7125 | 1110 | SEGB<3> |
| 187 | 7920 | -1165 | DUMMY<4> | 237 | 9135 | 716 | COM<37> | 287 | 7087 | 1110 | SEGA<3> |
| 188 | 8010 | -1165 | VRP | 238 | 9135 | 754 | COM<38> | 288 | 7049 | 1110 | SEGC<4> |
| 189 | 8100 | -1165 | VRP | 239 | 9135 | 792 | DUMMY<10> | 289 | 7011 | 1110 | SEGB<4> |
| 190 | 8190 | -1165 | VCC | 240 | 9135 | 830 | DUMMY<11> | 290 | 6973 | 1110 | SEGA<4> |
| 191 | 8280 | -1165 | VCC | 241 | 8835 | 1110 | DUMMY<12> | 291 | 6935 | 1110 | SEGC<5> |
| 192 | 8370 | -1165 | DUMMY<5> | 242 | 8797 | 1110 | DUMMY<13> | 292 | 6897 | 1110 | SEGB<5> |
| 193 | 8460 | -1165 | VSS | 243 | 8759 | 1110 | COM<39> | 293 | 6859 | 1110 | SEGA<5> |
| 194 | 8550 | -1165 | V0IN | 244 | 8721 | 1110 | COM<40> | 294 | 6821 | 1110 | SEGC<6> |
| 195 | 8640 | -1165 | V0IN | 245 | 8683 | 1110 | COM<41> | 295 | 6783 | 1110 | SEGB<6> |
| 196 | 8730 | -1165 | DUMMY<6> | 246 | 8645 | 1110 | COM<42> | 296 | 6745 | 1110 | SEGA<6> |
| 197 | 8820 | -1165 | DUMMY<7> | 247 | 8607 | 1110 | COM<43> | 297 | 6707 | 1110 | SEGC<7> |
| 198 | 9135 | -766 | DUMMY<8> | 248 | 8569 | 1110 | COM<44> | 298 | 6669 | 1110 | SEGB<7> |
| 199 | 9135 | -728 | DUMMY<9> | 249 | 8531 | 1110 | COM<45> | 299 | 6631 | 1110 | SEGA<7> |
| 200 | 9135 | -690 | COM<0> | 250 | 8493 | 1110 | COM<46> | 300 | 6593 | 1110 | SEGC<8> |

## Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

| No | X | Y | NAME | No | X | Y | NAME | No | X | Y | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 301 | 6555 | 1110 | SEGB<8> | 351 | 4655 | 1110 | SEGC<25> | 401 | 2755 | 1110 | SEGA<41> |
| 302 | 6517 | 1110 | SEGA<8> | 352 | 4617 | 1110 | SEGB<25> | 402 | 2717 | 1110 | SEGC<42> |
| 303 | 6479 | 1110 | SEGC<9> | 353 | 4579 | 1110 | SEGA<25> | 403 | 2679 | 1110 | SEGB<42> |
| 304 | 6441 | 1110 | SEGB<9> | 354 | 4541 | 1110 | SEGC<26> | 404 | 2641 | 1110 | SEGA<42> |
| 305 | 6403 | 1110 | SEGA<9> | 355 | 4503 | 1110 | SEGB<26> | 405 | 2603 | 1110 | SEGC<43> |
| 306 | 6365 | 1110 | SEGC<10> | 356 | 4465 | 1110 | SEGA<26> | 406 | 2565 | 1110 | SEGB<43> |
| 307 | 6327 | 1110 | SEGB<10> | 357 | 4427 | 1110 | SEGC<27> | 407 | 2527 | 1110 | SEGA<43> |
| 308 | 6289 | 1110 | SEGA<10> | 358 | 4389 | 1110 | SEGB<27> | 408 | 2489 | 1110 | SEGC<44> |
| 309 | 6251 | 1110 | SEGC<11> | 359 | 4351 | 1110 | SEGA<27> | 409 | 2451 | 1110 | SEGB<44> |
| 310 | 6213 | 1110 | SEGB<11> | 360 | 4313 | 1110 | SEGC<28> | 410 | 2413 | 1110 | SEGA<44> |
| 311 | 6175 | 1110 | SEGA<11> | 361 | 4275 | 1110 | SEGB<28> | 411 | 2375 | 1110 | SEGC<45> |
| 312 | 6137 | 1110 | SEGC<12> | 362 | 4237 | 1110 | SEGA<28> | 412 | 2337 | 1110 | SEGB<45> |
| 313 | 6099 | 1110 | SEGB<12> | 363 | 4199 | 1110 | SEGC<29> | 413 | 2299 | 1110 | SEGA<45> |
| 314 | 6061 | 1110 | SEGA<12> | 364 | 4161 | 1110 | SEGB<29> | 414 | 2261 | 1110 | SEGC<46> |
| 315 | 6023 | 1110 | SEGC<13> | 365 | 4123 | 1110 | SEGA<29> | 415 | 2223 | 1110 | SEGB<46> |
| 316 | 5985 | 1110 | SEGB<13> | 366 | 4085 | 1110 | SEGC<30> | 416 | 2185 | 1110 | SEGA<46> |
| 317 | 5947 | 1110 | SEGA<13> | 367 | 4047 | 1110 | SEGB<30> | 417 | 2147 | 1110 | SEGC<47> |
| 318 | 5909 | 1110 | SEGC<14> | 368 | 4009 | 1110 | SEGA<30> | 418 | 2109 | 1110 | SEGB<47> |
| 319 | 5871 | 1110 | SEGB<14> | 369 | 3971 | 1110 | SEGC<31> | 419 | 2071 | 1110 | SEGA<47> |
| 320 | 5833 | 1110 | SEGA<14> | 370 | 3933 | 1110 | SEGB<31> | 420 | 2033 | 1110 | SEGC<48> |
| 321 | 5795 | 1110 | SEGC<15> | 371 | 3895 | 1110 | SEGA<31> | 421 | 1995 | 1110 | SEGB<48> |
| 322 | 5757 | 1110 | SEGB<15> | 372 | 3857 | 1110 | SEGC<32> | 422 | 1957 | 1110 | SEGA<48> |
| 323 | 5719 | 1110 | SEGA<15> | 373 | 3819 | 1110 | SEGB<32> | 423 | 1919 | 1110 | SEGC<49> |
| 324 | 5681 | 1110 | SEGC<16> | 374 | 3781 | 1110 | SEGA<32> | 424 | 1881 | 1110 | SEGB<49> |
| 325 | 5643 | 1110 | SEGB<16> | 375 | 3743 | 1110 | SEGC<33> | 425 | 1843 | 1110 | SEGA<49> |
| 326 | 5605 | 1110 | SEGA<16> | 376 | 3705 | 1110 | SEGB<33> | 426 | 1805 | 1110 | SEGC<50> |
| 327 | 5567 | 1110 | SEGC<17> | 377 | 3667 | 1110 | SEGA<33> | 427 | 1767 | 1110 | SEGB<50> |
| 328 | 5529 | 1110 | SEGB<17> | 378 | 3629 | 1110 | SEGC<34> | 428 | 1729 | 1110 | SEGA<50> |
| 329 | 5491 | 1110 | SEGA<17> | 379 | 3591 | 1110 | SEGB<34> | 429 | 1691 | 1110 | SEGC<51> |
| 330 | 5453 | 1110 | SEGC<18> | 380 | 3553 | 1110 | SEGA<34> | 430 | 1653 | 1110 | SEGB<51> |
| 331 | 5415 | 1110 | SEGB<18> | 381 | 3515 | 1110 | SEGC<35> | 431 | 1615 | 1110 | SEGA<51> |
| 332 | 5377 | 1110 | SEGA<18> | 382 | 3477 | 1110 | SEGB<35> | 432 | 1577 | 1110 | SEGC<52> |
| 333 | 5339 | 1110 | SEGC<19> | 383 | 3439 | 1110 | SEGA<35> | 433 | 1539 | 1110 | SEGB<52> |
| 334 | 5301 | 1110 | SEGB<19> | 384 | 3401 | 1110 | SEGC<36> | 434 | 1501 | 1110 | SEGA<52> |
| 335 | 5263 | 1110 | SEGA<19> | 385 | 3363 | 1110 | SEGB<36> | 435 | 1463 | 1110 | SEGC<53> |
| 336 | 5225 | 1110 | SEGC<20> | 386 | 3325 | 1110 | SEGA<36> | 436 | 1425 | 1110 | SEGB<53> |
| 337 | 5187 | 1110 | SEGB<20> | 387 | 3287 | 1110 | SEGC<37> | 437 | 1387 | 1110 | SEGA<53> |
| 338 | 5149 | 1110 | SEGA<20> | 388 | 3249 | 1110 | SEGB<37> | 438 | 1349 | 1110 | SEGC<54> |
| 339 | 5111 | 1110 | SEGC<21> | 389 | 3211 | 1110 | SEGA<37> | 439 | 1311 | 1110 | SEGB<54> |
| 340 | 5073 | 1110 | SEGB<21> | 390 | 3173 | 1110 | SEGC<38> | 440 | 1273 | 1110 | SEGA<54> |
| 341 | 5035 | 1110 | SEGA<21> | 391 | 3135 | 1110 | SEGB<38> | 441 | 1235 | 1110 | SEGC<55> |
| 342 | 4997 | 1110 | SEGC<22> | 392 | 3097 | 1110 | SEGA<38> | 442 | 1197 | 1110 | SEGB<55> |
| 343 | 4959 | 1110 | SEGB<22> | 393 | 3059 | 1110 | SEGC<39> | 443 | 1159 | 1110 | SEGA<55> |
| 344 | 4921 | 1110 | SEGA<22> | 394 | 3021 | 1110 | SEGB<39> | 444 | 1121 | 1110 | SEGC<56> |
| 345 | 4883 | 1110 | SEGC<23> | 395 | 2983 | 1110 | SEGA<39> | 445 | 1083 | 1110 | SEGB<56> |
| 346 | 4845 | 1110 | SEGB<23> | 396 | 2945 | 1110 | SEGC<40> | 446 | 1045 | 1110 | SEGA<56> |
| 347 | 4807 | 1110 | SEGA<23> | 397 | 2907 | 1110 | SEGB<40> | 447 | 1007 | 1110 | SEGC<57> |
| 348 | 4769 | 1110 | SEGC<24> | 398 | 2869 | 1110 | SEGA<40> | 448 | 969 | 1110 | SEGB<57> |
| 349 | 4731 | 1110 | SEGB<24> | 399 | 2831 | 1110 | SEGC<41> | 449 | 931 | 1110 | SEGA<57> |
| 350 | 4693 | 1110 | SEGA<24> | 400 | 2793 | 1110 | SEGB<41> | 450 | 893 | 1110 | SEGC<58> |

## Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

| No | X | Y | NAME | No | X | Y | NAME | No | X | Y | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 451 | 855 | 1110 | SEGB<58> | 501 | -1045 | 1110 | SEGC<75> | 551 | -2945 | 1110 | SEGA<91> |
| 452 | 817 | 1110 | SEGA<58> | 502 | -1083 | 1110 | SEGB<75> | 552 | -2983 | 1110 | SEGC<92> |
| 453 | 779 | 1110 | SEGC<59> | 503 | -1121 | 1110 | SEGA<75> | 553 | -3021 | 1110 | SEGB<92> |
| 454 | 741 | 1110 | SEGB<59> | 504 | -1159 | 1110 | SEGC<76> | 554 | -3059 | 1110 | SEGA<92> |
| 455 | 703 | 1110 | SEGA<59> | 505 | -1197 | 1110 | SEGB<76> | 555 | -3097 | 1110 | SEGC<93> |
| 456 | 665 | 1110 | SEGC<60> | 506 | -1235 | 1110 | SEGA<76> | 556 | -3135 | 1110 | SEGB<93> |
| 457 | 627 | 1110 | SEGB<60> | 507 | -1273 | 1110 | SEGC<77> | 557 | -3173 | 1110 | SEGA<93> |
| 458 | 589 | 1110 | SEGA<60> | 508 | -1311 | 1110 | SEGB<77> | 558 | -3211 | 1110 | SEGC<94> |
| 459 | 551 | 1110 | SEGC<61> | 509 | -1349 | 1110 | SEGA<77> | 559 | -3249 | 1110 | SEGB<94> |
| 460 | 513 | 1110 | SEGB<61> | 510 | -1387 | 1110 | SEGC<78> | 560 | -3287 | 1110 | SEGA<94> |
| 461 | 475 | 1110 | SEGA<61> | 511 | -1425 | 1110 | SEGB<78> | 561 | -3325 | 1110 | SEGC<95> |
| 462 | 437 | 1110 | SEGC<62> | 512 | -1463 | 1110 | SEGA<78> | 562 | -3363 | 1110 | SEGB<95> |
| 463 | 399 | 1110 | SEGB<62> | 513 | -1501 | 1110 | SEGC<79> | 563 | -3401 | 1110 | SEGA<95> |
| 464 | 361 | 1110 | SEGA<62> | 514 | -1539 | 1110 | SEGB<79> | 564 | -3439 | 1110 | SEGC<96> |
| 465 | 323 | 1110 | SEGC<63> | 515 | -1577 | 1110 | SEGA<79> | 565 | -3477 | 1110 | SEGB<96> |
| 466 | 285 | 1110 | SEGB<63> | 516 | -1615 | 1110 | SEGC<80> | 566 | -3515 | 1110 | SEGA<96> |
| 467 | 247 | 1110 | SEGA<63> | 517 | -1653 | 1110 | SEGB<80> | 567 | -3553 | 1110 | SEGC<97> |
| 468 | 209 | 1110 | SEGC<64> | 518 | -1691 | 1110 | SEGA<80> | 568 | -3591 | 1110 | SEGB<97> |
| 469 | 171 | 1110 | SEGB<64> | 519 | -1729 | 1110 | SEGC<81> | 569 | -3629 | 1110 | SEGA<97> |
| 470 | 133 | 1110 | SEGA<64> | 520 | -1767 | 1110 | SEGB<81> | 570 | -3667 | 1110 | SEGC<98> |
| 471 | 95 | 1110 | SEGC<65> | 521 | -1805 | 1110 | SEGA<81> | 571 | -3705 | 1110 | SEGB<98> |
| 472 | 57 | 1110 | SEGB<65> | 522 | -1843 | 1110 | SEGC<82> | 572 | -3743 | 1110 | SEGA<98> |
| 473 | 19 | 1110 | SEGA<65> | 523 | -1881 | 1110 | SEGB<82> | 573 | -3781 | 1110 | SEGC<99> |
| 474 | -19 | 1110 | SEGC<66> | 524 | -1919 | 1110 | SEGA<82> | 574 | -3819 | 1110 | SEGB<99> |
| 475 | -57 | 1110 | SEGB<66> | 525 | -1957 | 1110 | SEGC<83> | 575 | -3857 | 1110 | SEGA<99> |
| 476 | -95 | 1110 | SEGA<66> | 526 | -1995 | 1110 | SEGB<83> | 576 | -3895 | 1110 | SEGC<100> |
| 477 | -133 | 1110 | SEGC<67> | 527 | -2033 | 1110 | SEGA<83> | 577 | -3933 | 1110 | SEGB<100> |
| 478 | -171 | 1110 | SEGB<67> | 528 | -2071 | 1110 | SEGC<84> | 578 | -3971 | 1110 | SEGA<100> |
| 479 | -209 | 1110 | SEGA<67> | 529 | -2109 | 1110 | SEGB<84> | 579 | -4009 | 1110 | SEGC<101> |
| 480 | -247 | 1110 | SEGC<68> | 530 | -2147 | 1110 | SEGA<84> | 580 | -4047 | 1110 | SEGB<101> |
| 481 | -285 | 1110 | SEGB<68> | 531 | -2185 | 1110 | SEGC<85> | 581 | -4085 | 1110 | SEGA<101> |
| 482 | -323 | 1110 | SEGA<68> | 532 | -2223 | 1110 | SEGB<85> | 582 | -4123 | 1110 | SEGC<102> |
| 483 | -361 | 1110 | SEGC<69> | 533 | -2261 | 1110 | SEGA<85> | 583 | -4161 | 1110 | SEGB<102> |
| 484 | -399 | 1110 | SEGB<69> | 534 | -2299 | 1110 | SEGC<86> | 584 | -4199 | 1110 | SEGA<102> |
| 485 | -437 | 1110 | SEGA<69> | 535 | -2337 | 1110 | SEGB<86> | 585 | -4237 | 1110 | SEGC<103> |
| 486 | -475 | 1110 | SEGC<70> | 536 | -2375 | 1110 | SEGA<86> | 586 | -4275 | 1110 | SEGB<103> |
| 487 | -513 | 1110 | SEGB<70> | 537 | -2413 | 1110 | SEGC<87> | 587 | -4313 | 1110 | SEGA<103> |
| 488 | -551 | 1110 | SEGA<70> | 538 | -2451 | 1110 | SEGB<87> | 588 | -4351 | 1110 | SEGC<104> |
| 489 | -589 | 1110 | SEGC<71> | 539 | -2489 | 1110 | SEGA<87> | 589 | -4389 | 1110 | SEGB<104> |
| 490 | -627 | 1110 | SEGB<71> | 540 | -2527 | 1110 | SEGC<88> | 590 | -4427 | 1110 | SEGA<104> |
| 491 | -665 | 1110 | SEGA<71> | 541 | -2565 | 1110 | SEGB<88> | 591 | -4465 | 1110 | SEGC<105> |
| 492 | -703 | 1110 | SEGC<72> | 542 | -2603 | 1110 | SEGA<88> | 592 | -4503 | 1110 | SEGB<105> |
| 493 | -741 | 1110 | SEGB<72> | 543 | -2641 | 1110 | SEGC<89> | 593 | -4541 | 1110 | SEGA<105> |
| 494 | -779 | 1110 | SEGA<72> | 544 | -2679 | 1110 | SEGB<89> | 594 | -4579 | 1110 | SEGC<106> |
| 495 | -817 | 1110 | SEGC<73> | 545 | -2717 | 1110 | SEGA<89> | 595 | -4617 | 1110 | SEGB<106> |
| 496 | -855 | 1110 | SEGB<73> | 546 | -2755 | 1110 | SEGC<90> | 596 | -4655 | 1110 | SEGA<106> |
| 497 | -893 | 1110 | SEGA<73> | 547 | -2793 | 1110 | SEGB<90> | 597 | -4693 | 1110 | SEGC<107> |
| 498 | -931 | 1110 | SEGC<74> | 548 | -2831 | 1110 | SEGA<90> | 598 | -4731 | 1110 | SEGB<107> |
| 499 | -969 | 1110 | SEGB<74> | 549 | -2869 | 1110 | SEGC<91> | 599 | -4769 | 1110 | SEGA<107> |
| 500 | -1007 | 1110 | SEGA<74> | 550 | -2907 | 1110 | SEGB<91> | 600 | -4807 | 1110 | SEGC<108> |

## Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

| No | X | Y | NAME | No | X | Y | NAME | No | X | Y | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 601 | -4845 | 1110 | SEGB<108> | 651 | -6745 | 1110 | SEGC<125> | 701 | -8645 | 1110 | COM<108> |
| 602 | -4883 | 1110 | SEGA<108> | 652 | -6783 | 1110 | SEGB<125> | 702 | -8683 | 1110 | COM<107> |
| 603 | -4921 | 1110 | SEGC<109> | 653 | -6821 | 1110 | SEGA<125> | 703 | -8721 | 1110 | COM<106> |
| 604 | -4959 | 1110 | SEGB<109> | 654 | -6859 | 1110 | SEGC<126> | 704 | -8759 | 1110 | COM<105> |
| 605 | -4997 | 1110 | SEGA<109> | 655 | -6897 | 1110 | SEGB<126> | 705 | -8797 | 1110 | DUMMY<26> |
| 606 | -5035 | 1110 | SEGC<110> | 656 | -6935 | 1110 | SEGA<126> | 706 | -8835 | 1110 | DUMMY<27> |
| 607 | -5073 | 1110 | SEGB<110> | 657 | -6973 | 1110 | SEGC<127> | 707 | -9135 | 830 | DUMMY<28> |
| 608 | -5111 | 1110 | SEGA<110> | 658 | -7011 | 1110 | SEGB<127> | 708 | -9135 | 792 | DUMMY<29> |
| 609 | -5149 | 1110 | SEGC<111> | 659 | -7049 | 1110 | SEGA<127> | 709 | -9135 | 754 | COM<104> |
| 610 | -5187 | 1110 | SEGB<111> | 660 | -7087 | 1110 | SEGC<128> | 710 | -9135 | 716 | COM<103> |
| 611 | -5225 | 1110 | SEGA<111> | 661 | -7125 | 1110 | SEGB<128> | 711 | -9135 | 678 | COM<102> |
| 612 | -5263 | 1110 | SEGC<112> | 662 | -7163 | 1110 | SEGA<128> | 712 | -9135 | 640 | COM<101> |
| 613 | -5301 | 1110 | SEGB<112> | 663 | -7201 | 1110 | SEGC<129> | 713 | -9135 | 602 | COM<100> |
| 614 | -5339 | 1110 | SEGA<112> | 664 | -7239 | 1110 | SEGB<129> | 714 | -9135 | 564 | COM<99> |
| 615 | -5377 | 1110 | SEGC<113> | 665 | -7277 | 1110 | SEGA<129> | 715 | -9135 | 526 | COM<98> |
| 616 | -5415 | 1110 | SEGB<113> | 666 | -7315 | 1110 | SEGC<130> | 716 | -9135 | 488 | COM<97> |
| 617 | -5453 | 1110 | SEGA<113> | 667 | -7353 | 1110 | SEGB<130> | 717 | -9135 | 450 | COM<96> |
| 618 | -5491 | 1110 | SEGC<114> | 668 | -7391 | 1110 | SEGA<130> | 718 | -9135 | 412 | COM<95> |
| 619 | -5529 | 1110 | SEGB<114> | 669 | -7429 | 1110 | SEGC<131> | 719 | -9135 | 374 | COM<94> |
| 620 | -5567 | 1110 | SEGA<114> | 670 | -7467 | 1110 | SEGB<131> | 720 | -9135 | 336 | COM<93> |
| 621 | -5605 | 1110 | SEGC<115> | 671 | -7505 | 1110 | SEGA<131> | 721 | -9135 | 298 | COM<92> |
| 622 | -5643 | 1110 | SEGB<115> | 672 | -7543 | 1110 | DUMMY<20> | 722 | -9135 | 260 | COM<91> |
| 623 | -5681 | 1110 | SEGA<115> | 673 | -7581 | 1110 | DUMMY<21> | 723 | -9135 | 222 | COM<90> |
| 624 | -5719 | 1110 | SEGC<116> | 674 | -7619 | 1110 | DUMMY<22> | 724 | -9135 | 184 | COM<89> |
| 625 | -5757 | 1110 | SEGB<116> | 675 | -7657 | 1110 | DUMMY<23> | 725 | -9135 | 146 | COM<88> |
| 626 | -5795 | 1110 | SEGA<116> | 676 | -7695 | 1110 | DUMMY<24> | 726 | -9135 | 108 | COM<87> |
| 627 | -5833 | 1110 | SEGC<117> | 677 | -7733 | 1110 | DUMMY<25> | 727 | -9135 | 70 | COM<86> |
| 628 | -5871 | 1110 | SEGB<117> | 678 | -7771 | 1110 | COM<131> | 728 | -9135 | 32 | COM<85> |
| 629 | -5909 | 1110 | SEGA<117> | 679 | -7809 | 1110 | COM<130> | 729 | -9135 | -6 | COM<84> |
| 630 | -5947 | 1110 | SEGC<118> | 680 | -7847 | 1110 | COM<129> | 730 | -9135 | -44 | COM<83> |
| 631 | -5985 | 1110 | SEGB<118> | 681 | -7885 | 1110 | COM<128> | 731 | -9135 | -82 | COM<82> |
| 632 | -6023 | 1110 | SEGA<118> | 682 | -7923 | 1110 | COM<127> | 732 | -9135 | -120 | COM<81> |
| 633 | -6061 | 1110 | SEGC<119> | 683 | -7961 | 1110 | COM<126> | 733 | -9135 | -158 | COM<80> |
| 634 | -6099 | 1110 | SEGB<119> | 684 | -7999 | 1110 | COM<125> | 734 | -9135 | -196 | COM<79> |
| 635 | -6137 | 1110 | SEGA<119> | 685 | -8037 | 1110 | COM<124> | 735 | -9135 | -234 | COM<78> |
| 636 | -6175 | 1110 | SEGC<120> | 686 | -8075 | 1110 | COM<123> | 736 | -9135 | -272 | COM<77> |
| 637 | -6213 | 1110 | SEGB<120> | 687 | -8113 | 1110 | COM<122> | 737 | -9135 | -310 | COM<76> |
| 638 | -6251 | 1110 | SEGA<120> | 688 | -8151 | 1110 | COM<121> | 738 | -9135 | -348 | COM<75> |
| 639 | -6289 | 1110 | SEGC<121> | 689 | -8189 | 1110 | COM<120> | 739 | -9135 | -386 | COM<74> |
| 640 | -6327 | 1110 | SEGB<121> | 690 | -8227 | 1110 | COM<119> | 740 | -9135 | -424 | COM<73> |
| 641 | -6365 | 1110 | SEGA<121> | 691 | -8265 | 1110 | COM<118> | 741 | -9135 | -462 | COM<72> |
| 642 | -6403 | 1110 | SEGC<122> | 692 | -8303 | 1110 | COM<117> | 742 | -9135 | -500 | COM<71> |
| 643 | -6441 | 1110 | SEGB<122> | 693 | -8341 | 1110 | COM<116> | 743 | -9135 | -538 | COM<70> |
| 644 | -6479 | 1110 | SEGA<122> | 694 | -8379 | 1110 | COM<115> | 744 | -9135 | -576 | COM<69> |
| 645 | -6517 | 1110 | SEGC<123> | 695 | -8417 | 1110 | COM<114> | 745 | -9135 | -614 | COM<68> |
| 646 | -6555 | 1110 | SEGB<123> | 696 | -8455 | 1110 | COM<113> | 746 | -9135 | -652 | COM<67> |
| 647 | -6593 | 1110 | SEGA<123> | 697 | -8493 | 1110 | COM<112> | 747 | -9135 | -690 | COM<66> |
| 648 | -6631 | 1110 | SEGC<124> | 698 | -8531 | 1110 | COM<111> | 748 | -9135 | -728 | DUMMY<30> |
| 649 | -6669 | 1110 | SEGB<124> | 699 | -8569 | 1110 | COM<110> | 749 | -9135 | -766 | DUMMY<31> |
| 650 | -6707 | 1110 | SEGA<124> | 700 | -8607 | 1110 | COM<109> | 750 | | | |

# PIN DESCRIPTION

**Table 3. Power Supply Pins**

| Name | I/O | Description |
|---|---|---|
| VDD3 | Supply | Main power supply |
| VDD3R | Supply | Internal regulator power supply<br>This pin is connected to VDD3. |
| VDD | Supply | Regulated power supply input pin for internal digital and DDRAM block.<br>This pin is connected to REG_OUT outside the chip with stabilization capacitor.<br>When the internal regulator is not used, VDD should be tied to VDD3 directly. |
| VSS VSSO<br>VSSA VSSB | GND | Ground |
| V1IN | I | LCD segment high selected driving voltage input pin |
| V1OUT | O | LCD segment high driving voltage output pin |
| VMIN | I | LCD common non-selected driving voltage input pin |
| VMOUT | O | LCD common/segment non-selected driving voltage output pin |
| V0IN | I | LCD segment low selected driving voltage input pin |
| VCC | I | LCD common high selected driving voltage input pin |
| VRP | O | LCD common high selected driving voltage output pin |
| VEE | I | LCD common low selected driving voltage input pin<br>The relationship between VCC, V1, VM, V0 and VEE:<br>VCC > V1 > VM > V0(=VSS) > VEE (V1 - VM = VM – V0, VCC –VM = VM - VEE) |
| VRN | O | LCD common low selected driving voltage output pin |
| VIN1 VIN1A | I | Power supply for 1' st booster circuit and VM amp |
| VIN2 | I | Power supply for 2' nd booster circuit |
| VOUT45 | O | 1' st booster output pin |
| VIN45 | I | Power supply for V1. Connect to VOUT45 or VIN1 |
| C11P C11M<br>C12P C12M | O | External capacitor connection pins used for 1' st booster circuit |
| V1T | I | Thermistor resistor connection pin |
| INTRS | I | External resister select pin for temperature compensation circuit<br>- INTRS = L : External resistor mode, INTRS = H : Internal resistor mode |
| DC2IN | I | Power supply for 2' nd booster. Connect to DC2OUT pin |
| DC2OUT | O | Power output pin for 2' nd booster input |
| C21P C21M<br>C22P C22M<br>C23P C23M | O | External capacitor connection pins used for 2' nd booster circuit |
| C31P C31M | O | External capacitor connection pins used for 3' rd booster circuit |

**Table 4. MPU Interface Pins**

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin.<br>When RSTB is “L”, initialization is executed.</td></tr>
<tr><td>PS<br>MPU[1:0]</td><td>I</td><td>MPU interface select pin
<table>
<tr><th>PS</th><th>MPU[1]</th><th>MPU[0]</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>8080-series 8bit interface</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>8080-series 16bit interface</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>6800-series 8bit interface</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>6800-series 16bit interface</td></tr>
<tr><td>L</td><td>L</td><td>X</td><td>3 pin SPI(Write only)</td></tr>
<tr><td>L</td><td>H</td><td>X</td><td>4 pin SPI(Write only)</td></tr>
</table></td></tr>
<tr><td>CS1B<br>CS2</td><td>I</td><td>Chip select input pins<br>Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB15 may be high impedance.</td></tr>
<tr><td>D/I<br>(RS)</td><td>I</td><td>Data / Instruction select input pin<br>– D/I = “H”: DB0 to DB15 are display data<br>– D/I = “L”: DB0 to DB7 are instruction data</td></tr>
<tr><td>WRB<br>(R/W)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>ReadWRBite control input pin<br>– R/W = “H”: read<br>– R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin<br>The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr>
</table></td></tr>
<tr><td>RDB<br>(E)</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>MPU[1]</th><th>MPU type</th><th>RDB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin<br>– R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.<br>– R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin<br>When RDB is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB[15:8]<br>DB[7]/SDI<br>DB[6]/SCL<br>DB[5:0]</td><td>I/O</td><td>-DB[15:0]: 16-bit bi-directional data bus.<br>-SDI: Serial data input pin. The data is latched at the rising edge of SCL.<br>-SCL: Serial clock input pin.</td></tr>
</table>

**Table 5. Oscillator and Power Regulator Pins**

| Name | I/O | Description |
|---|---|---|
| OSC1<br>OSC2 | O | CR oscillator output pin<br>When the internal CR oscillator is used, connect to OSC1 through a resistor.<br>OSC1 – OSC2: Using in normal display mode, partial display mode 0<br>When an external oscillator is used, OSC1 pin and OSC2 pin are connected to VSS. |
| OSC5 | I | External clock input pin<br>When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS. |
| REG_OUT | O | Internal voltage regulator output pin<br>The regulator output port from this pin is used as a power supplier for an internal digital block via VDD pins. |

**Table 6. Timing signal Pins for monitoring**

| Name | I/O | Description |
|---|---|---|
| CL | O | Shift clock output pin |
| PM | O | Field delimiter output pin |
| FR | O | Liquid crystal alternating current output pin |

**Table 7. LCD driver output pins**

| Name | I/O | Description |
|---|---|---|
| SEGA0 to 131 | O | LCD driving segment output (Red or Blue) |
| SEGB0 to 131 | O | LCD driving segment output (Green) |
| SEGC0 to131 | O | LCD driving segment output (Blue or Red) |
| COM0 to 131 | O | LCD common outputs |

**Table 9. LCD driver output pins**

| Name | I/O | Description |
|---|---|---|
| CS | O | EEPROM chip select output pin |
| SK | O | EEPROM serial clock output pin |
| E_DI | O | EEPROM serial data output pin |
| E_DO | I | EEPROM serial data input pin |

**Table 8. Test pins**

| Name | I/O | Description |
|---|---|---|

| | | |
|---|---|---|
| TEST[2:0] | I | Don't use these pins. IC maker's test pins<br>These pins must be tied to VDD3, not VDD. |

# FUNCTIONAL DESCRIPTION

## MPU INTERFACE

### Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B33B1X can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, D/I, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

### Parallel/Serial Interface

The S6B33B1X has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table9.

**Table 9. Parallel / Serial Interface Mode.**

| PS | MPU[1] | CS1B | CS2 | MPU bus type |
|---|---|---|---|---|
| H | L | CS1B | CS2 | 8080-Series MPU |
| | H | | | 6800-Series MPU |
| L | L | CS1B | CS2 | 3–Pin SPI |
| | H | | | 4-Pin SPI |

### Parallel Interface (PS="H")

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU[1] and the mode of data-bus is controlled by MPU[0] as shown in below. In accessing internal registers (D/I = "L"), only DB[7:0] are valid.

**Table 10. Microprocessor Selection for Parallel Interface**

| MPU[1] | MPU[0] | CS1B | CS2 | RDB | WRB | Data Bus | MPU bus type |
|---|---|---|---|---|---|---|---|
| L | L | CS1B | CS2 | RDB | WRB | DB[7:0] | 8080-series MPU |
| | H | | | | | DB[15:0] | |
| H | L | CS1B | CS2 | E | R/W | DB[7:0] | 6800-series MPU |
| | H | | | | | DB[15:0] | |

**Table 11. Parallel Data Transfer**

| D/I | 6800-series | | 8080-series | | Description |
|---|---|---|---|---|---|
| | RDB | WRB | RDB | WRB | |
| H | H | H | L | H | Read display data |
| H | H | L | H | L | Write display data |
| L | H | H | L | H | Read out internal status register |
| L | H | L | H | L | Write instruction data |

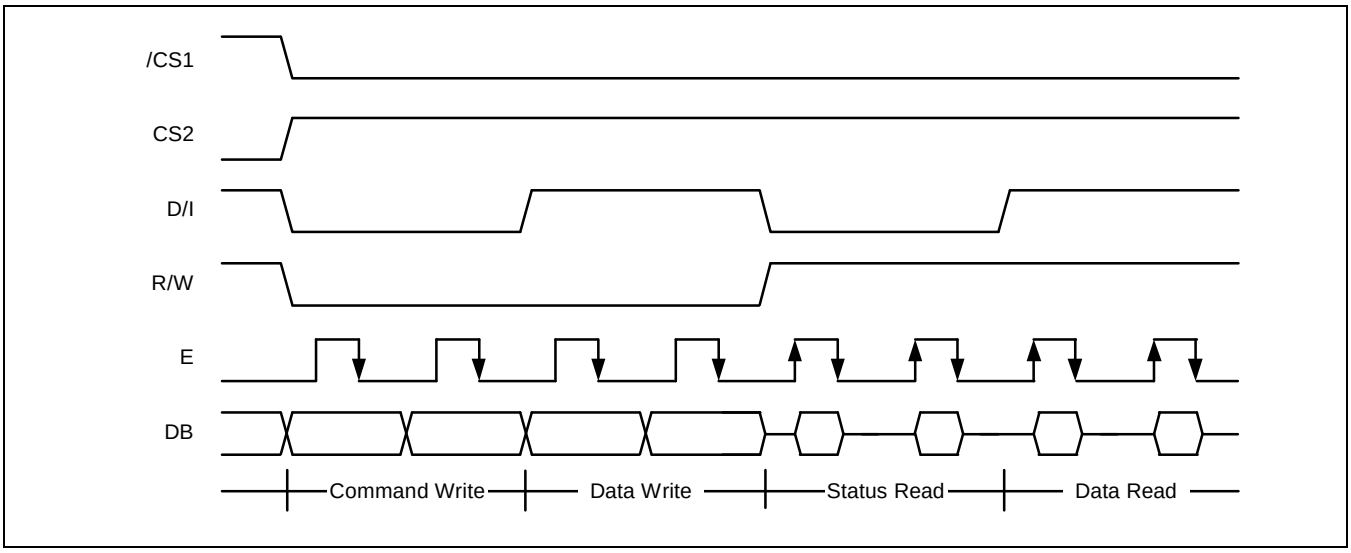



**Figure 8. 6800-Series MPU Interface protocol (MPU[1]="H")**

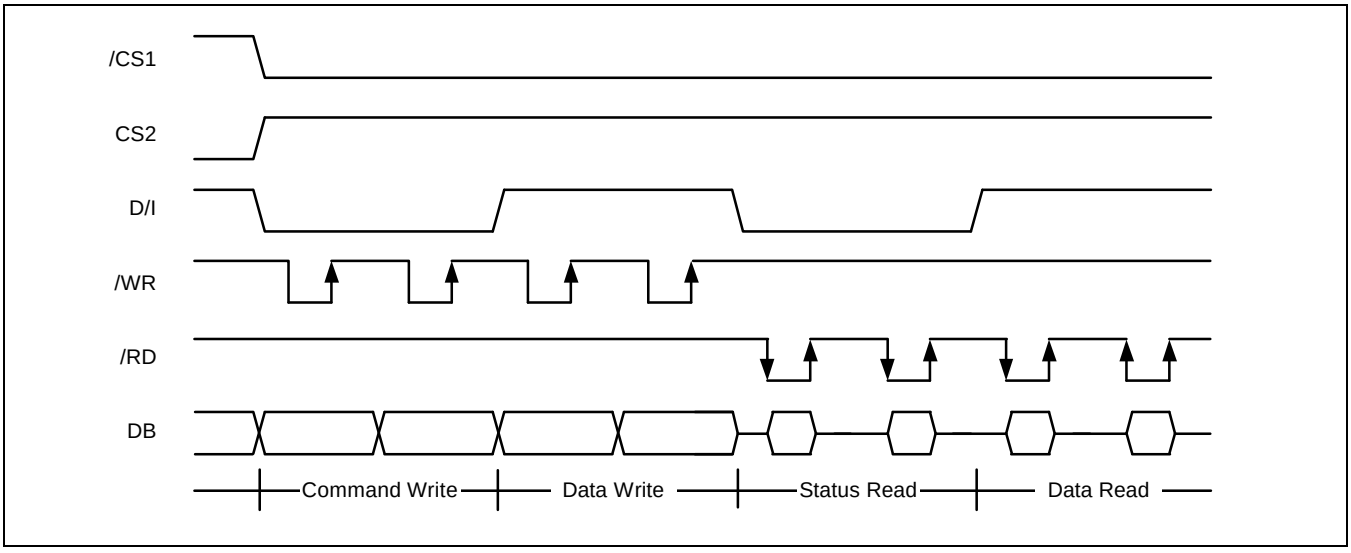



**Figure 9. 8080-Series MPU Interface Protocol (MPU[1]="L")**

### Serial Interface(PS="L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.
The serial interface type is selected by setting PS as shown in Table12.

**Table 12. Microprocessor Selection for Serial Interface**

| PS | MPU[1] | CS1B | CS2 | D/I | Serial Data | Serial Clock | SPI Mode |
|---|---|---|---|---|---|---|---|
| L | L | CS1B | CS2 | By S/W | DB[7] | DB[6] | 3-Pin |
| | H | CS1B | CS2 | D/I | | | 4-Pin |

### 3-Pin SPI Interface (PS = "L" & MPU[1] = "L")

In 3-Pin SPI Interface mode, the pre-defined instruction called Display Data Length is used to indicate whether serial data input is display or instruction data instead of D/I pin. The data is handled as instruction data until the Display Data Length instruction is issued. This Display Data Length instruction consists of three bytes instruction. The first byte instruction enables the next instruction to be valid, and data of the second two bytes indicate that a specified number of display data bytes(1 to 65536) are to be transmitted. Next two bytes after the display data string is handled as instruction data. For details, refer the Figure 8.

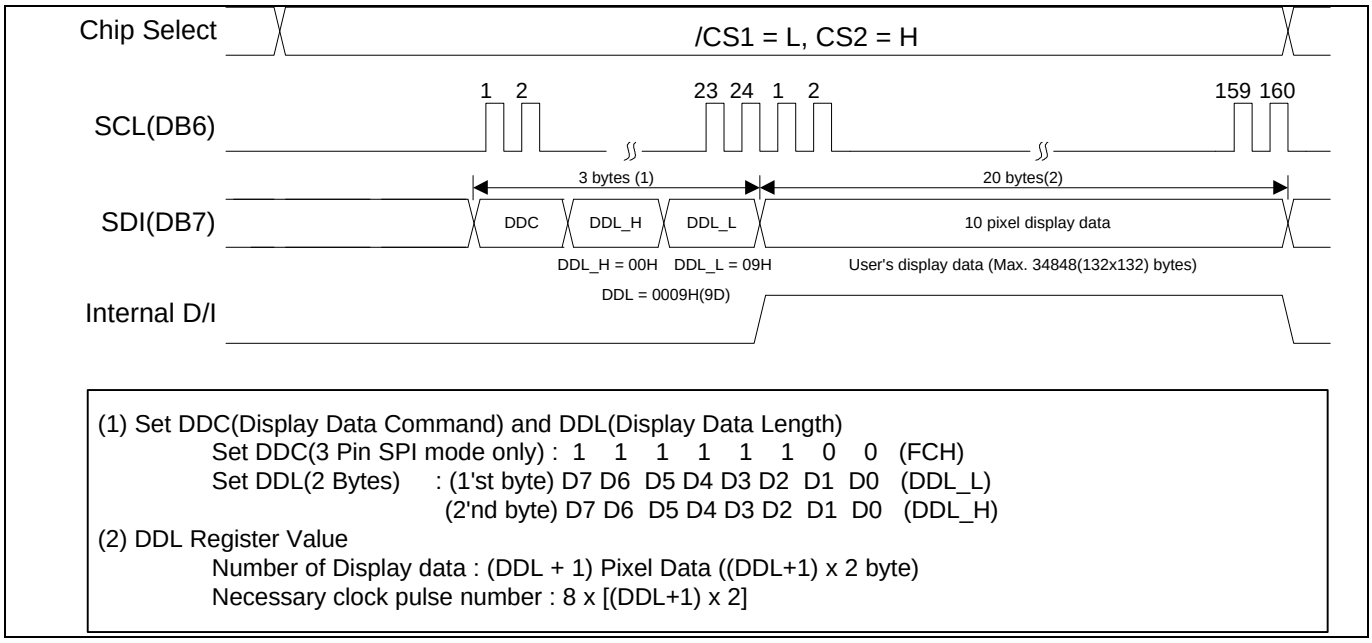



**Figure 10 3-Pin SPI Timing (D/I is not used)**

### 4-Pin Serial Interface (PS="L" & MPU[1]="H")

In 4-pin SPI interface mode, D/I pin is used for indicating whether serial data input is display or instruction data. Data is display data when D/I is high and instruction data when D/I is low.
Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.

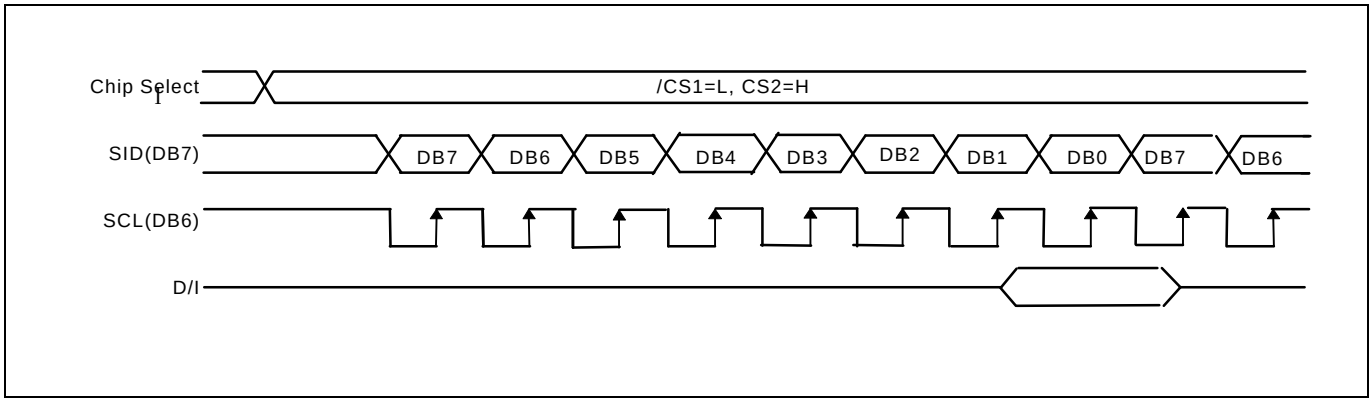



**Figure 11. 4-Pin Serial Interface Timing**

## EEPROM INTERFACE

### Chip Select output

There is CS pin for EEPROM chip selection. The EEPROM(BR93LL46F) can interface with an S6B33B1X only when CS is "H".

### EEPROM Interface Command

There are several Commands for EEPROM Interface.

| HEX | Commands | Param | Description |
|---|---|---|---|
| 80 | EEPROM Mode Out | 0 | Release EEPROM mode<br>Set data of temporary register to CR1 and CR2 if read mode |
| 81 | EEPROM Mode In | 1 | Enter EEPROM mode |
| 8C | EEPROM Read | 0 | Read from EEPROM and store it into temporary internal register |
| 8D | EEPROM Write | 0 | Write the data of CR1 and CR2 into EEPROM. |
| 70 | CR Volume Up | 0 | Increase CR volume(+1 step) |
| 71 | CR Volume Down | 0 | Decrease CR volume(-1 step) |
| 7F | Status Read Mode | 1 | Select data content at status read |

### Command Sequence

For EEPROM Read/Write, There is a regular Sequence.

| | Write Sequence | Read Sequence |
|---|---|---|
| 1 | Contrast Control Set | EEPROM Mode In(read) |
| 2 | EEPROM Mode In(write) | EEPROM Read |
| 3 | Time Wait | Time Wait |
| 4 | EEPROM Write | EEPROM Mode Out |
| 5 | Time Wait | - |
| 6 | EEPROM Mode Out | - |
| 7 | Time Wait | - |

### Data Transfer

In the EEPROM Sequence, (1)Write signal is created at EEPROM Write of Write Sequence, (2)Read signal is created at EEPROM Read of Read Sequence, (3)Write Enable signal is created at EEPROM Mode In of Write Sequence,and (4)Write Disable signal is created at EEPROM Mode Out of Write Sequence.

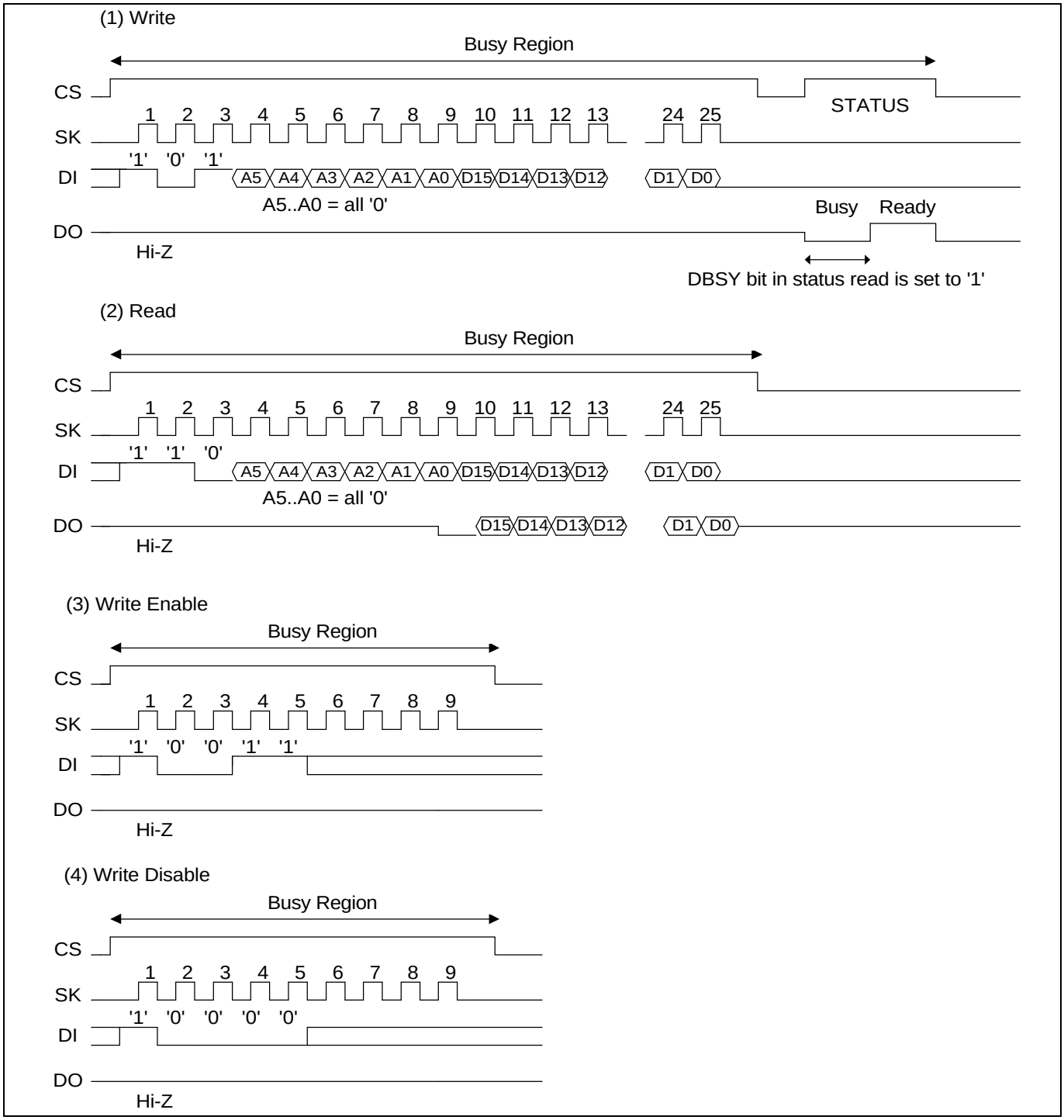



**Figure 12. Data Transfer**

### Time Wait

In the EEPROM Sequence, Time-wait is needed after the issue of EEPROM command. Wating time is needed more than 2 time of SK cycle time and don't use status read to check busy flag for time wait because busy flag in status read is not perfect to wait time. And do not execute a instruction in the Busy region.

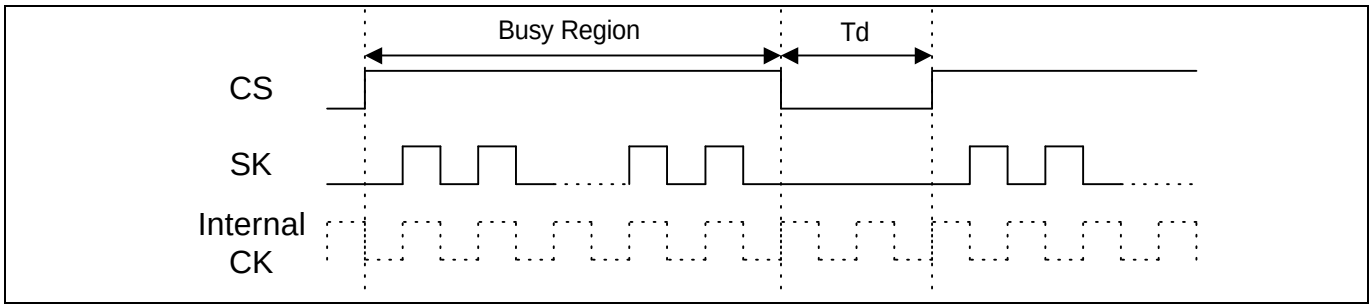



**Figure 12. EEPROM Interface Time Wait**

### EEPROM Sequence

The follow fiqure is a EEPROM Sequence Diagram.

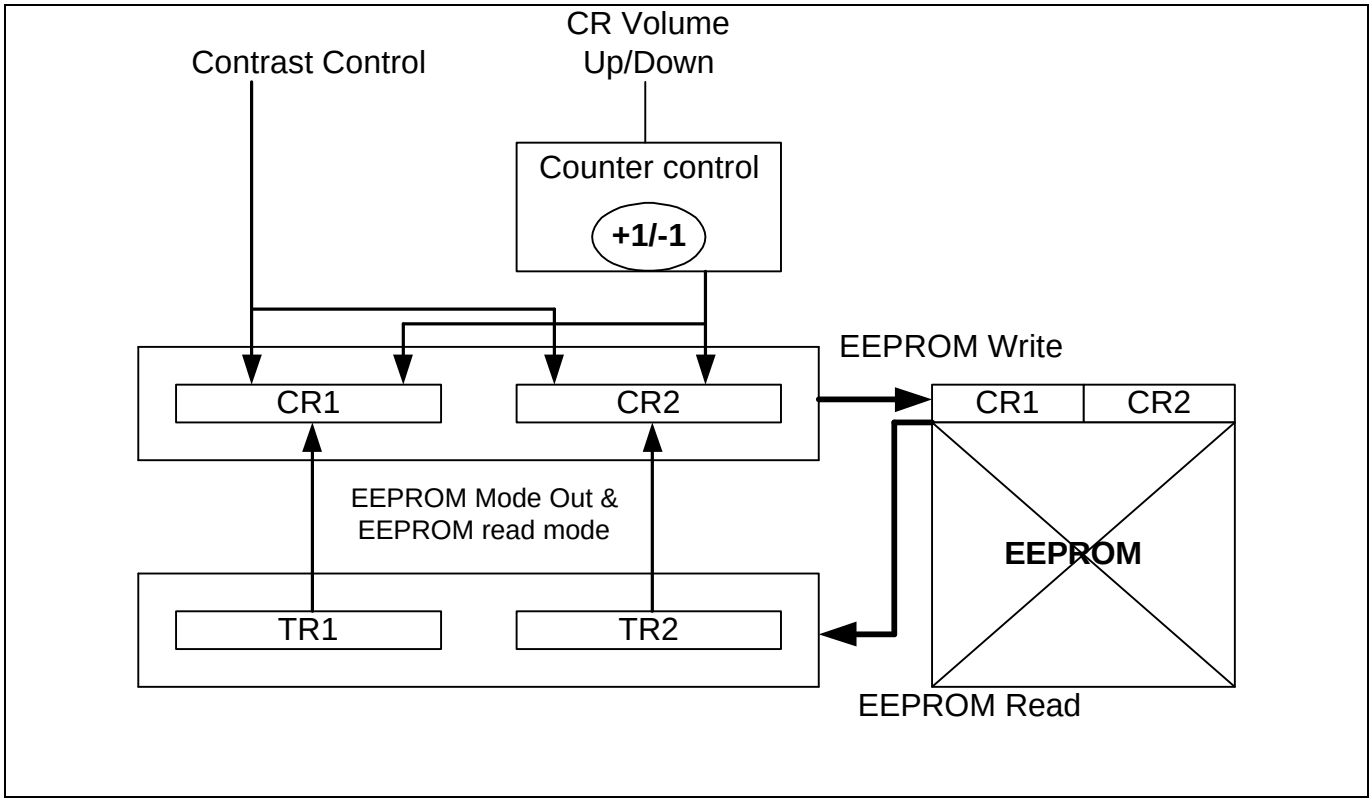



**Figure 13. EEPROM Sequence Diagram**

## DISPLAY DATA RAM

The on-chip display data RAM of S6B33B1X is a static RAM that is stored the data for the display. It is a 2,112 x 132 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

### DDRAM Address Area Selection

A part of DDRAM address area of S6B33B1X can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

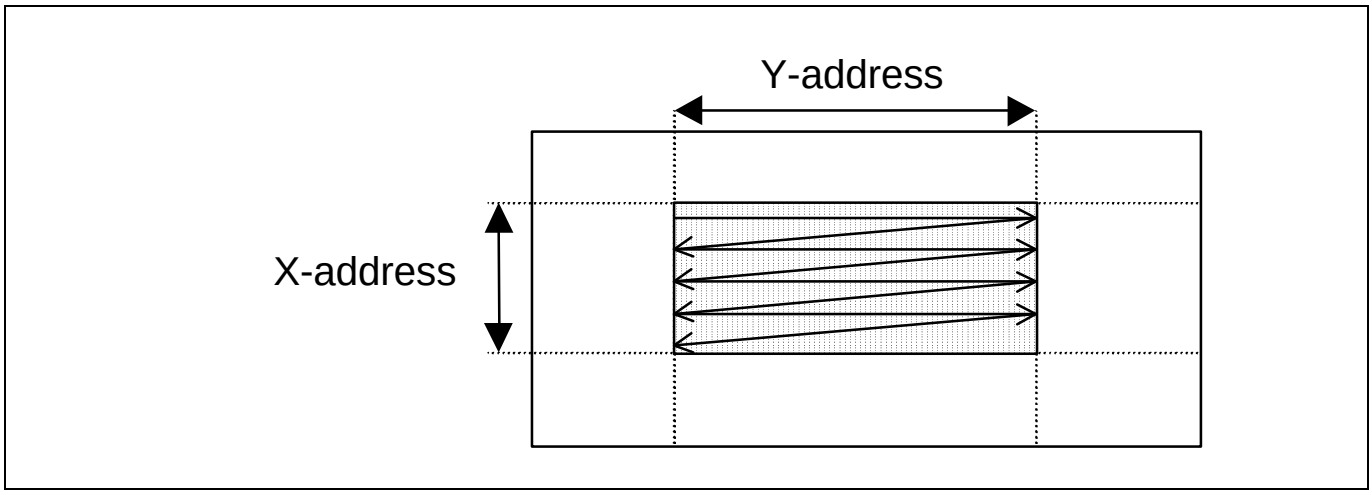



**Figure 14. DDRAM Address Area**

**Table 13. X address Control**

| | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| P1 | X start address set(Initial Status = 00H) | | | | | | | |
| P2 | X end address set(Initial Status = 83H) | | | | | | | |

**Table 14. Y address Control**

| | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| P1 | Y start address set (Initial status = 00H) | | | | | | | |
| P2 | Y end address set (Initial status = 83H) | | | | | | | |

### RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

**Y address count mode (Y address = 00h to 83h, X address = 00h to 83h)**

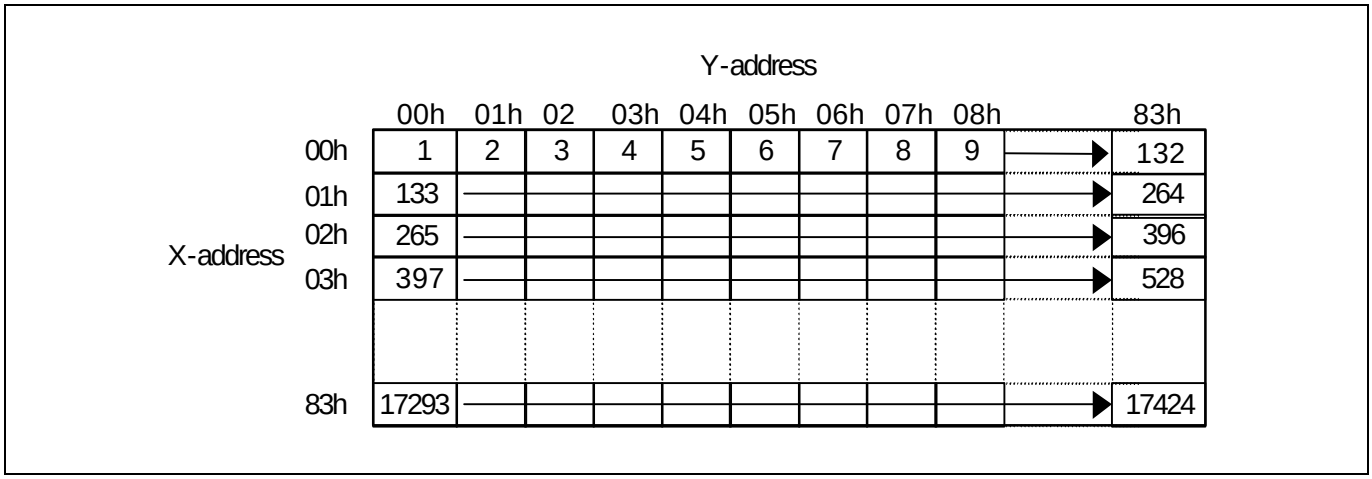



**Figure 15. Y address count mode**

**X address count mode (Y address =00h to 83h, X address = 00h to 83h)**

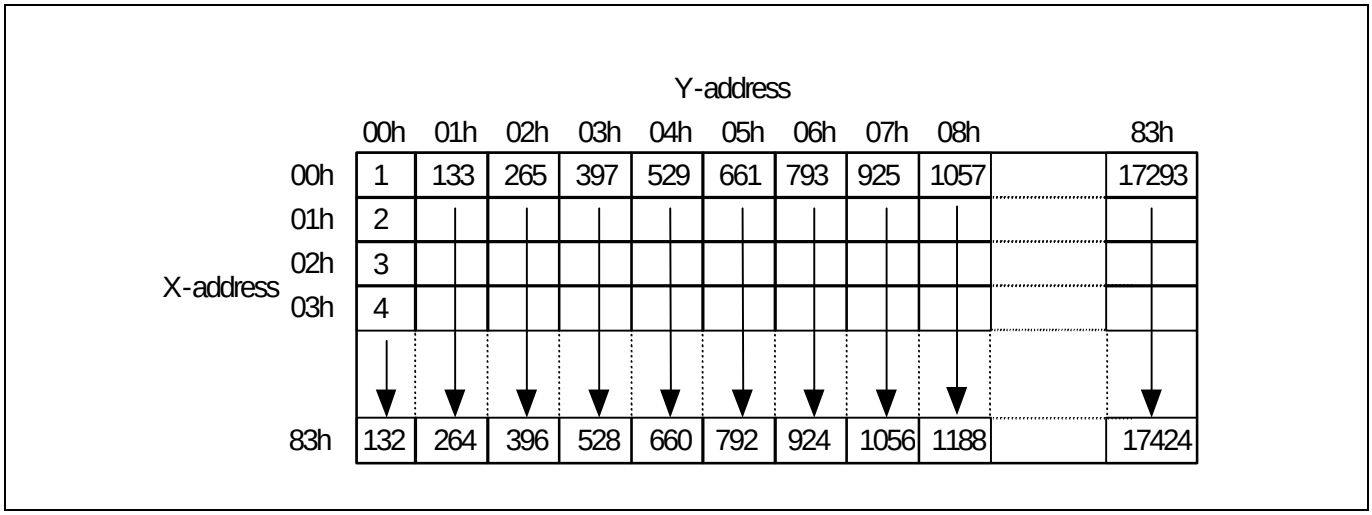



**Figure 16. X address count mode**

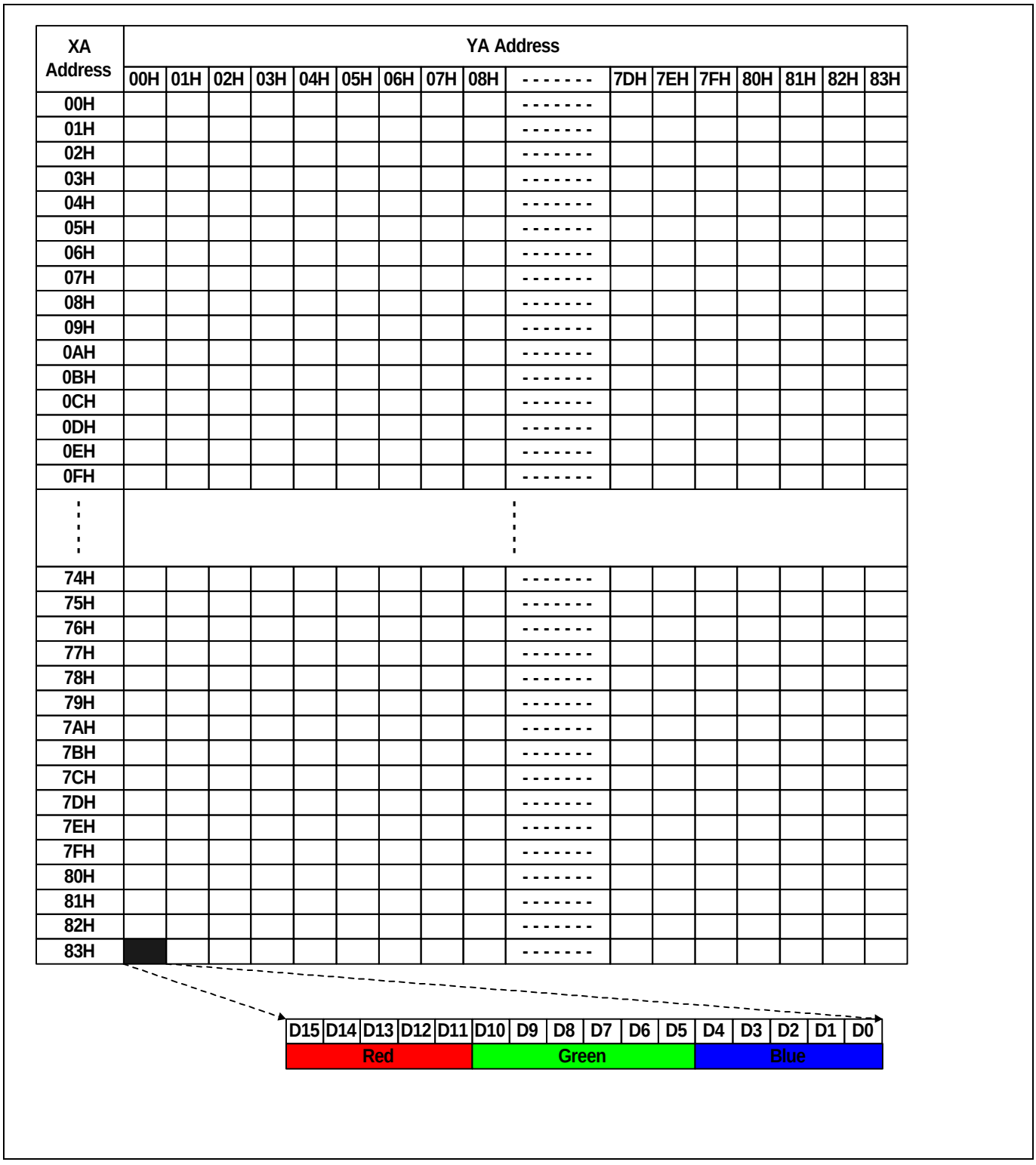



**Figure 17. Display Data RAM Map**

### Partial Display Mode

The S6B33B1X realizes the partial display function with low duty driving for saving power consumption and showing the various display duties. It is set as display start/end line number.

### Area Scroll Function

The S6B33B1X realizes the specific area scroll function. (1/132 duty case).

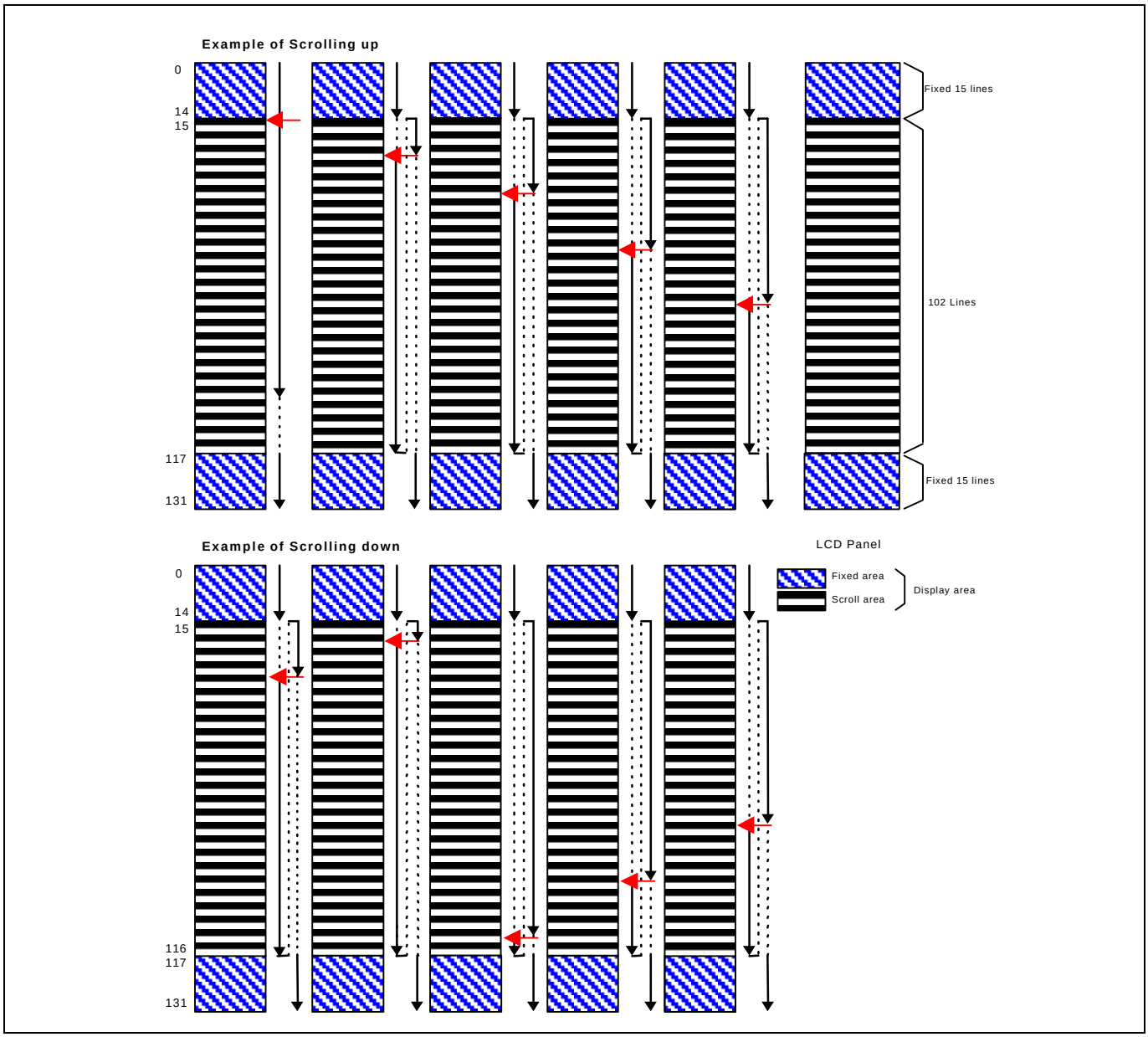



**Figure 18. Area scroll examples (duty = 1/132, center scroll mode)**

## Display Direction

### SDIR

The SDIR flag of Driver Output Mode Set instruction selects the direction of segment display.

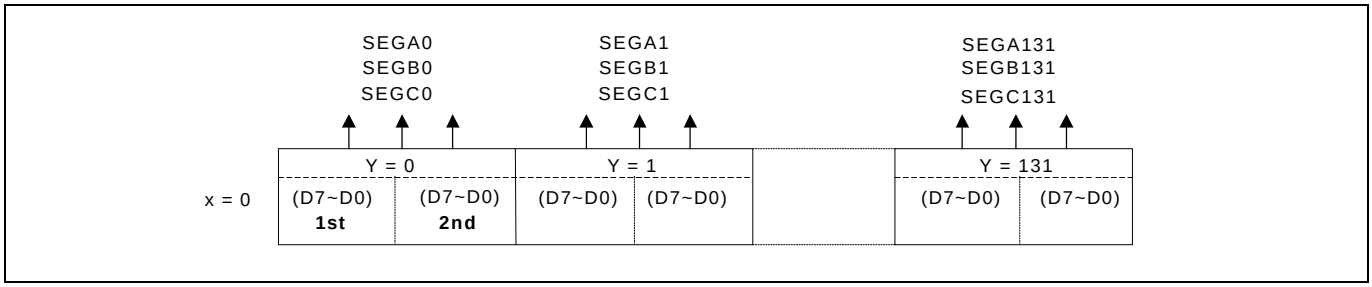



**Figure 19. 8-bit data bus mode when SDIR = 0**

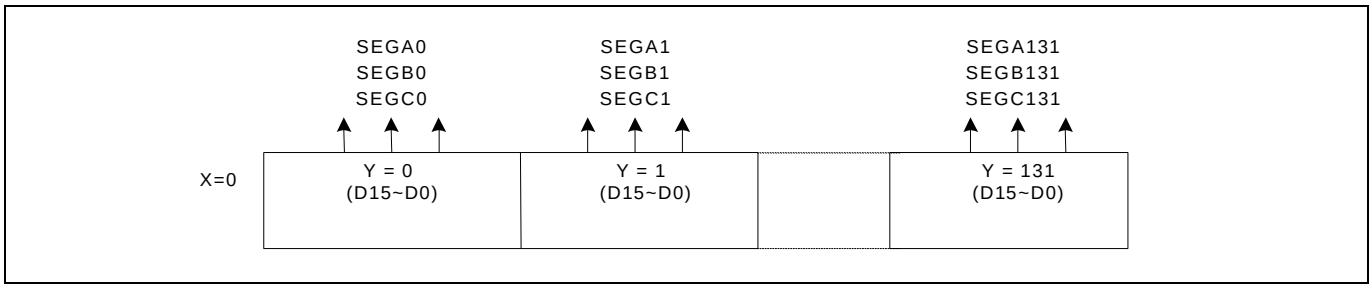



**Figure 20. 16-bit data bus mode when SDIR = 0**

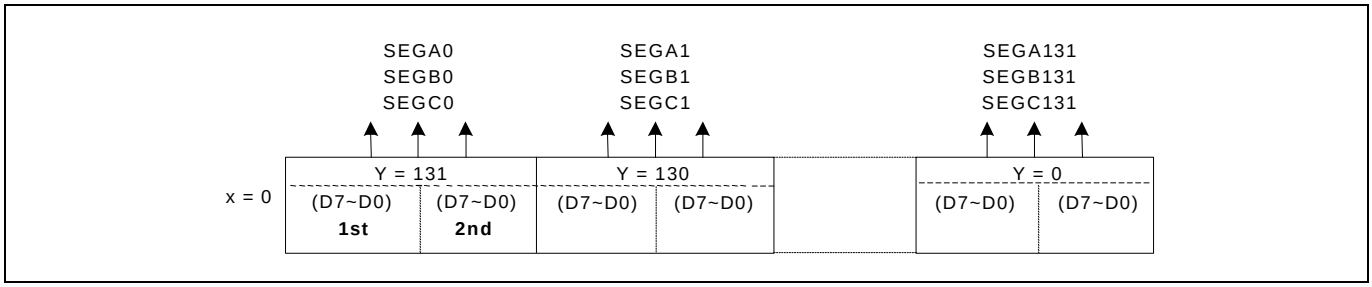



**Figure 21. 8-bit data bus mode when SDIR = 1**

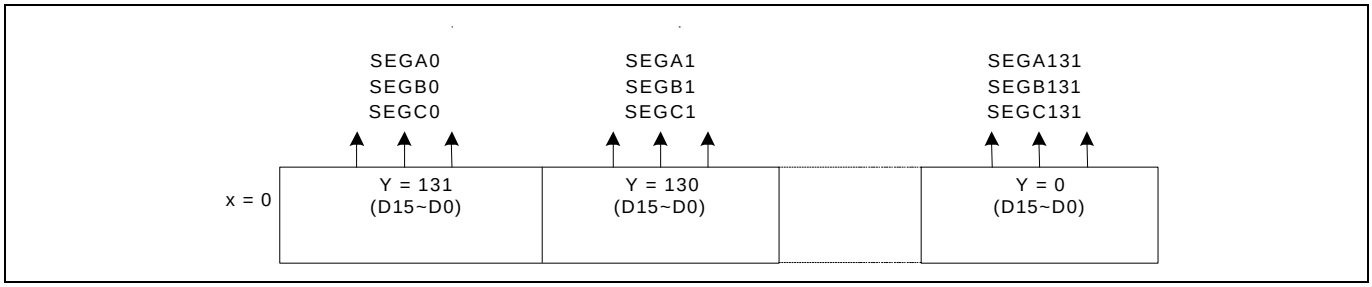
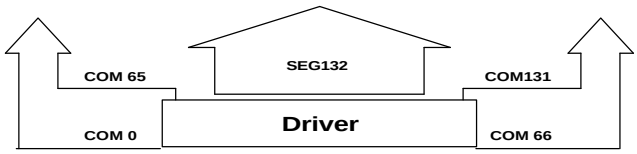


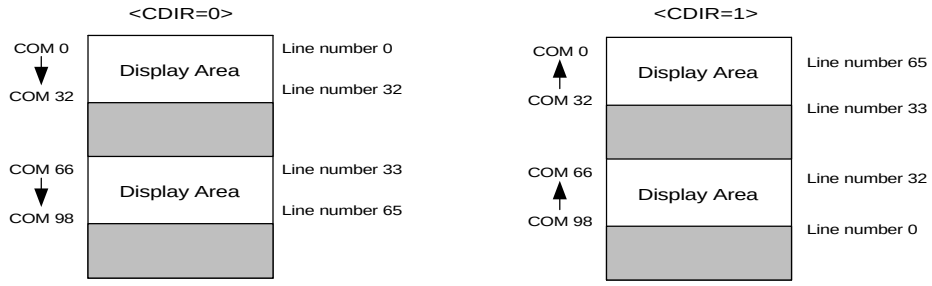

**Figure 22. 16-bit data bus mode when SDIR = 1**

## CDIR

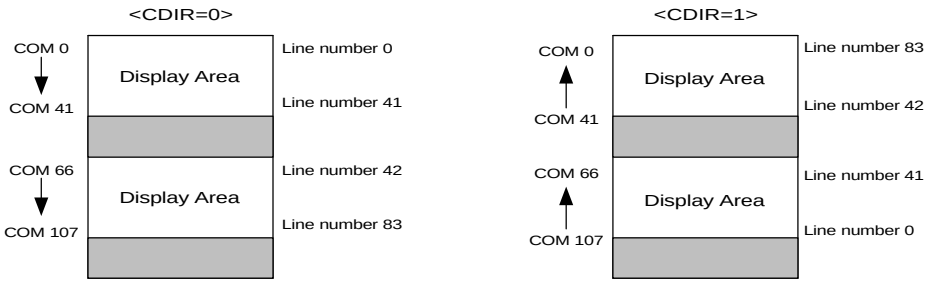
The CDIR flag of Drive Output Mode Set Instruction selects the direction of common scanning.



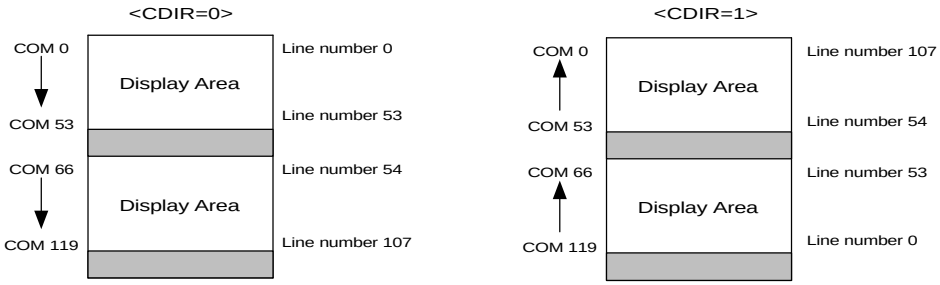

**66 Display Lines (DLN=00)**



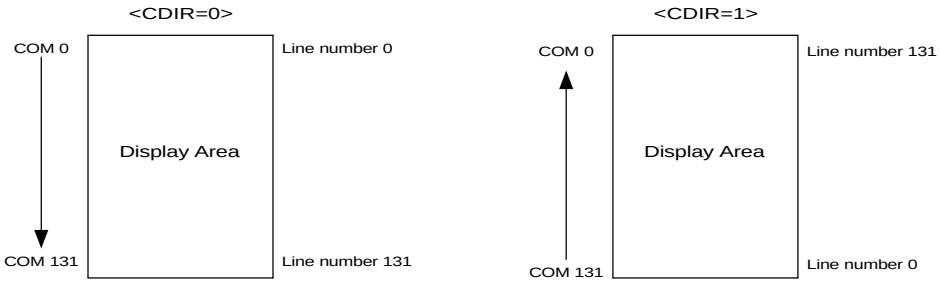

**84 Display Lines (DLN=01)**




**108 Display Lines (DLN=10)**

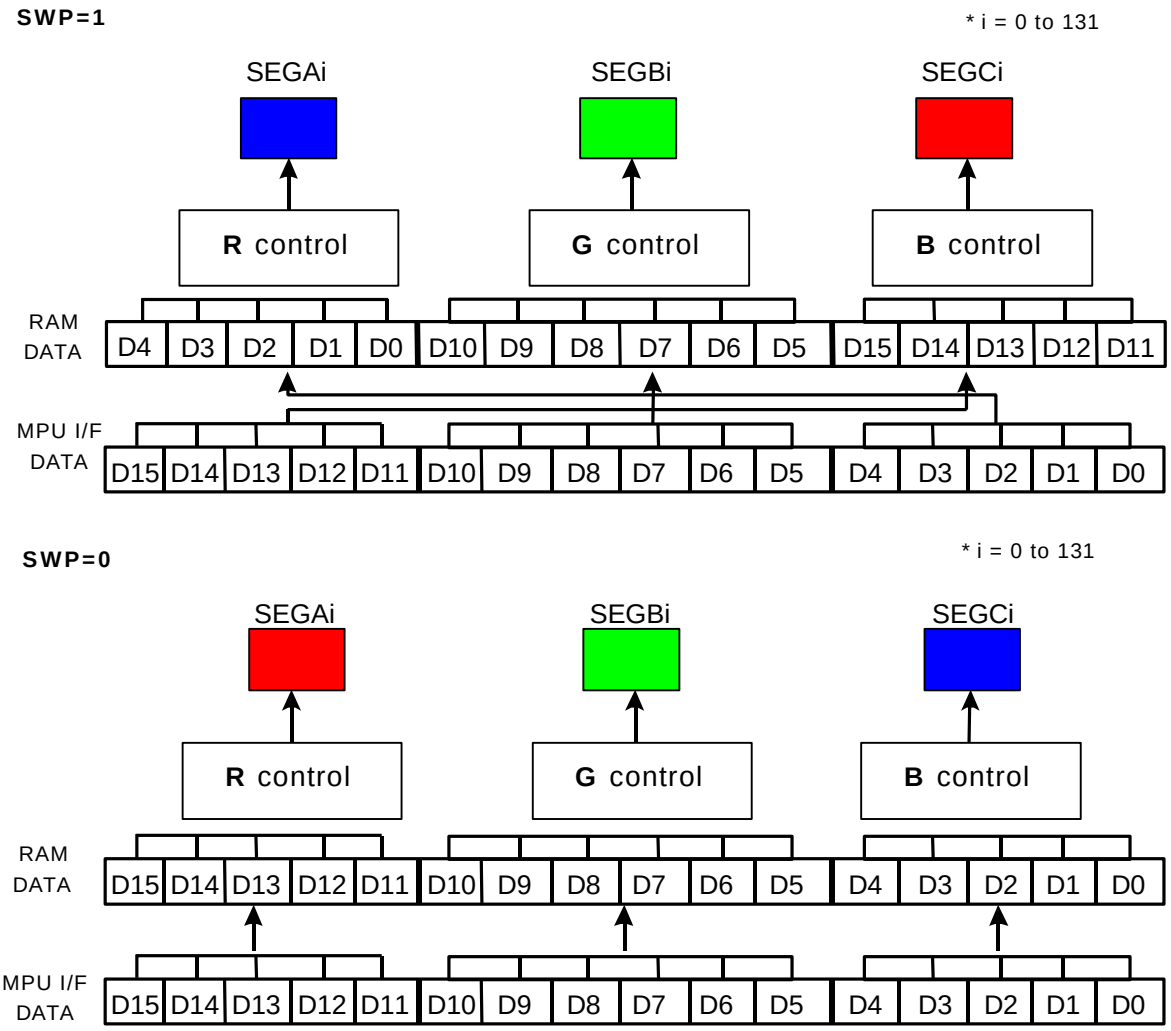



**132 Display Lines (DLN=11)**



### SWP

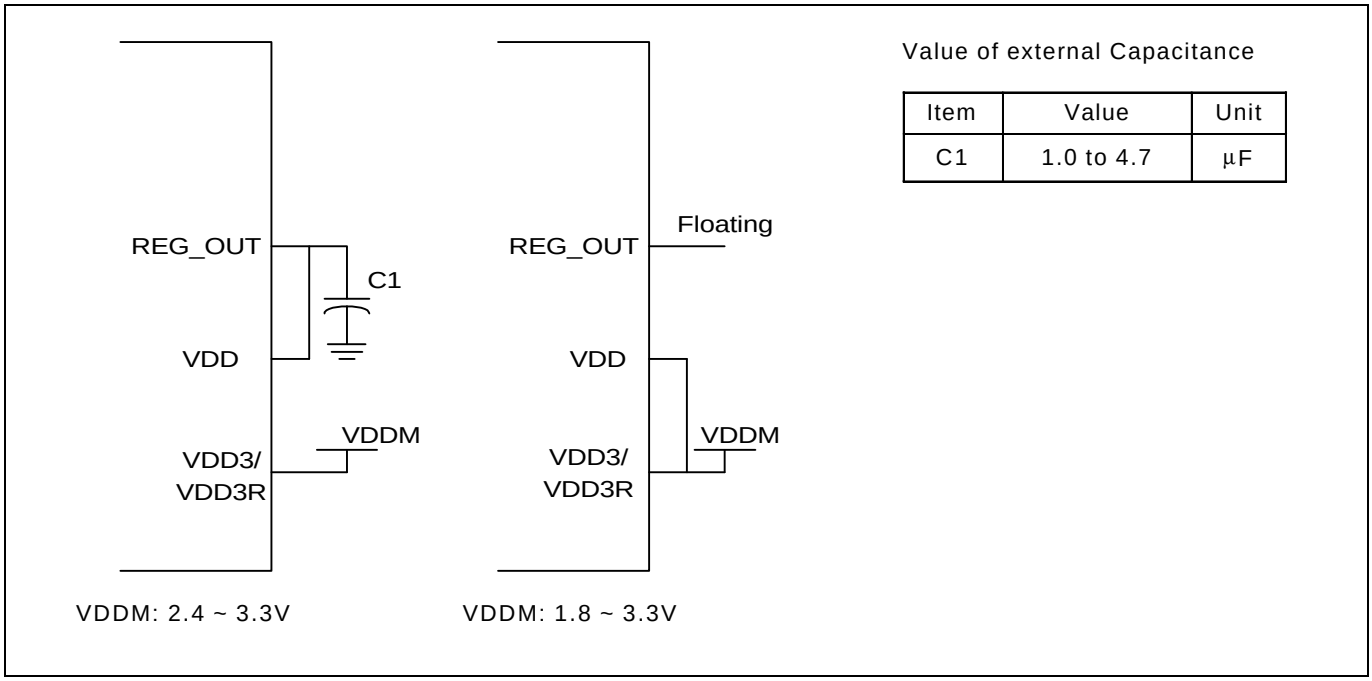
The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.




| | SEGAi | SEGBi | SEGCi | |
|---|---|---|---|---|
| SWP = 0 | RED | GREEN | BLUE | Color |
| | D15 ~ D11 | D10~ D5 | D4 ~ D0 | Assigned Bit |
| SWP = 1 | BLUE | GREEN | RED | Color |
| | D4~ D0 | D10 ~ D5 | D15 ~ D11 | Assigned Bit |

**Figure 23. The relationship between SEG outputs and RGB color**

### On-Chip Regulator Configuration




Value of external Capacitance

| Item | Value | Unit |
|---|---|---|
| C1 | 1.0 to 4.7 | µF |

**Figure 24. Regulator Application**

### Oscillator Circuit

When internal oscillator is used(EXT=0) : resistor between OSC1 and OSC2
When external clock is used (EXT=1), clock frequency should be adjusted to display mode which is selected.

### Example of external oscillator application

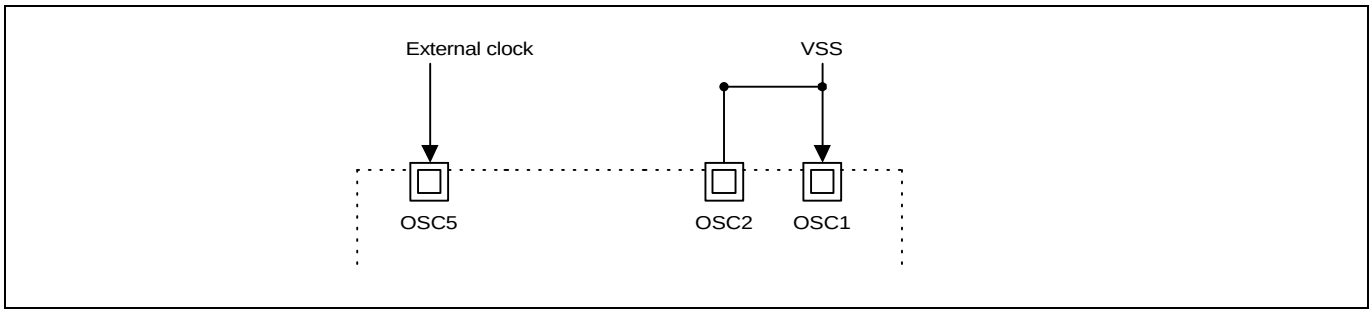



**Figure 25. External oscillator application**

### Example of internal oscillator application

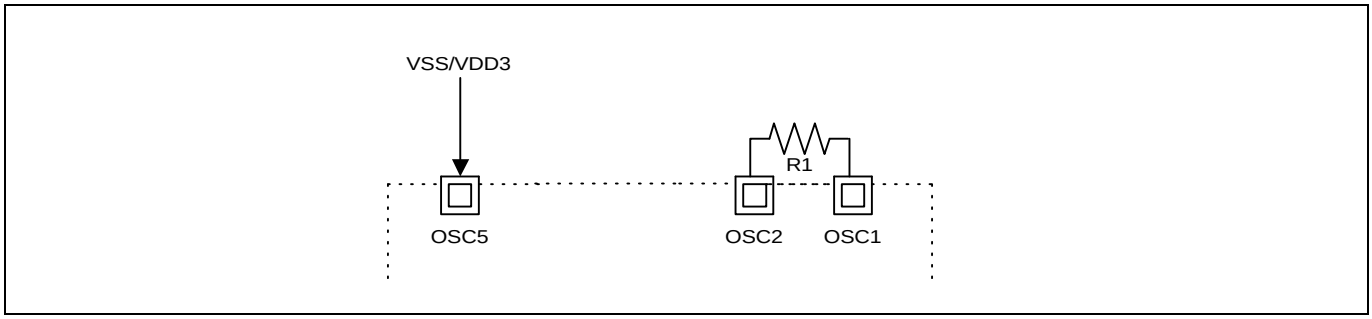
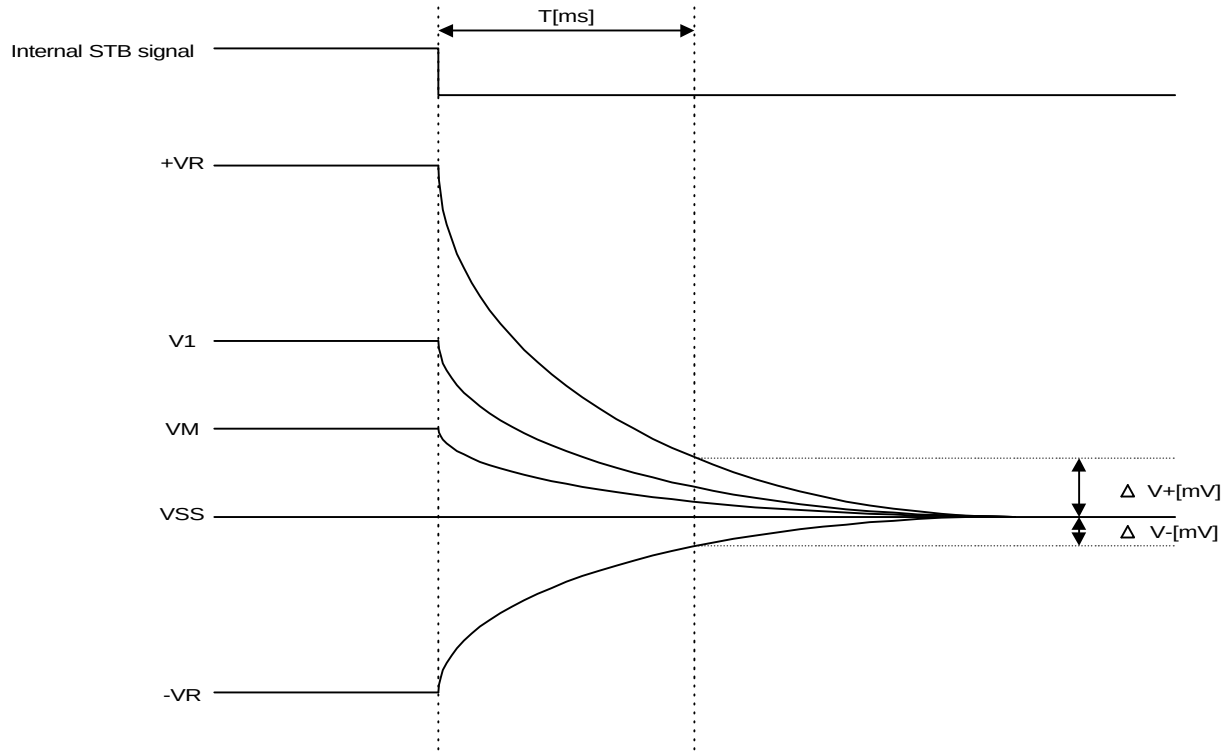



**Figure 26. Internal oscillator application**

### Discharge Circuit

Driving voltage level discharge time at standby ON.




The relation between voltage level and discharge time from when "Standby ON" command is inputted.

| LEVEL | CONDITION | T[ms] | ΔV+,ΔV-[mV] |
|---|---|---|---|
| +VR,V1,VM,-VR | +VR=12.0V, V1=3.0V, VM=1.5V, -VR=-9.0V at T=0 | 100 | < 50 |
| | | 300 | < 20 |

# INSTRUCTION DESCRIPTION

**Table 15. Instruction Table**

| Instruction Name | D/I | WRB | RDB | DB15 ~ DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Hex. | Parameter |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Non Operation | 0 | 0 | 1 | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 | |
| Oscillation Mode Set | 0 | 0 | 1 | * | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 | 1Byte |
| Driver Output Mode Set | 0 | 0 | 1 | * | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 1Byte |
| DC-DC Select | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 1Byte |
| Bias Set | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 | 1Byte |
| DCDC Clock Division Set | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24 | 1Byte |
| DCDC and AMP ON/OFF set | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 | 1Byte |
| Temperature Compensation Set | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 | 1Byte |
| Contrast Control | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A | 1Byte |
| Standby Mode OFF | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C | - |
| Standby Mode ON | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D | - |
| DDRAM Burst Mode OFF | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E | - |
| DDRAM Burst Mode ON | 0 | 0 | 1 | * | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2F | - |
| Addressing Mode Set | 0 | 0 | 1 | * | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 | 1Byte |
| ROW Vector Mode Set | 0 | 0 | 1 | * | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | 1Byte |
| N-line Inversion Set | 0 | 0 | 1 | * | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 | 1Byte |
| Entry Mode Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | 1Byte |
| X-address Area Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | 2Byte |
| Y-address Area Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | 2Byte |
| RAM Skip Area Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 | 1Byte |
| Display OFF | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 | - |
| Display ON | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 | - |
| Specified Display Pattern Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 | 1Byte |
| Partial Display Mode Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55 | 1Byte |
| Partial Display Start Line Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56 | 1Byte |
| Partial Display End Line Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 57 | 1Byte |
| Area Scroll Mode Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 59 | 4Byte |
| Scroll Start Line Set | 0 | 0 | 1 | * | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A | 1Byte |
| CR Volume Up | 0 | 0 | 1 | * | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70 | - |
| CR Volume Down | 0 | 0 | 1 | * | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 | - |
| Status Read Mode | 0 | 0 | 1 | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F | 1Byte |
| EEPROM Mode Out | 0 | 0 | 1 | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | - |
| EEPROM Mode In | 0 | 0 | 1 | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 | 1Byte |
| EEPROM Read | 0 | 0 | 1 | * | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 8C | - |
| EEPROM Write | 0 | 0 | 1 | * | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 8D | - |
| Set Display Data Length | X | X | X | * | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FC | 1Byte |
| Display Data Write | 1 | 0 | 1 | Display Data Write | | | | | | | | | - | - |
| Display Data Read | 1 | 1 | 0 | Display Data Read | | | | | | | | | - | - |
| Status Read | 0 | 1 | 0 | 0 | Status Data Read | | | | | | | | - | - |
| Test Mode1 | 0 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF | - |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Test Mode2 | 0 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FE | - |
| Test Mode3 | 0 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FD | - |
| Test Mode4 | 0 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | FB | - |
| Test Mode5 | 0 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | FA | - |
| Test Mode6 | 0 | 0 | 1 | * | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | F9 | - |

*: Don't care

Parameter: The number of parameter bytes that follows instruction data.

### Non Operation (00H)

This instruction is Non operation.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Oscillation Mode Set (02H)

Setting internal function mode.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | 0 | 0 | 0 | 0 | 0 | DIV2 | EXT | OSC |

DIV2: Display clock selecting
DIV2 = 0: Display clock = OSC clock (Initial status)
DIV2= 1: Display clock = OSC/2 clock

EXT: External clock selecting
EXT = 0: Internal clock mode (Initial status)
EXT = 1: External clock mode

OSC: Internal oscillator ON/OFF
OSC = 0: Internal oscillator OFF(Initial status)
OSC = 1: Internal oscillator ON

### Driver Output Mode Set(10H)

This instruction sets the display direction.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | | | 0 | 0 | DLN | | 0 | SDIR | SWP | CDIR |

DLN: Display Line number selecting

| DB5 | DB4 | Display Duty |
|---|---|---|
| 0 | 0 | 1/66 |
| 0 | 1 | 1/84 |
| 1 | 0 | 1/108 |
| 1 | 1 | 1/132 |

SDIR: Segment direction
This bit is for controlling the direction of segment driver.
SDIR = 0 (Initial status)
SWP: Swap segment output SEGAi and SEGCi
This bit is for swapping the output of segment driver.
SWP = 0 (Initial status)
CDIR: Common direction
This bit is for controlling the direction of common driver.
CDIR = 0 (Initial status)

### DC-DC Select (20H)

Selects DC-DC step-up of the common driver in normal and partial mode

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DC |

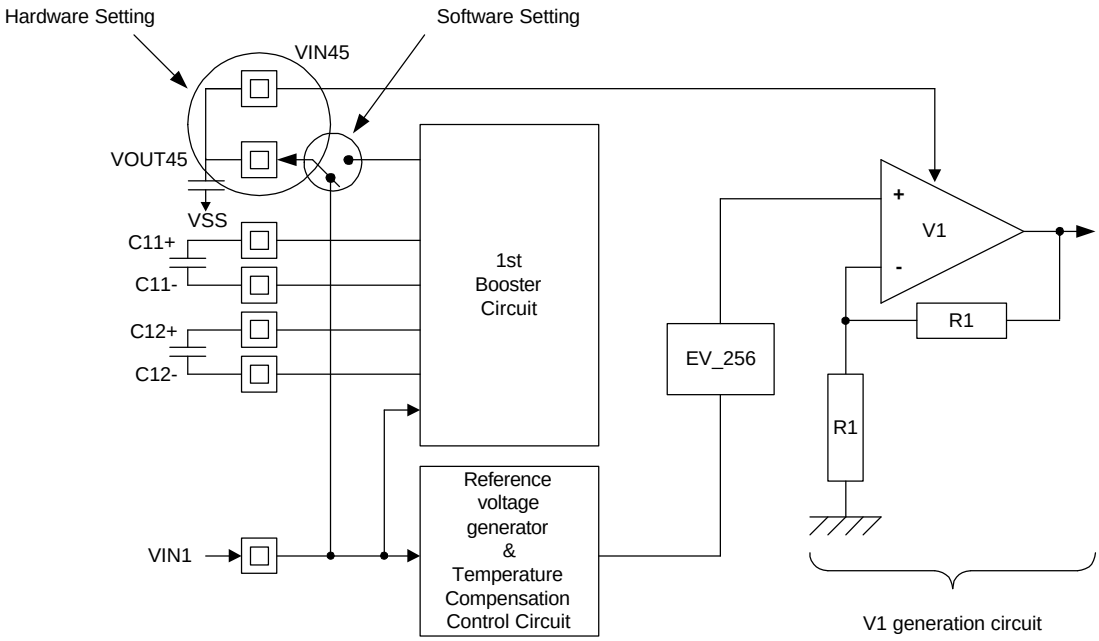
| DC : In normal mode, partial mode | |
|---|---|
| DB1 | DC-DC step up |
| 0 | X1.0 |
| 0 | X1.5 |

**DC-DC Select and power supply for V1 Op-Amp.**

Even if VIN45 is connected to VOUT45 or VIN1, a setup by software must be able to be performed. Power supply for V1 Op.Amp. is decided by Hardware setting and Software setting.

The example of usage is shown below.

Figure28. Example : Hardware Setting : VIN45 connected to VOUT45
Software Setting : Power supply for V1 Op.Amp. uses VIN1 ( not VOUT45).




Hardware setting : VIN45 connected to (1) VIN1 (when 1' st boosting is not used)
(2) VOUT45 (when 1' st boosting is used)

Software setting : DC-DC Select(20H) - DC
Set value "0" Power supply for V1 Op.Amp. uses VIN1 directly.
Set value "1" Power supply for V1 Op.Amp. uses VOUT45.

### Bias Set (22H)

This instruction set up the value of bias in normal mode and in partial mode.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Bias |

| Bias | | |
|---|---|---|
| DB0 | Bias | 2'nd boosting step |
| 0 | 1/5 | x(-4) |
| 1 | 1/6 | x(-4) |

### DCDC Clock Division Set(24H)

This instruction sets the internal booster clock frequency.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| | | | 0 | 0 | 0 | 0 | 0 | DIV | | |

DIV : DC-DC Charge Pump Division Ratio in Normal Mode Display and Partial Display Mode
- DIV = 101 (Initial status)

| DB2 | DB1 | DB0 | DIV |
|---|---|---|---|
| 0 | 0 | 0 | fPCK = fOSC/2 |
| 0 | 0 | 1 | fPCK = fOSC/4 |
| 0 | 1 | 0 | fPCK = fOSC/6 |
| 0 | 1 | 1 | fPCK = fOSC/8 |
| 1 | 0 | 0 | fPCK = fOSC/10 |
| 1 | 0 | 1 | fPCK = fOSC/12 |
| 1 | 1 | 0 | fPCK = fOSC/14 |
| 1 | 1 | 1 | fPCK = fOSC/16 |

Note: fOSC = ( ROUNDUP (Duty/3) + dummy) x 4 x 8 x frame frequency

### DC/DC and AMP ON/OFF Set (26H)

This instruction set up the DC/DC and Op-amp in common start up setting.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| | | | 0 | 0 | 0 | 0 | AMP | DCDC3 | DCDC2 | DCDC1 |

AMP: Built-in OP-AMP ON/OFF.
- AMP=0: OP-AMP OFF (Initial status)
- AMP=1: OP-AMP ON

DCDC1: Built-in 1' st Booster ON/OFF (Initial status)
- DCDC1= 0: 1' st Booster OFF (Initial status)
- DCDC1= 1: 1' st Booster ON

DCDC2: Built-in 2' nd Booster ON/OFF (Initial status)
- DCDC2= 0: 2' nd Booster OFF (Initial status)
- DCDC2= 1: 2' nd Booster ON

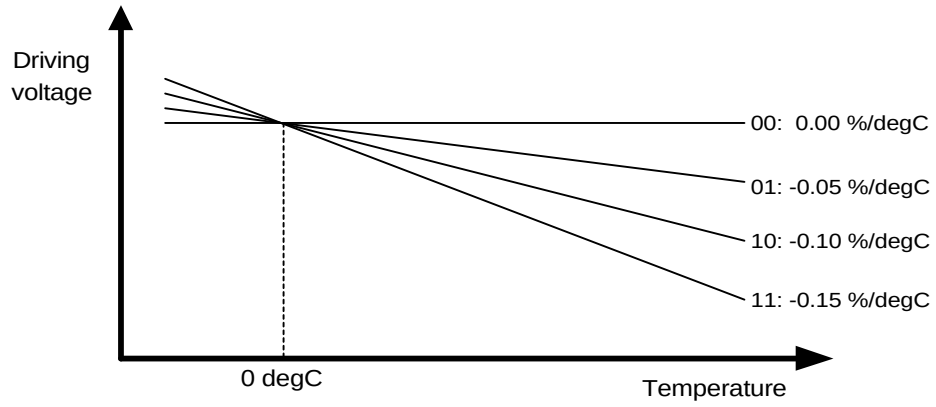
DCDC3: Built-in 3' rd Booster ON/OFF (Initial status)
- DCDC3= 0: 3' rd Booster OFF (Initial status)
- DCDC3= 1: 3' rd Booster ON

### Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

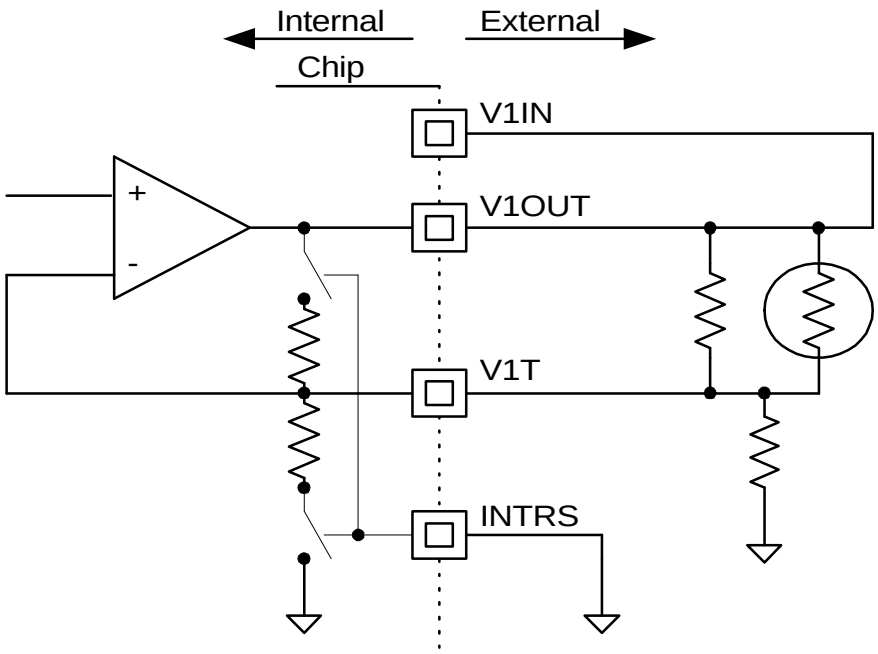
| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | TCS | |

TCS: Temperature compensation slope set
- TCS = 00 : 0.00%/degC (Initial status)
- TCS = 01 : -0.05%/degC
- TCS = 10 : -0.10%/degC
- TCS = 11 : -0.15%degC



**Temperature Compensation**

If external temperature compensation is needed, circuit diagram is described as below.
To use temperature compensation, two resistors and one thermistor are needed.



### Contrast Control (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode 0.

| D/I | /WR | /RD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | | | Contrast control value (0 to 255) | | | | | | | |

The relation between V1 voltage (typ.) and Contrast set value ( 3bit step case)

| Contrast(1) (HEX) | V1[V] | Contrast(1) (HEX) | V1[V] | Contrast(1) (HEX) | V1[V] | Contrast(1) (HEX) | V1[V] | Contrast(1) (HEX) | V1[V] | Contrast(1) (HEX) | V1[V] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | 2.000 | 30h | 2.244 | 60h | 2.488 | 90h | 2.731 | C0h | 2.975 | F0h | 3.219 |
| 08h | 2.041 | 38h | 2.284 | 68h | 2.528 | 98h | 2.772 | C8h | 3.016 | F8h | 3.259 |
| 10h | 2.081 | 40h | 2.325 | 70h | 2.569 | A0h | 2.813 | D0h | 3.056 | FFh | 3.300 |
| 18h | 2.122 | 48h | 2.366 | 78h | 2.609 | A8h | 2.853 | D8h | 3.097 | | |
| 20h | 2.163 | 50h | 2.406 | 80h | 2.650 | B0h | 2.894 | E0h | 3.138 | | |
| 28h | 2.203 | 58h | 2.447 | 88h | 2.691 | B8h | 2.934 | E8h | 3.178 | | |

### Standby Mode OFF (2CH)

This instruction releases the standby mode.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

The internal statuses during standby off are as following:

- All common and segment output: VSS or V1
- Oscillator circuit: On (EXT = 0, OSC=1),OFF (others)
- Displaying clocks (FR, PM, CL): In operation

Function and Pin condition at standby OFF

| Function/Pin | Condition |
|---|---|
| DC/DC booster(1' st,2' nd,3' rd) | ON(Operate) |
| COM outputs | +VR or VM or VSS or -VR |
| SEG outputs | V1 or VSS |

### Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

The internal statuses during standby on are as following:

- All common and segment output: VSS
- Oscillator circuit: OFF
- Displaying clocks (FR, PM, CL) are held.

Function and Pin condition at standby ON

| Function/Pin | Condition |
|---|---|
| DC/DC booster(1' st,2' nd,3' rd) | OFF |
| SEG and COM outputs | VSS |

LCD driving power output condition at Standby ON.

| level | Condition |
|---|---|
| +VR | VSS |
| V1 | VSS |
| VM | VSS |
| -VR | VSS |

**DDRAM Burst Mode OFF(2EH) /ON(2FH)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | BM |

BM: Internal DDRAM Burst Mode Interface Off/On Control
- 0 : Burst Mode Interface Off(Initial Status)
- 1 : Burst Mode Interface On

When BM=0, If MPU[0] is 0 then internal DDRAM I/F bpw(bits per word) is 8 bits.
Else MPU[0] is 1 then internal DDRAM I/F bpw(bits per word) is 16bits.
When BM=1, Regardless of MPU[0] bit, Internal DDRAM I/F bpw(bits per word) is 32 bits.

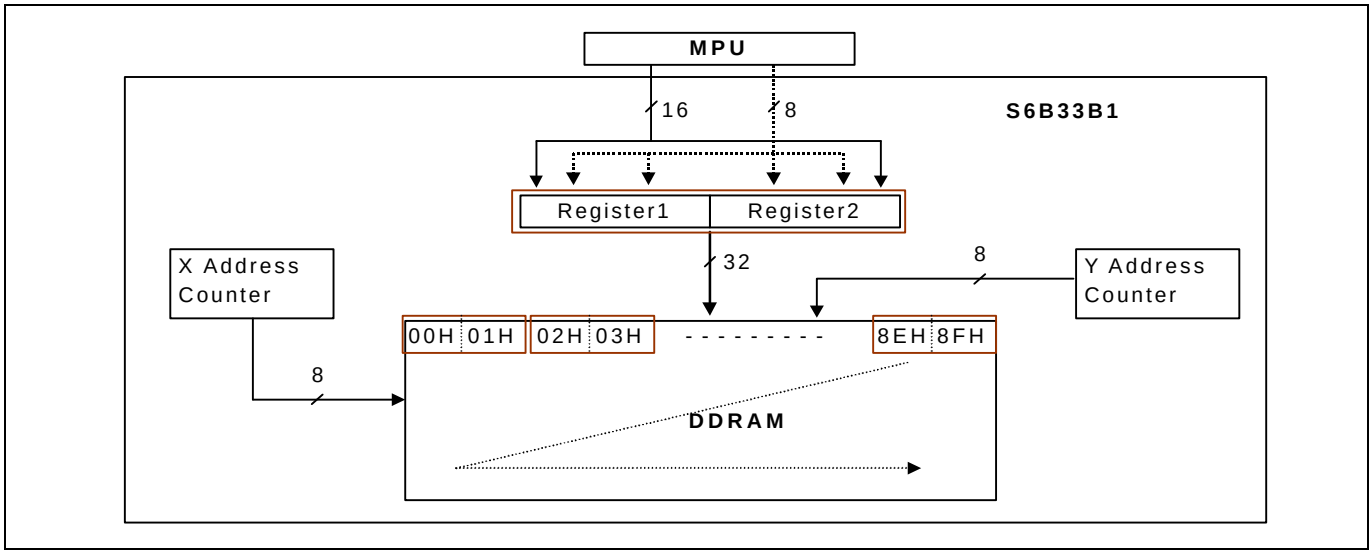



**Figure 27. Burst mode writing to DDRAM**

When burst mode is on, It is impossible to use X-address count mode(Page56), but there is a advantage because MPU access cycle time is about 1.5 times faster than the cycle time of Burst Mode Off.

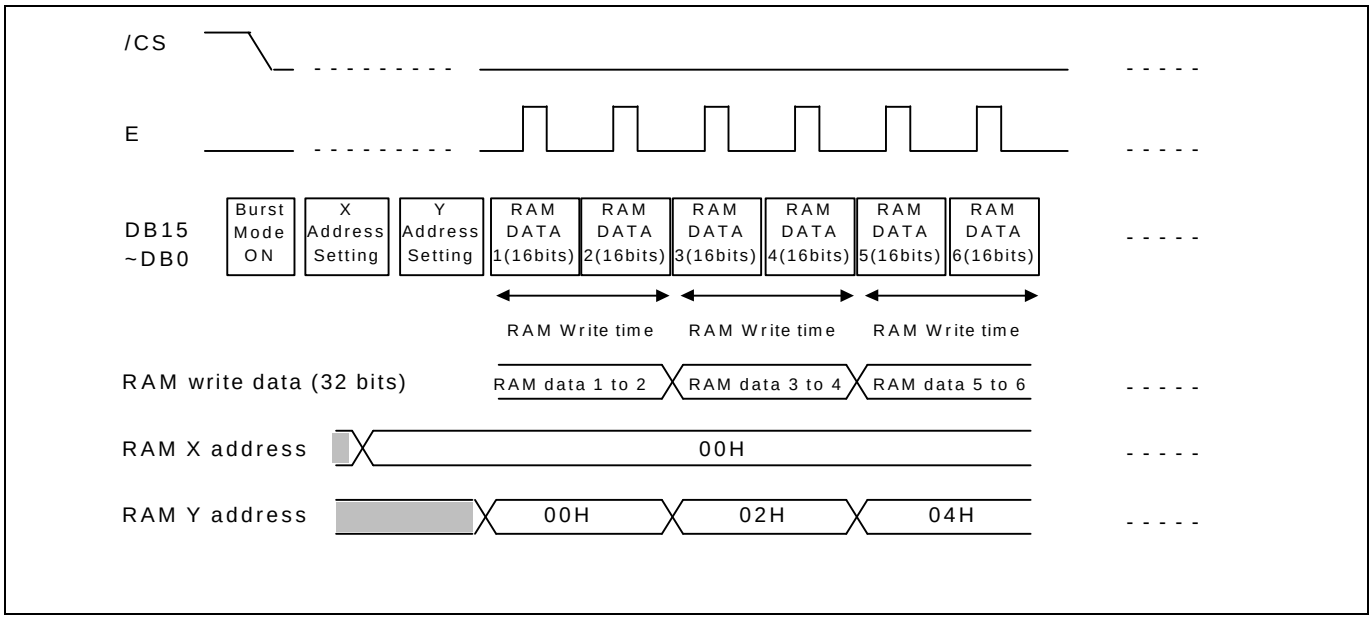



**Figure 28. Example of the Burst mode writing to DDRAM (68-mode 16-bit parallel interface)**

When DDRAM burst mode is used, note the following.
Notes:

1. Data is written to DDRAM each two words. If only one word data is written to DDRAM, the data will not be written.
   So, the number of word data must be even. It means that Y start address must be even and Y end address must be odd.
2. X address count mode can't be used.
3. Burst mode and normal mode write operation cannot be executed at the same time.
4. In the read data mode and serial interface mode, the burst mode can't be used.
5. In the 256 color mode with 16-bit data bus mode and 4,096 color mode with 8-bit data bus mode, The address is counted as burst mode enable. So these modes are influenced by above notes.

**Addressing Mode Set (30H)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | | | 0 | GSM | | DSG | SGF | SGP | | SGM |

GSM: Gray Scale Mode
- 00 : 65,536 color mode(Initial status)
- 01 : 4,096 color mode (refer to “Data Format Select(60H/61H)”)
- 10 : 256 color mode
- 11 : 256 color mode

DSG : Duty Adjust Setting
- 0 : Dummy subgroup is one subgroup (Initial status)
- 1 : Dummy subgroup is none

SGF : Sub Group Frame Inversion mode setting
- 0: SG Frame inversion OFF (Initial status)
- 1: SG Frame inversion ON

SGM : Sub Group inversion mode setting
- 0: SG inversion OFF (Initial status)
- 1: SG inversion ON

SGP : Sub Group Phase mode setting
- 00 : Same phase in all pixels
- 01 : Different phase by 1pixel-unit
- 10 : Different phase by 2pixel-unit
- 11 : Different phase by 4pixel-unit

**Row Vector Mode Set (32H)**

Setting ROW function.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| | | | 0 | 0 | 0 | 0 | INC | | | VEC |

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

| DB3 | DB2 | DB1 | Row Vector Increment Period |
|---|---|---|---|
| 0 | 0 | 0 | Every subgroup |
| 0 | 0 | 1 | Every 2subgroup |
| 0 | 1 | 0 | Every 4subgroup |
| 0 | 1 | 1 | Every 8subgroup |
| 1 | 0 | 0 | Every 16subgroup |
| 1 | 0 | 1 | Every 16subgroup |
| 1 | 1 | 0 | Every 16subgroup |
| 1 | 1 | 1 | Every subframe |

VEC: ROW Vector Sequence Mode
- 0: R1->R2->R3->R4 -> R1 …. (initial status)
- 1: R1->R3->R2->R4 -> R1 ….

### 256 Color Mode Palettes

At 256-color mode, the instruction and parameter below set each Gray Scale level of the Red/Green/Blue. Gray scale level is determined by GS data.

**Red Palette (38H)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| | | | 0 | 0 | 0 | GS data “000” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “001” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “010” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “011” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “100” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “101” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “110” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “111” to RAM data | | | | |

**Green Palette (3AH)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| | | | 0 | 0 | GS data “000” to RAM data | | | | | |
| | | | 0 | 0 | GS data “001” to RAM data | | | | | |
| | | | 0 | 0 | GS data “010” to RAM data | | | | | |
| | | | 0 | 0 | GS data “011” to RAM data | | | | | |
| | | | 0 | 0 | GS data “100” to RAM data | | | | | |
| | | | 0 | 0 | GS data “101” to RAM data | | | | | |
| | | | 0 | 0 | GS data “110” to RAM data | | | | | |
| | | | 0 | 0 | GS data “111” to RAM data | | | | | |

**Blue Palette (3CH)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | 0 | 0 | 0 | GS data “00” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “01” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “10” to RAM data | | | | |
| | | | 0 | 0 | 0 | GS data “11” to RAM data | | | | |

**Initial value for each Palette**

| Gray Scale Data | Initial Gray Scale Level | | |
|---|---|---|---|
| | Red | Green | Blue |
| 000 | 0 | 0 | 0 |
| 001 | 5 | 9 | 10 |
| 010 | 10 | 18 | 20 |
| 011 | 14 | 27 | 31 |
| 100 | 18 | 36 | - |
| 101 | 22 | 45 | - |
| 110 | 26 | 54 | - |
| 111 | 31 | 63 | - |

**The relationship between Gray Scale level and RAM data for Red/Blue**

| RAM Data | | | | | GS Level | RAM Data | | | | | GS Level |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DB4 | DB3 | DB2 | DB1 | DB0 | | DB4 | DB3 | DB2 | DB1 | DB0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 16 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 17 |
| 0 | 0 | 0 | 1 | 0 | 2 | 1 | 0 | 0 | 1 | 0 | 18 |
| 0 | 0 | 0 | 1 | 1 | 3 | 1 | 0 | 0 | 1 | 1 | 19 |
| 0 | 0 | 1 | 0 | 0 | 4 | 1 | 0 | 1 | 0 | 0 | 20 |
| 0 | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 | 1 | 21 |
| 0 | 0 | 1 | 1 | 0 | 6 | 1 | 0 | 1 | 1 | 0 | 22 |
| 0 | 0 | 1 | 1 | 1 | 7 | 1 | 0 | 1 | 1 | 1 | 23 |
| 0 | 1 | 0 | 0 | 0 | 8 | 1 | 1 | 0 | 0 | 0 | 24 |
| 0 | 1 | 0 | 0 | 1 | 9 | 1 | 1 | 0 | 0 | 1 | 25 |
| 0 | 1 | 0 | 1 | 0 | 10 | 1 | 1 | 0 | 1 | 0 | 26 |
| 0 | 1 | 0 | 1 | 1 | 11 | 1 | 1 | 0 | 1 | 1 | 27 |
| 0 | 1 | 1 | 0 | 0 | 12 | 1 | 1 | 1 | 0 | 0 | 28 |
| 0 | 1 | 1 | 0 | 1 | 13 | 1 | 1 | 1 | 0 | 1 | 29 |
| 0 | 1 | 1 | 1 | 0 | 14 | 1 | 1 | 1 | 1 | 0 | 30 |
| 0 | 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 | 1 | 31 |

**The relationship between Gray Scale level and Gray Scale data for Green**

| GS Data | | | | | | GS Level | GS Data | | | | | | GS Level |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 32 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 33 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 | 1 | 0 | 0 | 0 | 1 | 0 | 34 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 | 1 | 0 | 0 | 0 | 1 | 1 | 35 |
| 0 | 0 | 0 | 1 | 0 | 0 | 4 | 1 | 0 | 0 | 1 | 0 | 0 | 36 |
| 0 | 0 | 0 | 1 | 0 | 1 | 5 | 1 | 0 | 0 | 1 | 0 | 1 | 37 |
| 0 | 0 | 0 | 1 | 1 | 0 | 6 | 1 | 0 | 0 | 1 | 1 | 0 | 38 |
| 0 | 0 | 0 | 1 | 1 | 1 | 7 | 1 | 0 | 0 | 1 | 1 | 1 | 39 |
| 0 | 0 | 1 | 0 | 0 | 0 | 8 | 1 | 0 | 1 | 0 | 0 | 0 | 40 |
| 0 | 0 | 1 | 0 | 0 | 1 | 9 | 1 | 0 | 1 | 0 | 0 | 1 | 41 |
| 0 | 0 | 1 | 0 | 1 | 0 | 10 | 1 | 0 | 1 | 0 | 1 | 0 | 42 |
| 0 | 0 | 1 | 0 | 1 | 1 | 11 | 1 | 0 | 1 | 0 | 1 | 1 | 43 |
| 0 | 0 | 1 | 1 | 0 | 0 | 12 | 1 | 0 | 1 | 1 | 0 | 0 | 44 |
| 0 | 0 | 1 | 1 | 0 | 1 | 13 | 1 | 0 | 1 | 1 | 0 | 1 | 45 |
| 0 | 0 | 1 | 1 | 1 | 0 | 14 | 1 | 0 | 1 | 1 | 1 | 0 | 46 |
| 0 | 0 | 1 | 1 | 1 | 1 | 15 | 1 | 0 | 1 | 1 | 1 | 1 | 47 |
| 0 | 1 | 0 | 0 | 0 | 0 | 16 | 1 | 1 | 0 | 0 | 0 | 0 | 48 |
| 0 | 1 | 0 | 0 | 0 | 1 | 17 | 1 | 1 | 0 | 0 | 0 | 1 | 49 |
| 0 | 1 | 0 | 0 | 1 | 0 | 18 | 1 | 1 | 0 | 0 | 1 | 0 | 50 |
| 0 | 1 | 0 | 0 | 1 | 1 | 19 | 1 | 1 | 0 | 0 | 1 | 1 | 51 |
| 0 | 1 | 0 | 1 | 0 | 0 | 20 | 1 | 1 | 0 | 1 | 0 | 0 | 52 |
| 0 | 1 | 0 | 1 | 0 | 1 | 21 | 1 | 1 | 0 | 1 | 0 | 1 | 53 |
| 0 | 1 | 0 | 1 | 1 | 0 | 22 | 1 | 1 | 0 | 1 | 1 | 0 | 54 |
| 0 | 1 | 0 | 1 | 1 | 1 | 23 | 1 | 1 | 0 | 1 | 1 | 1 | 55 |
| 0 | 1 | 1 | 0 | 0 | 0 | 24 | 1 | 1 | 1 | 0 | 0 | 0 | 56 |
| 0 | 1 | 1 | 0 | 0 | 1 | 25 | 1 | 1 | 1 | 0 | 0 | 1 | 57 |
| 0 | 1 | 1 | 0 | 1 | 0 | 26 | 1 | 1 | 1 | 0 | 1 | 0 | 58 |
| 0 | 1 | 1 | 0 | 1 | 1 | 27 | 1 | 1 | 1 | 0 | 1 | 1 | 59 |
| 0 | 1 | 1 | 1 | 0 | 0 | 28 | 1 | 1 | 1 | 1 | 0 | 0 | 60 |
| 0 | 1 | 1 | 1 | 0 | 1 | 29 | 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| 0 | 1 | 1 | 1 | 1 | 0 | 30 | 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 0 | 1 | 1 | 1 | 1 | 1 | 31 | 1 | 1 | 1 | 1 | 1 | 1 | 63 |

### N-block inversion Set (34H)

This instruction set up N block inversion for AC driving.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | | FIM | FIP | 0 | N-block inversion | | | | |

FIM: Forcing Inversion Mode
FIM = 0: Forcing Inversion OFF (Initial status)
FIM = 1: Forcing Inversion ON
FIP: Forcing Inversion Period
FIP = 0: Forcing Inversion Period is one frame
FIP = 1: Forcing Inversion Period is two frames
N-block Inversion : This parameter indicates the basic period of polarity inversion.
The whole period of polarity inversion is decided by FIM, FIP and this parameter.

| DB7 | DB6 | DB5 | DB4 – DB0 | Polarity Inversion Period |
|---|---|---|---|---|
| x | X | x | 0 | every frame |
| 0 | X | x | 1 | every 1 block |
| : | : | : | : | : |
| 0 | X | x | 31 | every 31 blocks |
| 1 | 0 | x | 1 | every 1 block and every frame |
| : | : | : | : | : |
| 1 | 0 | x | 31 | every 31 blocks and every frame |
| 1 | 1 | x | 1 | every 1 block and every 2 frames |
| : | : | : | : | : |
| 1 | 1 | x | 31 | every 31 blocks and every 2 frames |

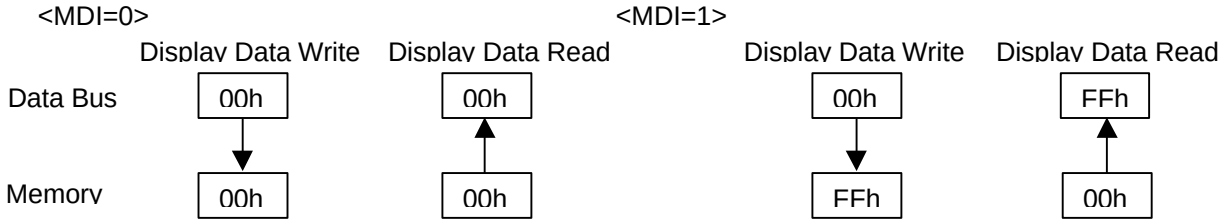
### Entry Mode Set (40H)

Setting internal function mode.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | 0 | 0 | 0 | 0 | HL | MDI | X/Y | RMW |

HL: When GSM is 10 or 11 (256 color mode),
Exchange higher and lower byte in 16-bit data bus mode only for "Display Data Write/Read"
HL = 0: Not exchanged status (Initial status)
HL = 1: Exchanged status

MDI: Memory data inversion setting for low power consumption.
MDI = 0: Memory data inversion OFF (Initial status)
MDI = 1: Memory data inversion ON




X/Y: Memory address counter mode setting
X/Y = 0: Y address counter mode (Initial status)
X/Y = 1: X address counter mode

RMW: Read modify write mode ON/OFF select
RMW = 0: Read modify write OFF (Initial status)
RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not increment in reading display data but in writing display data.

### X Address Area Set (42H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | X start address set (Initial Status = 00H) | | | | | | | |
| | | | X end address set (Initial Status = 83H) | | | | | | | |

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (X/Y = "H"), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end addresses must be set as a pair and X start address must be less than X end address.

### Y Address Area Set (43H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | Y start address set (Initial Status = 00H) | | | | | | | |
| | | | Y end address set (Initial Status = 83H) | | | | | | | |

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (X/Y = "L"), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end address must be set as a pair and Y start address must be less than Y end address.

### RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

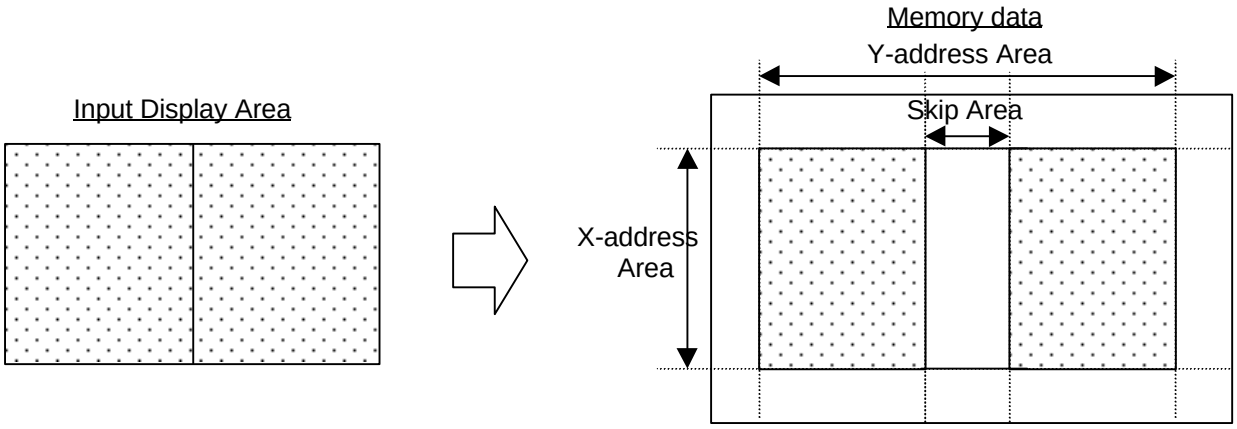
| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | RSK | |

RSK : RAM Skip function ON/OFF set

- RSK = 00 : No Skip
- RSK = 01 : Y address 3Eh-45h skip
- RSK = 10 : Y address 3Ah-49h skip
- RSK = 11 : Y address 36h-4Dh skip

#### RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM Y-address area. After setting RAM skip area, Y-address count skip this area and count. In other words, Y address after skip area is changed into Y address which added a part for skip area.



### Display OFF (50H)

Turn the display OFF(Initial status).
When display is off, all segment and common output are VM level.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

Function and Pin condition at Display OFF

| Function/Pin | Condition |
|---|---|
| DC/DC booster(1' st,2' nd,3' rd) | ON(Operate) |
| SEG and COM outputs | VSS |

### Display ON (51H)

Turns the display ON.
In case of being standby mode, this instruction does not work. This instruction is executed after standby mode off.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |

Function and Pin condition at Display ON

| Function/Pin | Condition |
|---|---|
| DC/DC booster(1' st,2' nd,3' rd) | ON(Operate) |
| COM outputs | +VR or VM or -VR |
| SEG outputs | V1 or VSS |

### Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

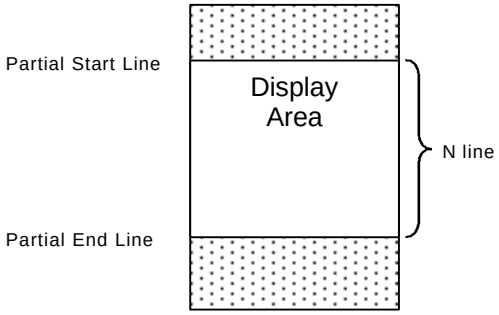
| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | SDP | |

SDP : Specified Display Pattern set
- SDP = 00 : Normal display
- SDP = 01 : Reverse display : Display data reversing mode setting without the contents of the display RAM
- SDP = 10 : Whole display pattern becomes OFF regardless of the RAM data.
- SDP = 11 : Whole display pattern becomes ON regardless of the RAM data.

**Partial Display Mode Set (55H)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PT |

PT: Partial Display ON/OFF
- PT = 0: Partial display OFF = Normal mode (Initial status)
- PT = 1: Partial display ON




No display Area : No COM Scanning field (COM = Vm fixed)

Except Partial Display Area : COM Timing is existing, but COM = Vm fixed

Partial Display Area : Real display field

**Operation in Partial Display Mode**

On scanning except partial display area
- SEG output select V0 or V1 level depend on “FR” value.
- All of COM output is fixed VM level.

On scanning partial display area
- It is equal to be in normal mode

### Partial Display Start Line Set (56H), Partial Display End Line Set(57H)

These 2 instructions set the partial display area and it is possible to display a part.

Partial Display Start Line Set (56H)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| | | | Partial start line | | | | | | | |

Partial Display End Line Set (57H)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| | | | Partial end line | | | | | | | |

| | |
|---|---|
| COM 0 | line 0 |
| COM 1 | line 1 |
| COM 2 | line 2 |
| COM 3 | line 3 |
| | : |
| | : |
| | : |
| COM 128 | line 128 |
| COM 129 | line 129 |
| COM 130 | line 130 |
| COM 131 | line 131 |

Parameter set appoints display line number. Parameter Size is able to be in a number of Display lines. Partial end line must set bigger number than Partial start line.

### Area scroll Set (59H)

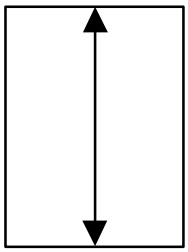
This instruction sets up area scroll field (start line, end line, Lower fixed line number), and it is possible to make screen to display as partial scroll field.

| D/I | /WR | /RD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | SCM | |
| | | | 0 | Scroll area start line | | | | | | |
| | | | 0 | Scroll area end line | | | | | | |
| | | | 0 | Lower fixed number | | | | | | |

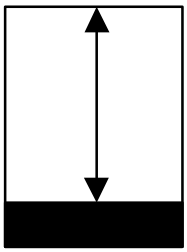
Note: In lower and center scroll mode, scroll area end line must be smaller than duty - lower fixed number.

**SCM: Scroll mode setting**

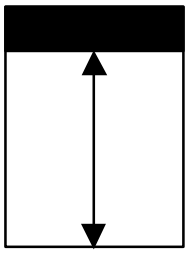
| DB1 | DB0 | Mode |
|---|---|---|
| 0 | 0 | Entire display(Initial status) |
| 0 | 1 | Upper scroll display |
| 1 | 0 | Lower scroll display |
| 1 | 1 | Center scroll display |



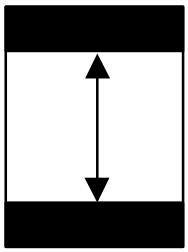
Entire Display



Upper Display



Lower Display



Center Display

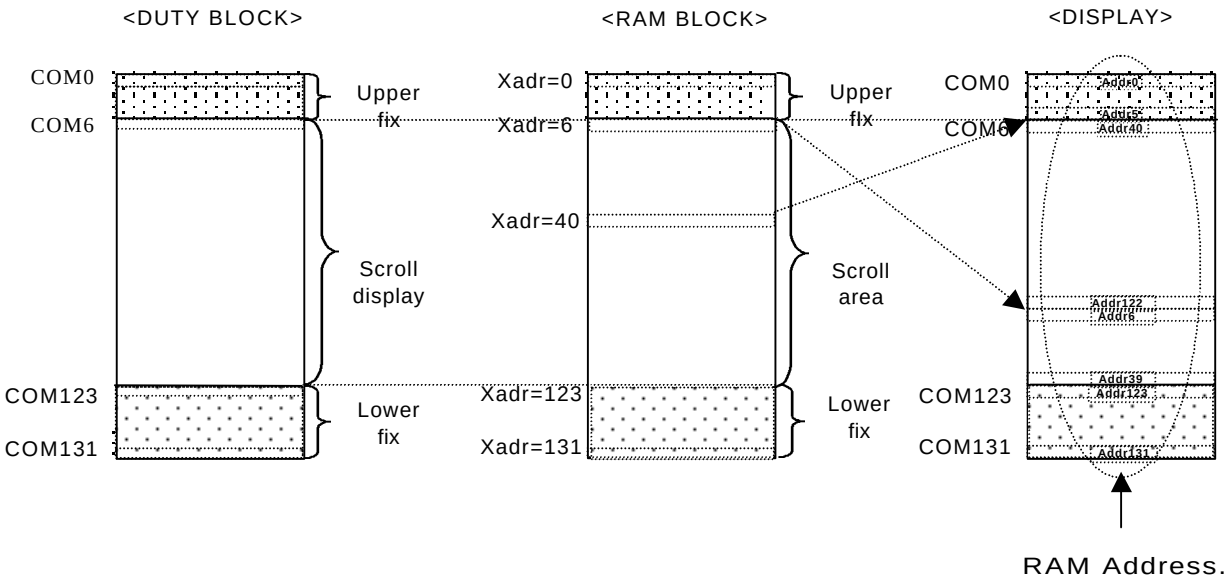
## Scroll Start Line Set (5AH)

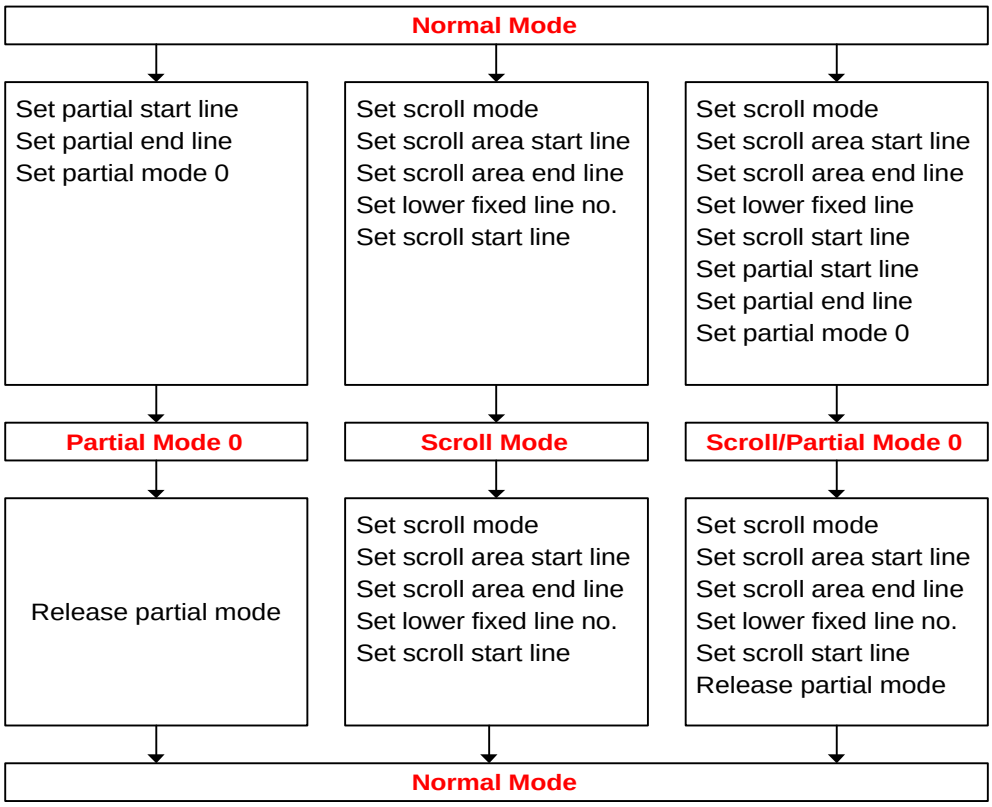
This instruction and parameter set up scroll start line. On this instruction, scroll start line becomes the first of area scroll field. Scroll operation is occurred every issue of this instruction.

| D/I | /WR | /RD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| | | | 0 | Scroll start line | | | | | | |

**<Example>**

-DLN : 2'b11 (1/132 Duty)
-SCM : 2'b11 (Center display mode)
-Scroll area start line : 6
-Scroll area end line : 122
-Lower fixed number : 9
-Scroll start line : 40






**Data Format Select (60H/61H)**

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | DFS |

DFS: 4,096 Color Mode Data Format Select
- 0 : 4,096 Color Data Format A (Initial Status)
  - 8 bit mode :
    - DB[7:0] : XXXXRRRR (1'st write)
    - DB[7:0] : GGGGBBBB(2'nd write)
  - 16 bit mode :
    - DB[15:0] :XXXXRRRRGGGGBBBB (12 bit)
- 1 : 4,096 Color Data Format B
  - 8 bit mode :
    - DB[7:0] : RRRRGGGG(1'st write)
    - DB[7:0] : BBBBRRRR (2'nd write)
    - DB[7:0] : GGGGBBBB(3'rd write)
  - 16 bit mode :
    - DB[15:0] :RRRRGGGGBBBBXXXX (12 bit)

## RAM Access

1) Case of Burst Mode Off

| Color | Data Bus | Y-address Count Mode | X-address Count Mode |
|---|---|---|---|
| 65K | 16 bit | Supported | Supported |
| | 8bit | Supported | Supported |
| 4K DFS=0 | 16 bit | Supported | Supported |
| | 8bit | Supported | Not Supported |
| 4K DFS=1 | 16 bit | Supported | Supported |
| | 8bit | Supported | Not Supported |
| 256 | 16 bit | Supported | Not Supported |
| | 8bit | Supported | Not Supported |

2) Case of Burst Mode ON

| Color | Data Bus | Y-address Count Mode | X-address Count Mode |
|---|---|---|---|
| 65K | 16 bit | Supported | Not Supported |
| | 8bit | Supported | Not Supported |
| 4K DFS=0 | 16 bit | Supported | Not Supported |
| | 8bit | Supported | Not Supported |
| 4K DFS=1 | 16 bit | Supported | Not Supported |
| | 8bit | Supported | Not Supported |
| 256 | 16 bit | Supported | Not Supported |
| | 8bit | Not Supported | Not Supported |

I

## Display Data Write/Read

| D/I | WRB | RDB | DB15 ~ DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | Display RAM write in data | | | | | | | | |
| 1 | 1 | 0 | Display RAM read out data | | | | | | | | |

**GSM = 00(65,536 Color Mode)**

(1) 16bit access mode

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1' st cycle | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 |
| 2' nd cycle | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 |

(2) 8bit access mode

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1' st cycle | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 |
| 2' nd cycle | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 |
| 3' rd cycle | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 |
| 4' th cycle | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 |

**GSM = 01(4,096 Color Mode)**

(1) 16bit access mode

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1' st cycle | X | X | X | X | R3 | R2 | R1 | R0 | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 |
| 2' nd cycle | X | X | X | X | R3 | R2 | R1 | R0 | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 |

(2) 8bit access mode

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1' st cycle | X | X | X | X | R3 | R2 | R1 | R0 |
| 2' nd cycle | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 |
| 3' rd cycle | X | X | X | X | R3 | R2 | R1 | R0 |
| 4' th cycle | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 |

**GSM = 10 or 11 (256 Color Mode)**

(1) 16bit access mode

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1' st cycle | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 |
| 2' nd cycle | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 |

(2) 8bit access mode

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1' st cycle | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 |
| 2' nd cycle | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 |
| 3' rd cycle | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 |
| 4' th cycle | R2 | R1 | R0 | G2 | G1 | G0 | B1 | B0 |

### CR Volume Up (70H)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Count up value of contrast control(1) or (2) depending on display mode at present.
If this command is issued at counter value = “FFh”, then counter value become “00”h.

### CR Volume Down (71H)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

Count down value of contrast control(1) or (2) depending on display mode at present.
If this command is issued at counter value = “00h”, then counter value become “FF”h.

### Status Read Mode (7FH)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | SRMD | |

The contents read by “Status Read” can be selected.

| SRMD | | Status Read |
|---|---|---|
| 0 | 0 | status |
| 0 | 1 | CR1 |
| 1 | 0 | CR2 |
| 1 | 1 | reserved |

### Status Read

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | BSY | DBSY | X/Y | PDM | PT | STB | REV | DP |
| | | | CR1 | | | | | | | |
| | | | CR2 | | | | | | | |

This instruction indicates the internal status of the S6B33B1X.

DP: ( 0 : Display OFF Status, 1 : Display ON Status )
REV: ( 0 : Display Image Non-Reversing, 1 : Display Image Reversing )
STB: ( 0 : Standby Mode OFF Status, 1 : Standby Mode ON Status )
PT: ( 0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status )
X/Y: ( 0 : Y-address Count Mode, 1 : X-address Count Mode )
BSY: Busy due to EEPROM access ( 0 : No Busy, 1 : Busy )
DBSY: EEPROM device busy for write access ( 0 : No Busy, 1 : Busy )

### EEPROM Mode Out (80H)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Release EEPROM control mode.

1) If this command is issued, then “write disable” should be executed on serial EEPROM interface.
2) If this command is issued during EEPROM read mode, then value in internal temporary register should be set into contrast control(1) and contrast control(2).

### EEPROM Mode In (81H)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | W/R |

W/R = ‘0’ : Read mode
W/R = ‘1’ : Write mode

1) If write mode command is issued, then “write enable” should be executed on serial EEPROM interface.

### EEPROM Read (8CH)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

16-bit data is read from EEPROM, and then it is stored into internal temporary register.

### EEPROM Write (8DH)

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

The value of contrast control(1)&(2) are stored into EEPROM.
If contrast control(2) does not exist like S6B33B1X, then contrast control(1) is stored as contrast control(2).

| | EEPROM data | |
|---|---|---|
| Contrast Control(2) | 15 ... 08 | 07 ... 00 |
| Exit | CR1 | CR2 |
| Not exit | CR1 | CR1 |

### Set Display Data Length (FCH)

This Instruction is only used in 3-pin SPI MPU interface mode(PS=”L”, MPU[1]=”L”). It consists of two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second and third bytes will be number of data bytes will be write. When DI is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted.
The next byte after the display data string is handled as command data.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | | | Number of display data upper 8bits (DDL_H) | | | | | | | |
| | | | Number of display data lower 8bits (DDL_L) | | | | | | | |

### Test Mode1 (FFH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### Test Mode2 (FEH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

### Test Mode3 (FDH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

### Test Mode4 (FBH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

### Test Mode5 (FAH)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

### Test Mode6 (F9H)

This Instruction is for testing IC. User is not permitted to access. if access, have to reset.

| D/I | WRB | RDB | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

# INSTRUCTION PARAMETER

**Table 16. Instruction Parameter**

| Instruction | Hex | Para. | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Oscillation Mode Set | 02H | 1 | 0 | 0 | 0 | 0 | 0 | DIV2 | EXT | OSC |
| | | | * | * | * | * | * | 0 | 0 | 0 |
| Driver Output Mode Set | 10H | 1 | 0 | 0 | DLN | | 0 | SDIR | SWP | 0 |
| | | | * | * | 0 | 0 | * | 0 | 0 | 0 |
| DC-DC Set | 20H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DC |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bias Set | 22H | 1 | 0 | 0 | | | 0 | 0 | 0 | Bias |
| | | | 0 | * | 0 | 0 | * | * | 0 | 0 |
| DCDC Clock Division Set | 24H | 1 | 0 | 0 | | | 0 | 0 | 0 | DIV |
| | | | * | * | 1 | 0 | * | * | 1 | 0 |
| DCDC and AMP ON/OFF Set | 26H | 1 | 0 | 0 | 0 | 0 | AMP | DCDC3 | DCDC2 | DCDC1 |
| | | | * | * | * | * | 0 | 0 | 0 | 0 |
| Temperature Compensation Set | 28H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | TCS | |
| | | | * | * | * | * | * | * | 0 | 0 |
| Contrast Control | 2AH | 1 | Contrast control value in normal and partial display mode0(0 to 255) | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Addressing Mode Set | 30H | 1 | 0 | GSM | | DSG | SGF | SGP | | SGM |
| | | | * | * | 0 | 0 | 0 | 0 | 0 | 0 |
| ROW Vector Mode Set | 32H | 1 | 0 | 0 | 0 | 0 | INC | | | VEC |
| | | | * | * | * | * | 0 | 0 | 0 | 0 |
| N-line Inversion Set | 34H | 1 | FIM | FIP | 0 | N-block Inversion | | | | |
| | | | 0 | 0 | * | 0 | 0 | 0 | 0 | 0 |
| Entry Mode Set | 40H | 1 | 0 | 0 | 0 | 0 | HL | MDI | X/Y | RMW |
| | | | * | * | * | * | * | 0 | 0 | 0 |
| X-address Area Set | 42H | 2 | X Start address set | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | X end address set | | | | | | | |
| | | | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| Y-address Area Set | 43H | 2 | Y start address set | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Y end address set | | | | | | | |
| | | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| RAM Skip Area Set | 42H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | RSK | |
| | | | * | * | * | * | * | * | 0 | 0 |
| Set Display Data Length | FCH | 2 | Number of display data DDL_H | | | | | | | |
| | | | Number of display data DDL_L | | | | | | | |
| Specified Display Pattern Set | 53H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | SDP | |
| | | | * | * | * | * | * | * | 0 | 0 |
| Partial Display Mode Set | 55H | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PT |
| | | | * | * | * | * | * | * | 0 | 0 |
| Partial Display Start Line Set | 56H | 1 | Partial start line | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Partial Display End Line Set | 57H | 1 | Partial end line | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 16. Instruction Parameter (Continued)**

| Instruction | Hex | Para. | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Area Scroll Mode Set | 59H | 4 | 0 | 0 | 0 | 0 | 0 | 0 | SCM | |
| | | | * | * | * | * | * | * | 0 | 0 |
| | | | Scroll area start line | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | Scroll area end line | | | | | | | |
| | | | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| | | | Lower Fixed number | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Scroll Start Line Set | 5AH | 1 | Scroll start line | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EEPROM Mode In | 81H | 1 | EEPROM Mode In | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Status Read Mode | 7F | 1 | Status Read Mode | | | | | | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Reset Operation

When RSTB becomes “L”, following procedure is occurred.

- X start address: 0, X end address: 131
- Y start address: 0, Y end address: 131
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set
  MDI = 0: Memory Data Inversion OFF
  OSC = 0: Oscillator OFF
  EXT = 0: Internal Oscillator Mode
  REV = 0: Reversing mode OFF
  X/Y = 0: Y-address Count Mode
  Standby Mode ON
- DCDC Clock Division Set
  DIV = 101: fPCK = fOSC/12x
- Duty Set
  Display Duty = 00H: 1/66 duty
- DC-DC Select
  DC = 0: X1 step-up
- Bias Set
  Bias = 0H: 1/5 bias
- DC/DC and AMP ON/OFF Set
  AMP =0: Built-in OP-AMP OFF
  DCDC1 =0: Built-in 1’st booster OFF
  DCDC2 =0: Built-in 2’nd booster OFF
  DCDC3 =0: Built-in 3’rd booster OFF
- N-block inversion
  FIM =0: Forcing Inversion OFF
  FIP =0: Forcing Inversion Period in one frame
  N-block inversion = 00H: frame inversion
- Partial Display Mode
  PT = 0: Partial Display Mode OFF
- Partial Display Area Set
  Partial start line = 00H
  Partial end line = 00H
-Area Scroll Set
  Mode = 00H : Entire Display Scroll Mode
  Area Start Line: 00H
  Area End Line: 83H
  Lower Fixed Line Number: 00H
- Scroll Start Line Set
  Scroll Start Line: 00H
- Addressing Mode Set
  GSM=00: 65,536 Color Mode
  DSG = 0: Mode 0
  SGF = 0: SG Frame Inversion OFF
  SGM = 0: SG Reverse Mode OFF
  SGP=00:Same phase in all pixel
- Row Vector Mode Set
  INC =000: Increment every subgroup
  VEC=0: R1->R2->R3->R4->R1-> ...

# SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage range | VDD | -0.3 to +4.0 | V |
| LCD Supply Voltage range | \|VCC – VEE\| | 24 | V |
| Input Voltage range | Vin | - 0.3 to VDD +0.3 | V |
| Operating Temperature range | TOPR | -30 to +70 | °C |
| Storage Temperature range | TSTR | -55 to +150 | °C |

## OPERATING VOLTAGE

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage (1) | VDD | 1.8 | - | 3.3 | V |
| Supply Voltage (2) | 2Vr | - | - | 20 | V |
| Supply Voltage (3) | VIN | 2.4 | 3.0 | 3.6 | V |

## DC CHARACTERISTICS (1)

(Vss = 0V, $V_{DD}$ = 1.8 to 3.3V, Ta = -30 to 70 °C)

| Item | | Symbol | Condition | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Operating voltage | | VDD | | 1.8 | | 3.3 | V | VDD |
| Operating voltage | | VIN1 | | 2.4 | - | 3.6 | V | VCI |
| Operating voltage | | DC2IN | 1/6 bias | 1.66 | - | 2.75 | V | DC2IN |
| | | | 1/5 bias | 1.33 | - | 2.2 | V | |
| Operating voltage | | VIN2 | | 2.4 | - | 5.4 | V | VIN2 |
| Operating voltage | | VIN45 | | 2.4 | - | 5.4 | V | VIN45 |
| Operating voltage | | 2Vr | 2Vr = \|(+VR)- (-VR)\| | 4.0 | - | 20 | V | +VR, -VR |
| Output voltage | | VREG | REG OUT voltage | 1.8 | 1.9 | 2.0 | V | VREG |
| Driving voltage input range | | VM | External power supply mode | 1.0 | | 1.65 | V | VM |
| | | VCC | | 5.99 | | 11.25 | V | VCC |
| | | VEE | | -8.25 | | -3.99 | V | VEE |
| Input voltage | High | $V_{IH}$ | | 0.8VDD | - | VDD | V | |
| | Low | $V_{IL}$ | | VSS | - | 0.2VDD | | |
| Output voltage | High | $V_{OH}$ | $I_{OH}$ = 0.5mA | 0.8VDD | - | VDD | V | |
| | Low | $V_{OL}$ | $I_{OL}$ = 0.5mA | VSS | - | 0.2VDD | | |
| Input leakage current | | $I_{IL}$ | VIN = VDD or VSS | -1.0 | - | +1.0 | µA | |
| Output leakage current | | $I_{OZ}$ | VIN = VDD or VSS | -3.0 | - | +3.0 | µA | |
| Oscillator Frequency Tolerance | Normal or Partial | $F_{OSC}$ | R1=? (fFR=80Hz target), DSG=0, 132 display lines | 50.688 | 56.32 | 61.952 | kHz | OSC1 - OSC2 |
| Oscillator Frequency Range | Normal or Partial | $F_{OSC}$ | (*1) | 35.200 | | 70.400 | kHz | OSC1 - OSC2 |
| Driving voltage input range | | V1<br>VM | | 2.0<br>1.0 | - | 3.3<br>1.65 | V | |

(*1) Minimum oscillator frequency range is defined at fFR=50Hz and display line number=132
Maximum oscillator frequency range is defined at fFR=100Hz and display line number=132

## DC CHARACTERISTICS (2)

(Vss = 0V, $V_{DD}$ = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

| Item | | Symbol | Condition | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Driver output resistance | SEG | $R_{ON-Seg}$ | V1=3.3 V, VM=1.65V, V0=0V, Ta = 25°C, Iload=100uA | - | 1.5 | 3.0 | kΩ | SEGn |
| | COM | $R_{ON-Com}$ | VCC=12 V, VM=1.5V, VEE=-9.0V, Ta = 25°C, Iload=100uA | - | 1.0 | 1.5 | kΩ | COMn |
| Current consumption | Normal Mode | IDD | VDD=VIN1=3.0V, V1=3.0V, Bias(1)=1/6, DC(1)=x1.5, Ta=25°C, Display line=132 DSG=0 (1dummy) $f_{OSC}$=140.8kHz (fFR=100Hz) Low current mode, No load, No access, All white pattern | - | TBD | TBD | μA | VDD |

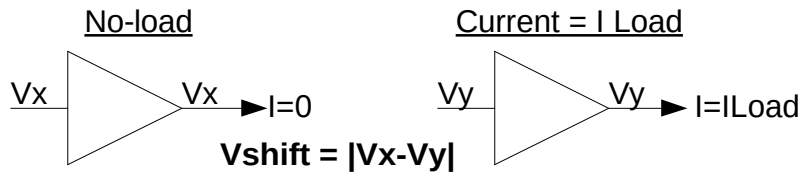
* : “TBD” is determined from lowest power consumption for dc-dc converter.

## DC CHARACTERISTICS (3)

(Vss = 0V, $V_{DD}$ = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

| Item | Symbol | Condition | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Voltage shift range(*1) | Δ (+VR) | Low current mode Isource = 80uA<br>High current mode Isource = 150 or 250uA | - | - | 100 | mV | +VR |
| | Δ (V1) | Low current mode Isource = 250uA<br>High current mode Isource = 500 or 1000uA | - | - | 20 | mV | V1 |
| | Δ (VM) | Low current mode Isource,sink = 250uA<br>High current mode Isource,sink = 500 or 1000uA | - | - | 20 | mV | VM |
| | Δ (-VR) | Low current mode Isink = 80uA<br>High current mode Isink = 150 or 250uA | - | - | 100 | mV | -VR |

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (in case of source current mode)




| Item | Symbol | Condition | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Tolerance of Bias ratio | Δ (+VR)_0<br>Δ (-VR)_0(*1) | No load | -100 | - | +100 | mV | +VR<br>-VR |

(*1) Tolerance of bias ratio definition
Δ (+VR)_0 = ((+VR) - VM ) – VM *Bias
Δ (-VR)_0 = ( VM - (-VR)) – VM *Bias

## DC CHARACTERISTICS (4)

(Vss = 0V, VDD = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

| Item | Symbol | Condition | | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Temperature compensation | ΔVt | VDD=VIN1=V1=3.0V, -20 to 70 °C | | -0.02 | - | +0.02 | %/°C | V1 |
| Tolerance of Contrast step of V1 | ΔVstep | | | 2.539 | 5.078 | 7.617 | mV | V1 |
| Voltage range | ΔV1 ΔVM | Contrast set = FFh | V1 | 3.25 | 3.3 | 3.35 | V | V1 |
| | | | VM | 1.60 | 1.65 | 1.70 | V | VM |
| | | Contrast set = 00h | V1 | 1.95 | 2.00 | 2.05 | V | V1 |
| | | | VM | 0.95 | 1.00 | 1.05 | V | VM |

| Item | | | Condition | | Max | Unit | Ref |
|---|---|---|---|---|---|---|---|
| | | | Load current | Voltage range | | | |
| Offset Voltage | ||+VR-VM| -|VM -(-VR)|| | | I Load = +100uA (+VR)<br>I Load = -100uA (-VR) | +VR=5.0~TBD V<br>V1=2.0~3.3V<br>VM=1.0~1.65V<br>-VR=-3.0~-TBD V | 100 | mV | Fig.1 |
| | ||V1-VM| -|VM-V0|| | A | I Load = +100uA ( V1, VM ) | | 50 | mV | Fig.2 |
| | | B | I Load = +100uA (+VR)<br>I Load = -100uA (-VR) | | | | |

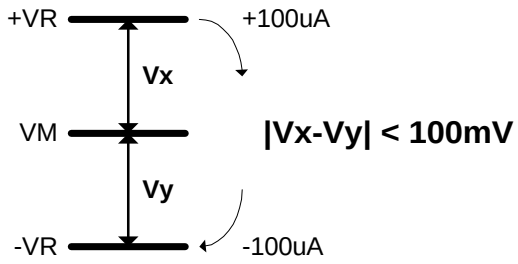



Fig. 1: Offset voltage definition (+VR,VM,-VR)

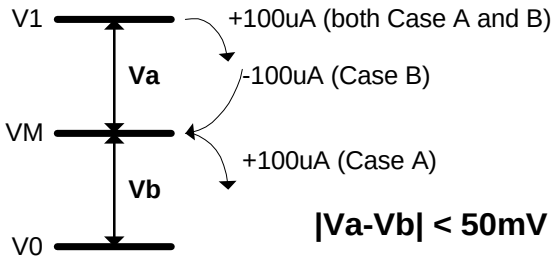


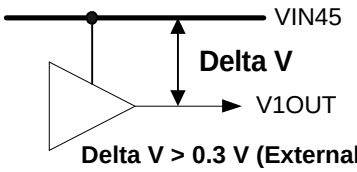

Fig. 2: Offset voltage definition (V1,VM,V0)

## DC CHARACTERISTICS (5)

(Vss = 0V, $V_{DD}$ = 1.8 to 3.3V, VIN1=2.4 to 3.6V, Ta = -30 to 70 °C)

| Item | | Range | |
|---|---|---|---|
| | | Min | Max (DC(1) and DC(2) = X1.5) |
| Voltage Level | V1OUT | 2.0 V | 3.3 V(*1) |
| | VMOUT | 1.0 V | 1.65 V(*2) |
| | DC2OUT | 1.67 V | 2.75 V(*3) |

(*1) This definition is shown as below




**Delta V > 0.3 V (External VIN45)**

**Delta V > 0.5 V (VIN45 = VOUT45)**

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

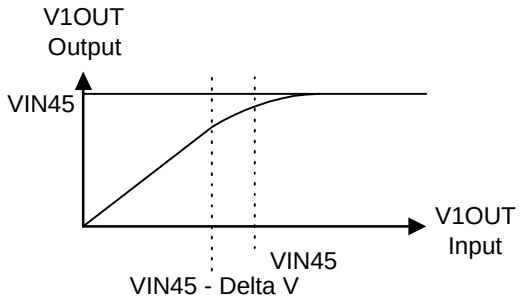
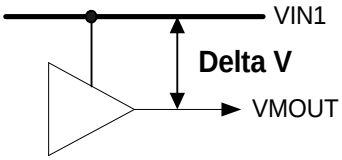



**Fig. 1**

(*2) This definition is shown as below




**Delta V > 0.3 V**

If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1. In this case, VMOUT output level must not be unstable. Refer to Fig.2

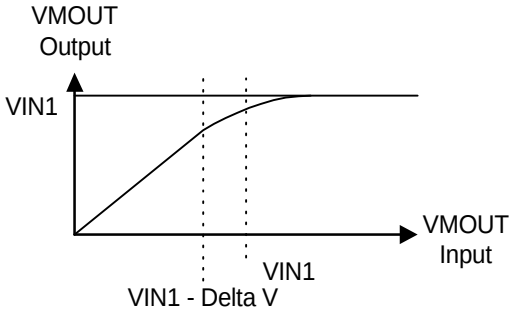
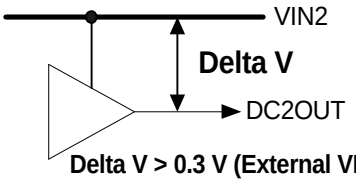



**Fig. 2**

(*3) This definition is shown as below




**Delta V > 0.3 V (External VIN2)**

**Delta V > 0.5 V (VIN2 = VOUT45)**

If DC2OUT input voltage is set over VIN2, DC2OUT output voltage must be clipped near VIN2. In this case, VMOUT output level must not be unstable. Refer to Fig.3

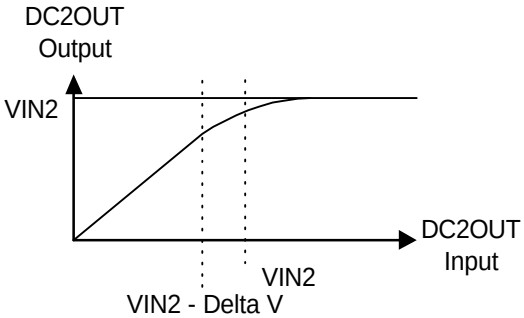
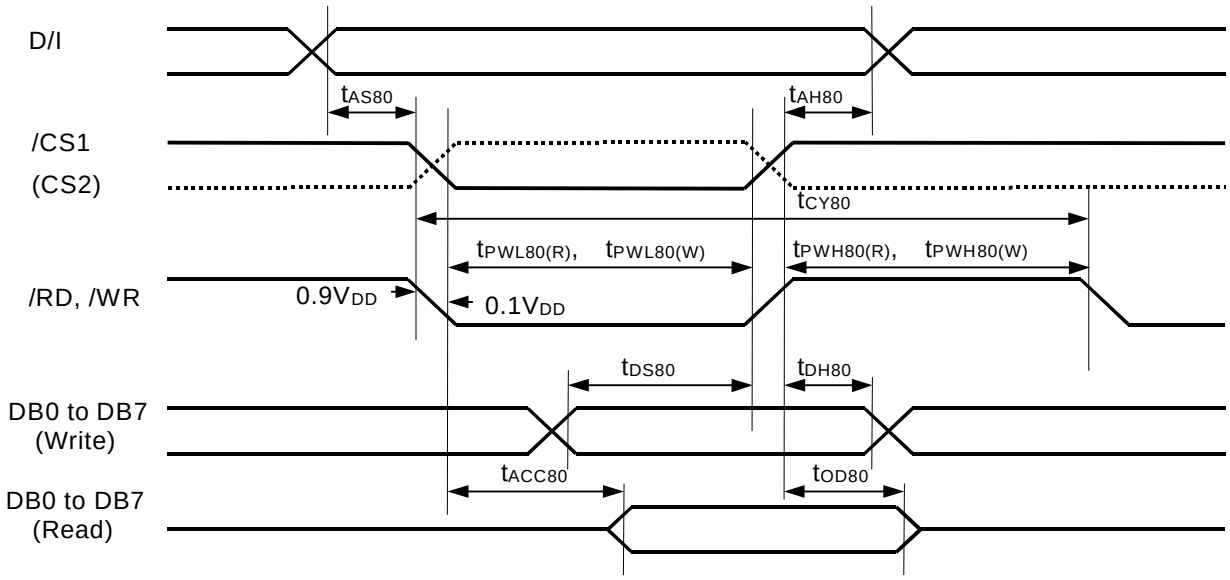



**Fig.3**

## AC CHARACTERISTICS

### Read / Write Characteristics (8080-series MPU)




** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

**Figure 29. Parallel Interface (8080-series MPU) Timing Diagram**

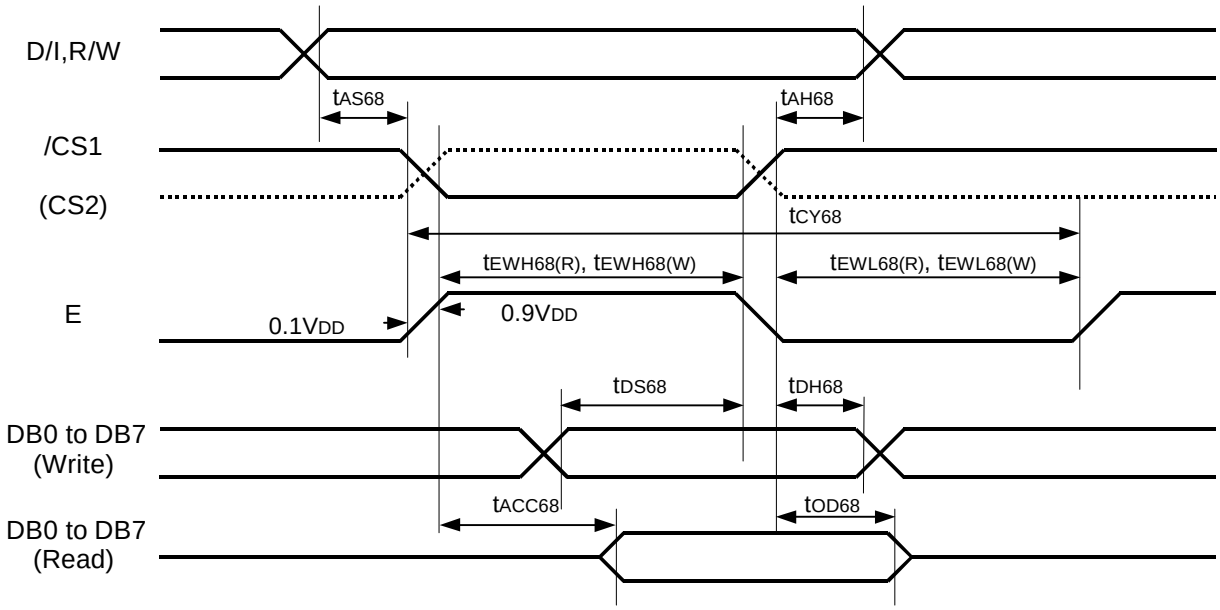
**Table 17. AC Characteristics (8080-series Parallel Mode)**

(VDD3 = 1.8 to 3.3V, Ta = -30 to +70°C)

| Item | Signal | Symbol | Condition | Min. | | Max. (3.3V/1.8V) | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 3.3V | 1.8V | | |
| Address setup time<br>Address hold time | D/I | $t_{AS80}$<br>$t_{AH80}$ | | 0<br>0 | 0<br>0 | -<br>- | ns |
| System cycle time | | $t_{CY80}$ | | 150 | 360 | - | ns |
| Pulse width low for write<br>Pulse width High for write | WRB<br>(WRB) | $t_{PWLW}$<br>$t_{PWHW}$ | | 50<br>30 | 100<br>75 | -<br>- | ns |
| Pulse width low for read<br>Pulse width high for read | RDB<br>(RDB) | $t_{PWLR}$<br>$t_{PWHR}$ | | 50<br>30 | 100<br>75 | -<br>- | ns |
| Data setup time<br>Data hold time | DB0<br>to<br>DB15 | $t_{DS80}$<br>$t_{DH80}$ | | 5<br>8 | 10<br>14 | -<br>- | ns |
| Read access time<br>Output disable time | | $t_{ACC80}$<br>$t_{OD80}$ | CL = 100 pF | - | | 60 / 120<br>tEWHR | ns |

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < ($t_{CY80}$ - $t_{PWLW}$ - $t_{PWHW}$ ) for write, (tr + tf) < ($t_{CY80}$ - $t_{PWLR}$ - $t_{PWHR}$ ) for read

### Read / Write Characteristics (6800-series Microprocessor)




** $t_{EWH68(W)}$ and $t_{EWH68(R)}$ is specified in the overlapped period when /CS1 is low (CS2 is high) and E is high.

**Figure 30. Parallel Interface (6800-series MPU) Timing Diagram**

**Table 18. AC Characteristics (6800-series Parallel Mode)**

($V_{DD3}$ = 1.8 to 3.3V, Ta = -30 to +70°C)

| Item | Signal | Symbol | Condition | Min. | | Max. (3.3V/1.8V) | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 3.3V | 1.8V | | |
| Address setup time<br>Address hold time | D/I<br>R/W | $t_{AS68}$<br>$t_{AH68}$ | | 0<br>0 | 0<br>0 | -<br>- | ns |
| System cycle time | | $t_{CY68}$ | | 150 | 360 | - | ns |
| Enable width high for write<br>Enable width low for write | RDB<br>(E) | $t_{EWHW}$<br>$t_{EWLW}$ | | 50<br>30 | 100<br>75 | -<br>- | ns |
| Enable width high for read<br>Enable width low for read | RDB<br>(E) | $t_{EWHR}$<br>$t_{EWLR}$ | | 50<br>30 | 100<br>75 | -<br>- | ns |
| Data setup time<br>Data hold time | DB0<br>to<br>DB15 | $t_{DS68}$<br>$t_{DH68}$ | | 5<br>8 | 10<br>14 | -<br>- | ns |
| Read access time<br>Output disable time | | $T_{ACC68}$<br>$t_{OD68}$ | $C_L$ = 100 pF | - | | 60 / 120 | ns |
| | | | | tEWLR | | | |

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 10 ns or less.
(tr + tf) < ($t_{CY68}$ - $t_{EWHW}$ - $t_{EWLW}$ ) for write, (tr + tf) < ($t_{CY68}$ - $t_{EWHR}$ - $t_{EWLR}$ ) for read

## Serial Data Interface Timing

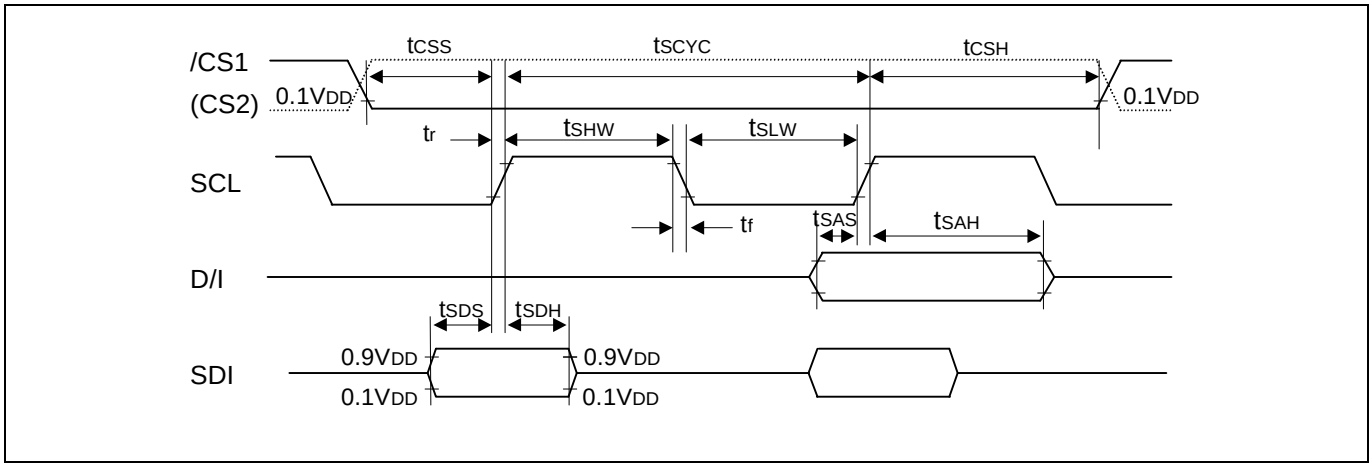



**Table 31. Serial Data Interface Timing**

($V_{DD3}$ = 1.8 to 3.3V, Ta = -30 to +70°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCL Cycle Time | SCL | $t_{CSC}$ | | 50 | - | ns |
| SCL High Pulse Width | SCL | $t_{SHW}$ | | 20 | - | ns |
| SCL Low Pulse Width | SCL | $t_{SLW}$ | | 20 | - | ns |
| SDI Setup time | SDI | $t_{SDS}$ | | 20 | - | ns |
| SDI Hold time | SDI | $t_{SDH}$ | | 20 | - | ns |
| D/I Setup time | D/I | $t_{SAS}$ | | 20 | - | ns |
| D/I Hold time | D/I | $t_{SAH}$ | | 20 | - | ns |
| Chip Select Setup time | CS1B (CS2) | $t_{CSS}$ | | 20 | - | ns |
| Chip Select Hold time | CS1B (CS2) | $t_{CHS}$ | | 20 | - | ns |

## EEPROM Interface Timing

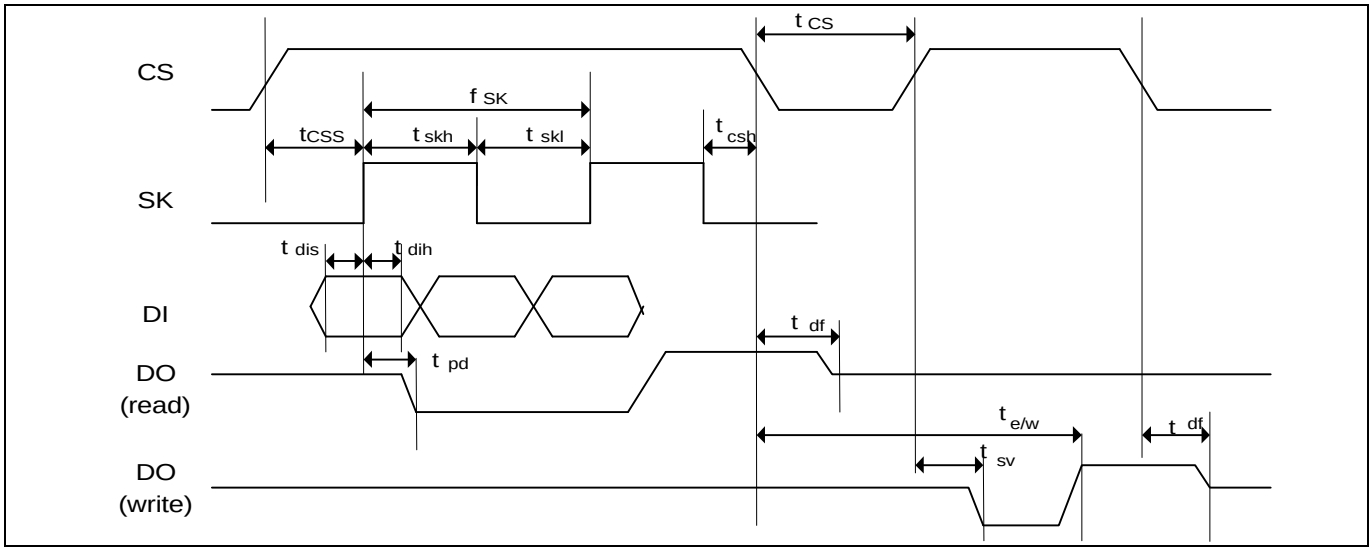



**Table 32. Serial Data Interface Timing**

($V_{DD3}$ = 1.8 to 3.3V, Ta = -30 to +70°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| SK Cycle Time | SK | $f_{SK}$ | | | 50 | kHz |
| SK High Pulse Width | SK | $t_{SKH}$ | | 10 | | us |
| SK Low Pulse Width | SK | $t_{SKL}$ | | 10 | | us |
| E_DI Setup time | E_DI | $t_{dis}$ | | 4 | | us |
| E_DI Hold time | E_DI | $t_{dih}$ | | 4 | | us |
| Chip Select Setup time | CS | $t_{CSS}$ | | 10 | | us |
| Chip Select Hold time | CS | $t_{CSh}$ | | 10 | | us |
| Chip Select Low Pulse Width | CS | $t_{CS}$ | | 10 | | us |
| Delay time | - | $t_{pd}$ | | | 20 | us |
| Settling time | - | $t_{sv}$ | | | 20 | us |
| Disable time | - | $t_{df}$ | | | 10 | us |
| Write Cycle time | - | $T_{e/w}$ | | | 250 | ms |

NOTE: *1. The EEPROM Interface timing is specified when OSC frequency is 200 kHz .

### Reset Input Timing

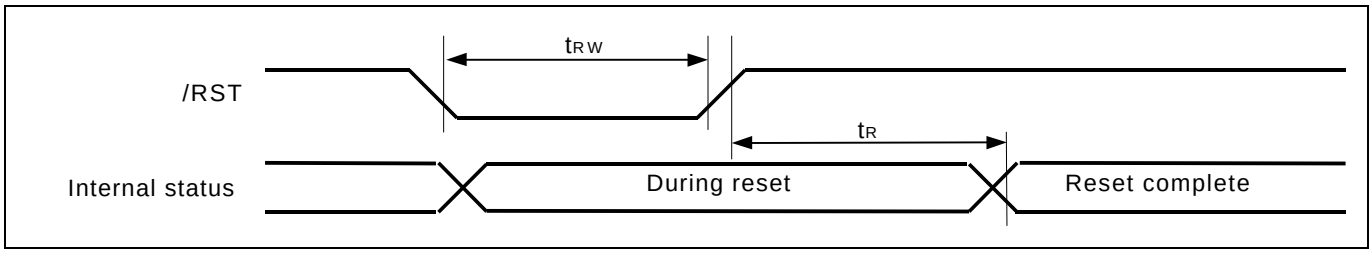



**Figure 33. Reset Input Timing Diagram**

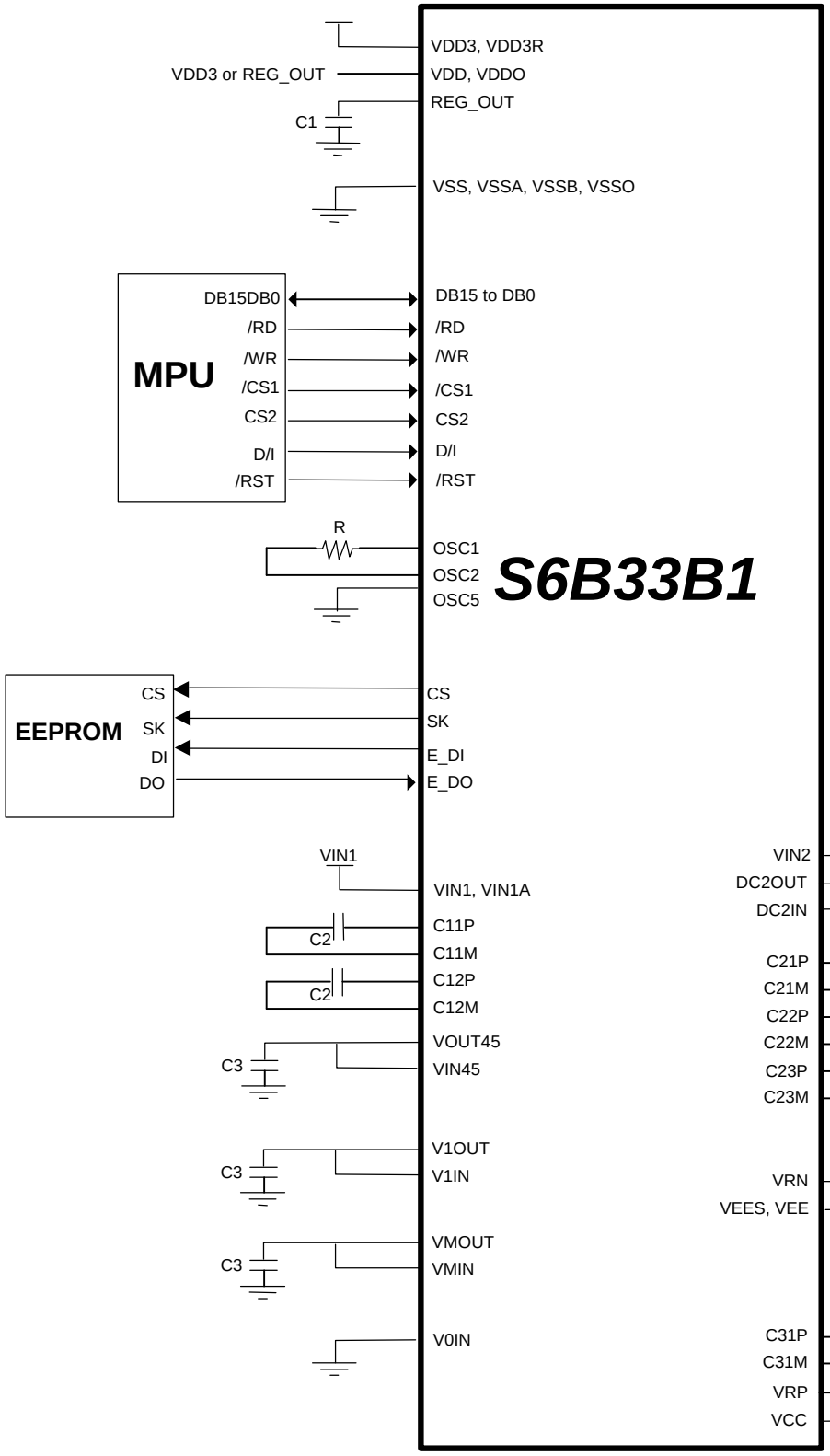
**Table 20. AC Characteristics (Reset mode)**

($V_{DD3}$ = 1.8 to 3.3V, Ta = -30 to +70°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Reset low pulse width | RSTB | $T_{RW}$ | | 1000 | - | ns |
| Reset time | - | $t_R$ | | - | 1000 | ns |

# SYSTEM APPLICATION DIAGRAM

## Internal Power Mode




External Components

| Name | Device |
|---|---|
| R | Resistors |
| C1,C2,C3 | Capacitors |
| D1 | Schottky barrier diode |

Value of external Capacitors

| Item | Capacitance |
|---|---|
| C1 | 1.0 to 4.7µF |
| C2 | 1.0 to 2.2µF |
| C3 | 1.0 to 2.2µF |
| D1 | Vforward = Max. 0.3V at 1mA<br>Vreverse = Min. 15V |

Maximum rating voltage of capacitors

| Item | Maximum rating voltage |
|---|---|
| REG_OUT to VSS | 3V |
| VOUT45 to VSS | 11V |
| C11P to C11M | 6V |
| C12P to C12M | 6V |
| VMOUT to VSS | 3V |
| DC2OUT to VSS | 5V |
| V1OUT to VSS | 6V |
| C21P to C21M | 5V |
| C22P to C22M | 10V |
| C23P to C23M | 13V |
| VSS to VRN | 13V |
| C31P to C31M | 17V |
| VRP to VSS | 18V |

*Without EEPROM, E_DO pin has to connected to VDD3

## External Power Mode